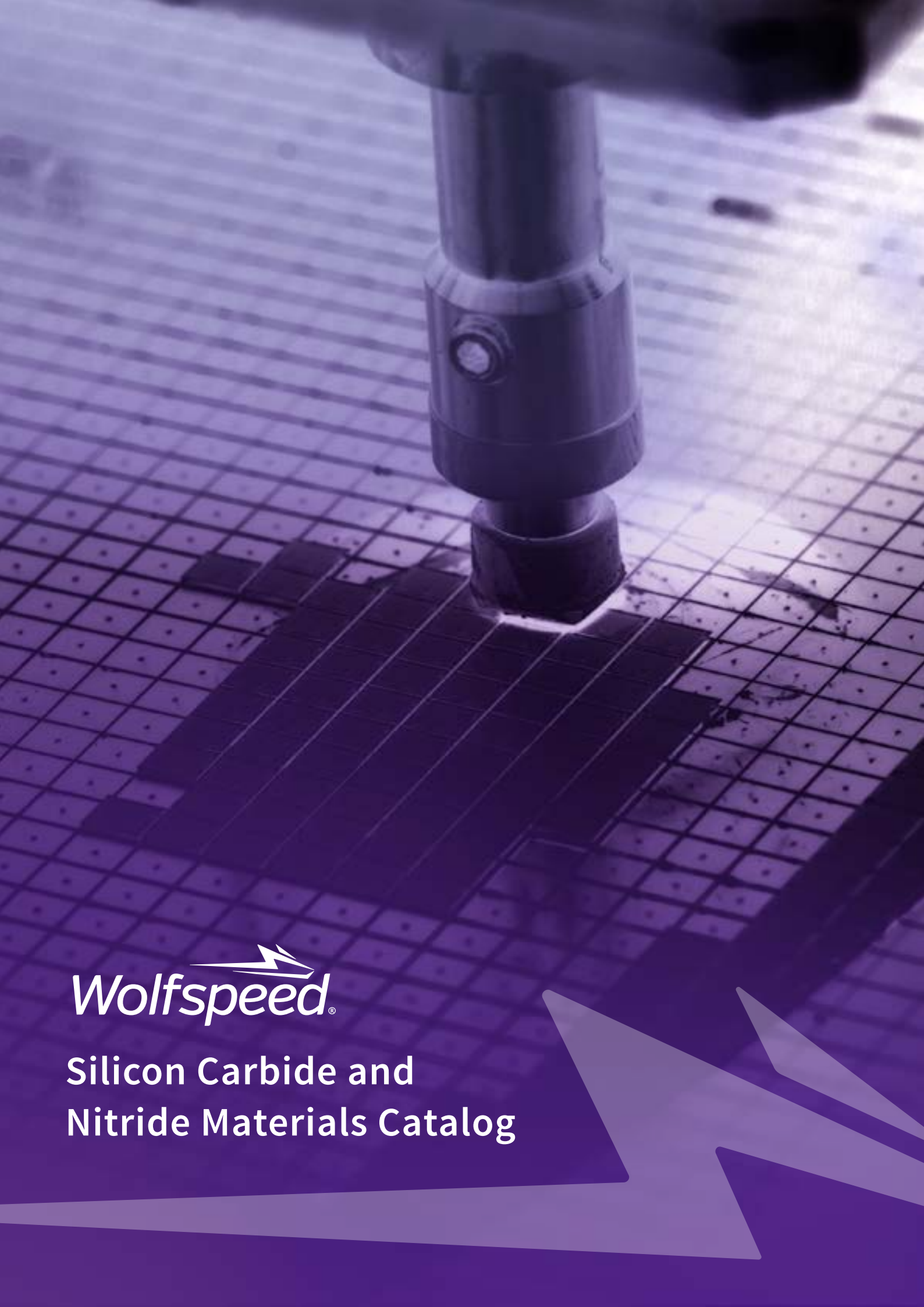


Wolfspeed®

# Silicon Carbide and Nitride Materials Catalog

# WOLFSPEED MATERIALS

## Industry-Leading Portfolio, Innovation and Scale

Wolfspeed is a fully integrated materials supplier with the largest and most diverse product portfolio serving our global customer base with a broad range of applications. We are the technology commercialization leader with the capacity and scale to bring large diameter wafers and high-quality epitaxy to the market in mass production volumes.

Wolfspeed has long-proven expertise in SiC and GaN materials technology advancement with the focus and commitment to bring high-quality solution platforms across all applications.

**n-TYPE**
SiC Substrates

**HPSI**
High Purity Semi-Insulating SiC Substrates

**SiC EPITAXY**
n-type and p-type Epitaxial Layers

**NITRIDE EPITAXY**
GaN, AlGaN, AlInN Epitaxial Layers

### APPLICATIONS

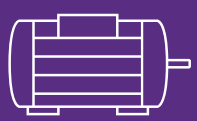
SiC and GaN materials enable faster, smaller, lighter and more powerful electronic systems. Wolfspeed is committed to providing our customers with the materials needed to facilitate the rapid expansion and adoption of the technology within the industry.

Our materials enable devices that power Renewable Energy, Base Stations & Telecom, Traction, Industrial Motor Control, Automotive applications and Aerospace and Defense.

RENEWABLE ENERGY

BASE STATIONS TELECOM

TRACTION



INDUSTRIAL MOTOR CONTROL

AUTOMOTIVE

AEROSPACE AND DEFENSE

## PHYSICAL PROPERTIES

| | |
|---|---|
| Polytype | Single-Crystal 4H |
| Supported diameters | 100 mm & 150 mm |
| Crystal structure | Hexagonal |
| Bandgap | 3.26 eV |
| Thermal conductivity (n-type; 0.020 Ω*cm) | a~4.2 W/cm • K @ 298 K |
| | c~3.7 W/cm • K @ 298 K |
| Thermal conductivity (HPSI) | a~4.9 W/cm • K @ 298 K |
| | c~3.9 W/cm • K @ 298 K |
| Lattice parameters | a=3.073 Å |
| | c=10.053 Å |
| Mohs hardness | 9 |

## DIMENSIONAL PROPERTIES, TERMINOLOGY, AND METHODS*

**DIAMETER**

The linear dimension across the surface of a wafer. Measurement is performed using an automated optical micrometer, traceable to the ANSI standard, providing the average value for each individual wafer.

**THICKNESS, CENTER POINT**

Measured with ANSI-certified non-contact tools at the center of each individual wafer.

**SURFACE ORIENTATION**

Denotes the orientation of the surface of a wafer with respect to a crystallographic plane within the lattice structure. In wafers cut intentionally "off orientation," the direction of cut is parallel to the primary flat, away from the secondary flat. Measured with x-ray goniometer on a sample of one wafer per boule in the center of the wafer.

**ORTHOGONAL MISORIENTATION**

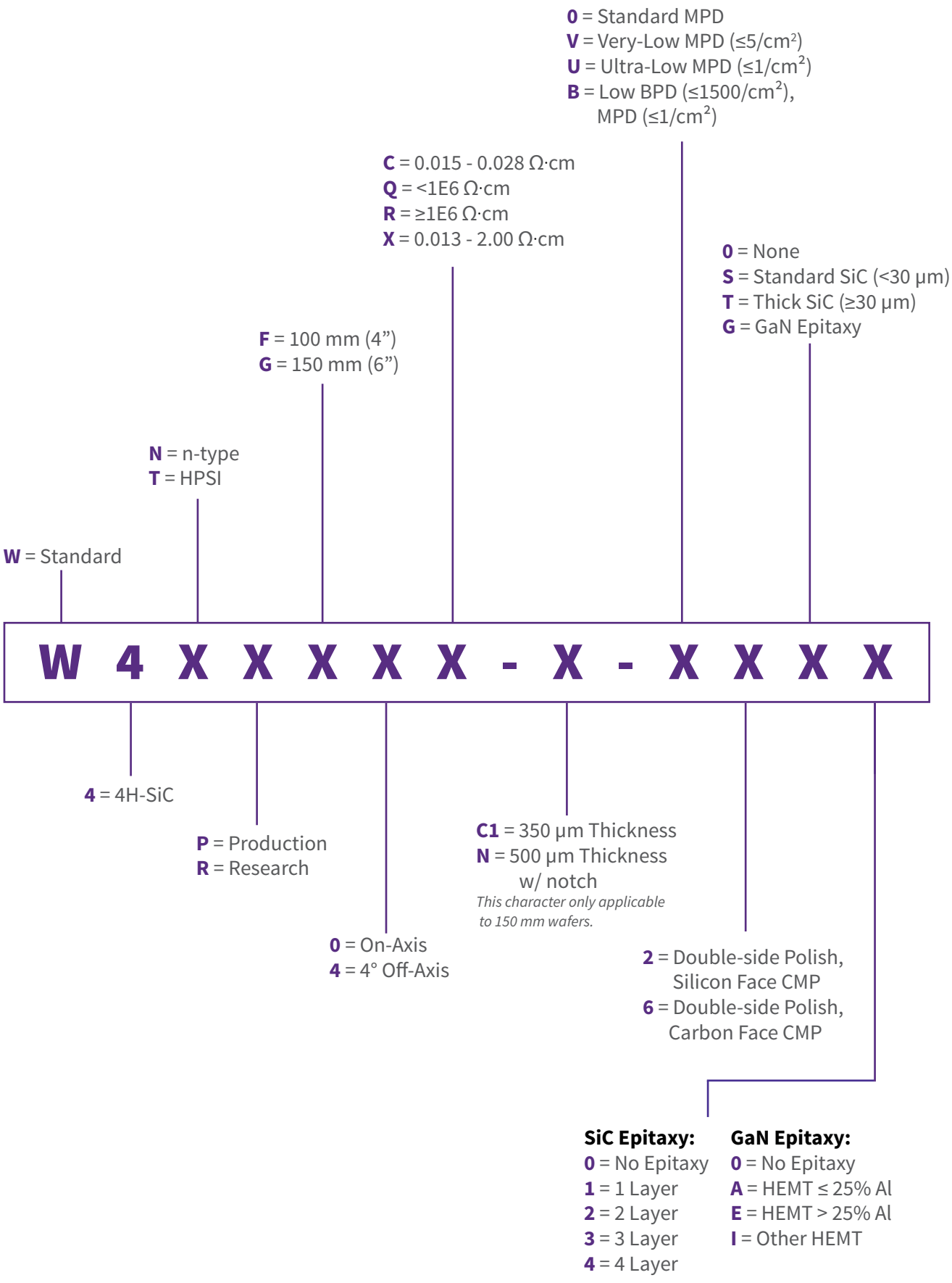
In wafers intentionally cut "off orientation," the angle between the projection of the surface normal onto a (0001) plane and the nearest [11$\bar{2}$0] direction.

**WAFER SCRIBE**

Wolfspeed is transitioning to a new wafer scribe format based upon SEMI specification M12-0706. This conversion, which is projected to be fully integrated in 2022, brings several improvements. The M12-based scribe will be positioned upright when the major flat or notch is oriented up, making the scribe easier to read when the wafers are loaded into cassettes. The new format includes a wafer supplier identification code, validating the wafer's authenticity. It also includes a checksum, which is an error-detection method that prevents OCR mis-read errors and reduces the instance of processing errors associated with such events.


***Notes:*** ** Please reference SEMI M55.*

# HOW TO ORDER


**0** = Standard MPD
**V** = Very-Low MPD (≤5/cm²)
**U** = Ultra-Low MPD (≤1/cm²)
**B** = Low BPD (≤1500/cm²), MPD (≤1/cm²)
**C** = 0.015 - 0.028 Ω·cm
**Q** = <1E6 Ω·cm
**R** = ≥1E6 Ω·cm
**X** = 0.013 - 2.00 Ω·cm
**0** = None
**S** = Standard SiC (<30 µm)
**T** = Thick SiC (≥30 µm)
**G** = GaN Epitaxy
**F** = 100 mm (4")
**G** = 150 mm (6")
**N** = n-type
**T** = HPSI
**W** = Standard
W 4 X X X X X - X - X X X X
**4** = 4H-SiC
**P** = Production
**R** = Research
**0** = On-Axis
**4** = 4° Off-Axis
**C1** = 350 µm Thickness
**N** = 500 µm Thickness w/ notch
*This character only applicable to 150 mm wafers.*
**2** = Double-side Polish, Silicon Face CMP
**6** = Double-side Polish, Carbon Face CMP
**SiC Epitaxy:**
**0** = No Epitaxy
**1** = 1 Layer
**2** = 2 Layer
**3** = 3 Layer
**4** = 4 Layer
**GaN Epitaxy:**
**0** = No Epitaxy
**A** = HEMT ≤ 25% Al
**E** = HEMT > 25% Al
**I** = Other HEMT

# Our Products

# N-TYPE SiC SUBSTRATE

## PRODUCT DESCRIPTIONS

The Materials Business Unit produces a wide assortment of n-type conductive SiC products ranging in wafer diameters up to 150 mm. Wolfspeed's industry-leading, high-volume platform process provides our customers with the highest degree of material quality, supply assurance and economies of scale.

| Part Number | Description |
|---|---|
| W4NRF4C-V200 | 4H-SiC, n-type, Research Grade, 100 mm, 4° Off-Axis, 0.015-0.028 Ω·cm, Very Low MPD ≤5/cm$^2$, 350 µm Thick w/ 32.5 mm Flat, Double-Sided Polish Silicon Face CMP Epi Ready, Bare Substrate |
| W4NPF4C-V200 | 4H-SiC, n-type, Production Grade, 100 mm, 4° Off-Axis, 0.015-0.028 Ω·cm, Very Low MPD ≤5/cm$^2$, 350 µm Thick w/ 32.5 mm Flat, Double-Sided Polish Silicon Face CMP Epi Ready, Bare Substrate |
| W4NRF4C-U200 | 4H-SiC, n-type, Research Grade, 100 mm, 4° Off-Axis, 0.015-0.028 Ω·cm, Ultra Low MPD ≤1/cm$^2$, 350 µm Thick w/ 32.5 mm Flat, Double-Sided Polish Silicon Face CMP Epi Ready, Bare Substrate |
| W4NPF4C-U200 | 4H-SiC, n-type, Production Grade, 100 mm, 4° Off-Axis, 0.015-0.028 Ω·cm, Ultra Low MPD ≤1/cm$^2$, 350 µm Thick, w/ 32.5 mm Flat Double-Sided Polish Silicon Face CMP Epi Ready, Bare Substrate |
| W4NPF4C-B200 | 4H-SiC, n-type, Production Grade, 100 mm, 4° Off-Axis, 0.015-0.028 Ω·cm, Ultra Low MPD ≤1/cm$^2$, Low BPD ≤1500/cm$^2$, 350 µm Thick w/ 32.5 mm Flat, Double-Sided Polish Silicon Face CMP Epi Ready, Bare Substrate |
| W4NRG4C-C1-V200 | 4H-SiC, n-type, Research Grade, 150 mm, 4° Off-Axis, 0.015-0.028 Ω·cm, Very Low MPD ≤5/cm$^2$, 350 µm Thick w/ 47.5 mm Flat, Double-Sided Polish Silicon Face CMP Epi Ready, Bare Substrate |
| W4NPG4C-C1-V200 | 4H-SiC, n-type, Production Grade, 150 mm, 4° Off-Axis, 0.015-0.028 Ω·cm, Very Low MPD ≤5/cm$^2$, 350 µm Thick w/ 47.5 mm Flat, Double-Sided Polish Silicon Face CMP Epi Ready, Bare Substrate |
| W4NRG4C-C1-U200 | 4H-SiC, n-type, Research Grade, 150 mm, 4° Off-Axis, 0.015-0.028 Ω·cm, Ultra Low MPD ≤1/cm$^2$, 350 µm Thick w/ 47.5 mm Flat, Double-Sided Polish Silicon Face CMP Epi Ready, Bare Substrate |
| W4NPG4C-C1-U200 | 4H-SiC, n-type, Production Grade, 150 mm, 4° Off-Axis, 0.015-0.028 Ω·cm, Ultra Low MPD ≤1/cm$^2$, 350 µm Thick w/ 47.5 mm Flat, Double-Sided Polish Silicon Face CMP Epi Ready, Bare Substrate |
| W4NPG4C-C1-B200 | 4H-SiC, n-type, Production Grade, 150 mm, 4° Off-Axis, 0.015-0.028 Ω·cm, Ultra Low MPD ≤1/cm$^2$, Low BPD ≤1500/cm$^2$, 350 µm Thick w/ 47.5 mm Flat, Double-Sided Polish Silicon Face CMP Epi Ready, Bare Substrate |

**FLAT LENGTH**

Linear dimension of the flat measured with automated optical micrometer on a sample of one wafer per boule (see Figure 1).

**PRIMARY FLAT**

The flat of the longest length on the wafer, oriented such that the chord is parallel with a specified low-index crystal plane.

**PRIMARY FLAT ORIENTATION**

The primary flat is the $(1\bar{1}00)$ plane with the flat face parallel to the $[11\bar{2}0]$ direction. Measured with XRD back reflection technique.

**SECONDARY FLAT**

A flat of shorter length than the primary flat, whose position with respect to the primary flat identifies the face of the wafer. Not applicable to 150 mm wafers.

**SECONDARY FLAT ORIENTATION**

The secondary flat is 90˚ clockwise from the primary flat, ±5˚, referencing the silicon face up.

**MARKING**

For silicon face polished material, the carbon face of each individual wafer is laser-marked with OCR-compatible font, similar to definitions and characteristics in SEMI M12. The laser markings are offset right when looking at the carbon face with the primary flat oriented down (see Figure 1 and 2). For carbon face polished material, the silicon face of each individual wafer is laser-marked.

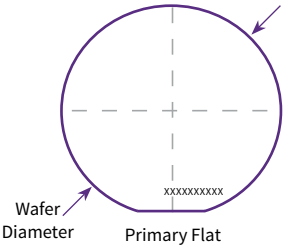



**Figure 1.** Diameter, primary flat location and marking orientation, carbon face up for silicon face polished 150 mm wafers

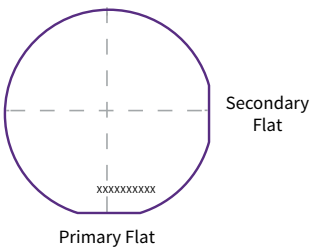



**Figure 2.** Primary flat location and marking orientation, carbon face up for silicon face polished 100 mm wafers

## PRODUCT SPECIFICATIONS

| 100 mm Diameter n-type Substrates | |
|---|---|
| Diameter | 100.0 mm +0.0/-0.5 mm |
| Thickness | 350.0 µm ± 25.0 µm |
| Dopant | Nitrogen |
| Primary flat length | 32.5 mm ± 2.0 mm |
| Secondary flat length | 18.0 mm ± 2.0 mm |
| Surface orientation | 4.0˚ toward [11$\bar{2}$0] ± 0.5˚ |
| Surface finish | Back face optical polish, epi-face CMP |
| Orthogonal misorientation | ± 5.0˚ |
| Primary flat orientation | [11$\bar{2}$0] ± 5.0˚ |
| Secondary flat orientation | 90.0˚ CW from primary ± 5.0˚, silicon face up |
| TTV | ≤15 µm |
| Warp | ≤45 µm |
| LTV (average, 1 cm² site) | ≤4 µm |
| Edge chips by diffuse lighting | |
| Production-grade | None permitted ≥0.5 mm width and depth |
| Research-grade | Maximum 2 ≤1.0 mm width & depth |

| 150 mm Diameter n-type Substrates | |
|---|---|
| Diameter | 150.0 mm ± 0.25 mm |
| Thickness | 350 µm ± 25 µm |
| Dopant | Nitrogen |
| Primary flat length | 47.5 mm ± 1.5 mm |
| Secondary flat length | None |
| Surface orientation | 4.0˚ toward [11$\bar{2}$0] ± 0.5˚ |
| Surface finish | Back face optical polish, epi-face CMP |
| Orthogonal misorientation | ± 5.0˚ |
| Primary flat orientation | [11$\bar{2}$0] ± 5˚ |
| Secondary flat orientation | N/A |
| TTV | ≤10 µm |
| Warp | ≤40 µm |
| SFQR (max, 1 cm² site) | ≤5 µm |
| LTV (average, 1 cm² site) | |
| Production-grade | ≤2 µm |
| Research-grade | ≤4 µm |
| Edge chips by diffuse lighting | |
| Production-grade | None permitted ≥0.5 mm width and depth |
| Research-grade | Maximum 2 ≤1.0 mm width & depth |

# HIGH PURITY SEMI-INSULATING SiC SUBSTRATE

## PRODUCT DESCRIPTIONS

The Materials Business Unit produces a wide assortment of semi-insulating SiC products ranging in wafer diameters up to 150 mm. Wolfspeed's High Purity Semi-Insulating wafers are not vanadium-doped.

| Part Number | Description |
|---|---|
| W4TRF0R-0200 | 4H-SiC, HPSI, Research Grade, 100 mm, On-Axis, ≥1E6 Ω·cm, Standard MPD, 500 µm Thick w/ 32.5 mm Flat, Double-Sided Polish Silicon Face CMP Epi Ready, Bare Substrate |
| W4TPF0R-0200 | 4H-SiC, HPSI, Production Grade, 100 mm, On-Axis, ≥1E6 Ω·cm, Standard MPD, 500 µm Thick w/ 32.5 mm Flat, Double-Sided Polish Silicon Face CMP Epi Ready, Bare Substrate |
| W4TRG0R-N-0200 | 4H-SiC, HPSI, Research Grade, 150 mm, On-Axis, ≥1E6 Ω·cm, Standard MPD, 500 µm Thick w/ Notch, Double-Sided Polish Silicon Face CMP Epi Ready, Bare Substrate |
| W4TPG0R-N-0200 | 4H-SiC, HPSI, Production Grade, 150 mm, On-Axis, ≥1E6 Ω·cm, Standard MPD, 500 µm Thick w/ Notch, Double-Sided Polish Silicon Face CMP Epi Ready, Bare Substrate |

**FLAT LENGTH** — Linear dimension of the flat measured with automated optical micrometer on a sample of one wafer per boule (see Figure 1).

**PRIMARY FLAT** — The flat of the longest length on the wafer, oriented such that the chord is parallel with a specified low-index crystal plane. Not applicable to 150 mm wafers.

**PRIMARY FLAT ORIENTATION** — The primary flat is the $(1\bar{1}00)$ plane with the flat face parallel to the $[11\bar{2}0]$ direction. Measured with XRD back reflection technique.

**SECONDARY FLAT** — A flat of shorter length than the primary flat, whose position with respect to the primary flat identifies the face of the wafer. Not applicable to 150 mm wafers.

**SECONDARY FLAT ORIENTATION** — The secondary flat is 90˚ clockwise from the primary flat, ±5˚, referencing the silicon face up.

**MARKING** — For silicon face polished material, the carbon face of each individual wafer is laser-marked with OCR-compatible font, similar to definitions and characteristics in SEMI M12. The laser markings are offset right when looking at the carbon face with the primary flat oriented down (see Figure 1).

**150 MM HPSI MARKING AND NOTCH:** — All 150 mm HPSI products have a notch with 1.0 mm (+0.25, -0.00) depth. A line drawn from the wafer center to the notch is parallel to the $[1\bar{1}00] \pm 5.0^{\circ}$ direction. The laser markings are offset right when looking at the carbon face with the notch oriented down (see Figure 2).

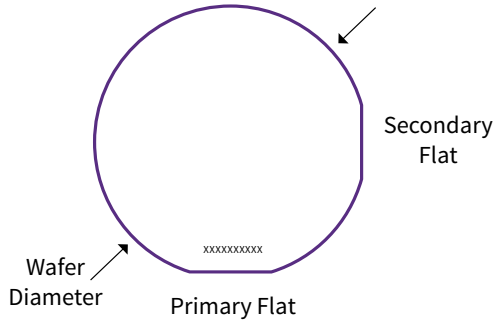



**Figure 1.** Diameter, primary and secondary flat locations and marking orientation, carbon face up for silicon face polished 100 mm HPSI wafers

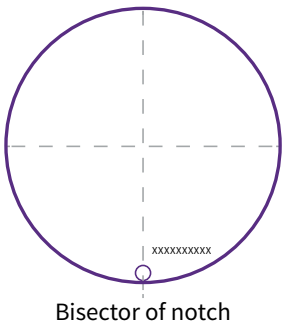



**Figure 2.** Notch location and marking orientation, carbon face up for face polished 150 mm HPSI wafers

## PRODUCT SPECIFICATIONS

| 100 mm Diameter Semi-Insulating Substrates | |
|---|---|
| Diameter | 100.0 mm +0.0/-0.5 mm |
| Thickness | 500.0 µm ± 25.0 µm |
| Primary flat length | 32.5 mm ± 2.0 mm |
| Secondary flat length | 18.0 mm ± 2.0 mm |
| Surface orientation | (0001) ± 0.25˚ |
| Surface finish | Back face optical polish, epi-face CMP |
| Primary flat orientation | [11$\bar{2}$0] ± 5.0˚ |
| Secondary flat orientation | 90.0˚ CW from primary ± 5.0˚, silicon face up |
| Resistivity | ≥1E6 Ω·cm |
| TTV | ≤10 µm |
| Warp | ≤35 µm |
| LTV (average, 1 $cm^2$ site) | ≤2 µm |
| Edge chips by diffuse lighting | |
| Production-grade | None permitted ≥0.5 mm width and depth |
| Research-grade | Maximum 2 ≤1.0 mm width & depth |

| 150 mm Diameter Semi-Insulating Substrates | |
|---|---|
| Diameter | 150.0 mm ± 0.25 mm |
| Thickness | 500 µm ± 25 µm |
| Notch depth | 1.0 mm +0.25 mm, -0.00 mm |
| Notch orientation | [1$\bar{1}$00] ± 5.0˚ |
| Surface orientation | (0001) ± 0.25˚ |
| Surface finish | Back face optical polish, epi-face CMP |
| Resistivity | ≥1E6 Ω·cm |
| TTV | ≤10 µm |
| Warp | ≤40 µm |
| LTV (average, 1 $cm^2$ site) | ≤3 µm |
| Edge chips by diffuse lighting | |
| Production-grade | None permitted ≥0.5 mm width and depth |
| Research-grade | Maximum 2 ≤1.0 mm width & depth |

# SiC SUBSTRATE

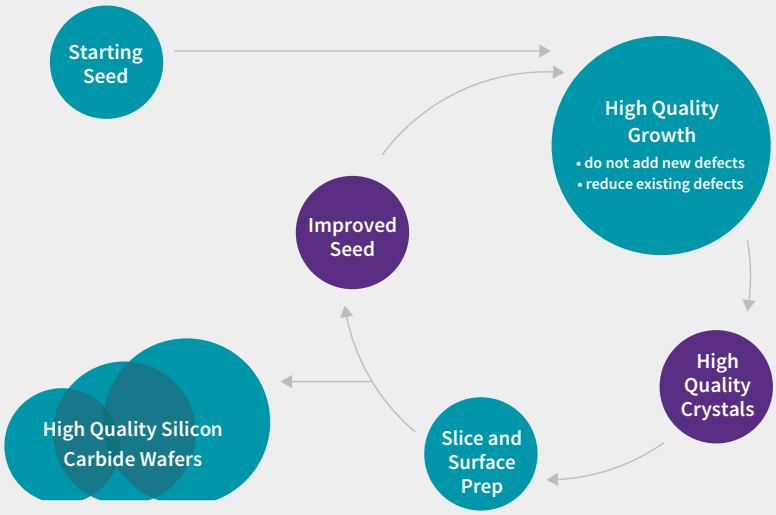
## SURFACE FINISH SPECIFICATIONS

| Attribute | Production-Grade | Research-Grade |
|---|---|---|
| Edge chips/indents by high intensity light | None permitted ≥0.5 mm width and depth | Maximum 2 ≤1.0 mm width & depth |
| Total usable area* Quantitative by automated optical surface inspection and 2mmx2mm site map | ≥90% area | ≥70% area |
| Striations by high intensity light | None permitted | 3 allowed ≤3 mm each |
| Polytype areas by UV illumination | ≤5% area | ≤5% area |
| Area contamination (stains) by high intensity light | None permitted | None permitted |
| Cracks by high-intensity light | None permitted | None permitted |
| Hex plates by high-intensity light* | None permitted | None permitted |
| Scratch length by automated optical surface inspection* | Cumulative ≤150 mm | Cumulative ≤150 mm |

***Notes:*** **3 mm edge exclusion for 100 and 150 mm substrates.*

## THE WOLFSPEED ADVANTAGE

Wolfspeed's proprietary crystal growth process is based upon a seeded-sublimation method and therefore requires careful control and incremental development of high-quality seeds. Wolfspeed's focus on high-quality growth conditions that avoid introducing new defects, while reducing existing defects, results in generational improvements in both boule and seed quality. Combine that with 30+ years of manufacturing experience and unmatched crystal growth capacity, and it is clear that Wolfspeed Materials has more cycles of learning and more generational improvements than any other manufacturer in the industry. As such, Wolfspeed Materials has significantly reduced most forms of crystalline defects, and practically eliminated some defects such as bar stacking faults and hex plates.



## SURFACE FINISH DESCRIPTIONS

| | |
|---|---|
| **(AREA) CONTAMINATION** | Any foreign matter on the surface in localized areas which is revealed under high-intensity (or diffuse) illumination as discolored, mottled, or cloudy appearance resulting from smudges, stains or water spots. |
| **CRACKS** | A fracture or cleavage of the wafer that extends from the front-side surface of the wafer to the back-side surface of the wafer. Cracks must exceed 0.25 mm in length under high-intensity illumination in order to discriminate fracture lines from crystalline striations. Fracture lines typically exhibit sharp, thin lines of propagation, which discriminate them from material striations. |
| **EDGE CHIPS** | Any edge anomalies in excess of dimensions defined in the table on page 9. As viewed under high intensity illumination, edge chips are determined as unintentionally missing material from the edge of the wafer. |
| **EDGE EXCLUSION** | The outer annulus of the wafer is designated as wafer handling area and is excluded from surface finish criteria. This annulus is 3 mm for 100 mm and 150 mm substrates. |
| **HEX PLATE** | Hexagonal-shaped platelets on the surface of the wafer which appear silver in color to the unaided eye, under high intensity light. |
| **FOREIGN POLYTYPES** (also referred to as "Inclusions" or "Crystallites") | Regions of the wafer crystallography which are polycrystalline or of a different polytype material than the remainder of the wafer, such as 6H mixed in with a 4H type substrate. Foreign polytype regions may exhibit color changes or distinct boundary lines, and are judged in terms of area percent under UV illumination. |
| **SCRATCHES** | A scratch is defined as a singular cut or groove into the front-side wafer surface with a length-to-width ratio of greater than 5 to 1, and detected and classified by Lasertec SICA. |
| **STRIATIONS** | Striations in silicon carbide are defined as linear crystallographic defects extending down from the surface of the wafer which may or may not pass through the entire thickness of the wafer, and generally follow crystallographic planes over its length. |
| **TOTAL USABLE AREA** | A cumulative subtraction of all noted defect areas from the front-side wafer quality area beyond the edge exclusion zone, with regard to a defined grid. The remaining percent value indicates the proportion of the front-side surface to be free of all noted defects, as measured by Lasertec SICA or Candela (does not include edge exclusion). |

# SiC EPITAXY

## PRODUCT DESCRIPTIONS

Wolfspeed produces n-type and p-type SiC epitaxial layers on SiC substrates, and has the widest range of available layer thickness from sub-micron to >200 µm. Unless noted otherwise on the product quotation, the epitaxial layer structure will meet or exceed the following specifications. Additional comments, terms and conditions may be found in the specification document.

| Product Description | | |
|---|---|---|
| **Conductivity** | **n-type** | **p-type** |
| Dopant | Nitrogen | Aluminum |
| Net doping density | $N_D$-$N_A$ | $N_A$-$N_D$ |
| Silicon face | 5E14 – 1E19/cm$^3$ | 5E14 – 1E20/cm$^3$ |
| Carbon face | 1E16 – 1E19/cm$^3$ | Not available |
| Tolerance | ±20% | ±50% |
| Thickness range – Silicon face | | |
| 0.2–200 microns | ±8% of selected thickness | ±10% of selected thickness |
| Thickness range – Carbon face | | |
| 0.2–1.0 microns | ±25% of selected thickness | Not available |
| 1.0–10.0 microns | ±15% of selected thickness | Not available |

## PRODUCT SPECIFICATIONS

| Characteristics | Maximum Acceptability Limits | | Test Methods | Defect Definitions (See pg. 11) | Methodology (See pg. 11) |
|---|---|---|---|---|---|
| Large-point defects | 100 mm wafer | 20 | Diffuse Illumination | D1 | M1, M2 |
| | 150 mm wafer | 25 | | | |
| Scratches | cumulative scratch length ≤150 mm | | | D2 | |
| Backside cleanliness | 95% clean | | | D3 | |
| Edge chips | See Substrate Specifications | | | D4 | M2 |
| Epi defects* | <3/cm$^2$ | | Candela CS20 / Lasertec SICA | D5-D6 | M3 |
| Net doping | See Product Description table | | CV | - | M4 |
| Thickness | See Product Description table | | FTIR | - | M5 |

***Note: 3 mm edge exclusion for 100 and 150 mm, <70 µm thickness***

# SiC EPIWAFER

## DEFINITIONS

### D1. LARGE-POINT DEFECTS
Defects which exhibit a clear shape to the unassisted eye and are > 50 microns across. These features include downfall, triangles, silicon droplets, and pits. Large point defects less than 3 mm apart count as one defect.

### D2. SCRATCHES
A scratch is defined as a singular cut or groove into the front-side wafer surface with a length-to-width ratio of greater than 5 to 1, and detected by diffuse illumination with the unaided eye.

### D3. BACKSIDE CLEANLINESS
Verified by inspecting for contamination on the wafer backside using diffuse illumination and the unaided eye. Backside cleanliness specified as percent area clean.

### D4. EDGE CHIPS
As viewed under diffuse illumination, edge chips are determined as unintentionally missing material from the edge of the wafer.

### D5. EPITAXY DEFECTS
The sum of discrete defect counts. These include triangles, downfall, carrots, particles, and silicon droplets.

### D6. AUTOMATED DEFECT CLASSIFICATION & ACCURACY
Defect maps are provided only as representations of wafer quality. Defect classification, location, and count will not be absolutely accurate.

## METHODOLOGY

M1. 3 mm edge exclusion for 100 and 150 mm.

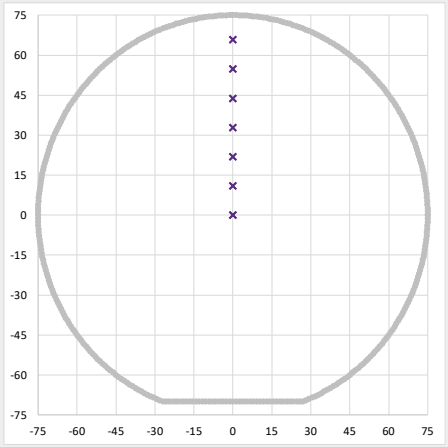
M2. Inspection performed under diffuse illumination.

M3. Automated optical inspection.

M4. Net doping is determined as an average value of multiple points along radius opposite major flat using CV profiling. Rotational symmetry preserved.

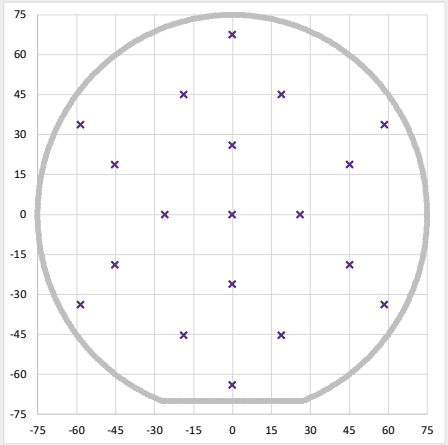
M5. Thickness is determined as an average value across the wafer using FTIR, or mass difference for layers <5 µm.

## CV MEASUREMENT POINTS (EPI DOPING)*:




| Pt. | x_mm | y_mm |
|---|---|---|
| 1 | 0 | 0 |
| 2 | 0 | 10.95 |
| 3 | 0 | 21.90 |
| 4 | 0 | 32.85 |
| 5 | 0 | 43.80 |
| 6 | 0 | 54.75 |
| 7 | 0 | 65.70 |

## FTIR POINTS (EPI THICKNESS)*:




| Pt. | x_mm | y_mm |
|---|---|---|
| 1 | 0.00 | 67.50 |
| 2 | -58.45 | 33.76 |
| 3 | -45.22 | 18.74 |
| 4 | -18.74 | 45.22 |
| 5 | 0.00 | 26.07 |
| 6 | 18.74 | 45.22 |
| 7 | 45.22 | 18.80 |
| 8 | 58.45 | 33.75 |
| 9 | 45.22 | -18.74 |
| 10 | 26.04 | 0.00 |

| Pt. | x_mm | y_mm |
|---|---|---|
| 11 | 0.00 | 0.00 |
| 12 | 0.00 | -26.04 |
| 13 | -26.04 | 0.00 |
| 14 | -45.22 | -18.74 |
| 15 | -58.46 | -33.75 |
| 16 | -18.74 | -45.22 |
| 17 | 18.74 | -45.22 |
| 18 | 58.45 | -33.76 |
| 19 | 0.00 | -64.00 |

***Notes:*** ** Values listed in tables are for 150 mm wafers. Both patterns scale for 100 mm wafers.*

# NITRIDE EPITAXY

## PRODUCT DESCRIPTIONS

Wolfspeed produces GaN, $Al_xGa_{1-x}N$ and $Al_{1-y}In_yN$ epitaxial layers on SiC substrates. Unless noted otherwise on the product quotation, the epitaxial layer structure will meet or exceed the following specifications (1). Contact Wolfspeed Materials Sales for specification on custom epitaxy requests. Additional comments, terms and conditions may be found in the specification document.

## STRUCTURAL LAYER SPECIFICATIONS

**Nitride Epitaxial Layer Specifications**

| Property | Value or Range | Precision | Measurement Technique |
|---|---|---|---|
| Substrate | On-axis SiC (Semi-Insulating) | - | - |
| Composition (2) | $Al_xGa_{1-x}N$ or $Al_{1-y}In_yN$ | $\Delta x = \pm 0.015$<br>$\Delta y = \pm 0.02$ | XRD peak splitting |
| | $0 \le x \le 0.3$, $0 \le y \le 0.2$, certain restrictions apply | | |
| Thickness (3) | 1.0 µm to 3.0 µm GaN | Average thickness within ± 15% of target thickness and uniformity <10%. (4) | X-ray or white light interferometry |
| | 0.5 nm to 1.0 µm AlN | | |
| | 1.0 nm to 1.0 µm $Al_xGa_{1-x}N$ | | |
| | 1.0 nm to 1.0 µm $Al_{1-y}In_yN$ | | |
| | 2.0 nm to 5.0 nm GaN (Cap Layer) | | |
| | 5.0 nm to 100 nm SiN (Cap Layer) | | |
| GaN Crystallinity | < 250 arcsec (3 µm layer on SiC substrate) | - | XRD (0006) FWHM (center point) |
| $Al_{0.25}Ga_{0.75}N$ | < 500 arcsec (3 µm layer on SiC substrate) | - | XRD (0006) FWHM (center point) (5) |
| Visible Defects | < 50/cm² | - | Differential interference microscopy at 50x in cross pattern with 5 mm edge exclusion |

## ELECTRICAL LAYER SPECIFICATIONS

| Nitride Epitaxial Layer Specifications | | | |
|---|---|---|---|
| **Property** | **Value or Range** | **Precision** | **Measurement Technique** |
| Dopant type | n-type (Si)<br>HEMT buffer (Fe and/or C) | - | - |
| Carrier concentration (unintentionally doped) | < 1E16/cm$^3$, n-type | - | CV |
| Carrier concentration (n-type, Si doped) | 1E16 to 2E19/cm$^3$ | ± 50% | CV (wafer center, room temperature) |
| Carrier concentration of HEMT structure | >8E12/cm$^2$ (25 nm $Al_{0.25}Ga_{0.75}N$) | - | Contactless non-destructive carrier concentration |
| Mobility of HEMT structure | $\mu \geq 1500$ cm$^2$ V$^{-1}$ s$^{-1}$ (25 nm $Al_{0.25}Ga_{0.75}N$) | - | Contactless non-destructive mobility |
| Sheet Resisitivity | <2% uniformity | - | Contactless non-destructive sheet resisitivity |

1. Certain additional restrictions may apply and will be presented on the product quotation.
2. Quaternary compositions available upon special request.
3. Range given for undoped layers. Maximum achievable thickness for doped layers or heterostructures will be reduced.
4. Precision specification applies only to layers ≥ 0.01 µm thick. Uniformity = (100 x standard deviation / mean).
5. Please specify epitaxy structure details upon submission of RFQ (i.e. thickness, doping, composition).
6. Custom structures available. Contact Wolfspeed Materials Sales for more information on custom epitaxy requests.

www.wolfspeed.com/materials | materials_sales@wolfspeed.com



2021 - NC - V2