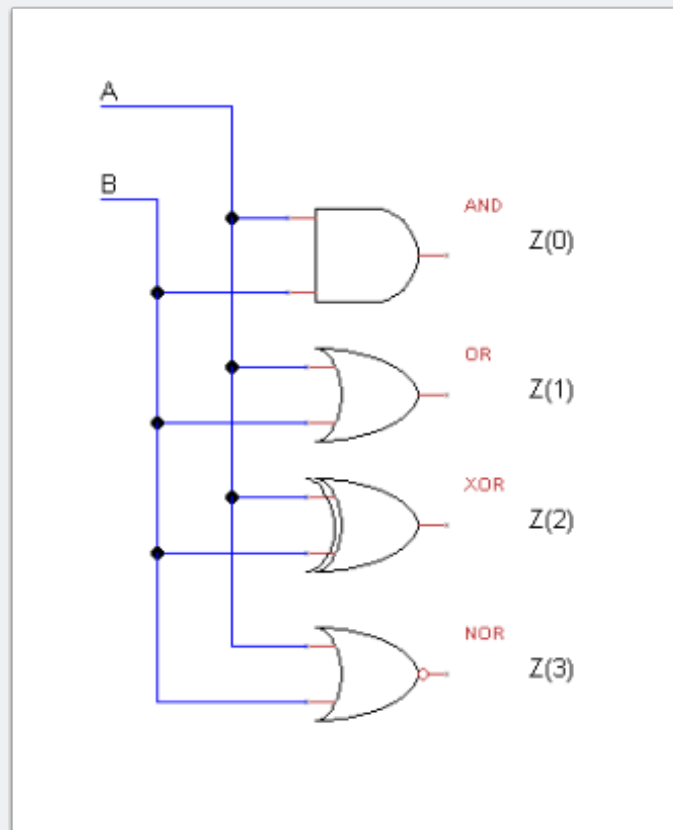


Simple VERILOG example using VIVADO 2015 with ZYBO FPGA board v 0.1

Aim

I am FPGA novice and want to try classical FPGA design tutorials. I bought perfect modern FPGA board ZYBO (**ZY**nq **BO**ard) based on Xilinx Z-7010 from Digilent but latest tools from Xilinx VIVADO 2015.2 more focused on AP SoC programming while I want to just pure FPGA design without any linuxes bootloaders etc. So I wrote this tutorial to help people like me :)

In this example we make simple scheme: 2 signals IN and 4 OUT.



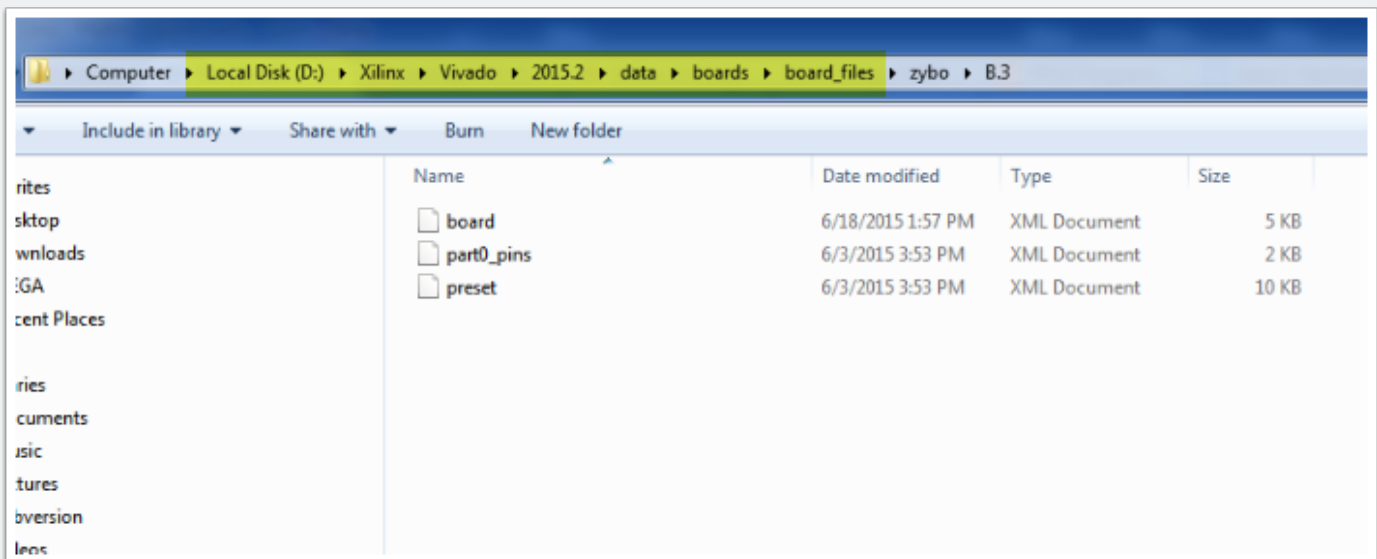
Simple VERILOG example using VIVADO 2015 with ZYBO FPGA board v 0.1

Preconditions: Adding Zybo Board to Vivado

Vivado 2015.2 under Windows 7 64 bit was used with 16 GB of RAM.

Before using Zybo with Vivado you should add Zybo Definitions File to Vivado.

1. Good source for Board Definition files is [Zynqbook website](#). Download [The_Zynq_Book_Tutorial_Sources_Aug15.zip](#)
2. Copy **zybo** folder with content from Archive path `\sources\zybo\setup\board_part` into `D:\Xilinx\Vivado\2015.2\data\boards\board_files` (if `D:\Xilinx\Vivado\2015.2` is my PC you probably have `C:\Xilinx` etc...)
3. In `board_files` you should see other boards so now our Zybo known by Vivado.
4. Download [ZYBO_Master.xdc from Digilent website](#) unpack constraints files on local hard disk for example on Desktop.



Simple VERILOG example using VIVADO 2015 with ZYBO FPGA board v 0.1

Phase 1. Preparation.

I have latest Vivado Design Edition from Xilinx which comes with Digilent Zybo board.

Launch your Vivado.



Simple VERILOG example using VIVADO 2015 with ZYBO FPGA board v 0.1

Create new project



Simple VERILOG example using VIVADO 2015 with ZYBO FPGA board v 0.1

New Project

Click Next

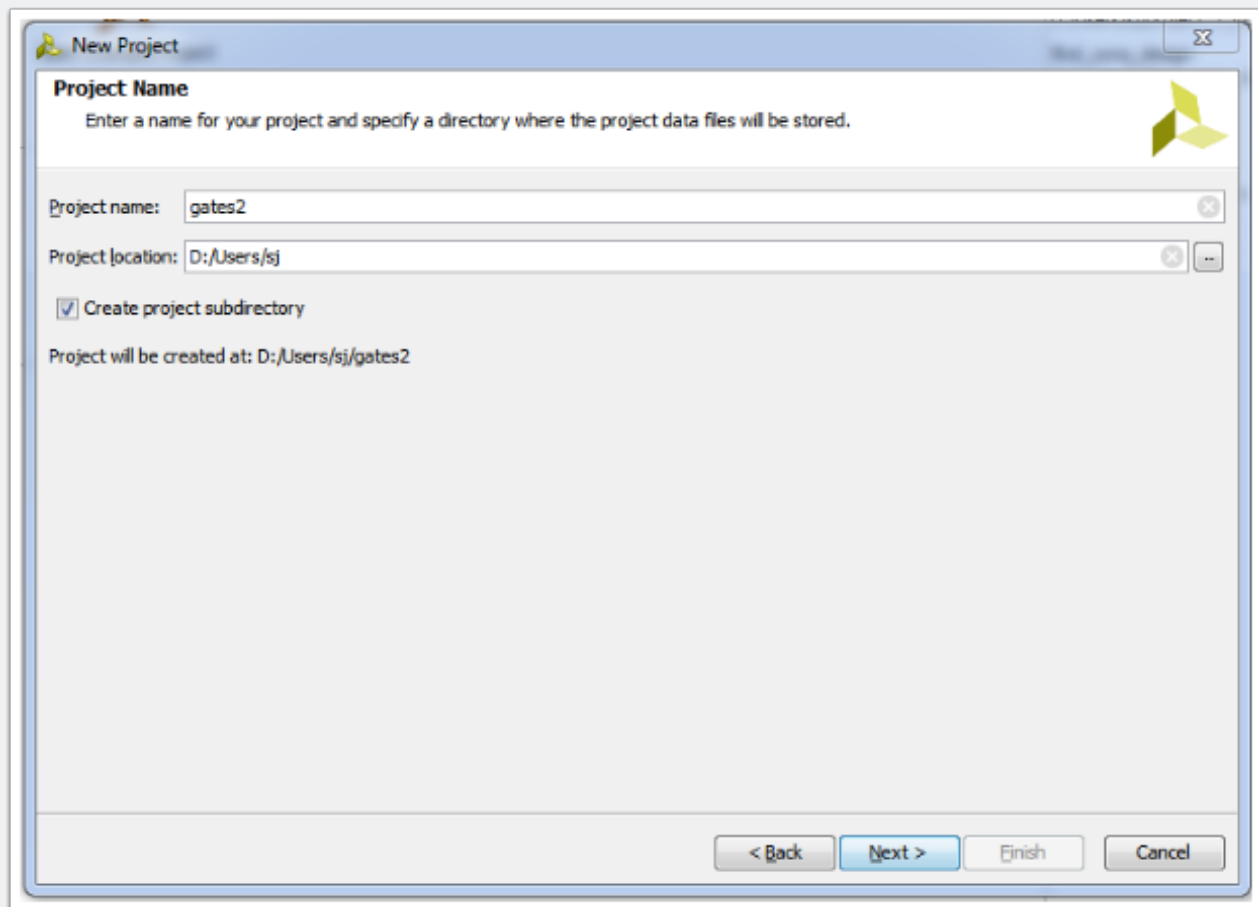


Simple VERILOG example using VIVADO 2015 with ZYBO FPGA board v 0.1

Set project name.

Set project name to **gates2**,

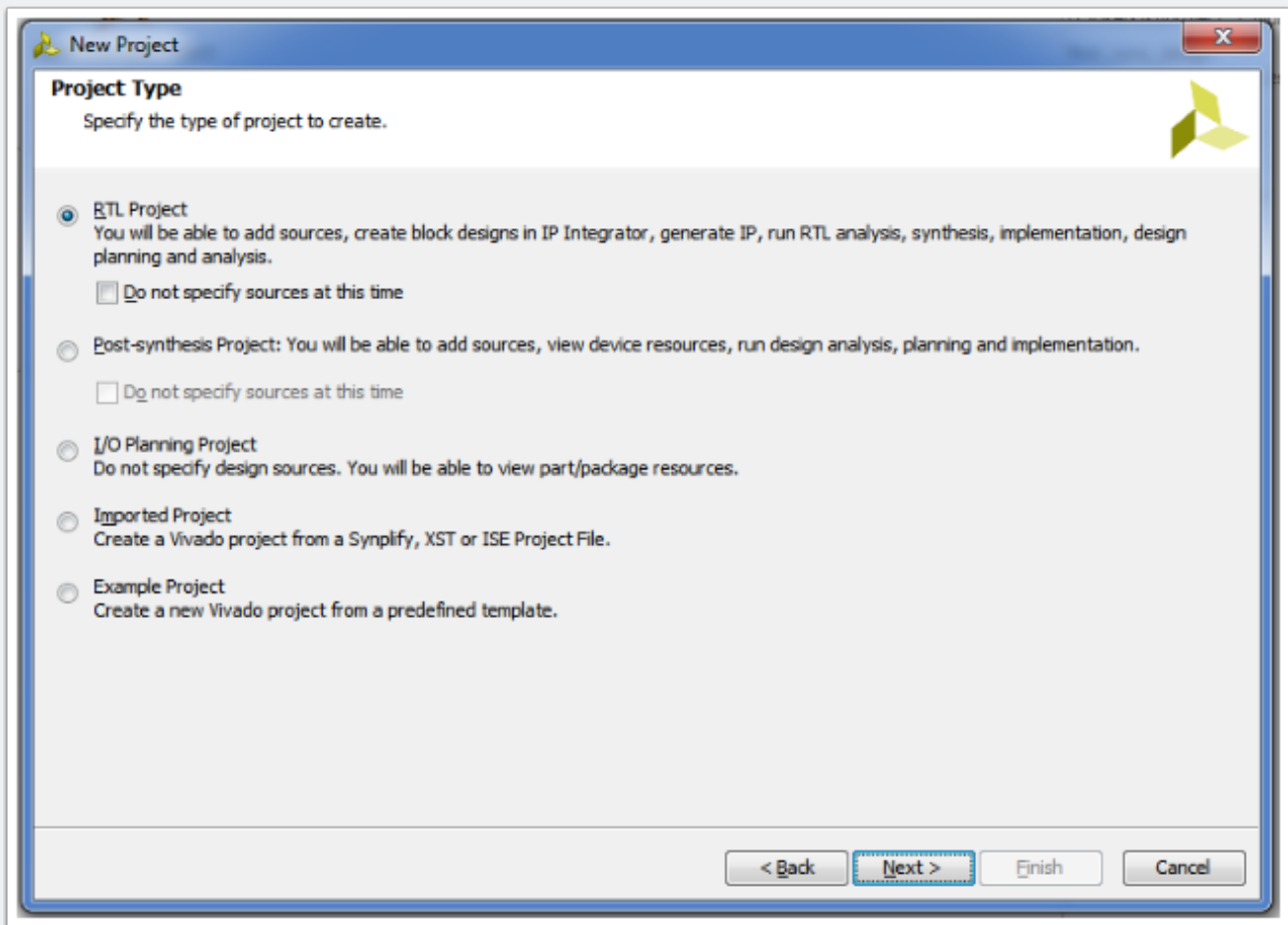
Keep rest settings unchanged unless you know what you doing.



Simple VERILOG example using VIVADO 2015 with ZYBO FPGA board v 0.1

Project Type

Keep default RTL(Register Transfer Level) project, Press Next



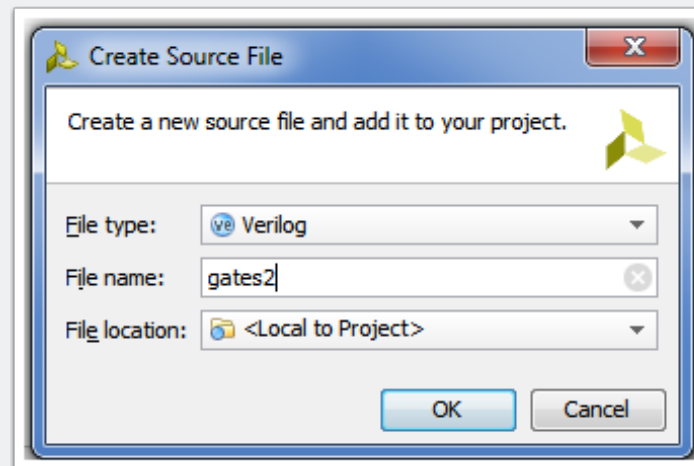
Add sources

In this tutorial we decided to use Verilog language so make sure it set correctly. Simulator language you can keep unchanged.

Simple VERILOG example using VIVADO 2015 with ZYBO FPGA board v 0.1

Create Source File

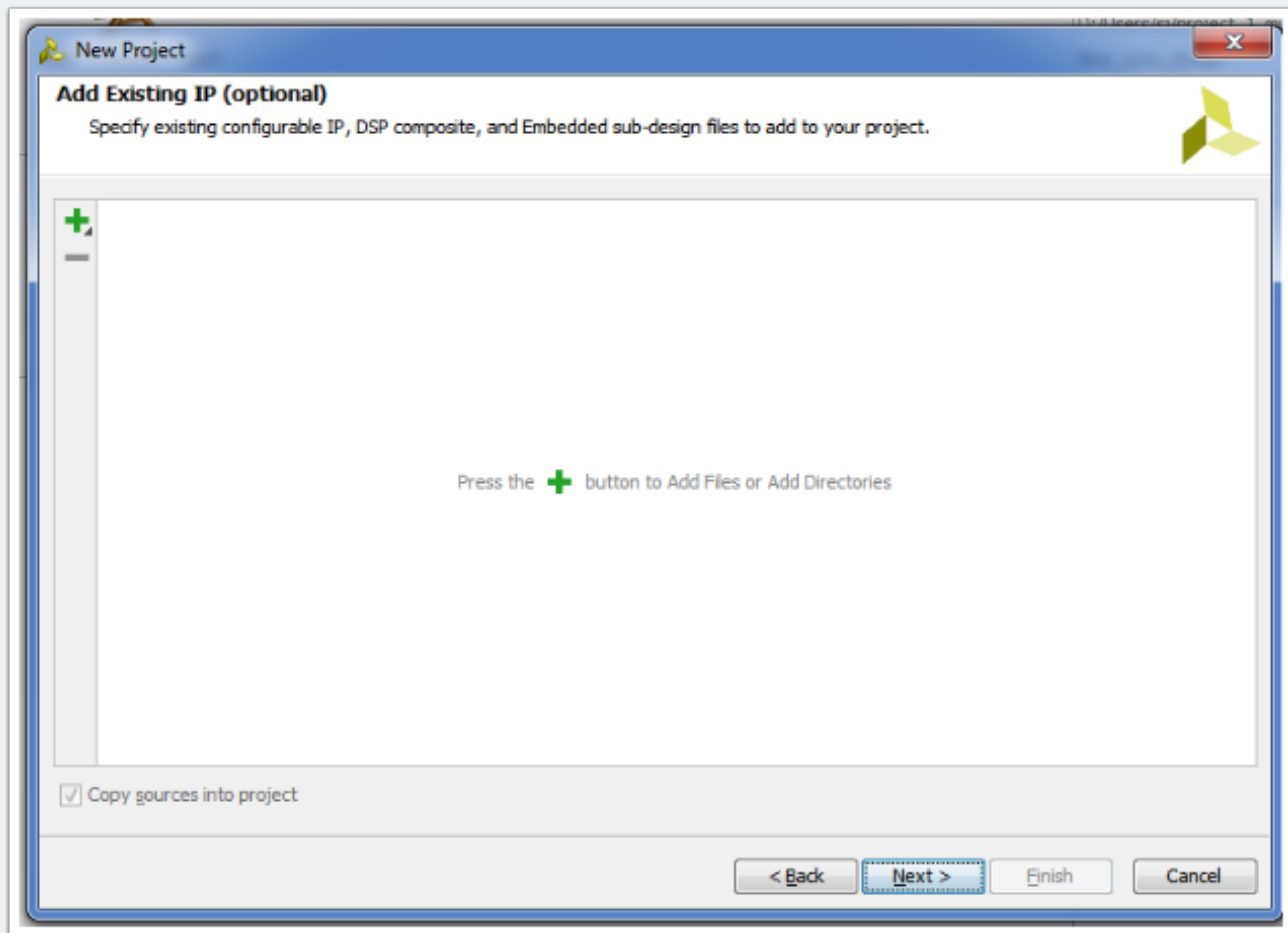
Set Filename to **gates2**. Keep the rest unchanged. Press OK. Press Next.



Simple VERILOG example using VIVADO 2015 with ZYBO FPGA board v 0.1

Add Existing IP

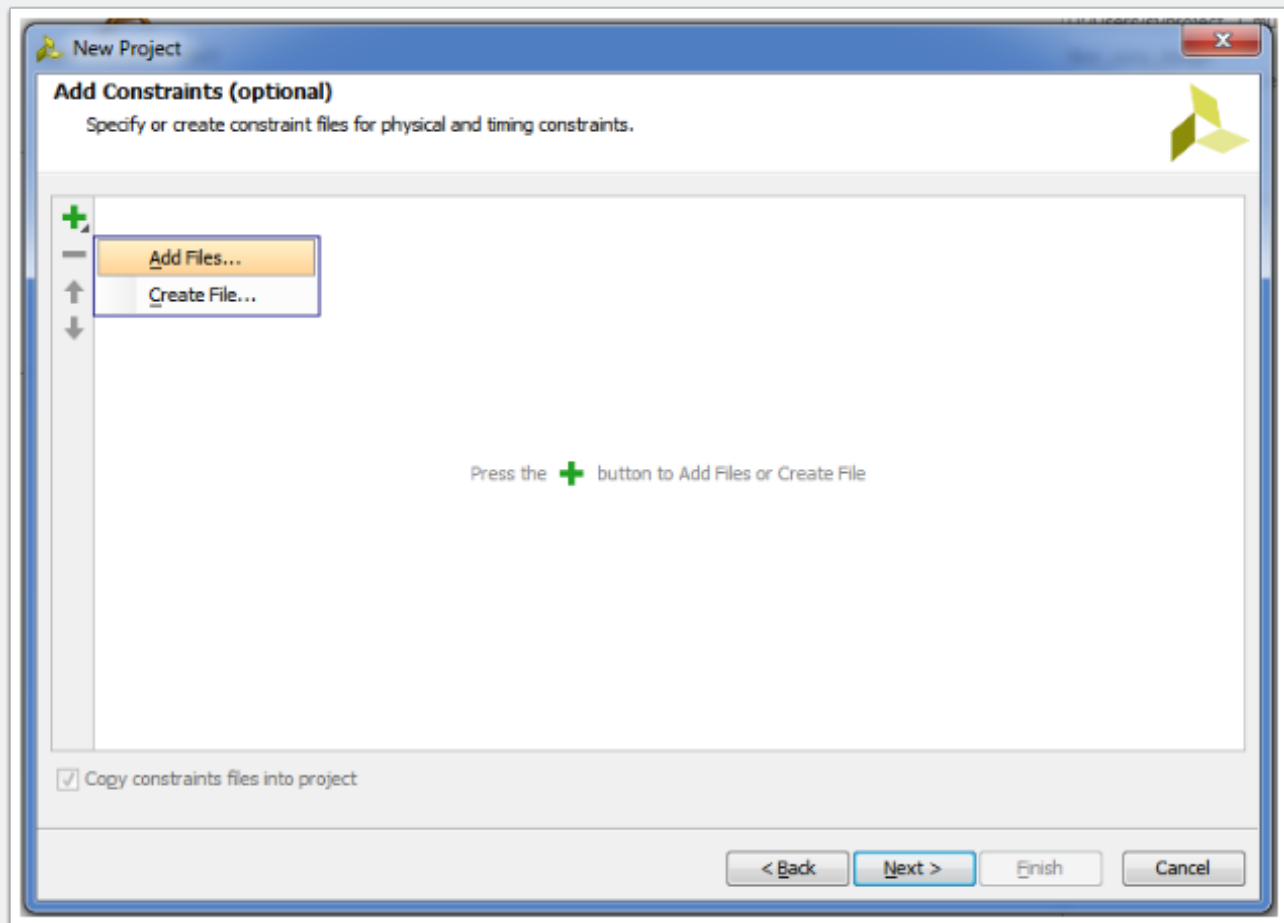
Click Next.



Simple VERILOG example using VIVADO 2015 with ZYBO FPGA board v 0.1

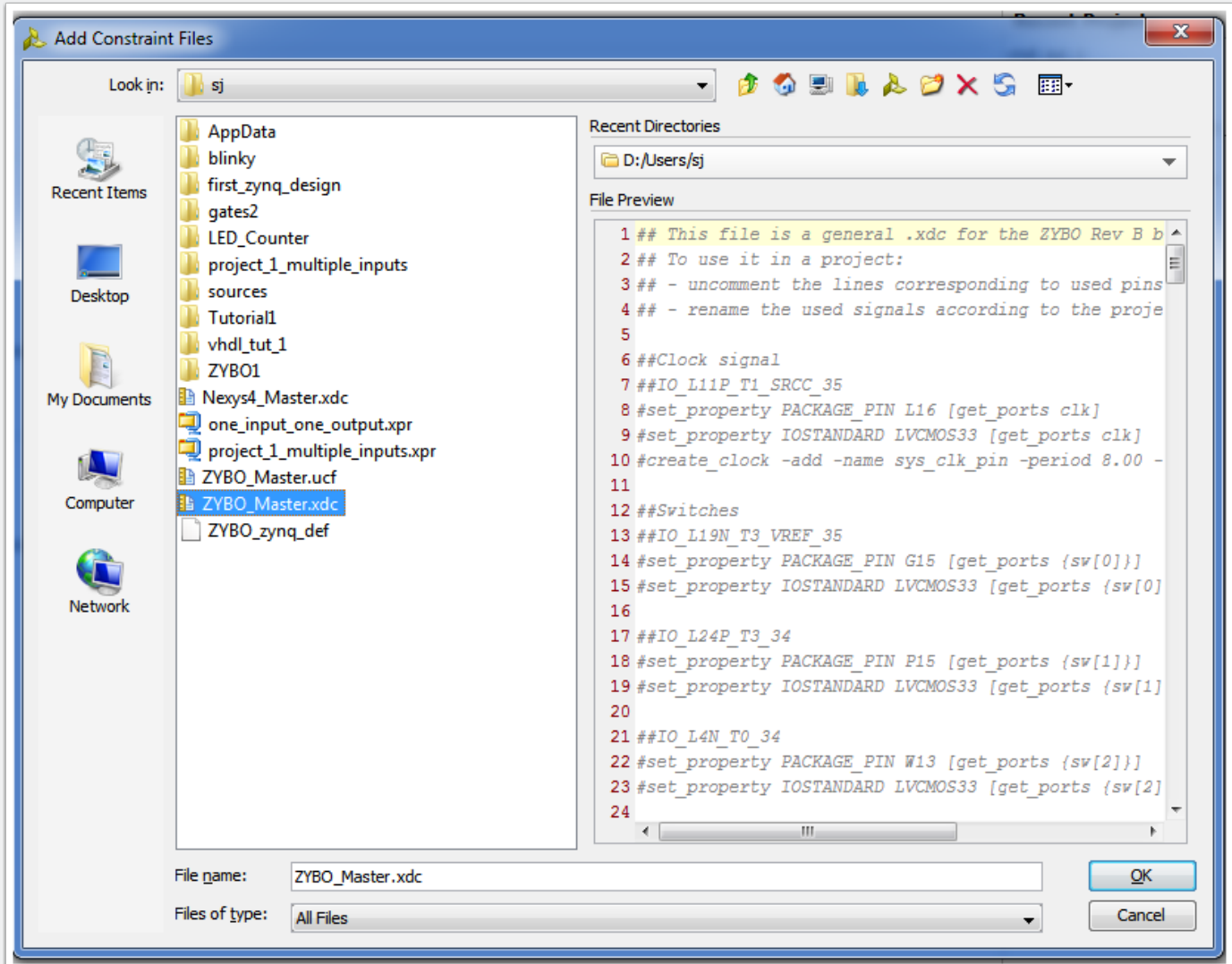
Add Constraints

Click "+", Add Files.



Simple VERILOG example using VIVADO 2015 with ZYBO FPGA board v 0.1

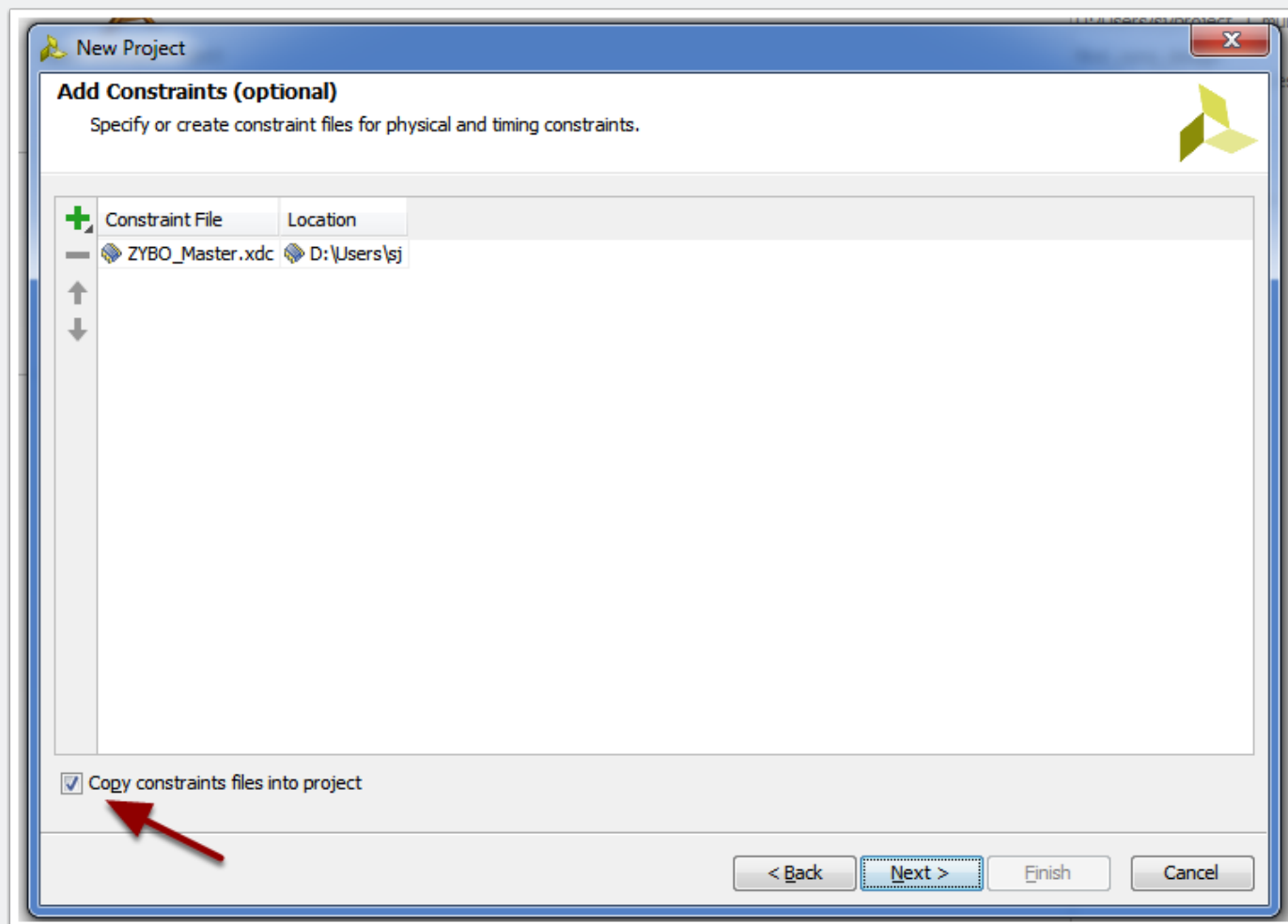
Add Constraint file we downloaded at Precondition step.



Simple VERILOG example using VIVADO 2015 with ZYBO FPGA board v 0.1

Make sure: Copy constraints files into project - Checked.

Click - Next



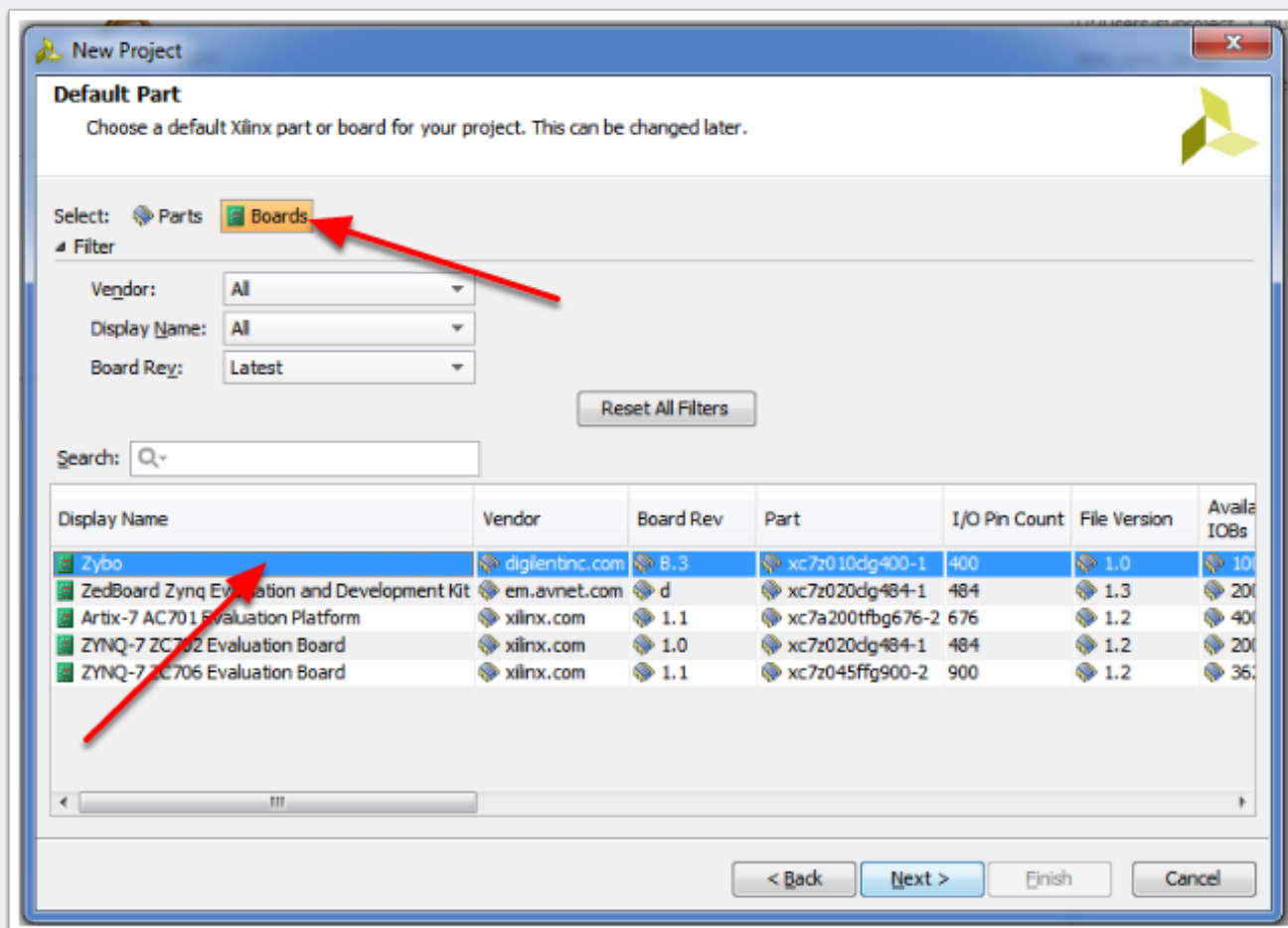
Default Part

Click on boards and select Zybo. If you still don't have it follow steps in Preconditions: Adding Zybo board to Vivado.

Simple VERILOG example using VIVADO 2015 with ZYBO FPGA board v 0.1

If you don't see ZYBO goto Preconditions Step.

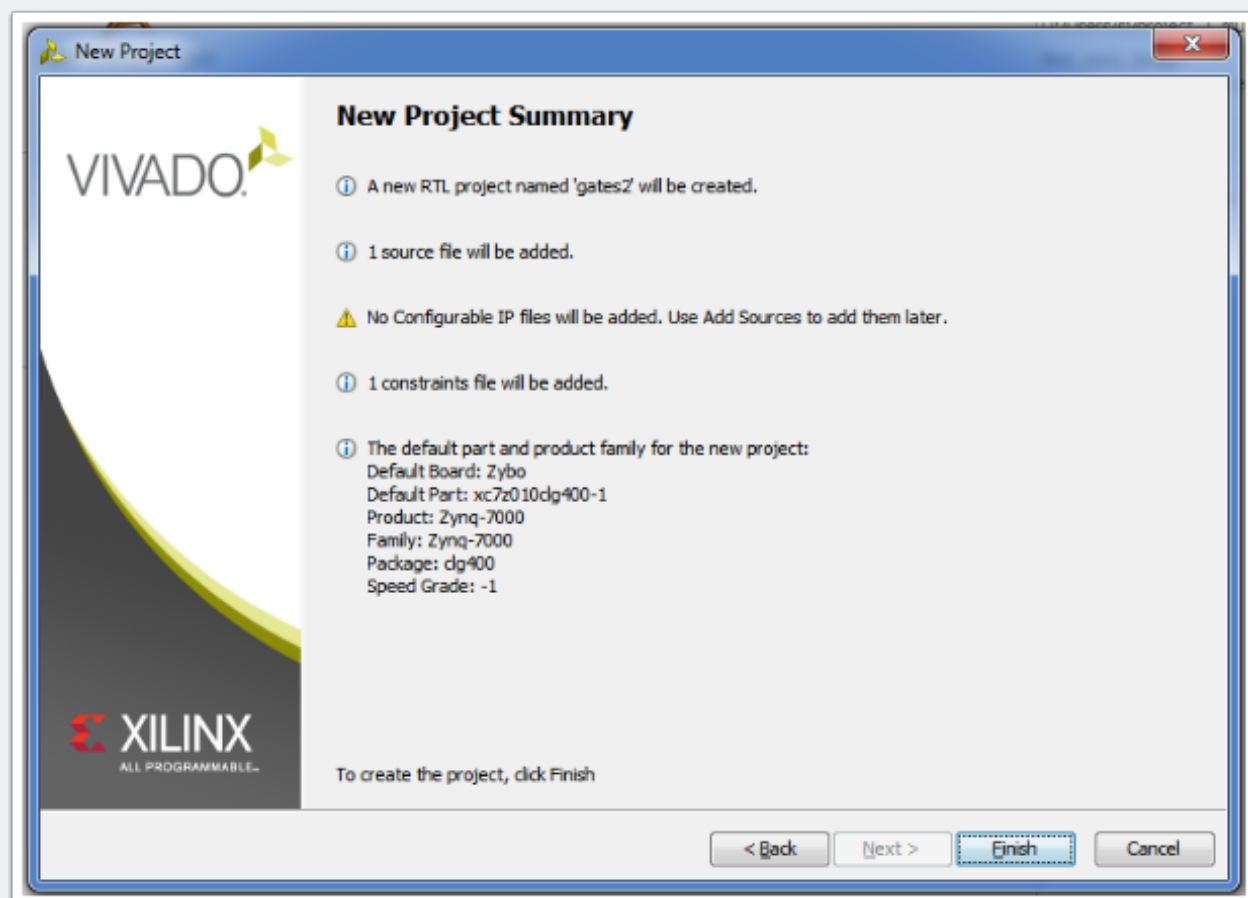
Next.



Simple VERILOG example using VIVADO 2015 with ZYBO FPGA board v 0.1

New Project Summary

Finish

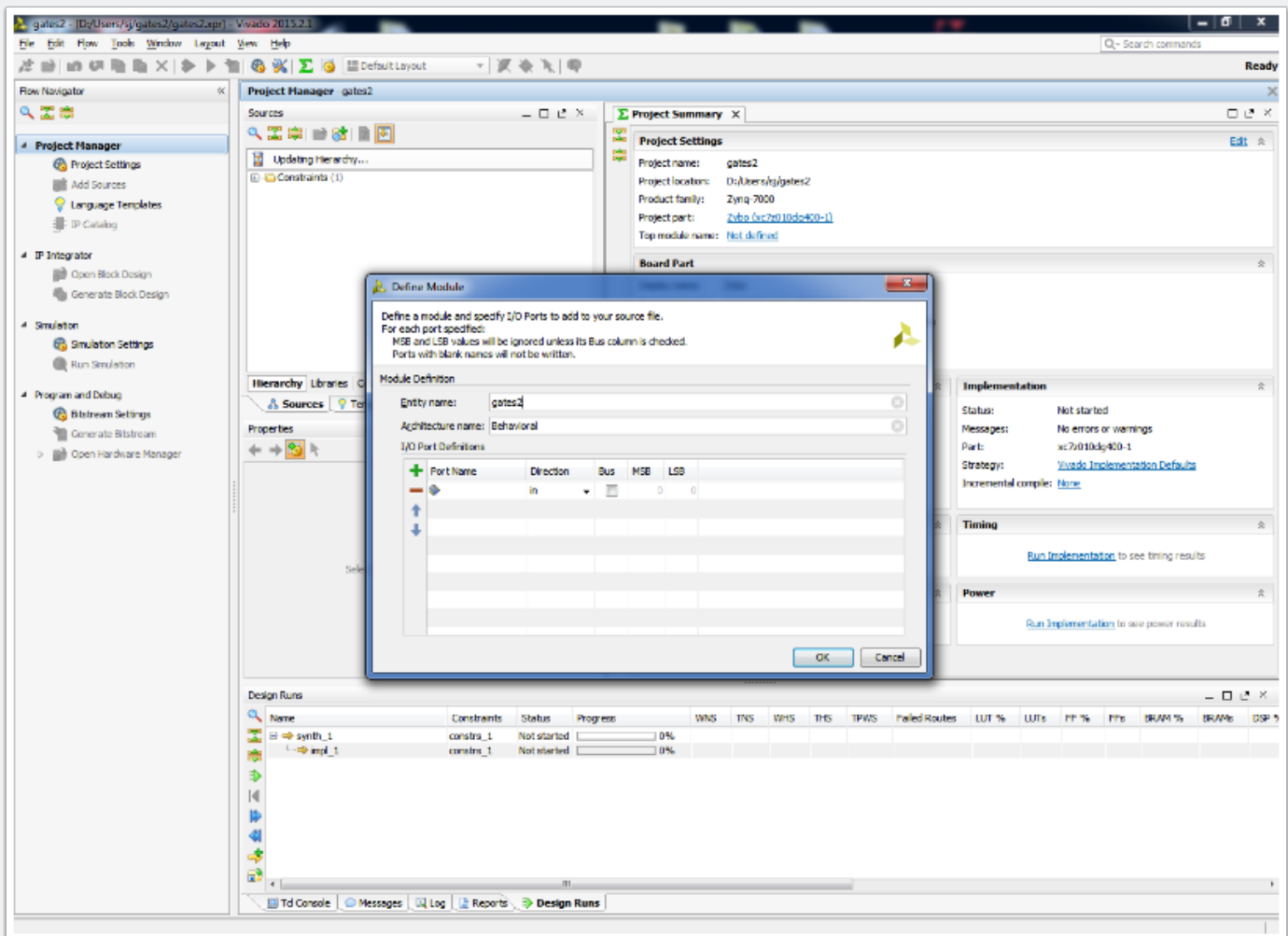


Simple VERILOG example using VIVADO 2015 with ZYBO FPGA board v 0.1

Phase 2. Editing Project

Project files generated and ready for your design.

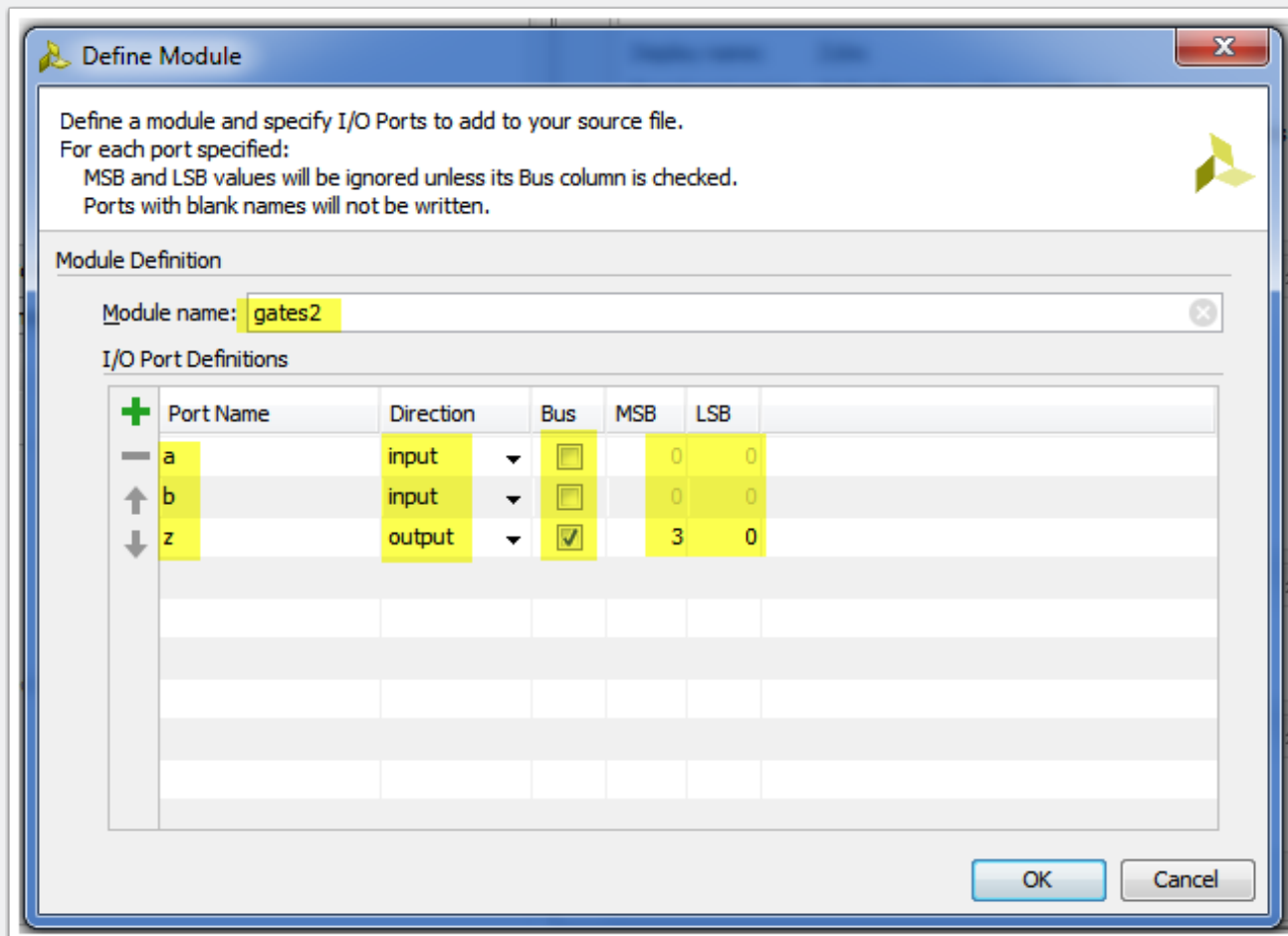
We will implement 2 input gates and 4 output basic gates **and**, **or**, **xor** and **nor**.



Define I/O ports as below

Simple VERILOG example using VIVADO 2015 with ZYBO FPGA board v 0.1

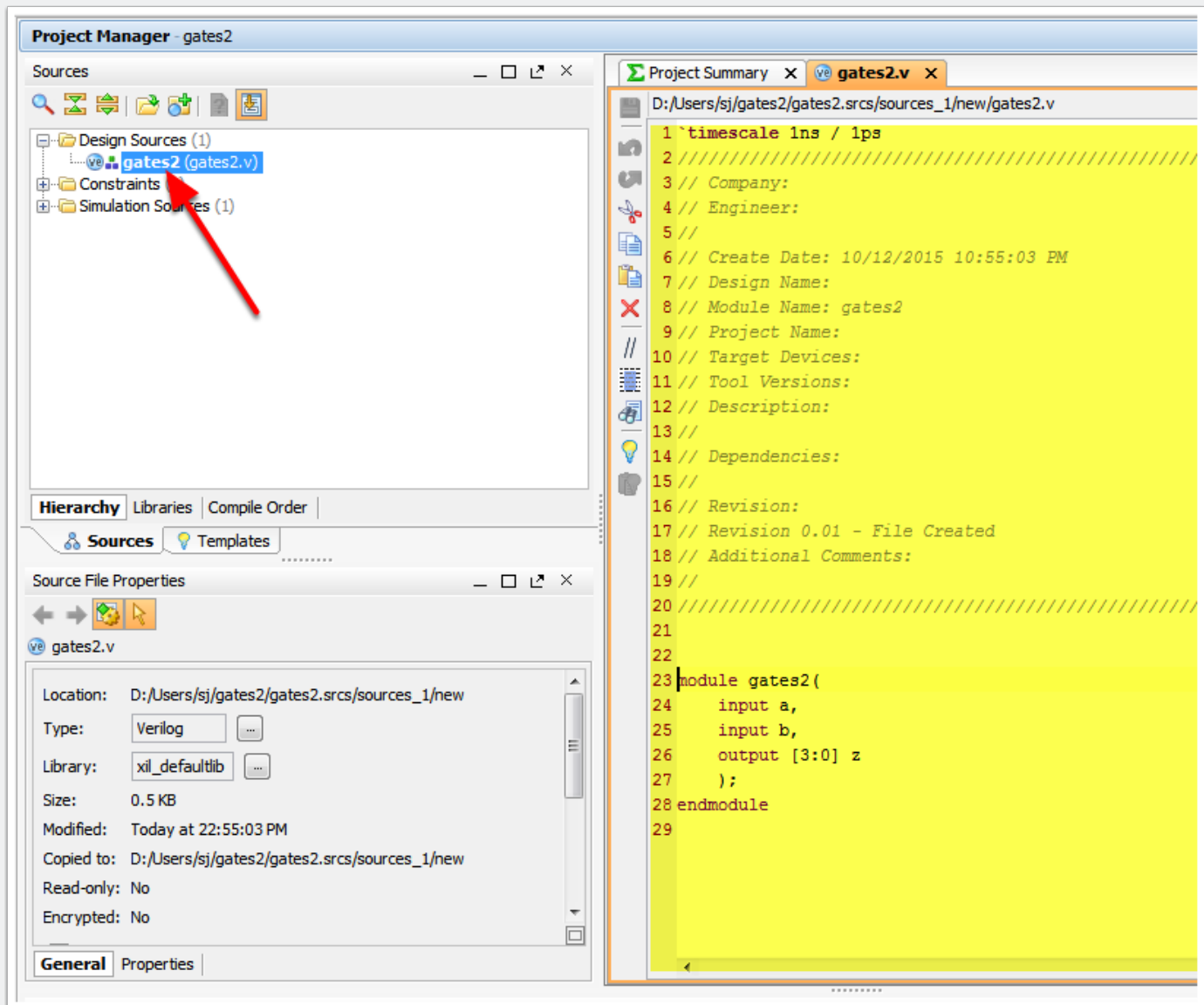
OK



Simple VERILOG example using VIVADO 2015 with ZYBO FPGA board v 0.1

Select Verilog Design

Click on Source file in Project Manager>Sources>Design Sources - Source code on Right-hand side should appear.



The screenshot displays the Vivado 2015 Project Manager interface. On the left, the 'Sources' tree shows 'Design Sources (1)' containing the file 'gates2 (gates2.v)', which is highlighted with a red arrow. Below the tree, the 'Source File Properties' window for 'gates2.v' is open, showing details such as its location, type (Verilog), and size. On the right, the 'Project Summary' window shows the source code for 'gates2.v'.

```
1 `timescale 1ns / 1ps
2 //////////////////////////////////////////////////
3 // Company:
4 // Engineer:
5 //
6 // Create Date: 10/12/2015 10:55:03 PM
7 // Design Name:
8 // Module Name: gates2
9 // Project Name:
10 // Target Devices:
11 // Tool Versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //////////////////////////////////////////////////
21
22
23 module gates2(
24     input a,
25     input b,
26     output [3:0] z
27 );
28 endmodule
29
```

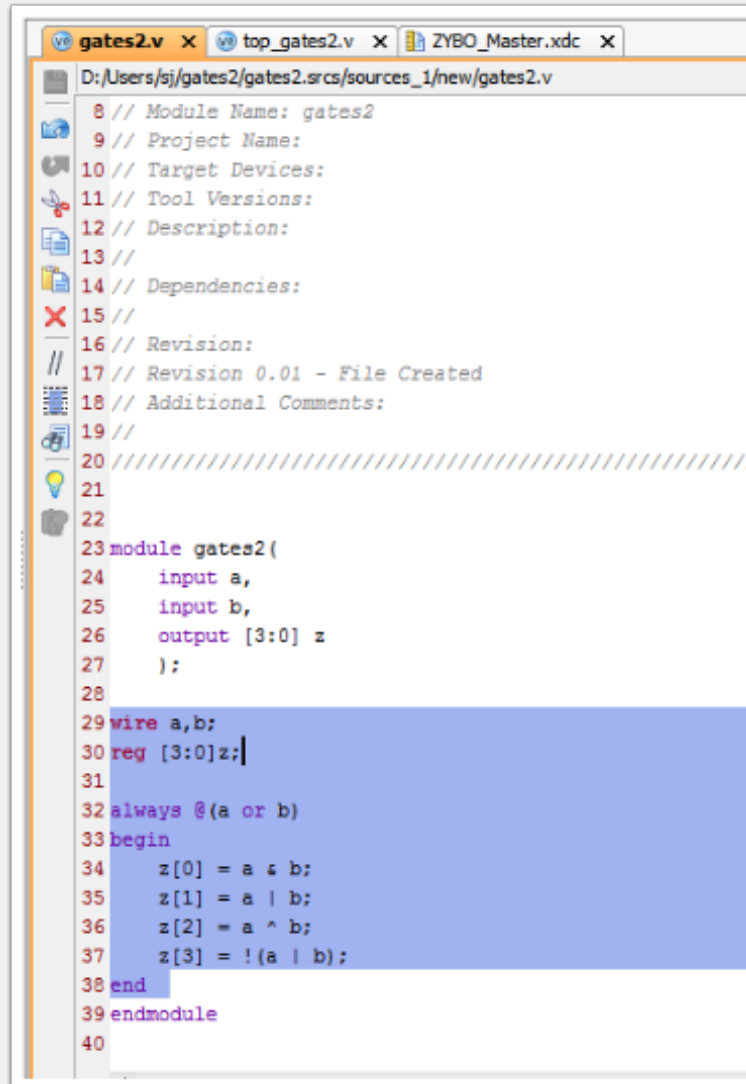
Simple VERILOG example using VIVADO 2015 with ZYBO FPGA board v 0.1

Changes to source code.

Modify Verilog file - add lines as highlighted below.

```
wire a,b;  
reg [3:0]z;  
always @(a or b)  
begin  
    z[0] = a & b;  
    z[1] = a | b;  
    z[2] = a ^ b;  
    z[3] = !(a | b);  
end
```

Simple VERILOG example using VIVADO 2015 with ZYBO FPGA board v 0.1



```
8 // Module Name: gates2
9 // Project Name:
10 // Target Devices:
11 // Tool Versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 ////////////////////////////////////////////////////////////////////
21
22
23 module gates2(
24     input a,
25     input b,
26     output [3:0] z
27 );
28
29 wire a,b;
30 reg [3:0]z;
31
32 always @(a or b)
33 begin
34     z[0] = a & b;
35     z[1] = a | b;
36     z[2] = a ^ b;
37     z[3] = !(a | b);
38 end
39 endmodule
40
```

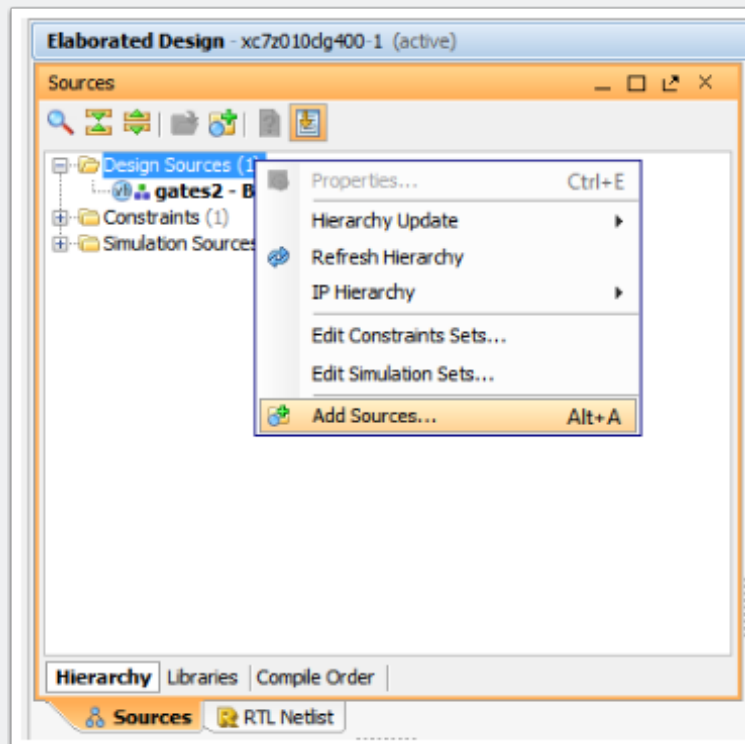
Create top file

Rightclick on Design Sources and select Add Sources.

1. Add or create design sources.

Simple VERILOG example using VIVADO 2015 with ZYBO FPGA board v 0.1

2. "+" > Create File



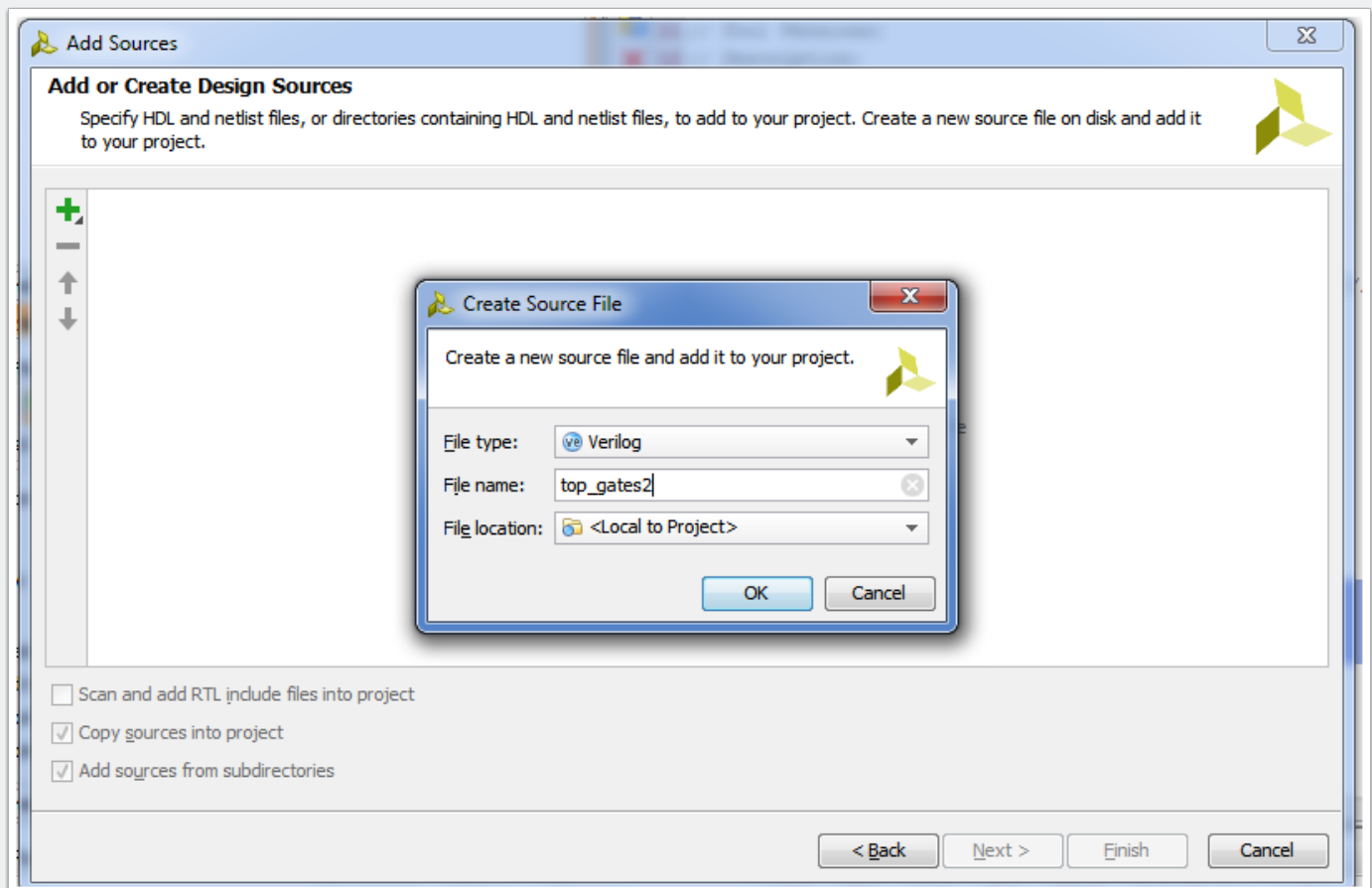
Simple VERILOG example using VIVADO 2015 with ZYBO FPGA board v 0.1

File Type :Verilog,

File name: top_gates2

OK

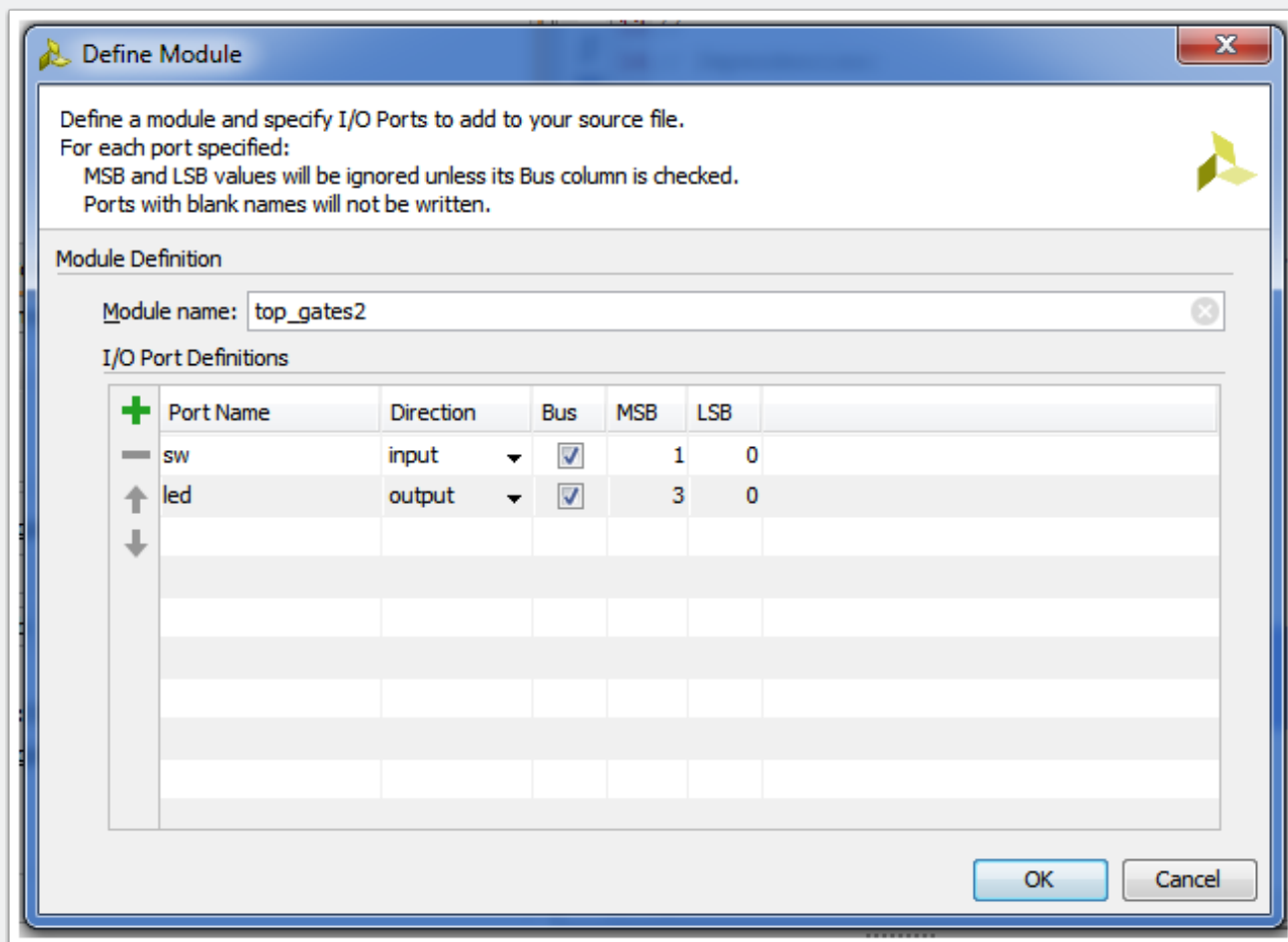
Finish



Simple VERILOG example using VIVADO 2015 with ZYBO FPGA board v 0.1

Define Module

Add sw and led as on image below.

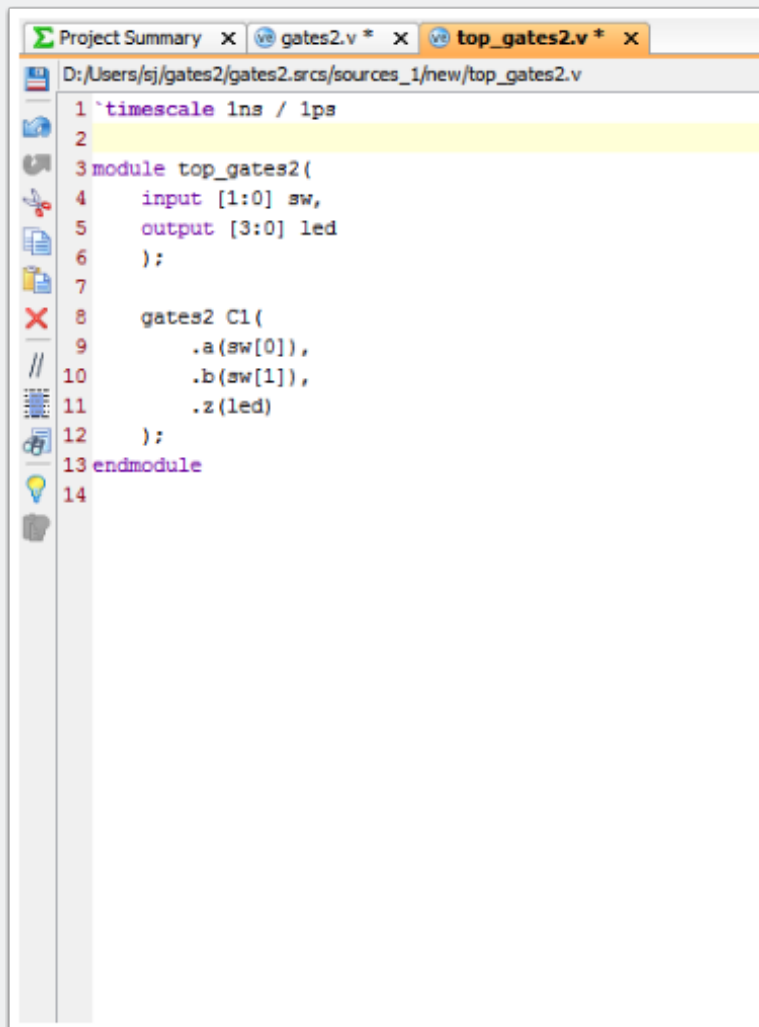


Replace default source code.

```
`timescale 1ns / 1ps
module top_gates2(
    input [1:0] sw,
    output [3:0] led
```

Simple VERILOG example using VIVADO 2015 with ZYBO FPGA board v 0.1

```
);  
  
gates2 C1(  
    .a(sw[0]),  
    .b(sw[1]),  
    .z(led)  
);  
endmodule
```

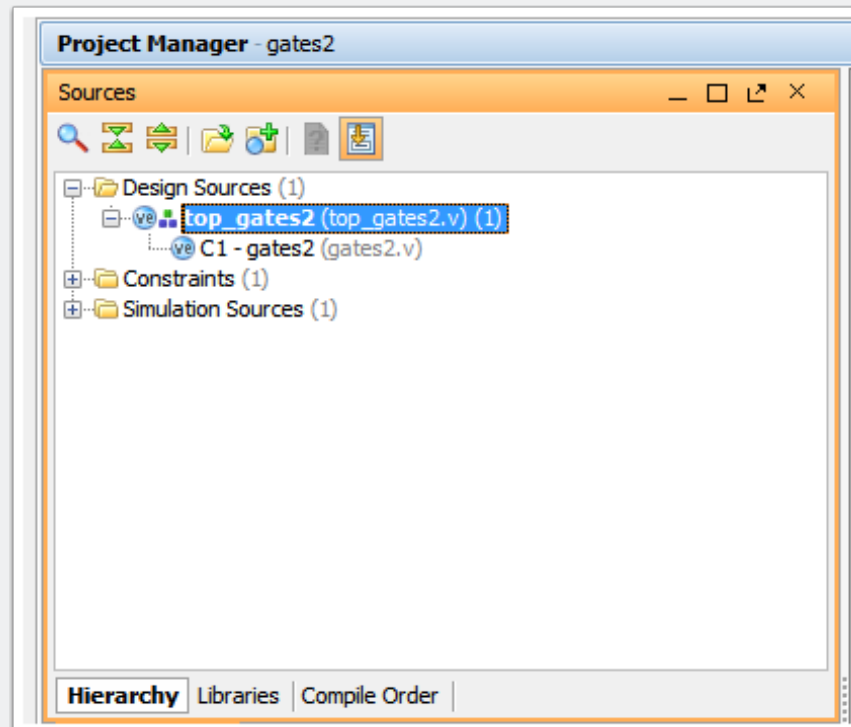


```
Project Summary x gates2.v * x top_gates2.v * x  
D:/Users/sj/gates2/gates2.srscs/sources_1/new/top_gates2.v  
1 `timescale 1ns / 1ps  
2  
3 module top_gates2(  
4     input [1:0] sw,  
5     output [3:0] led  
6 );  
7  
8     gates2 C1(  
9         .a(sw[0]),  
10        .b(sw[1]),  
11        .z(led)  
12    );  
13 endmodule  
14
```


Simple VERILOG example using VIVADO 2015 with ZYBO FPGA board v 0.1

Top Design

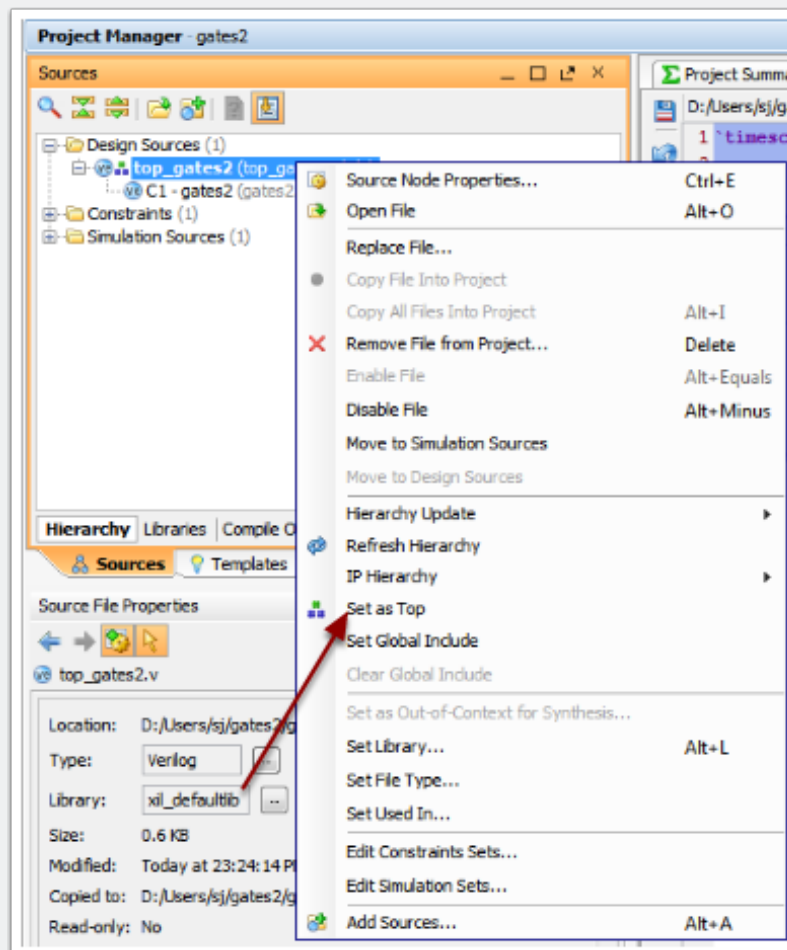
We have single top design interface file which use our gates2 design as component.



Simple VERILOG example using VIVADO 2015 with ZYBO FPGA board v 0.1

top design

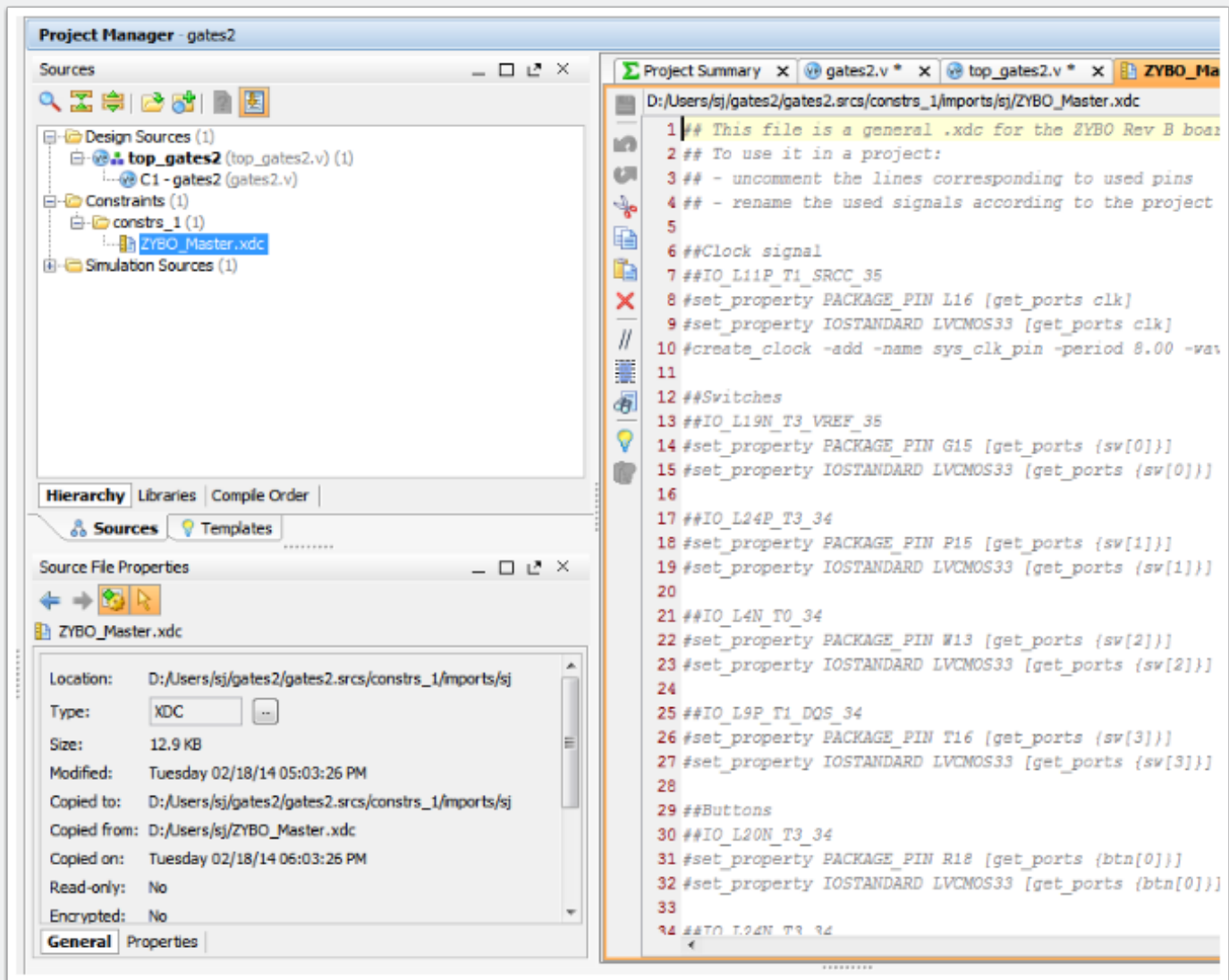
Make sure our top file became parent of gates2 file. Otherwise set it manually with **Set as Top**.



Simple VERILOG example using VIVADO 2015 with ZYBO FPGA board v 0.1

Amend Constraints file

Select xdc file from Sources>Constraints



The screenshot displays the Vivado Project Manager interface. The 'Sources' window on the left shows a project named 'gates2' with a 'Constraints' folder containing 'ZYBO_Master.xdc'. The 'Source File Properties' window is open for 'ZYBO_Master.xdc', showing its location and type. The 'Project Summary' window on the right displays the contents of the xdc file, which includes comments and configuration for the ZYBO Rev B board, such as clock signal settings and pin configurations.

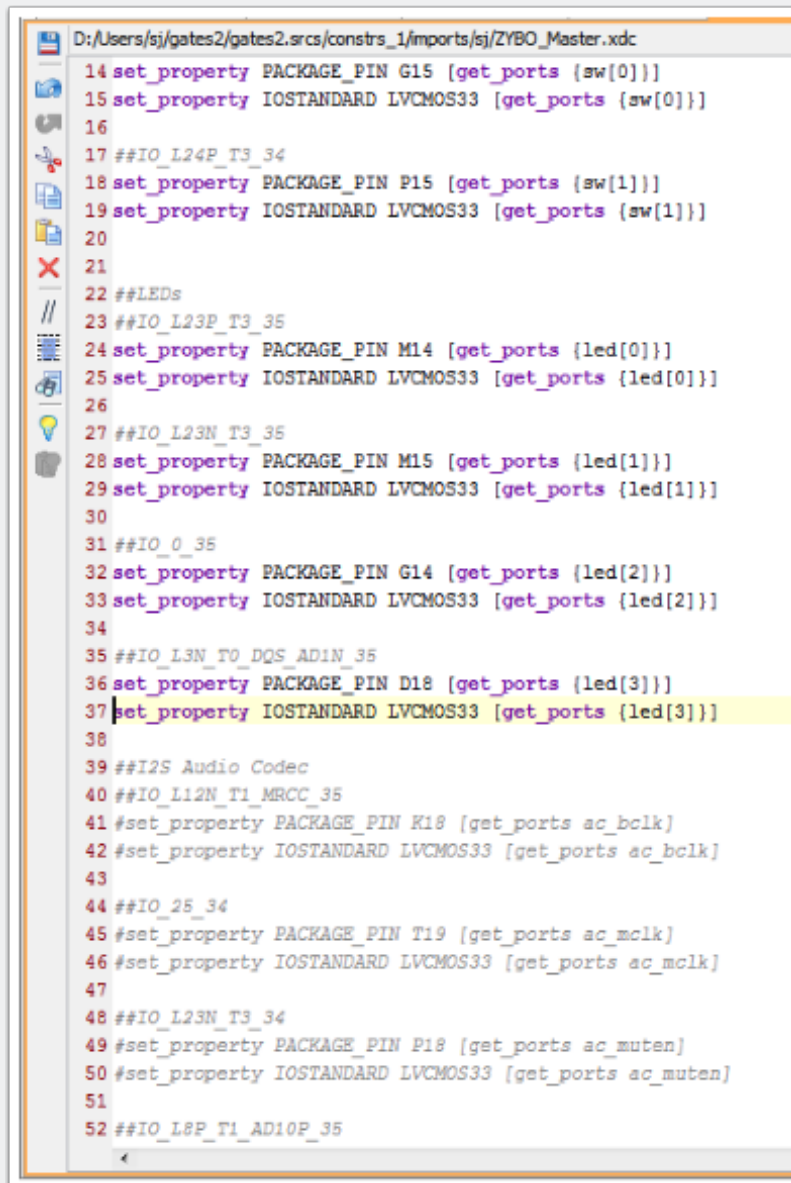
```
1 ## This file is a general .xdc for the ZYBO Rev B board
2 ## To use it in a project:
3 ## - uncomment the lines corresponding to used pins
4 ## - rename the used signals according to the project
5
6 ##Clock signal
7 ##IO_L11P_T1_SRCC_35
8 #set_property PACKAGE_PIN L16 [get_ports clk]
9 #set_property IOSTANDARD LVCMOS33 [get_ports clk]
10 #create_clock -add -name sys_clk_pin -period 8.00 -wa
11
12 ##Switches
13 ##IO_L19N_T3_VREF_35
14 #set_property PACKAGE_PIN G15 [get_ports {sw[0]}]
15 #set_property IOSTANDARD LVCMOS33 [get_ports {sw[0]}]
16
17 ##IO_L24P_T3_34
18 #set_property PACKAGE_PIN P15 [get_ports {sw[1]}]
19 #set_property IOSTANDARD LVCMOS33 [get_ports {sw[1]}]
20
21 ##IO_L4N_T0_34
22 #set_property PACKAGE_PIN W13 [get_ports {sw[2]}]
23 #set_property IOSTANDARD LVCMOS33 [get_ports {sw[2]}]
24
25 ##IO_L9P_T1_DQS_34
26 #set_property PACKAGE_PIN T16 [get_ports {sw[3]}]
27 #set_property IOSTANDARD LVCMOS33 [get_ports {sw[3]}]
28
29 ##Buttons
30 ##IO_L20N_T3_34
31 #set_property PACKAGE_PIN R18 [get_ports {btn[0]}]
32 #set_property IOSTANDARD LVCMOS33 [get_ports {btn[0]}]
33
34 ##IO_L24N_T3_34
```

Simple VERILOG example using VIVADO 2015 with ZYBO FPGA board v 0.1

Changes in xdc file

Uncomment lines of I/O ports we need to use.

Save file.



```
D:/Users/sj/gates2/gates2.srcs/constrs_1/imports/sj/ZYBO_Master.xdc
14 set_property PACKAGE_PIN G15 [get_ports {sw[0]]}
15 set_property IOSTANDARD LVCMOS33 [get_ports {sw[0]]}
16
17 ##IO_L24P_T3_34
18 set_property PACKAGE_PIN P15 [get_ports {sw[1]]}
19 set_property IOSTANDARD LVCMOS33 [get_ports {sw[1]]}
20
21
22 ##LEDs
23 ##IO_L23P_T3_35
24 set_property PACKAGE_PIN M14 [get_ports {led[0]]}
25 set_property IOSTANDARD LVCMOS33 [get_ports {led[0]]}
26
27 ##IO_L23N_T3_35
28 set_property PACKAGE_PIN M15 [get_ports {led[1]]}
29 set_property IOSTANDARD LVCMOS33 [get_ports {led[1]]}
30
31 ##IO_0_35
32 set_property PACKAGE_PIN G14 [get_ports {led[2]]}
33 set_property IOSTANDARD LVCMOS33 [get_ports {led[2]]}
34
35 ##IO_L3N_T0_DQS_AD1N_35
36 set_property PACKAGE_PIN D18 [get_ports {led[3]]}
37 set_property IOSTANDARD LVCMOS33 [get_ports {led[3]]}
38
39 ##I2S Audio Codec
40 ##IO_L12N_T1_MRCC_35
41 #set_property PACKAGE_PIN K18 [get_ports ac_bclk]
42 #set_property IOSTANDARD LVCMOS33 [get_ports ac_bclk]
43
44 ##IO_25_34
45 #set_property PACKAGE_PIN T19 [get_ports ac_mclk]
46 #set_property IOSTANDARD LVCMOS33 [get_ports ac_mclk]
47
48 ##IO_L23N_T3_34
49 #set_property PACKAGE_PIN P18 [get_ports ac_muten]
50 #set_property IOSTANDARD LVCMOS33 [get_ports ac_muten]
51
52 ##IO_L8P_T1_AD10P_35
```

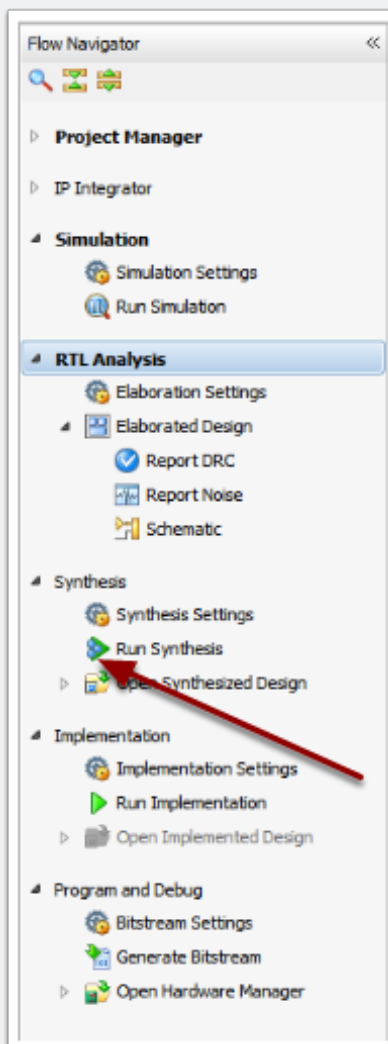
Simple VERILOG example using VIVADO 2015 with ZYBO FPGA board v 0.1

Phase 3 - Synthesis and uploading to device.

At Synthesis phase we convert our circuit from register transfer level (RTL) into a design implementation in terms of logic gates.

In Flow Navigator on Lefthand side.:

Next steps can be **Simulation>Run Simulation** or **RTL Analysis>Schematic** but we skip them in this tutorial and come directly to **Synthesis>Run Synthesis**.

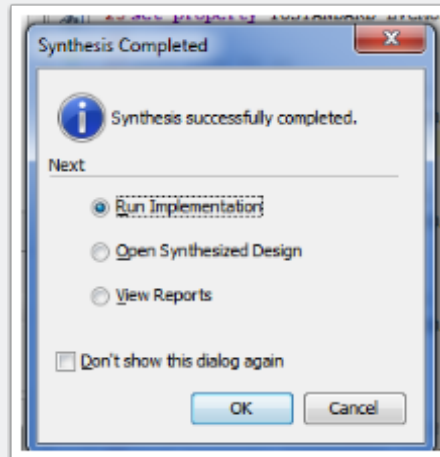


Simple VERILOG example using VIVADO 2015 with ZYBO FPGA board v 0.1

Synthesis completion

Leave default Run Implementation

OK

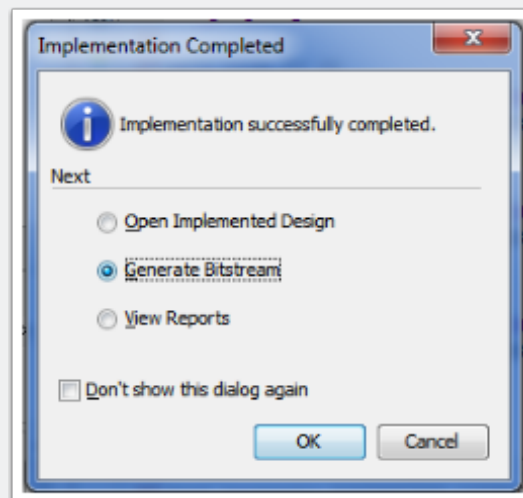


Simple VERILOG example using VIVADO 2015 with ZYBO FPGA board v 0.1

Generate Bitstream

Select Generate Bitstream

OK



Simple VERILOG example using VIVADO 2015 with ZYBO FPGA board v 0.1

Final

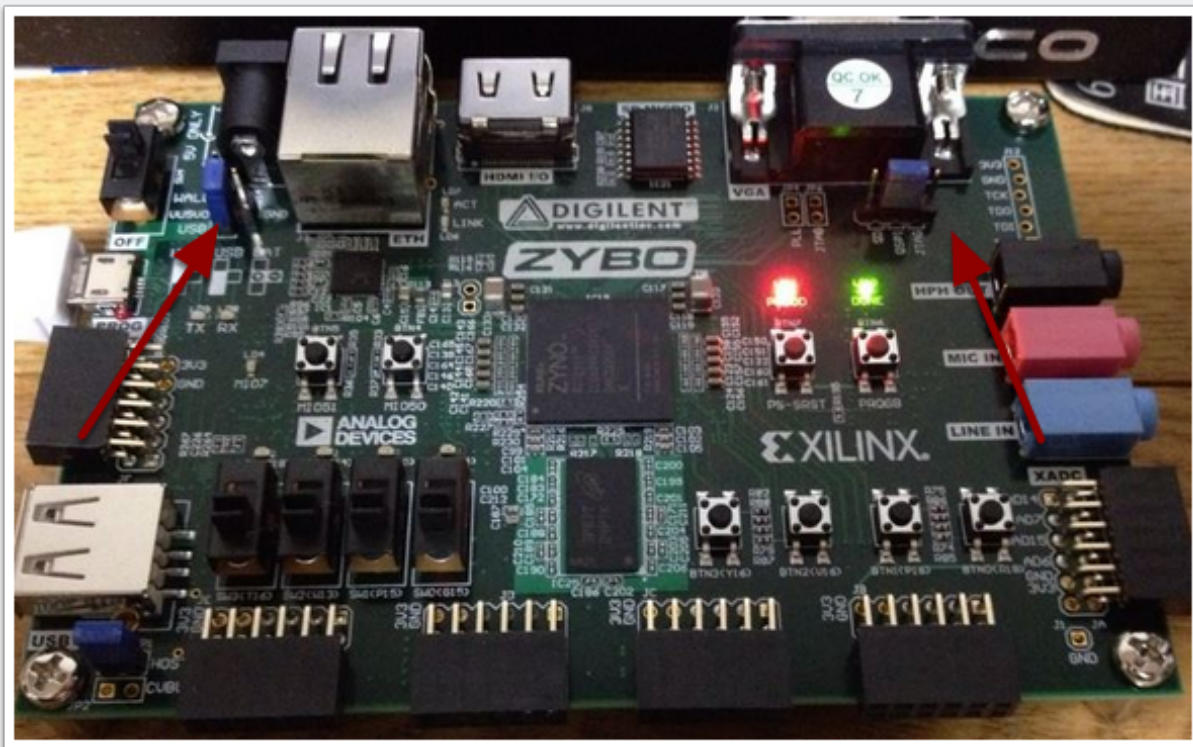
Pay attention to jumpers.

JP7 - It should set to USB.

JP5 can be JTAG or QSPI

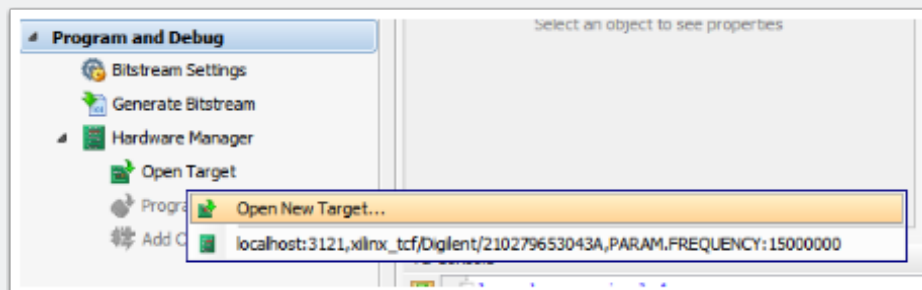
Connect ZYBO to PC with Micro-USB cable.

Photo taken from <http://marsee101.blog19.fc2.com/blog-entry-2745.html>

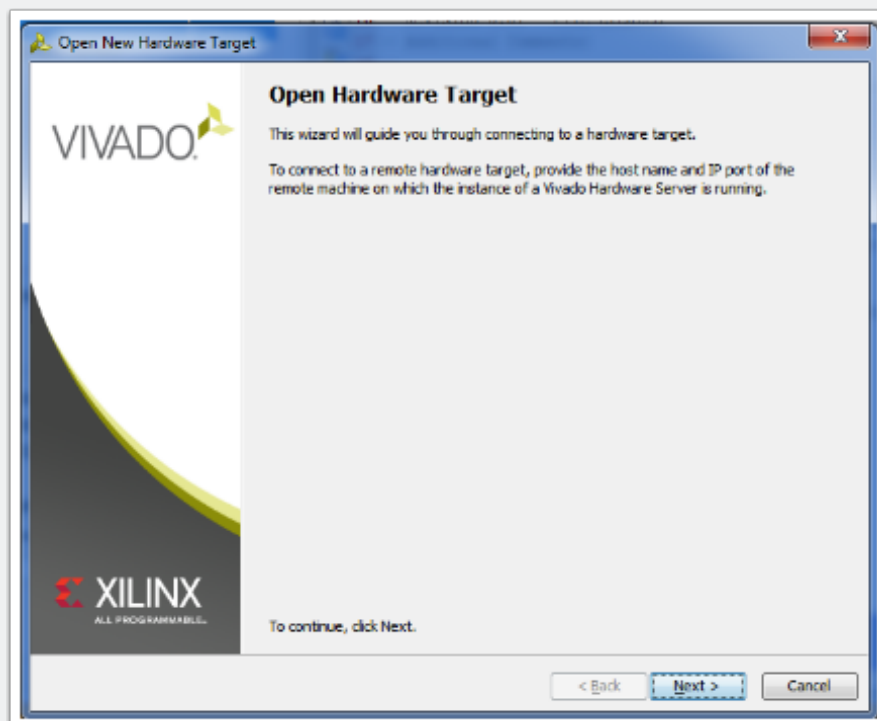


Simple VERILOG example using VIVADO 2015 with ZYBO FPGA board v 0.1

Program ZYBO

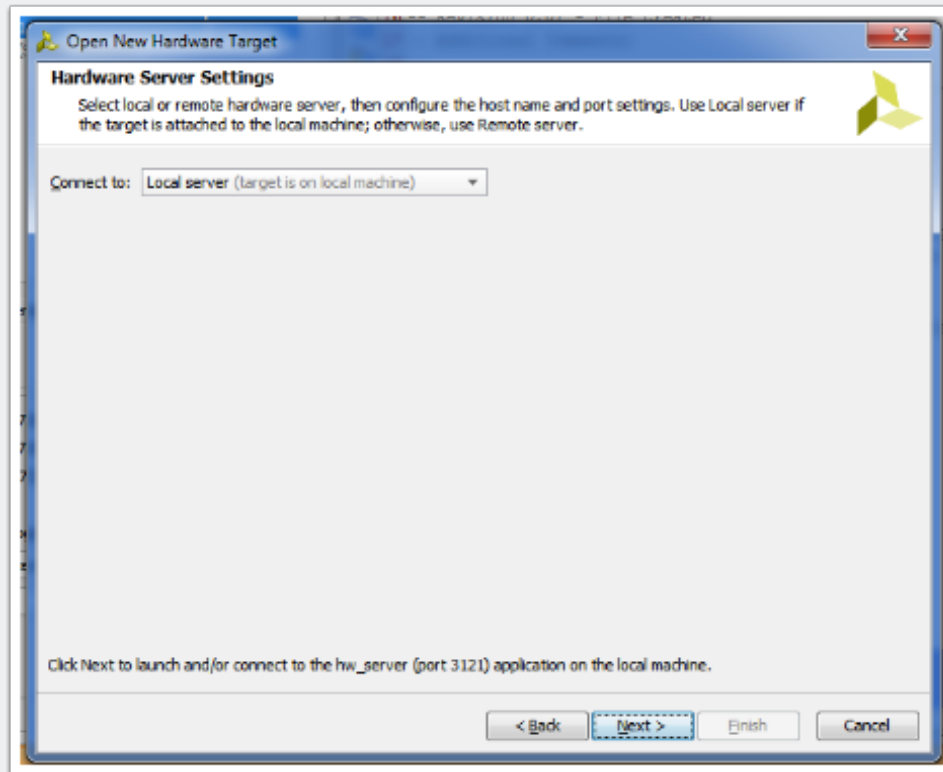


Next



Simple VERILOG example using VIVADO 2015 with ZYBO FPGA board v 0.1

Next

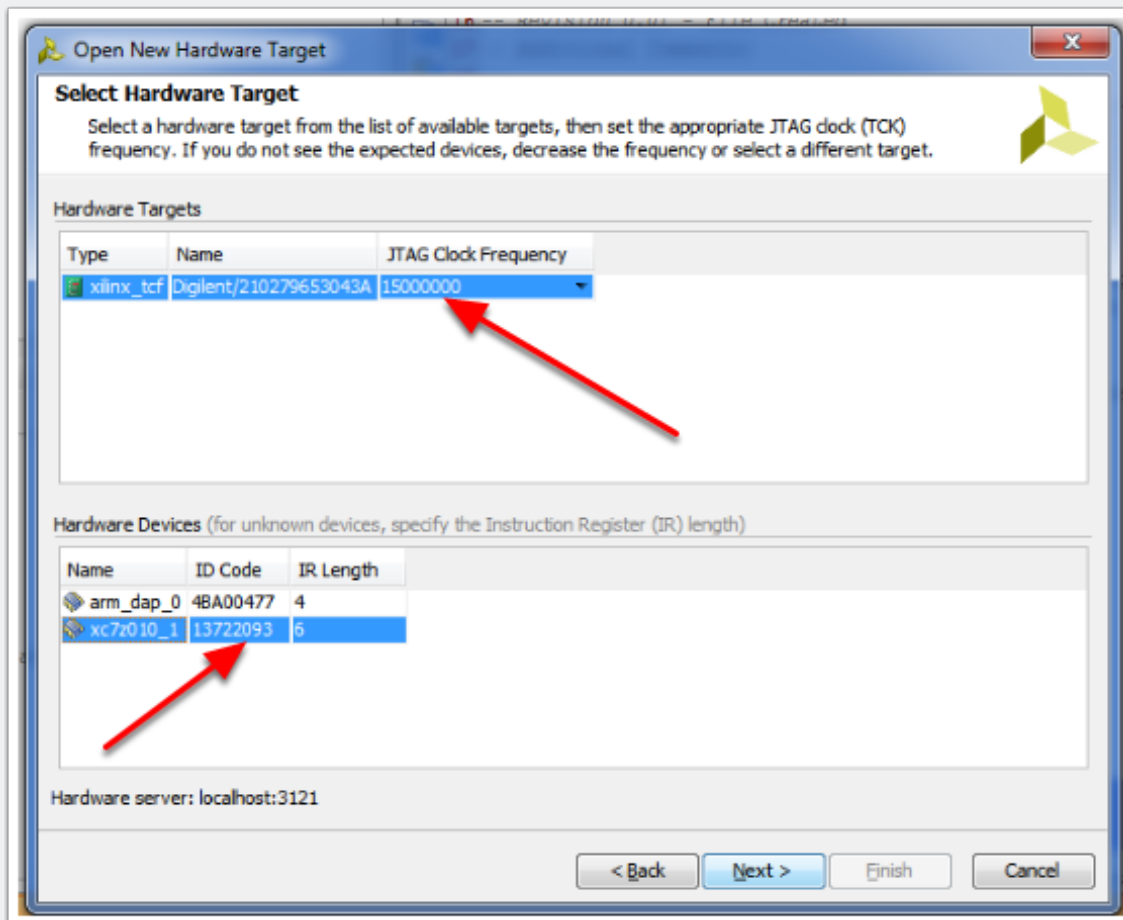


Simple VERILOG example using VIVADO 2015 with ZYBO FPGA board v 0.1

Make sure you have similar setting like on picture below.

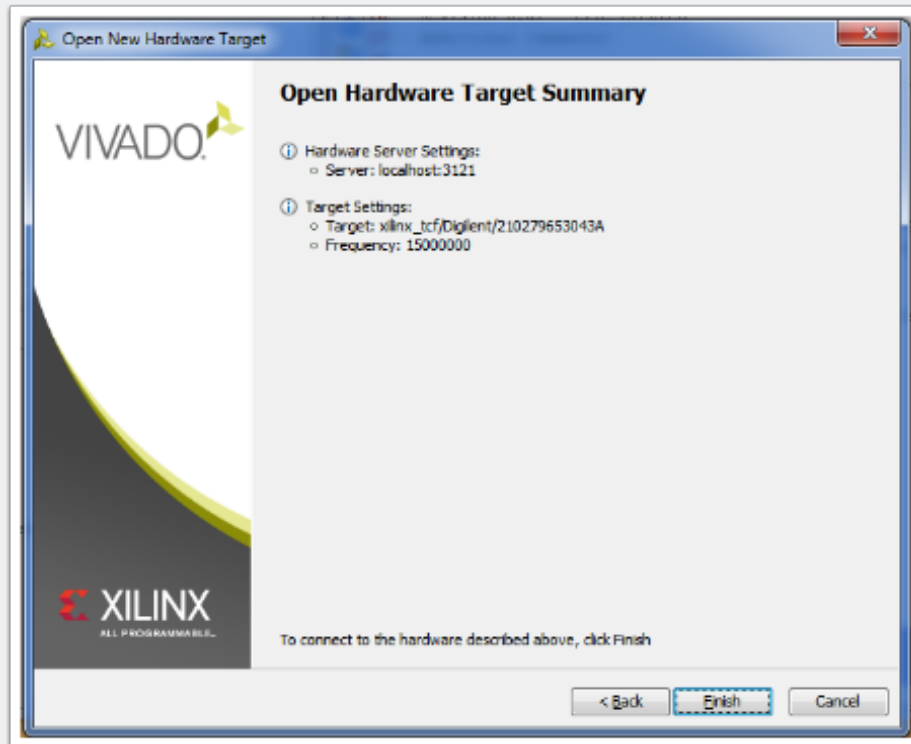
Select xc7z010_1

Next

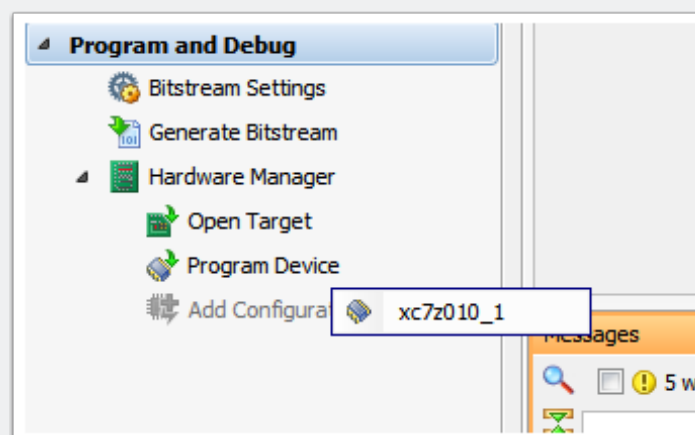


Simple VERILOG example using VIVADO 2015 with ZYBO FPGA board v 0.1

Finish

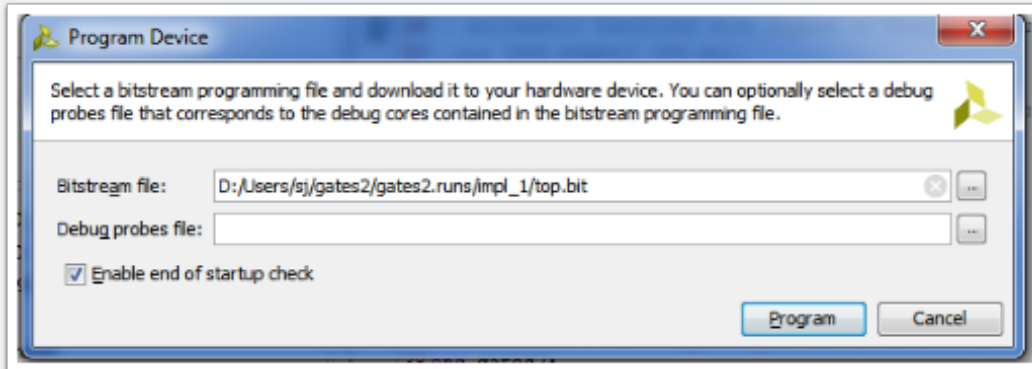


Program device > xc7z010_1

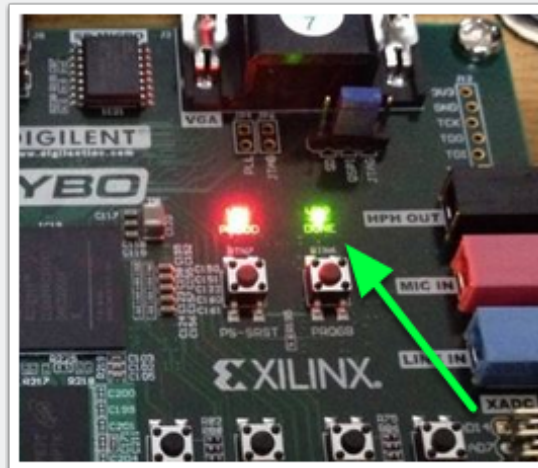


Simple VERILOG example using VIVADO 2015 with ZYBO FPGA board v 0.1

Program



As confirmation of successful upload Green Led will set



Simple VERILOG example using VIVADO 2015 with ZYBO FPGA board v 0.1

Use switches to confirm **and**, **or**, **xor** and **nor** operations.

Archive of project [available](#).

PDF version of this lesson [available](#).



Reference

1. <http://www.slideshare.net/MaryalaSrinivas/verilog-tutorial>
2. <http://www.instructables.com/id/Learn-Verilog-A-Brief-Tutorial-Series-on-FPGA-Desi/?ALLSTEPS>
3. [The ZYNQ BOOK](#) - Make sure you download not only book archive but also tutorials book with sources.
4. HDL Chip Design- A Practical Guide for Designing, Synthesizing and Simulating ASICs and FPGAs Using VHDL or Verilog. By Douglas J. Smith
5. [ZYBO Reference Manual](#)

Simple VERILOG example using VIVADO 2015 with ZYBO FPGA board v 0.1

Files

1. [Project Archive](#)
2. [ZYBO Board Definition File.](#)
3. [ZYBO Master xdc file.](#)

Feedback

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