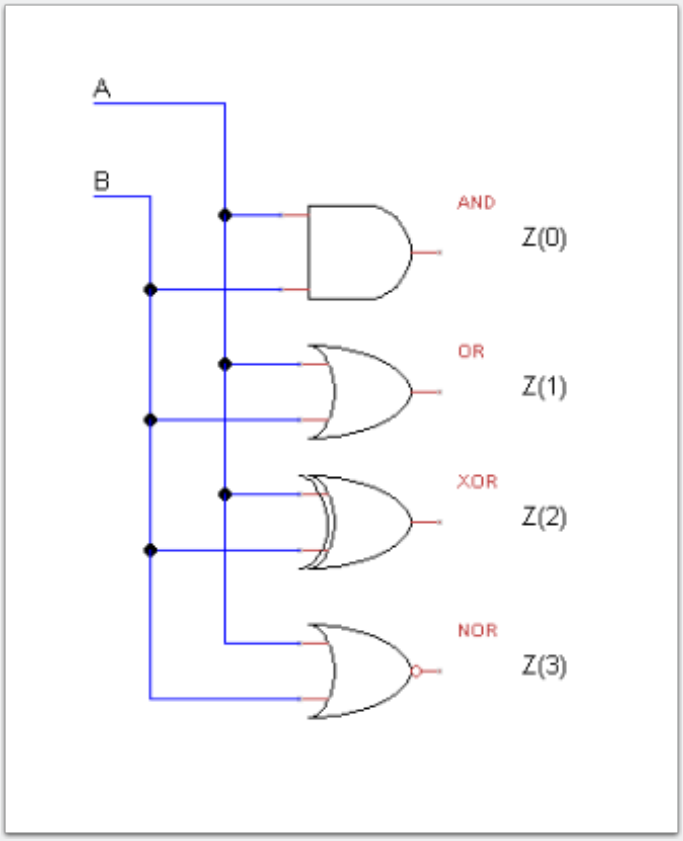
Simple VERILOG example using VIVADO 2015 with ZYBO FPGA board v 0.1

Aim

I am FPGA novice and want to try classical FPGA design tutorials. I bought perfect modern FPGA board ZYBO (**ZY**nq **BO**ard) based on Xilinx Z-7010 from Digilent but latest tools from Xilinx VIVADO 2015.2 more focused on AP SoC programming while I want to just pure FPGA design without any linuxes bootloaders etc. So I wrote this tutorial to help people like me :)

In this example we make simple scheme: 2 signals IN and 4 OUT.



Preconditions: Adding Zybo Board to Vivado

Vivado 2015.2 under Windows 7 64 bit was used with 16 GB of RAM.

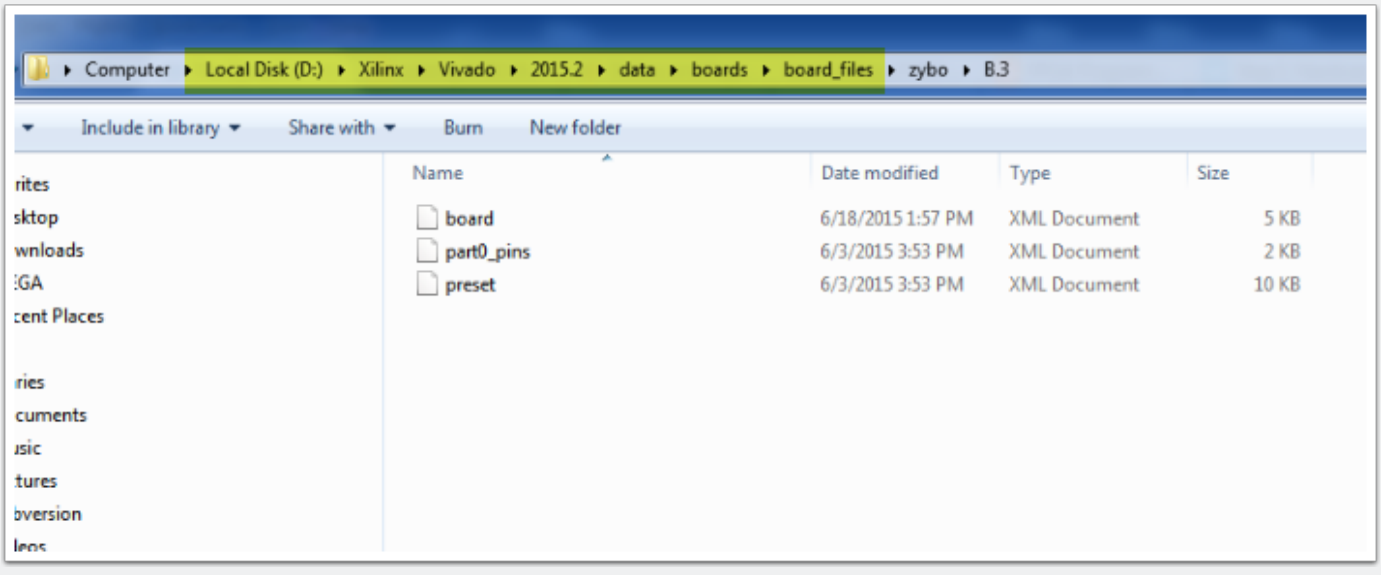
Before using Zybo with Vivado you should add Zybo Definitions File to Vivado.

1. Good source for Board Definition files is Zynqbook website.Download The_Zynq_Book_Tutorial_Sources_Aug15.zip

2. Copy **zybo** folder with content from Archive path **\sources\zybo\setup\board_part** into D:\Xilinx\Vivado\2015.2**\data\boards\board_files** (if D:\Xilinx\Vivado\2015.2 is my PC you probably have C:\Xilinx etc...)

3. In board_files you should see other boards so now our Zybo known by Vivado.

4. Download ZYBO_Master.xdc from Digilent website unpack constraints files on local hard disk for example on Desktop.

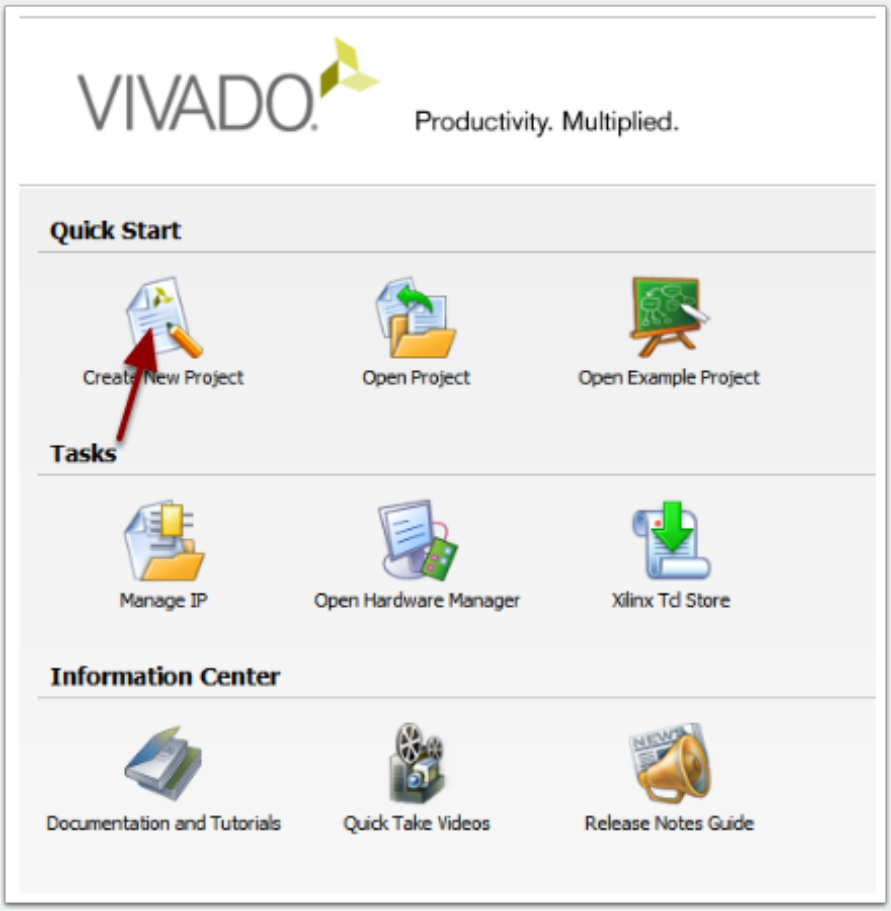


Phase 1. Preparation.

I have latest Vivado Design Edition from Xilinx which comes with Digilent Zybo board.

Launch your Vivado.

Create new project



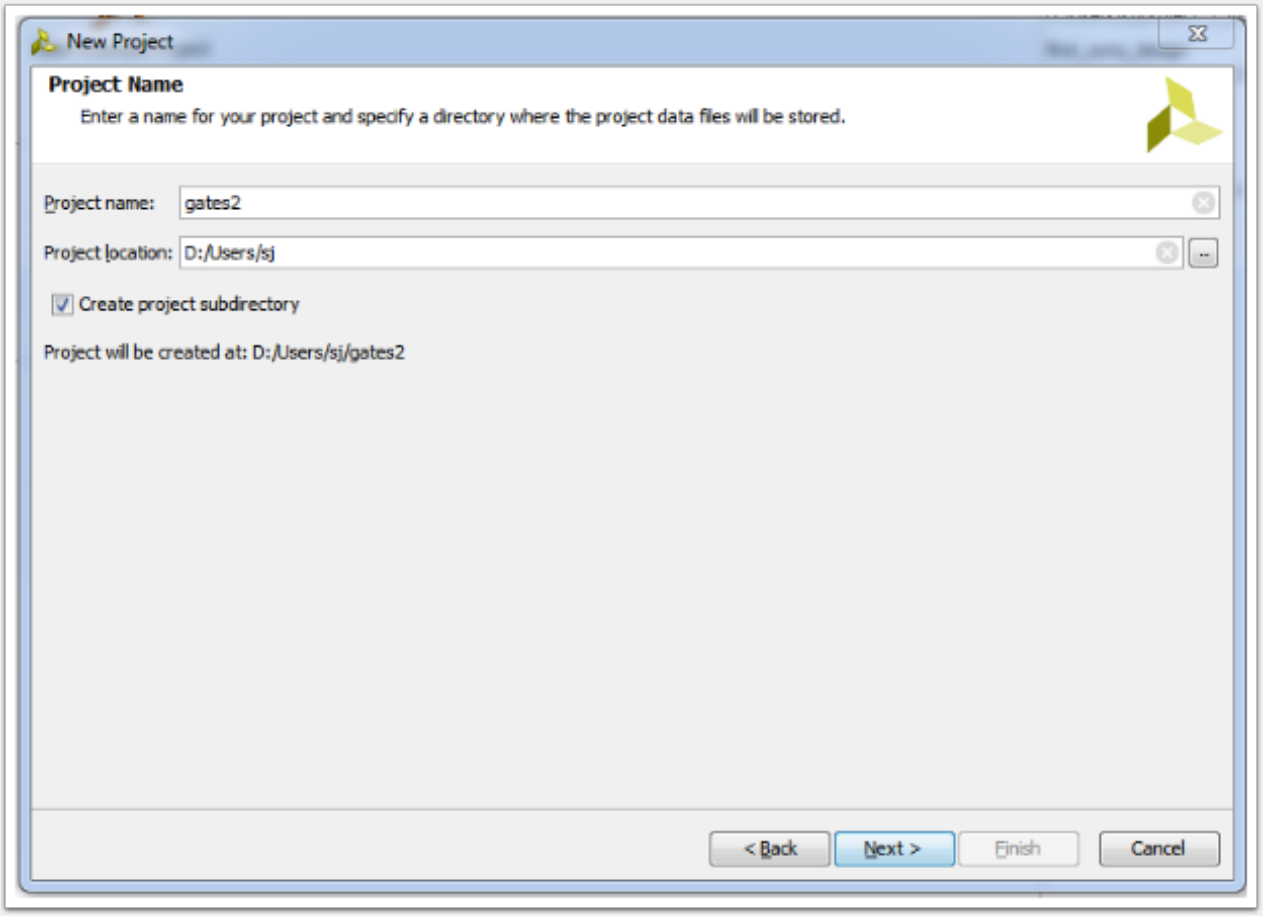
New Project

Click Next

Set project name.

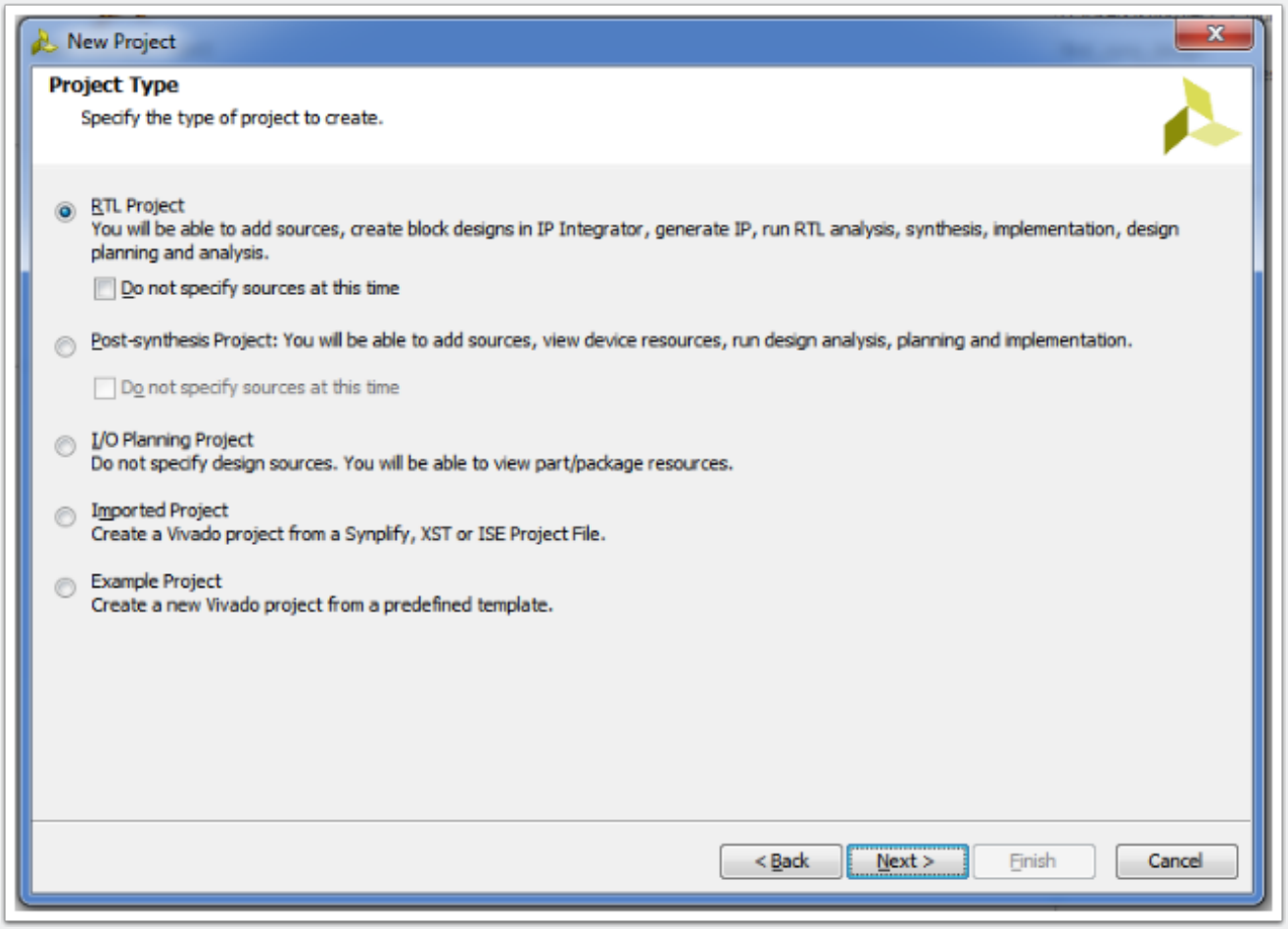
Set project name to **gates2**,

Keep rest settings unchanged unless you know what you doing.



Project Type

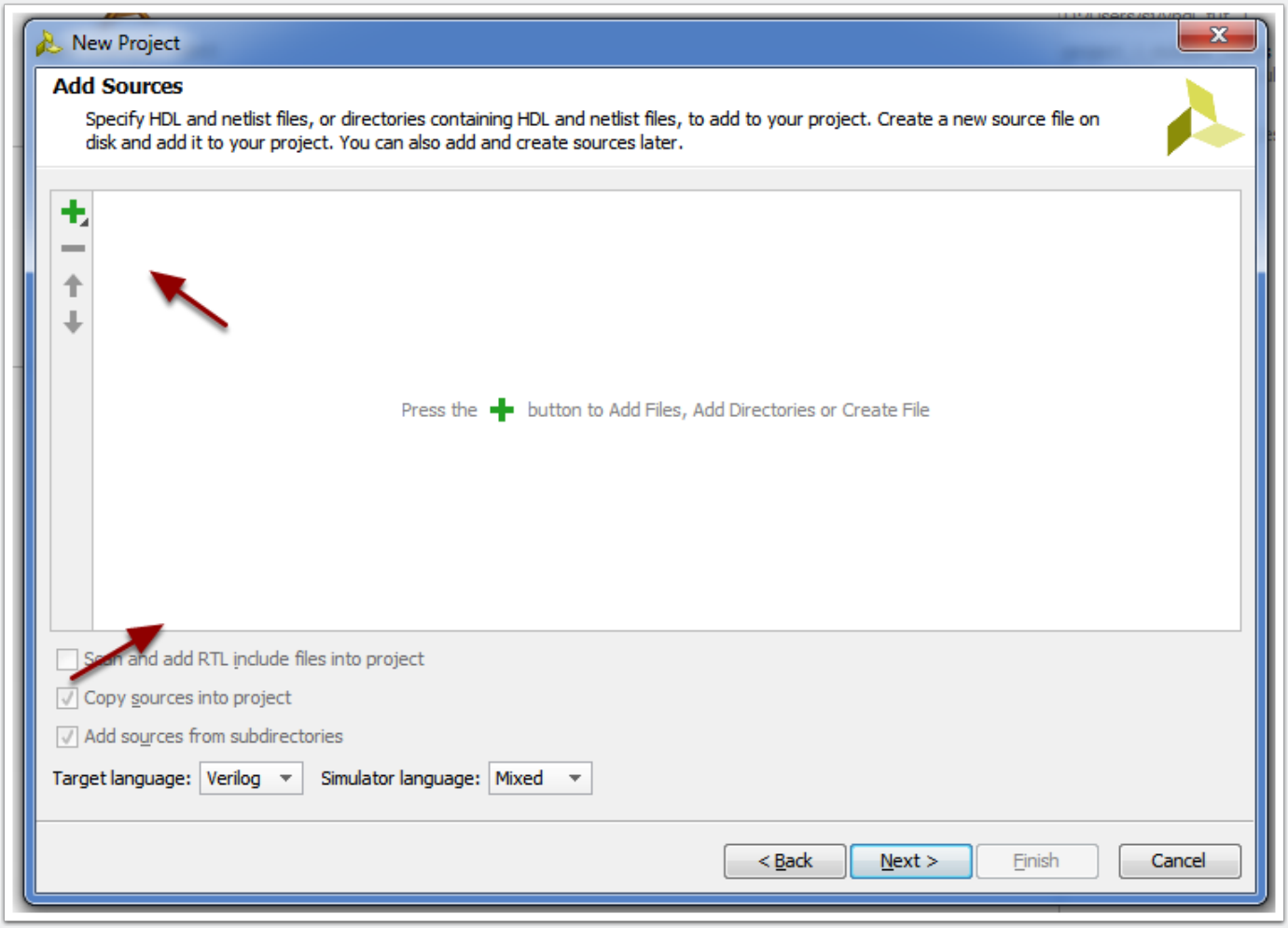
Keep default RTL(Register Transfer Level) project, Press Next



Add sources

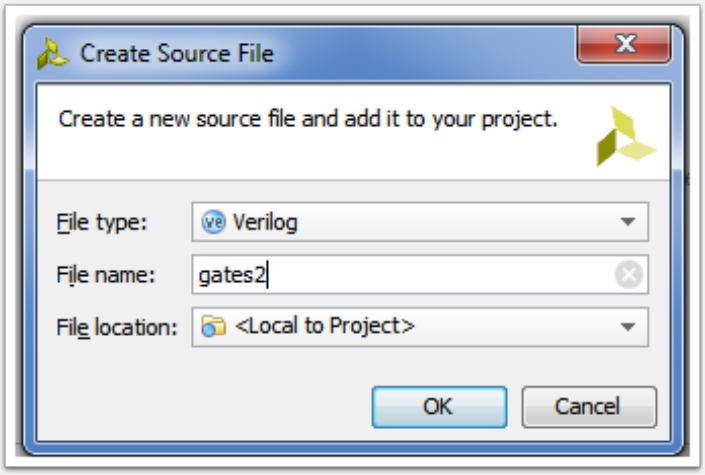
In this tutorial we decided to use Verilog language so make sure it set correctly. Simulator language you can keep unchanged.

Click on "+" - Select - Create File.



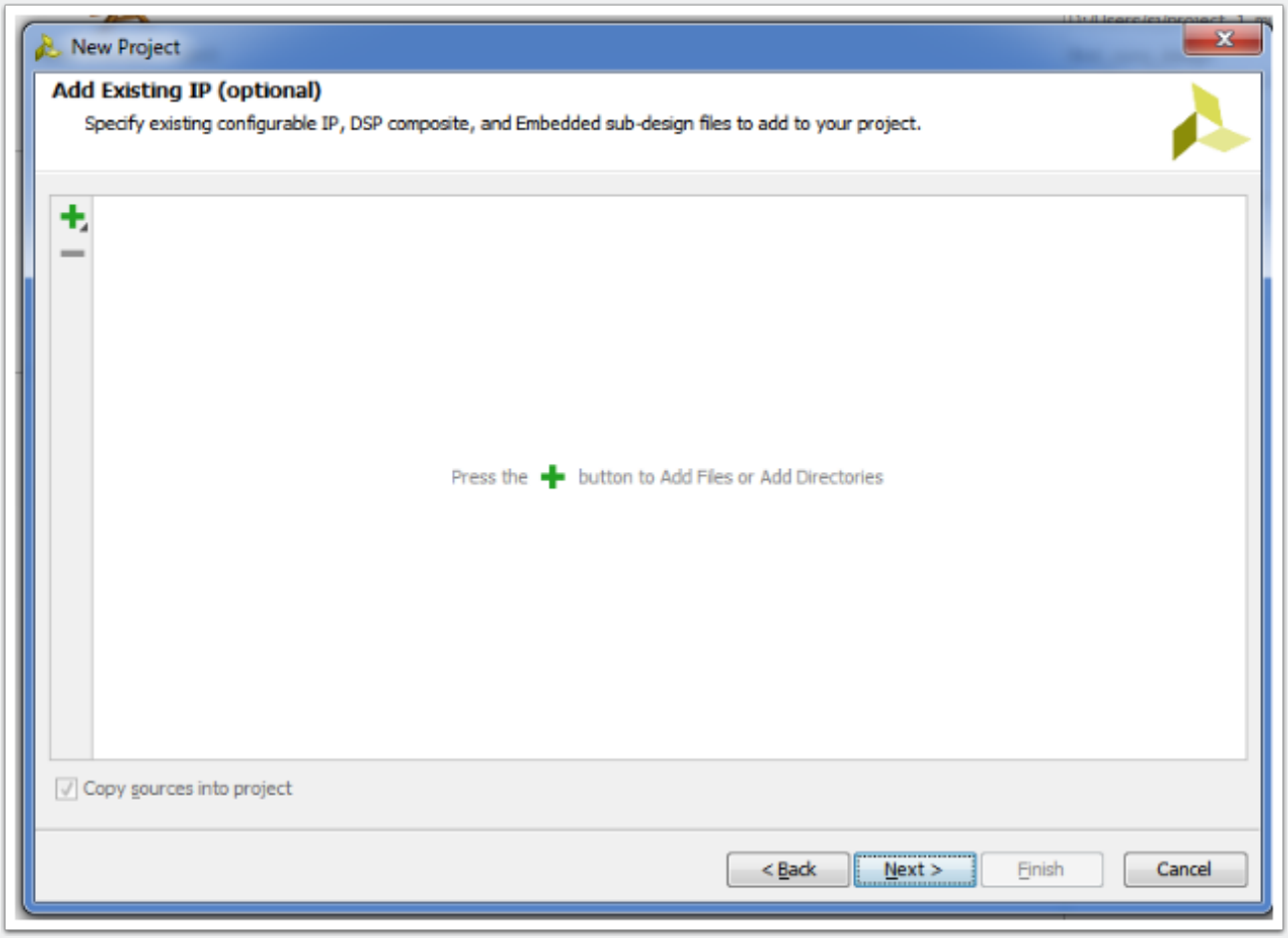
Create Source File

Set Filename to **gates2**. Keep the rest unchaged. Press OK. Press Next.



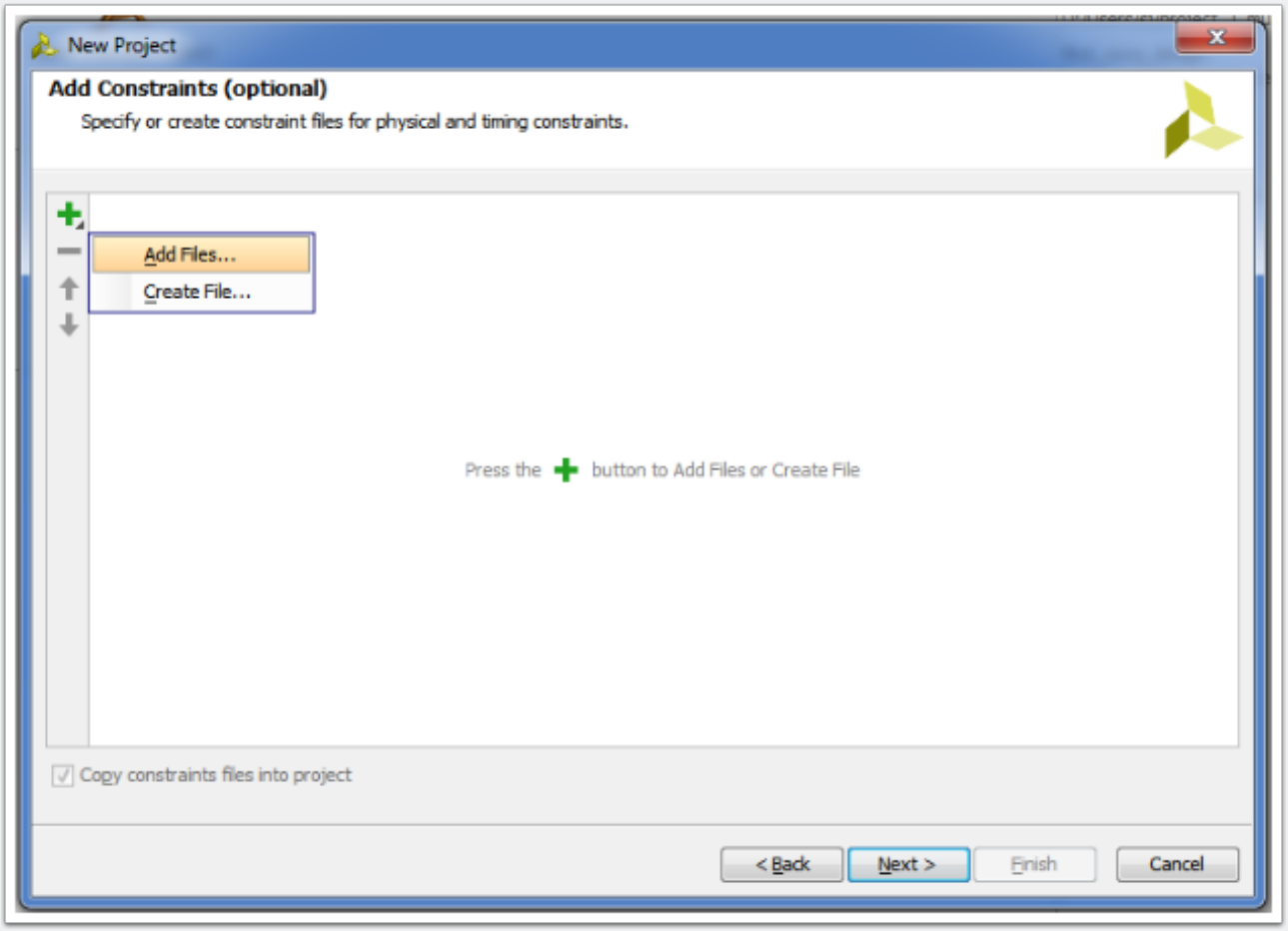
Add Existing IP

Click Next.

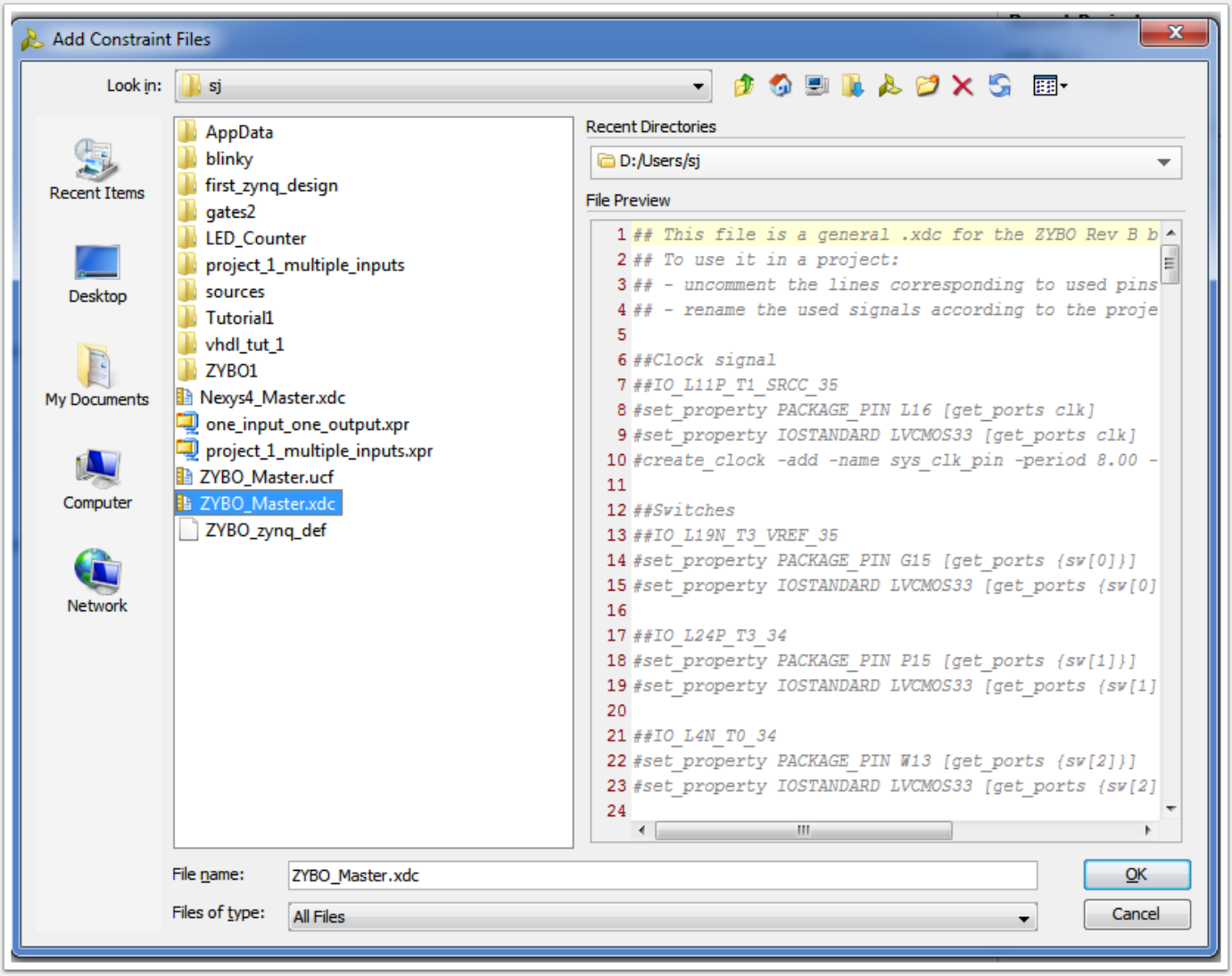


Add Constraints

Click "+", Add Files.

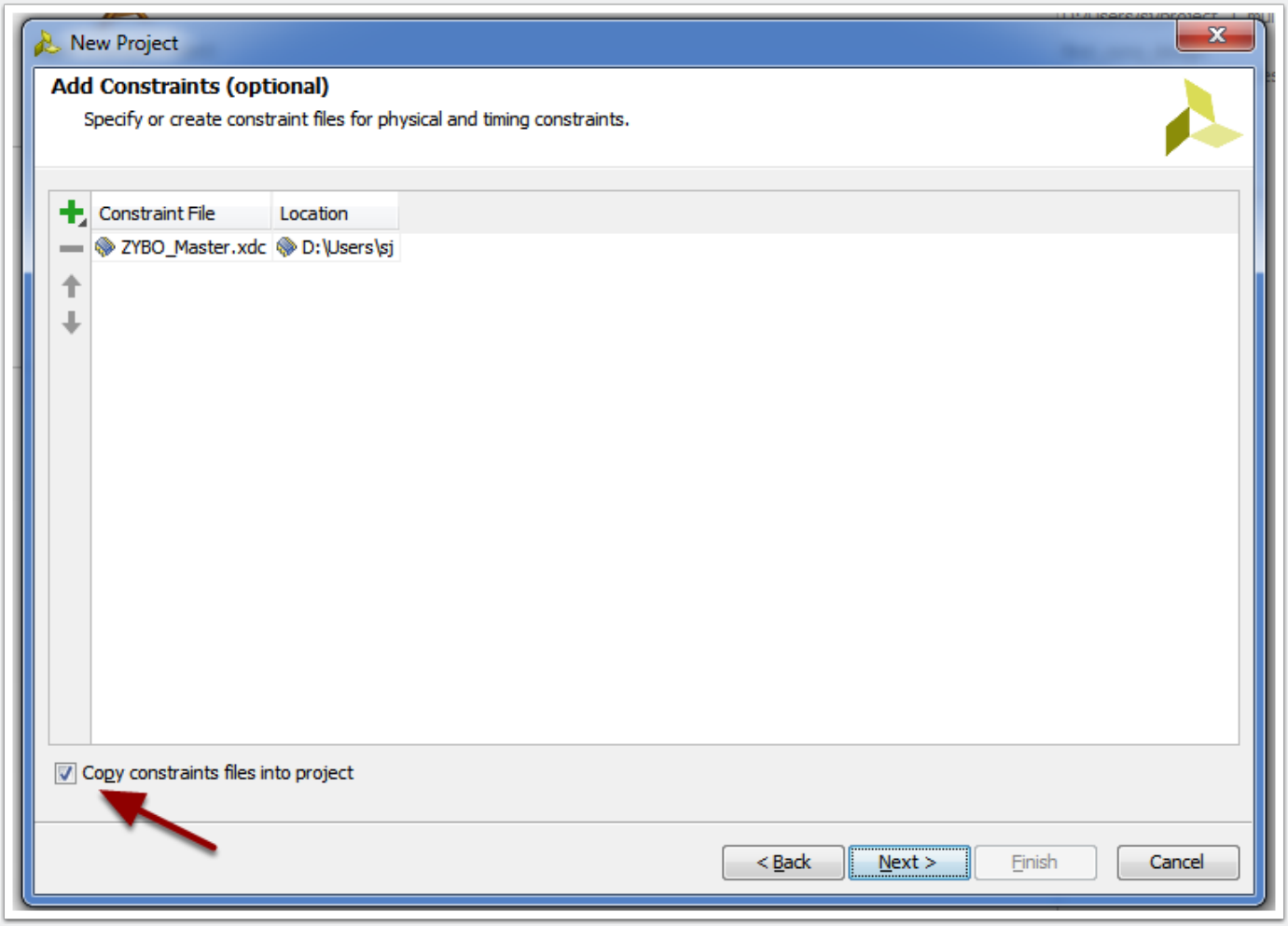


Add Constraint file we downloaded at Precondition step.



Make sure: Copy constraints files into project - Checked.

Click - Next

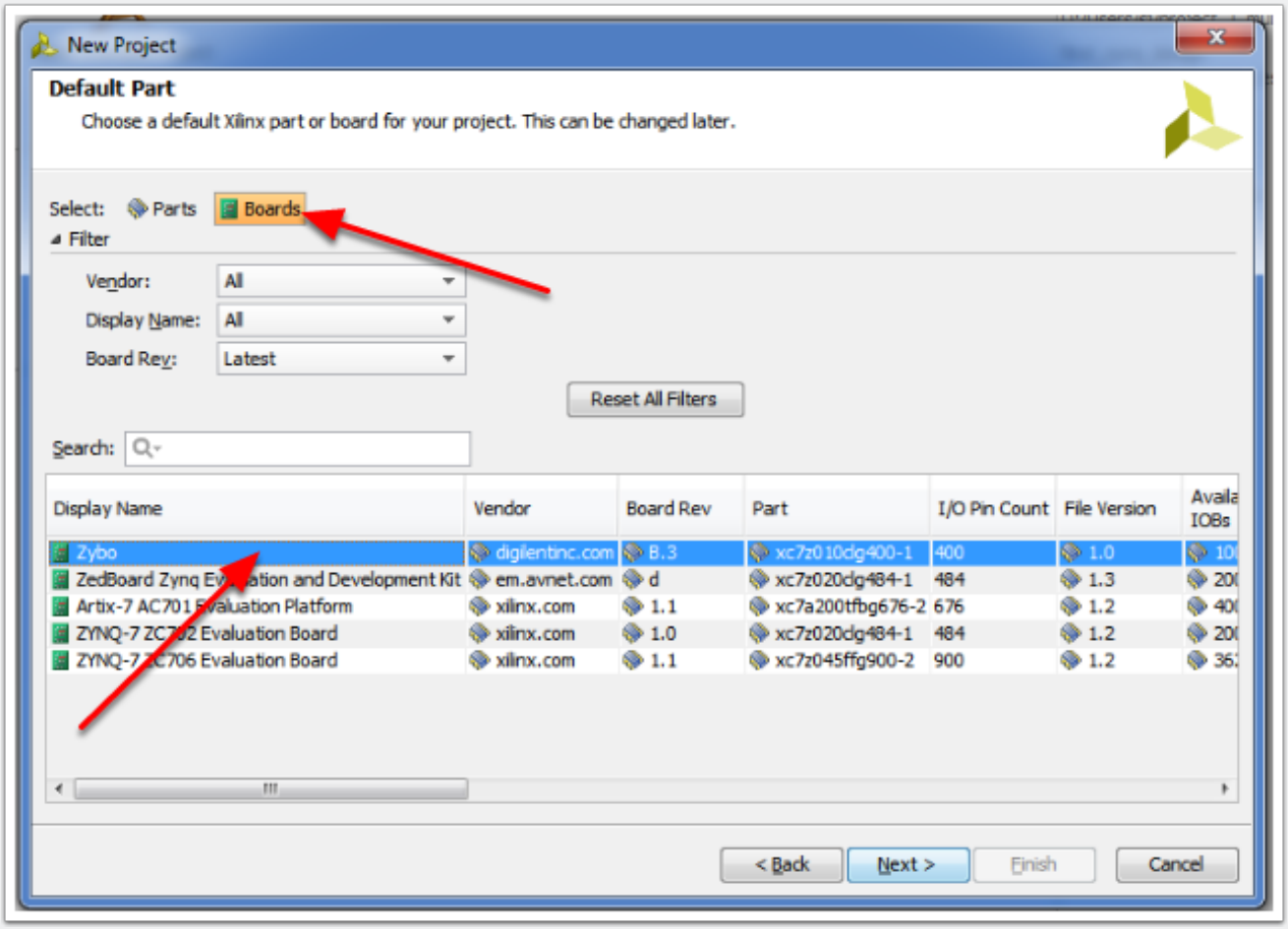


Default Part

Click on boards and select Zybo. If you still don't have it follow steps in Preconditions: Adding Zybo board to Vivado.

If you don't see ZYBO goto Preconditions Step.

Next.



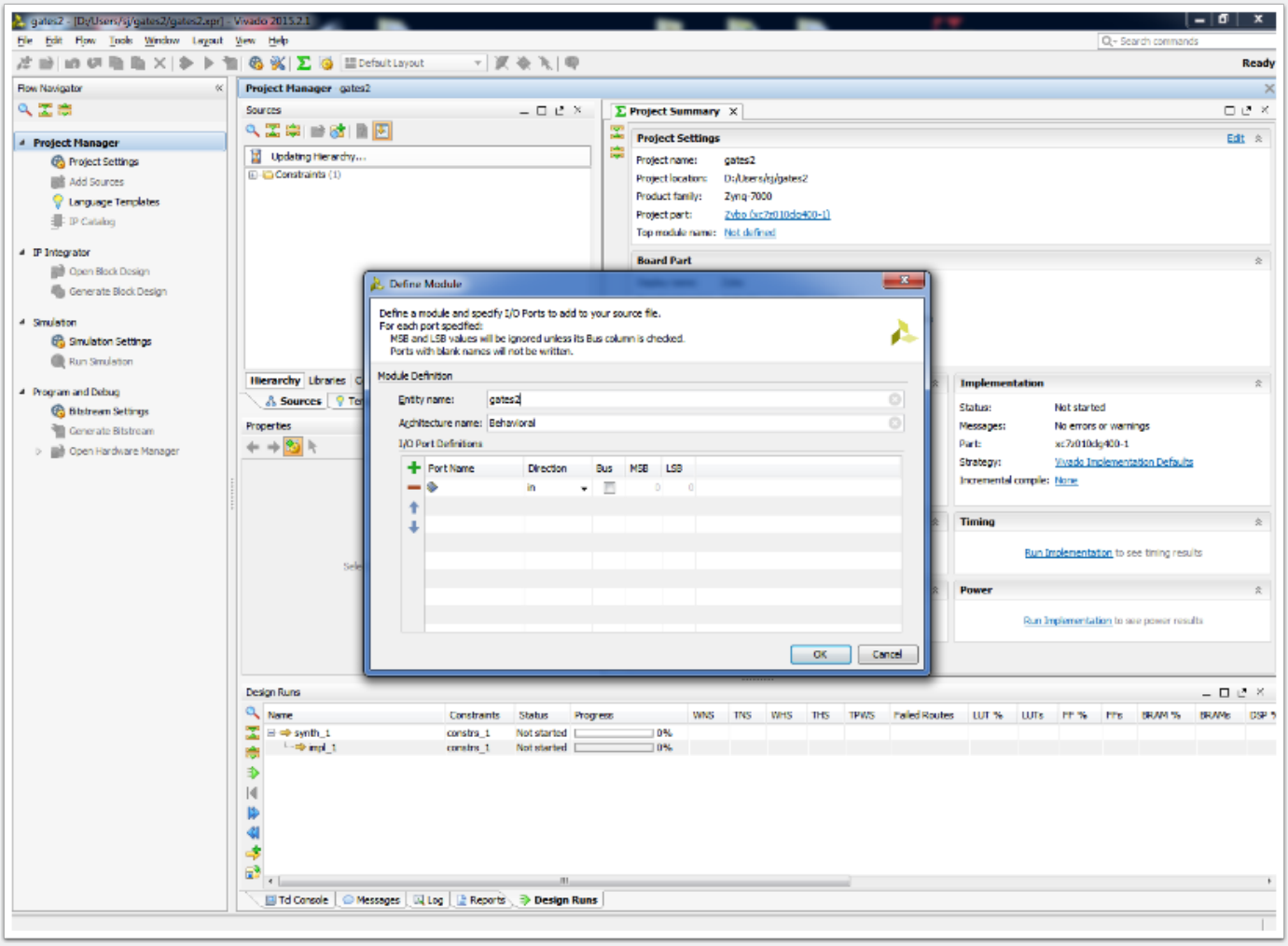
New Project Summary

Finish

Phase 2. Editing Project

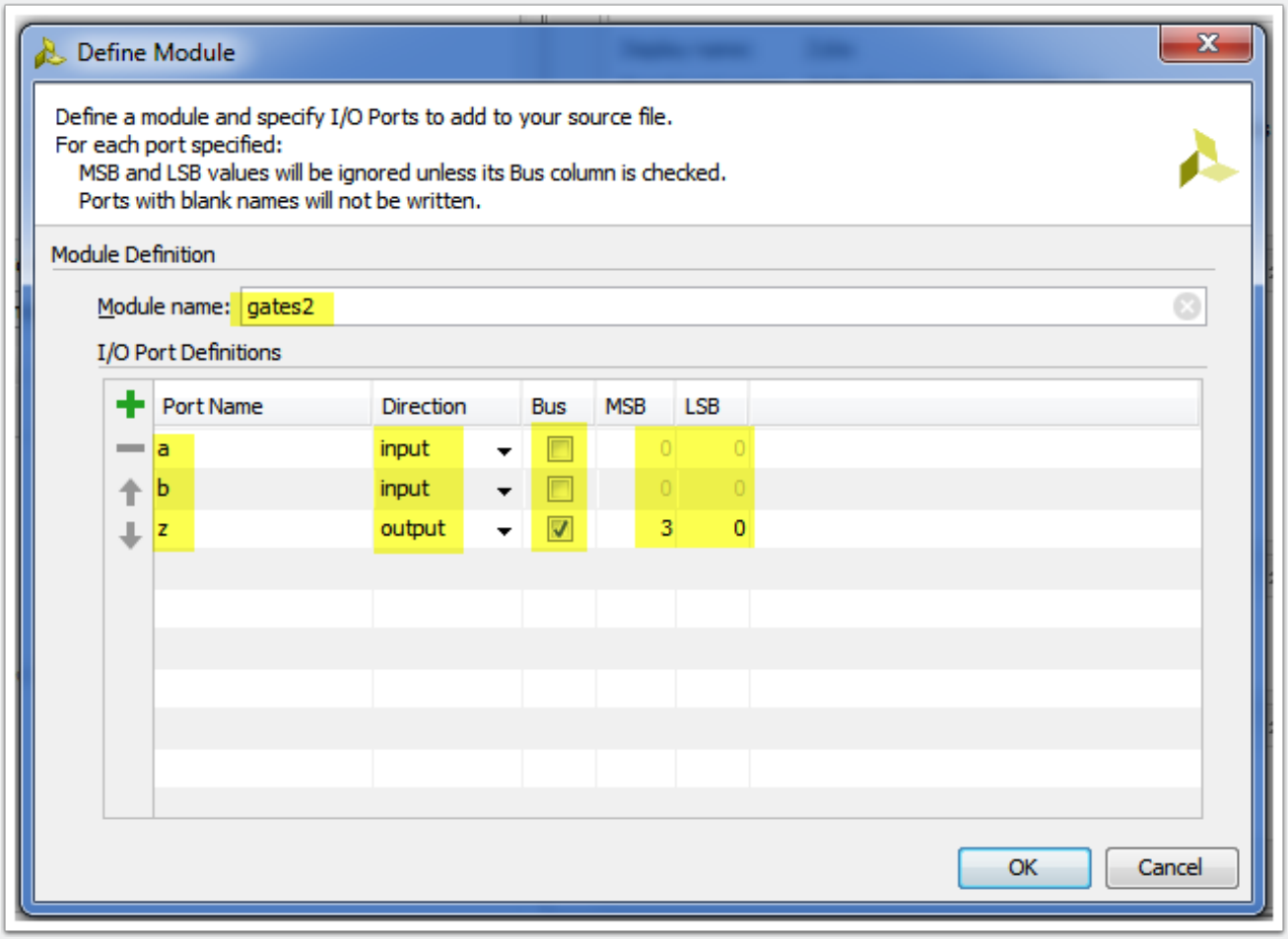
Project files generated and ready for your design.

We will implement 2 input gates and 4 output basic gates **and**, **or**, **xor and nor.**



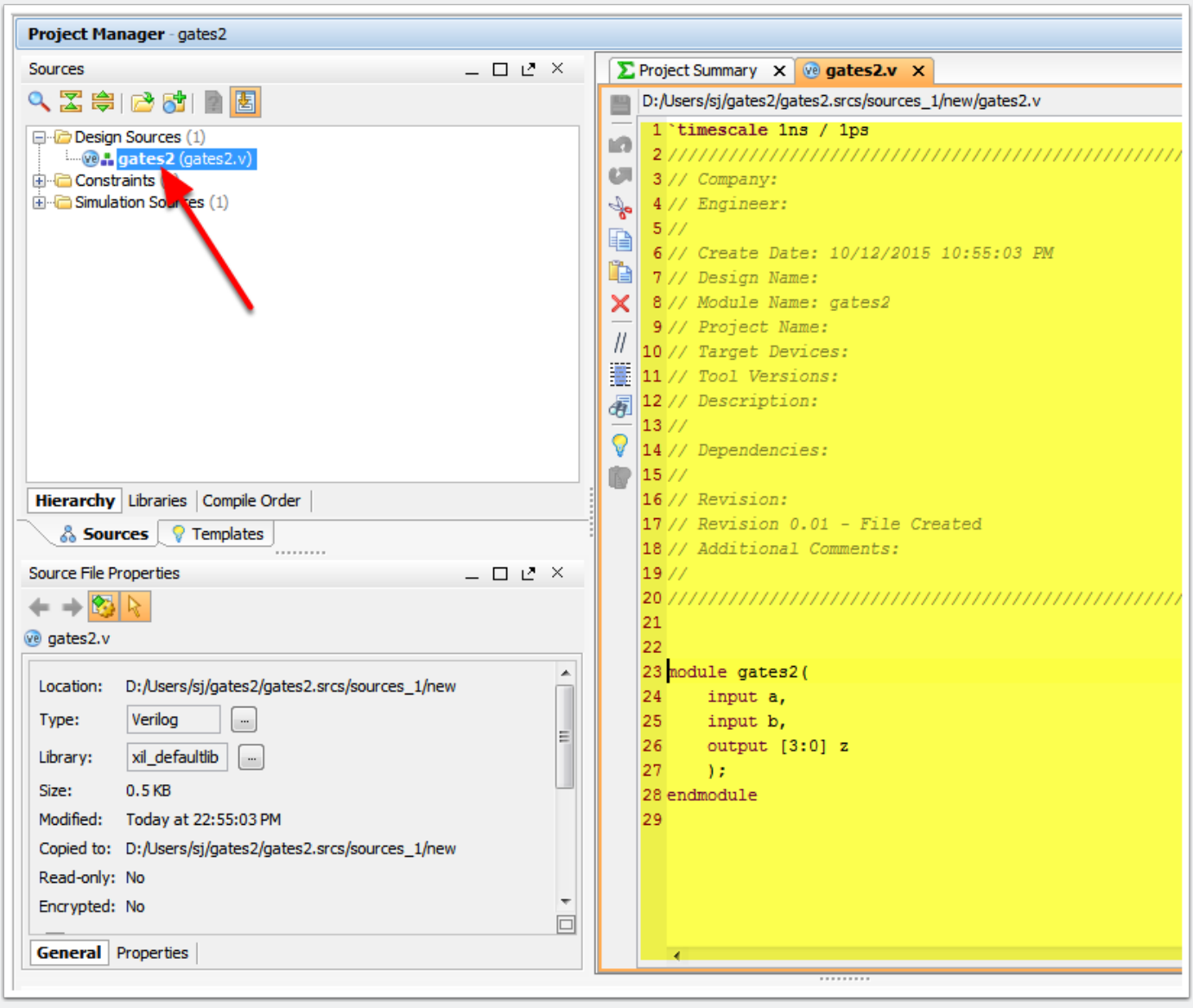
Define I/O ports as below

OK


Define Module
Define a module and specify I/O Ports to add to your source file.
For each port specified:
MSB and LSB values will be ignored unless its Bus column is checked.
Ports with blank names will not be written.
Module Definition
Module name: gates2
I/O Port Definitions
Port Name
Direction
Bus
MSB
LSB
a
input
0
0
b
input
0
0
z
output
3
0
OK
Cancel

Select Verilog Design

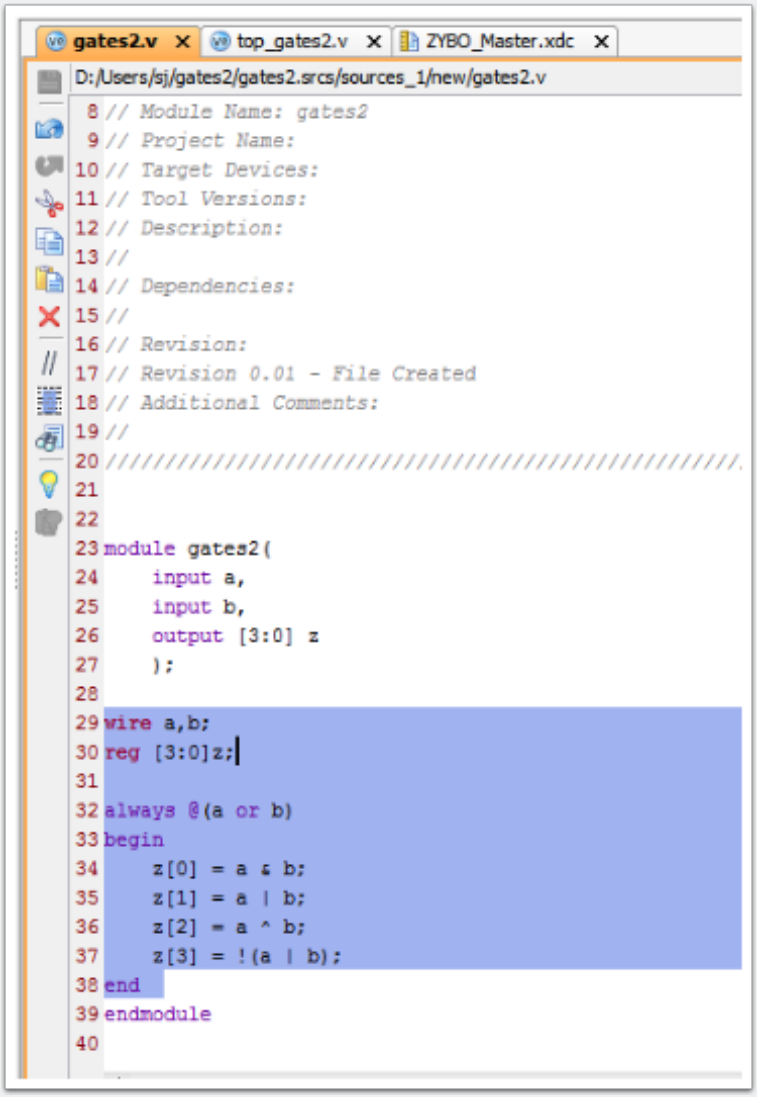
Click on Source file in Project Manager>Sources>Design Sources - Source code on Right-hand side should appear.



Changes to source code.

Modify Verilog file - add lines as highlighted below.

```
wire a,b;
reg [3:0]z;
always @(a or b)
begin
   z[0] = a & b;
   z[1] = a | b;
   z[2] = a ^ b;
   z[3] = !(a | b);
end
```

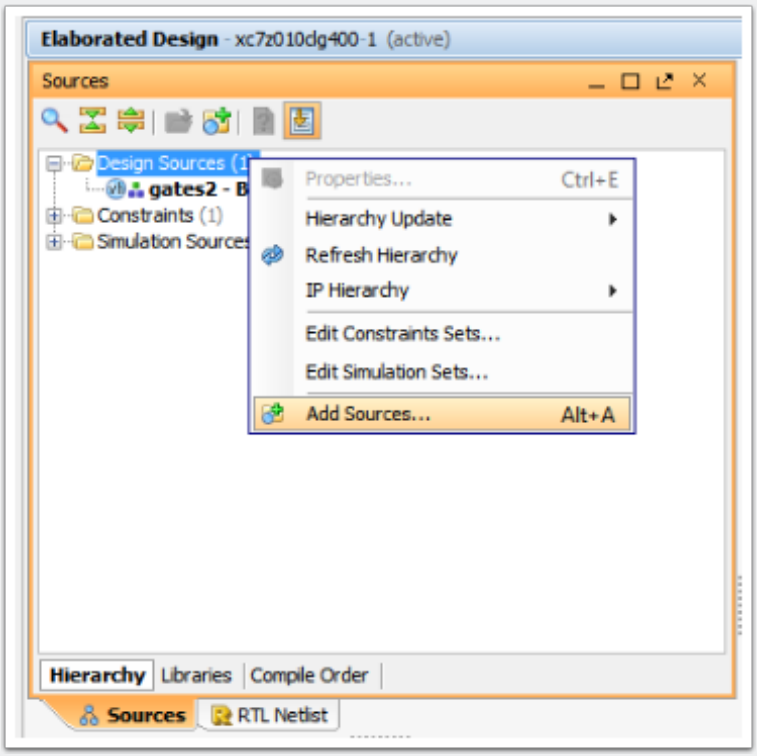


Create top file

Rightclick on Design Sources and select Add Sources.

1. Add or create design souces.

2. "+" > Create File

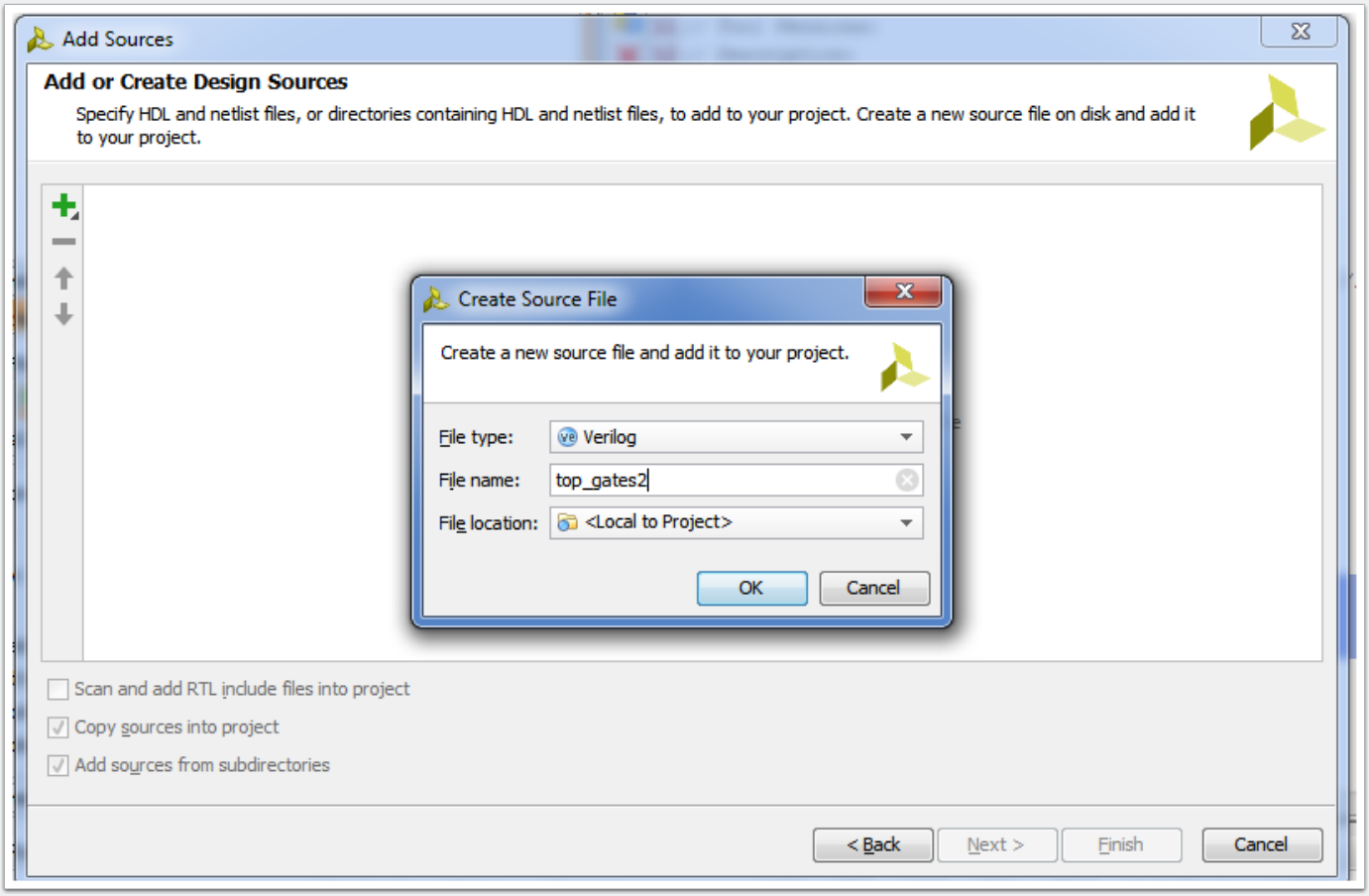


File Type :Verilog,

File name: top_gates2

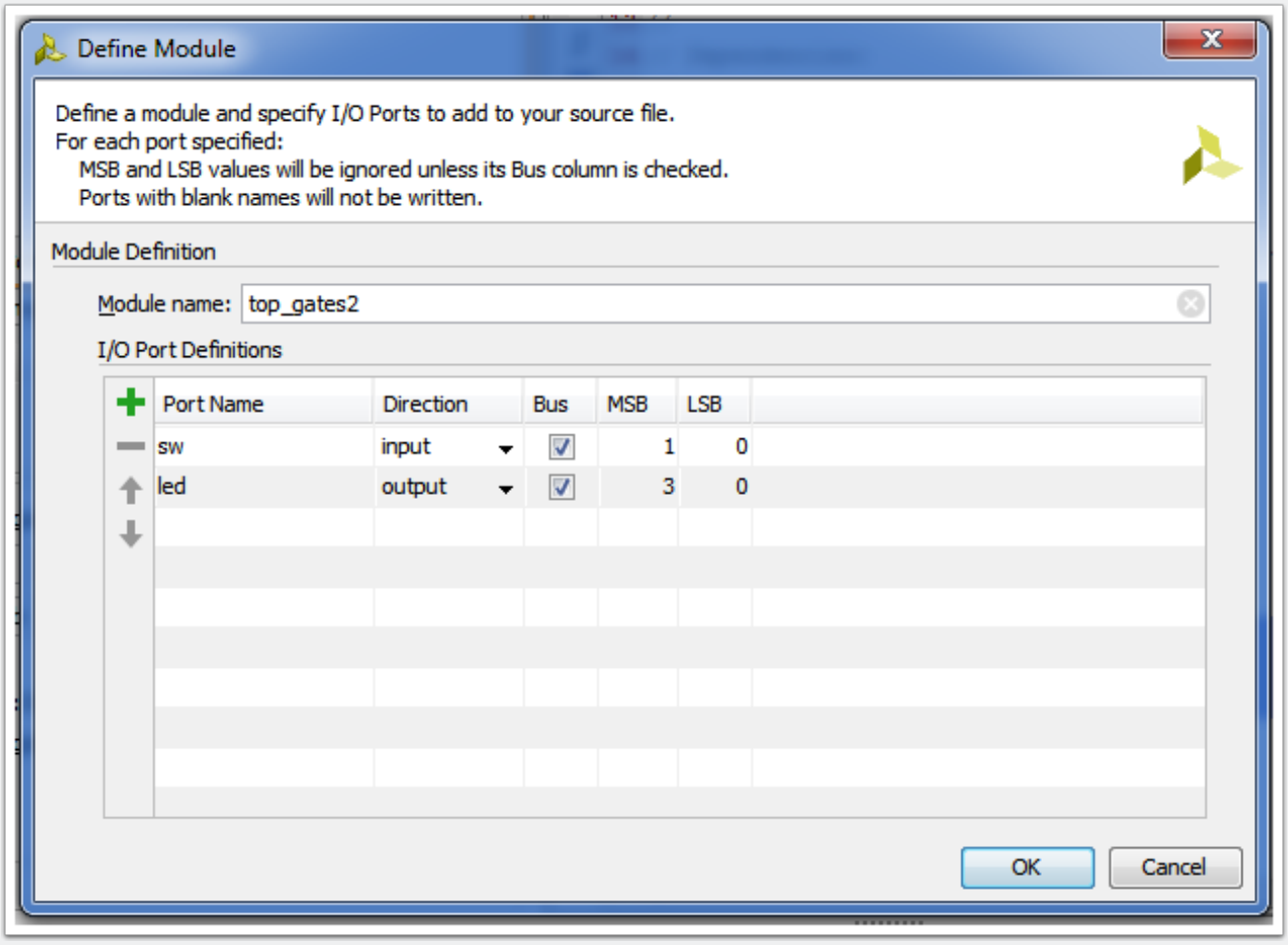
OK

Finish



Define Module

Add sw and led as on image below.

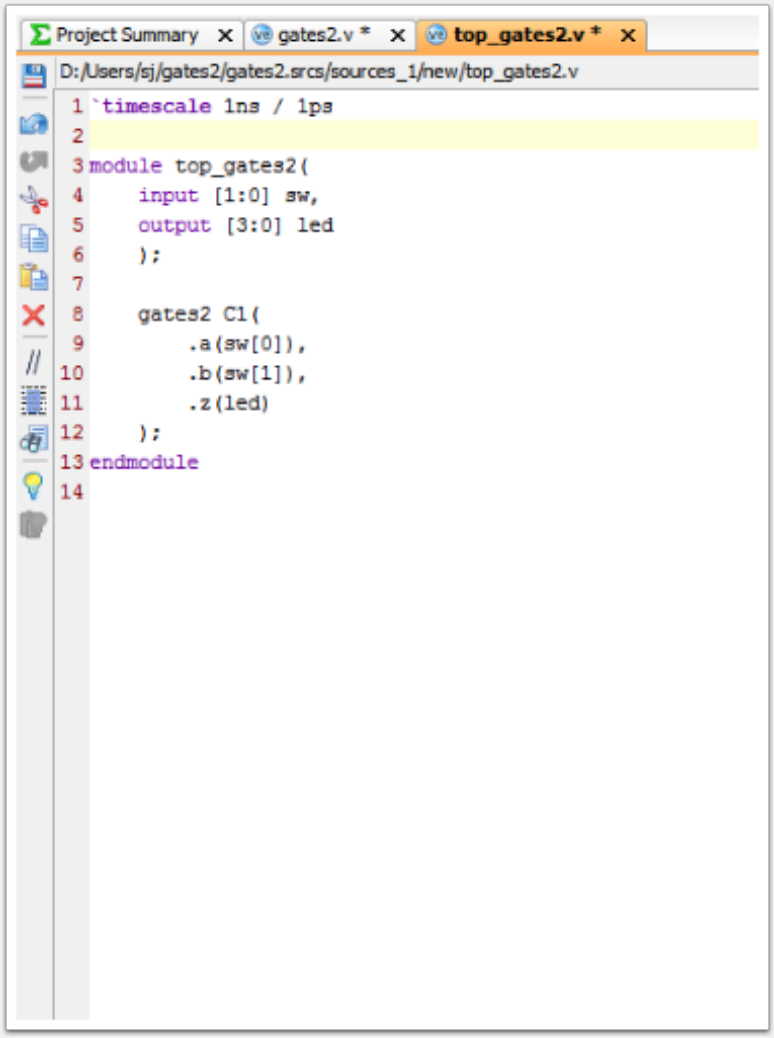


Replace default source code.

```
`timescale 1ns / 1ps
module top_gates2(
    input [1:0] sw,
    output [3:0] led
```

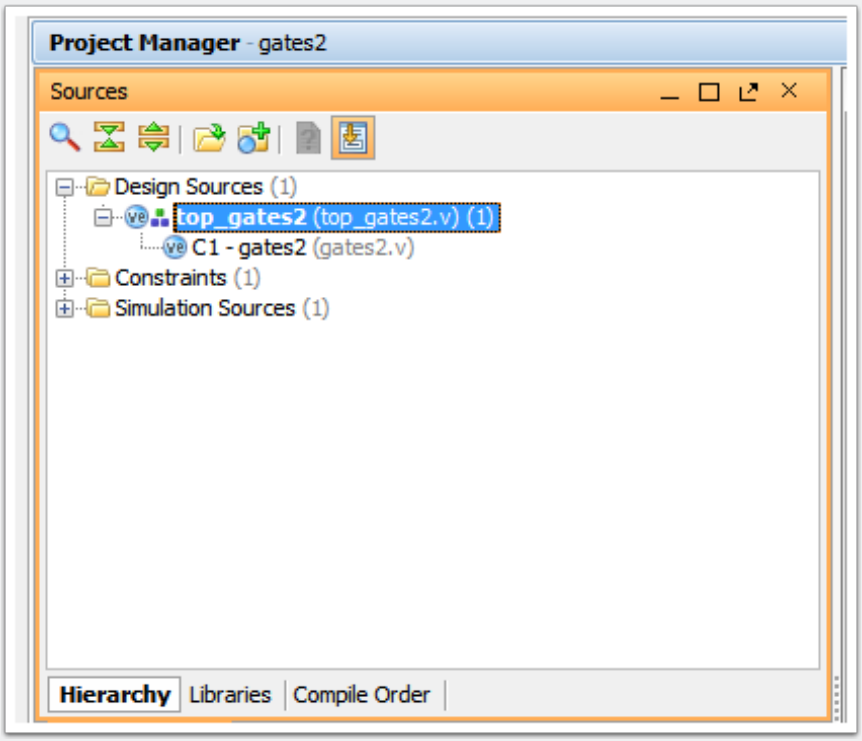
```
    );

    gates2 C1(
        .a(sw[0]),
        .b(sw[1]),
        .z(led)
    );
endmodule
```



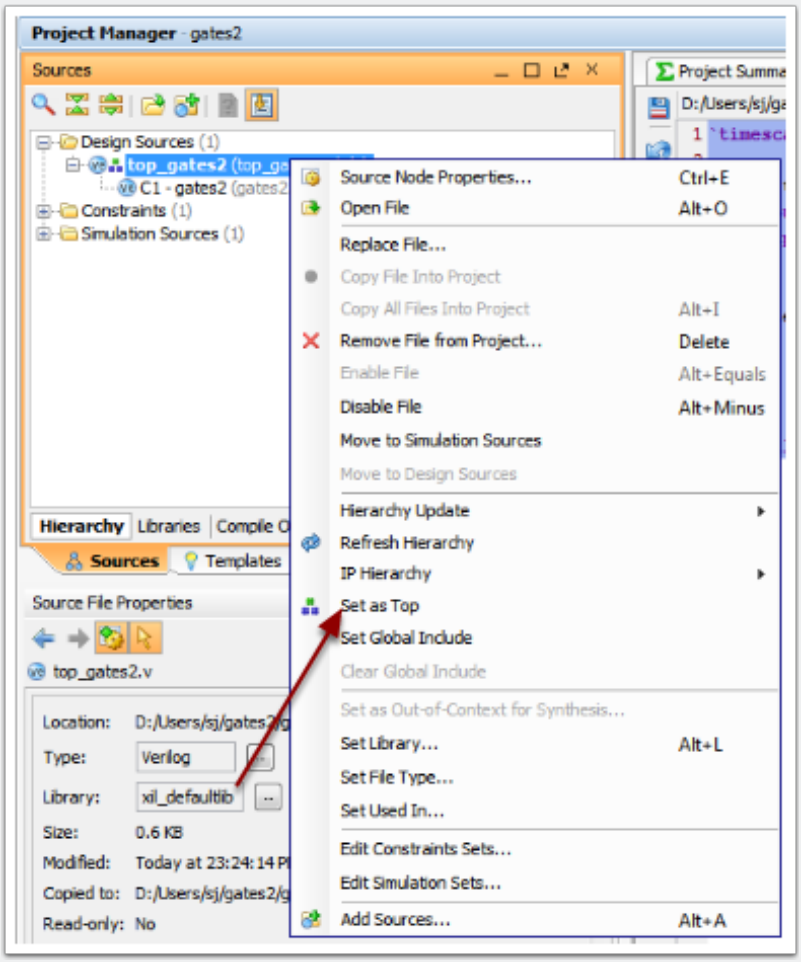
Top Design

We have single top design interface file which use our gates2 design as component.



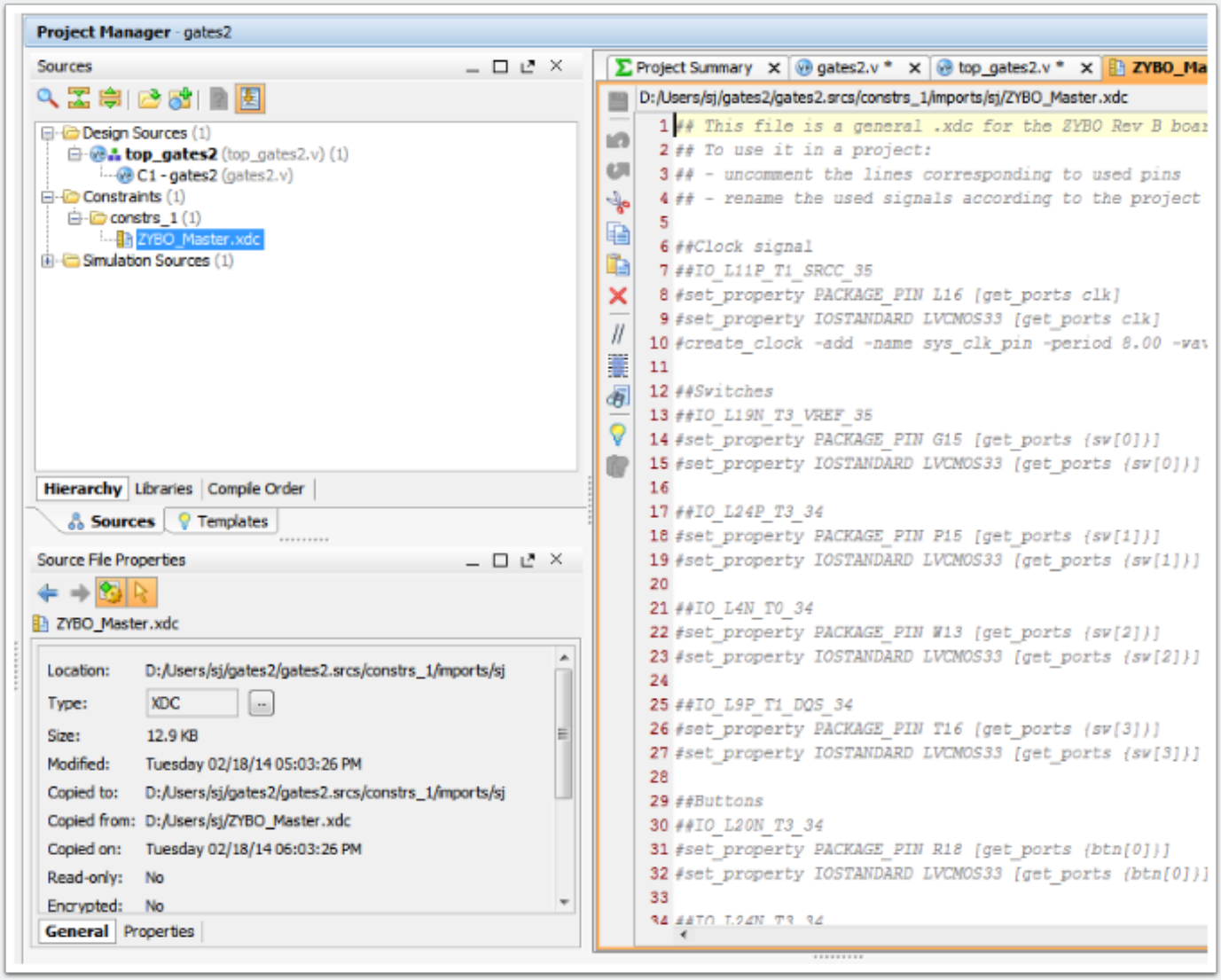
top design

Make sure our top file became parent of gates2 file. Otherwise set it manually with **Set as Top**.



Amend Constraints file

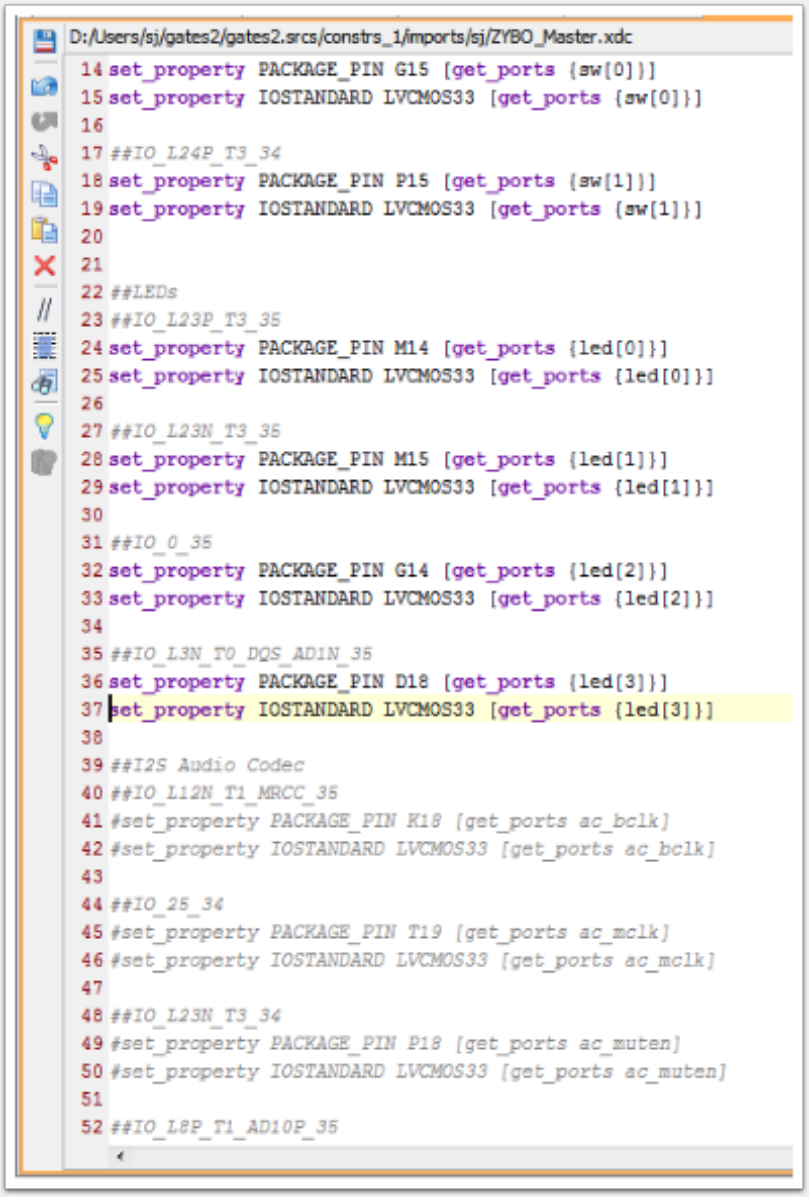
Select xdc file from Sources>Constraints



Changes in xdc file

Uncomment lines of I/O ports we need to use.

Save file.

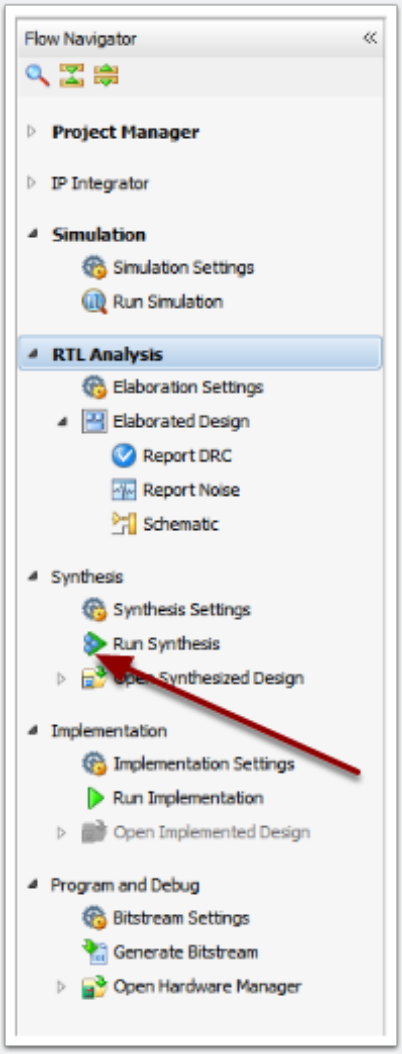


Phase 3 - Synthesis and uploading to device.

At Synthesis phase we convert our circuit from register transfer level (RTL) into a design implementation in terms of logic gates.

In Flow Navigator on Lefthand side.:

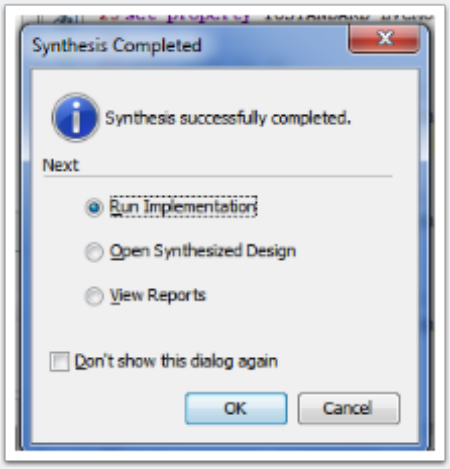
Next steps can be **Simulation**>**Run Simulation** or **RTL Analysis>Schematic** but we skip them in this tutorial and come directly to **Synthesis>Run Synthesis**.



Synthesis complention

Leave default Run Implementation

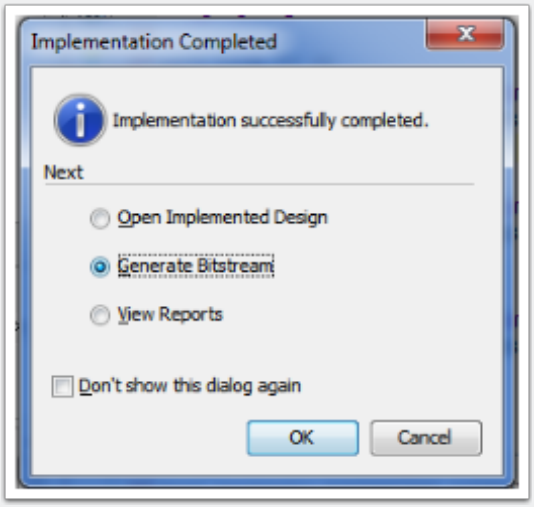
OK



Generate Bitstream

Select Generate Bitstream

OK



Final

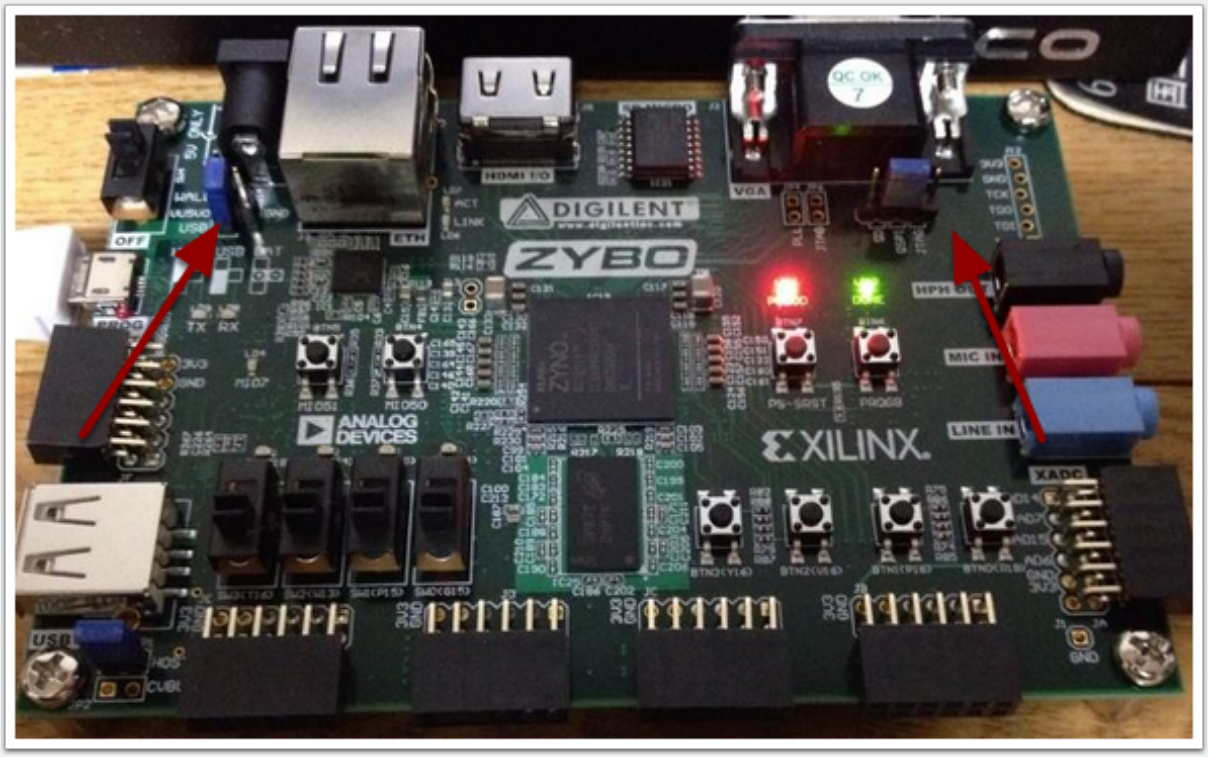
Pay attention to jumpers.

JP7 - It should set to USB.

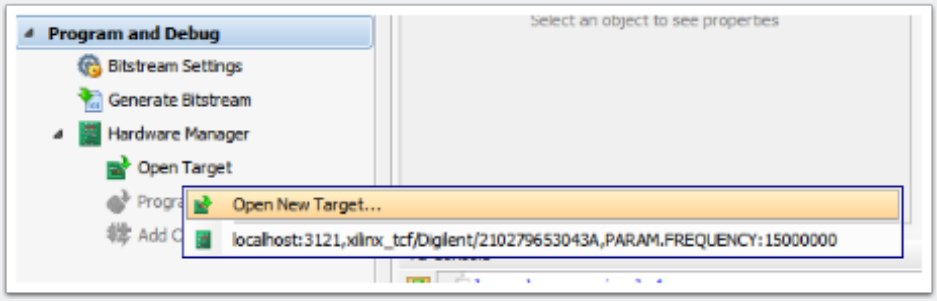
JP5 can be JTAG or QSPI

Connect ZYBO to PC with Micro-USB cable.

Photo taken from http://marsee101.blog19.fc2.com/blog-entry-2745.html

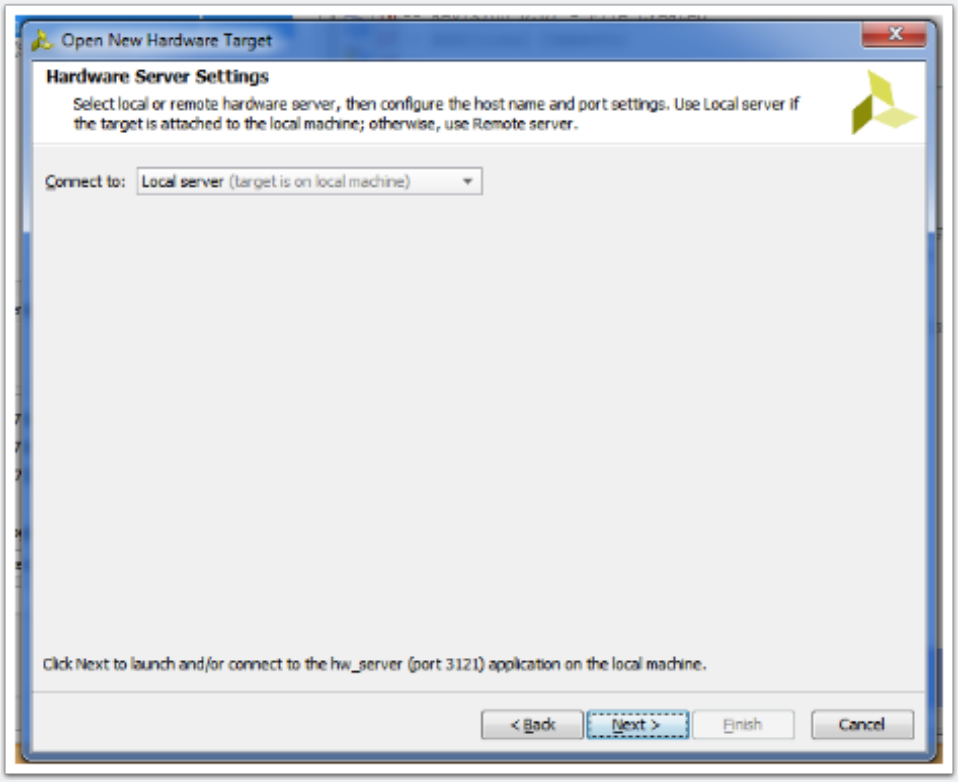


Program ZYBO



Next

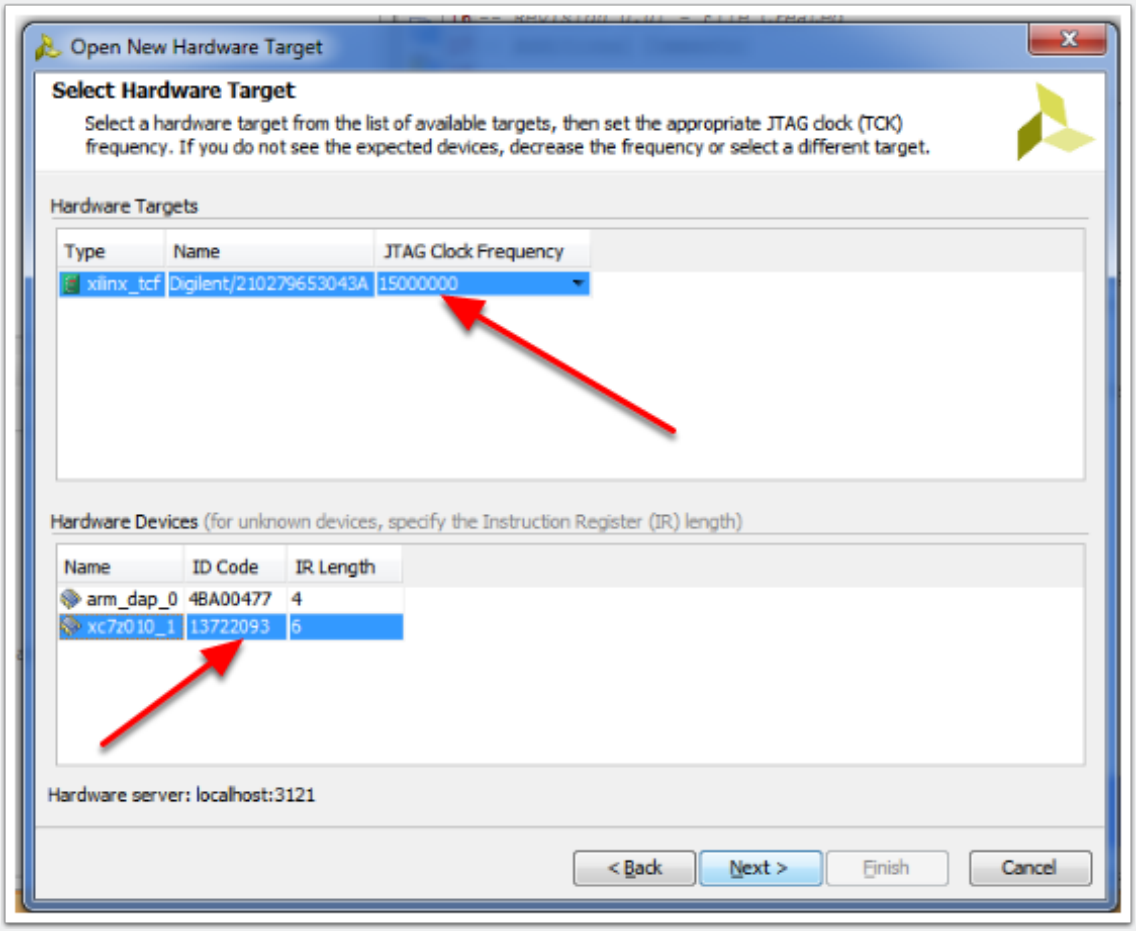
Next


Open New Hardware Target
Hardware Server Settings
Select local or remote hardware server, then configure the host name and port settings. Use Local server if the target is attached to the local machine; otherwise, use Remote server.
Connect to:
Local server (target is on local machine)
Click Next to launch and/or connect to the hw_server (port 3121) application on the local machine.
< Back
Next >
Finish
Cancel

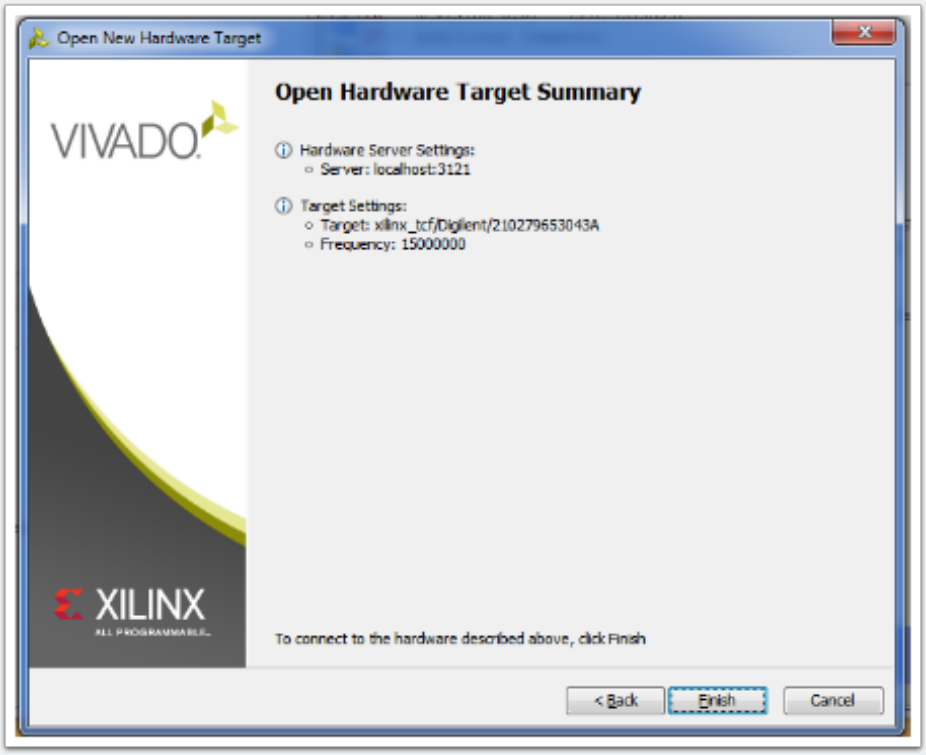
Make sure you have similar setting like on picture below.

Select xc7z010_1

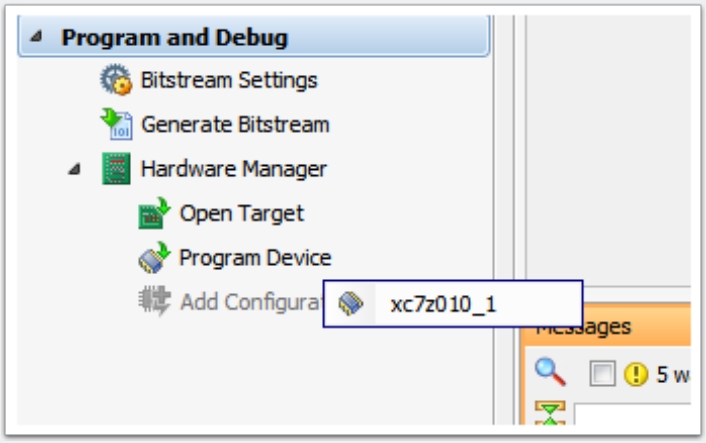
Next



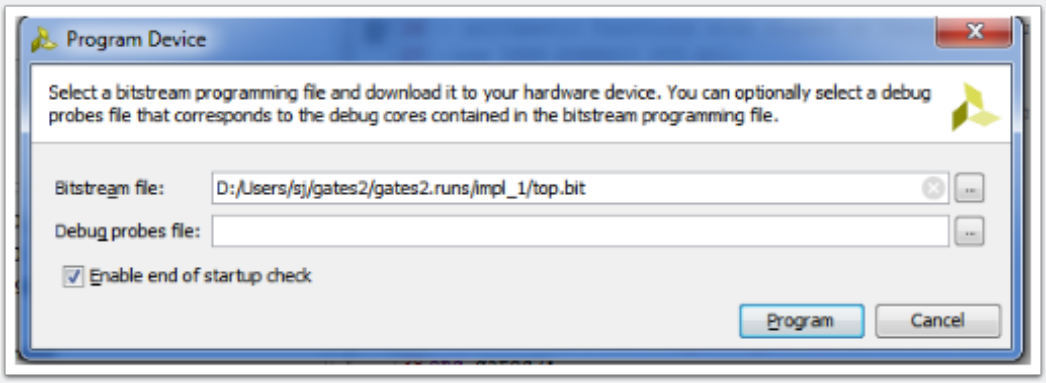
Finish



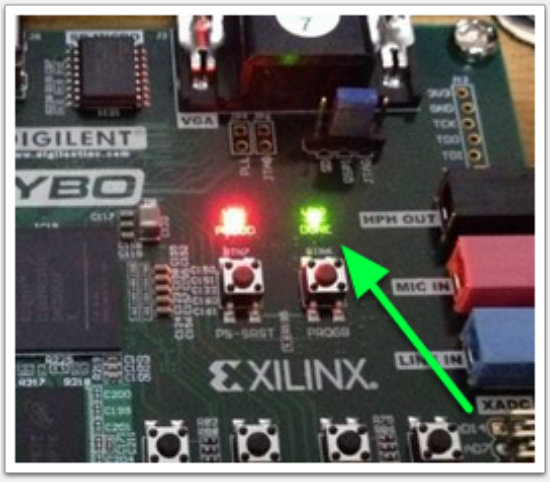
Program device > xc7z010_1



Program



As confirmation of successfull upload Greed Led will set



Use switches to confirm **and**, **or**, **xor** and **nor** operations.

Archive of project available.

PDF version of this lesson available.

Reference

1. http://www.slideshare.net/MaryalaSrinivas/verilog-tutorial

2. http://www.instructables.com/id/Learn-Verilog-A-Brief-Tutorial-Series-on-FPGA-Desi/?ALLSTEPS

3. The ZYNQ BOOK - Make sure you download not only book archive but also tutorials book with sources.

4. HDL Chip Design- A Practical Guide for Designing, Synthesizing and Simulating ASICs and FPGAs Using VHDL or Verilog. By Douglas J. Smith

5. ZYBO Reference Manual

Files

1. Project Archive

2. ZYBO Board Definition File.

3. ZYBO Master xdc file.

Feedback

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