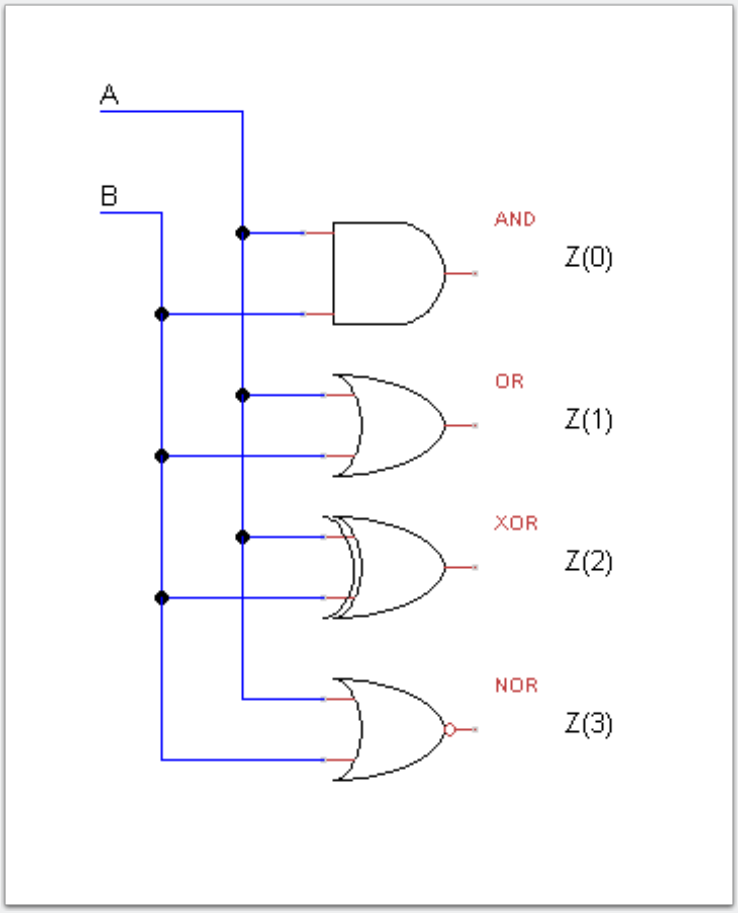
Simple VHDL example using VIVADO 2015 with ZYBO FPGA board

Aim

I am FPGA novice and want to try classical FPGA design tutorials. I bought perfect modern FPGA board ZYBO (**ZY**nq **BO**ard) based on Xilinx Z-7010 from Digilent but latest tools from Xilinx VIVADO 2015.2 more focused on AP SoC programming while I want to just pure FPGA design without any linuxes bootloaders etc. So I wrote this tutorial to help people like me :)

In this example we make simple scheme: 2 signals IN and 4 OUT.



Preconditions: Adding Zybo Board to Vivado

Vivado 2015.2 under Windows 7 64 bit was used with 16 GB of RAM.

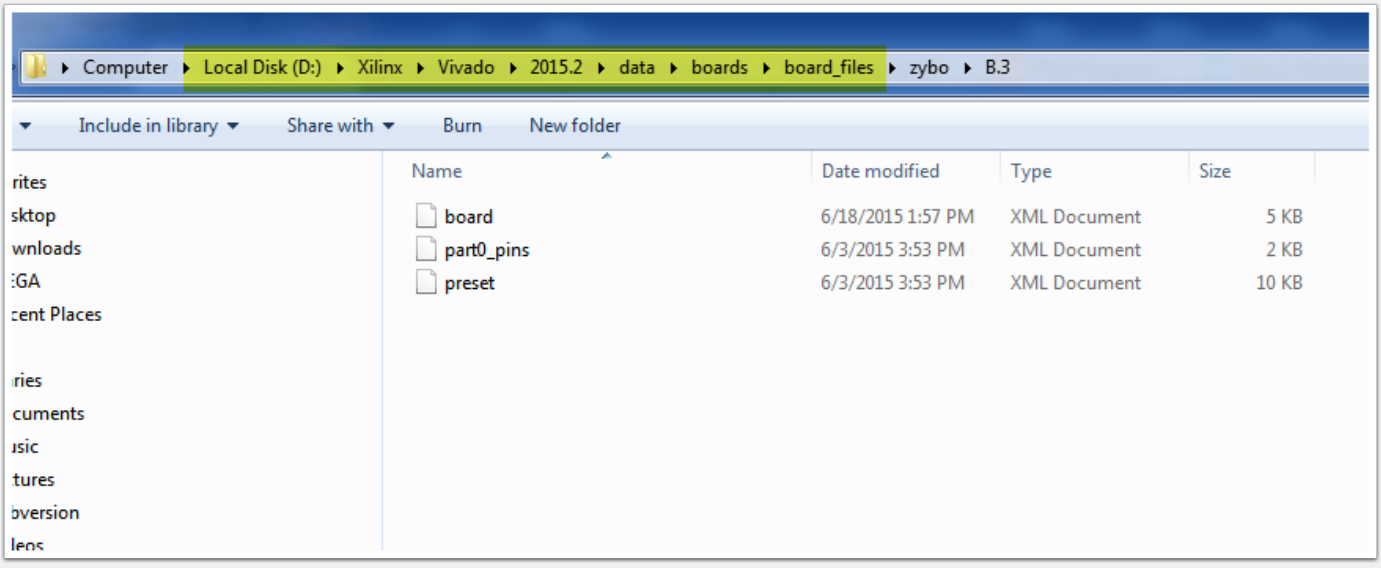
Before using Zybo with Vivado you should add Zybo Definitions File to Vivado.

1. Good source for Board Definition files is Zynqbook website.Download The_Zynq_Book_Tutorial_Sources_Aug15.zip

2. Copy **zybo** folder with content from Archive path **\sources\zybo\setup\board_part** into D:\Xilinx\Vivado\2015.2**\data\boards\board_files** (if D:\Xilinx\Vivado\2015.2 is my PC you probably have C:\Xilinx etc...)

3. In board_files you should see other boards so now our Zybo known by Vivado.

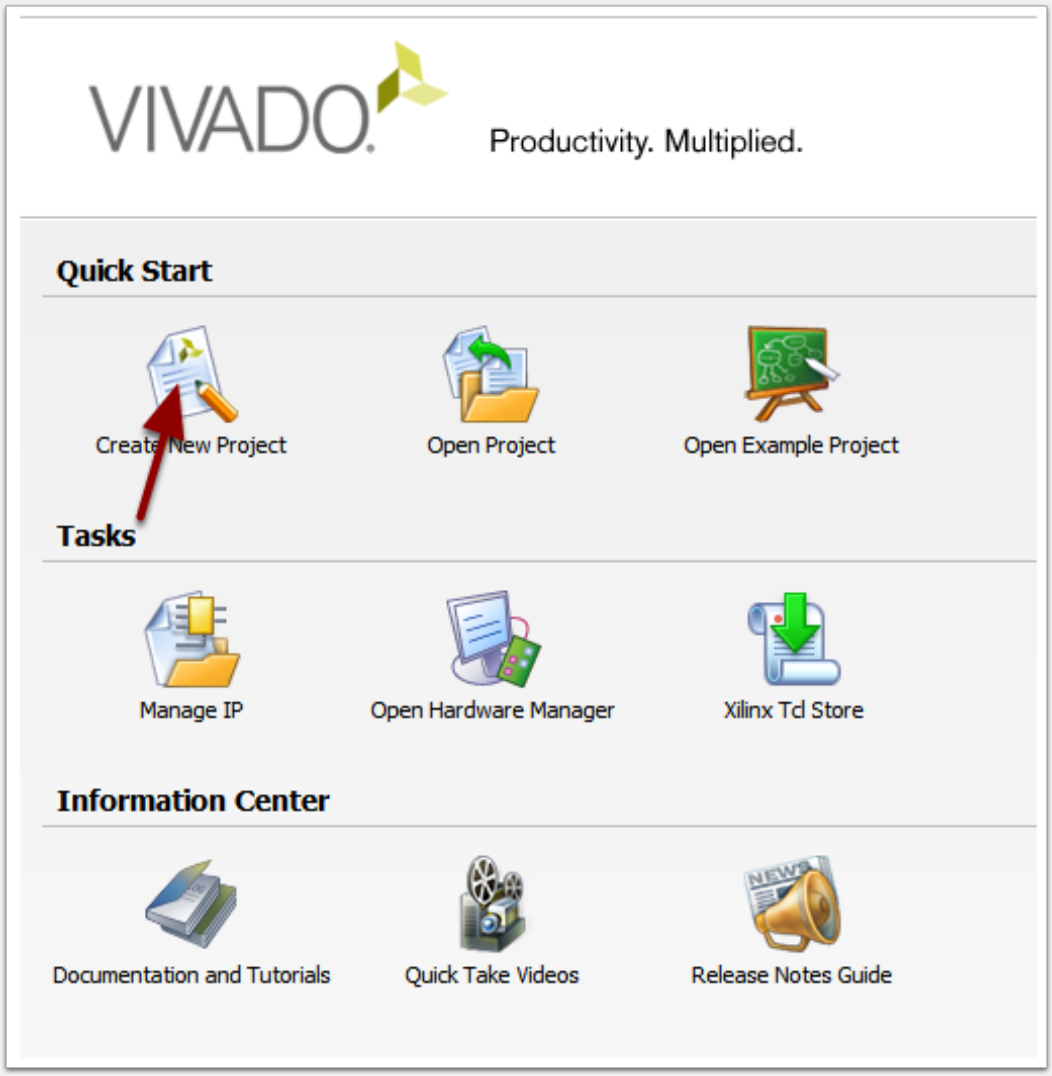
4. Download ZYBO_Master.xdc from Digilent website unpack constraints file it on local hard disk.



Launch Vivado

I have latest Vivado Design Edition from Xilinx which comes with Digilent Zybo board.

Create new project



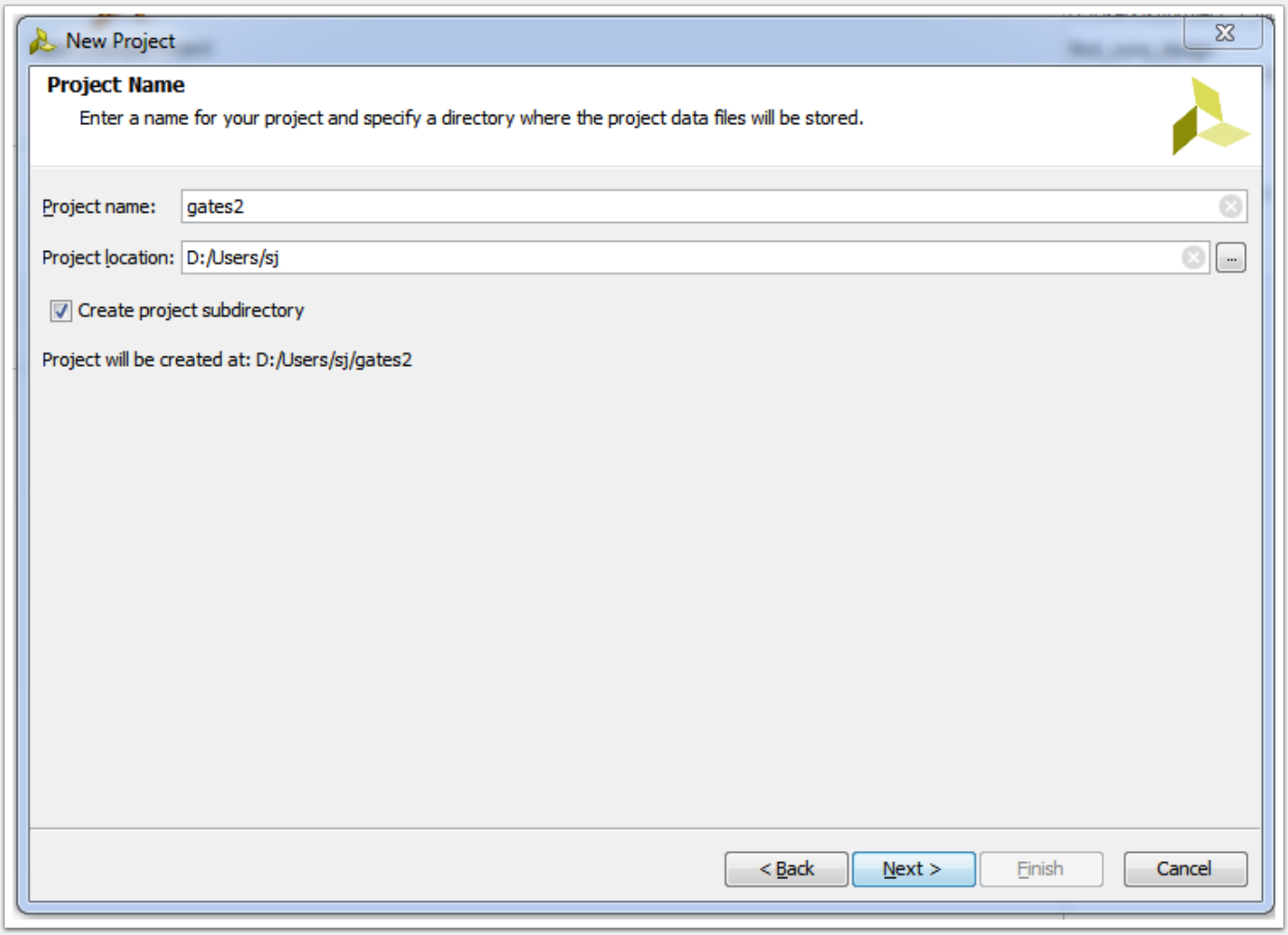
New Project

Click Next

Set project name.

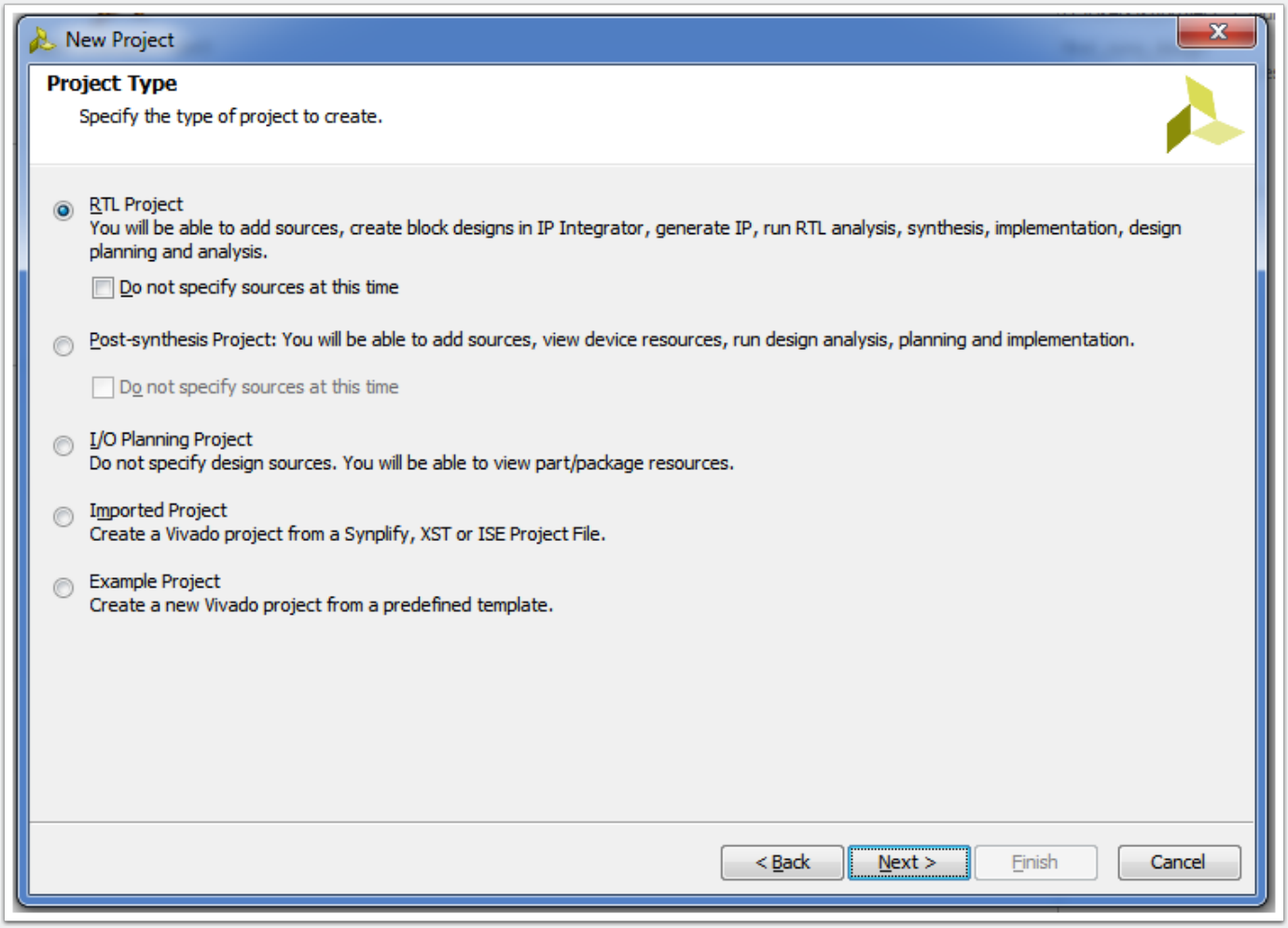
Set project name to **gates2**,

Keep rest settings unchanged unless you know what you doing.



Project Type

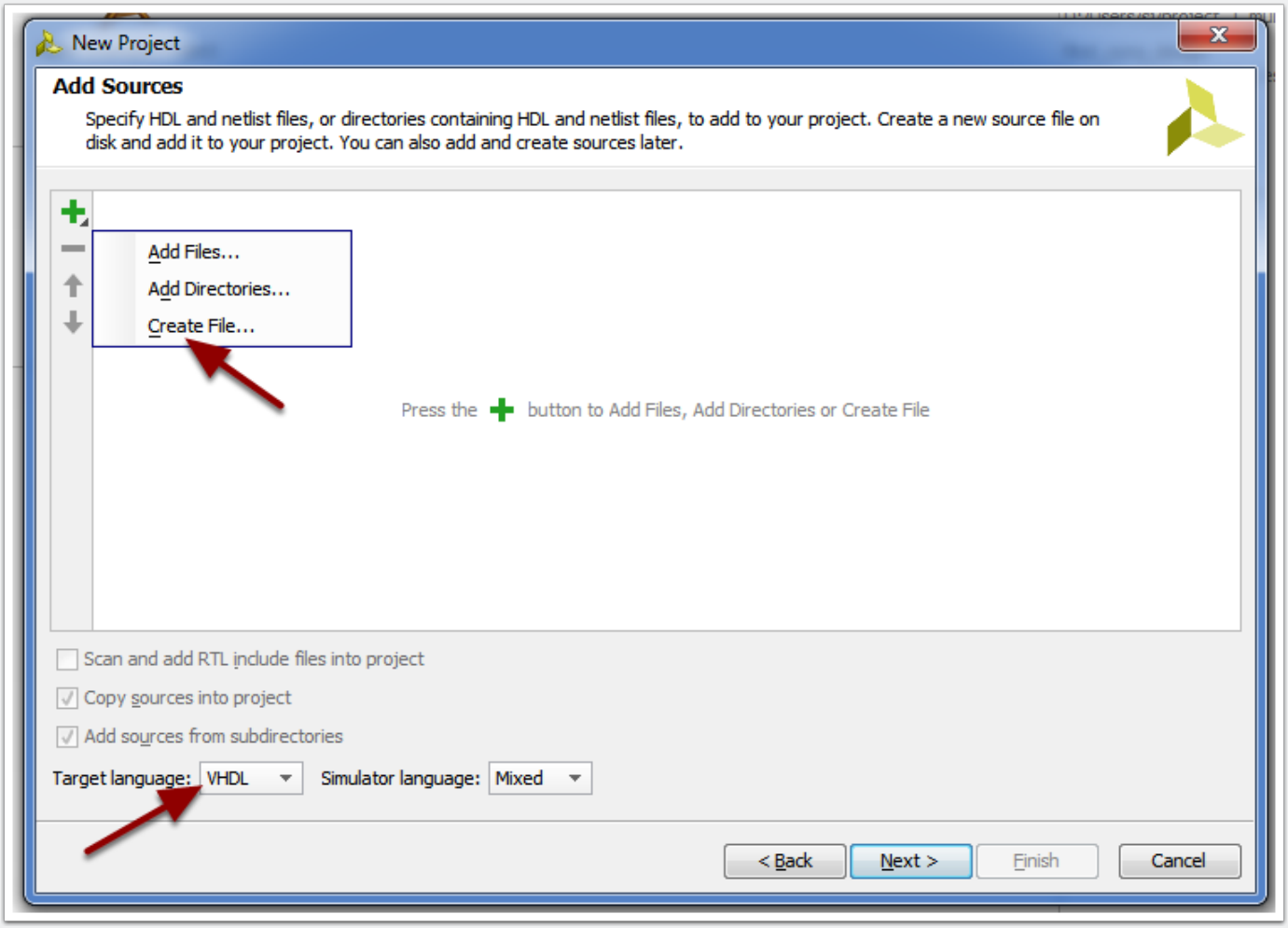
Keep default RTL project, Press Next



Add sources

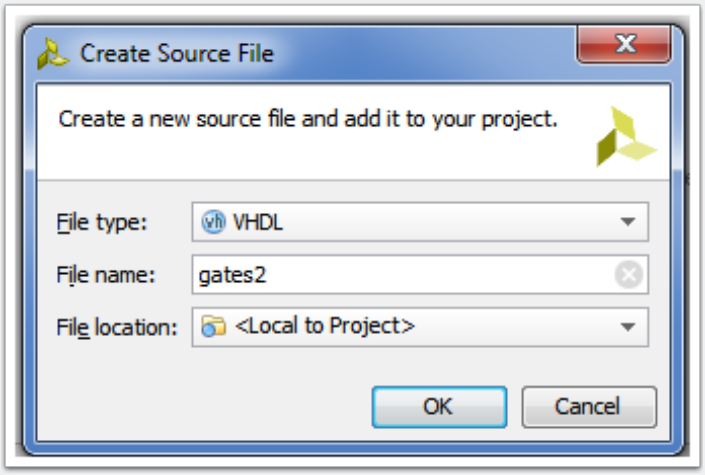
In this tutorial we decided to use VHDL language so make sure it set correctly. Simulator language you can keep unchanged.

Click on "+" - Select - Create File.



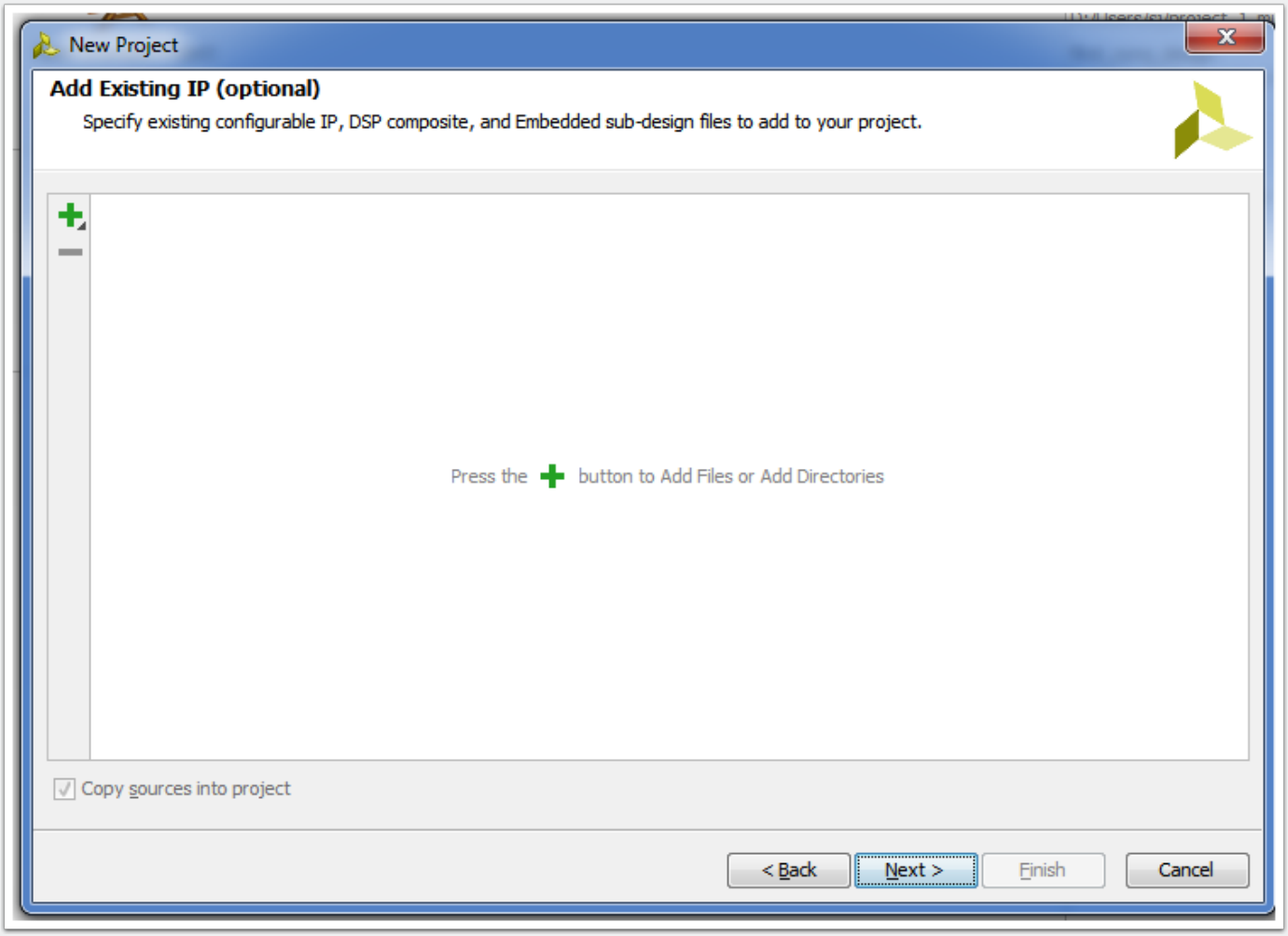
Create Source File

Set Filename to **gates2**. Keep the rest unchaged. Press OK. Press Next.



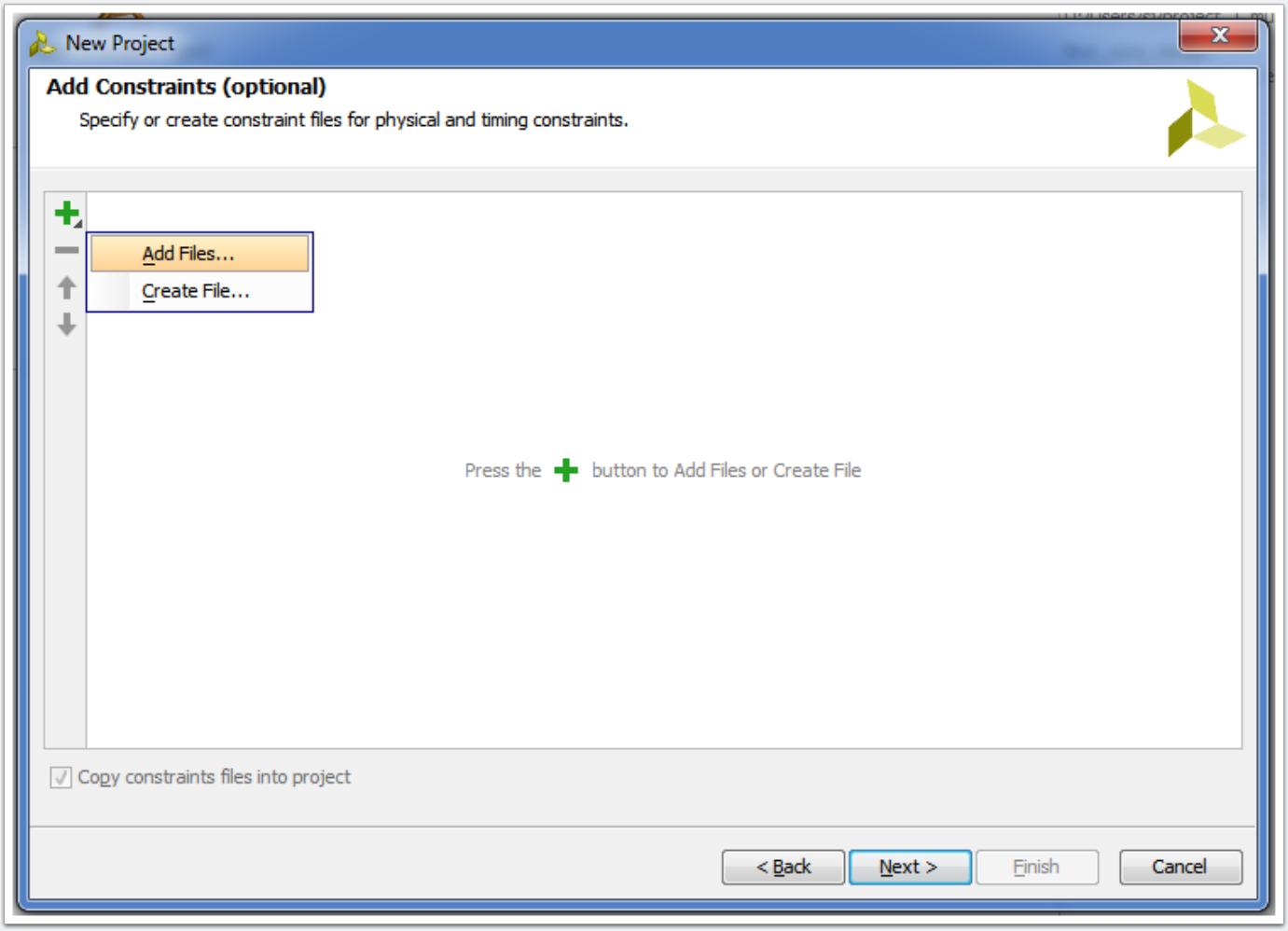
Add Existing IP

Click Next.



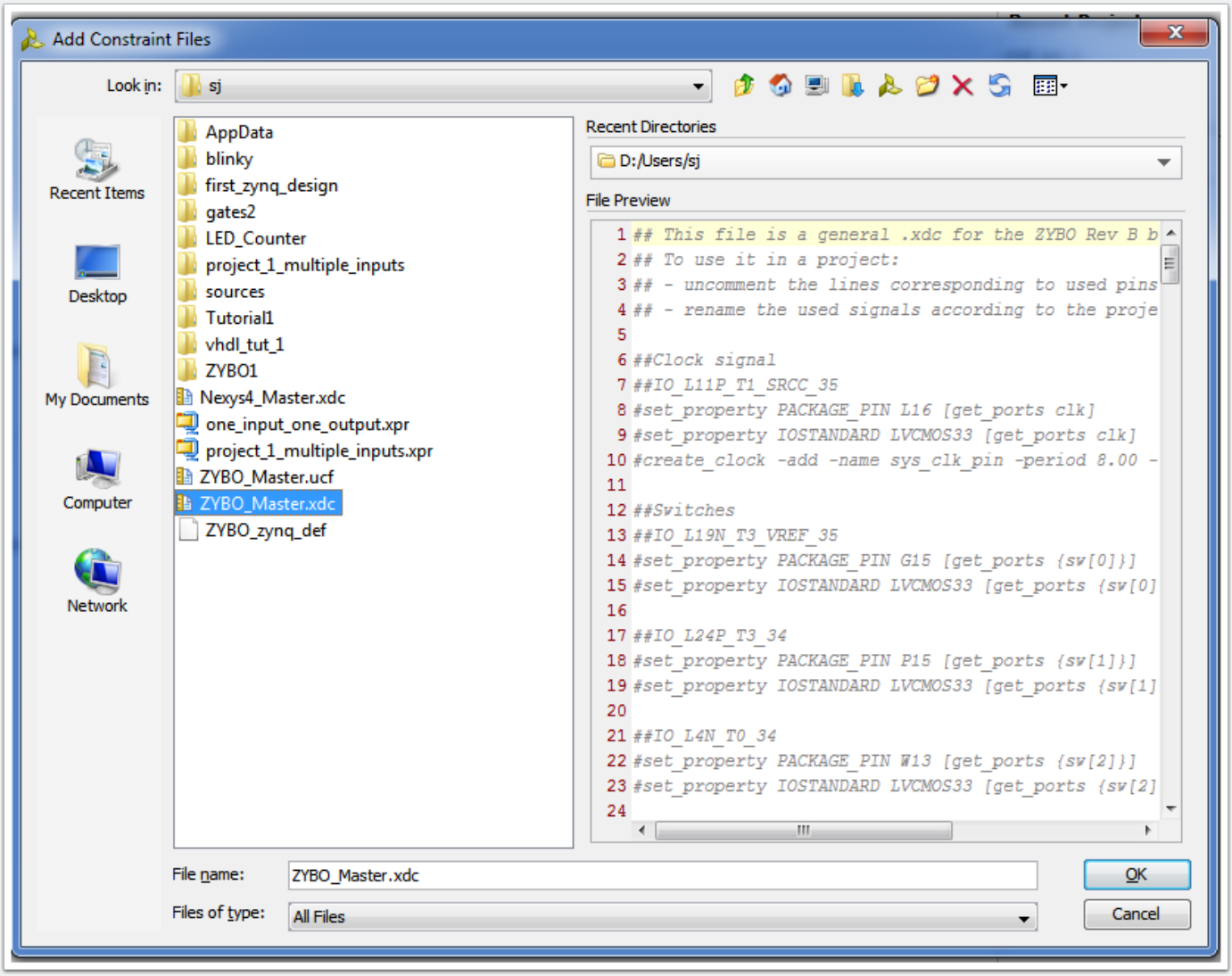
Add Constraints

Click "+", Add Files.



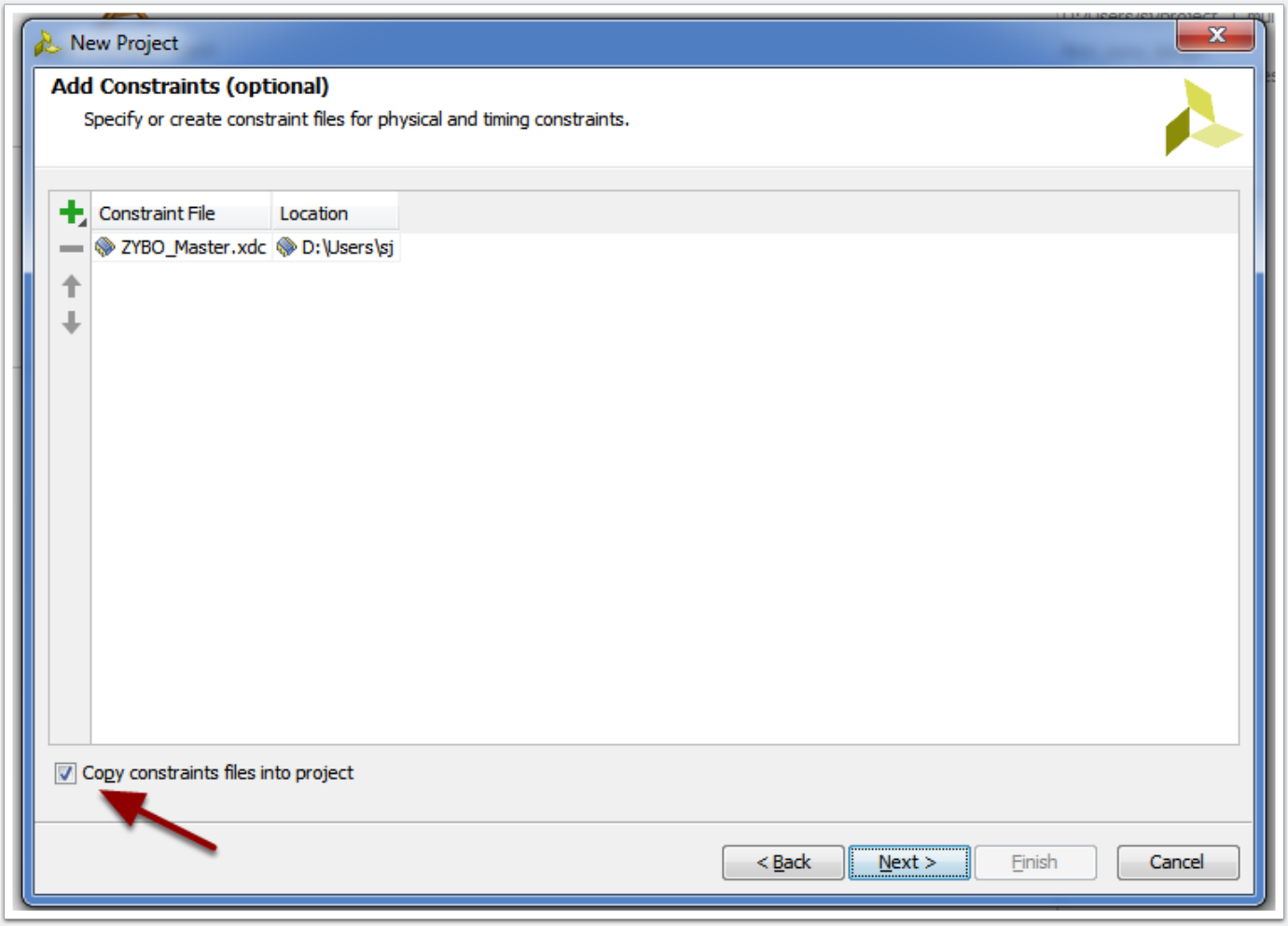
Simple VHDL example using VIVADO 2015 with ZYBO FPGA board

Add Constraint file we downloaded at Precondition step.



Make sure: Copy constraints files into project - Checked.

Click - Next



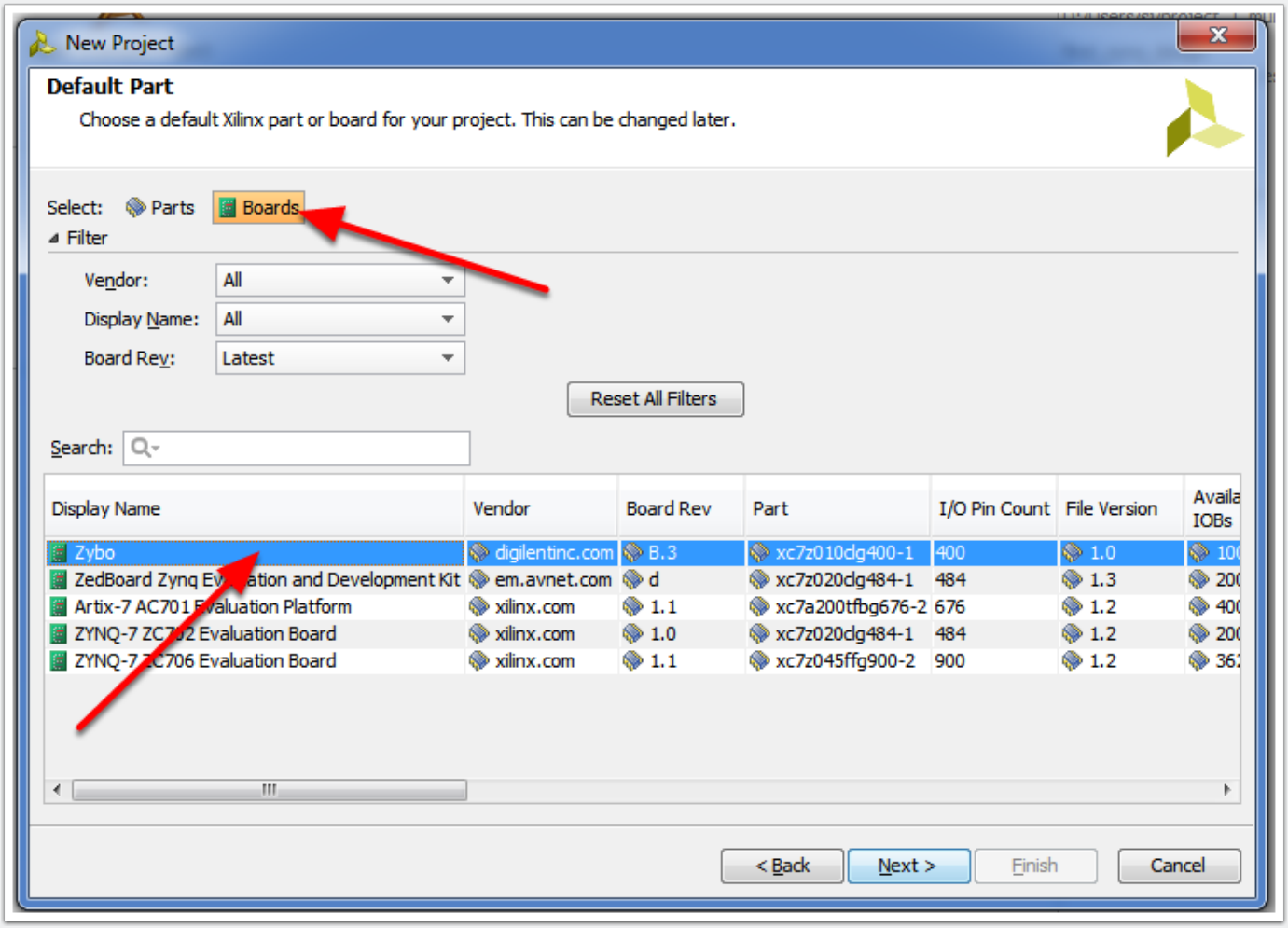
Default Part

Click on boards and select Zybo. If you still don't have it follow steps in Preconditions: Adding Zybo board to Vivado.

Simple VHDL example using VIVADO 2015 with ZYBO FPGA board

If you don't see ZYBO goto Preconditions Step.

Next.



New Project Summary

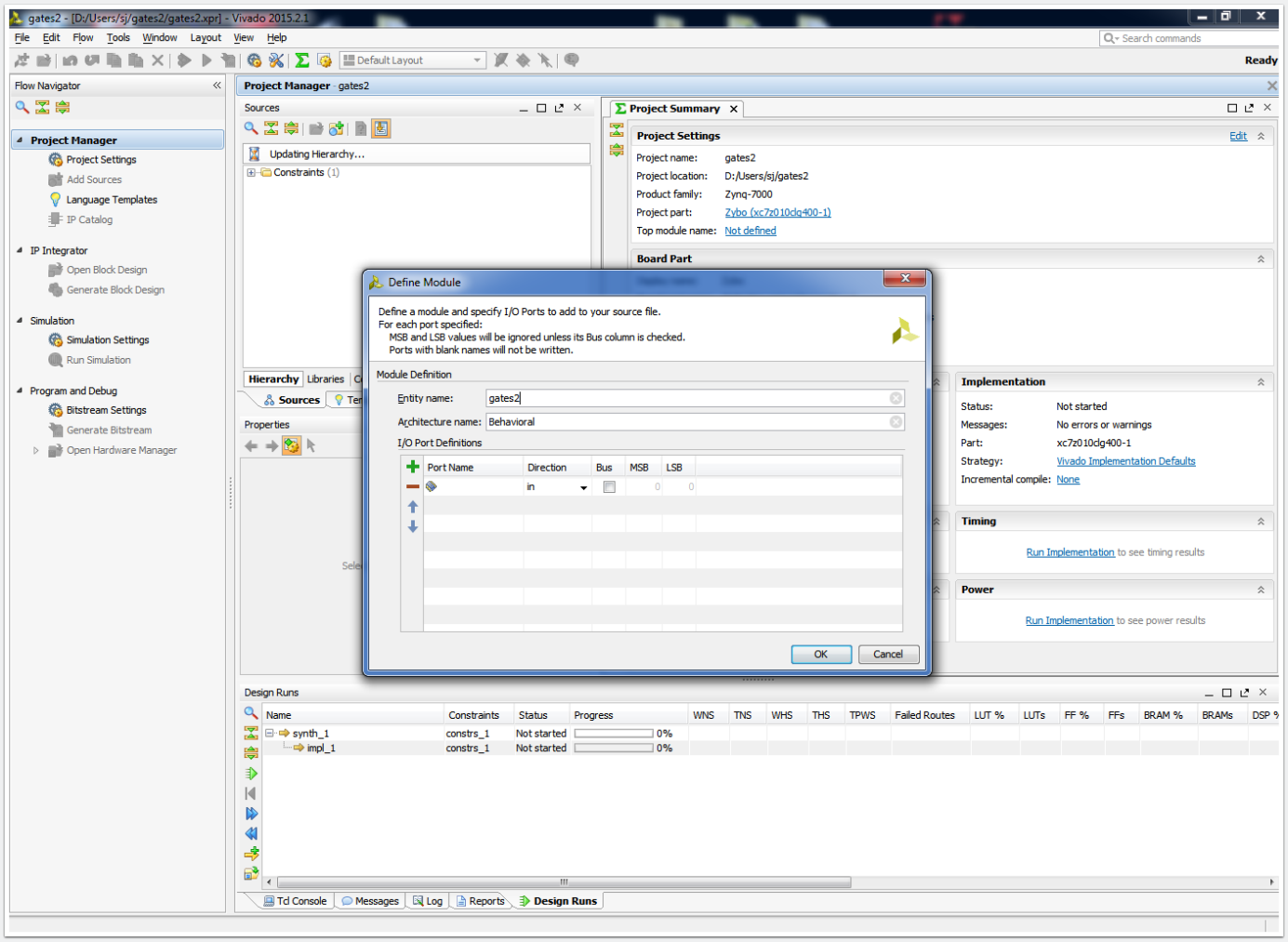
Finish

New Project main view

Project files generated and ready for your design.

Simple VHDL example using VIVADO 2015 with ZYBO FPGA board

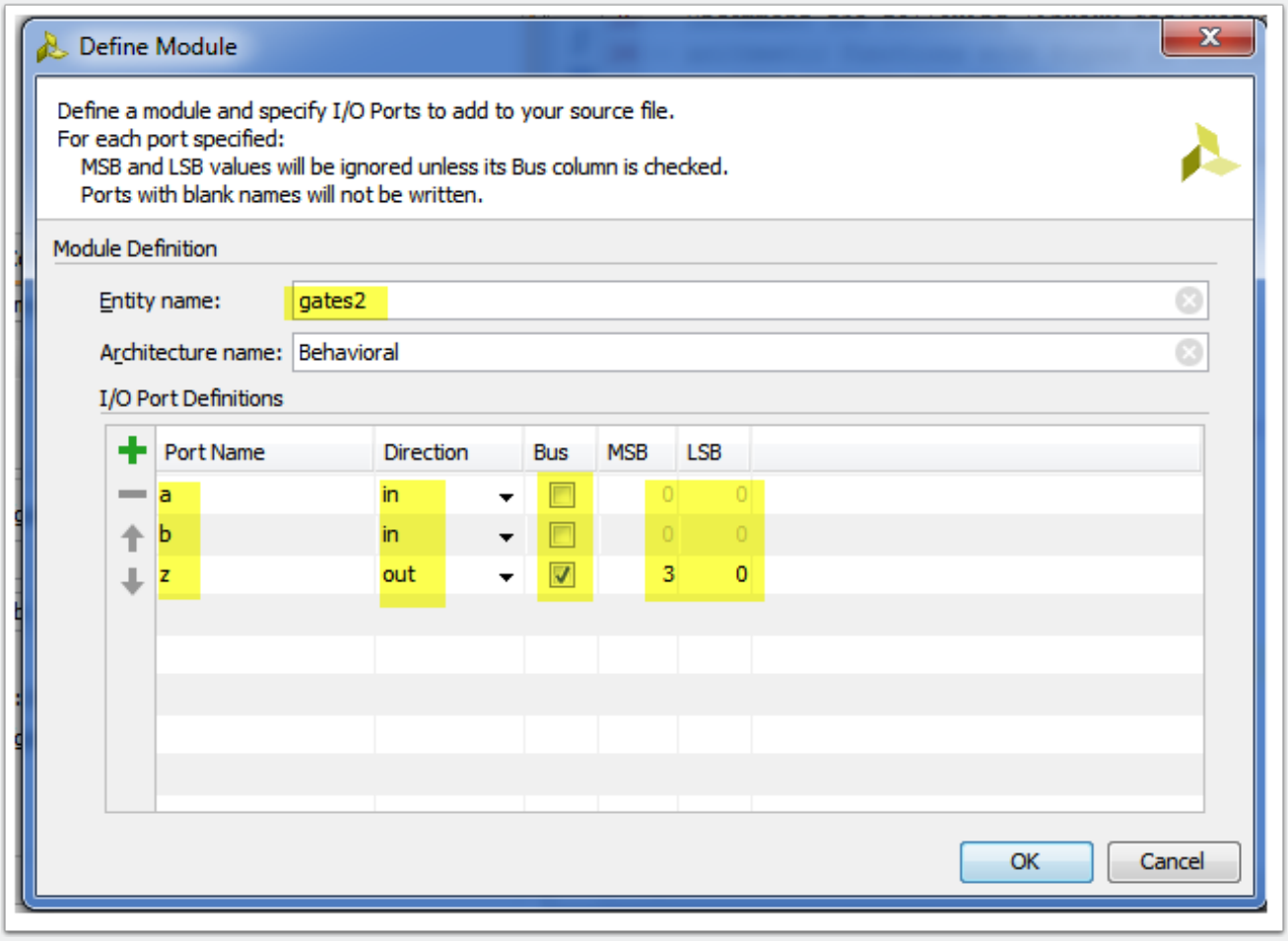
We will implement 2 input gates and 4 output basic gates **and**, **or**, **xor and nor.**



Simple VHDL example using VIVADO 2015 with ZYBO FPGA board

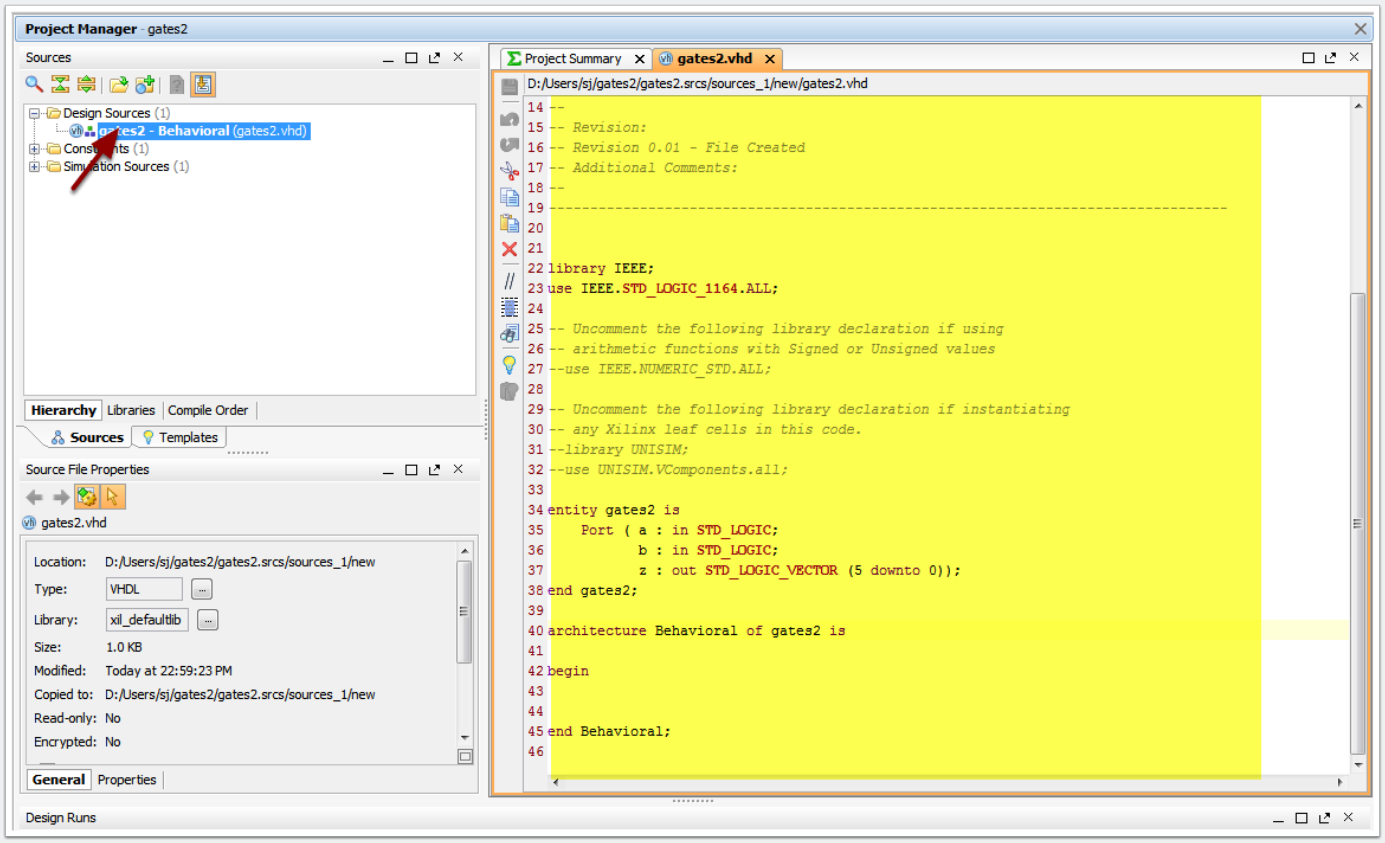
Define I/O ports as below

OK



Select VHDL Design

Click on Source file in Project Manager>Sources>Design Sources - Source code on Righthand side should appear.

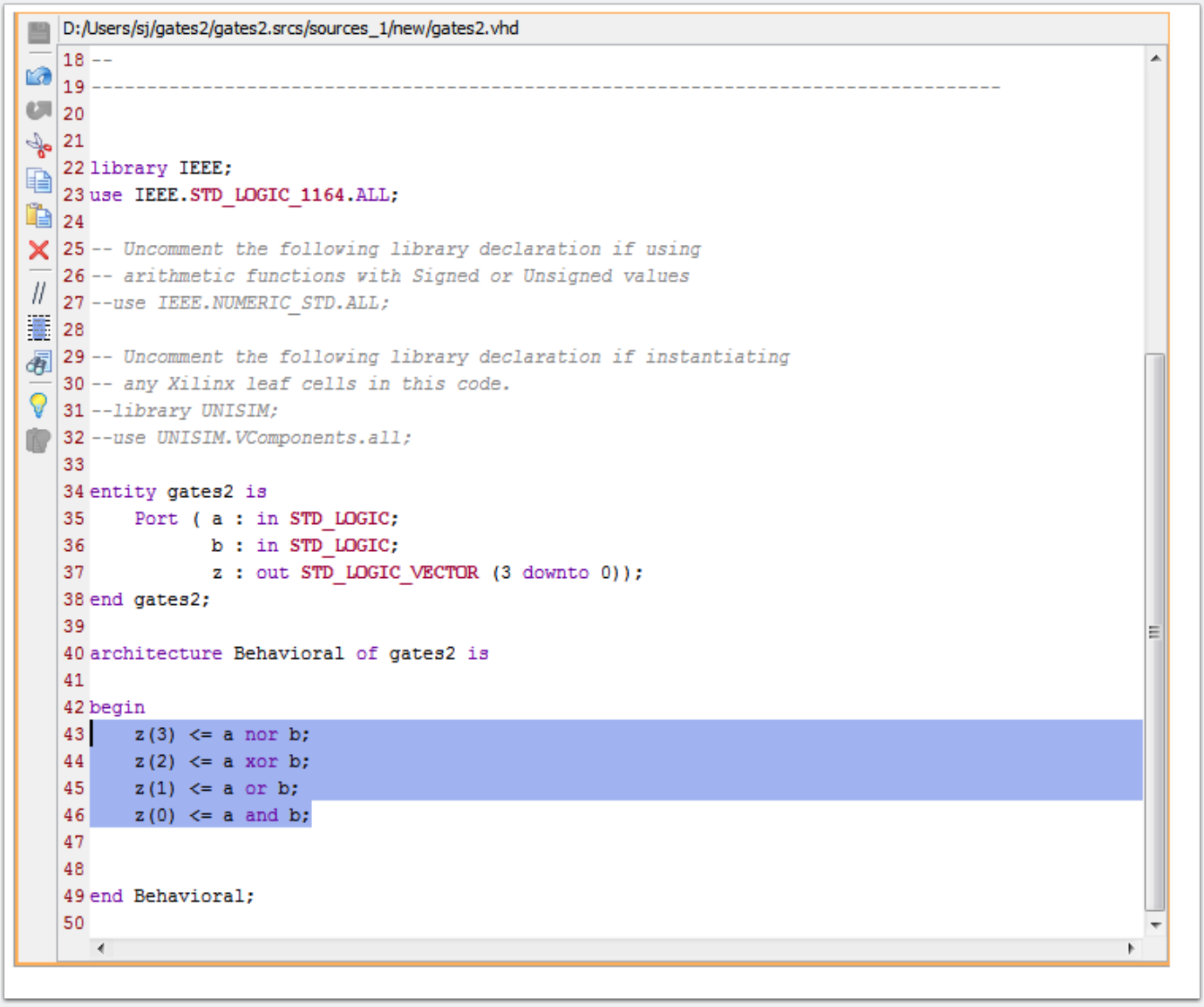


Changes to source code.

Modify VHDL file - add lines as highlighted below.

Simple VHDL example using VIVADO 2015 with ZYBO FPGA board

z(0) <= a and b;
z(1) <= a or b;
z(2) <= a xor b;
z(3) <= a nor b;

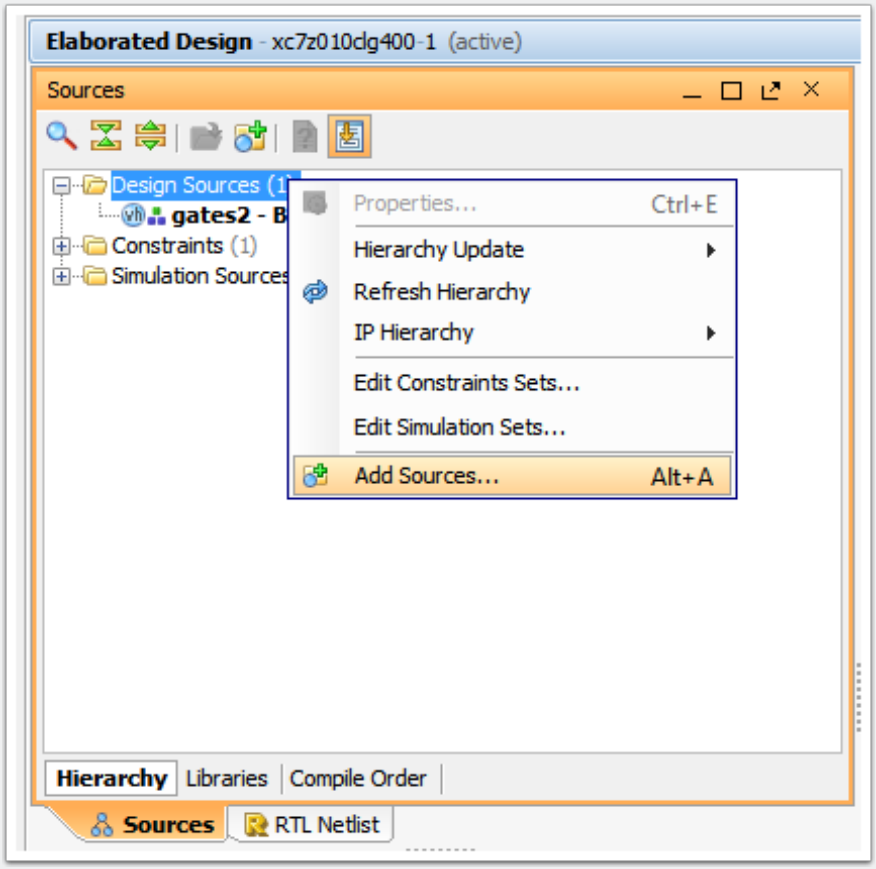


Create top file

Rightclick on Design Sources and select Add Sources.

1. Add or create design souces.

2. "+" > Create File

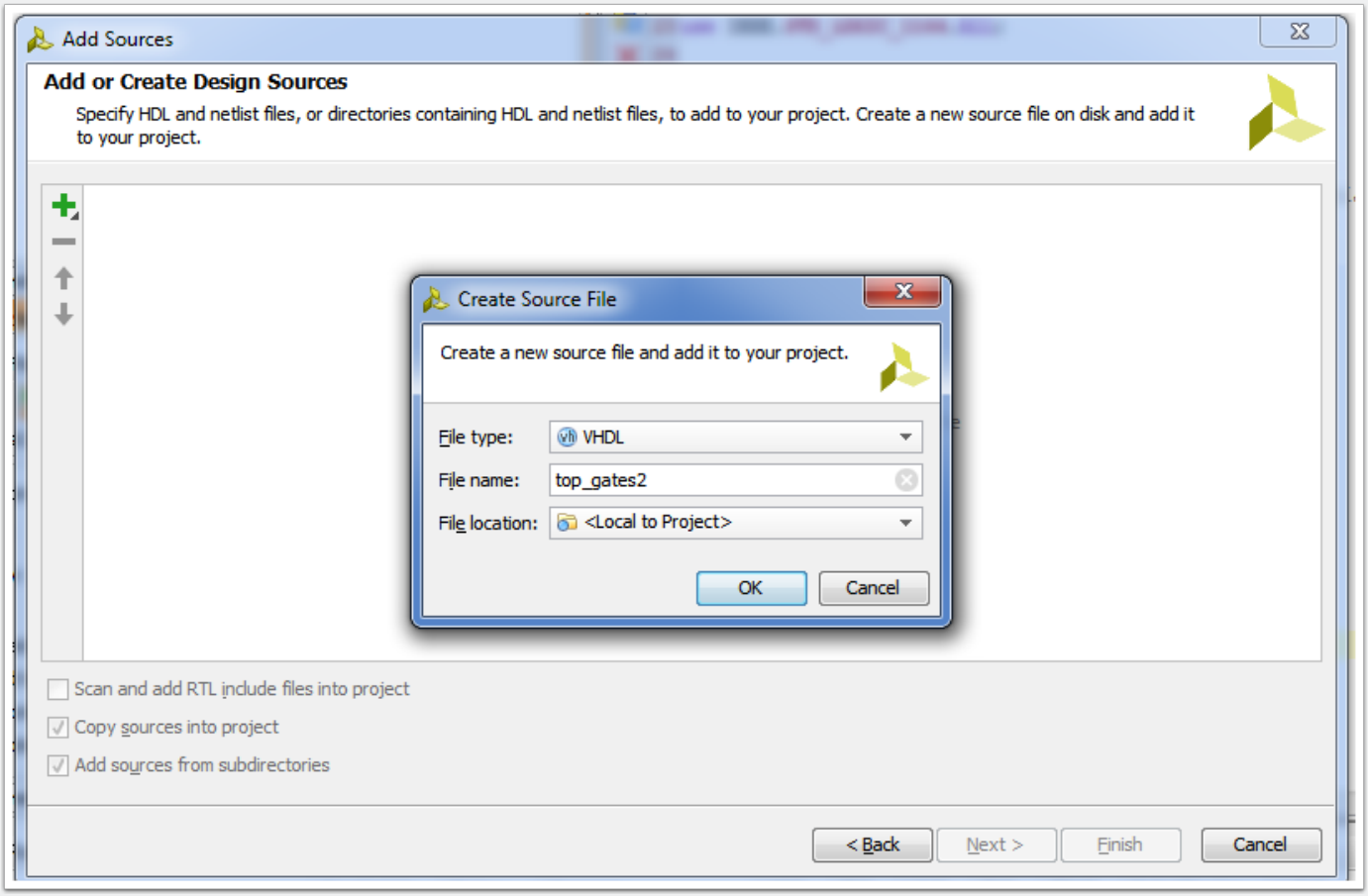


File Type :VHDL,

File name: top_gates2

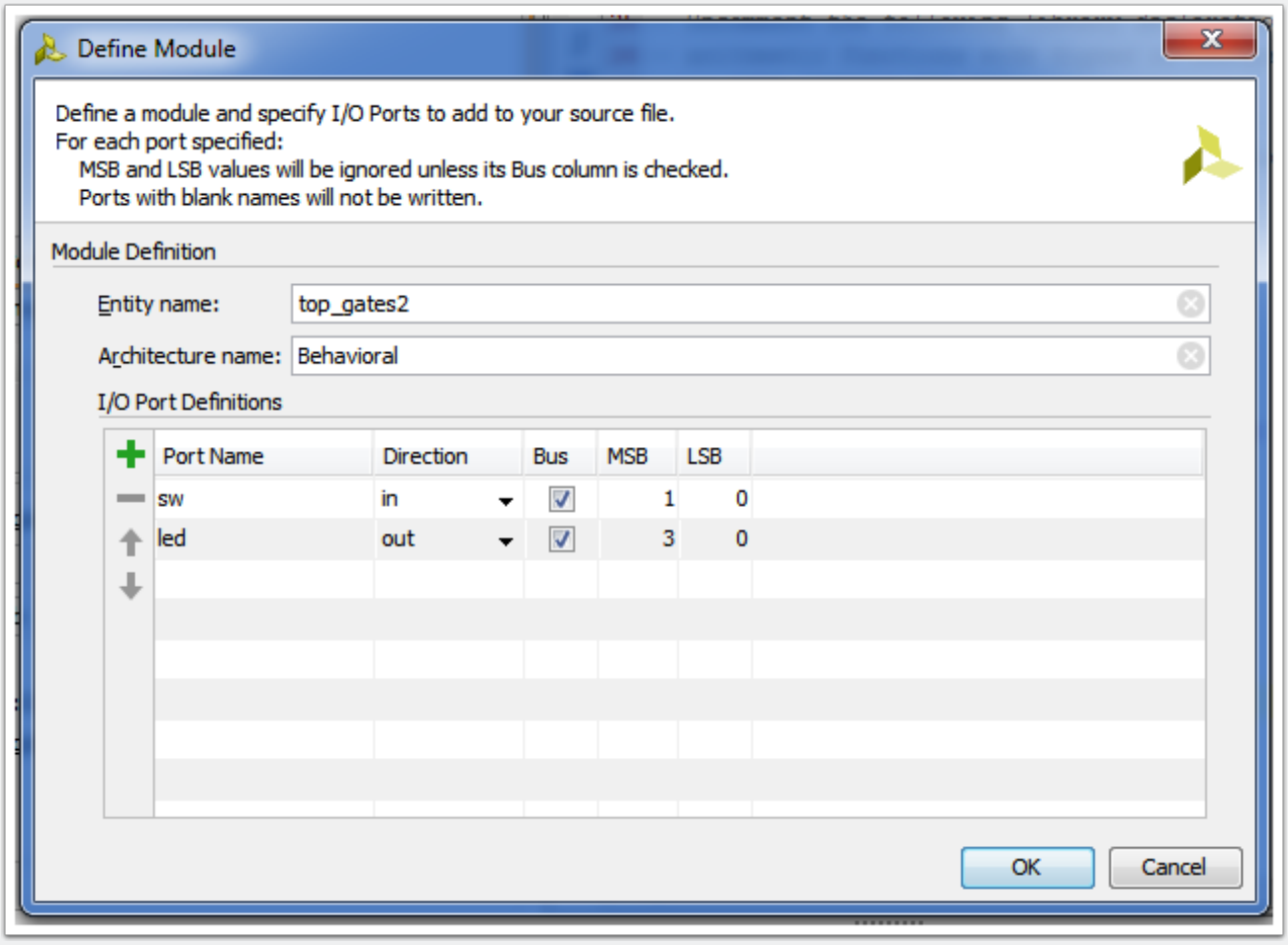
OK

Finish


Add Sources
Add or Create Design Sources
Specify HDL and netlist files, or directories containing HDL and netlist files, to add to your project. Create a new source file on disk and add it to your project.
Create Source File
Create a new source file and add it to your project.
File type:
VHDL
File name:
top_gates2
File location:
<Local to Project>
OK
Cancel
Scan and add RTL include files into project
Copy sources into project
Add sources from subdirectories
< Back
Next >
Finish
Cancel

Define Module

Add sw and led as on image below.



Replace default source code.

```
library IEEE;

use IEEE.STD_LOGIC_1164.ALL;
```

Simple VHDL example using VIVADO 2015 with ZYBO FPGA board

```
entity top_gates2 is

  Port (

     sw : in STD_LOGIC_VECTOR (1 downto 0);

     led : out STD_LOGIC_VECTOR (3 downto 0)

  );

end top_gates2;
architecture top_gates2 of top_gates2 is

component gates2 is

  Port (

     a : in STD_LOGIC;

     b : in STD_LOGIC;

     z : out STD_LOGIC_VECTOR (3 downto 0)

  );

end component;

begin

  cl : gates2
```

Simple VHDL example using VIVADO 2015 with ZYBO FPGA board

```
    port map (
        a => sw(0),
        b => sw(1),
        z(0) => led(0),
        z(1) => led(1),
        z(2) => led(2),
        z(3) => led(3)
    );
end top_gates2;
```

Simple VHDL example using VIVADO 2015 with ZYBO FPGA board

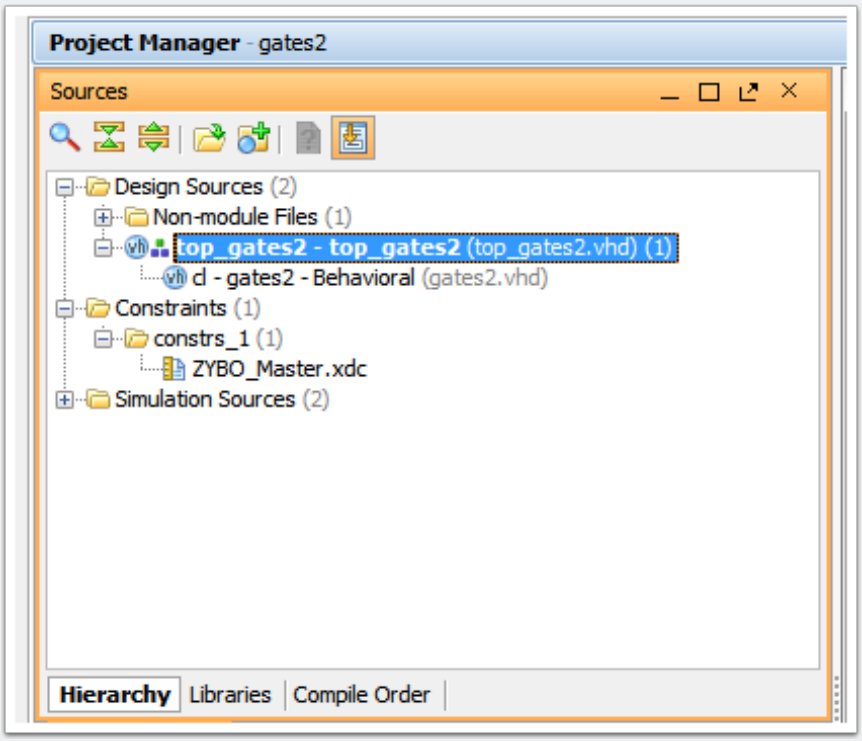
Project Summary | Schematic | gates2.vhd | **top.vhd** | ZYBO_Master.xdc

D:/Users/sj/gates2/gates2.srcs/sources_1/new/top.vhd

```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3
4  entity top is
5      Port (
6          sw : in STD_LOGIC_VECTOR (1 downto 0);
7          led : out STD_LOGIC_VECTOR (3 downto 0)
8      );
9  end top;
10
11 architecture top of top is
12
13 component gates2 is
14     Port (
15         a : in STD_LOGIC;
16         b : in STD_LOGIC;
17         z : out STD_LOGIC_VECTOR (3 downto 0)
18        );
19 end component;
20
21 begin
22     c1 : gates2
23
24     port map (
25         a => sw(0),
26         b => sw(1),
27         z(0) => led(0),
28         z(1) => led(1),
29         z(2) => led(2),
30         z(3) => led(3)
31     );
32
33 end top;
```

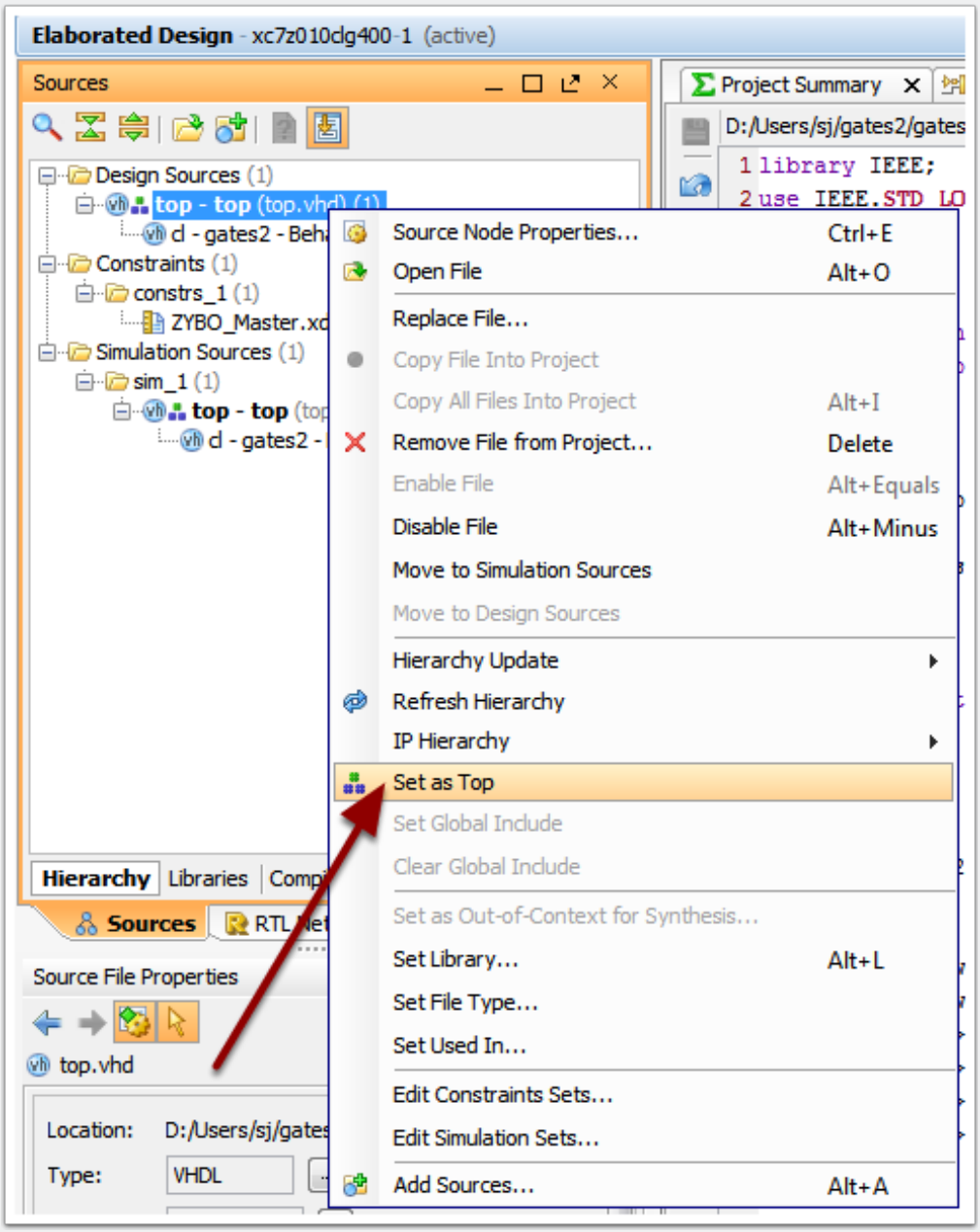
Top Design

We have single top design interface file which use our gates2 design as component.



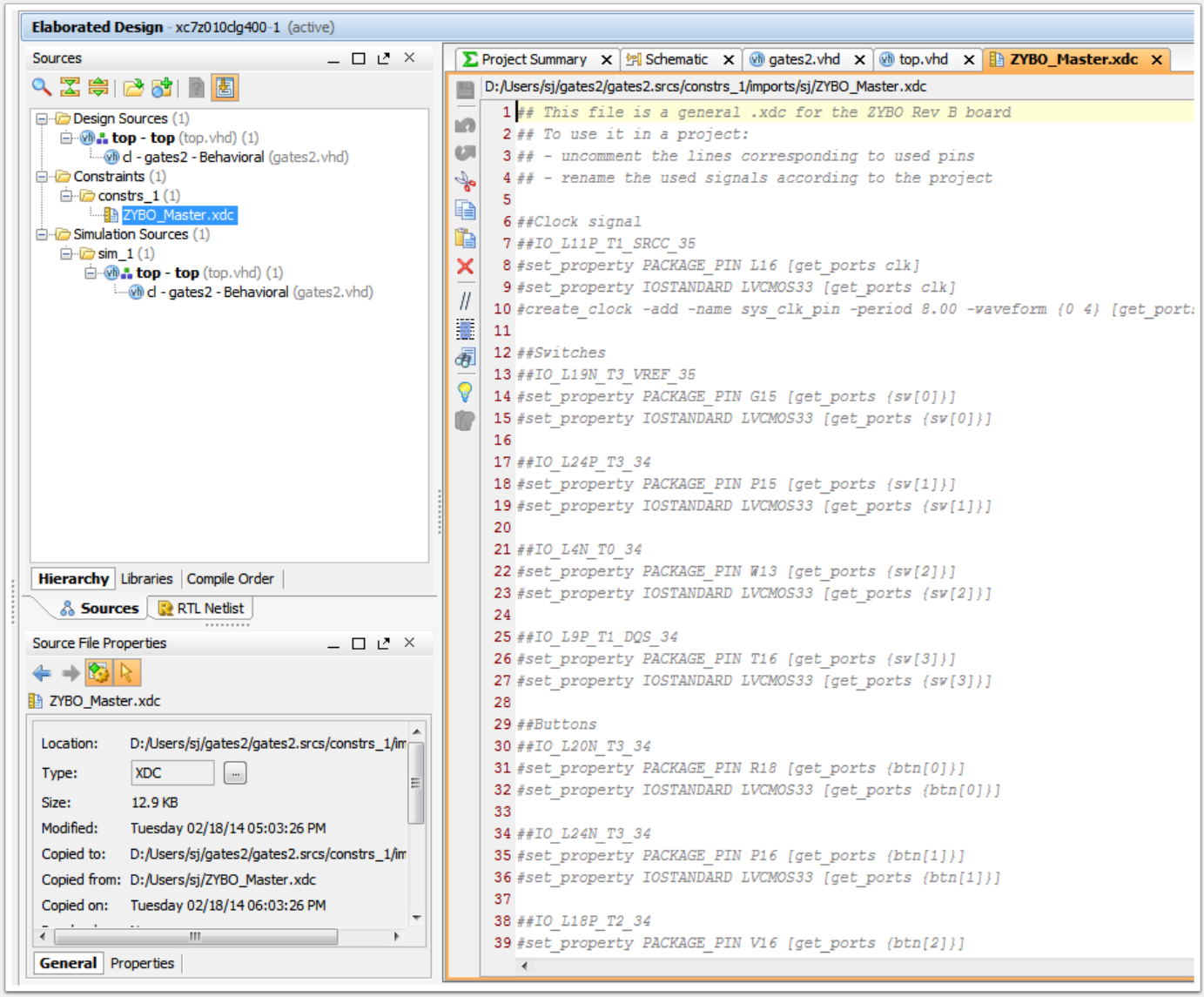
top design

Make sure our top file became parent of gates2 file. Otherwise set it manually with **Set as Top**.



Amend Constraints file

Select xdc file from Sources>Constraints



Changes in xdc file

Uncomment lines of I/O port we need to use.

Save file.

Simple VHDL example using VIVADO 2015 with ZYBO FPGA board

D:/Users/sj/gates2/gates2.srcs/constrs_1/imports/sj/ZYBO_Master.xdc

```
14 set_property PACKAGE_PIN G15 [get_ports {sw[0]}]
15 set_property IOSTANDARD LVCMOS33 [get_ports {sw[0]}]
16
17 ##IO_L24P_T3_34
18 set_property PACKAGE_PIN P15 [get_ports {sw[1]}]
19 set_property IOSTANDARD LVCMOS33 [get_ports {sw[1]}]
20
21
22 ##LEDs
23 ##IO_L23P_T3_35
24 set_property PACKAGE_PIN M14 [get_ports {led[0]}]
25 set_property IOSTANDARD LVCMOS33 [get_ports {led[0]}]
26
27 ##IO_L23N_T3_35
28 set_property PACKAGE_PIN M15 [get_ports {led[1]}]
29 set_property IOSTANDARD LVCMOS33 [get_ports {led[1]}]
30
31 ##IO_0_35
32 set_property PACKAGE_PIN G14 [get_ports {led[2]}]
33 set_property IOSTANDARD LVCMOS33 [get_ports {led[2]}]
34
35 ##IO_L3N_T0_DQS_AD1N_35
36 set_property PACKAGE_PIN D18 [get_ports {led[3]}]
37 set_property IOSTANDARD LVCMOS33 [get_ports {led[3]}]
38
39 ##I2S Audio Codec
40 ##IO_L12N_T1_MRCC_35
41 #set_property PACKAGE_PIN K18 [get_ports ac_bclk]
42 #set_property IOSTANDARD LVCMOS33 [get_ports ac_bclk]
43
44 ##IO_25_34
45 #set_property PACKAGE_PIN T19 [get_ports ac_mclk]
46 #set_property IOSTANDARD LVCMOS33 [get_ports ac_mclk]
47
48 ##IO_L23N_T3_34
49 #set_property PACKAGE_PIN P18 [get_ports ac_muten]
50 #set_property IOSTANDARD LVCMOS33 [get_ports ac_muten]
51
52 ##IO_L8P_T1_AD10P_35
```

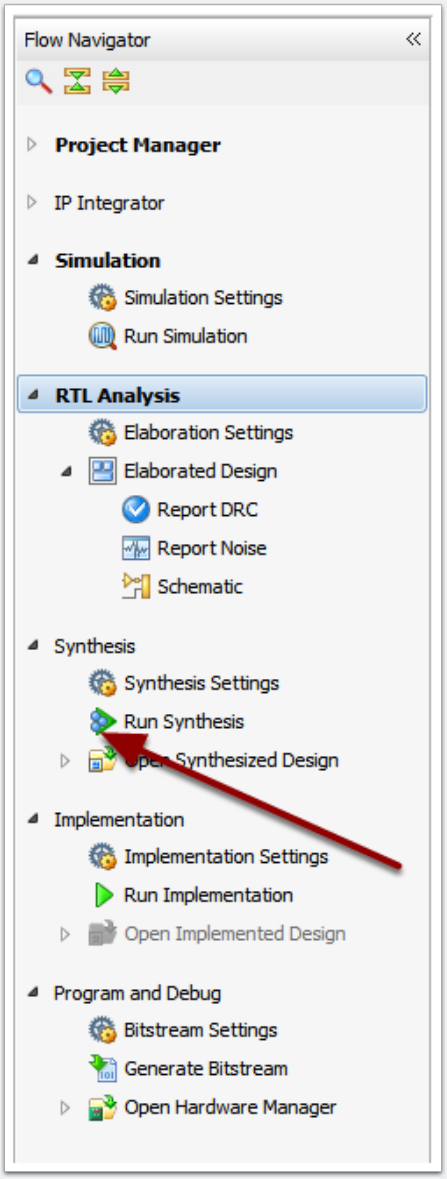
Synthesis

At Synthesis phase we convert our circuit from register transfer level (RTL) into a design implementation in terms of logic gates.

In Flow Navigator on Lefthand side.:

Next steps can be **Simulation**>**Run Simulation** or **RTL Analysis>Schematic** but we skip them in this tutorial and come directly to **Synthesis>Run Synthesis**.

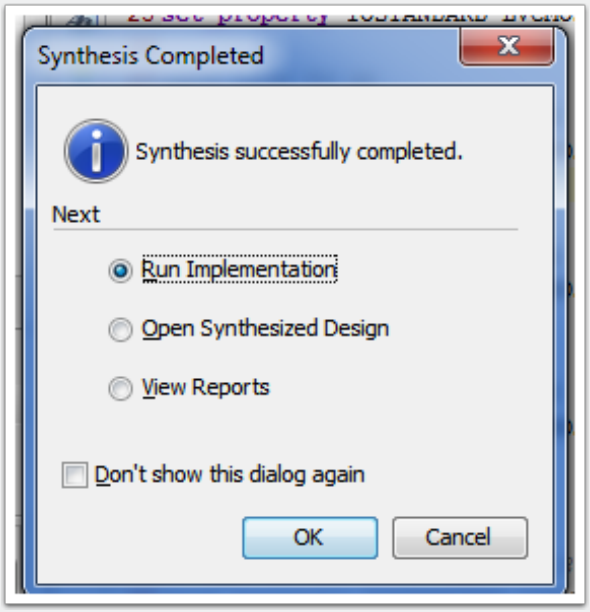
Simple VHDL example using VIVADO 2015 with ZYBO FPGA board



Synthesis complention

Leave default Run Implementation

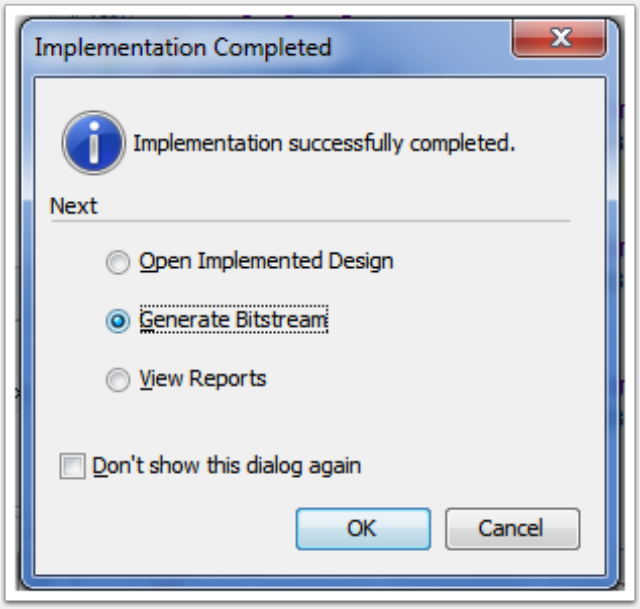
OK



Generate Bitstream

Select Generate Bitstream

OK



Final

Pay attention to jumpers.

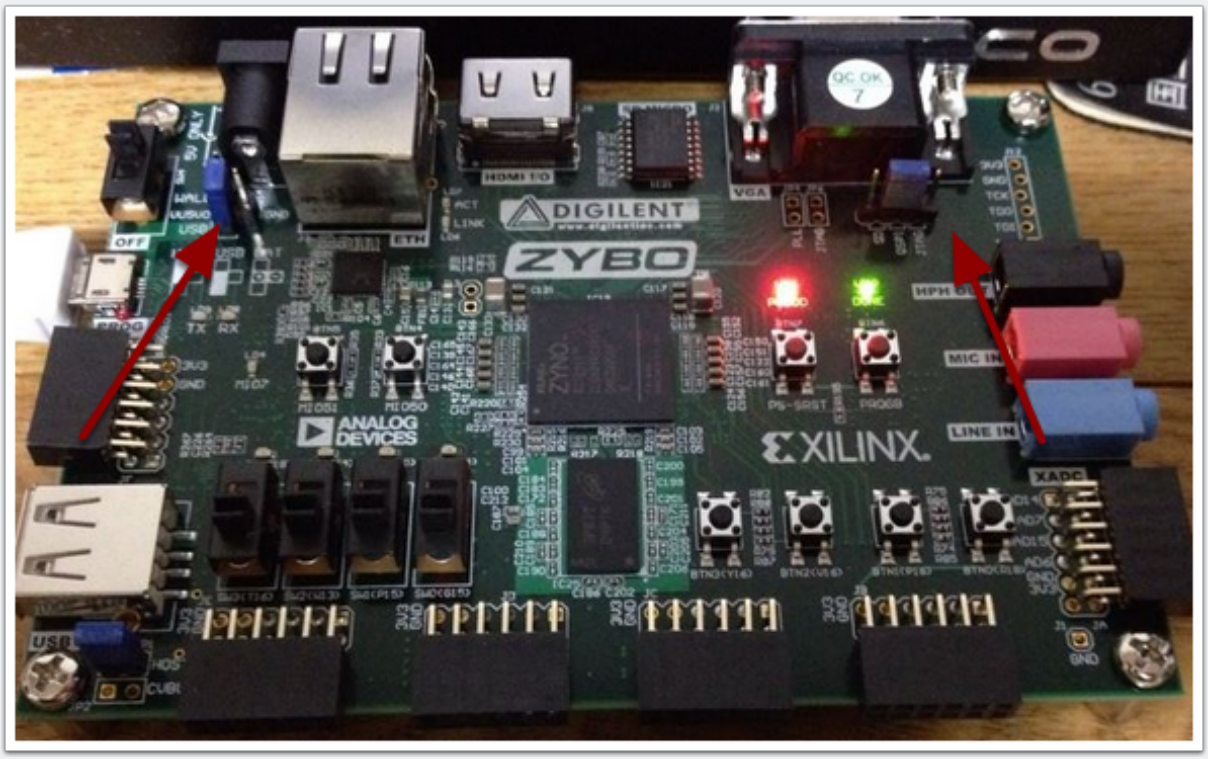
JP7 - It should set to USB.

JP5 can be JTAG or QSPI

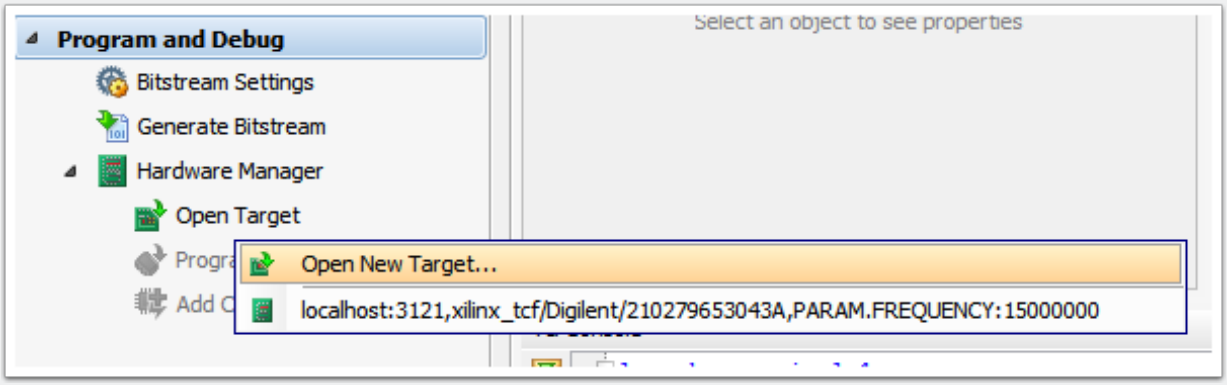
Connect ZYBO to PC with Micro-USB cable.

Simple VHDL example using VIVADO 2015 with ZYBO FPGA board

Photo from http://marsee101.blog19.fc2.com/blog-entry-2745.html



Program ZYBO

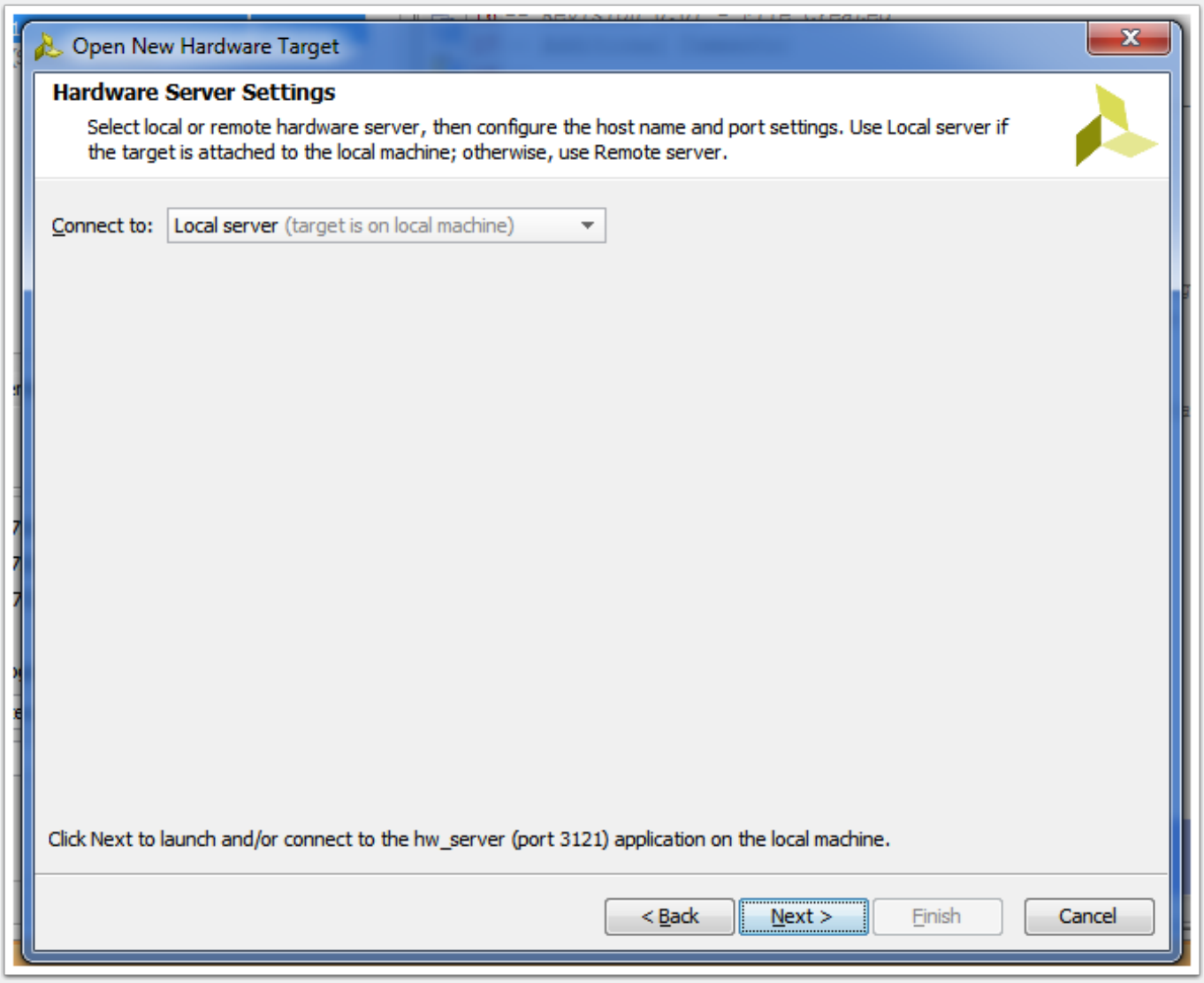


Simple VHDL example using VIVADO 2015 with ZYBO FPGA board

Next

Simple VHDL example using VIVADO 2015 with ZYBO FPGA board

Next

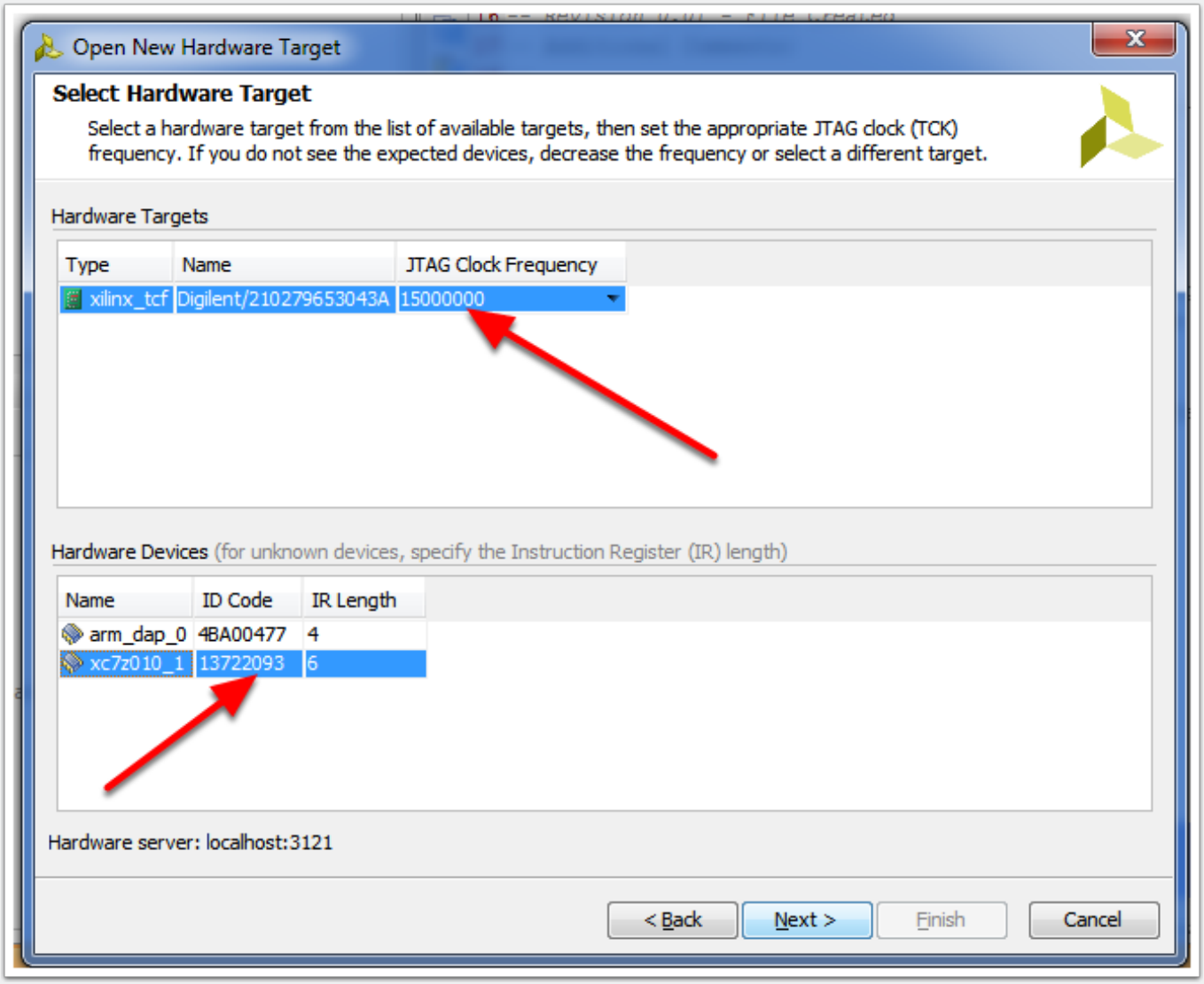


Simple VHDL example using VIVADO 2015 with ZYBO FPGA board

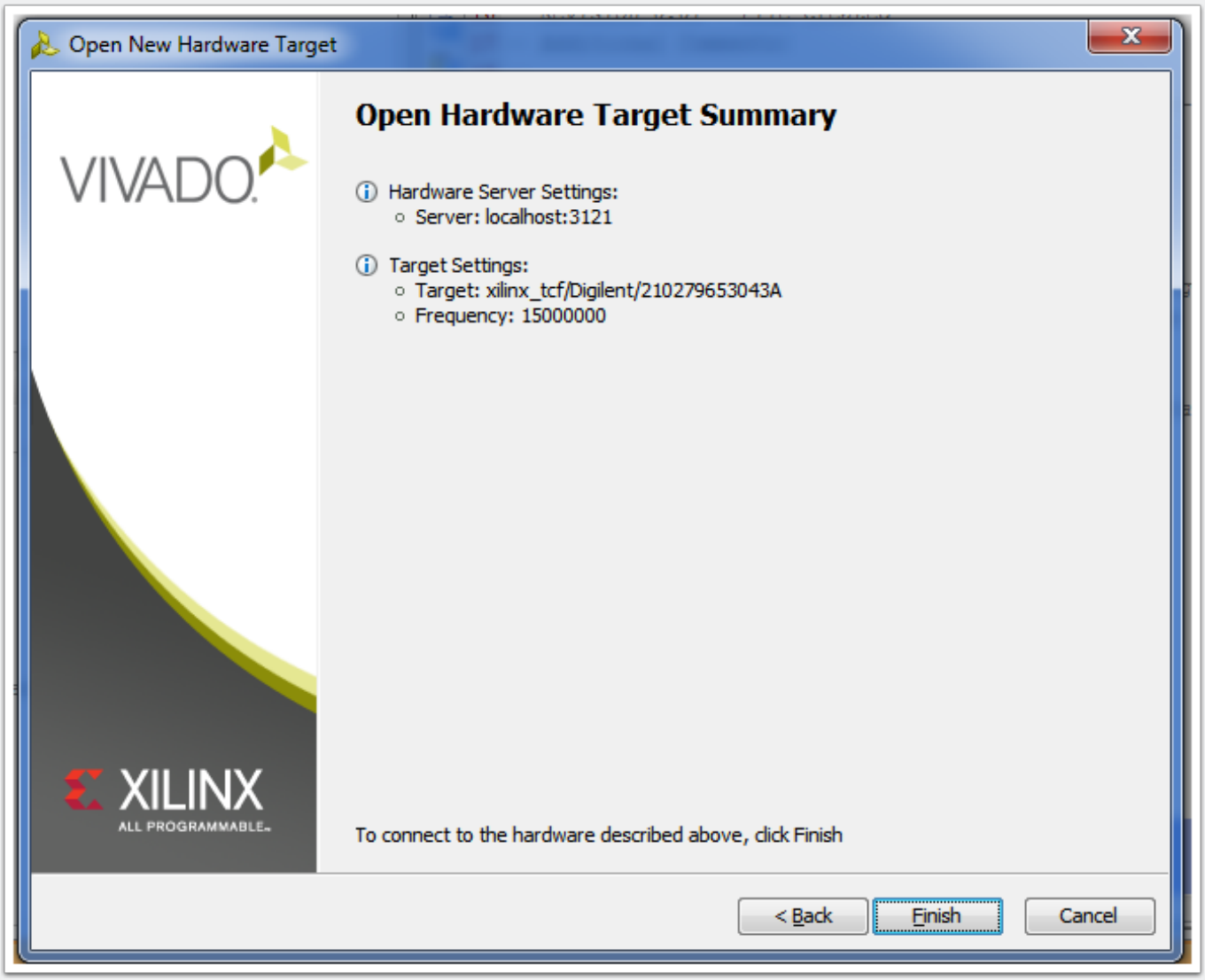
Make sure you have similar setting like on picture below.

Select xc7z010_1

Next

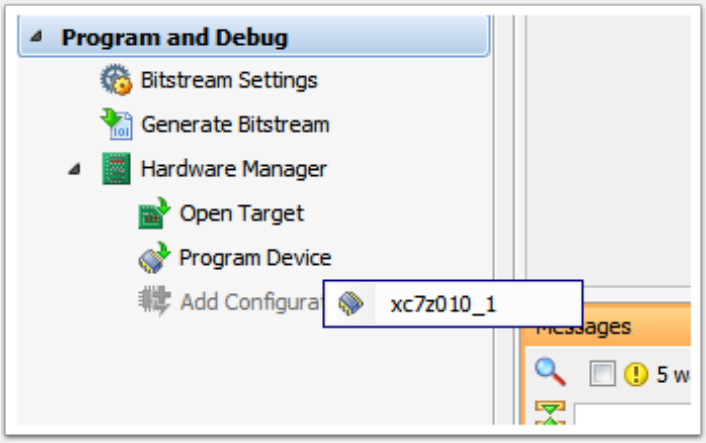


Finish

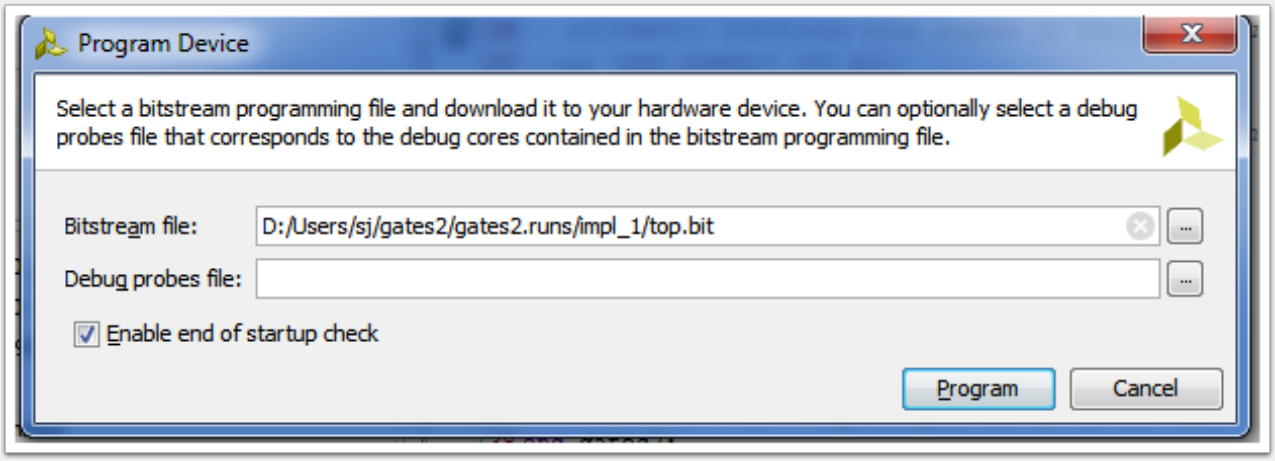

Open New Hardware Target
VIVADO
Open Hardware Target Summary
Hardware Server Settings:
Server: localhost:3121
Target Settings:
Target: xilinx_tcf/Digilent/210279653043A
Frequency: 15000000
XILINX
ALL PROGRAMMABLE
To connect to the hardware described above, click Finish
< Back
Finish
Cancel

Simple VHDL example using VIVADO 2015 with ZYBO FPGA board

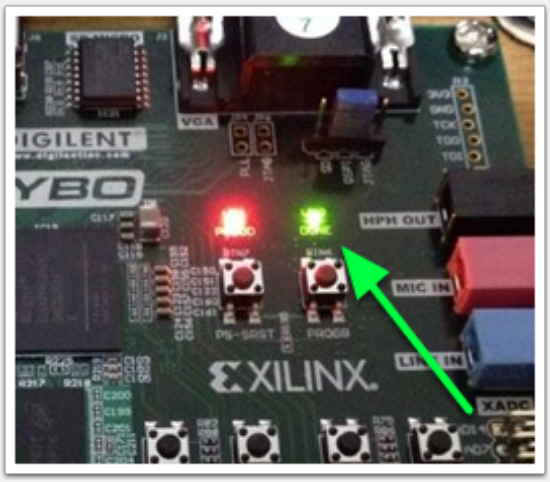
Program device > xc7z010_1



Program



As confirmation of successfull upload Greed Led will set



Use switches to confirm **and**, **or**, **xor** and **nor** operations.

Archive of project available.

Reference

1. Digital Design Using Digilent FPGA Boards VHDL/ Active-HDL edition. Richard E. Haskell, Darrin M. Hanna

2. Learning By Example Using VHDL. Advanced Digital Design With a NEXYS 2 FPGA Board. Richard E. Haskell, Darrin M. Hanna

3. The ZYNQ BOOK - Make sure you download not only book archive but also tutorials book with sources.

4. HDL Chip Design- A Practical Guide for Designing, Synthesizing and Simulating ASICs and FPGAs Using VHDL or Verilog. By Douglas J. Smith

5. ZYBO Reference Manual