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Simulation and Construction of a Half-Bridge Class D Audio Amplifier

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Abstract

Simulation and Construction of a Half-Bridge Class D Audio Amplifier

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Usage of class D audio amplifiers has become increasingly widespread in recent years, mainly due to their high efficiency, which can reach almost 100 %. Class D amplifiers can also be compact, making them suitable for mobile applications. In contrast, the most efficient conventional amplifiers such as class B can reach a maximum efficiency of 78.5 %. The high efficiency of class D amplifiers can be attributed to the switching stage, which in the case of a half-bridge design consists of two amplifying MOSFETs. These MOSFETs are never on at the same time, which minimizes the quiescent current and thereby the power losses. The goal of this project was to design, simulate and construct a half-bridge class D audio amplifier. A working amplifier with 80 % efficiency was built, with power losses occuring mainly in the voltage regulators. Simulations of the amplifier corresponded well with the constructed amplifier apart from issues originating from the aforementioned voltage regulation as well as the triangle wave generator. The goal of the project was achieved and the finished amplifier possessed good sound quality and little unwanted noise. To further improve on the design, better voltage regulation, a full-bridge configuration and a feedback loop could be utilized.

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Populärvetenskaplig sammanfattning

Projektets syfte var att designa, simulera och bygga en klass D-ljudförstärkare. Denna typ av förstärkare har en teoretisk verkningsgrad på 100 % vilket gör den utmärkt för applikationer där låg effektförbrukning är viktigt. Som jämförelse har de effektivaste traditionella förstärkarna som klass B en maximal teoretisk verkningsgrad på 78.5 %. Klass D-förstärkare är så kallade "switching"-förstärkare där de förstärkande transistorerna ständigt slås på och av. Att transistorerna inte är på hela tiden är vad som ger klass D-förstärkare dess höga verkningsgrad. I detta projekt visade det sig att simuleringar överensstämde väl med den uppbyggda kretsen men att det fanns ett antal saker att ta hänsyn till; exempelvis så förlorades en del effekt i form av värme i spänningsregulatorerna, vilket var ett problem som inte fanns i simuleringarna. Trots detta erhölls en relativt hög verkningsgrad på 80 %. Utsignalen hade en del störningar men det var inget som märktes då man spelade musik genom en högtalare.

Acknowledgments

We would like to thank our supervisor, Prof. Jörgen Olsson, for his support and guidance throughout this project, as well as Dr. Uwe Zimmermann for assisting with the PCB design and supplying various components that improved our circuit. We would also like to extend our gratitude and appreciation to the second-year IT students with whom we shared a lab; they were forced to suffer through various deafening speaker tests and never complained. Lastly, we would like to thank the numerous culinary establishments around the Ångström laboratory for their never-ending supply of food and caffeinated beverages.

Contents

1 Introduction

With the increasing usage of battery powered devices such as phones, laptops and other portable devices, low power consumption, compact design and efficiency has become more important than ever. Compared to traditional linear amplifiers, class D amplifiers have a much higher efficiency (theoretically 100 %) and an overall lower power consumption. They can also be high-powered yet compact. All this has made class D amplifiers rather popular in recent times, especially in devices with limited heat dissipation.

A common misconception is that the D stands for "digital" which is wrong; class D amplifiers might use digital components but the power stage that amplifies the signal is analog. The power stage uses a switching technique that allows the amplifying MOSFETs to mainly operate in their linear regions. This minimizes the resistance of the MOSFETs, and thereby the power losses.

The goal of this project was to design and build a working half-bridge class D amplifier for learning purposes and to document the process. Good sound quality, low noise and high efficiency were secondary goals. It was decided that we would design as much as possible by ourselves with discrete components and rely on ICs only if necessary. Also, the final construction was to be compared with computer simulations to understand the challenges in realizing a class D amplifier. Lastly, the project included etching a PCB for the finalized amplifier design and placing it in a chassis with a dedicated power supply.

2 Theory

2.1 Linear amplifiers

Linear amplifiers such as class A, B, AB and C are the most ordinary amplifier types. They create an output that is proportional to the input, and are classified according to their collector current waveform.

The output stage of a class A amplifier normally consists of an emitter (or source) follower and has a high bias current. The transistor conducts for the entire signal cycle and the output stage consumes considerable power, even without signal. Class A amplifiers have a theoretical maximum efficiency of 25 % [1].

The class B amplifier utilizes a push-pull stage, which means that two transistors are connected in such a way that both cannot conduct simultaneously. The bias current has no DC component and thereby the transistors conduct for half a signal cycle each and dissipate no power when there is no input. Therefore a maximum efficiency of 78.5 % is possible, but crossover distortion becomes a problem [1].

Crossover distortion can be eliminated by using a combination of class A and class B, the class AB amplifier. This is done by biasing the push-pull stage of the class B amplifier with a small DC component. This means that the transistors conduct at the same time for small signals, increasing the risk of short circuiting the output stage. The power relationships of the class AB amplifier are similar to those of class B [1].

The main advantage of linear amplifiers is the high fidelity output that can be achieved, but it comes at the cost of relatively low efficiency.

2.2 Switching amplifiers

Switching amplifiers such as class D and class T sample the input signal and amplify it using a number of MOSFETs. Unlike linear amplifiers, the power stage MOSFETs turn completely on and off during the signal cycle.

The main difference between class D and class T is how the output stage is driven, as class T amplifiers use a signal and feedback to constantly change the characteristics of the switching signal [2].

Switching amplifiers have almost no quiescent power dissipation, thus allowing efficiencies close to 100 %, but because the signal is sampled some of the information will be lost [2]. Feedback, though not necessary, can also be used in switching amplifiers to reduce noise and increase stability.

A block diagram of a half-bridge class D amplifier can be seen in fig. 1.

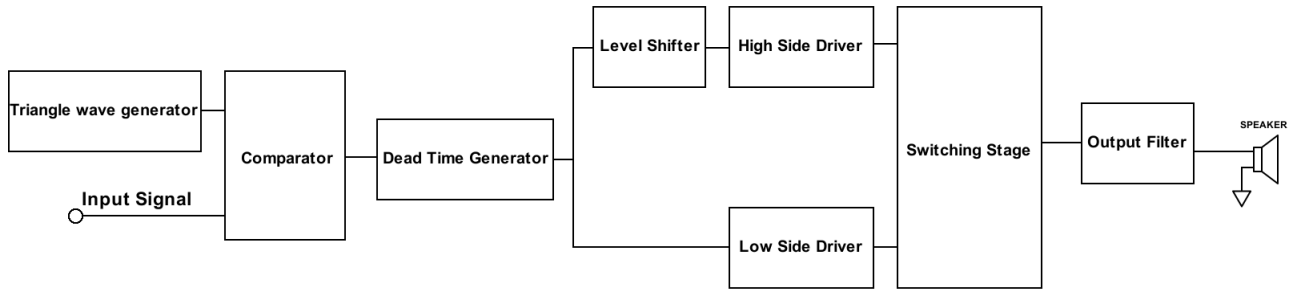

Figure 1: Block diagram of a PMOS/NMOS class D amplifier.

2.3 Pulse-width modulation (PWM)

Pulse-width modulation (PWM) is one method used by class D amplifiers to transfer the input signal. PWM is often used to control LEDs, motors and cooling fans.

A PWM signal can be created by comparing the input signal with a high frequency carrier wave, e.g. a triangle wave, using a high-speed comparator [3]. The comparator will essentially sample the input as it outputs a logic high (1) when the input signal is higher than the carrier wave and a logic low (0) when the input signal is lower than the carrier wave, thus creating a PWM signal.

The input signal will be sampled with the frequency of the carrier wave. The Nyquist-Shannon sampling theorem requires the sampling frequency to be twice that of the input bandwidth to reconstruct the signal from its samples, but this condition is insufficient in the case of switching audio amplifiers, as too low of a sampling frequency will make the carrier wave hard to filter out and create lots of ripples in the output signal. Therefore a sampling frequency of at least 10 times the bandwidth is a more suitable condition if audio quality is of concern [3].

2.4 Switching stage

The power stage, also known as the switching stage, amplifies the PWM and consists of a number of MOSFETs; two in the case of a half-bridge design and four in a full-bridge design.

In a half-bridge PMOS/NMOS design, the source of the PMOS is connected to the supply voltage and is generally referred to as the "high-side" MOSFET, while the source of the NMOS is usually connected to ground or negative supply voltage and is known as the "low-side" MOSFET. When the PWM is low, the high-side MOSFET is on and connects the output to the supply voltage. When the PWM is high, the low-side is on which connects the output to ground or negative supply voltage. This yields an amplified PWM signal. It is possible to build a half-bridge class D amplifier with two NMOS transistors, but it requires more level-shifting etc. than the PMOS/NMOS design.

Because PWM is used, the MOSFETs will be either in their cut-off or linear regions where they dissipate little power and will spend time in their saturated regions only when they are switching modes. This is the reason why class D amplifiers are highly efficient. The switching time needs to be kept as low as possible to minimize switching losses. Slower MOSFETs require longer dead time. [3].

To ensure high efficiency the internal resistance between drain and source (R_{DSon}) of the MOSFETs must be low.

2.5 Dead time

If one MOSFET turns on at the same time as the other turns off, a shoot-through current will pass through the switching stage to ground. This is due to MOSFETs not switching modes instantly, causing a short circuit between supply voltage and ground. If a short circuit happens, large amounts of heat may develop, causing component damage and high power losses. Therefore, to avoid the shoot-through current a time delay (dead time) needs to be implemented between the switch modes of the MOSFET. The dead time is achieved by manipulating the PWM, but this causes distortion. Because of this the dead time should be minimized.

2.6 Level shifting and MOSFET drivers

A level shifter moves the signal from one logic level to another. The PWM produced by the comparator cannot drive both MOSFETs because of their difference in source voltage. To compensate, the PWM must be level shifted for one of the MOSFETs. For the PMOS the PWM has to be shifted to a level above the switching stage supply voltage to ensure it is in the cut-off region.

To decrease the time between the on and off modes of the MOSFETS, one or more drivers may be used. A driver amplifies the current that flows to the gate of a MOSFET, charging the gate capacitor quicker.

2.7 Low-pass filter

In order to recover the amplified input signal from the PWM, the high frequency triangle wave components must be filtered out using a low-pass filter. The roll-off of the filter has to be fast, since a slow roll-off might leave some of the high frequency triangle wave components behind. If a DC component is present in the amplified signal it must be removed to not damage the speaker.

3 Method

3.1 Simulations in LTspice

The software LTspice was used to design and simulate the different stages of the amplifier separately as well as the amplifier as a whole. For initial testing the "PULSE" option of the voltage source was used to generate a triangle wave in place of the triangle wave generator, together with the built-in LT1720 comparator model and a sine wave. As our triangle wave generator and comparator designs were finalized, they were slotted into the schematic.

After the PMOS/NMOS switching stage was working as intended, the level shifter and drivers were implemented. When the PWM was properly amplified the low-pass filter and dead time generator were added. The dead time had to be adjusted several times during the refinement of the design. The NMOS/NMOS solution was also tested but it was abandoned due to its complexity.

3.2 Construction

After the full amplifier design worked as intended in the simulations, most of it was constructed on breadboards as seen in fig. 2. Initially, two power supplies were utilized; the TTi EL183 as negative voltage supply and the built-in power supply of the Metex MS-9150 function generator for the positive voltage supply. After altering the circuit to accept single-supply operation the MS-9150 was used exclusively.

Since the simulations showed current spikes reaching 2 A in the switching stage and the breadboards used for the other stages were rated for ~0.5 A, the MOSFETs, filter components and voltage regulators involved in the switching stage were soldered to a perfboard (fig. 2) able to handle more current.

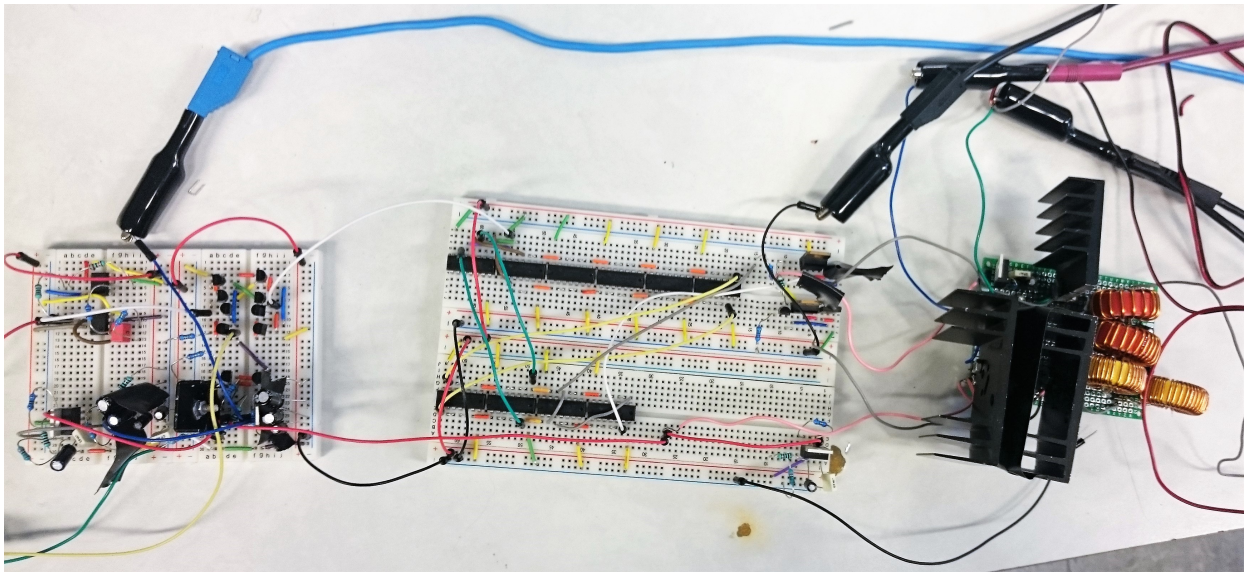

Figure 2: The full amplifier on multiple connected breadboards and a perfboard.

Multiple units of the digital oscilloscope Rohde & Schwarz HMO1002 were utilized to measure the aforementioned triangle wave, PWM, input and output signals etc. The oscilloscopes had an input impedance of 1 MΩ, allowing accurate measurements since the resistances in the circuit were rather low.

For initial testing of the full amplifier, a 4 Ω high current resistor was used. When the output signal quality had been tweaked enough to be listenable an old 6 Ω speaker was connected. The speaker and its specification used is shown in fig. 3 and fig. 4.

Figure 3: The speaker used for testing sound quality.

Figure 4: The speaker specifications.

3.3 PCB design and assembly

A PCB for the amplifier was designed in the EDA software suite KiCad and the full amplifier KiCad schematic can be found in Appendix B. The circuit was drawn in EESchema and then the layout was done in PCBnew, both subprograms to KiCad. The areas of the board without copper tracks were utilized as a ground plane. The PCB design was then printed on photo paper and with heat the ink was fastened to a copper plated plastic board. The PCB was etched with a solution that dissolved all the copper not covered with ink, leaving only the desired connections. Holes were drilled and the components were soldered on. The complete PCB can be seen in fig. 5 and the chassis (an old computer case) in which it was mounted is shown in fig. 6. Lastly, a heatsink for the MOSFETs and most of the voltage regulators was mounted.

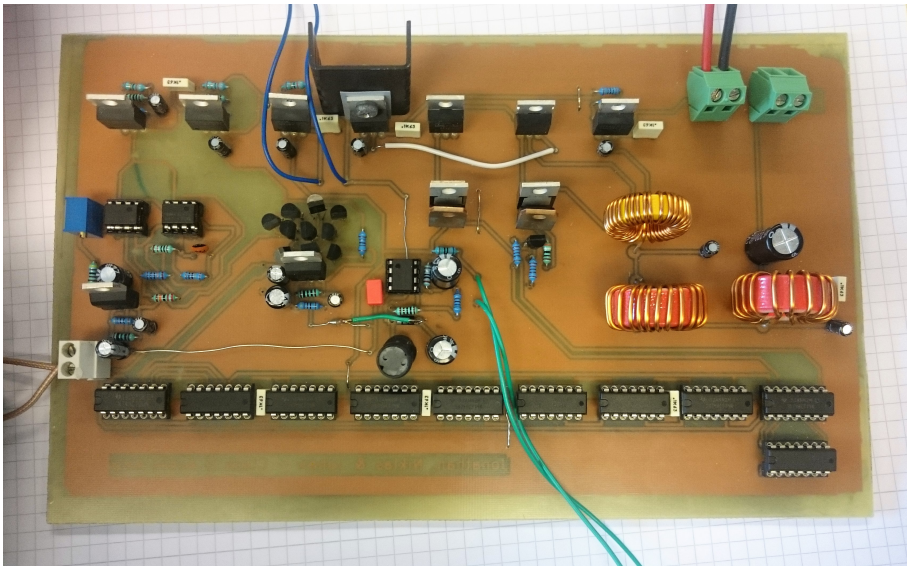

Figure 5: The amplifier PCB with mounted components.

Figure 6: The chassis in which the PCB was mounted, with a power switch and a standby switch.

3.4 Efficiency

To measure the efficiency of the amplifier the input power, P_{in} and output power P_{out} were measured to deduce the efficiency $\eta = \frac{P_{out}}{P_{in}}$. To measure P_{in}, a 2 Ω resistor was connected between supply voltage and the input. The voltage drop over the 2 Ω resistor was measured to calculate the current. P_{out} was evaluated the same way, but with a 4 Ω load. A computer playing sine waves at a very high volume was used as input signal.

4 Design

4.1 Preliminary design

4.1.1 Triangle wave generator

The triangle wave generator shown in figure 7 utilizes two op-amps, one functioning as a non-inverting Schmitt trigger (U1) and the other as an integrator (U2). A Schmitt trigger is essentially a comparator with hysteresis; it outputs a logic value until the input changes sufficiently to trigger a change to the other logic value. "Non-inverting" refers to the output voltage having the same polarity as the input voltage. The Schmitt trigger will output a square wave, which the integrator converts to a triangle wave.

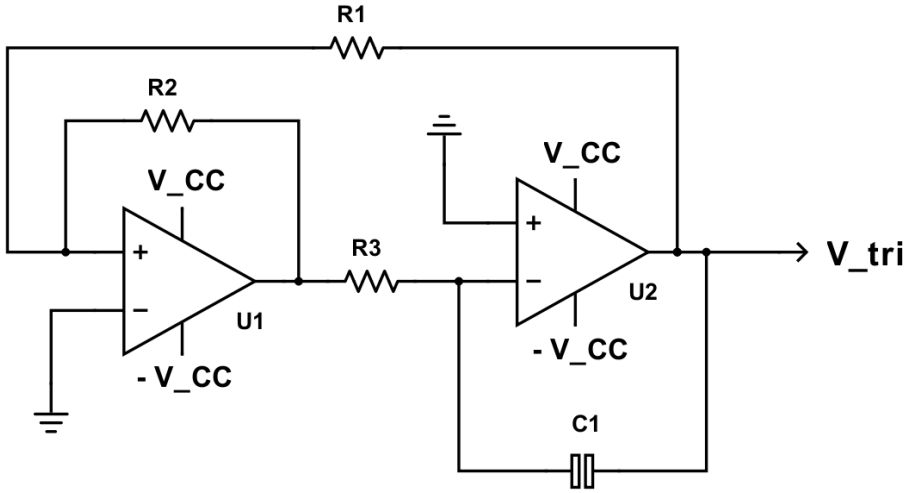

Figure 7: The two op-amp triangle wave generator.

The output amplitude V_{tri} is the level where the Schmitt trigger output switches from one logic level to another. It is given by

$$V_{tri} = V_{in} \cdot \frac{R_1}{R_2}. \tag{1}$$

The frequency of the triangle wave can be calculated with the formula

$$f = \frac{1}{4R_3C_1}\frac{V_{in}}{V_{tri}}. \tag{2}$$

Since it is dependent on R_3, C_1 and V_{tri}, the frequency is affected by the values of all passive components.

The circuit is able to self-oscillate since the output of the Schmitt trigger must be either low or high when the circuit is powered on; when it is high, the integrator will output a falling ramp and for a low Schmitt trigger output, the integrator will produce a rising ramp. The output of the integrator is fed back to the input of the Schmitt trigger, keeping the oscillation going.

The goal was to create a triangle wave with a frequency around 200 kHz or more, as this would fulfill the aforementioned recommendation of a sampling frequency ten times the bandwidth (in this case the audible frequency range). Such a high frequency requires the op-amps to have high enough slew rates and bandwidth.

4.1.2 Comparator

The design of the comparator (fig. 8) was found in [3]. MOSFETs were substituted for BJTs, mostly due to material cost. A tail current for the comparator is generated in the current mirror comprised of Q9, Q10 and R_4.

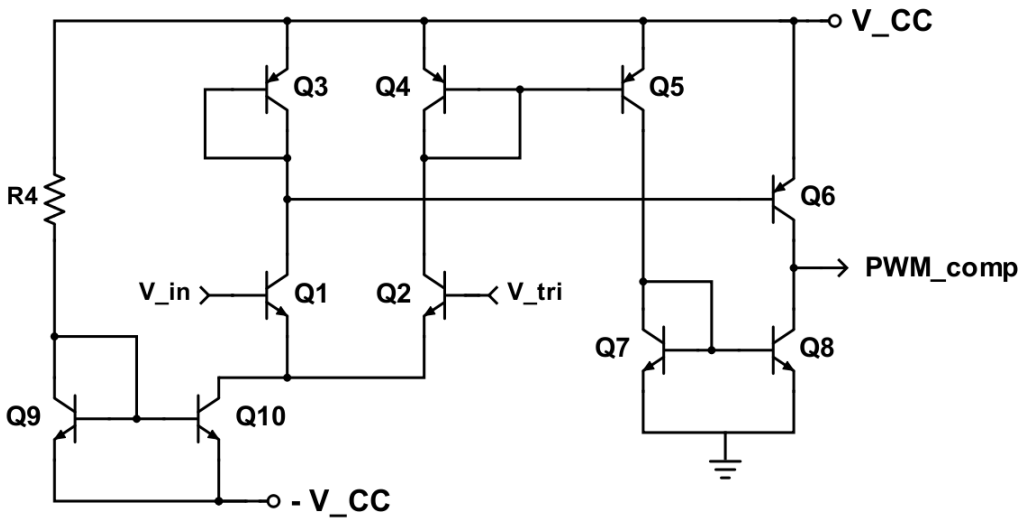

Figure 8: The BJT-based comparator and current mirror, with input signal V_{in} and triangle wave input V_{tri} labeled.

The comparator compares V_{in} and V_{tri} and outputs V_{CC} when the difference between them is positive and 0 V (ground) when it is negative. This will create the PWM signal. It is important that the audio signal is bounded within the triangle wave, as clipping will occur if the amplitude of the signal exceeds that of the carrier wave [3]; if the input is higher in amplitude than the triangle, the comparator will output a constant logic high in the PWM until the input signal is lowered beneath the maximum amplitude of the triangle wave. This also happens when the input signal is lower than the minimum voltage of the triangle wave. An example of this can be seen in fig. 10 where arrows point at the "holes" created in the scenario shown in fig. 9.

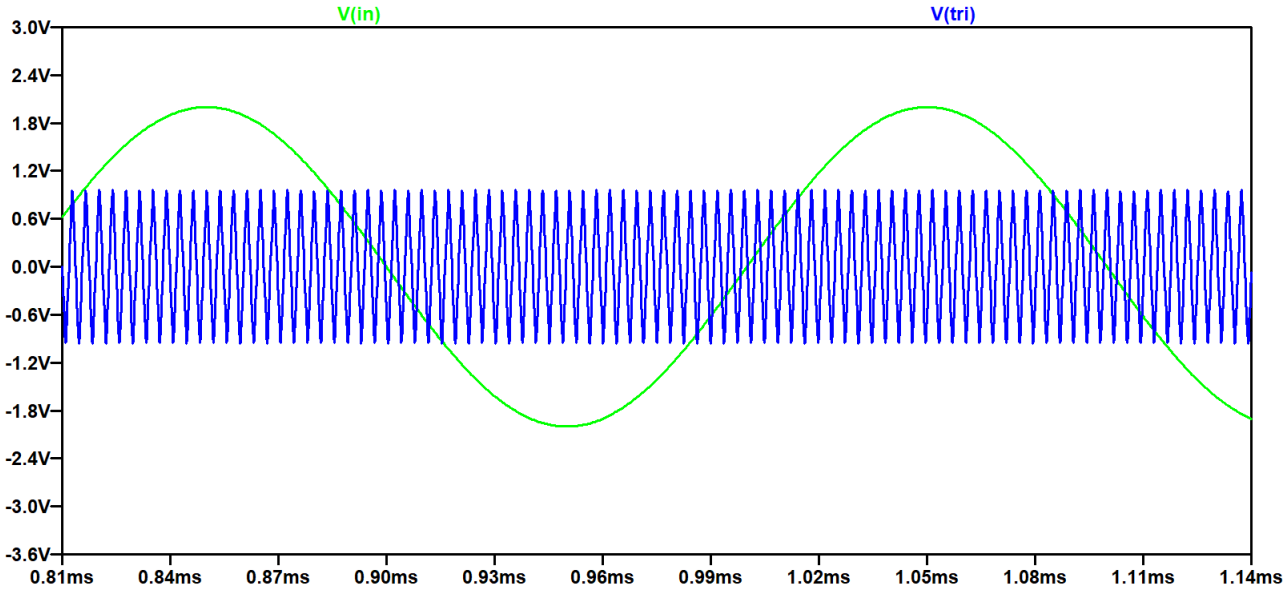

Figure 9: An input sine wave that is not bounded within the triangle wave.

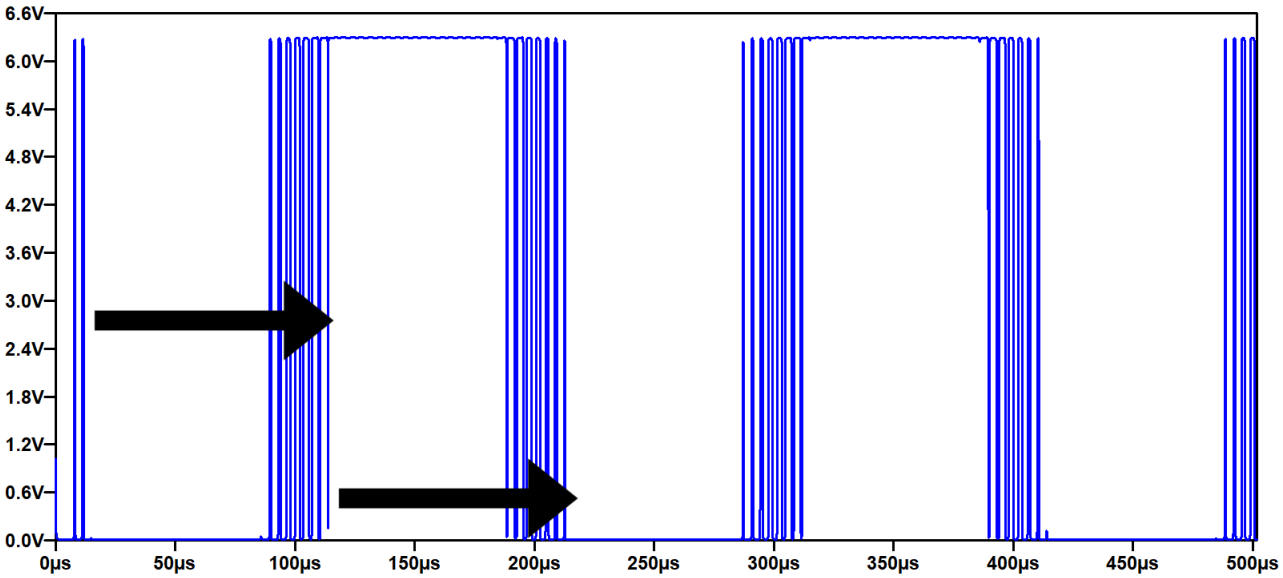

Figure 10: The "holes" created in the PWM when the sine wave is not bounded within the triangle wave.

4.1.3 Dead time generator

The dead time generator in fig. 11 was implemented with a series of logic gates, a design found in [3]. The propagation delay of the inverters is exploited to create dead time. The dead time created needs to be large enough to prevent a shoot-through current and to phase shift the low-side PWM to compensate for the phase shift of the level shifter. The input and the inverted input is fed into two NAND gates together with a feedback, which is the same phase-shifted signal. This shortens the on-duration of the PWM. The inverted signal is inverted back.

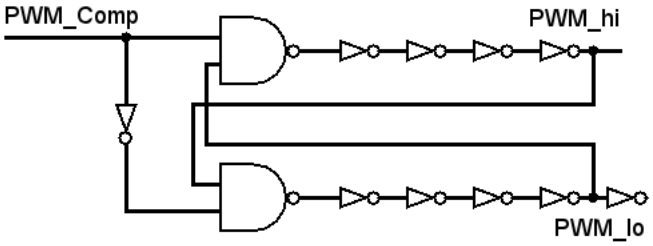

Figure 11: The dead time generator based on logic gates.

4.1.4 Level shifter and MOSFET drivers

To level shift the PWM a simple inverting BJT-based shifter (fig. 12) was constructed. It consists of three resistors and an NPN transistor. When the PWM is applied to the base of the NPN the logic high level of the PWM will cause the NPN to conduct, creating a voltage divider with R_6 and R_7, which shifts the logic high to a given level. When the NPN is switched off the output will be connected to V_{CC} through R_6. Because the level shifter is connected to the bases of the driver transistors, very little current will flow and the voltage drop over R_6 will be negligible. The output voltage will then be equal to V_{CC}, thus inverting the PWM. The new high value of the PWM is given by the supply voltage and the new low value is given by the formula

$$V_{new\,low} = V_{CC} - (V_{old\,high} - 0.7) \cdot \frac{\beta R_6}{R_5 + R_7(1+\beta)} \tag{3}$$

where β is the common-emitter current gain, V_{CC} is the supply voltage and $V_{old\,high}$ is the the maximum value of the PWM before the level shifter.

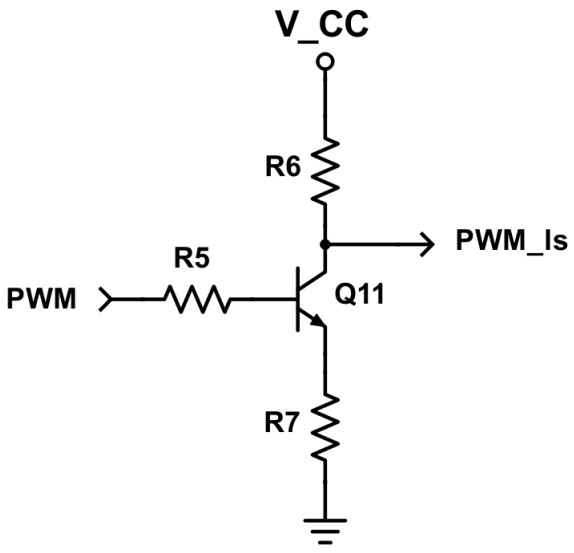

Figure 12: The BJT inverting level shifter.

The driver (fig. 13) is a push-pull stage consisting of one PNP and one NPN. When the PWM is on the PNP will conduct current to the output and when the PWM is off the NPN will conduct. The low resistance of the BJTs will increase the current flow while maintaining the same voltage.

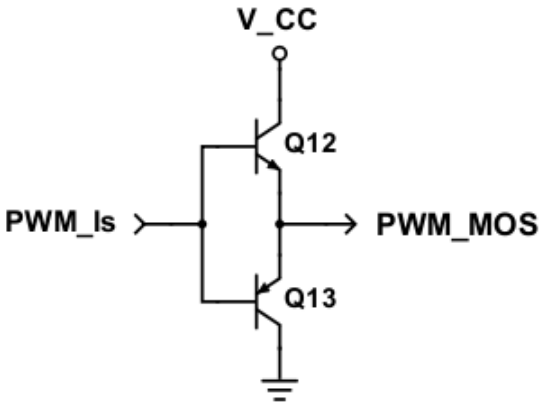

Figure 13: The BJT-based push-pull gate driver.

4.1.5 Switching stage

In fig. 14 the switching stage is shown. Freewheeling diodes were implemented to avoid current spikes when a MOSFET turns off due to the inductive load.

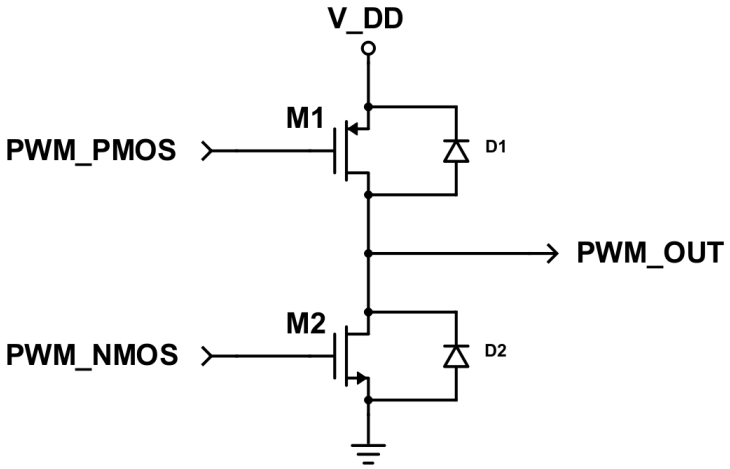

Figure 14: The switching stage consisting of one NMOS and one PMOS transistor.

4.1.6 Low-pass filter and load

A fourth order Butterworth low-pass filter, shown in fig. 15, was chosen. A filter of lesser order can be used, but the roll-off will be slower, making it harder to filter out the triangle wave frequency component. A capacitor was used in series with R_{load} to remove any DC component.

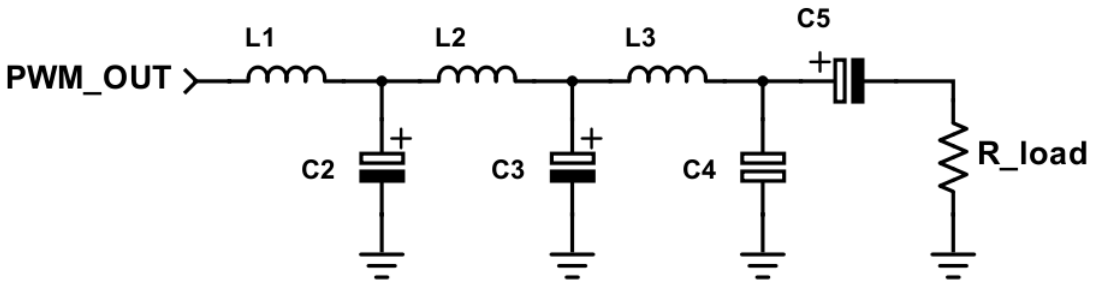

Figure 15: The low-pass output filter with load.

4.1.7 Full LTspice schematic

The schematic for the full amplifier simulation can be seen in fig. 16.

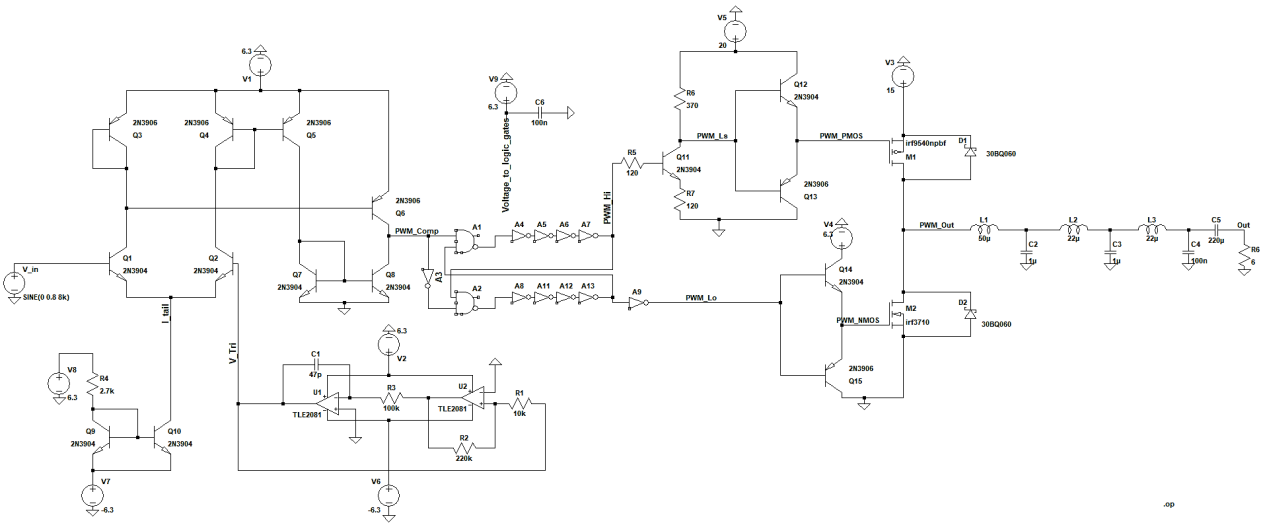

Figure 16: The full amplifier schematic in LTspice.

4.2 Final design

Component models and values can be found in Appendix A .

It was found that the comparator was very sensitive to offsets in the triangle wave. Even small offsets ($100 - 200$ mV) caused the transistors in the comparator to slowly heat up and draw more current, in some cases destroying one or more transistors. This was solved by connecting a 100 kΩ potentiometer to the Schmitt trigger op-amp (U1) to adjust the offset of the square wave and in turn, the offset of the triangle wave output. Centering the triangle wave stabilized the temperatures and currents in the comparator. Further unexpected behavior came from the comparator when the input cable was left unconnected; the input node was pushed down to roughly the same level as the bottom part of the triangle wave. This made the comparator always output 0 V, since the triangle wave was always higher in amplitude than the input. When this happened, the low-side MOSFET was constantly in its on state and the high-side constantly in its off state, essentially muting the output. This behavior did not seem harmful to the amplifier or

the speaker and could be mitigated by coupling a resistor between input and ground. The BJTs used in the comparator were 2N3904 and 2N3906. They are cheap yet fast and able to handle the current in the comparator, making them suitable for a comparator like this.

The op-amp model used was TLE2081CP, it has the speed and the slew rate required for the triangle wave generator to function.

It was noted that the speaker would pop when powering the positive voltage supply on and off. To reduce this pop a switch was connected to the dead time generator, turning it on and off. This way the output could be muted, since no signal could come through from the comparator and the switching stage MOSFETs stayed in their off states. This also helped muting when connecting the audio cable, not letting through the said pops and noises. In practice, the switch enables a standby mode with lower power consumption. However, this solution only removed the popping sound when turning the amplifier off, while the pop when turning the amplifier on (with standby enabled) became less intense and occurred only the first time the switch was toggled after the main power supply was turned on.

LM338T variable voltage regulators were used to get cleaner positive voltages (6.3, 15 and 20 V) throughout the circuit and the regulator L7905 supplied -6.3 V for the triangle wave generator, comparator and low-side driver. 6.3 V was chosen because of regulator specifications and due to the fact that the low-side MOSFET needed more voltage than its threshold voltage (with some margin). Additionally, the logic gates could only handle up to 7 V supply voltage. 15 V was used in the switching stage and 20 V for the level shifter and high-side driver.

To power the amplifier with a single supply, MC34063 was used. It converts positive voltage to negative voltage with a high switching frequency (far higher than the cut-off of the low-pass filter). Decoupling capacitors were placed between the two supply voltage rails in close proximity to all ICs, including the MC340630, to minimize noise.

IRF9540 was used as high-side while IRF3710 was used as low-side. They both have a threshold voltage of ± 4 V. The IRF3710 has $R_{DSon} = 23$ mΩ which is very low, while the IRF9540 R_{DSon} is 117 mΩ. These MOSFETs were chosen because of their fast switching speeds and high tolerances. A high tolerance for current is needed as large currents may flow through the stage. The level shifting was done from 0-6.3 V to 7-20 V.

To achieve a long enough dead time, more inverters than those shown in fig. 11 were used.

4.3 PCB design

The PCB design was essentially the same circuit as on the breadboards and can be found in Appendix B. The major difference was that instead of the MS-9150, a 24 V laptop power supply with a DC adapter was used. A stereo input jack was used but since the amplifier operates in mono, the channels were summed together according to fig 17.

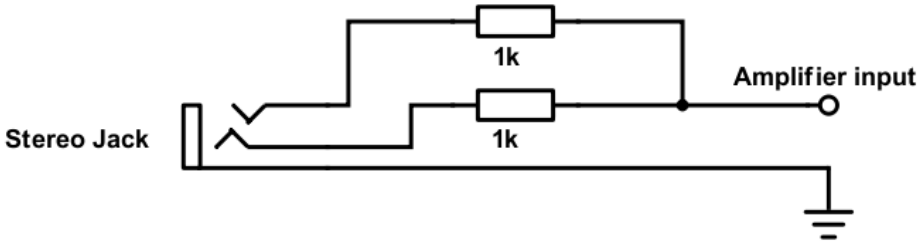

Figure 17: The stereo signal from the audio jack summed to mono before the amplifier input.

5 Results

5.1 Simulation results

The triangle wave alongside the sine wave input is shown in fig. 18 and fig. 19.

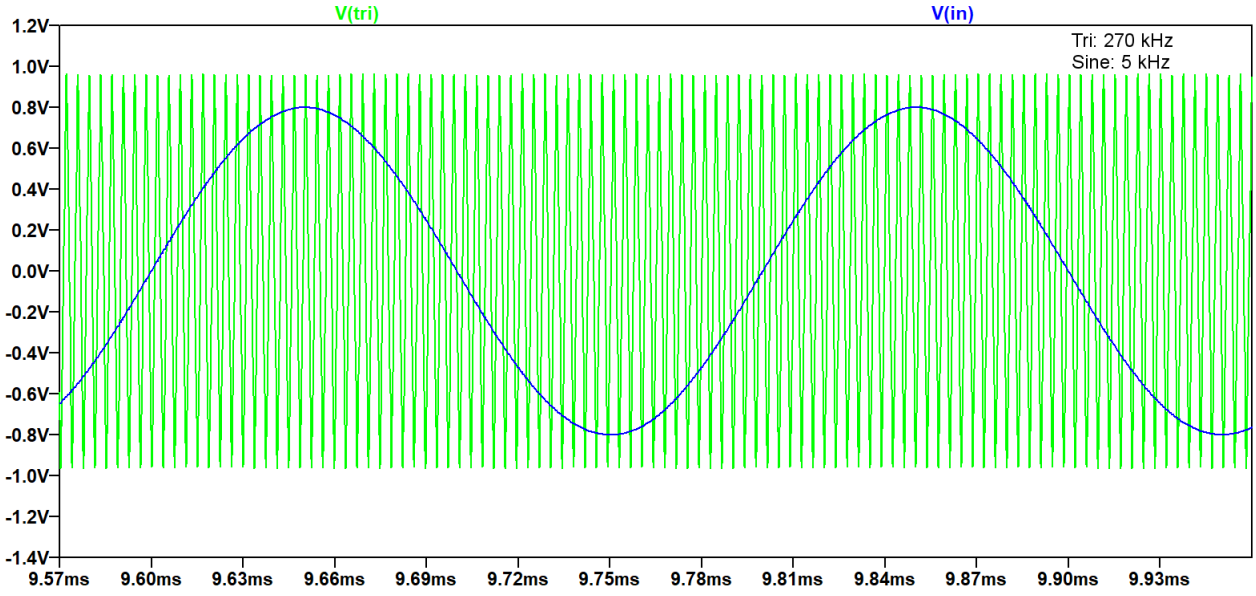

Figure 18: Simulated 5 kHz sine wave (blue) and 270 kHz triangle wave (green).

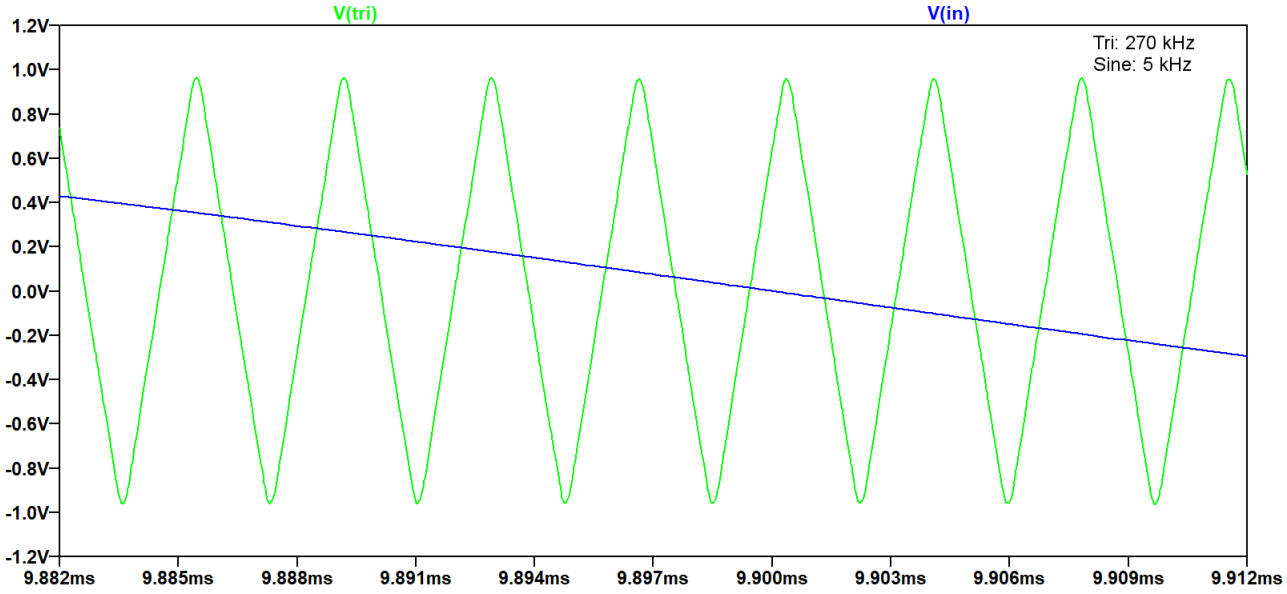

Figure 19: Close-up of the simulated 5 kHz sine wave (blue) and the 270 kHz triangle wave (green).

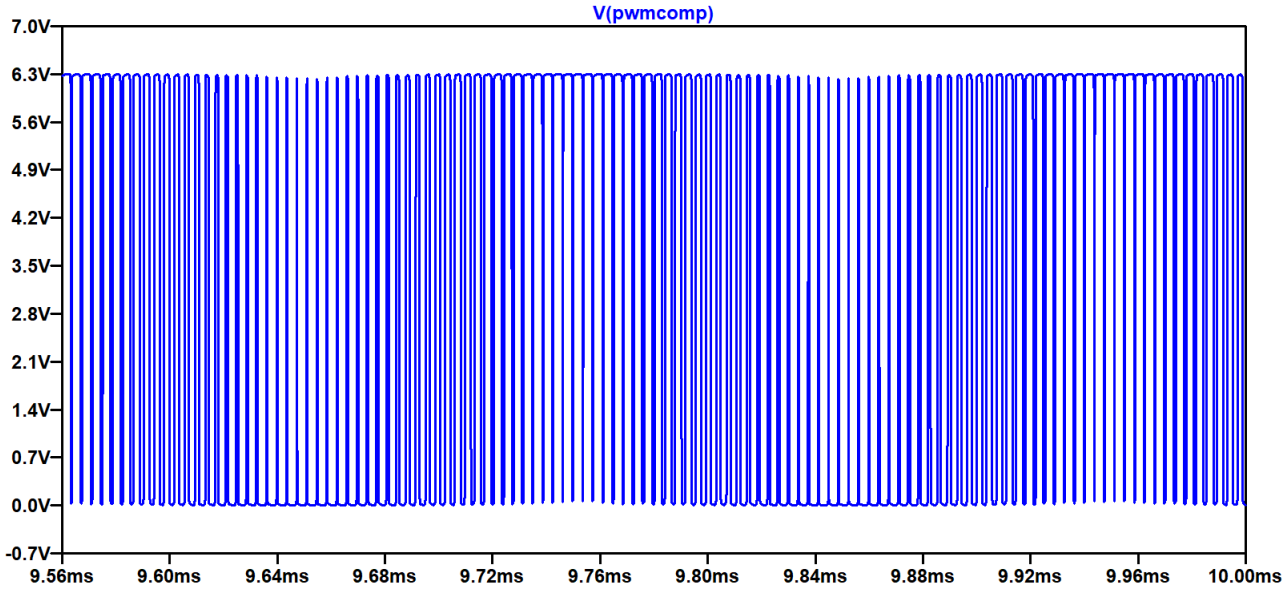

Figure 20: The PWM generated from the 5 kHz sine wave during the same time frame as fig. 18.

A sine wave input and its amplified output is shown in fig. 21 and 22.

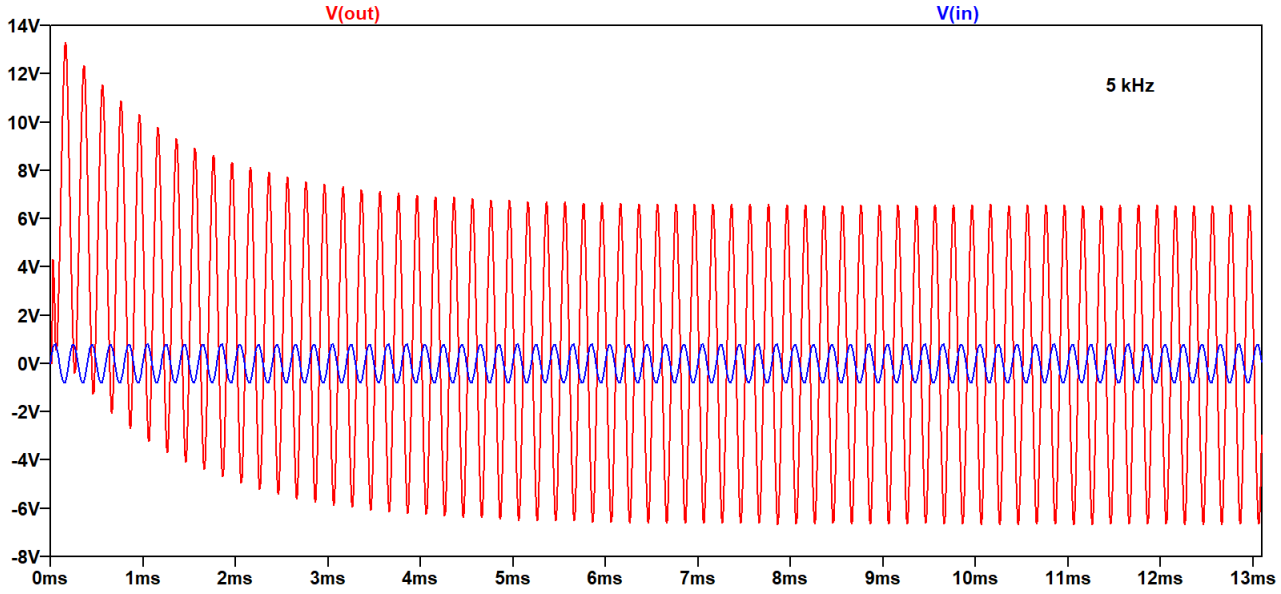

Figure 21: Simulated 5 kHz sine wave input (blue) and the amplified signal (red), with transient response.

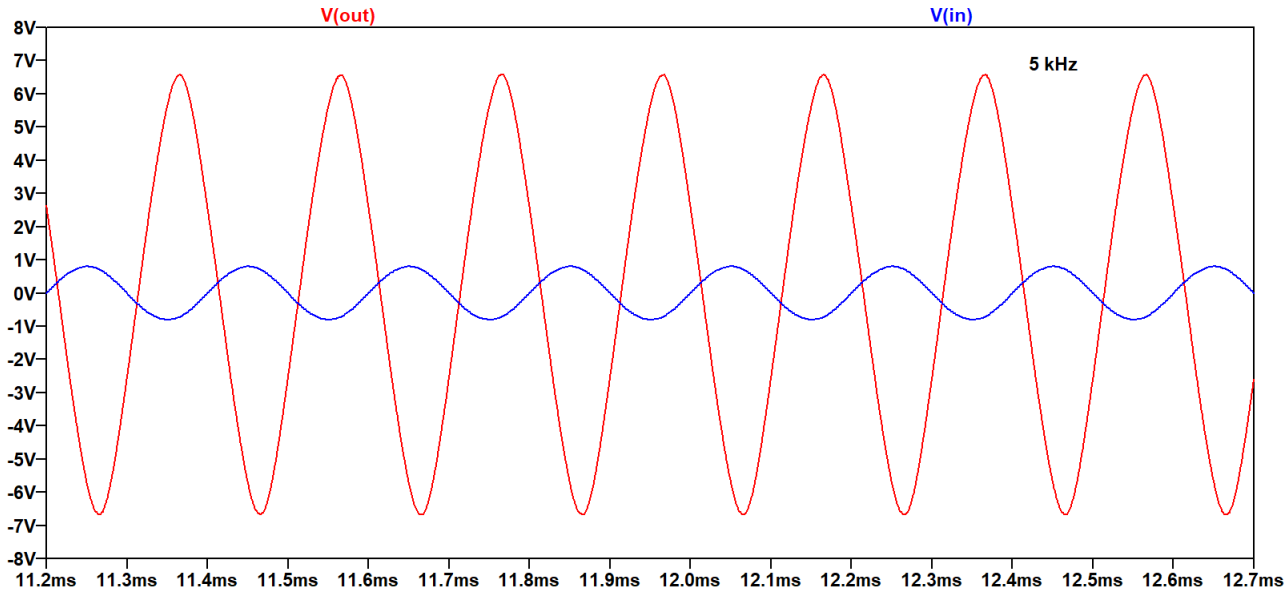

Figure 22: Close-up of the simulated 5 kHz sine wave input (blue) and the amplified signal (red) at its steady state.

The PWM signal from the switching stage is shown in fig. 23.

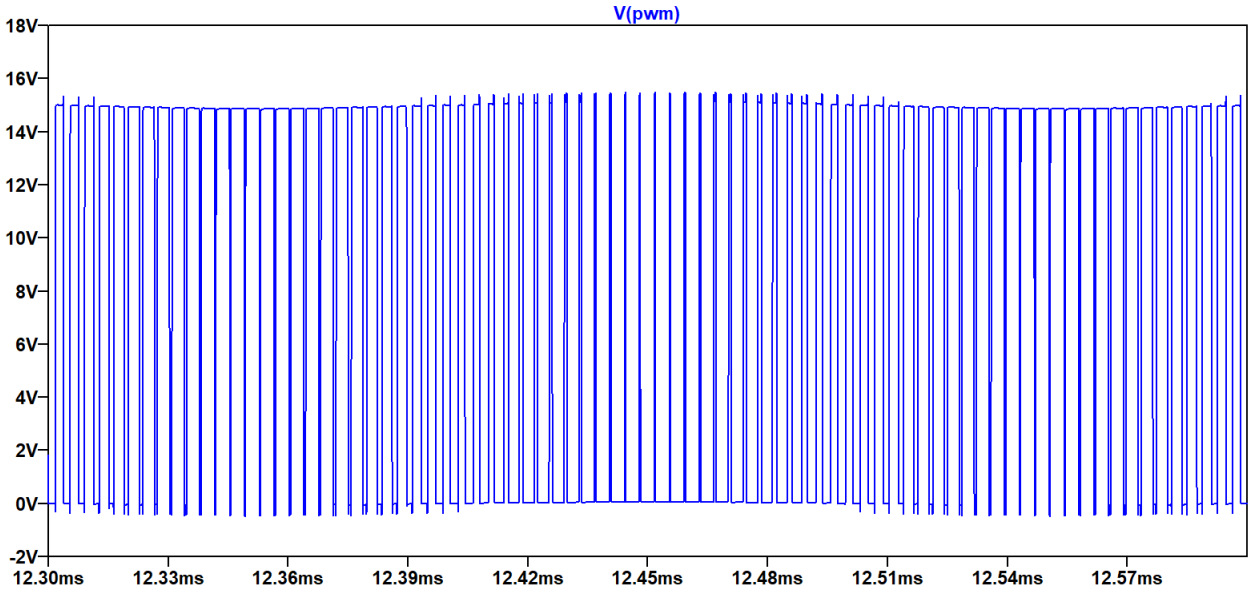

Figure 23: Simulated PWM signal with 5 kHz sine wave input.

The frequency response of the filter can be seen in fig. 24. It has a lower cut-off frequency of 120 Hz and an upper cut-off frequency of 26.5 kHz. The ripple seen is at 52 kHz and has an attenuation of -5.3 dB. At the frequency of the triangle wave (202 kHz) the attenuation of the filter is -82 dB.

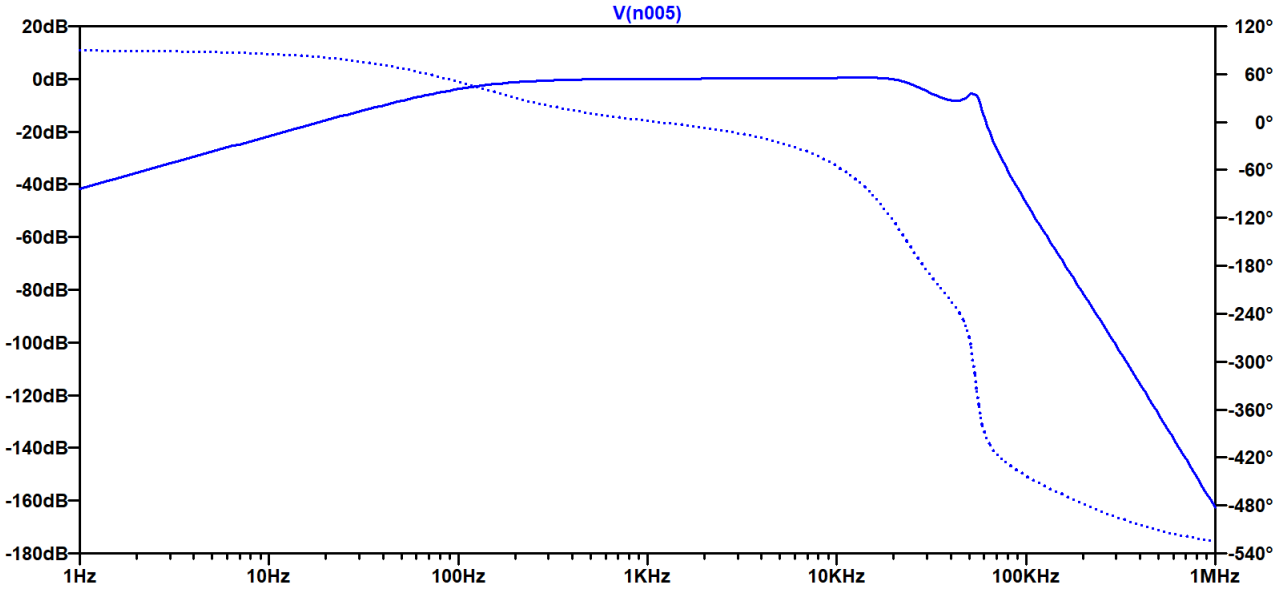

Figure 24: The frequency response (continuous line) and phase response (dotted line) of the output filter.

5.2 Measurements with resistor load

In fig. 25 an input sine wave with frequency 5 kHz alongside the triangle wave with frequency 202 kHz is shown when a 4 Ω resistor was used as load. In fig. 26 a close-up of the setup is shown, where ripples in the input signal are more apparent.

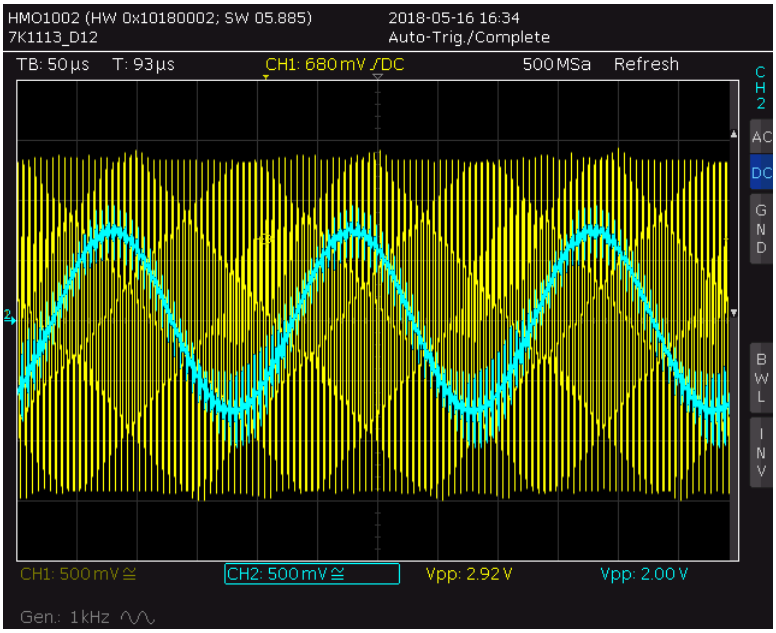

Figure 25: 5 kHz input sine wave (blue) alongside the 202 kHz triangle wave (yellow). Load: Resistor, 4 Ω.

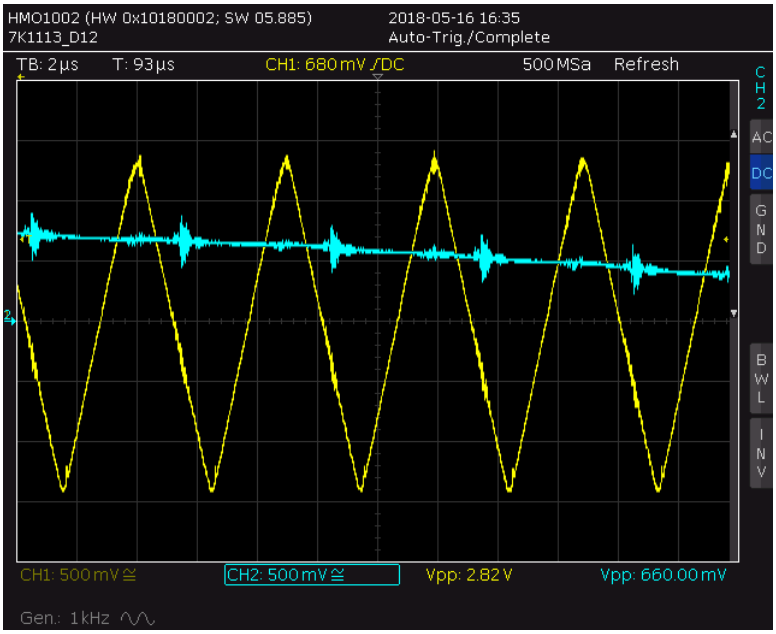

Figure 26: Zoomed-in view of the 5 kHz sine wave (blue) alongside the 202 kHz triangle wave (yellow). Load: Resistor, 4 Ω.

The comparator output PWM can be seen in fig. 27 and in fig. 28, a close-up is shown.

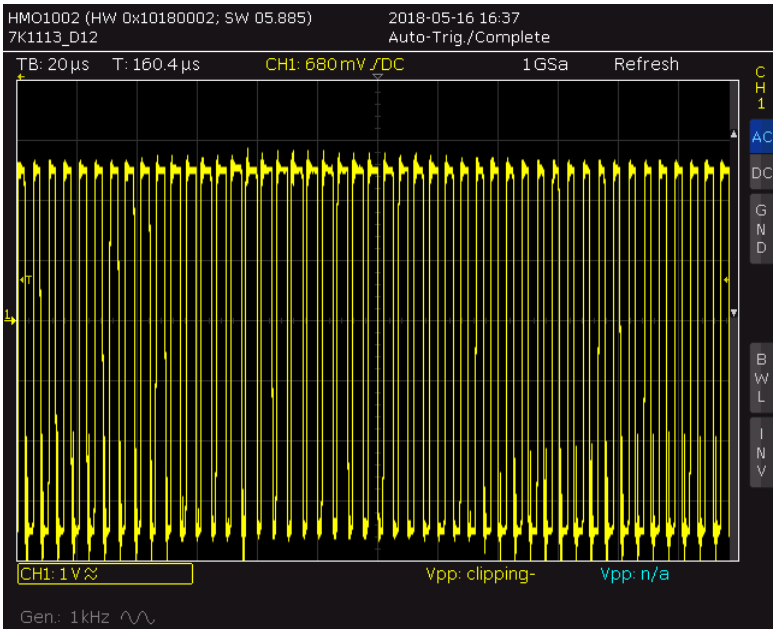

Figure 27: The PWM signal from the comparator. Load: Resistor, 4 Ω.

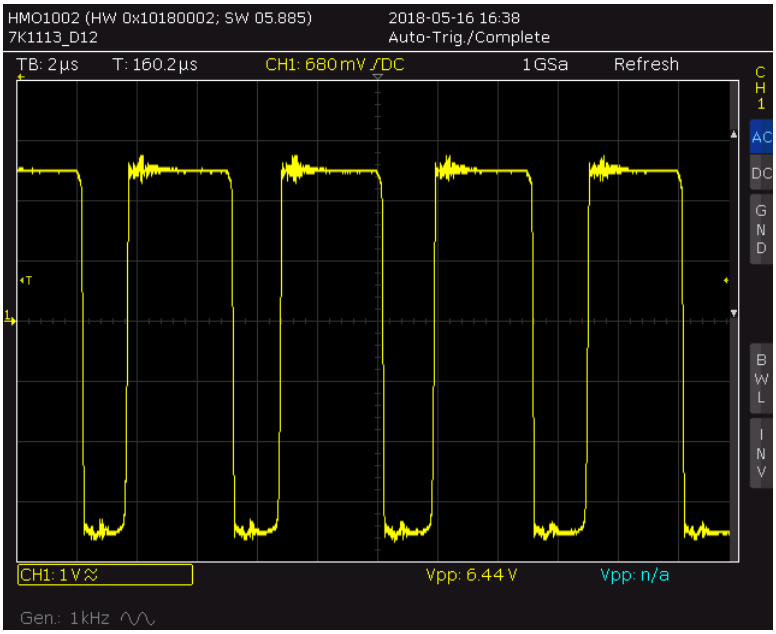

Figure 28: Zoomed-in view of the PWM signal from the comparator. Load: Resistor, 4 Ω.

In fig. 29, the output PWM with a 4 Ω resistor is shown, a lot of ripples can be seen. A closer look at the output PWM is shown in fig. 30.

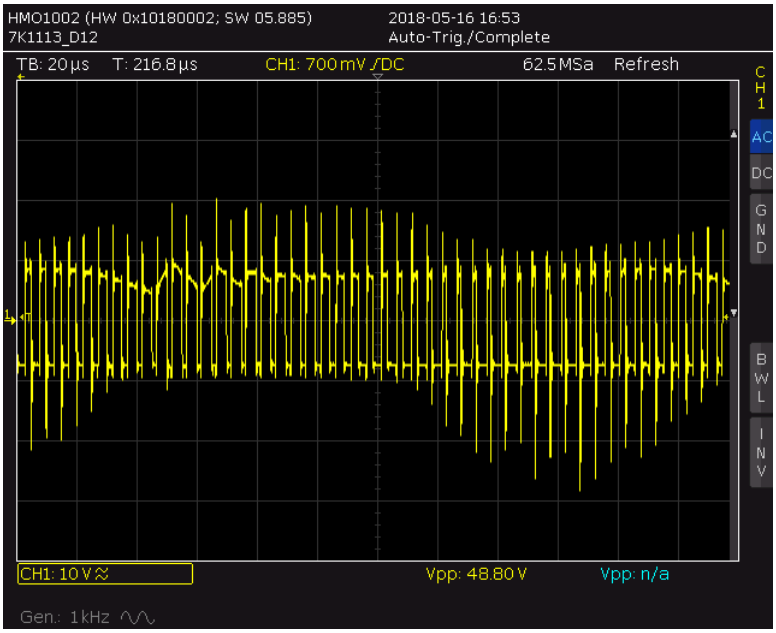

Figure 29: Output PWM signal after switching stage. Load: Resistor, 4 Ω.

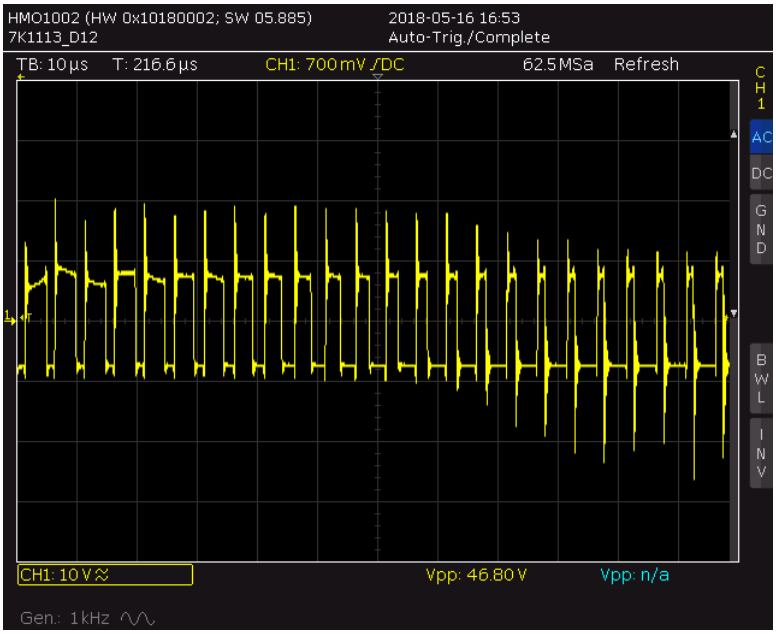

Figure 30: Closer look at the output PWM signal after switching stage. Load: Resistor, 4 Ω.

5.3 Measurements with speaker load

The output PWM when using a speaker can be seen in fig. 31. Zoomed-in views of the PWM are shown in fig. 32 and fig. 33.

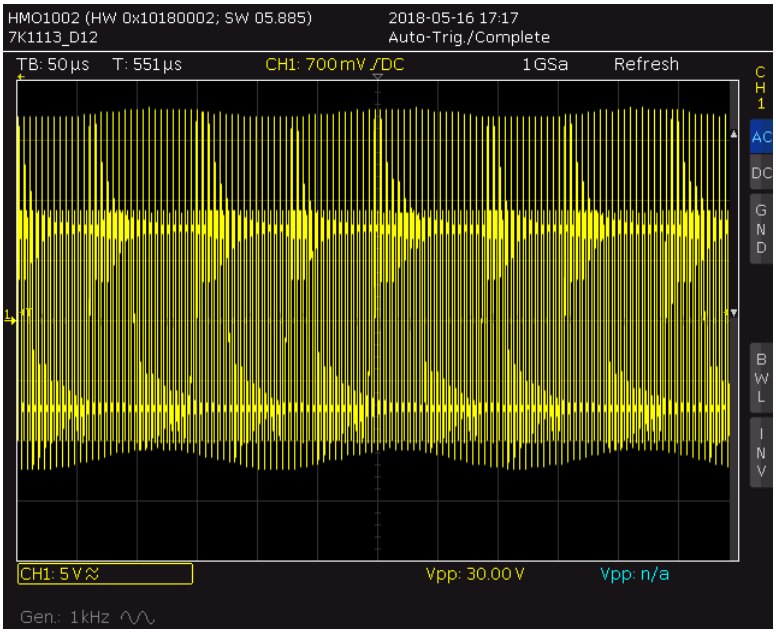

Figure 31: Output PWM signal after switching stage. Load: Speaker, 6 Ω.

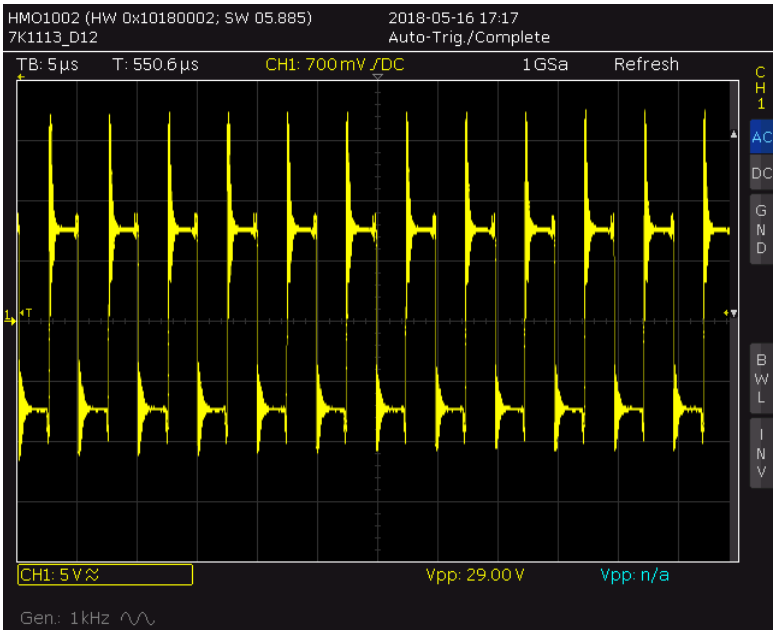

Figure 32: Close-up of the output PWM signal after switching stage. Load: Speaker, 6 Ω.

Figure 33: Extreme close-up of the output PWM signal after the switching stage. Load: Speaker, 6 Ω.

A 5 kHz sine wave input signal and its amplified output signal can be seen in fig. 34. The output has a lot of ripples and a close up of them is shown in fig. 35.

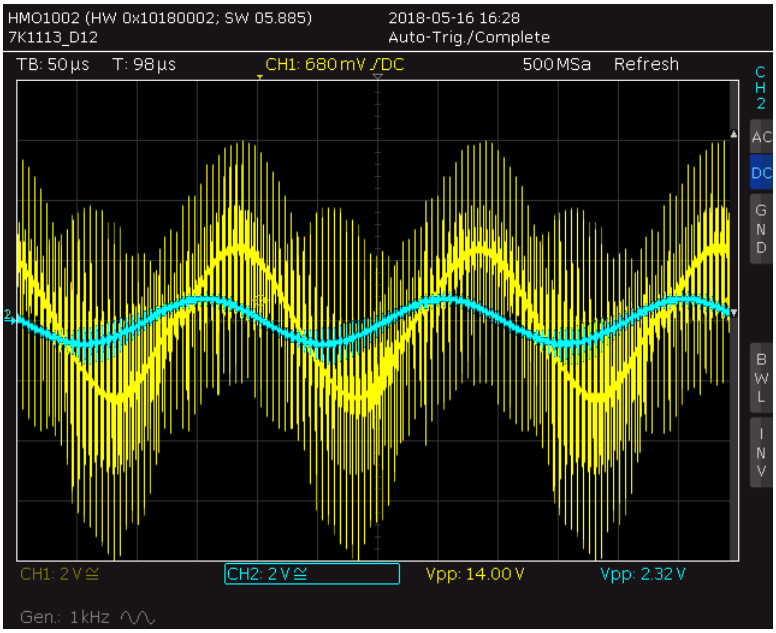

Figure 34: Output signal (yellow) with 5 kHz sine wave input (blue). Load: Speaker, 6 Ω.

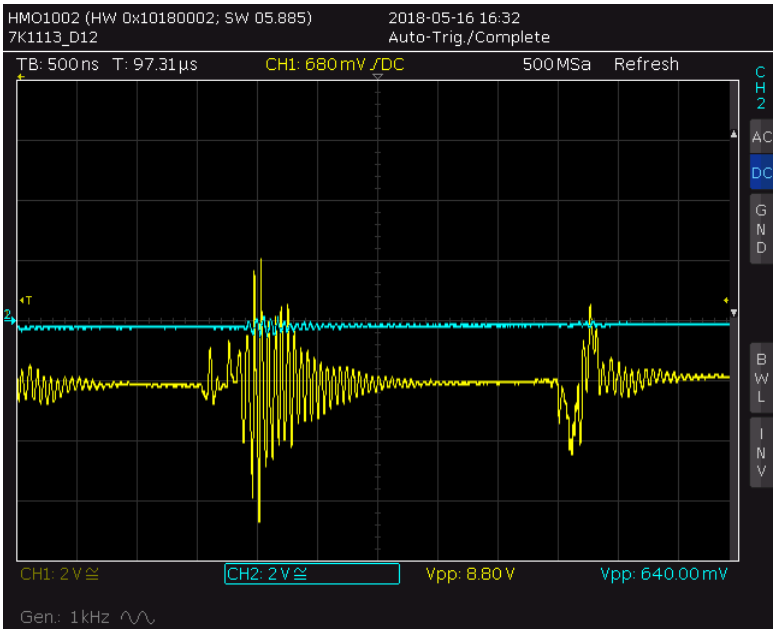

Figure 35: Close-up of the ripples seen in the output signal (fig. 34) with 5 KHz sine wave. Load: Speaker, 6 Ω.

Ripples in the 6.3 V supply voltage for the dead time generator and in the ground plane are shown in fig. 36 and fig. 37.

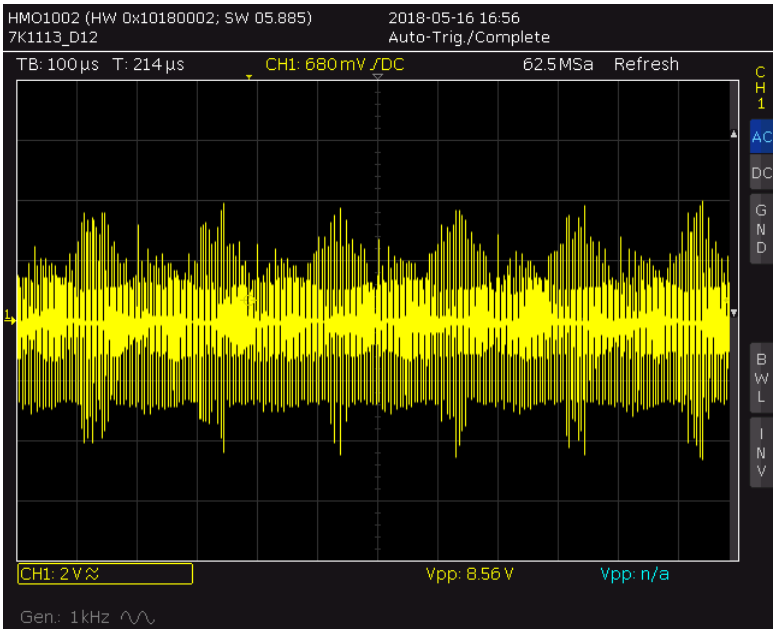

Figure 36: Ripples in the output of the 6.3 V regulator for the dead time generator.

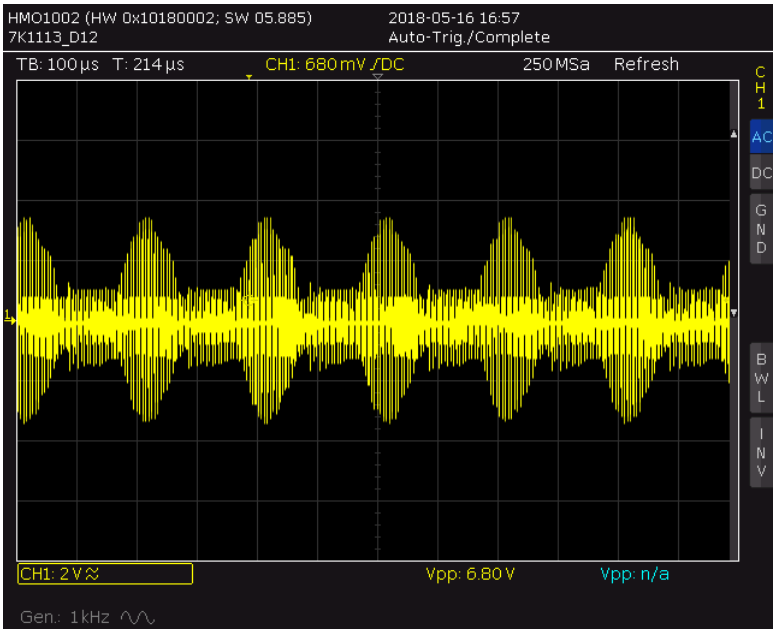

Figure 37: Ripples in the ground plane.

5.4 Measurements with single power supply and speaker load

In fig. 38 and fig. 39 the output PWM is shown.

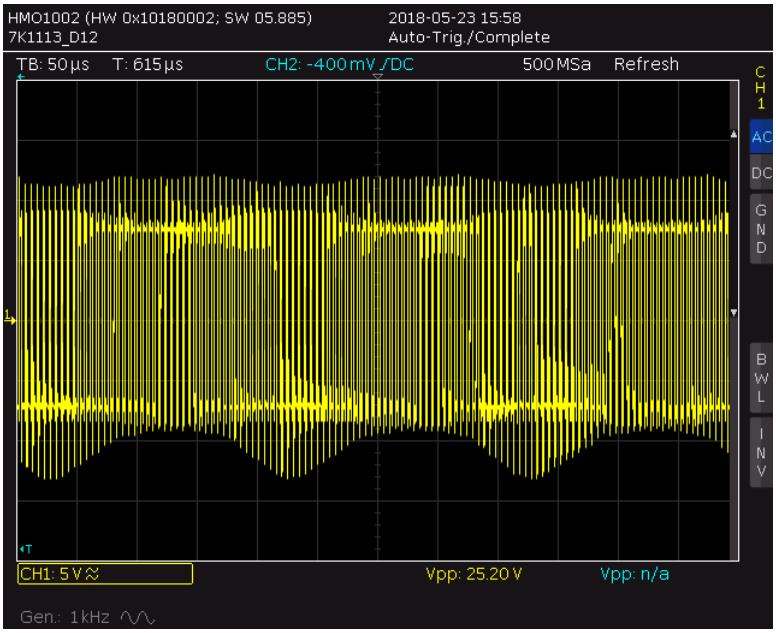

Figure 38: The output PWM after use of the MC34063 circuit. Load: Speaker 6 Ω.

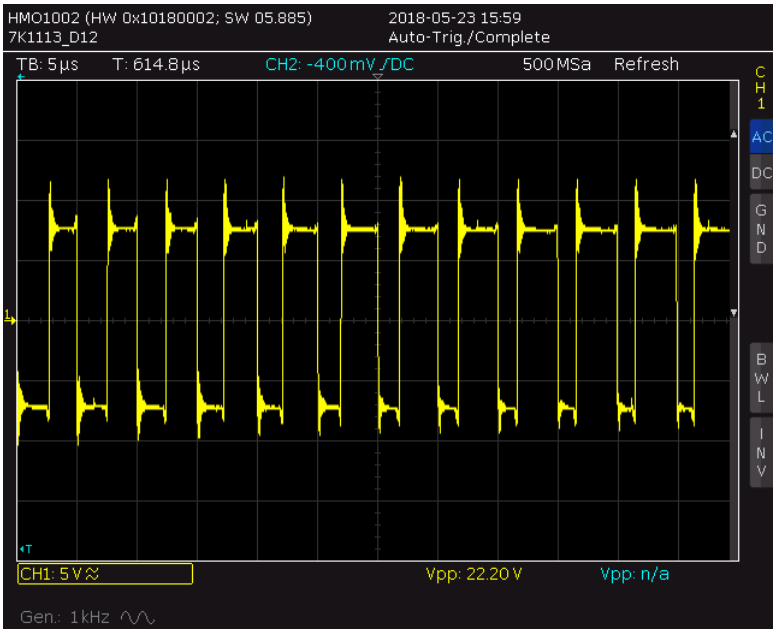

Figure 39: Close-up of the output signal PWM after use of the MC34063 circuit. Load: Speaker 6 Ω.

The input side by side with the output can be seen in fig. 40

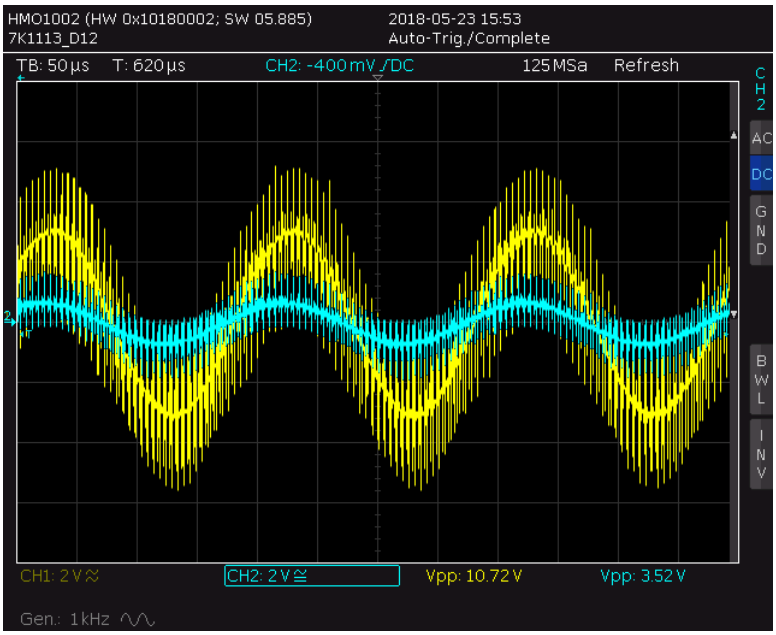

Figure 40: The 5 kHz sine wave input signal (blue) and output signal (yellow) after use of the MC34063 circuit. Load: Speaker 6 Ω.

In fig. 41, a close-up of the high-side and low-side PWM signals after the dead time generator is shown.

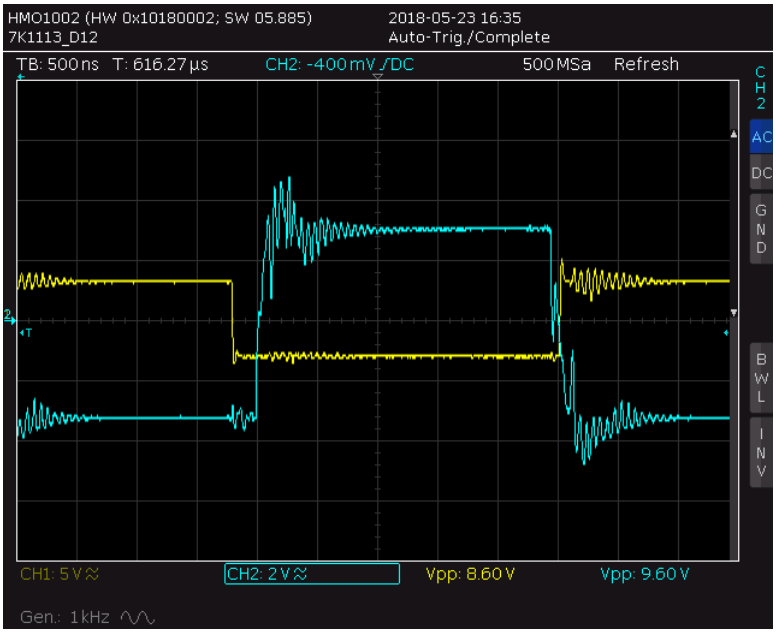

Figure 41: PWM signal to high-side (yellow) and low-side (blue) after dead time generator. Load: Speaker, 6 Ω.

The PWM signal after high-side and low-side drivers is shown in fig. 42. Zoomed-in images of the signals crossing each other are shown in fig. 43 and fig. 44. It can be seen that the high-side (yellow) is switched off (high-side is off at the high logic level) before the low-side (blue) is switched on (low-side is on at the high logic level) and later that the low-side is switched off before the high-side is switched on.

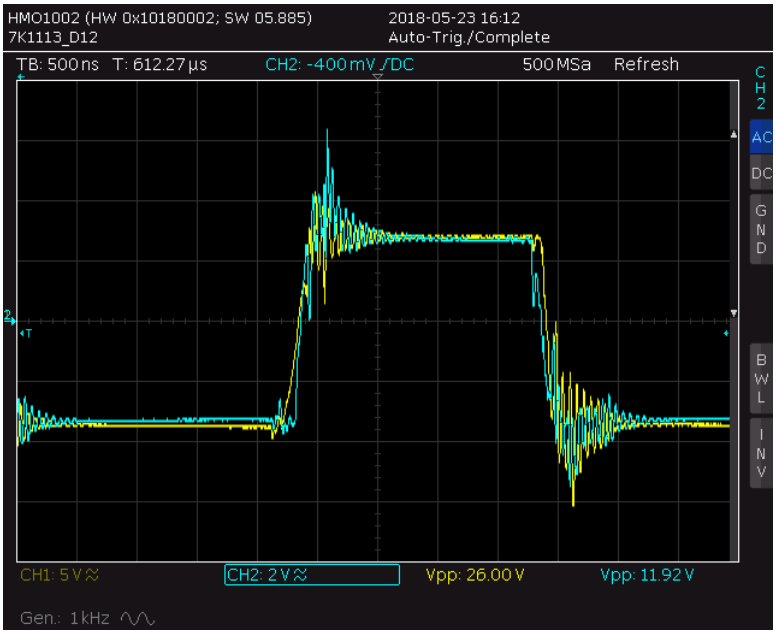

Figure 42: PWM signal to high-side (yellow) and low-side (blue) after drivers. Load: Speaker, 6 Ω.

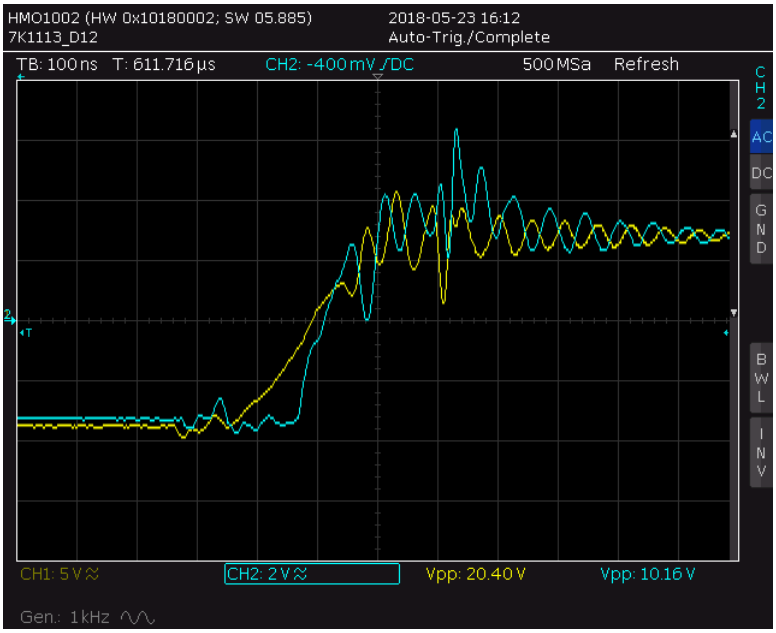

Figure 43: Close-up of the left side of the PWM signal to high-side (yellow) and low-side (blue) after drivers. Load: Speaker, 6 Ω.

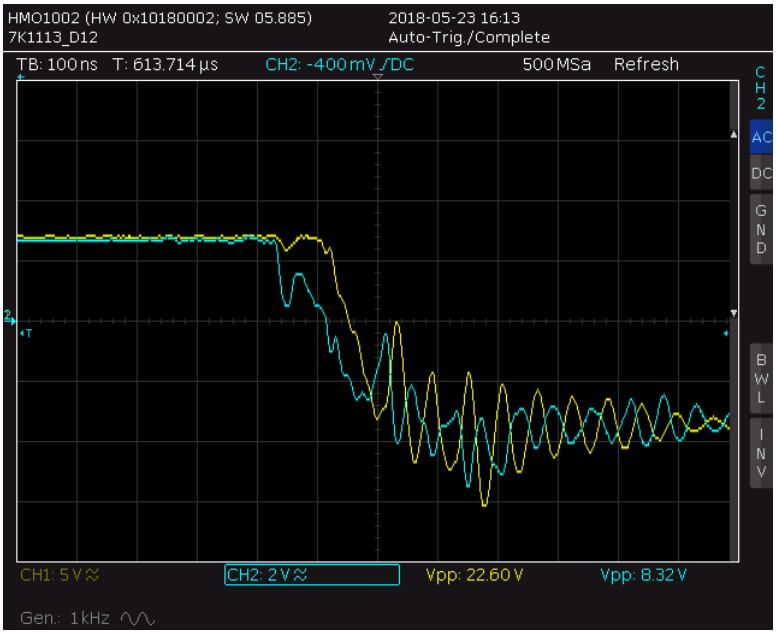

Figure 44: Close-up of the right side of the PWM signal to high-side (yellow) and low-side (blue) after drivers. Load: Speaker, 6 Ω.

The ripples in the 6.3 V rail and the ground plane is shown in fig. 45 and fig. 46

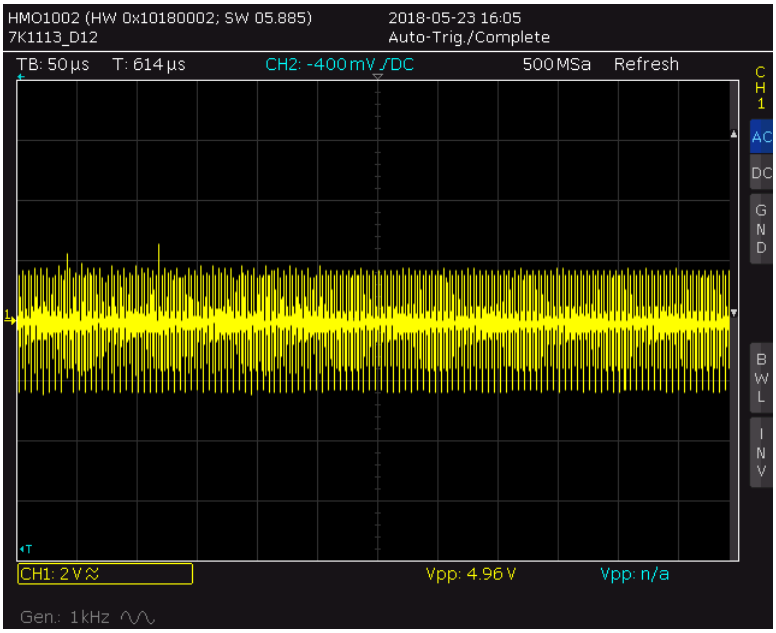

Figure 45: Ripples in the 6.3 V supply after use of the MC34063 circuit.

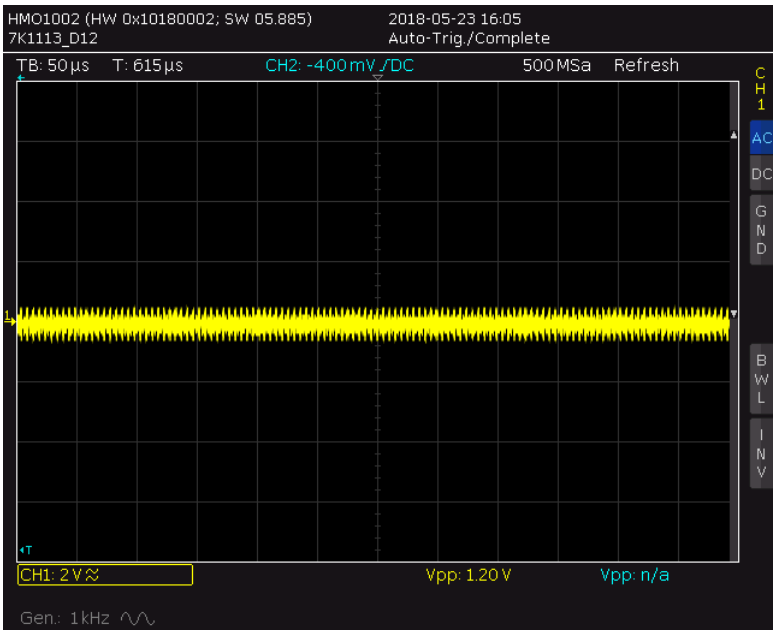

Figure 46: Ripples in the ground plane after use of the MC34063 circuit.

5.5 Sound quality

Subjectively, the finalized amplifier sounds good, though it may not be considered "hifi". Little to no distortion can be heard and the frequency response is natural. Even though the ripples in the output seem large in oscillograms most of it is either very low in volume or high in frequency, above both the audible frequency range and what a typical speaker is capable of reproducing. The small amount of background noise is mostly drowned out when playing music at listenable volumes. The MC34063 introduced some strange noises noticeable at low volumes. This was solved by connecting an extra capacitor and a large

resistor between the MC34063 circuit and ground, as suggested by Dr. Uwe Zimmermann [4]. The amplifier on PCB had overall less noise than the breadboards, but sound quality was the same.

5.6 Efficiency

The input power was found to be 6.0 W and the output power was 4.8 W, giving an efficiency of 80 %.

6 Discussion

6.1 Comparison between simulation and construction

Simulations of the amplifier in LTspice are overall much cleaner with little to no ripples. The large ripples seen in the output signal of the constructed amplifier originate mostly from the breadboards and voltage regulators. Most of these ripples are not present in the simulations since ideal voltage sources are used and no parasitic capacitances etc. are present. The ideal voltage sources are ripple-free and not affected by the rest of the circuit, something that cannot be achieved in an actual construction. This shows that voltage supply and regulation is very important when building a class D amplifier, as the efficiency and linearity of the output signal both were much higher in the simulations. The PWM is much cleaner in the simulations as well, due to the same reasons as above. The ripples in the PWM become ripples in the output signal.

It can be seen in fig. 22 that within the first 3 ms the output is not stable, perhaps due to the large capacitor at the output taking some time to charge. This is essentially a DC component but due to its short duration it would not be harmful to the speaker if present in the actual construction. The output signal is phase-shifted which is expected, but it is not a problem for music playback.

Fig. 26 shows that the constructed triangle wave generator does not produce much more ripples than the simulated one (fig. 19), credit to fast op-amps and consistent voltage regulation. However there is quite a large difference in frequency; 270 kHz in simulations and 202 kHz on breadboard. This is largely due to the simulations relying on ideal components. Simulations are good for knowing what components affect which parameters to what extent, but some trial and error is needed to get the desired frequency in the actual constructed circuit.

6.2 Problems and potential improvements

The sound quality is more than acceptable taking into account that this is a very simple design and that it was not the main goal of the project. To further reduce noise and distortion a feedback loop could be implemented, but it would require an error amplifier before the comparator input. A full-bridge configuration would also improve sound quality. Using the full-bridge amplifier design would also have eliminated the issue of the

DC component in the output since the amplifier would then "idle" at 0 V. Full-bridge designs can also achieve higher amplification with the same voltage supply since they use four MOSFETs instead of two.

A more elegant solution to the popping problem when turning the amplifier on and off would be implementing a timer IC, to make sure that the power stage is the last thing to turn on. The standby switch was chosen instead since it was easier and faster to implement.

One major problem with the triangle wave generator was that the formulae (1) and (2) did not correspond to the simulation or the constructed circuit (simulation and construction were however quite similar). This is probably because the formulae were derived with ideal op-amps in mind. This caused some confusion and made the initial component selection harder.

The triangle wave generator worked well both in simulation and in practice, even though the two differed in frequency and amplitude. The op-amps need to be fast enough for the desired triangle wave frequency and faster components than the TLE2081CP might be capable of producing a faster triangle wave. Slower op-amps like the LM741 are also able to generate a triangle wave, albeit with significantly lower frequency.

The BJT-based comparator works very well and creates the PWM needed, as long as the input signal is bounded by the triangle wave. A suitable IC would also work while taking up less space on the board. The output signal amplitude and therefore the volume will depend on how large the input is compared to the triangle wave. Therefore the maximum volume is limited to when the input amplitude is close to 100 % of the triangle wave amplitude.

Ideally a delay IC would have been used for the dead time generator, as this would have reduced the total number of ICs, but a suitable delay IC that was also available for purchase was not found. The NOT gates were used instead since they were readily available. This increased the physical size occupied on the breadboard and PCB but did not seem have a large effect on sound quality. The ICs chosen were of the types HCT (High-speed CMOS with transistor–transistor logic (TTL)) and AHCT (Advanced high-speed CMOS with TTL) to ensure fast switching from high to low in the logic gates and to minimize distortion in the PWM and output signal.

Because most parts of the circuit were sensitive to ripples in the supply voltage, voltage regulators were required, preferably implemented with capacitors to lessen ripples. This ensured a high quality triangle wave and less noise making it to the output, among other things. The voltage regulators and their implementations must be chosen carefully. They must operate at a high efficiency, otherwise the efficiency traits of the class D amplifier design will be forfeit. Many of the heat sinks to the positive supply rails got rather hot, not too hot to touch but above ambient temperature. This is due to the linear voltage regulators dissipating heat when the input voltage is much higher than the output voltage. Losing large amounts of power in the regulators negates the sole purpose of class D. However, given more time, this could have been improved.

If switching regulators are used they must have an oscillation frequency above the audible frequency range or the low-pass filter cutoff, as this frequency may be superimposed on the output at some point in the signal chain. If noise is present, decoupling capacitors

between voltage rails and ground may be needed, especially in close proximity to the ICs, as this will reduce noise further.

When the MC34063 circuit was implemented, it could be seen that even though more audible noise reached the speaker, the ripples in the 6.3 V supply (fig. 45) and ground (fig. 46) became smaller and less present. The audible noise is probably due to the switching inverter itself, however the previously used main negative voltage supply may itself have introduced ripples in the system. When the switching voltage inverter was used instead, those ripples vanished.

Even though the voltage regulators heat up, the MOSFETs output little to no heat and seem to be working as they should. Ideally a high side MOSFET with lower R_{DSon} than the IRF9540 would be used, this would yield a higher efficiency and less produced heat.

The efficiency of 80 % shows that our design is capable of being more efficient than the theoretical limit of class B (78.5 %). Considering that the emphasis of this project was on the principle of class D and not efficiency, it is rather good. Total harmonic distortion (THD) would need to be measured together with the efficiency, which has not been done. With the 6 Ω speaker there is however little audible distortion, even at the same high input levels.

The breadboards used were not ideal to connect such a large and sensitive circuit as this amplifier. When the amplifier did not work as intended it was often caused by loose connections within the breadboard, which made troubleshooting frustrating. Breadboard rails also have parasitic capacitances between them which surely created audible noise. Cable lengths were kept to a minimum but a number of longer cables were required between the breadboards. These cables acted as antennas, introducing even more noise into the circuit. The PCB design avoided many of these noise sources, which became evident when listening at low volumes.

The laptop power supply used with the PCB design did not seem to introduce any additional noise to the circuit, even though it utilized switching. The circuit on PCB also produced less audible noise than the breadboard design, probably due to better connections and shorter wires on the PCB.

7 Conclusion

The goal of this project was to build a working class D amplifier and this was accomplished with good sound quality and relatively low noise. A rather high efficiency (80 %) was achieved. To reach the extremely high efficiency class D amplifiers are capable of, one must be cautious of how the required voltages are achieved and how they are regulated.

The constructed amplifier did not perform to the level of the simulations, but simulations were very useful when troubleshooting and when the final design needed to be altered.

Dedicated ICs for the comparator, dead time generator etc. would have required less real estate on the boards than the discrete component approach. However, all our designs seemed to be working well, with the advantage that most of the parts used are easy to find and very cheap.

Many aspects could have been improved with more complicated designs such as a full-bridge and/or by adding feedback. In contrast, these things would have increased the complexity of this project and the half-bridge amplifier constructed had many qualities while also being manageable during our short time frame.

References

[1] A. S. Sedra and K. C. Smith. *Microelectronic Circuits*. Oxford University Press, 2016.

[2] *Linear And Switching Amplifier Overview*. Tripath Technology Inc., 1997. URL: `http://www.profusionplc.com/images/application%20notes/an3.pdf`, retrieved 2018-05-15.

[3] A. I. Colli-Menchi, M. A. Rojas-Gonzalez and E. Sánchez-Sinencio. *Design Techniques for Integrated CMOS Class-D Audio Amplifiers*. World Scientific, 2016.

[4] Uwe Zimmermann, senior lecturer at Department of Engineering Sciences, Solid State Electronics, Uppsala University.

Appendix A List of components and values

Identifier	Type	Model/Value
M1	PMOS	IRF9540N
M2	NMOS	IRF3710
Q12	NPN	BD241C
Q13	PNP	BD242C
Q1, Q2, Q7-Q11	NPN	2N3904
Q3-Q6	PNP	2N3906
-	Voltage regulator	LM338T
-	Voltage regulator	LM7905
-	Voltage regulator	MC34063
U1, U2	Op-amp	TLE2081CP
-	Inverter	SN74HCT14N
-	NAND	SN74AHCT00N
C1	Capacitor (Ceramic)	47 pF
C2, C3	Capacitor (Electrolytic)	1 μF
C4	Capacitor (Film)	100 nF
C5	Capacitor (Electrolytic)	220 μF
L1	Inductor	50 μH
L2, L3	Inductor	22 μH
R1	Resistor	10 kΩ
R2	Resistor	220 kΩ
R3	Resistor	100 kΩ
R4	Resistor	2.7 kΩ
R5	Resistor	120 Ω
R6	Resistor	390 Ω
R7	Resistor	120 Ω

Appendix B KiCad schematics

Note that the component naming here is not consistent with previous figures.