SkyBridge-3D-CMOS 2.0: IC Technology for Stacked-Transistor 3D ICs beyond FinFETs

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***Abstract*—For sub-5nm technology nodes, gate-all-around (GAA) FETs are positioned to replace FinFETs to enable the continued miniaturization of ICs in the future. In this paper, we introduce SkyBridge-3D-CMOS 2.0, a 3D-IC technology featuring integration of stacked vertical GAAFETs and 3D interconnects. It aims to provide an integrated solution to critical technology aspects, especially when scaling to sub-5nm nodes. We address important aspects such as 3D fabric components, CAD tool flow, compact model for the GAAFETs and a scalable manufacturing process. The fabric features junctionless accumulation-mode field effect transistors (JAMFETs) including various configurations with multiple threshold voltages and multiple nanowires per transistor, to meet performance and stand-by power constraints of modern SoCs. Furthermore, we develop BSIM-CMG-based compact models for these device configurations to enable technology assessment using SPICE simulations. To enable scalable manufacturing, we create virtual process decks incorporating etch and deposition models using Process Explorer, an industry standard process emulation tool. Technology assessment using ring oscillators shows that SkyBridge-3D-CMOS 2.0 at the chosen design point, using 16nm gate length and 10-nm nanowires, achieves ∼18% performance and 31% energy efficiency improvement versus 7nm FinFET CMOS. Area analysis of standard cells shows up to 6x benefit versus aggressively scaled 2D-5T cells.**

***Index Terms*—3D-IC, CMOS scaling, Stacked GAAFETs, virtual fabrication**

I. Introduction

Continuous downscaling of transistors is the key driver of miniaturization of integrated circuits (ICs). This scaling is achieved by shrinking the bottom-most metal layer pitch and contacted gate pitch (CGP) of transistors. Since CGP scaling involves reducing gate length, short channel effects have become dominant below 20nm technology node. In order to better manage the short channel effects, transistors have evolved from planar FETs to FinFETs; FinFETs have better control over the channel. However, below 5nm technology node, even FinFETs have several shortcomings. Gate length and contact thickness compete for cell width, while intra-cell routing congestion limits cell height [1]. RC parasitics and variability resulting from thin fins limit circuit performance [2] [3].

Gate-all-around (GAA) FETs with vertical and lateral nanowire channels are set to replace FinFETs as the primary devices of choice in the near future. GAAFETs allow for relaxed channel dimensions while providing good channel control – this is because the channel in GAAFET is wrapped by the gate from all sides. In lateral nanowire FETs, nanowires/nanosheets are stacked on top of each other thus improving the surface area of the channel without the need for multiple fins. However, CGP scaling still depends on gate length scaling and hence it does not solve scaling issues altogether. The best solution is to decouple CGP and gate length by having the channel perpendicular to the wafer surface - essentially by using vertical nanowire FETs (VNFETs). In addition to CGP scaling advantages and improved short channel control, VNFETs are also more naturally suitable for fine-grained 3D stacking; 3D is critical for keeping up with aggressive scaling and interconnect needs in future ICs. However, simply replacing the FinFETs with GAAFETs while keeping other aspects of IC design such as local and global interconnect schemes, contact access schemes, manufacturing pathway, thermal management etc. the same, is likely only a temporary solution [4]. Bearing this in mind, in recent years, novel IC fabrics incorporating stacked vertical gate-all-around (V-GAA) junctionless transistors, which offer a paradigm shift in technology scaling as well as design, have been proposed [5] [6]. These approaches architect all aspects of IC design from devices to circuit style, connectivity, thermal management and manufacturing pathway. In [5], the authors proposed a vertical IC fabric based on dynamic-style circuits. However, it leads to circuit designs that are not compatible with static CMOS and is a departure from what the industry is currently using. In [6], a vertically composed 3D-CMOS IC fabric is proposed. However, it uses devices based on single nanowire junctionless FETs which lead to lower drive currents, resulting in performance degradation in especially smaller circuit designs where interconnect benefits due to 3D are less pronounced. Besides, both of these works were benchmarked against a 16nm node and do not yet include technology optimizations for scaling to sub-5nm nodes.

In this paper, we present SkyBridge-3D-CMOS 2.0 (SkyBridge 2.0), a fine-grained 3D-IC fabric for future stacked-transistor ICs. Partly inspired by works in [5] [6], SkyBridge 2.0 addresses several key challenges when scaling to sub-5nm node and beyond. It is envisioned to provide an integrated solution to critical technology aspects such as characterization of 3D fabric components, scalable CAD tool flow, a compact model for the GAAFETs, as well as a scalable manufacturing flow. It incorporates vertical junctionless accumulation mode

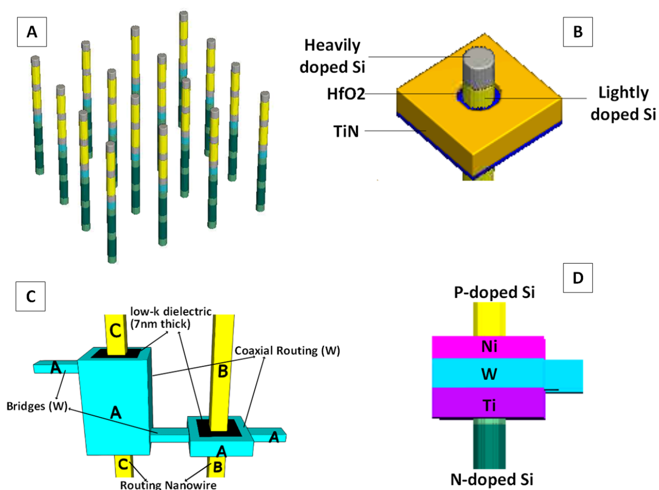

Fig. 1. SkyBridge 2.0 Fabric Components

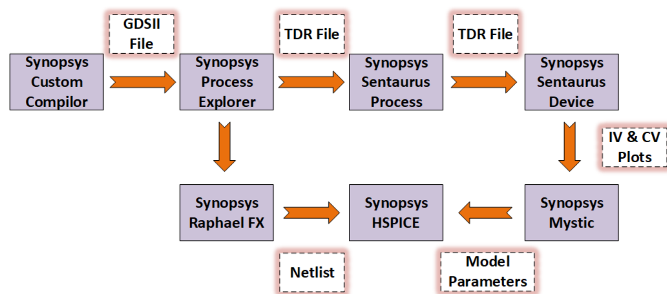

Fig. 2. 3D Process Emulation and Evaluation Framework

TABLE I
TECHNOLOGY DESIGN RULES FOR SKYBRIDGE 2.0

Parameters	Dimensions
Gate Length (nm)	16
Spacer Thickness (nm)	5nm
NW Diameter (nm)	10
NW Pitch (nm)	58
Number of NWs	1, 2, 4
Nominal Vdd (V)	0.6
Channel Orientation	[001]
NW Height (nm)	200

(JAM) FETs as the active devices which have comparable performance to FinFETs while having better short channel characteristics. Using TCAD simulations, we characterized various configurations of JAMFETs including multiple threshold voltages and multiple nanowires per transistor, to meet both performance and stand-by power constraints in modern SoC designs. Our industrial CAD tool flow co-optimizes key elements of both process and design, critical for development of advanced nodes. To accurately capture the JAMFET device behavior, we developed a compact model based on industry-standard BSIM-CMG [7] using the Synopsys Mystic TCAD-to-SPICE tool [8]. Using the state-of-the-art process emulation tool Sentaurus Process Explorer (SPX) [8], we developed process flows using industry-proven unit processes to obtain fab-realistic 3D models of fabric components and standard cells in SkyBridge 2.0. Together with the extracted compact model and 3D layout interconnect, including RC parasitics extracted by Synopsys Raphael-FX [8], we created a netlist of a five-stage ring oscillator for bottom-up technology assessment following widely-used methodologies for new IC fabric evaluations. The results indicate that SkyBridge 2.0, at the chosen design point of 10-nm nanowires, achieves $\sim 18\%$ performance and 31% energy efficiency improvement versus aggressively scaled 7nm FinFET CMOS. Area analysis of standard cells shows up to 6x benefit versus aggressively scaled 2D-5T cells.

The rest of the paper is organized as follows. Section II introduces SkyBridge 2.0 and its key fabric features. Section III outlines the CAD framework for bottom-up evaluation of the fabric. Section IV delves into the scalable manufacturing pathway. Section V shows technology benchmarking and results. Section VI concludes the paper.

II. SKYBRIDGE 2.0 FABRIC COMPONENTS

The SkyBridge 2.0 fabric is designed to realize fine-grained 3D integration by co-envisioning its components, assembly and fabrication process and providing an integrated solution for all core technology challenges. Its assembly is based on a uniform vertical pre-doped nanowire template (see Fig. 1A) which is functionalized by layer-by-layer selective material deposition to create the required fabric components. The functionality of these components depend on their material types and geometries. The detailed manufacturing pathway using process emulation is covered in Section IV.

All IC components of SkyBridge 2.0 are vertically composed by selective material deposition around nanowires. Components are placed and connected on these nanowires either in series (on one nanowire) or in parallel (across multiple nanowires connected in parallel) to build CMOS circuits. Uniform vertical gate-all-around (V-GAA) junctionless accumulation mode field effect transistor (JAMFET) [9] are the active devices in SkyBridge 2.0; an n-type JAMFET transistor is shown in Fig. 1B. In contrast to junctionless FETs (JLFETs), JAMFETs have additional source/drain implantation to increase the source/drain doping ($\sim 10^{20} cm^{-3}$) for reducing the series resistance on a nanowire. Furthermore, the channel is somewhat lightly doped ($\sim 10^{18} cm^{-3}$) and thus are expected to have lower random dopant fluctuations and threshold voltage variability as compared to JLFETs. Thus JAMFETs have significantly higher drain current as compared to JLFETs. Degraded short channel performance and band-to-band tunneling (BTBT) induced parasitic BJT action are the major challenges for JAMFETs. However, short channel effects performance is still better than FinFETs and device-level optimizations can reduce the BTBT effect as shown in [10]. Compared to JLFETs employed in [5] [6], JAMFETs have comparable performance to FinFETs at the cost of slight manufacturing complexity. This along with the true fine-grained 3D integration, with dense connections and design, yields significantly higher performance at the fabric-level vs

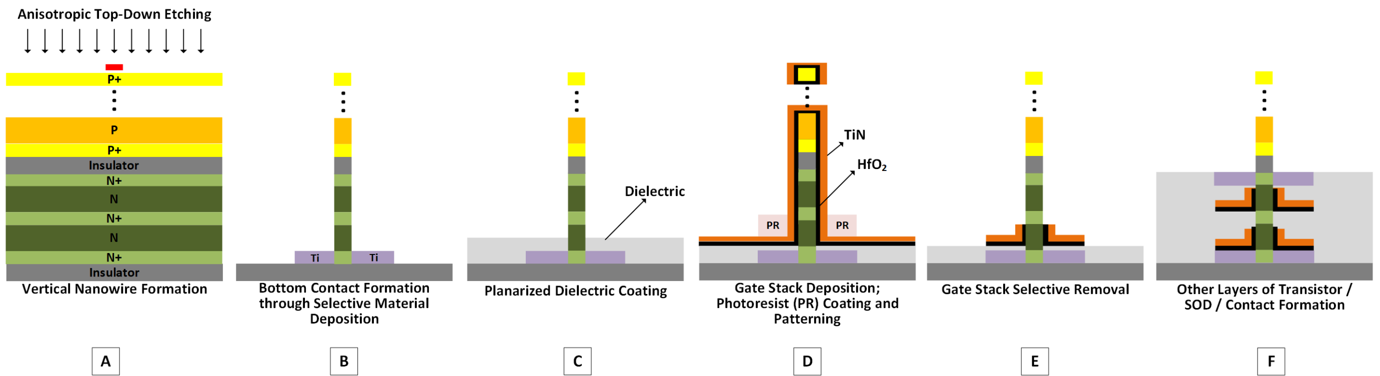

Fig. 3. SkyBridge 2.0 process flow for stacked n-type transistor fabrication.

state-of-the art FinFETs.

The fabric greatly improves connectivity thanks to its 3D interconnect structures, as well as higher intrinsic circuit density. In contrast to traditional CMOS and parallel/sequential integration where interconnections are mostly made through horizontal metal wires, in many metal layers above the transistor layers, the fabric features a true 3D interconnection framework with specifically architected 3D interconnection structures as shown in Fig. 1C,D: I) Wrap-around contacts ensure good ohmic contact with the nanowires which results in smaller S/D series resistance for JAMFETs; II) Bridges provide horizontal connections between adjacent nanowires; III) Coaxial Routing structures carry signals vertically along nanowires; IV) nanowires can be used for vertical routing since they are heavily-doped and silicided and thus have good conductivity; V) Interlayer-Connection (ILC) provides good ohmic contact between p- and n-doped regions of a nanowire, which is designed with materials chosen based on the required work function (detailed structure and chosen materials are shown and explained in Fig. 1). This framework provides very high connectivity due to its routing flexibility in all three dimensions.

III. SkyBridge 2.0 CAD Tool Flow

In this section, an industrial CAD tool flow is outlined. Synopsys Custom Compiler [9] is used to draw 2D layouts required for defining the masks for the lithography steps during the process emulation. Sentaurus Process Explorer (SPX) [8], a state-of-the-art process emulation tool, is used to build a full set of virtual process decks. The 3D models are then sent to Synopsys TCAD Sentaurus Process [8] for process simulations such as doping, meshing and contact generation. After process simulations, the models are sent to Synopsys TCAD Sentaurus Device [8] to obtain the electrical properties of the fabric components. The IV and CV characteristics obtained from the device simulations are sent to the Mystic tool for development of a BSIM-CMG based compact model. The same 3D structures are sent to Synopsys Raphael FX [8] for extracting 3D layout-specific RC parasitic netlist. The compact model and parasitic RC netlist are combined to generate standard cell netlists which are used in HSPICE simulations. Fig. 2 shows the block diagram of the framework.

IV. SkyBridge 2.0 Manufacturing Pathway

Wafer-scale manufacturing pathway is integral for any new IC technology. Foundries use virtual fabrication techniques by emulation of hundreds of processes typically involved in large-scale manufacturing. Virtual process flows are crucial for process integration engineers to gain valuable insights before proceeding to the wafer testing phase. Following a similar mindset, we present a wafer-scale manufacturing pathway for SkyBridge 2.0 derived by physics-driven virtual process integration. Using a state-of-the-art process emulation tool, Synopsys Sentaurus Process Explorer, we developed process flows using industry-proven unit processes to obtain fab-realistic 3D models of components and cells. The flow recipes and parameters were also calibrated by some of our previous cleanroom experience and also from experimental demonstrations from other research groups, as well as tolerances accepted in industrial flows.

A. Wafer Preparation

In SkyBridge 2.0, an IC is processed as a single wafer in contrast to the parallel/monolithic 3D integration, where circuits are manufactured in a layer-by-layer manner. The wafer preparation step is the first step in the pathway. This step generates the starting wafer for the SkyBridge 2.0 assembly. The starting wafer is a customized dual-doped silicon (Si) wafer. As shown in Fig. 3A, at the bottom of the wafer is an insulator on bulk Si which can be connected to the package heat sink through backside metallization; on the top are dual-doped n-type and p-type Si layers separated by an insulating layer. Within each n-type and p-type Si layer, there are epitaxially-grown layers of heavily and lightly doped regions. Stacked layers of Si epi with a wide doping range for a certain layer and a sharp doping concentration steepness between doped regions have been experimentally demonstrated [11]. Furthermore, since doping is done once at the wafer-level, processing of these layers doesn't add a lot of manufacturing complexity. Using epitaxial deposition models in SPX, the

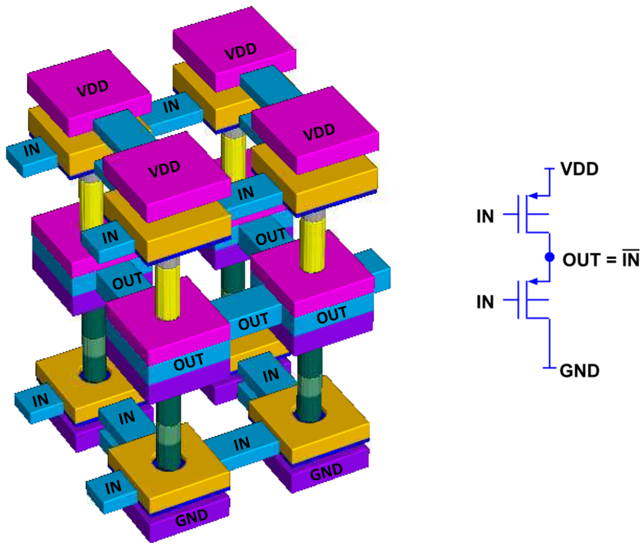

Fig. 4. 3D Model of 4-nanowire inverter cell generated by Process Explorer (isolation dielectric not shown.)

aforementioned steps were followed to generate the 3D model of the starting wafer.

B. Nanowire Template Formation

In SkyBridge 2.0, ideally, all the nanowires have similar aspect ratio, and maintain uniform distances between each other. High aspect ratio uniform vertical nanowires with smooth surfaces can be achieved through patterning with processes such as the Bosch process, Inductively Coupled Plasma (ICP) etching. ICP etch is shown to have elevated etch rates, high directionality aiding in creating anisotropic profiles required for smooth vertical sidewalls and high aspect ratio. Furthermore, several research groups have demonstrated high aspect ratio nanowires that are in line with SkyBridge 2.0's requirements. These groups have demonstrated nanowires of various widths ranging from 30 nm to 5 nm, the highest aspect ratio being 50:1. The process steps in SPX for template formation was as follows: 1) A hard mask was patterned through lithography to define the nanowire template; followed by 2) anisotropic etching of dual-doped Si wafer resulting in the formation of the template.

C. Contact Formation

Nanowire patterning is followed by a contact formation step. SkyBridge 2.0 features wrap-around contacts for achieving low contact resistance with the nanowire. Unified deposition models in SPX support several deposition processes to achieve this. The steps for forming the contacts in SPX is as follows: 1) anisotropic deposition model was used to deposit Titanium (Ti); 2) overcoating of photoresist was used to define the contact region; 3) regions surrounding the nanowires were exposed using lithography. The region of exposure is determined by the minimum material dimension requirements as outlined in SkyBridge 2.0 design rules [10]; 4) excessive Ti was then etched away to form the contact (see Fig. 3C).

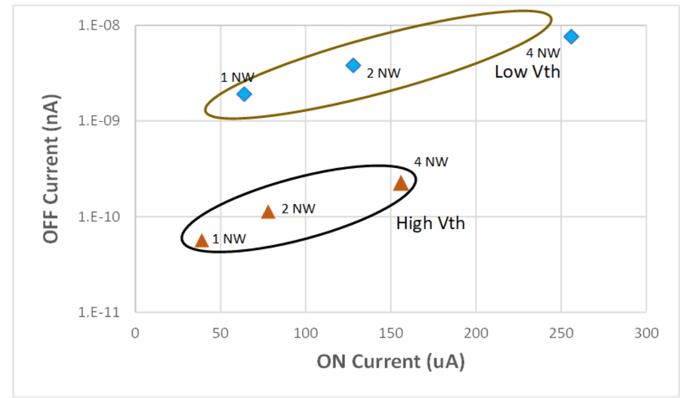

Fig. 5. Intrinsic leakage current versus ON current for six device configurations.

D. Planarization

Since SkyBridge 2.0's manufacturing pathway is primarily based on material deposition, each layer needs to be planarized between depositions. However, this might result in etch-layout dependence effects. Such effects result in non-planar surfaces which can cause lithographic focus imbalance and alignment errors. Furthermore, formation of sloping layers reproducing the shape of an underlying insulator results in high parasitic capacitance. Through etch and deposition models such effects were modeled in SPX. In order to overcome such effects, a multi-pronged planarization scheme outlined in [11] is used: 1) a layer of insulating Nitride was isotropically deposited so as to uniformly cover the nanowires; 2) a litho-resist such as Hydrogen Silsesquioxane (HSQ) was coated completely covering the nanowires; 3) CMP was used to remove excess HSQ, thus exposing the tip of the nanowire; 4) the resist etch-back was isotropically stopping at a targeted resist thickness in the areas in-between pillars; 5) an isotropic etch was performed to etch-back the Nitride layer in areas not covered by the resist and set its final thickness; 6) resist is stripped off.

E. Gate Stack Deposition

Selective gate material deposition is a key process step in S3DC assembly. High-k gate dielectric and gate electrode are deposited in selective places in the nanowire template to form GAA devices. The channel length is determined by the material deposition step which can be controlled with very high precision. SPX supports atomic layer deposition models which can be used to achieve a very uniform thin coating of gate electrode and gate dielectric. The process steps for gate stack deposition is as follows: anisotropic deposition of Titanium Nitride (TiN); B) isotropic deposition of high-K dielectric (HfO_2); C) lithography step to define gate electrodes; D) anisotropic etching of TiN resulting in rounded corners. The subsequent layers were deposited in a similar way with a planarization step in between each layer. Fig. 4 shows the 3D model of 4-nanowire inverter cell generated by SPX using the outlined manufacturing pathway.

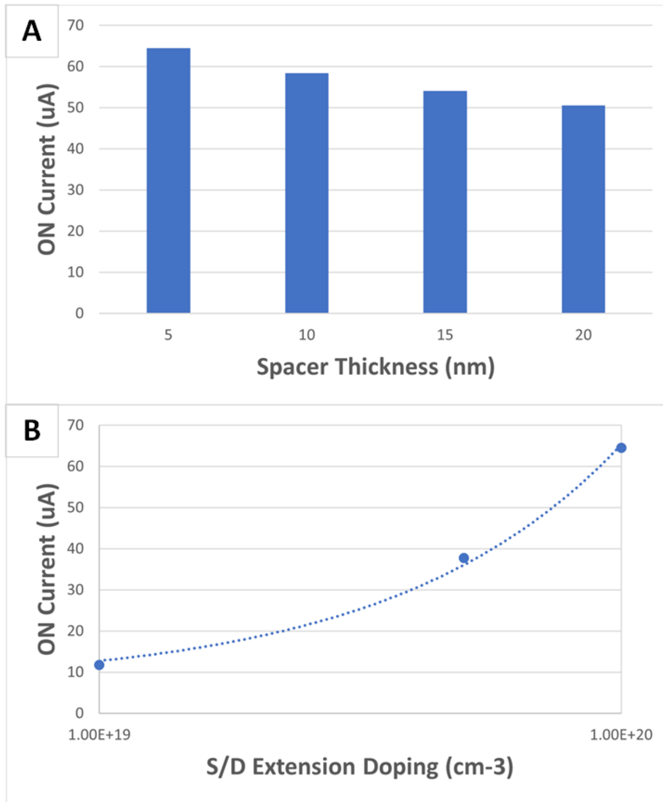

Fig. 6. (A) ON current versus spacer thickness for low Vth, four nanowire device configuration; (B) ON current versus S/D extension doping for low Vth, four nanowire device configuration.

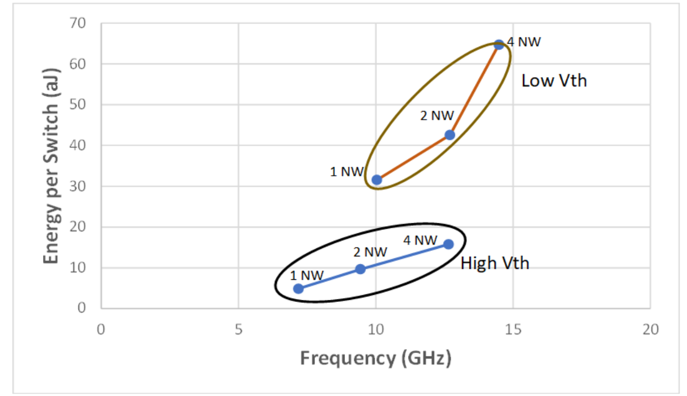

Fig. 7. Energy per switch versus the operational frequency of a 5 stage ring oscillator for six device configurations.

V. Technology Benchmarking and Evaluation

A. Characterization of SkyBridge 2.0 Components

All the fabric components of SkyBridge 2.0 were characterized including ILC, ohmic contacts, coaxial routing structures and JAMFETs using 3D Sentaurus TCAD Process and Device simulators. The technology design rules for SkyBridge 2.0 are outlined in Table I. Process simulator created the device structure emulating actual process flow; process parameters include such as ion implantation dosage, anneal duration and temperature, deposition parameters etc. The resultant device structures were then used in Device simulations to extract device characteristics accounting for nanoscale confinement, surface and coulomb scattering and mobility degradation effects. Since the use of multiple threshold voltages (Vth) for devices has become the norm to cater to high-performance and low power designs, two Vth flavors are supported in SkyBridge 2.0. High Vth and low Vth devices were achieved with work function engineering at the nominal voltage of 0.6v. The leakage for high and low Vth devices were 10pA and 2nA, respectively. In addition to Vth flavors, SkyBridge 2.0 also supports combining multiple nanowires to boost the ON current of the devices. JAMFETs based on 1, 2 and 4 nanowires are supported. Figure 6 shows the intrinsic leakage and ON current for various device configurations. As evident from the figure, the low Vth transistor based on four nanowires achieves the best ON current and worst leakage current while the high Vth transistor based on one nanowire achieves the lowest leakage current. The performance of p-type devices slightly lagged behind of n-type JAMFETs because of mobility degradation.

A device performance study for various S/D spacer and doping configurations were also carried out. The spacer thickness optimization is an RC-optimization problem. The smaller the thickness is, the closer are the S/D and gate electrodes, which results in higher parasitic capacitance. Higher capacitance impacts performance and also device power consumption. However, the smaller spacer thickness also results in smaller series S/D resistance thus boosting ON current. Fig. 6A shows the ON current for various S/D spacer thicknesses ranging from 5nm to 20nm. As the spacer thickness increases, the ON current decreases due to increase in series resistance of the S/D extension region. Fig. 6B shows the ON current for various S/D extension doping. As the S/D extension doping increases, the ON current of the device increases due to availability of additional charge carriers.

B. Circuit-level Performance Analysis

Technology benchmarking is typically done using ring oscillators (ROs). They are useful for early technology assessment and may also be used for device optimization. A five-stage RO consisting of inverters is used to assess SkyBridge 2.0. Each inverter stage drives three other inverter gates resulting in a fan-out of three (FO3) load. To account for BOEL load, we used 50 nanowire pitch long wires between each stage. In order to assess the trade-offs between performance and power, performance and energy analysis is performed for the various device configurations, i.e., high and low Vth and multiple nanowires per device. The RO configuration with inverters consisting of low Vth 4-nanowire JAMFETs performs the best with frequency of 15 GHz due to high drive current. To compare the energy consumption, Fig. 7 shows the energy per switch versus frequency for various configurations. The high Vth version with single nanowire has the lowest energy consumption due to lower leakage and area. As regards to best

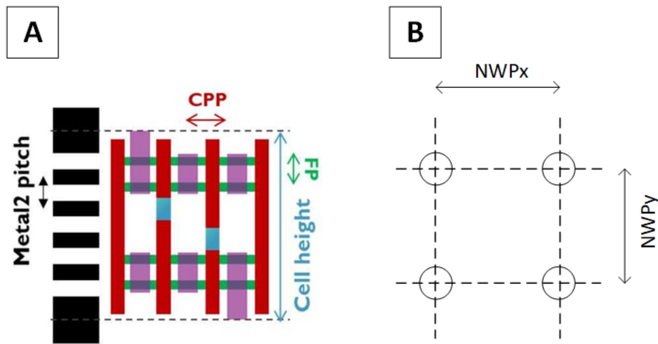

Fig. 8. (A) Standard cell dimensions for 2D-CMOS; (B) Cell dimensions for SkyBridge 2.0

TABLE II
STANDARD CELL AREA ANALYSIS

Std. Cell	Usage (%)	2D-5T	S2.0-1NW	S2.0-2NW	S2.0-4NW
INV	3.5	3	1	2	3
BF	3	4	2	3	4
NAND2	3	4	2	3	4
NOR2	3	4	2	3	4
OAI22	3	6	2	3	4
AOI22	4	6	2	3	4
Sum	19.5	88.5	35.5	55	74.5
Ave. Width	-	4.54	1.82	2.82	3.82
Cell Height	-	5	2	2	2
Ave. Area	-	22.69	3.64	5.64	7.64
Benefits vs 2D	-	1	6.23	4.02	2.97

configuration for performance per power, High Vth version with four nanowires might be the best option as it provides the best of both worlds.

In order to estimate the benefits of SkyBridge 2.0, ring oscillators with high performance (SLVT) inverters from ASU FinFET 7nm PDK [12] were employed. The same five stage RO with each stage driving three inverters (FO3) is considered. To account for BOEL wiring load, 50 CGP long wires are considered. The ROs achieved achieved a highest frequency of 12.6 GhZ and 85.6 aJ of energy per switch. This indicates close to 18% performance improvement and around 31% energy efficiency for the JAMFETs over 7nm FinFETs. This is attributed to the fact that JAMFETs have comparable performance versus FinFETs while requiring lower energy for switching because of small parasitic capacitance and better SCE performance.

C. Area Analysis

In order to estimate the area benefits of SkyBridge 2.0, we use a set of standard cells to calculate the weighted average cell width of aggressively scaled 2D-CMOS to compare with SkyBridge 2.0 standard cells with various nanowire configurations. For 2D-CMOS, the 5-track cell height (4 signal tracks plus power rail) with single diffusion break is seen as the limit of traditional scaling. Area of a standard cell is the product of cell height (Y-axis) and width (X-axis). The width indicates the minimum contacted gate pitch required for implementing a particular standard cell, i.e., NAND2 has 2 active transistors plus 2 dummy transistors at the cell boundary so the cell is 4 contacted gate pitches (CPP) wide. For SkyBridge 2.0, area of standard cell is calculated as a product of nanowire pitches (NWP) required to implement the cell in NWPx and NWPy axes as shown in Fig. 8B. Additionally, for SkyBridge 2.0, we calculated NWPs for various device configurations, i.e., 1, 2 and 4 nanowires. The usage indicates the percentage utilization of standard cells in a typical design. The usage and the width of cells are used to calculate the weighted average area of all the cells to get area benefits of SkyBridge 2.0 versus 2D-CMOS. Table II shows the results of this area comparison. SkyBridge 2.0 shows up to 6x area benefits versus aggressively scaled 2D-5T.

VI. CONCLUSION

In this paper, we proposed SkyBridge-3D-CMOS 2.0, a fine-grained 3D fabric technology for future stacked ICs. SkyBridge 2.0 envisions all key aspects of IC technology from device, interconnect, to manufacturing. A wafer-scale manufacturing process using virtual process emulation is also proposed. All the fabric components are fully validated using Process and Device simulations. Device performance studies are presented in order to show trade-offs between power and performance. Finally, RO analysis shows that SkyBridge 2.0 achieves close to 18% performance improvement, 31% energy efficiency versus the 7nm FinFET CMOS. Area analysis of standard cells of SkyBridge 2.0 shows up to 6x benefits versus aggressively scaled 2D-5T cells.

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