
SmartFusion2 System-on-Chip FPGAs

Introduction

Microsemi's SmartFusion[®]2 system-on-chip (SoC) FPGAs integrate fourth generation flash-based FPGA fabric, an ARM[®] Cortex[™]-M3 processor, and high performance communications interfaces on a single chip. The SmartFusion2 FPGA is the industry's lowest power, the most secure, and has the highest reliability of any programmable logic solution. SmartFusion2 offers up to 3.6X the gate density and up to 2X the performance of previous flash-based FPGA families and includes multiple memory blocks and multiply accumulate blocks for DSP processing. The 166 MHz ARM Cortex-M3 processor is enhanced with ETM and 8 Kbyte instruction cache, and additional peripherals including CAN, Gigabit Ethernet, and high speed USB. High speed serial interfaces enable PCIe[®], XAUI/XGXS plus native SERDES communication while DDR2/DDR3 memory controllers provide high speed memory interfaces.

SmartFusion2 Device Status

Family Devices	Status
M2S005	Advance
M2S010T/M2S010	Advance
M2S025T/M2S025	Advance
M2S050T	Preliminary
M2S050	Advance
M2S090T/M2S090	Advance
M2S0100T/M2S0100	Advance
M2S150T/M2S150	Advance

SmartFusion2 Product Brief and Pin Descriptions

The product brief and pin descriptions are published separately:

SmartFusion2 Product Brief

SmartFusion2 Pin Descriptions

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SmartFusion2 DC and Switching Characteristics

General Specifications

Operating Conditions

Stresses beyond those listed in [Table 1](#) may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute maximum ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the recommended operating conditions specified in [Table 2-2](#) on [page 2-2](#) is not implied.

Table 1 • Absolute Maximum Ratings

Symbol	Parameter	Limits		Units	Notes
		Min.	Max.		
VDD	DC core supply voltage. Must always power this pin.	-0.3	1.32	V	
VDD_2V5	DC Bias supply voltage. Must always power this pin.	-0.3	2.75	V	
VPP	Power supply for charge pumps (for normal operation and programming). Must always power this pin.	-0.3	3.63	V	
MDDR_PLL_VDDA	Analog power pad for MDDR PLL	-0.3	3.63	V	
FDDR_PLL_VDDA	Analog power pad for FDDR PLL	-0.3	3.63	V	
PLL0_PLL1_MDDR_VDDA	Analog power pad for MDDR PLL	-0.3	3.63	V	
CCC_XX[01]_PLL_VDDA	Analog power pad for PLL0-5	-0.3	3.63	V	
SERDES_[01]_PLL_VDDA	High supply voltage for PLL SERDES[01]	-0.3	3.63	V	
SERDES_[01]_L[0123]_VDDAPLL	Analog power for SERDES[01] PLL Lane0 to Lane3. This is a +2.5 V SERDES internal PLL supply.	-0.3	2.75	V	
SERDES_[01]_L[0123]_VDDAIO	Tx/Rx analog I/O voltage. Low voltage power for the lanes of SERDESIF0. This is a +1.2 V SERDES PMA supply.	-0.3	1.32	V	
SERDES_[01]_VDD	PCIe/PCS power supply	-0.3	1.32	V	
VDDIx	DC FPGA I/O buffer supply voltage for MSIO I/O bank	-0.3	3.63	V	
	DC FPGA I/O buffer supply voltage for MSIOD/DDRIO I/O banks	-0.3	2.75	V	
VI	I/O Input voltage for MSIO I/O bank	-0.3	3.63	V	
	I/O Input voltage for MSIOD/DDRIO I/O bank	-0.3	2.75	V	
VPPNVM	Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to VPP.	-0.3	3.63	V	
T _{STG}	Storage temperature	-65	150	°C	1
T _J	Junction temperature	-	125	°C	

Note:

1. For flash programming and retention maximum limits, refer to [Table 3](#) on [page 11](#). For recommended operating conditions, refer to [Table 2](#) on [page 10](#).



Table 2 • Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
T _J	Operating junction temperature	Commercial	0	25	85	°C	
		Industrial	-40	25	100	°C	
	Programming junction temperatures	Commercial	0	25	85	°C	
		Industrial	0	25	85	°C	
VDD	DC core supply voltage. Must always power this pin.		1.14	1.2	1.26	V	
VDD_2V5	DC Bias supply voltage. Must always power this pin.	1.2 V range	1.14	1.2	1.26	V	
		2.5 V range	2.375	2.5	2.625	V	
VPP	Power supply for charge pumps (for normal operation and programming)	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	
MDDR_PLL_VDDA	Analog power pad for MDDR PLL	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	
FDDR_PLL_VDDA	Analog power pad for FDDR PLL	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	
PLL0_PLL1_MDDR_VDDA	Analog power pad for MDDR PLL	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	
CCC_XX[01]_PLL_VDDA	Analog power pad for PLL0 to PLL5	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	
SERDES_[01]_PLL_VDDA	High supply voltage for PLL SERDES[01]	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	
SERDES_[01]_L[0123]_VDDAPLL	Analog power for SERDES[01] PLL Lane0 to Lane3. This is a +2.5 V SERDES internal PLL supply.		2.375	2.5	2.625	V	
SERDES_[01]_L[0123]_VDDAIO	Tx/Rx analog I/O voltage. Low voltage power for the lanes of SERDESIF0. This is a +1.2 V SERDES PMA supply.		1.14	1.2	1.26	V	
SERDES_[01]_VDD	PCIe/PCS power supply		1.14	1.2	1.26	V	
VDDIx	1.2 V DC supply voltage		1.14	1.2	1.26	V	
	1.5 V DC supply voltage		1.425	1.5	1.575	V	
	1.8 V DC supply voltage		1.71	1.8	1.89	V	
	2.5 V DC supply voltage		2.375	2.5	2.625	V	
	3.3 V DC supply voltage		3.15	3.3	3.45	V	
	LVDS differential I/O		2.375	2.5	3.45	V	
	B-LVDS, M-LVDS, Mini-LVDS, RSDS differential I/O		2.375	2.5	2.625	V	
LVPECL differential I/O		3.15	3.3	3.45	V		
VREFx	Reference voltage supply for FDDR (bank 0) and MDDR (bank 5)		0.49 * VDDIx	0.5 * VDDIx	0.51 * VDDIx	V	
VPPNVM	Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to VPP.	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	

Table 3 • FPGA and Embedded Flash Programming, Storage, and Operating Limits

Product Grade	Storage Temperature	Programming Temperature	Element	Grade Programming Cycles	Retention
Commercial	Min. T _J = 0°C Max. T _J = 85°C	Min. T _J = 0°C Max. T _J = 85°C	FPGA	500	20 years
		Min. T _J = 0°C Max. T _J = 85°C	Embedded flash	< 1,000	20 years
				< 10,000	10 years
Industrial	Min. T _J = -40°C Max. T _J = 100°C	Min. T _J = 0°C Max. T _J = 85°C	FPGA	500	20 years
		Min. T _J = -40°C Max. T _J = 100°C	Embedded flash	< 1,000	20 years
				< 10,000	10 years

Thermal Characteristics

Introduction

The temperature variable in the Microsemi SoC Products Group Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption will cause the chip's junction temperature to be higher than the ambient, case, or board temperatures. EQ 1 through EQ 3 give the relationship between thermal resistance, temperature gradient, and power.

$$\theta_{JA} = \frac{T_J - T_A}{P} \quad \text{EQ 1}$$

$$\theta_{JB} = \frac{T_J - T_B}{P} \quad \text{EQ 2}$$

$$\theta_{JC} = \frac{T_J - T_C}{P} \quad \text{EQ 3}$$

where

θ_{JA} = Junction-to-air thermal resistance

θ_{JB} = Junction-to-board thermal resistance

θ_{JC} = Junction-to-case thermal resistance

T_J = Junction temperature

T_A = Ambient temperature

T_B = Board temperature (measured 1.0 mm away from the package edge)

T_C = Case temperature

P = Total power dissipated by the device



Table 4 • Package Thermal Resistance

Product	θ_{JA}			θ_{JC}	θ_{JB}	Units
	Still Air	1.0 m/s	2.5 m/s			
M2S005						
FG484	TBD	TBD	TBD	TBD	TBD	°C/W
VF400	TBD	TBD	TBD	TBD	TBD	°C/W
M2S010						
FG484	18.2	14.8	13.6	8.8	4.9	°C/W
VF400	TBD	TBD	TBD	TBD	TBD	°C/W
M2S025						
FG484	TBD	TBD	TBD	TBD	TBD	°C/W
VF400	TBD	TBD	TBD	TBD	TBD	°C/W
M2S050						
FG484	15.3	12.2	11	6.3	3.2	°C/W
FG896	14.7	12.5	10.9	7.2	4.9	°C/W
VF400	TBD	TBD	TBD	TBD	TBD	°C/W
M2S090						
FG676	TBD	TBD	TBD	TBD	TBD	°C/W
FG484	TBD	TBD	TBD	TBD	TBD	°C/W
M2S100						
FC1152	TBD	TBD	TBD	TBD	TBD	°C/W
M2S150						
FC1152	TBD	TBD	TBD	TBD	TBD	°C/W

Theta-JA

Junction-to-ambient thermal resistance (θ_{JA}) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in actual performance of the product. It should be used with caution, but it is useful for comparing the thermal performance of one package to another.

The maximum power dissipation allowed is calculated using EQ 4.

$$\text{Maximum Power Allowed} = \frac{T_{J(\text{MAX})} - T_{A(\text{MAX})}}{\theta_{JA}}$$

EQ 4

The absolute maximum junction temperature is 100°C. EQ 5 shows a sample calculation of the absolute maximum power dissipation allowed for the M2S050T-FG896 package at commercial temperature and in still air, where

$$\theta_{JA} = 14.7^\circ\text{C/W (taken from Table 4 on page 12).}$$

$$T_A = 85^\circ\text{C}$$

$$\text{Maximum Power Allowed} = \frac{100^\circ\text{C} - 85^\circ\text{C}}{14.7^\circ\text{C/W}} = 1.088 \text{ W}$$

EQ 5

The power consumption of a device can be calculated using the Microsemi SoC Products Group power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package. If the power consumption is higher than the device's maximum allowable power dissipation, a heat sink can be attached on top of the case, or the airflow inside the system must be increased.

Theta-JB

Junction-to-board thermal resistance (θ_{JB}) measures the ability of the package to dissipate heat from the surface of the chip to the PCB. As defined by the JEDEC (JESD-51) standard, the thermal resistance from junction to board uses an isothermal ring cold plate zone concept. The ring cold plate is simply a means to generate an isothermal boundary condition at the perimeter. The cold plate is mounted on a JEDEC standard board with a minimum distance of 5.0 mm away from the package edge.

Theta-JC

Junction-to-case thermal resistance (θ_{JC}) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks. Constant temperature is applied to the surface in consideration and acts as a boundary condition. This only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration.



Calculating Power Dissipation

Quiescent Supply Current

Table 5 • Quiescent Supply Current Characteristics

Power Supplies Configuration	Modes and Power Supplies		Notes
	Non-Flash*Freeze mode	Flash*Freeze mode	
FPGA Core	On	Off	
VDD / SERDES_[01]_VDD	On	On	1
VPP / VPPNVM	On	On	
MDDR_PLL_VDDA / FDDR_PLL_VDDA/ CCC_XX[01]_PLL_VDDA / PLL0_PLL1_MDDR_VDDA	0 V	0 V	
SERDES_[01]_PLL_VDDA	0 V	0 V	3
SERDES_[01]_L[0123]_VDDAPLL / VDD_2V5	On	On	3
SERDES_[01]_L[0123]_VDDAIIO	On	On	3
VDDIx	On	On	2, 4
VREFx	On	On	
MSSDDR CLK	32 KHz	32 KHz	
RAM	On	Sleep state	
MSS Controller	50 MHz	50 MHz	
50 MHz Oscillator (enable/disable)	Enabled	Disabled	
1 MHz Oscillator (enable/disable)	Disabled	Disabled	
Crystal Oscillator (enable/disable)	Disabled	Disabled	
Notes:			
1. SERDES_[01]_VDD Power Supply is shorted to VDD.			
2. VDDIx has been set to ON for test conditions as described. Banks on the east side should always be powered with the appropriate VDDI bank supplies. For details on bank power supplies, refer to the "Recommendation for Unused Bank Supplies" table in the SmartFusion2 Board Design Guidelines application note.			
3. SERDES and DDR blocks to be unused.			
4. No Differential (i.e. LVDS) I/O's or ODT attributes to be used.			

Table 6 • Quiescent Supply Current

Parameter	Modes	Conditions	M2S050T	Units
			VDD = 1.2 V	
IDC1	Non-Flash*Freeze mode	Typical conditions (25°C)	7.5	mA
IDC2	Flash*Freeze mode	Typical conditions (25°C)	0.387	mA

Average Fabric Temperature and Voltage Derating Factors

Table 7 • Average Temperature and Voltage Derating Factors for Fabric Timing Delays (normalized to $T_J = 85^\circ\text{C}$, worst-case $V_{DD} = 1.14\text{ V}$)

Array Voltage VCC (V)	Junction Temperature ($^\circ\text{C}$)					
	-40°C	0°C	25°C	70°C	85°C	100°C
1.14	0.831	0.886	0.919	0.980	1.000	1.021
1.2	0.752	0.802	0.832	0.888	0.906	0.925
1.26	0.689	0.735	0.762	0.813	0.830	0.848

Timing Model

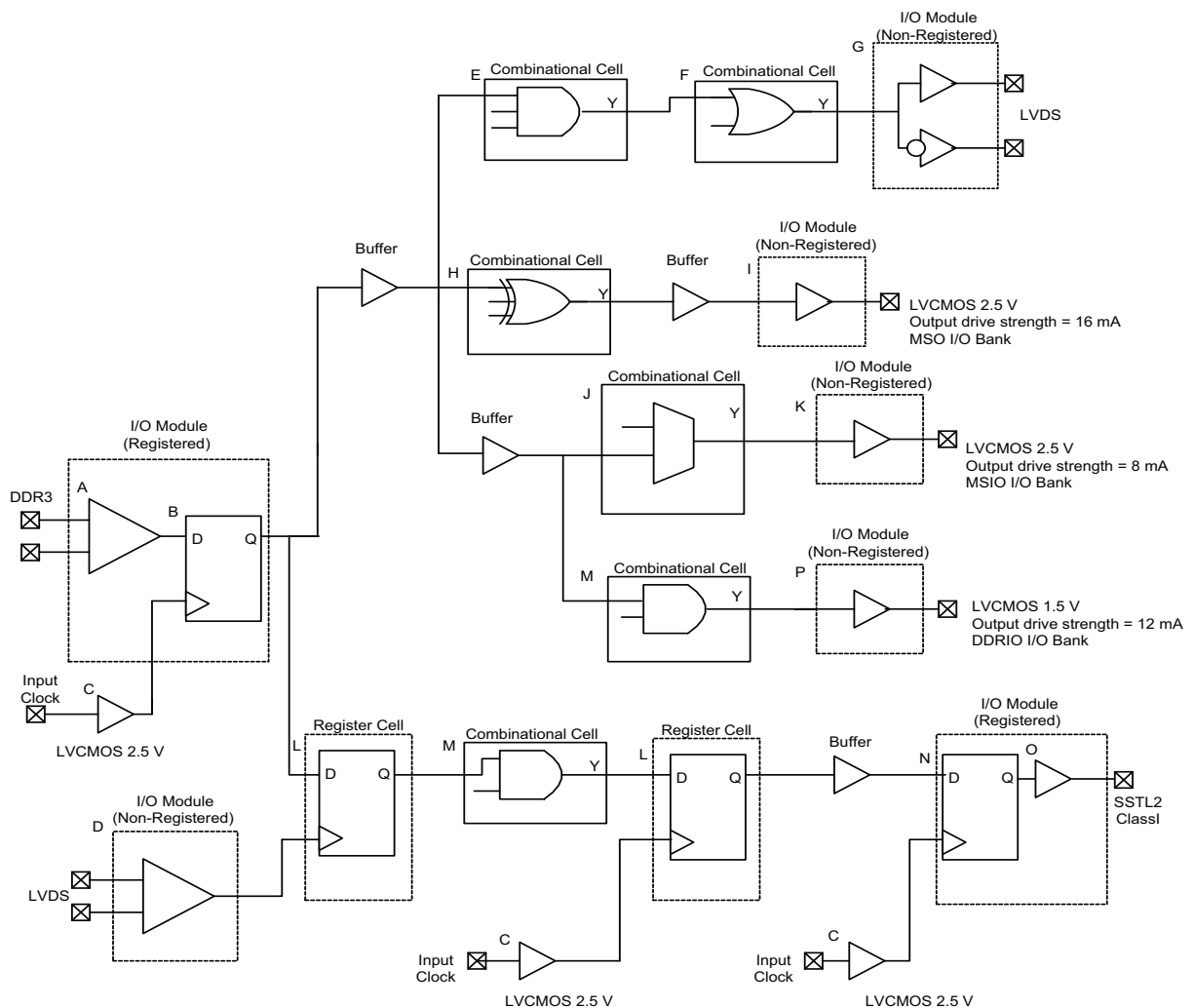


Figure 1 • Timing Model



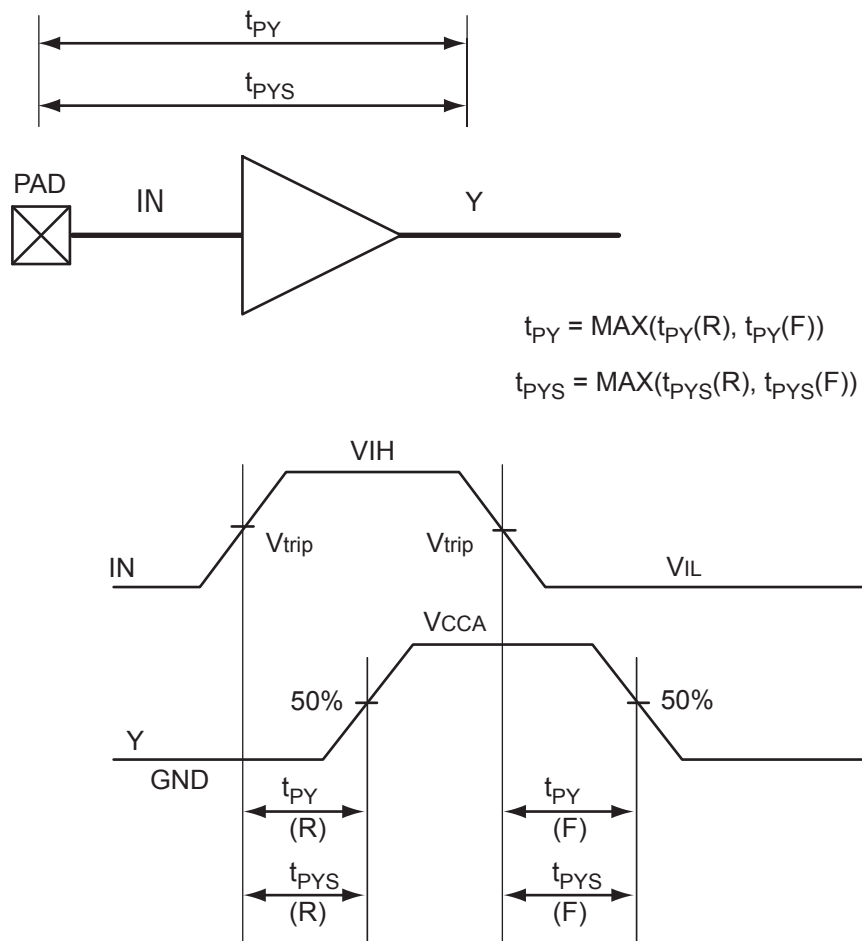
Table 8 • Timing Model Parameters

Index	Parameter	Description	Value	Units	For more information
A	t_{PY}	Propagation delay of DDR3 receiver	1.676	ns	Refer to page 53
B	t_{iCLKQ}	Clock-to-Q of the Input Data Register	0.168	ns	Refer to page 67
	t_{iSUD}	Setup Time of the Input Data Register	0.376	ns	Refer to page 67
C	t_{RCKH}	Input High Delay for Global Clock	1.655	ns	Refer to page 80
	t_{RCKL}	Input Low Delay for Global Clock	0.901	ns	Refer to page 80
D	t_{PY}	Input Propagation Delay of LVDS Receiver	3.1	ns	Refer to page 57
E	t_{DP}	Propagation Delay of a three input AND Gate	0.22	ns	Refer to page 77
F	t_{DP}	Propagation Delay of a OR Gate	0.172	ns	Refer to page 77
G	t_{DP}	Propagation Delay of a LVDS Transmitter	2.155	ns	Refer to page 57
H	t_{DP}	Propagation Delay of a three input XOR Gate	0.24	ns	Refer to page 77
I	t_{DP}	Propagation Delay of LVCMOS 2.5 V Transmitter, Drive strength of 16 mA on the MSIO Bank	2.393	ns	Refer to page 25
J	t_{DP}	Propagation Delay of a two input MUX gate	0.172	ns	Refer to page 77
K	t_{DP}	Propagation Delay of LVCMOS 2.5 V Transmitter, Drive strength of 8 mA on the MSIO Bank	2.29	ns	Refer to page 25
L	t_{CLKQ}	Clock-to-Q of the Data Register	0.114	ns	Refer to page 79
	t_{SUD}	Setup Time of the Data Register	0.267	ns	Refer to page 79
M	t_{DP}	Propagation Delay of a two input AND gate	0.172	ns	Refer to page 77
N	t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.277	ns	Refer to page 67
	t_{OSUD}	Setup Time of the Output Data Register	TBD	ns	Refer to page 67
O	t_{DP}	Propagation Delay of SSTL2, Class I Transmitter on the MSIO Bank	2.037	ns	Refer to page 45
P	t_{DP}	Propagation Delay of LVCMOS 1.5 V Transmitter, Drive strength of 12 mA, fast slew on the DDRIO Bank	3.298	ns	Refer to page 32

User I/O Characteristics

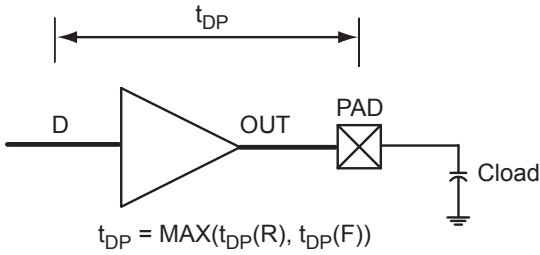
There are three types of I/Os supported in the SmartFusion2 FPGA Family: MSIO, MSIOD, and DDRIO I/O banks. The I/O standards supported by the different I/O banks is described in the "I/Os" section of the *SmartFusion2 FPGA Fabric Architecture User's Guide*.

Input Buffer and AC Loading

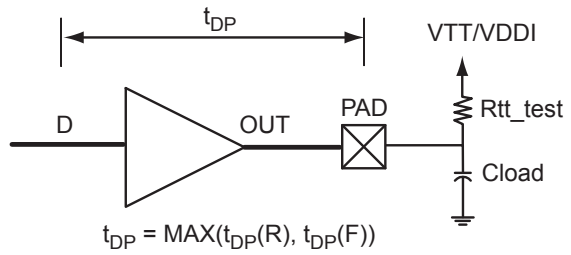


Output Buffer and AC Loading

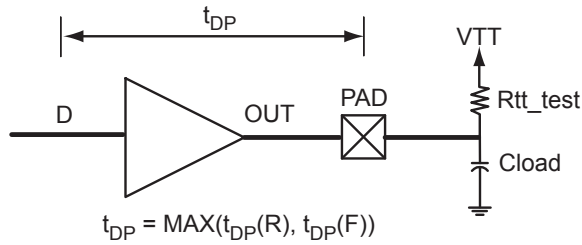
Single-Ended I/O Test Setup



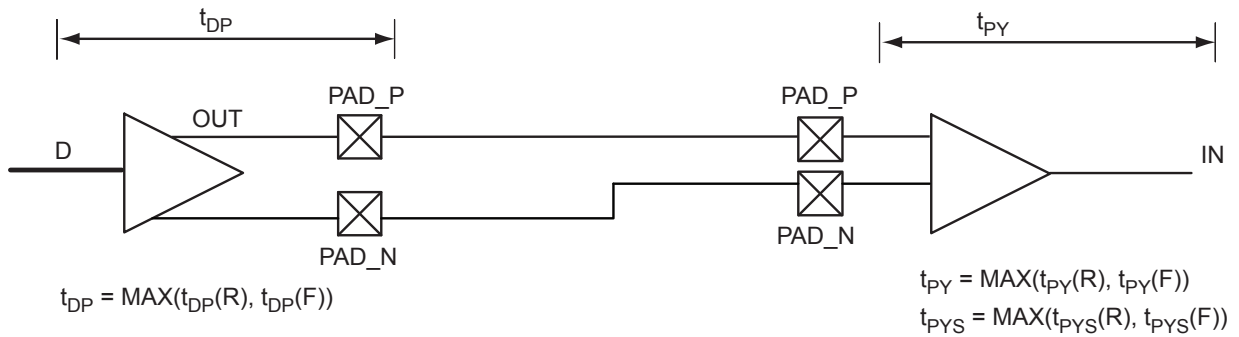
HSTL/PCI Test Setup



Voltage-Referenced, Singled-Ended I/O Test Setup



Differential I/O Test Setup



Tristate Buffer and AC Loading

The tristate path for enable path loadings is described in the respective specifications. The methodology of characterization is illustrated by the enable path test point shown in Figure 2.

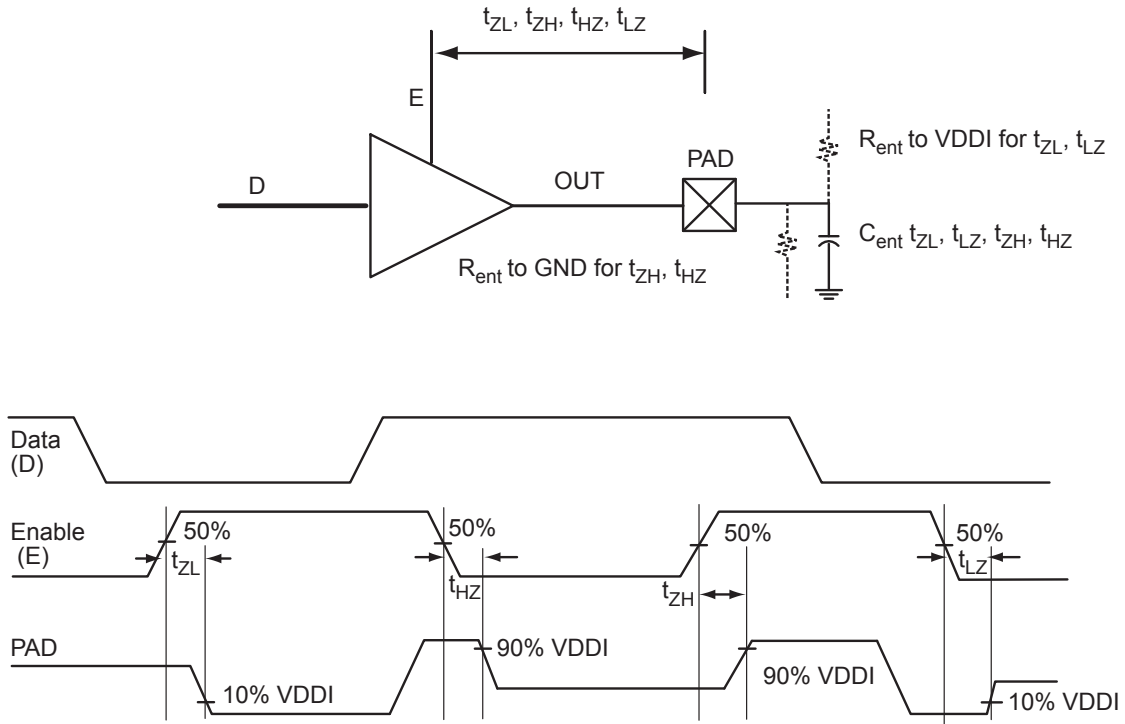


Figure 2 • Tristate Buffer for Enable Path Test Point



Detailed I/O Characteristics

Table 9 • Input Capacitance

Symbol	Definition	Minimum	Maximum	Units
C _{IN}	Input capacitance	–	10	pF

Table 10 • I/O Weak Pull-Up/Pull-Down Resistances for DDRIO I/O Bank
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values at VOH/VOL Level

VDDI Domain	DDRIO I/O Bank				Notes
	R(WEAK PULL-UP) at VOH (Ω)		R(WEAK PULL-DOWN) at VOL (Ω)		
	Min.	Max.	Min.	Max.	
3.3 V	N/A	N/A	N/A	N/A	–
2.5 V	10.6 K	17.3 K	10.5 K	18.1 K	1, 2
1.8 V	1.11 K	19.3 K	11.2 K	20.9 K	1, 2
1.5 V	10 K	13.4 K	9.99 K	13.4 K	1, 2
1.2 V	10.3 K	14.5 K	10.3 K	14.7 K	1, 2

Notes:

1. $R(\text{WEAK PULL-DOWN}) = (VOL_{\text{spec}}) / I(\text{WEAK PULL-DOWN MAX})$
2. $R(\text{WEAK PULL-UP}) = (VDDI_{\text{max}} - VOH_{\text{spec}}) / I(\text{WEAK PULL-UP MIN})$

Table 11 • I/O Weak Pull-Up/Pull-Down Resistances for MSIO I/O Bank
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values at VOH/VOL Level

VDDI Domain	MSIO I/O Bank				Notes
	R(WEAK PULL-UP) at VOH (Ω)		R(WEAK PULL-DOWN) at VOL (Ω)		
	Min.	Max.	Min.	Max.	
3.3 V	9.9 K	14.7 K	10.1 K	15.3 K	–
2.5 V	10.1 K	15.1 K	10.1 K	15.7 K	1, 2
1.8 V	10.4 K	16.2 K	10.4 K	17.3 K	1, 2
1.5 V	10.7 K	17.3 K	10.8 K	18.9 K	1, 2
1.2 V	11.3 K	19.7 K	11.5 K	22.7 K	1, 2

Notes:

1. $R(\text{WEAK PULL-DOWN}) = (VOL_{\text{spec}}) / I(\text{WEAK PULL-DOWN MAX})$
2. $R(\text{WEAK PULL-UP}) = (VDDI_{\text{max}} - VOH_{\text{spec}}) / I(\text{WEAK PULL-UP MIN})$

Table 12 • I/O Weak Pull-Up/Pull-Down Resistances for MSIOD I/O Bank
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values at VOH/VOL Level

VDDI Domain	R(WEAK PULL-UP) at VOH (Ω)		R(WEAK PULL-DOWN) at VOL (Ω)		Notes
	Min.	Max.	Min.	Max.	
3.3 V	N/A	N/A	N/A	N/A	–
2.5 V	9.6 K	14.1 K	9.5 K	13.9 K	1, 2
1.8 V	9.7 K	14.7 K	9.7 K	14.5 K	1, 2
1.5 V	9.9 K	15.3 K	9.8 K	15 K	1, 2
1.2 V	10.3 K	16.7 K	10 K	16.2 K	1, 2

Notes:

1. $R(\text{WEAK PULL-DOWN}) = (VOL_{\text{spec}}) / I(\text{WEAK PULL-DOWN MAX})$
2. $R(\text{WEAK PULL-UP}) = (VDDI_{\text{max}} - VOH_{\text{spec}}) / I(\text{WEAK PULL-UP MIN})$

Table 13 • Schmitt Trigger Input Hysteresis
Hysteresis Voltage Value for Schmitt Trigger Mode Input Buffers

Input Buffer Configuration	Hysteresis Value (typical, unless otherwise noted)
3.3 V LVTTTL / LVCMOS / PCI / PCI-X	$0.05 \times VDDI$ (worst-case)
2.5 V LVCMOS	$0.05 \times VDDI$ (worst-case)
1.8 V LVCMOS	$0.1 \times VDDI$ (worst-case)
1.5 V LVCMOS	60 mV
1.2 V LVCMOS	20 mV



Single-Ended I/O Standards

Low Voltage Complementary Metal Oxide Semiconductor (LVCMOS)

LVCMOS is a widely used switching standard implemented in CMOS transistors. This standard is defined by JEDEC (JESD 8-5). The LVCMOS standards supported in SmartFusion2 SoC FPGAs are LVCMOS12, LVCMOS15, LVCMOS18, LVCMOS25, and LVCMOS33.

3.3 V LVCMOS/LVTTL

LVCMOS 3.3 V or Low-Voltage Transistor-Transistor Logic (LVTTL) is a general standard for 3.3 V applications.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 14 • LVTTL/LVCMOS 3.3 V DC Voltage Specification

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		3.15	3.3	3.45	V	
LVTTL/LVCMOS 3.3 V DC Input Voltage Specification							
VIH (DC)	DC input logic High		2.0	–	3.45	V	
VIL (DC)	DC input logic Low		–0.3	–	0.8	V	
IIH (DC)	Input current High		–	–	10	μA	
IIL (DC)	Input current Low		–	–	10	μA	
LVCMOS 3.3 V DC Output Voltage Specification							
VOH	DC output logic High		VDDI – 0.4	–	–	V	1
VOL	DC output logic Low		–	–	0.4	V	1
LVTTL 3.3 V DC Output Voltage Specification							
VOH	DC output logic High		2.4	–	–	V	
VOL	DC output logic Low		–	–	0.4	V	

Notes:

1. The VOH/VOL test points selected ensure compliance with LVCMOS 3.3 V JESD8-B requirements.

Table 15 • LVTTL/LVCMOS 3.3 V Minimum and Maximum AC Input and Output Levels

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
LVTTL/LVCMOS 3.3 V AC Specifications							
Fmax	Maximum data rate (for MSIO I/O bank)	AC loading: 10 pF / 500 Ohm load, maximum drive/slew	–	–	600	Mbps	
LVTTL/LVCMOS 3.3 V AC Test Parameters Specifications							
Vtrip	Measuring/trip point for data path		–	1.4	–	V	
Rent	Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	5	–	pF	
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF	

Table 16 • LVTTTL/LVCMOS 3.3 V Transmitter Drive Strength Specifications

Output Drive Selection	VOH (V)	VOL (V)	IOH (at VOH) mA	IOL (at VOL) mA	Notes
MSIO I/O Bank					
2 mA	VDDI – 0.4	0.4	2	2	
4 mA	VDDI – 0.4	0.4	4	4	
8 mA	VDDI – 0.4	0.4	8	8	
12 mA	VDDI – 0.4	0.4	12	12	
16 mA	VDDI – 0.4	0.4	16	16	
20 mA	VDDI – 0.4	0.4	20	20	

Note: For a detailed I/V curve, use the corresponding IBIS models: www.microsemi.com/soc/download/ibis/default.aspx.

AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 3.0 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 17 • LVTTTL/LVCMOS 3.3 V Receiver Characteristics

	On-Die Termination (ODT)	t _{py}		t _{pys}		Units
		–1	Std.	–1	Std.	
LVTTTL/LVCMOS 3.3 V (For MSIO I/O bank)	None	3.016	3.549	3.34	3.93	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 18 • LVTTTL/LVCMOS 3.3 V Transmitter Characteristics

Output Drive Selection	Slew Control	t _{DP}		t _{ENZL}		t _{ENZH}		t _{ENHZ}		t _{ENLZ}		Units
		–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	
LVTTTL/LVCMOS 3.3 V (for MSIO I/O bank)												
2 mA	Slow	3.161	3.719	3.487	4.101	3.292	3.872	3.642	4.283	3.443	4.05	ns
4 mA	Slow	2.311	2.72	2.927	3.444	4.403	5.18	3.078	3.622	4.554	5.358	ns
8 mA	Slow	2.117	2.491	4.22	4.965	4.773	5.615	4.371	5.143	4.924	5.793	ns
12 mA	Slow	2.033	2.392	5.595	6.582	5.389	6.34	5.746	6.76	5.54	6.518	ns
16 mA	Slow	2.044	2.405	5.826	6.854	5.567	6.549	5.977	7.032	5.718	6.727	ns
20 mA	Slow	2.129	2.505	6.018	7.08	5.818	6.844	6.169	7.258	5.969	7.022	ns



LVC MOS 2.5 V

LVC MOS 2.5 V is a general standard for 2.5 V applications and is supported in SmartFusion2 FPGAs in compliance to the JEDEC specification JESD8-5A.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 19 • LVC MOS 2.5 V DC Voltage Specification

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		2.375	2.5	2.625	V	
LVC MOS 2.5 V DC Input Voltage Specification							
VIH (DC)	DC input logic High for (MSIOD and DDRIO I/O bank)		1.7	–	2.625	V	
VIH (DC)	DC input logic High (for MSIO I/O bank)		1.7	–	3.45	V	
VIL (DC)	DC input logic Low		–0.3	–	0.7	V	
IIH (DC)	Input current High		–	–	10	μA	
IIL (DC)	Input current Low		–	–	10	μA	
LVC MOS 2.5 V DC Output Voltage Specification							
VOH	DC output logic High	VDDI – 0.4	–	–	–	V	1
VOL	DC output logic Low		–	–	0.4	V	1

Notes:

1. The VOH/VOL test points selected ensure compliance with LVC MOS 2.5 V JEDEC8-5A requirements.

Table 20 • LVC MOS 2.5 V Minimum and Maximum AC Input and Output Levels

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
LVC MOS 2.5 V AC Specifications							
Fmax	Maximum data rate (for DDRIO I/O bank)	AC loading: 5 pF load, maximum drive/slew	–	–	250	Mbps	
Fmax	Maximum data rate (for MSIO I/O bank)	AC loading: 10 pF / 500 Ohm load, maximum drive/slew	–	–	410	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank)	AC loading: 10 pF / 500 Ohm load, maximum drive/slew	–	–	420	Mbps	
	Supported output driver calibrated impedance (for DDRIO I/O bank)			75, 60, 50, 33, 25, 20		Ohms	
LVC MOS 2.5 V AC Test Parameters Specifications							
Vtrip	Measuring/trip point for data path			1.2		V	
Rent	Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})			2K		Ohms	
Cent	Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})			5		pF	
Cload	Capacitive loading for data path (t_{DP})			5		pF	

Table 21 • LVCMOS 2.5 V Transmitter Drive Strength Specifications

Output Drive Selection			VOH (V)	VOL (V)	IOH (at VOH)	IOL (at VOL)	Notes
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank	Min.	Max.	mA	mA	
2 mA	2 mA	2 mA	VDDI – 0.4	0.4	2	2	
4 mA	4 mA	4 mA	VDDI – 0.4	0.4	4	4	
6 mA	6 mA	6 mA	VDDI – 0.4	0.4	6	6	
8 mA	8 mA	8 mA	VDDI – 0.4	0.4	8	8	
12 mA	12 mA	12 mA	VDDI – 0.4	0.4	12	12	
16 mA	N/A	16 mA	VDDI – 0.4	0.4	16	16	

Note: For a detailed I/V curve, use the corresponding IBIS models: www.microsemi.com/soc/download/ibis/default.aspx.

AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 2.375 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 22 • LVCMOS 2.5 V Receiver Characteristics

	On-Die Termination (ODT)	t _{py}		t _{pys}		Units
		–1	Std.	–1	Std.	
LVCMOS 2.5 V (for DDRIO I/O bank)	None	1.907	2.244	2.105	2.478	ns
LVCMOS 2.5 V (for MSIO I/O bank)	None	3.07	3.612	3.412	4.014	ns
LVCMOS 2.5 V (for MSIOD I/O bank)	None	2.885	3.395	3.32	3.905	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 23 • LVCMOS 2.5 V Transmitter Characteristics

Output Drive Selection	Slew Control	t _{DP}		t _{ENZL}		t _{ENZH}		t _{ENHZ}		t _{ENLZ}		Units
		–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	
LVCMOS 2.5 V (for DDRIO I/O bank with FIXED CODES)												
2 mA	Slow	3.678	4.326	3.791	4.46	3.766	4.43	3.967	4.666	3.669	4.316	ns
	Medium	3.191	3.754	3.372	3.968	3.295	3.876	3.548	4.174	3.198	3.762	ns
	Medium fast	3.076	3.619	3.263	3.84	3.179	3.739	3.439	4.046	3.082	3.625	ns
	Fast	3.064	3.604	3.256	3.831	3.168	3.727	3.432	4.037	3.071	3.613	ns
4 mA	Slow	3.111	3.659	4.64	5.46	4.247	4.997	4.816	5.666	4.423	5.203	ns
	Medium	2.677	3.149	4.127	4.856	3.72	4.377	4.303	5.062	3.896	4.583	ns
	Medium fast	2.571	3.024	4.023	4.734	3.626	4.267	4.199	4.94	3.802	4.473	ns
	Fast	2.559	3.01	4.016	4.726	3.62	4.26	4.192	4.932	3.796	4.466	ns
6 mA	Slow	2.933	3.45	4.974	5.852	4.568	5.375	5.15	6.058	4.744	5.581	ns
	Medium	2.667	3.137	4.726	5.561	4.276	5.032	4.902	5.767	4.452	5.238	ns
	Medium fast	2.546	2.994	4.617	5.433	4.163	4.899	4.793	5.639	4.339	5.105	ns
	Fast	2.533	2.98	4.608	5.422	4.157	4.891	4.784	5.628	4.333	5.097	ns



Table 23 • LVCMOS 2.5 V Transmitter Characteristics (continued)

Output Drive Selection	Slew Control	t _{DP}		t _{ENZL}		t _{ENZH}		t _{ENHZ}		t _{ENLZ}		Units
		-1	Std.	-1	Std.	-1	Std.	-1	Std.	-1	Std.	
8 mA	Slow	2.877	3.384	5.09	5.99	4.662	5.485	5.266	6.196	4.838	5.691	ns
	Medium	2.461	2.895	4.512	5.309	4.07	4.789	4.688	5.515	4.246	4.995	ns
	Medium fast	2.357	2.772	4.42	5.201	3.977	4.679	4.596	5.407	4.153	4.885	ns
	Fast	2.345	2.759	4.415	5.194	3.971	4.672	4.591	5.4	4.147	4.878	ns
12 mA	Slow	2.761	3.248	5.287	6.221	4.839	5.693	5.463	6.427	5.015	5.899	ns
	Medium	2.361	2.777	4.692	5.521	4.223	4.969	4.868	5.727	4.399	5.175	ns
	Medium fast	2.262	2.661	4.616	5.431	4.137	4.868	4.792	5.637	4.313	5.074	ns
	Fast	2.251	2.648	4.613	5.428	4.131	4.861	4.789	5.634	4.307	5.067	ns
16 mA	Slow	2.691	3.165	5.473	6.44	4.98	5.859	5.649	6.646	5.156	6.065	ns
	Medium	2.302	2.708	4.863	5.722	4.345	5.112	5.039	5.928	4.521	5.318	ns
	Medium fast	2.207	2.596	4.81	5.66	4.265	5.018	4.986	5.866	4.441	5.224	ns
	Fast	2.196	2.583	4.808	5.657	4.26	5.012	4.984	5.863	4.436	5.218	ns
LVCMOS 2.5 V (for MSIO I/O bank)												
2 mA	None	3.462	4.074	3.876	4.56	3.803	4.474	3.951	4.648	3.878	4.562	ns
4 mA	None	2.565	3.018	3.943	4.639	4.699	5.528	4.017	4.726	4.773	5.615	ns
6 mA	None	2.374	2.794	4.844	5.699	5.091	5.989	4.918	5.786	5.165	6.076	ns
8 mA	None	2.29	2.695	5.782	6.803	5.531	6.507	5.856	6.89	5.605	6.594	ns
12 mA	None	2.315	2.724	5.947	6.996	5.719	6.728	6.021	7.083	5.793	6.815	ns
16 mA	None	2.393	2.816	6.354	7.475	6.007	7.067	6.428	7.562	6.081	7.154	ns
LVCMOS 2.5 V (for MSIOD I/O bank)												
2 mA	None	2.187	2.573	4.885	5.748	4.742	5.579	4.99	5.87	4.847	5.701	ns
4 mA	None	1.815	2.135	5.349	6.293	5.128	6.034	5.454	6.415	5.233	6.156	ns
6 mA	None	1.689	1.987	5.741	6.755	5.466	6.432	5.846	6.877	5.571	6.554	ns
8 mA	None	1.613	1.898	6.163	7.251	5.773	6.792	6.268	7.373	5.878	6.914	ns
12 mA	None	1.632	1.919	6.452	7.592	5.979	7.035	6.557	7.714	6.084	7.157	ns

1.8 V LVCMOS

LVCMOS 1.8 is a general standard for 1.8 V applications and is supported in SmartFusion2 FPGAs in compliance to the JEDEC specification JESD8-7A.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 24 • LVCMOS 1.8 V DC Voltage Specification

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		1.710	1.8	1.89	V	
LVCMOS 1.8 V DC Input Voltage Specification							
VIH (DC)	DC input logic High for (MSIOD and DDRIO I/O bank)	$0.65 * VDDI$	–	–	1.89	V	
VIH (DC)	DC input logic High (for MSIO I/O bank)	$0.65 * VDDI$	–	–	3.45	V	
VIL (DC)	DC input logic Low	–0.3	–	–	$0.35 * VDDI$	V	
IIH (DC)	Input current High	–	–	–	10	μA	
IIL (DC)	Input current Low	–	–	–	10	μA	
LVCMOS 1.8 V DC Output Voltage Specification							
VOH	DC output logic High	$VDDI - 0.45$	–	–	–	V	
VOL	DC output logic Low	–	–	–	0.45	V	

Table 25 • LVCMOS 1.8 V Minimum and Maximum AC Input and Output Levels

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
LVCMOS 1.8 V AC Specifications							
Fmax	Maximum data rate (for DDRIO I/O bank)	AC loading: 5 pF load, maximum drive/slew	–	–	200	Mbps	
Fmax	Maximum data rate (for MSIO I/O bank)	AC loading: 10 pF / 500 Ohm load, maximum drive/slew	–	–	295	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank)	AC loading: 10 pF / 500 Ohm load, maximum drive/slew	–	–	320	Mbps	
	Supported output driver calibrated impedance (for DDRIO I/O bank)			75, 60, 50, 33, 25, 20		Ohms	
LVCMOS 1.8 V AC Test Parameters Specifications							
Vtrip	Measuring/trip point for data path		–	0.9	–	V	
Rent	Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	2k	–	Ohms	
Cent	Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	5	–	pF	
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF	



Table 26 • LVCMOS 1.8 V Transmitter Drive Strength Specifications

Output Drive Selection			VOH (V)	VOL (V)	IOH (at VOH)	IOL (at VOL)	Notes
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank	Min.	Max.	mA	mA	
2 mA	2 mA	2 mA	VDDI – 0.4	0.45	2	2	
4 mA	4 mA	4 mA	VDDI – 0.4	0.45	4	4	
6 mA	6 mA	6 mA	VDDI – 0.4	0.45	6	6	
8 mA	8 mA	8 mA	VDDI – 0.4	0.45	8	8	
10 mA	10 mA	10 mA	VDDI – 0.4	0.45	10	10	
12 mA	N/A	12 mA	VDDI – 0.4	0.45	12	12	
N/A	N/A	16 mA	VDDI – 0.4	0.45	16	16	

Note: For a detailed I/V curve, use the corresponding IBIS models: www.microsemi.com/soc/download/ibis/default.aspx.

AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 1.71 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 27 • LVCMOS 1.8 V Receiver Characteristics

	On-Die Termination (ODT)	t _{py}		t _{pys}		Units
		–1	Std.	–1	Std.	
LVCMOS 1.8 V (for DDRIO I/O bank)	None	2.088	2.458	2.334	2.747	ns
	50	2.11	2.484	2.414	2.841	ns
	75	2.104	2.477	2.397	2.822	ns
	150	2.1	2.471	2.375	2.795	ns
LVCMOS 1.8 V (for MSIO I/O bank)	None	3.948	4.645	4.224	4.969	ns
	50	4.372	5.144	5.11	6.012	ns
	75	4.214	4.957	4.722	5.556	ns
	150	4.077	4.797	4.473	5.263	ns
LVCMOS 1.8 V (for MSIOD I/O bank)	None	3.613	4.25	3.885	4.571	ns
	50	4.079	4.799	5.237	6.161	ns
	75	3.899	4.586	4.608	5.421	ns
	150	3.723	4.38	4.17	4.905	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 28 • LVCMOS 1.8 V Transmitter Characteristics

Output Drive Selection	Slew Control	t _{DP}		t _{ENZL}		t _{ENZH}		t _{ENHZ}		t _{ENLZ}		Units
		-1	Std.	-1	Std.	-1	Std.	-1	Std.	-1	Std.	
LVCMOS 1.8 V (for DDRIO I/O bank)												
2 mA	Slow	4.225	4.971	4.686	5.512	4.292	5.05	4.975	5.853	4.517	5.314	ns
	Medium	3.814	4.487	4.409	5.186	3.908	4.596	4.698	5.527	4.197	4.937	ns
	Medium fast	3.617	4.256	4.264	5.015	3.775	4.44	4.553	5.356	4.064	4.781	ns
	Fast	3.595	4.229	4.254	5.004	3.764	4.427	4.543	5.345	4.053	4.768	ns
4 mA	Slow	3.906	4.595	5.179	6.092	4.676	5.5	5.468	6.433	4.965	5.841	ns
	Medium	3.508	4.127	4.894	5.757	4.353	5.12	5.183	6.098	4.642	5.461	ns
	Medium fast	3.311	3.896	4.757	5.595	4.215	4.958	5.046	5.936	4.504	5.299	ns
	Fast	3.287	3.867	4.736	5.571	4.2	4.941	5.025	5.912	4.489	5.282	ns
6 mA	Slow	3.691	4.342	5.392	6.342	4.86	5.717	5.681	6.683	5.149	6.058	ns
	Medium	3.321	3.907	5.129	6.034	4.562	5.366	5.418	6.375	4.851	5.707	ns
	Medium fast	3.142	3.696	4.988	5.867	4.439	5.221	5.277	6.208	4.728	5.562	ns
	Fast	3.121	3.671	4.981	5.859	4.429	5.21	5.27	6.2	4.718	5.551	ns
8 mA	Slow	3.594	4.228	5.588	6.574	5.015	5.899	5.877	6.915	5.304	6.24	ns
	Medium	3.234	3.805	5.315	6.252	4.72	5.552	5.604	6.593	5.009	5.893	ns
	Medium fast	3.054	3.593	5.18	6.093	4.593	5.403	5.469	6.434	4.882	5.744	ns
	Fast	3.032	3.568	5.171	6.083	4.584	5.392	5.46	6.424	4.873	5.733	ns
10 mA	Slow	3.478	4.091	5.815	6.841	5.213	6.133	6.104	7.182	5.502	6.474	ns
	Medium	3.124	3.676	5.562	6.542	4.91	5.775	5.851	6.883	5.199	6.116	ns
	Medium fast	2.951	3.471	5.439	6.398	4.789	5.634	5.728	6.739	5.078	5.975	ns
	Fast	2.931	3.448	5.432	6.389	4.782	5.625	5.721	6.73	5.071	5.966	ns
12 mA	Slow	3.407	4.009	5.859	6.892	5.256	6.182	6.148	7.233	5.545	6.523	ns
	Medium	3.067	3.608	5.616	6.606	4.972	5.848	5.905	6.947	5.261	6.189	ns
	Medium fast	2.901	3.413	5.504	6.475	4.858	5.714	5.793	6.816	5.147	6.055	ns
	Fast	2.882	3.391	5.504	6.474	4.852	5.707	5.793	6.815	5.141	6.048	ns
16 mA	Slow	3.348	3.939	5.994	7.051	5.351	6.294	6.283	7.392	5.64	6.635	ns
	Medium	3.02	3.553	5.766	6.783	5.073	5.967	6.055	7.124	5.362	6.308	ns
	Medium fast	2.858	3.363	5.674	6.674	4.965	5.84	5.963	7.015	5.254	6.181	ns
	Fast	2.84	3.341	5.673	6.673	4.959	5.834	5.962	7.014	5.248	6.175	ns



Table 28 • LVCMOS 1.8 V Transmitter Characteristics (continued)

Output Drive Selection	Slew Control	t _{DP}		t _{ENZL}		t _{ENZH}		t _{ENHZ}		t _{ENLZ}		Units
		-1	Std.	-1	Std.	-1	Std.	-1	Std.	-1	Std.	
LVCMOS 1.8 V (for MSIO I/O bank)												
2 mA	Slow	3.422	4.026	4.697	5.525	5.233	6.156	4.682	5.507	5.218	6.138	ns
4 mA	Slow	3.194	3.758	5.426	6.383	5.664	6.663	5.411	6.365	5.649	6.645	ns
6 mA	Slow	3.119	3.669	6.398	7.526	6.132	7.214	6.383	7.508	6.117	7.196	ns
8 mA	Slow	3.143	3.697	6.652	7.825	6.309	7.422	6.637	7.807	6.294	7.404	ns
10 mA	Slow	3.18	3.741	7.028	8.268	6.529	7.68	7.013	8.25	6.514	7.662	ns
12 mA	Slow	3.253	3.827	7.159	8.421	6.627	7.796	7.144	8.403	6.612	7.778	ns
LVCMOS 1.8 V (for MSIOD I/O bank)												
2 mA	Slow	2.704	3.18	5.182	6.096	4.993	5.873	5.245	6.17	5.056	5.947	ns
4 mA	Slow	2.225	2.616	5.72	6.729	5.445	6.405	5.783	6.803	5.508	6.479	ns
6 mA	Slow	1.979	2.327	6.358	7.48	5.976	7.03	6.421	7.554	6.039	7.104	ns
8 mA	Slow	1.984	2.333	6.609	7.775	6.174	7.264	6.672	7.849	6.237	7.338	ns
10 mA	Slow	2.008	2.361	6.903	8.121	6.388	7.514	6.966	8.195	6.451	7.588	ns

1.5 V LVCMOS

LVCMOS 1.5 is a general standard for 1.5 V applications and is supported in SmartFusion2 FPGAs in compliance to the JEDEC specification JESD8-11A.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 29 • LVCMOS 1.5 V DC Voltage Specification

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		1.425	1.5	1.575	V	
LVCMOS 1.5 V DC Input Voltage Specification							
VIH (DC)	DC input logic High for (MSIOD and DDRIO I/O banks)		0.65 * VDDI	–	1.575	V	
VIH (DC)	DC input logic High (for MSIO I/O bank)		0.65 * VDDI	–	3.45	V	
VIL (DC)	DC input logic Low		–0.3	–	0.35 * VDDI	V	
IIH (DC)	Input current High		–	–	10	µA	
IIL (DC)	Input current Low		–	–	10	µA	
LVCMOS 1.5 V DC Output Voltage Specification							
VOH	DC output logic High		VDDI * 0.75	–	–	V	
VOL	DC output logic Low		–	–	VDDI * 0.25	V	

Table 30 • LVCMOS 1.5 V Minimum and Maximum AC Input and Output Levels

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
LVCMOS 1.5 V AC Specifications							
Fmax	Maximum data rate (for DDRIO I/O bank)	AC loading: 5 pF load, maximum drive/slew	–	–	130	Mbps	
Fmax	Maximum data rate (for MSIO I/O bank)	AC loading: 10 pF / 500 Ohm load, maximum drive/slew	–	–	80	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank)	AC loading: 10 pF / 500 Ohm load, maximum drive/slew	–	–	170	Mbps	
	Supported output driver calibrated impedance (for DDRIO I/O bank)			75, 60, 50, 40		Ohms	
LVCMOS 1.5 V AC Test Parameters Specifications							
Vtrip	Measuring/trip point		–	0.75	–	V	
Rent	Resistance for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		–	5	–	pF	
Cload	Capacitive loading for data path (t _{DP})		–	5	–	pF	



Table 31 • LVC MOS 1.5 V Transmitter Drive Strength Specifications

Output Drive Selection			VOH (V)		VOL (V)		IOH (at VOH) mA	IOL (at VOL) mA	Notes
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank	Min.	Max.					
2 mA	2 mA	2 mA	VDDI * 0.75	VDDI * 0.25	2	2			
4 mA	4 mA	4 mA	VDDI * 0.75	VDDI * 0.25	4	4			
6 mA	6 mA	6 mA	VDDI * 0.75	VDDI * 0.25	6	6			
8 mA	N/A	8 mA	VDDI * 0.75	VDDI * 0.25	8	8			
N/A	N/A	10 mA	VDDI * 0.75	VDDI * 0.25	10	10			
N/A	N/A	12 mA	VDDI * 0.75	VDDI * 0.25	12	12			

Note: For a detailed I/V curve, use the corresponding IBIS models: www.microsemi.com/soc/download/ibis/default.aspx.

AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 1.425 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 32 • LVC MOS 1.5 V Receiver Characteristics

	On-Die Termination (ODT)	t _{py}		t _{pys}		Units
		-1	Std.	-1	Std.	
LVC MOS 1.5 V (for DDRIO I/O bank)	None	2.173	2.558	2.257	2.655	ns
	50	2.214	2.606	2.348	2.762	ns
	75	2.19	2.578	2.313	2.72	ns
	150	2.196	2.584	2.286	2.689	ns
LVC MOS 1.5 V (for MSIO I/O bank)	None	4.786	5.63	4.979	5.857	ns
	50	5.667	6.667	6.33	7.446	ns
	75	5.357	6.302	5.765	6.783	ns
	150	5.071	5.966	5.321	6.259	ns
LVC MOS 1.5 V (for MSIOD I/O bank)	None	4.481	5.273	4.673	5.499	ns
	50	5.592	6.58	6.881	8.097	ns
	75	5.144	6.053	5.758	6.775	ns
	150	4.769	5.611	5.106	6.008	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 33 • LVC MOS 1.5 V Transmitter Characteristics

Output Drive Selection	Slew Control	t _{DP}		t _{ENZL}		t _{ENZH}		t _{ENHZ}		t _{ENLZ}		Units
		-1	Std.	-1	Std.	-1	Std.	-1	Std.	-1	Std.	
LVC MOS 1.5 V (for DDRIO I/O bank)												
2 mA	Slow	5.087	5.985	4.971	5.848	5.156	6.065	5.353	6.298	4.922	5.791	ns
	Medium	4.563	5.368	4.67	5.494	4.642	5.46	5.052	5.944	4.442	5.226	ns
	Medium fast	4.302	5.062	4.513	5.308	4.385	5.158	4.895	5.758	4.312	5.073	ns
	Fast	4.275	5.03	4.491	5.283	4.359	5.127	4.873	5.733	4.302	5.062	ns

Table 33 • LVCMOS 1.5 V Transmitter Characteristics (continued)

Output Drive Selection	Slew Control	t _{DP}		t _{ENZL}		t _{ENZH}		t _{ENHZ}		t _{ENLZ}		Units
		-1	Std.	-1	Std.	-1	Std.	-1	Std.	-1	Std.	
4 mA	Slow	4.419	5.2	5.706	6.712	5.15	6.058	6.088	7.162	5.532	6.508	ns
	Medium	3.945	4.641	5.463	6.427	4.818	5.668	5.845	6.877	5.2	6.118	ns
	Medium fast	3.708	4.362	5.315	6.252	4.679	5.505	5.697	6.702	5.061	5.955	ns
	Fast	3.683	4.333	5.301	6.236	4.67	5.493	5.683	6.686	5.052	5.943	ns
6 mA	Slow	4.217	4.962	6.099	7.175	5.427	6.384	6.481	7.625	5.809	6.834	ns
	Medium	3.753	4.415	5.796	6.818	5.094	5.992	6.178	7.268	5.476	6.442	ns
	Medium fast	3.524	4.147	5.654	6.651	4.968	5.844	6.036	7.101	5.35	6.294	ns
	Fast	3.497	4.114	5.649	6.645	4.956	5.83	6.031	7.095	5.338	6.28	ns
8 mA	Slow	4.078	4.798	6.266	7.371	5.555	6.535	6.648	7.821	5.937	6.985	ns
	Medium	3.636	4.279	5.998	7.056	5.255	6.182	6.38	7.506	5.637	6.632	ns
	Medium fast	3.415	4.108	5.861	6.895	5.137	6.042	6.243	7.345	5.519	6.492	ns
	Fast	3.39	3.989	5.854	6.886	5.128	6.032	6.236	7.336	5.51	6.482	ns
10 mA	Slow	4.01	4.718	6.41	7.541	5.666	6.665	6.792	7.991	6.048	7.115	ns
	Medium	3.579	4.211	6.152	7.237	5.366	6.312	6.534	7.687	5.748	6.762	ns
	Medium fast	3.364	3.958	6.026	7.089	5.253	6.18	6.408	7.539	5.635	6.63	ns
	Fast	3.337	3.926	6.02	7.081	5.242	6.166	6.402	7.531	5.624	6.616	ns
12 mA	Slow	3.945	4.641	6.515	7.664	5.753	6.768	6.897	8.114	6.135	7.218	ns
	Medium	3.53	4.153	6.266	7.371	5.45	6.411	6.648	7.821	5.832	6.861	ns
	Medium fast	3.321	3.907	6.163	7.251	5.337	6.278	6.545	7.701	5.719	6.728	ns
	Fast	3.298	3.881	6.16	7.247	5.331	6.271	6.542	7.697	5.713	6.721	ns
LVCMOS 1.5 V (for MSIO I/O bank)												
2 mA	Slow	4.401	5.178	5.442	6.402	5.707	6.714	5.393	6.344	5.658	6.656	ns
4 mA	Slow	4.031	4.743	7.093	8.345	6.671	7.848	7.044	8.287	6.622	7.79	ns
6 mA	Slow	4.06	4.776	7.371	8.672	6.85	8.06	7.322	8.614	6.801	8.002	ns
8 mA	Slow	4.212	4.955	7.954	9.358	7.185	8.453	7.905	9.3	7.136	8.395	ns
LVCMOS 1.5 V (for MSIOD I/O bank)												
2 mA	Slow	2.717	3.197	6.046	7.112	5.715	6.722	6.101	7.177	5.77	6.787	ns
4 mA	Slow	2.41	2.835	6.744	7.934	6.302	7.414	6.799	7.999	6.357	7.479	ns
6 mA	Slow	2.418	2.845	7.118	8.374	6.597	7.761	7.173	8.439	6.652	7.826	ns



1.2 V LVCMOS

LVCMOS 1.2 is a general standard for 1.2 V applications and is supported in SmartFusion2 FPGAs in compliance to the JEDEC specification JESD8-12A.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 34 • LVCMOS 1.2 V DC Voltage Specification

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		1.14	1.2	1.26	V	
LVCMOS 1.2 V DC Input Voltage Specification							
VIH (DC)	DC input logic High for (MSIOD and DDRIO I/O bank)		0.65 * VDDI	–	1.26	V	
VIH (DC)	DC input logic High (for MSIO I/O bank)		0.65 * VDDI	–	3.45	V	
VIL (DC)	DC input logic Low		–0.3	–	0.35 * VDDI	V	
IIH (DC)	Input current High		–	–	10	µA	
IIL (DC)	Input current Low		–	–	10	µA	
LVCMOS 1.2 V DC Output Voltage Specification							
VOH	DC output logic High		VDDI * 0.75	–	–	V	
VOL	DC output logic Low		–	–	VDDI * 0.25	V	

Table 35 • LVCMOS 1.2 V Minimum and Maximum AC Input and Output Levels

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
LVCMOS 1.2 V AC Specifications							
Fmax	Maximum data rate (for DDRIO I/O bank)	AC loading: 2 pF load, maximum drive/slew	–	–	75	Mbps	
Fmax	Maximum data rate (for MSIO I/O bank)	AC loading: 2.5 pF load, maximum drive/slew	–	–	50	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank)	AC loading: 2.5 pF load, maximum drive/slew	–	–	100	Mbps	
Rref	Supported output driver calibrated impedance (for DDRIO I/O bank)			75, 60, 50, 40		Ohms	
LVCMOS 1.2 V AC Test Parameters Specifications							
Vtrip	Measuring/trip point		–	0.6	–	V	
Rent	Resistance for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		–	5	–	pF	
Cload	Capacitive loading for data path (t _{DP})		–	5	–	pF	

Table 36 • LVCMOS 1.2 V Transmitter Drive Strength Specifications

Output Drive Selection			VOH (V)	VOL (V)	IOH (at VOH) mA	IOL (at VOL) mA	Notes
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank	Min.	Max.			
2 mA	2 mA	2 mA	VDDI * 0.75	VDDI * 0.25	2	2	
4 mA	4 mA	4 mA	VDDI * 0.75	VDDI * 0.25	4	4	
N/A	N/A	6 mA	VDDI * 0.75	VDDI * 0.25	6	6	

Note: For a detailed I/V curve, use the corresponding IBIS models: www.microsemi.com/soc/download/ibis/default.aspx.

AC Switching Characteristics

Worst Commercial-Case Conditions: $T_j = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 1.14\text{ V}$

AC Switching Characteristics for Receiver (Input Buffers)

Table 37 • LVCMOS 1.2 V Receiver Characteristics

	On-Die Termination (ODT)	t_{PY}		t_{PYS}		Units
		-1	Std.	-1	Std.	
LVCMOS 1.2 V (for DDRIO I/O bank)	None	2.265	2.664	2.278	2.68	ns
	50	2.276	2.676	2.247	2.645	ns
	75	2.29	2.693	2.246	2.645	ns
	150	2.29	2.694	2.26	2.658	ns
LVCMOS 1.2 V (for MSIO I/O bank)	None	8.488	9.985	8.481	9.977	ns
	50	TBD	TBD	TBD	TBD	ns
	75	TBD	TBD	TBD	TBD	ns
	150	TBD	TBD	TBD	TBD	ns
LVCMOS 1.2 V (for MSIOD I/O bank)	None	8.141	9.578	8.145	9.583	ns
	50	TBD	TBD	TBD	TBD	ns
	75	TBD	TBD	TBD	TBD	ns
	150	TBD	TBD	TBD	TBD	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 38 • LVCMOS 1.2 V Transmitter Characteristics

Output Drive Selection	Slew Control	t_{DP}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		Units
		-1	Std.	-1	Std.	-1	Std.	-1	Std.	-1	Std.	
LVCMOS 1.2 V (for DDRIO I/O bank)												
2 mA	Slow	5.812	6.837	6.017	7.078	5.867	6.902	6.529	7.68	5.794	6.816	ns
	Medium	5.146	6.054	5.702	6.707	5.215	6.134	6.214	7.309	5.495	6.464	ns
	Medium fast	4.813	5.662	5.554	6.533	4.886	5.747	6.066	7.135	5.357	6.302	ns
	Fast	4.778	5.621	5.541	6.518	4.851	5.707	6.053	7.12	5.347	6.29	ns
4 mA	Slow	5.29	6.223	6.654	7.828	5.834	6.863	7.166	8.43	6.346	7.465	ns
	Medium	4.658	5.479	6.348	7.468	5.522	6.496	6.86	8.07	6.034	7.098	ns
	Medium fast	4.333	5.098	6.185	7.277	5.387	6.338	6.697	7.879	5.899	6.94	ns
	Fast	4.298	5.056	6.175	7.265	5.378	6.327	6.687	7.867	5.89	6.929	ns
6 mA	Slow	5.095	5.994	6.925	8.147	6.048	7.115	7.437	8.749	6.56	7.717	ns
	Medium	4.499	5.293	6.619	7.787	5.738	6.75	7.131	8.389	6.25	7.352	ns
	Medium fast	4.19	4.929	6.473	7.615	5.607	6.596	6.985	8.217	6.119	7.198	ns
	Fast	4.155	4.888	6.464	7.605	5.599	6.587	6.976	8.207	6.111	7.189	ns
LVCMOS 1.2 V (for MSIO I/O bank)												
2 mA	Slow	6.723	7.909	9.734	11.451	8.636	10.16	9.599	11.292	8.501	10.001	ns
4 mA	Slow	7.045	8.288	10.848	12.762	9.283	10.921	10.713	12.603	9.148	10.762	ns



SmartFusion2 DC and Switching Characteristics

Table 38 • LVCMOS 1.2 V Transmitter Characteristics (continued)

Output Drive Selection	Slew Control	t_{DP}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		Units
		-1	Std.	-1	Std.	-1	Std.	-1	Std.	-1	Std.	
LVCMOS 1.2 V (for MSIOD I/O bank)												
2 mA	Slow	3.866	4.549	7.988	9.397	7.523	8.85	8.055	9.476	7.59	8.929	ns
4 mA	Slow	3.755	4.41	8.93	10.505	8.277	9.737	8.997	10.584	8.344	9.816	ns

3.3 V PCI/PCIX

Peripheral Component Interface (PCI) for 3.3 V standards specify support for 33 MHz and 66 MHz PCI bus applications.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 39 • PCI/PCI-X DC Voltage Specification – Applicable to MSIO Bank ONLY

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
PCI/PCIX Recommended DC Operating Conditions							
VDDI	Supply voltage		3.15	3.3	3.45	V	
PCI/PCIX DC Input Voltage Specification							
VI	DC input voltage		0	–	3.45	V	
I _{IH} (DC)	Input current High		–	–	10	μA	
I _{IL} (DC)	Input current Low		–	–	10	μA	
PCI/PCIX DC Output Voltage Specification							
VOH	DC output logic High		Per PCI Specification			V	
VOL	DC output logic Low		Per PCI Specification			V	

Table 40 • PCI/PCI-X Minimum and Maximum AC Input and Output Levels – Applicable to MSIO Bank ONLY

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
PCI/PCI-X AC Specifications							
F _{max}	Maximum data rate (MSIO I/O bank)	AC Loading: per JEDEC specifications	–	–	630	Mbps	
PCI/PCI-X AC Test Parameters Specifications							
V _{trip}	Measuring/trip point for data path (falling edge)		–	0.615 * VDDI	–	V	
V _{trip}	Measuring/trip point for data path (rising edge)		–	0.285 * VDDI	–	V	
R _{tt_test}	Resistance for data test path		–	25	–	Ohms	
R _{ent}	Resistance for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		–	2K	–	Ohms	
C _{ent}	Capacitive loading for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		–	5	–	pF	



SmartFusion2 DC and Switching Characteristics

AC Switching Characteristics

Worst Commercial-Case Conditions: $T_j = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 3.0\text{ V}$

AC Switching Characteristics for Receiver (Input Buffers)

Table 41 • AC Switching Characteristics for Receiver (Input Buffers)

	On-Die Termination (ODT)	t_{PY}		t_{PYS}		Units
		-1	Std.	-1	Std.	
PCI/PCIX (for MSIO I/O bank)	None	2.29	2.694	2.296	2.701	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 42 • AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

	t_{DP}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		Units
	-1	Std.	-1	Std.	-1	Std.	-1	Std.	-1	Std.	
PCI/PCIX (for MSIO I/O bank)											
	2.146	2.525	2.269	2.67	2.312	2.72	6.171	7.259	5.64	6.634	ns

Memory Interface and Voltage Referenced I/O Standards

High-Speed Transceiver Logic (HSTL)

The High-Speed Transceiver Logic (HSTL) standard is a general purpose high-speed bus standard sponsored by IBM (EIA/JESD8-6). SmartFusion2 devices support two classes of the 1.5 V HSTL. These differential versions of the standard require a differential amplifier input buffer and a push-pull output buffer.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 43 • HSTL DC Voltage Specification

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		1.425	1.5	1.575	V	
VTT	Termination voltage		0.698	0.750	0.803	V	
VREF	Input reference voltage		0.698	0.750	0.803	V	
HSTL DC Input Voltage Specification							
VIH (DC)	DC input logic High		VREF + 0.1	–	1.575	V	
VIL (DC)	DC input logic Low		–0.3	–	VREF – 0.1	V	
IIH (DC)	Input current High		–	–	10	V	
IIL (DC)	Input current Low		–	–	10	V	
HSTL DC Output Voltage Specification							
HSTL Class I							
VOH	DC output logic High		VDDI – 0.4	–	–	V	
VOL	DC output logic Low		–	–	0.4	V	
IOH at VOH	Output minimum source DC current (MSIOD I/O bank)		–7.8	–	–	mA	1
IOL at VOL	Output minimum sink current (MSIOD I/O bank)		7.8	–	–	mA	1
IOH at VOH	Output minimum source DC current (MSIO and DDRIO I/O banks)		–8.0	–	–	mA	
IOL at VOL	Output minimum sink current (MSIO and DDRIO I/O banks)		8.0	–	–	mA	
HSTL Class II (Applicable to MSIO and DDRIO I/O Bank Only)							
VOH	DC output logic High		VDDI – 0.4	–	–	V	
VOL	DC output logic Low		–	–	0.4	V	
IOH at VOH	Output minimum source DC current		–16.0	–	–	mA	
IOL at VOL	Output minimum sink current		16.0	–	–	mA	
HSTL DC Differential Voltage Specifications							
VID (DC)	DC input differential voltage		0.2	–	–	V	

Notes:

1. MSIOD I/O bank HSTL Class I does not meet standard JEDEC test point. Use provided lower current values as specified.



Table 44 • HSTL Minimum and Maximum AC Input and Output Levels

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
HSTL AC Differential Voltage Specifications							
VDIFF (AC)	AC input differential voltage		0.4	–	–	V	
Vx (AC)	AC differential cross point voltage		0.68	–	0.9	V	
HSTL AC Specifications							
Fmax	Maximum data rate (DDRIO I/O bank)	AC loading: per JEDEC specifications	–	–	800	Mbps	
Fmax	Maximum data rate (for MSIO I/O bank)	AC loading: 3 pF / 50 Ohm load	–	–	140	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank)	AC loading: 3 pF / 50 Ohm load	–	–	180	Mbps	
Rref	Supported output driver calibrated impedance (for DDRIO I/O bank)	Reference resistance = 191 Ohms	–	25.5, 47.8	–	Ohms	
RTT	Effective impedance value (with respect to reference resistor of 191 Ohms) (ODT for DDRIO I/O bank only)	Reference resistance = 191 Ohms	–	47.8	–	Ohms	
RTT	Effective impedance value (ODT for MSIO and MSIOD I/O banks only)	Reference resistance = 191 Ohms	–	50, 75, 150	–	Ohms	
HSTL AC Test Parameters Specification							
Vtrip	Measuring/trip point for data path		–	0.75	–	V	
Rent	Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	5	–	pF	
Rtt_test	Reference resistance for data test path for SSTL15 Class I (t_{DP})		–	50	–	Ohms	
Rtt_test	Reference resistance for data test path for SSTL15 Class II (t_{DP})		–	25	–	Ohms	
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF	

AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 45 • HSTL Receiver Characteristics

	On-Die Termination (ODT)	t _{py}		Units
		-1	Std.	
HSTL (for DDRIO I/O bank)				
Pseudo differential	None	1.678	1.975	ns
	47.8	1.684	1.983	ns
True differential	None	1.712	2.015	ns
	47.8	1.723	2.027	ns
HSTL (for MSIO I/O bank)				
Pseudo differential	None	7.898	9.292	ns
	50	7.958	9.362	ns
	75	7.928	9.327	ns
	150	7.906	9.301	ns
True differential	None	8.366	9.842	ns
	50	8.25	9.705	ns
	75	8.27	9.728	ns
	150	8.339	9.809	ns
HSTL (for MSIOD I/O bank)				
Pseudo differential	None	7.081	8.331	ns
	50	7.096	8.348	ns
	75	7.098	8.351	ns
	150	7.055	8.3	ns
True differential	None	7.282	8.566	ns
	50	7.198	8.468	ns
	75	7.223	8.497	ns
	150	7.245	8.523	ns



AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 46 • HSTL Transmitter Characteristics

	t_{DP}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		Units
	-1	Std.	-1	Std.	-1	Std.	-1	Std.	-1	Std.	
HSTL Class I											
For DDRIO I/O Bank											
Single-ended	2.767	3.255	2.568	3.022	2.568	3.022	2.58	3.036	2.58	3.036	ns
Differential	2.601	3.059	3.002	3.531	3	3.53	3.014	3.545	3.012	3.544	ns
For MSIO I/O Bank											
Single-ended	4.171	4.906	3.433	4.04	3.404	4.005	3.378	3.975	3.349	3.94	ns
Differential	3.983	4.686	4.057	4.773	4.048	4.762	4.005	4.712	3.996	4.701	ns
For MSIOD I/O Bank											
Single-ended	2.421	2.849	2.285	2.689	2.263	2.663	2.342	2.755	2.32	2.729	ns
Differential	2.381	2.802	2.638	3.103	2.624	3.087	2.694	3.169	2.68	3.153	ns
HSTL Class II											
For DDRIO I/O Bank											
Single-ended	2.597	3.056	2.537	2.985	2.537	2.985	2.549	2.999	2.549	2.999	ns
Differential	2.51	2.952	2.975	3.5	2.972	3.497	2.987	3.514	2.984	3.511	ns

Stub-Series Terminated Logic

Stub-Series Terminated Logic (SSTL) for 2.5 V (SSTL2), 1.8 V (SSTL18), and 1.5 V (SSTL15) is supported in SmartFusion2 devices. SSTL2 is defined by JEDEC standard JESD8-9B and SSTL18 is defined by JEDEC standard JESD8-15. SmartFusion2 SSTL I/O configurations are designed to meet double data rate standards DDR/2/3 for general purpose memory buses. Double data rate standards are designed to meet their JEDEC specifications as defined by JEDEC standard JESD79F for DDR, JEDEC standard JESD79-2F for DDR, JEDEC standard JESD79-3D for DDR3, and JEDEC standard JESD209A for LPDDR.

Stub-Series Terminated Logic 2.5 V (SSTL2)

SSTL2 Class I and Class II are supported in SmartFusion2 devices and also comply with reduced and full drive of double data rate (DDR) standards. SmartFusion2 FPGA I/O supports both standards for single-ended signaling and differential signaling for SSTL2. This standard requires a differential amplifier input buffer and a push-pull output buffer.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 47 • DDR1/SSTL2 DC Voltage Specification

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		2.375	2.5	2.625	V	
VTT	Termination voltage		1.164	1.250	1.339	V	
VREF	Input reference voltage		1.164	1.250	1.339	V	
DDR/SSTL2 DC Input Voltage Specification							
VIH (DC)	DC input logic High	VREF + 0.15		–	2.625	V	
VIL (DC)	DC input logic Low		–0.3	–	VREF – 0.15	V	
IIH (DC)	Input current High		–	–	10	μA	
IIL (DC)	Input current Lo		–	–	10	μA	
DDR/SSTL2 DC Output Voltage Specification							
SSTL2 Class I (DDR Reduced Drive)							
VOH	DC output logic High	VTT + 0.608		–	–	V	
VOL	DC output logic Low		–	–	VTT – 0.608	V	
IOH at VOH	Output minimum source DC current		8.1	–	–	mA	
IOL at VOL	Output minimum sink current		–8.1	–	–	mA	
SSTL2 Class II (DDR Full Drive) – Applicable to MSIO and DDRIO I/O Banks ONLY							
VOH	DC output logic High	VTT + 0.81		–	–	V	
VOL	DC output logic Low		–	–	VTT – 0.81	V	
IOH at VOH	Output minimum source DC current		16.2	–	–	mA	
IOL at VOL	Output minimum sink current		–16.2	–	–	mA	
SSTL2 DC Differential Voltage Specification							
VID (DC)	DC input differential voltage		0.3	–	–	V	



Table 48 • DDR1/SSTL2 Minimum and Maximum AC Input and Output Levels

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
SSTL2 AC Differential Voltage Specification							
V _{DIFF} (AC)	AC input differential voltage		0.7	–	–	V	
V _x (AC)	AC differential cross point voltage		0.5 * V _{DDI} – 0.2	–	0.5 * V _{DDI} + 0.2	V	
SSTL2 AC Specifications							
F _{max}	Maximum data rate (for DDRIO I/O bank)	AC loading: per JEDEC specifications	–	–	400	Mbps	
F _{max}	Maximum data rate (for MSIO I/O bank)	AC loading: 10 pF / 50 Ohm load	–	–	575	Mbps	
F _{max}	Maximum data rate (for MSIOD I/O bank)	AC loading: 30 pF / 50 Ohm load	–	–	700	Mbps	
R _{ref}	Supported output driver calibrated impedance (for DDRIO I/O bank)	Reference resistor = 150 Ohms	–	20, 42	–	Ohms	
AC Test Parameters Specifications							
V _{trip}	Measuring/trip point for data path		–	1.25	–	V	
R _{ent}	Resistance for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		–	2K	–	Ohms	
C _{ent}	Capacitive loading for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		–	5	–	pF	
R _s	Series resistance for data test path (t _{DP})		–	25	–	Ohms	
R _{tt_test}	Reference resistance for data test path for SSTL2 Class I (t _{DP})		–	50	–	Ohms	
R _{tt_test}	Reference resistance for data test path for SSTL2 Class II (t _{DP})		–	25	–	Ohms	
C _{load}	Capacitive loading for data path (t _{DP})		–	5	–	pF	

AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, V_{DD} = 1.14 V, V_{DDI} = 2.375 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 49 • DDR1/SSTL2 Receiver Characteristics

	On-Die Termination (ODT)	t _{py}		Units
		–1	Std.	
SSTL2 (for DDRIO I/O bank)				
Pseudo differential	None	1.624	1.911	ns
True differential	None	1.661	1.953	ns
SSTL2 (for MSIO I/O bank)				
Pseudo differential	None	2.899	3.411	ns
True differential	None	2.773	3.263	ns
SSTL2 (for MSIOD I/O bank)				
Pseudo differential	None	2.553	3.004	ns
True differential	None	2.527	2.973	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 50 • DDR1/SSTL2 Transmitter Characteristics

	t_{DP}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		Units
	-1	STD	-1	STD	-1	STD	-1	STD	-1	STD	
SSTL2 Class I											
For DDRIO I/O Bank											
Single-ended	2.533	2.979	2.179	2.564	2.174	2.558	2.226	2.619	2.221	2.613	ns
Differential	2.25	2.648	2.449	2.881	2.446	2.878	2.496	2.936	2.493	2.933	ns
For MSIO I/O Bank											
Single-ended	2.037	2.398	2.103	2.474	2.097	2.466	2.159	2.54	2.153	2.532	ns
Differential	2.215	2.606	2.461	2.895	2.454	2.887	2.522	2.967	2.515	2.959	ns
For MSIOD I/O Bank											
Single-ended	1.606	1.889	1.663	1.957	1.664	1.959	1.764	2.075	1.765	2.077	ns
Differential	1.743	2.05	1.848	2.173	1.837	2.16	1.948	2.291	1.937	2.278	ns
SSTL2 Class II											
For DDRIO I/O Bank											
Single-ended	2.208	2.597	2.098	2.469	2.096	2.466	2.145	2.524	2.143	2.521	ns
Differential	2.115	2.489	2.415	2.842	2.415	2.842	2.462	2.897	2.462	2.897	ns
For MSIO I/O Bank											
Single-ended	2.274	2.676	2.027	2.384	2.02	2.375	2.083	2.45	2.076	2.441	ns
Differential	2.443	2.874	2.333	2.745	2.327	2.737	2.394	2.817	2.388	2.809	ns



Stub-Series Terminated Logic 1.8 V (SSTL18)

SSTL18 Class I and Class II are supported in SmartFusion2 devices, and also comply with the reduced and full drive double data rate (DDR2) standard. SmartFusion2 FPGA I/Os support both standards for single-ended signaling and differential signaling for SSTL18. This standard requires a differential amplifier input buffer and a push-pull output buffer.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 51 • SSTL18 DC Voltage Specification

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		1.71	1.8	1.89	V	
VTT	Termination voltage		0.838	0.900	0.964	V	
VREF	Input reference voltage		0.838	0.900	0.964	V	
SSTL18 DC Input Voltage Specification							
VIH (DC)	DC input logic High	VREF + 0.125	–	–	1.89	V	
VIL (DC)	DC input logic Low		–0.3	–	VREF – 0.125	V	
IIH (DC)	Input current High		–	–	10	μA	
IIL (DC)	Input current Low		–	–	10	μA	
SSTL18 DC Output Voltage Specification							
SSTL18 Class I (DDR2 Reduced Drive)							
VOH	DC output logic High	VTT + 0.603	–	–	–	V	
VOL	DC output logic Low		–	–	VTT – 0.603	V	
IOH at VOH	Output minimum source DC current (MSIO I/O bank only)		4.7	–	–	mA	1
IOL at VOL	Output minimum sink current (MSIO I/O bank only)		–4.7	–	–	mA	1
IOH at VOH	Output minimum source DC current (MSIOD I/O bank only)		6.3	–	–	mA	1
IOL at VOL	Output minimum sink current (MSIOD I/O bank only)		–6.3	–	–	mA	1
IOH at VOH	Output minimum source DC current (DDRIO I/O bank only)		6.5	–	–	mA	1
IOL at VOL	Output minimum sink current (DDRIO I/O bank only)		–6.5	–	–	mA	1

Notes:

1. MSIO I/O bank SSTL18/DDR2 reduced drive does not have a standard test point. This is defined to fit within the DDR2 reduced drive I/V curve minimums.
2. MSIO I/O bank SSTL18/DDR2 Class II does not meet the standard JEDEC test points. Use provided lower current values as specified.

Table 51 • SSTL18 DC Voltage Specification (continued)

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
STL18 Class II (DDR2 Full Drive) – Applicable to MSIO and DDRIO I/O Banks ONLY							
VOH	DC output logic High		VTT + 0.603	–	–	V	
VOL	DC output logic Low		–	–	VTT– 0.603	V	
IOH at VOH	Output minimum source DC current (MSIO I/O bank only)		9.3	–	–	mA	
IOL at VOL	Output minimum sink current (MSIO I/O bank only)		–9.3	–	–	mA	
IOH at VOH	Output minimum source DC current (DDRIO I/O bank only)		13.4	–	–	mA	
IOL at VOL	Output minimum sink current (DDRIO I/O bank only)		–13.4	–	–	mA	
SSTL18 DC Differential Voltage Specification							
VID (DC)	DC input differential voltage		0.3	–	–	V	

Notes:

1. MSIO I/O bank SSTL18/DDR2 reduced drive does not have a standard test point. This is defined to fit within the DDR2 reduced drive I/V curve minimums.
2. MSIO I/O bank SSTL18/DDR2 Class II does not meet the standard JEDEC test points. Use provided lower current values as specified.



Table 52 • SSTL18 Minimum and Maximum AC Input and Output Levels

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
SSTL18 AC Differential Voltage Specification							
V _{DIFF} (AC)	AC input differential voltage		0.7			V	
V _x (AC)	AC differential cross point voltage		0.5 * V _{DDI} - 0.175	-	0.5 * V _{DDI} + 0.175	V	
SSTL18 AC Specification							
F _{max}	Maximum data rate (for DDRIO I/O bank)	AC loading: per JEDEC specification	-	-	800	Mbps	
F _{max}	Maximum data rate (for MSIO I/O bank)	AC loading: 3 pF / 25 Ohm load	-	-	432	Mbps	
F _{max}	Maximum data rate (for MSIOD I/O bank)	AC loading: 3 pF / 25 Ohm load	-	-	430	Mbps	
R _{ref}	Supported output driver calibrated impedance (for DDRIO I/O bank)	Reference resistor = 150 Ohms	-	20, 42		Ohms	
R _{TT}	Effective impedance value (with respect to reference resistor 150 Ohms) (ODT for DDRIO I/O bank only)	Reference resistor = 150 Ohms	-	50, 75, 150		Ohms	
AC Test Parameters Specifications							
V _{trip}	Measuring/trip point for data path		-	0.9	-	V	
R _{ent}	Resistance for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		-	2K	-	Ohms	
C _{ent}	Capacitive loading for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		-	5	-	pF	
R _s	Series resistance for data test path (t _{DP})		-	25	-	Ohms	
R _{tt_test}	Reference resistance for data test path for SSTL18 Class I (t _{DP})		-	50	-	Ohms	
R _{tt_test}	Reference resistance for data test path for SSTL18 Class II (t _{DP})		-	25	-	Ohms	
C _{load}	Capacitive loading for data path (t _{DP})		-	5	-	pF	

AC Switching Characteristics

Worst Commercial-Case Conditions: $T_j = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 1.71\text{ V}$

AC Switching Characteristics for Receiver (Input Buffers)

Table 53 • DDR2/SSTL18 Receiver Characteristics

	On-Die Termination (ODT)	t_{py}		Units
		-1	STD	
SSTL18 (for DDRIO I/O bank)				
Pseudo differential	None	1.64	1.929	ns
	50	1.644	1.935	ns
	75	1.645	1.936	ns
	150	1.643	1.934	ns
True differential	None	1.7	2	ns
	50	1.708	2.009	ns
	75	1.702	2.003	ns
	150	1.703	2.003	ns
SSTL18 (for MSIO I/O bank)				
Pseudo differential	None	4.432	5.215	ns
	50	3.785	4.453	ns
	75	3.995	4.701	ns
	150	4.217	4.962	ns
True differential	None	4.491	5.283	ns
	50	4.443	5.227	ns
	75	4.451	5.236	ns
	150	4.47	5.258	ns
SSTL18 (for MSIOD I/O bank)				
Pseudo differential	None	3.745	4.405	ns
	50	3.743	4.404	ns
	75	3.737	4.397	ns
	150	3.733	4.391	ns
True differential	None	3.96	4.659	ns
	50	3.947	4.643	ns
	75	3.945	4.641	ns
	150	3.958	4.656	ns



AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 54 • DDR2/SSTL18 Transmitter Characteristics

	t_{DP}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		Units
	-1	STD	-1	STD	-1	STD	-1	STD	-1	STD	
SSTL18 Class I											
For DDRIO I/O Bank											
Single-ended	2.506	2.948	2.287	2.69	2.284	2.687	2.318	2.727	2.315	2.724	ns
Differential	2.374	2.793	2.812	3.309	2.811	3.307	2.839	3.341	2.838	3.339	ns
For MSIO I/O Bank											
Single-ended	3.084	3.629	2.789	3.28	2.777	3.266	2.77	3.258	2.758	3.244	ns
Differential	2.832	3.332	3.331	3.918	3.324	3.91	3.313	3.898	3.306	3.89	ns
For MSIOD I/O Bank											
Single-ended	1.991	2.342	1.955	2.299	1.952	2.296	2.02	2.376	2.017	2.373	ns
Differential	2.039	2.4	2.203	2.592	2.195	2.582	2.269	2.669	2.261	2.659	ns
SSTL18 Class II											
For DDRIO I/O Bank											
Single-ended	2.334	2.746	2.251	2.648	2.245	2.641	2.282	2.685	2.276	2.678	ns
Differential	2.275	2.676	2.716	3.196	2.712	3.191	2.743	3.228	2.739	3.223	ns
For MSIO I/O Bank											
Single-ended	3.298	3.88	2.71	3.189	2.693	3.168	2.691	3.167	2.674	3.146	ns
Differential	3.184	3.746	3.172	3.731	3.163	3.721	3.154	3.711	3.145	3.701	ns

Stub-Series Terminated Logic 1.5 V (SSTL15)

SSTL15 Class I and Class II are supported in SmartFusion2 devices, and also comply with the reduced and full drive double data rate (DDR3) standard. SmartFusion2 FPGA I/O supports both standards for single-ended signaling and differential signaling for SSTL18. This standard requires a differential amplifier input buffer and a push-pull output buffer.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 55 • SSTL15 DC Voltage Specification (for DDRIO I/O Bank Only)

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		1.425	1.5	1.575	V	
VTT	Termination voltage		0.698	0.750	0.803	V	
VREF	Input reference voltage		0.698	0.750	0.803	V	
SSTL15 DC Input Voltage Specification							
VIH(DC)	DC input logic High	VREF + 0.1		–	1.575	V	
VIL(DC)	DC input logic Low		–0.3	–	VREF – 0.1	V	
IIH (DC)	Input current High		–	–	10	μA	
IIL (DC)	Input current Low		–	–	10	μA	
SSTL15 DC Output Voltage Specification							
DDR3/SSTL15 Class I (DDR3 Reduced Drive)							
VOH	DC output logic High		0.8 * VDDI	–	–	V	
VOL	DC output logic Low		–	–	0.2 * VDDI	V	
IOH at VOH	Output minimum source DC current		6.5	–	–	mA	
IOL at VOL	Output minimum sink current		–6.5	–	–	mA	
SSTL15 Class II (DDR3 Full Drive)							
VOH	DC output logic High		0.8 * VDDI	–	–	V	
VOL	DC output logic Low		–	–	0.2 * VDDI	V	
IOH at VOH	Output minimum source DC current		7.6	–	–	mA	
IOL at VOL	Output minimum sink current		–7.6	–	–	mA	
SSTL15 Differential Voltage Specification							
VID (DC)	DC input differential voltage		0.2	–	–	V	



Table 56 • SSTL15 Minimum and Maximum AC Input and Output Levels (for DDRIO I/O Bank Only)

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
SSTL15 Differential Voltage Specification							
V _{DIFF} (AC)	AC input differential voltage		0.7	–	–	V	
V _x (AC)	AC differential cross point voltage		0.5 * V _{DDI} – 0.150	–	0.5 * V _{DDI} + 0.150	V	
SSTL15 AC Specification							
F _{max}	Maximum data rate (for DDRIO I/O bank)	AC loading: per JEDEC specifications			800	Mbps	
R _{ref}	Supported output driver calibrated impedance	Reference resistor = 240 Ohms		34, 40		Ohms	
R _{TT}	Effective impedance value (with respect to reference resistor 240 ohms) (ODT for DDRIO I/O bank only)	Reference resistor = 240 Ohms		20, 30, 40, 60, 120		Ohms	
AC Test Parameters Specifications							
V _{trip}	Measuring/trip point for data path		–	0.75	–	V	
R _{ent}	Resistance for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		–	2K	–	Ohms	
C _{ent}	Capacitive loading for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		–	5	–	pF	
R _s	Series resistance for data test path (t _{DP})		–	25	–	Ohms	
R _{tt_test}	Reference resistance for data test path for SSTL15 Class I (t _{DP})		–	50	–	Ohms	
R _{tt_test}	Reference resistance for data test path for SSTL15 Class II (t _{DP})		–	25	–	Ohms	
C _{load}	Capacitive loading for data path (t _{DP})		–	5	–	pF	

AC Switching Characteristics

Worst Commercial-Case Conditions: $T_j = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 1.425\text{ V}$

AC Switching Characteristics for Receiver (Input Buffers)

Table 57 • SSTL15 Receiver Characteristics

	On-Die Termination (ODT)	t_{py}		Units
		-1	Std.	
DDR3/SSTL15 (for DDRIO I/O bank)				
Pseudo differential	None	1.676	1.972	ns
	20	1.689	1.988	ns
	30	1.689	1.987	ns
	40	1.681	1.977	ns
	60	1.685	1.983	ns
	120	1.685	1.983	ns
True differential	None	1.726	2.031	ns
	20	1.742	2.049	ns
	30	1.735	2.041	ns
	40	1.735	2.04	ns
	60	1.733	2.039	ns
	120	1.725	2.029	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 58 • DDR3/SSTL15 Transmitter Characteristics

	t_{DP}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		Units
	-1	STD	-1	STD	-1	STD	-1	STD	-1	STD	
DDR3 Reduced Drive/SSTL15 Class I											
For DDRIO I/O Bank											
Single-ended	2.786	3.278	2.574	3.027	2.577	3.031	2.585	3.04	2.588	3.044	ns
Differential	2.533	2.98	3.123	3.674	3.122	3.672	3.132	3.685	3.131	3.683	ns
DDR3 Full Drive/SSTL15 Class II											
For DDRIO I/O Bank											
Single-ended	2.74	3.223	2.566	3.018	2.569	3.022	2.577	3.031	2.58	3.035	ns
Differential	2.531	2.978	2.961	3.484	2.959	3.482	2.97	3.494	2.968	3.492	ns



Low Power Double Data Rate (LPDDR)

LPDDR reduced and full drive low power double data rate standards are supported in SmartFusion2 FPGA I/Os. This standard requires a differential amplifier input buffer and a push-pull output buffer.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 59 • LPDDR DC Voltage Specification

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		1.71	1.8	1.89	V	
VTT	Termination voltage		0.838	0.900	0.964	V	
VREF	Input reference voltage		0.838	0.900	0.964	V	
LPDDR DC Input Voltage Specification							
VIH (DC)	DC input logic High		0.3 * VDDI	–	1.89	V	
VIL (DC)	DC input logic Low		–0.3	–	0.7 * VDDI	V	
IIH (DC)	Input current High		–	–	10	µA	
IIL (DC)	Input current Low		–	–	10	µA	
LPDDR DC Output Voltage Specification							
VOH	DC output logic High		0.9 * VDDI	–	–	V	
VOL	DC output logic Low		–	–	0.1 * VDDI	V	
IOH at VOH	Output minimum source DC current		0.1	–	–	mA	
IOL at VOL	Output minimum sink current		–0.1	–	–	mA	
LPDDR Differential Voltage Specification							
VID (DC)	DC input differential voltage		0.4 * VDDI	–	–	V	
VDIFF (AC)	AC input differential voltage		0.6 * VDDI			V	
Vx (AC)	AC differential cross point voltage		0.4 * VDDI	–	0.6 * VDDI	V	

Table 60 • LPDDR Minimum and Maximum AC Input and Output Levels

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
LPDDR AC Specifications							
Fmax	Maximum data rate	AC loading: per JEDEC specifications				Mbps	
Rref	Supported output driver calibrated impedance	Reference resistor = 150 Ohms		20, 42		Ohms	
Rtt	Effective impedance value – ODT	Reference resistor = 150 Ohms		50, 70, 150		Ohms	
AC Test Parameters Specifications							
Vtrip	Measuring/trip point for data path		–	0.9	–	V	
Rent	Resistance for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		–	5	–	pF	
Rs	Series resistance for data test path (t _{DP})		–	25	–	Ohms	
Rtt_test	Reference resistance for data test path for LPDDR (t _{DP})		–	50	–	Ohms	
Cload	Capacitive loading for data path (t _{DP})		–	5	–	Ohms	

AC Switching Characteristics

Table 61 • LPDDR Receiver Characteristics

	On-Die Termination (ODT)	t_{py}		Units
		-1	Std.	
LPDDR (for DDRIO I/O Bank)				
Pseudo differential	None	1.64	1.93	ns
	50	1.645	1.937	ns
	75	1.643	1.934	ns
	150	1.641	1.931	ns
True differential	None	1.7	2	ns
	50	1.708	2.009	ns
	75	1.703	2.003	ns
	150	1.702	2.003	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 62 • LPDDR Transmitter Characteristics

	t_{DP}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		Units
	-1	Std.	-1	Std.	-1	Std.	-1	Std.	-1	Std.	
LPDDR Reduced Drive											
For DDRIO I/O Bank											
Single-ended	2.506	2.948	2.293	2.697	2.289	2.693	2.324	2.734	2.32	2.73	ns
Differential	2.315	2.725	2.773	3.262	2.775	3.265	2.801	3.295	2.803	3.298	ns
LPDDR Full Drive											
For DDRIO I/O Bank											
Single-ended	2.334	2.746	2.249	2.645	2.243	2.639	2.28	2.682	2.274	2.676	ns
Differential	2.284	2.687	2.714	3.192	2.715	3.193	2.742	3.225	2.743	3.226	ns



Differential I/O Standards

Configuration of the I/O modules as a differential pair is handled by Microsemi SoC Products Group Libero software when the user instantiates a differential I/O macro in the design. Differential I/Os can also be used in conjunction with the embedded Input register (InReg), Output register (OutReg), Enable register (EnReg), and Double Data Rate registers (DDR).

LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard.

Minimum and Maximum Input and Output Levels

Table 63 • LVDS DC Voltage Specification

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage	2.5 V range	2.375	2.5	2.625	V	
VDDI	Supply voltage	3.3 V range	3.15	3.3	3.45	V	
LVDS DC Input Voltage Specification							
VI	DC Input voltage	2.5 V range	0	–	2.925	V	
VI	DC input voltage	3.3 V range	0	–	3.45	V	
IIH (DC)	Input current High		–	–	10	μA	
IIL (DC)	Input current Low		–	–	10	μA	
LVDS DC Output Voltage Specification							
VOH	DC output logic High		1.25	1.425	1.6	V	
VOL	DC output logic Low		0.9	1.075	1.25	V	
LVDS Differential Voltage Specification							
VOD	Differential output voltage swing		250	350	450	mV	
VOCM	Output common mode voltage		1.125	1.25	1.375	V	
VICM	Input common mode voltage		0.05	1.25	1.375	V	
VID	Input differential voltage		100	350	600	mV	

Table 64 • LVDS Minimum and Maximum AC Input and Output Levels

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Fmax	Maximum data rate (for MSIO I/O bank)	AC loading: 2 pF / 100 Ohm differential load	–	–	535	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank) – no pre-emphasis	AC loading: 2 pF / 100 Ohm differential load	–	–	700	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank) – minimum pre-emphasis	AC loading: 2 pF / 100 Ohm differential load	–	–	TBD	Mbps	
Fmax	Maximum data rate (for MSIOD I/O Bank) – medium pre-emphasis	AC loading: 2 pF / 100 Ohm differential load	–	–	TBD	Mbps	
Rt	Termination resistance		–	100	–	Ohms	
AC Test Parameters Specifications							
Vtrip	Measuring/trip point for data path		–	Cross point	–	V	
Rent	Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	5	–	pF	

LVDS25 AC Switching Characteristics

Worst Commercial-Case Conditions: $T_j = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

AC Switching Characteristics for Receiver (Input Buffers)

Table 65 • LVDS25 Receiver Characteristics

	On-Die Termination (ODT)	t_{PY}		Units
		-1	Std.	
LVDS (for MSIO I/O bank)	None	2.896	3.407	ns
	100	2.872	3.377	ns
LVDS (for MSIOD I/O bank)	None	2.645	3.112	ns
	100	2.62	3.083	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 66 • LVDS25 Transmitter Characteristics

	t_{DP}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		Units
	-1	Std.	-1	Std.	-1	Std.	-1	Std.	-1	Std.	
LVDS (for MSIO I/O bank)	2.155	2.534	2.443	2.873	2.434	2.863	2.504	2.946	2.495	2.936	ns
LVDS (for MSIOD I/O bank)											
No pre-emphasis	1.671	1.965	1.879	2.211	1.848	2.174	1.979	2.329	1.948	2.292	ns
Min. pre-emphasis	1.585	1.864	1.892	2.226	1.858	2.185	1.992	2.344	1.958	2.303	ns
Max. pre-emphasis	1.544	1.816	1.901	2.237	1.864	2.193	2.001	2.355	1.964	2.311	ns

LVDS33 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 67 • LVDS33 Receiver Characteristics

	On Die Termination (ODT)	t_{PY}		Units
		-1	Std.	
LVDS33 (for MSIO I/O bank)	None	2.863	3.368	ns
	100	2.811	3.306	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 68 • LVDS33 Transmitter Characteristics

	t_{DP}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		Units
	-1	Std.	-1	Std.	-1	Std.	-1	Std.	-1	Std.	
LVDS33 (for MSIO I/O bank)	0.963	1.132	1.086	1.277	1.086	1.277	1.147	1.35	1.147	1.35	ns



B-LVDS

Bus LVDS (B-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 69 • B-LVDS DC Voltage Specification

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		2.375	2.5	2.625	V	
Bus LVDS DC Input Voltage Specification							
VI	DC input voltage		0	–	2.925	V	
IIH (DC)	Input current High		–	–	10	µA	
IIL (DC)	Input current Low		–	–	10	µA	
Bus LVDS DC Output Voltage Specification (for MSIO I/O Bank ONLY)							
VOH	DC output logic High		1.25	1.425	1.6	V	
VOL	DC output logic Low		0.9	1.075	1.25	V	
Bus LVDS Differential Voltage Specification							
VOD	Differential output voltage swing (for MSIO I/O bank ONLY)		240	–	460	mV	
VOCM	Output common mode voltage (for MSIO I/O bank ONLY)		1.1	–	1.5	V	
VICM	Input common mode voltage		0.05	–	2.4 – VID/2	V	
VID	Input differential voltage		100	–	2 * VDDI	mV	

Table 70 • B-LVDS Minimum and Maximum AC Input and Output Levels

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Bus LVDS AC Specifications							
Fmax	Maximum data rate (for MSIO I/O bank)	AC loading: 2 pF / 100 Ohm differential load	–	–	500	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank, receiver ONLY)		–	–	–	Mbps	
Rt	Termination resistance		–	27	–	Ohms	
Bus LVDS AC Test Parameters Specifications							
Vtrip	Measuring/trip point for data path		–	Cross point	–	V	
Rent	Resistance for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		–	5	–	pF	

AC Switching Characteristics

Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

AC Switching Characteristics for Receiver (Input Buffers)

Table 71 • AC Switching Characteristics for Receiver (Input Buffers)

	On-Die Termination (ODT)	t_{PY}		Units
		-1	Std.	
Bus-LVDS (for MSIO I/O Bank)	None	2.863	3.368	ns
	100	2.811	3.306	ns
Bus-LVDS (for MSIOD I/O Bank)	None	2.591	3.048	ns
	100	2.552	3.003	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 72 • AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

	t_{DP}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		Units
	-1	Std.	-1	Std.	-1	Std.	-1	Std.	-1	Std.	
Bus-LVDS (for MSIO I/O Bank)	2.278	2.679	2.375	2.794	2.368	2.785	2.436	2.867	2.429	2.858	ns

M-LVDS

M-LVDS specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers.

Minimum and Maximum Input and Output Levels

Table 73 • M-LVDS DC Voltage Specification

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
M-LVDS Recommended DC Operating Conditions							
VDDI	Supply voltage		2.375	2.5	2.625	V	
M-LVDS DC Input Voltage Specification							
VI	DC input voltage		0	–	2.925	V	
I _{IH} (DC)	Input current High		–	–	10	μA	
I _{IL} (DC)	Input current Low		–	–	10	μA	
M-LVDS DC Output Voltage Specification (for MSIO I/O Bank ONLY)							
VOH	DC output logic High		1.25	1.425	1.6	V	
VOL	DC output logic Low		0.9	1.075	1.25	V	
M-LVDS Differential Voltage Specification							
VOD	Differential output voltage Swing (for MSIO I/O bank ONLY)		480	–	650	mV	
VOCM	Output common mode voltage (for MSIO I/O bank ONLY)		0.3	–	2.1	V	
VICM	Input common mode voltage		0.3	–	1.2	V	
VID	Input differential voltage		50	–	2400	mV	



Table 74 • M-LVDS Minimum and Maximum AC Input and Output Levels

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
M-LVDS AC Specifications							
Fmax	Maximum data rate (for MSIO I/O bank)	AC loading: 2 pF / 100 Ohm differential load	–	–	500	Mbps	
Rt	Termination resistance		–	50	–	Ohms	
M-LVDS AC Test Parameters Specifications							
VTrip	Measuring/trip point for data path		–	Cross point	–	V	
Rent	Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	5	–	pF	

AC Switching Characteristics

Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

AC Switching Characteristics for Receiver (Input Buffers)

Table 75 • AC Switching Characteristics for Receiver (Input Buffers)

	On-Die Termination (ODT)	t_{py}		Units
		–1	Std.	
M-LVDS (for MSIO I/O bank)	None	2.863	3.368	ns
	100	2.811	3.306	ns
M-LVDS (for MSIOD I/O bank)	None	2.591	3.048	ns
	100	2.552	3.003	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 76 • AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

	t_{DP}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		Units
	–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	
M-LVDS (for MSIO I/O bank)	2.278	2.679	2.375	2.794	2.368	2.785	2.436	2.867	2.429	2.858	ns

Mini-LVDS

Mini-LVDS is an unidirectional interface from the timing controller to the column drivers and is designed to the Texas Instruments Standard SLDA007A.

Mini-LVDS Minimum and Maximum Input and Output Levels

Table 77 • Mini-LVDS DC Voltage Specification

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		2.375	2.5	2.625	V	
Mini-LVDS DC Input Voltage Specification							
VI	DC Input voltage		0	–	2.925	V	
Mini-LVDS DC Output Voltage Specification							
VOH	DC output logic High		1.25	1.425	1.6	V	
VOL	DC output logic Low		0.9	1.075	1.25	V	
Mini-LVDS Differential Voltage Specification							
VOD	Differential output voltage swing		300	–	600	mV	
VOCM	Output common mode voltage		1	–	1.4	V	
VICM	Input common mode voltage		0.3	–	1.2	V	
VID	Input differential voltage		200	–	600	mV	

Table 78 • Mini-LVDS Minimum and Maximum AC Input and Output Levels

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Mini-LVDS AC Specifications							
Fmax	Maximum data rate (for MSIO I/O bank)	AC loading: 2 pF / 100 Ohm differential load	–	–	520	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank, No pre-emphasis)	AC loading: 2 pF / 100 Ohm differential load	–	–	700	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank) – Min. pre-emphasis	AC loading: 2 pF / 100 Ohm differential load	–	–	700	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank) – Med. pre-emphasis	AC loading: 2 pF / 100 Ohm differential load	–	–	TBD	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank) – Max. pre-emphasis	AC loading: 2 pF / 100 Ohm differential load	–	–	TBD	Mbps	
Rt	Termination resistance		50		150	Ohms	
Mini-LVDS AC Test Parameters Specifications							
VTrip	Measuring/trip point for data path		–	Cross point	–	V	
Rent	Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	5	–	pF	



AC Switching Characteristics

Worst Commercial-Case Conditions: $T_j = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

AC Switching Characteristics for Receiver (Input Buffers)

Table 79 • AC Switching Characteristics for Receiver (Input Buffers)

	On-Die Termination (ODT)	t_{PY}		Units
		-1	Std.	
Mini-LVDS (for MSIO I/O bank)	None	2.934	3.45	ns
	100	2.945	3.463	ns
Mini-LVDS (for MSIOD I/O bank)	None	2.683	3.157	ns
	100	2.728	3.209	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 80 • AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

	t_{DP}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		Units
	-1	Std.	-1	Std.	-1	Std.	-1	Std.	-1	Std.	
Mini-LVDS (for MSIO I/O bank)	2.12	2.493	2.335	2.746	2.329	2.739	2.396	2.819	2.39	2.812	ns
Mini-LVDS (for MSIOD I/O Bank)											
No pre-emphasis	1.681	1.977	1.601	1.884	1.592	1.872	1.701	2.002	1.692	1.99	ns
Min. pre-emphasis	1.671	1.965	1.882	2.214	1.849	2.175	1.982	2.332	1.949	2.293	ns
Med. pre-emphasis	1.585	1.864	1.889	2.222	1.854	2.181	1.989	2.34	1.954	2.299	ns
Max. pre-emphasis	1.544	1.816	1.898	2.233	1.861	2.189	1.998	2.351	1.961	2.307	ns

RSDS

Reduced Swing Differential Signaling (RSDS) is similar to an LVDS high-speed interface using differential signaling. RSDS has a similar implementation to LVDS devices and is only intended for point-to-point applications.

Minimum and Maximum Input and Output Levels

Table 81 • RSDS DC Voltage Specification

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		2.375	2.5	2.625	V	
RSDS DC Input Voltage Specification							
VI	DC input voltage		0	–	2.925	V	
RSDS DC Output Voltage Specification							
VOH	DC output logic High		1.25	1.425	1.6	V	
VOL	DC output logic Low		0.9	1.075	1.25	V	
RSDS Differential Voltage Specification							
VOD	Differential output voltage swing		100	–	600	mV	
VOCM	Output common mode voltage		0.5	–	1.5	V	
VICM	Input common mode voltage		0.3	–	1.5	V	
VID	Input differential voltage		100	–	2 * VDDI	mV	

Table 82 • RSDS Minimum and Maximum AC Input and Output Levels

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
RSDS AC Specifications							
Fmax	Maximum data rate (for MSIO I/O bank)	AC loading: 2 pF / 100 Ohm differential load	–	–	520	Mbps	
Fmax	Maximum data Rate (for MSIOD I/O banks, No pre-emphasis)	AC loading: 2 pF / 100 Ohm differential load	–	–	700	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank) – Min. pre-emphasis	AC loading: 2 pF / 100 Ohm differential load	–	–	700	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank) – Med. pre-emphasis	AC loading: 2 pF / 100 Ohm differential load	–	–	TBD	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank) – Max. pre-emphasis	AC loading: 2 pF / 100 Ohm differential load	–	–	TBD	Mbps	
Rt	Termination resistance			100		Ohms	
AC Test Parameters Specifications							
VTrip	Measuring/trip point for data path		–	Cross point	–	V	
Rent	Resistance for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		–	5	–	pF	



AC Switching Characteristics

Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

AC Switching Characteristics for Receiver (Input Buffers)

Table 83 • AC Switching Characteristics for Receiver (Input Buffers)

	On-Die Termination (ODT)	t_{PY}		Units
		-1	Std.	
RSDS (for MSIO I/O bank)	None	2.908	3.42	ns
	100	2.925	3.44	ns
RSDS (for MSIOD I/O bank)	None	2.641	3.108	ns
	100	2.69	3.166	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 84 • AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

	t_{DP}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		Units
	-1	Std.	-1	Std.	-1	Std.	-1	Std.	-1	Std.	
RSDS (for MSIO I/O bank)	2.12	2.493	2.335	2.746	2.329	2.74	2.396	2.819	2.39	2.813	ns
RSDS (for MSIOD I/O bank)											
No pre-emphasis	1.681	1.977	1.6	1.882	1.59	1.87	1.7	2	1.69	1.988	ns
Min. pre-emphasis	1.671	1.965	1.879	2.21	1.845	2.171	1.979	2.328	1.945	2.289	ns
Med. pre-emphasis	1.585	1.864	1.889	2.222	1.854	2.181	1.989	2.34	1.954	2.299	ns
Max. pre-emphasis	1.544	1.816	1.898	2.233	1.861	2.189	1.998	2.351	1.961	2.307	ns

LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Similar to LVDS, two pins are needed. It also requires external resistor termination. SmartFusion2 devices support only LVPECL receivers and do not support LVPECL transmitters.

Minimum and Maximum Input and Output Levels

Table 85 • LVPECL DC Voltage Specification – Applicable to MSIO I/O Banks Only

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		3.15	3.3	3.45	V	
LVPECL DC Input Voltage Specification							
VIH (DC)	DC input logic High		–	–	2.3	V	
VIL (DC)	DC input logic Low		1.6	–	–	V	
LVPECL Differential Voltage Specification							
VICM	Input common mode voltage		0.3		2.8	V	
VIDIFF	Input differential voltage		100	300	1,000	mV	

Table 86 • LVPECL Minimum and Maximum AC Input and Output Levels – Applicable to MSIO I/O Banks Only

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
LVPECL AC Specifications							
Fmax	Maximum data rate (for MSIO I/O bank)		–	–	900	Mbps	

AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 2.375 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 87 • LVPECL Receiver Characteristics

	On-Die Termination (ODT)	t _{py}		Units
		–1	Std.	
LVPECL (for MSIO I/O bank)	None	2.631	3.094	ns
	100	2.654	3.12	ns

I/O Register Specifications

Input Register

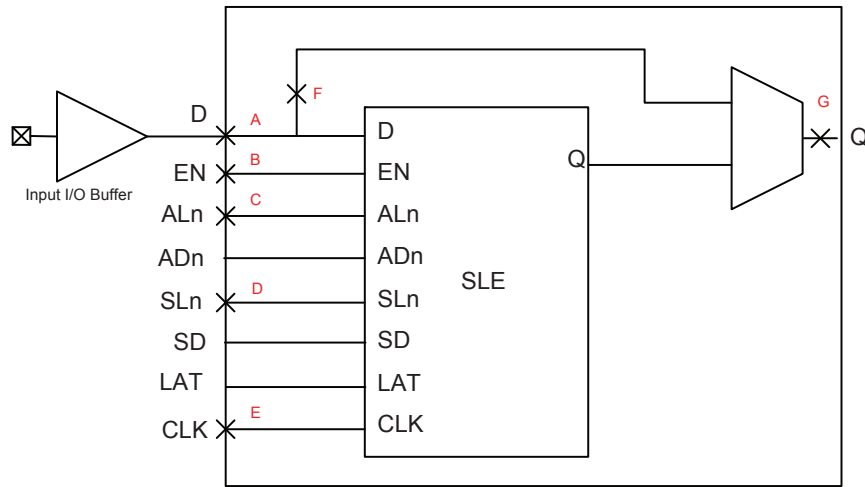


Figure 3 • Timing Model for Input Register

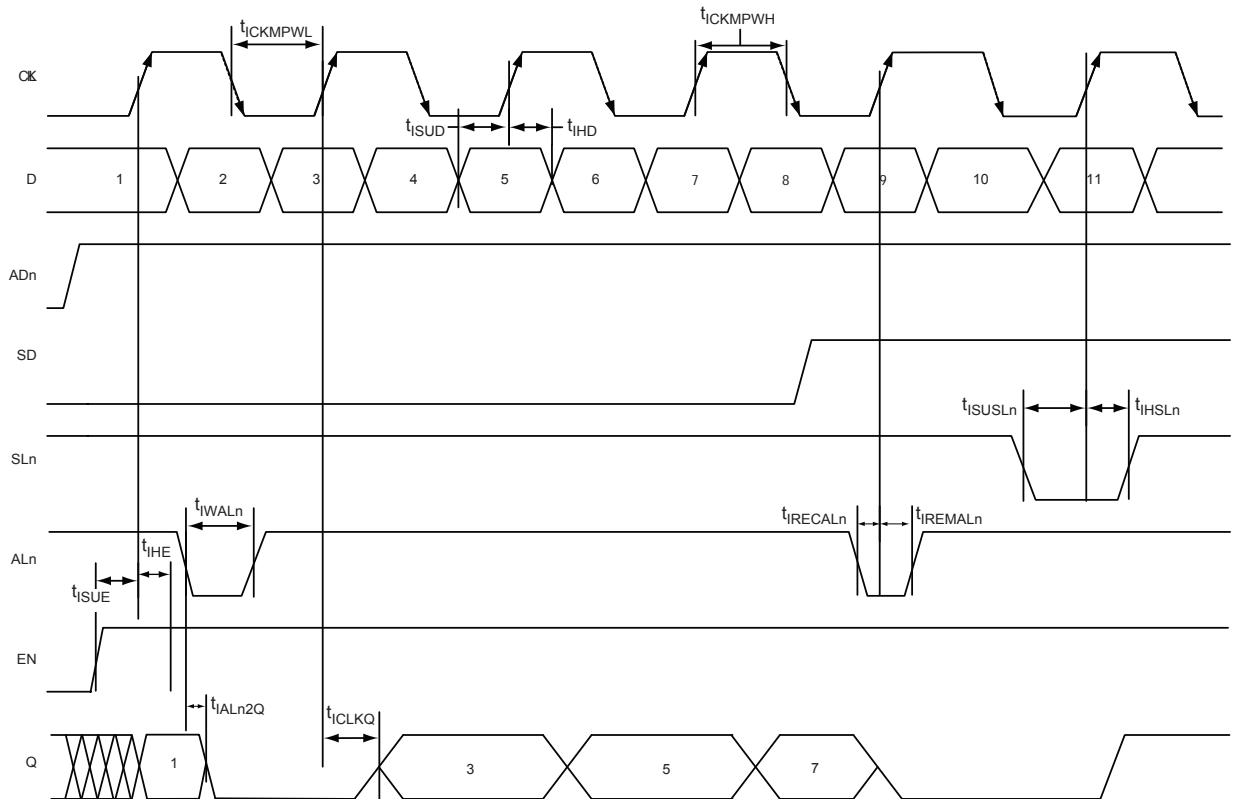


Figure 4 • I/O Register Input Timing Diagram

Table 88 • Input Data Enable Register Propagation Delays
Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Measuring Nodes (from, to)*	-1	Std.	Units
t_{BYP}	Bypass Delay of the Input Register	F, G	0.371	0.437	ns
t_{CLKQ}	Clock-to-Q of the Input Register	E, G	0.168	0.198	ns
t_{SUD}	Data Setup Time for the Input Register	A, E	0.376	0.443	ns
t_{IHD}	Data Hold Time for the Input Register	A, E	0	0	ns
t_{SUE}	Enable Setup Time for the Input Register	B, E	0.485	0.57	ns
t_{IHE}	Enable Hold Time for the Input Register	B, E	0	0	ns
t_{SUSL}	Synchronous Load Setup Time for the Input Register	D, E	0.485	0.57	ns
t_{IHSL}	Synchronous Load Hold Time for the Input Register	D, E	0	0	ns
t_{IALn2Q}	Asynchronous Clear-to-Q of the Input Register ($AD_n=1$)	C, G	0.658	0.774	ns
	Asynchronous Preset-to-Q of the Input Register ($AD_n=0$)	C, G	0.618	0.727	ns
t_{IREMAl_n}	Asynchronous Load Removal Time for the Input Register	C, E	0	0	ns
t_{IRECAL_n}	Asynchronous Load Recovery Time for the Input Register	C, E	0.078	0.091	ns
t_{IWAL_n}	Asynchronous Load Minimum Pulse Width for the Input Register	C, C	0.32	0.376	ns
t_{CKMPWH}	Clock Minimum Pulse Width High for the Input Register	E, E	0.079	0.093	ns
t_{CKMPWL}	Clock Minimum Pulse Width Low for the Input Register	E, E	0.168	0.197	ns

Note: *For the derating values at specific junction temperature and voltage supply levels, refer to [Table 7 on page 15](#) for derating values.

Output/Enable Register

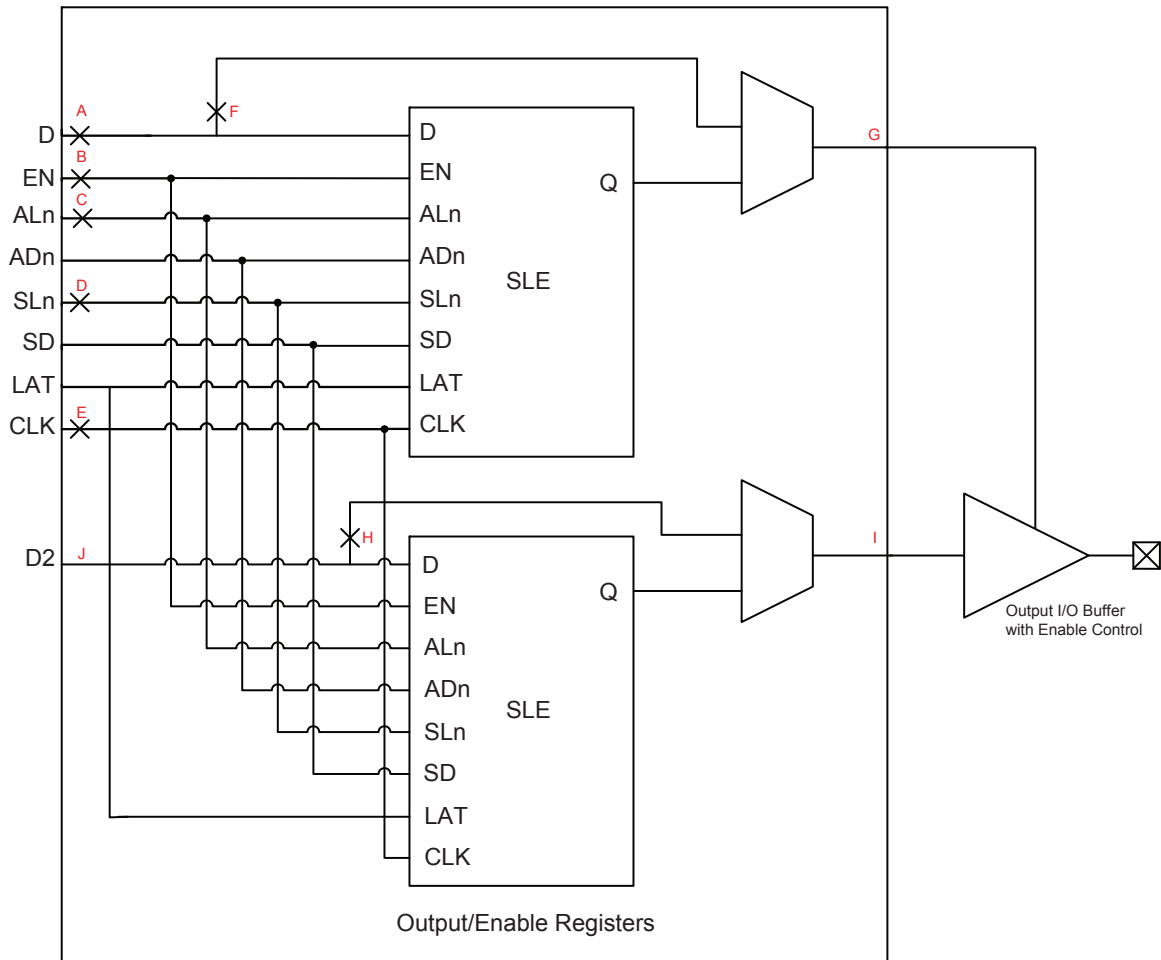


Figure 5 • Timing Model for Output/Enable Register

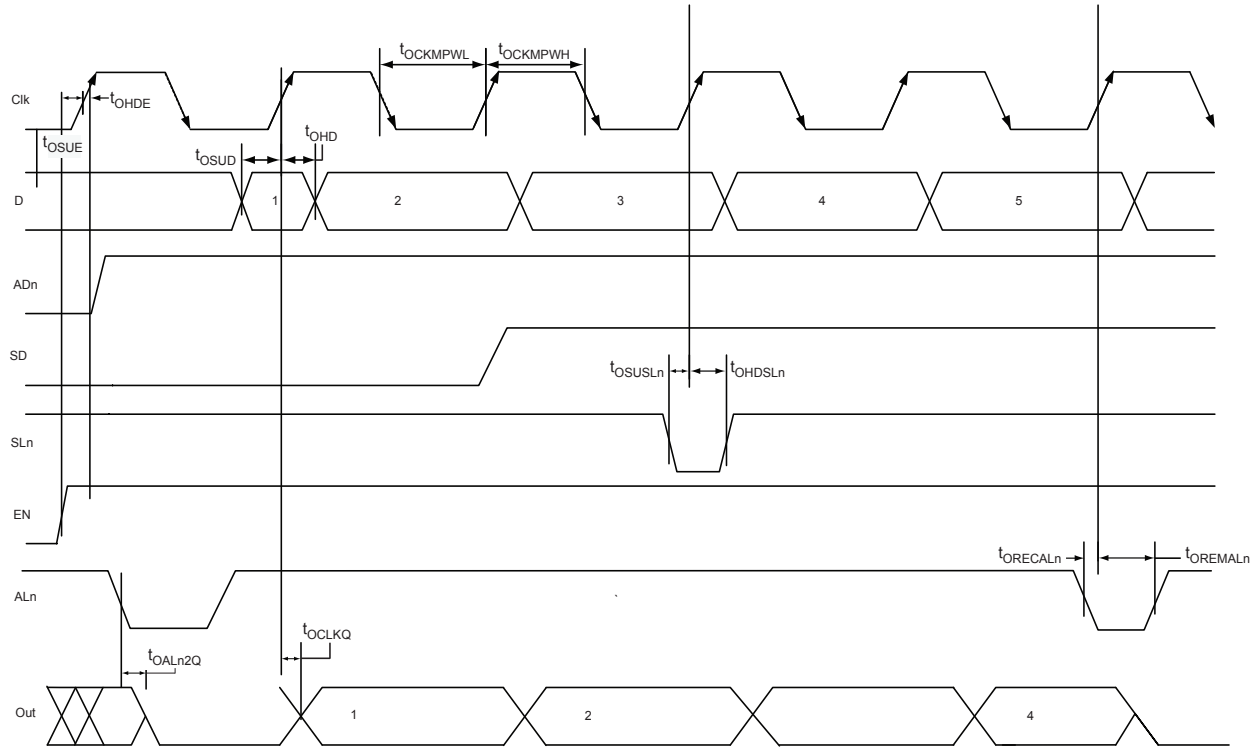


Figure 6 • I/O Register Output Timing Diagram



Table 89 • Output Data/Enable Register Propagation Delays
Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Measuring Nodes (from, to)*	-1	Std.	Units
t_{OBYP}	Bypass Delay of the Output/Enable Register	F, G or H, I	0.371	0.437	ns
t_{OCLKQ}	Clock-to-Q of the Output/Enable Register	E, G or E, I	0.277	0.326	ns
t_{OSUD}	Data Setup Time for the Output/Enable Register	A, E or J, E	TBD	TBD	ns
t_{OHD}	Data Hold Time for the Output/Enable Register	A, E or J, E	TBD	TBD	ns
t_{OSUE}	Enable Setup Time for the Output/Enable Register	B, E	0.441	0.519	ns
t_{OHE}	Enable Hold Time for the Output/Enable Register	B, E	0	0	ns
t_{OSUSL}	Synchronous Load Setup Time for the Output/Enable Register	D, E	0.207	0.243	ns
t_{OHSL}	Synchronous Load Hold Time for the Output/Enable Register	D, E	0	0	ns
t_{OALn2Q}	Asynchronous Clear-to-Q of the Output/Enable Register ($AD_n = 1$)	C, G or C, I	0.531	0.625	ns
	Asynchronous Preset-to-Q of the Output/Enable Register ($AD_n = 0$)	C, G or C, I	0.555	0.653	ns
$t_{OREMALn}$	Asynchronous Load Removal Time for the Output/Enable Register	C, E	0	0	ns
$t_{ORECALn}$	Asynchronous Load Recovery Time for the Output/Enable Register	C, E	0.036	0.042	ns
t_{OWALn}	Asynchronous Load Minimum Pulse Width for the Output/Enable Register	C, C	0.32	0.376	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width High for the Output/Enable Register	E, E	0.079	0.093	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width Low for the Output/Enable Register	E, E	0.168	0.197	ns

Note: *For the derating values at specific junction temperature and voltage supply levels, refer to [Table 7 on page 15](#) for derating values.

DDR Module Specification

Input DDR Module

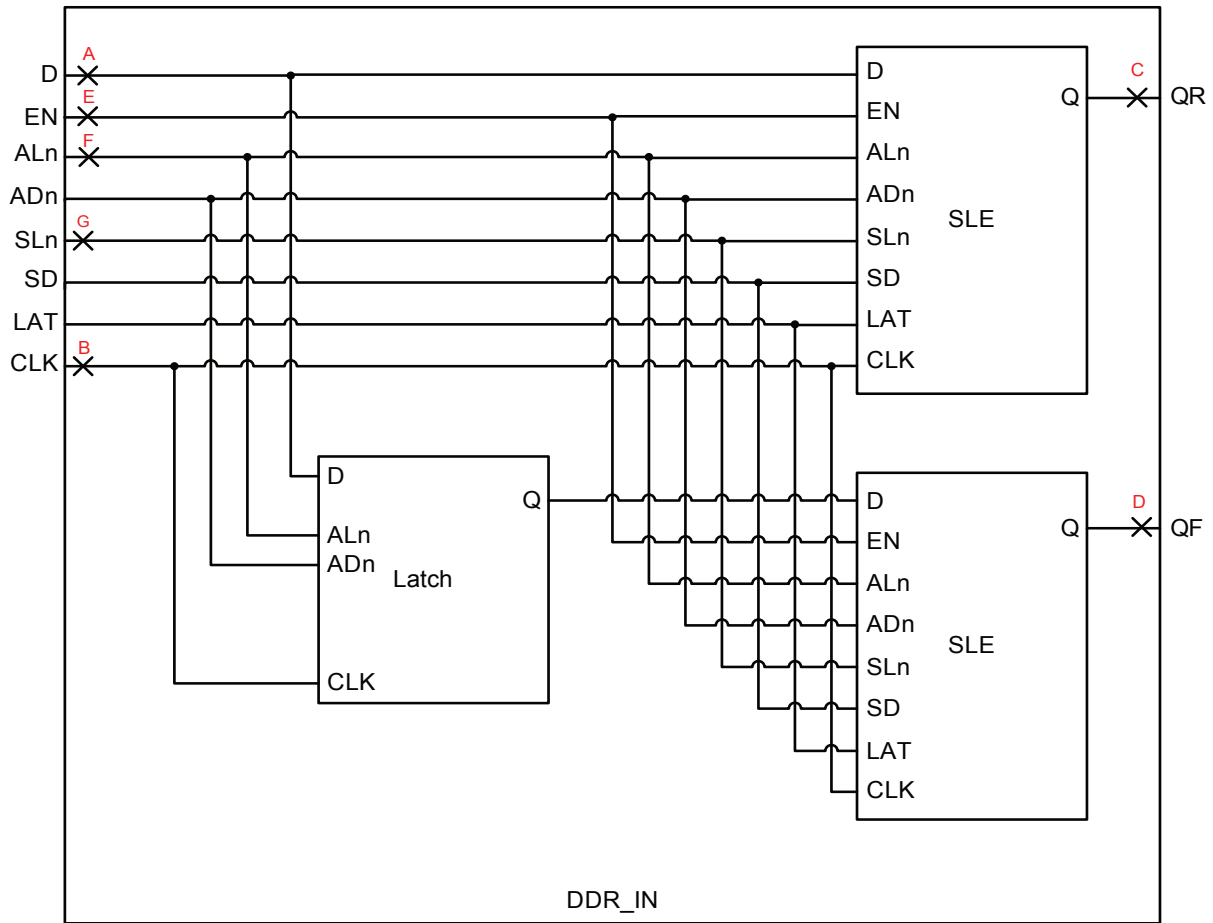


Figure 7 • Input DDR Module

Input DDR Timing Diagram

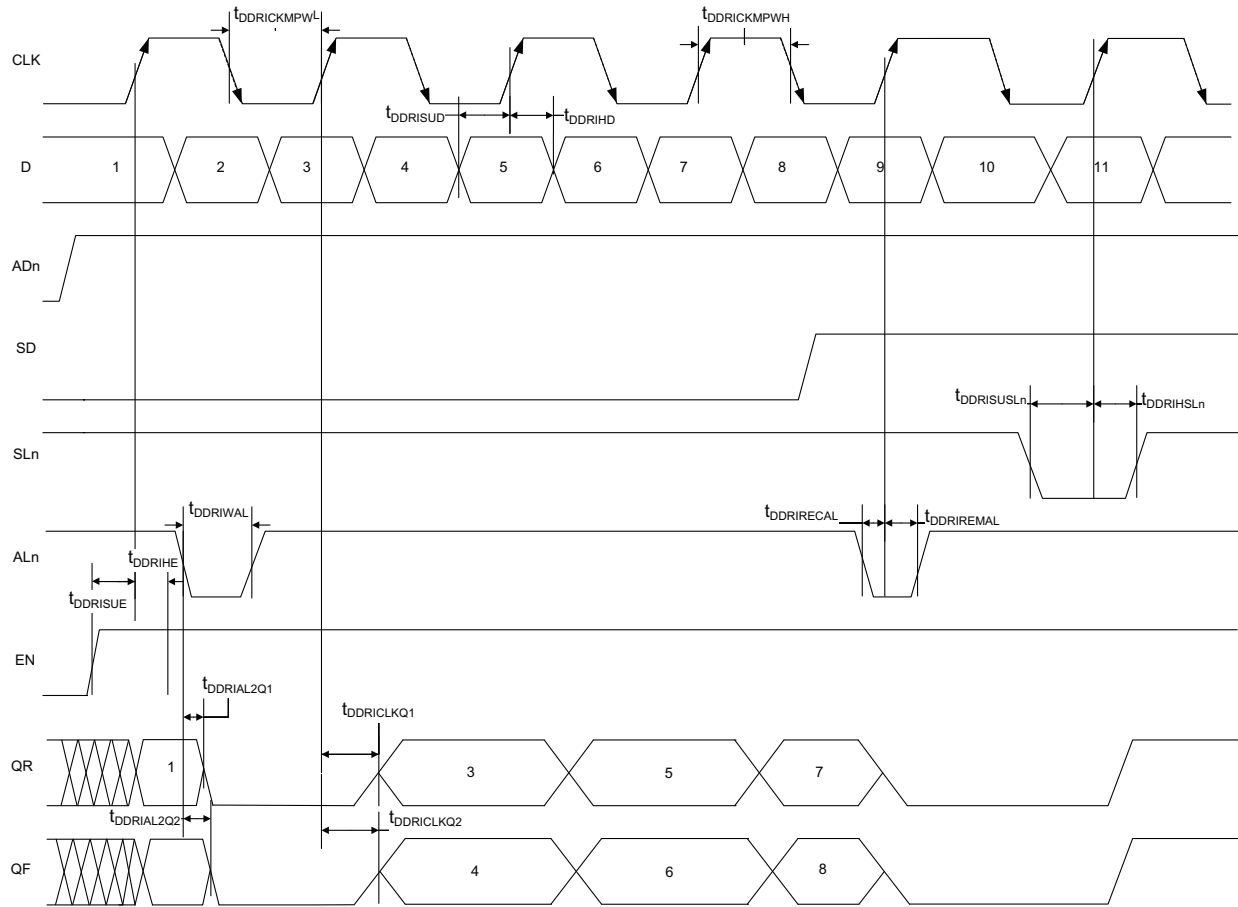


Figure 8 • Input DDR Timing Diagram

Timing Characteristics

Table 90 • Input DDR Propagation Delays

Parameter	Description	Measuring Nodes (from, to)	-1	Std.	Units
t_{DDRICKQ1}	Clock-to-Out Out_QR for Input DDR	B, C	0.168	0.198	ns
t_{DDRICKQ2}	Clock-to-Out Out_QF for Input DDR	B, D	0.175	0.205	ns
t_{DDRISUD}	Data Setup for Input DDR	A, B	0.376	0.443	ns
t_{DDRIHD}	Data Hold for Input DDR	A, B	0	0	ns
t_{DDRISUE}	Enable Setup for Input DDR	E, B	0.485	0.57	ns
t_{DDRIHE}	Enable Hold for Input DDR	E, B	0	0	ns
t_{DDRISUSL_n}	Synchronous Load Setup for Input DDR	G, B	0.485	0.57	ns
t_{DDRIHSL_n}	Synchronous Load Hold for Input DDR	G, B	0	0	ns
$t_{\text{DDRIAL2Q1}}$	Asynchronous Load-to-Out QR for Input DDR	F, C	0.618	0.727	ns
$t_{\text{DDRIAL2Q2}}$	Asynchronous Load-to-Out QF for Input DDR	F, D	0.569	0.67	ns
t_{DDRIEMAL}	Asynchronous Load Removal time for Input DDR	F, B	0	0	ns
$t_{\text{DDRIRECAL}}$	Asynchronous Load Recovery time for Input DDR	F, B	0.078	0.091	ns
t_{DDRIWAL}	Asynchronous Load Minimum Pulse Width for Input DDR	F, F	0.32	0.376	ns
$t_{\text{DDRICKMPWH}}$	Clock Minimum Pulse Width High for Input DDR	B, B	0.079	0.093	ns
$t_{\text{DDRICKMPWL}}$	Clock Minimum Pulse Width Low for Input DDR	B, B	0.168	0.197	ns

Output DDR Module

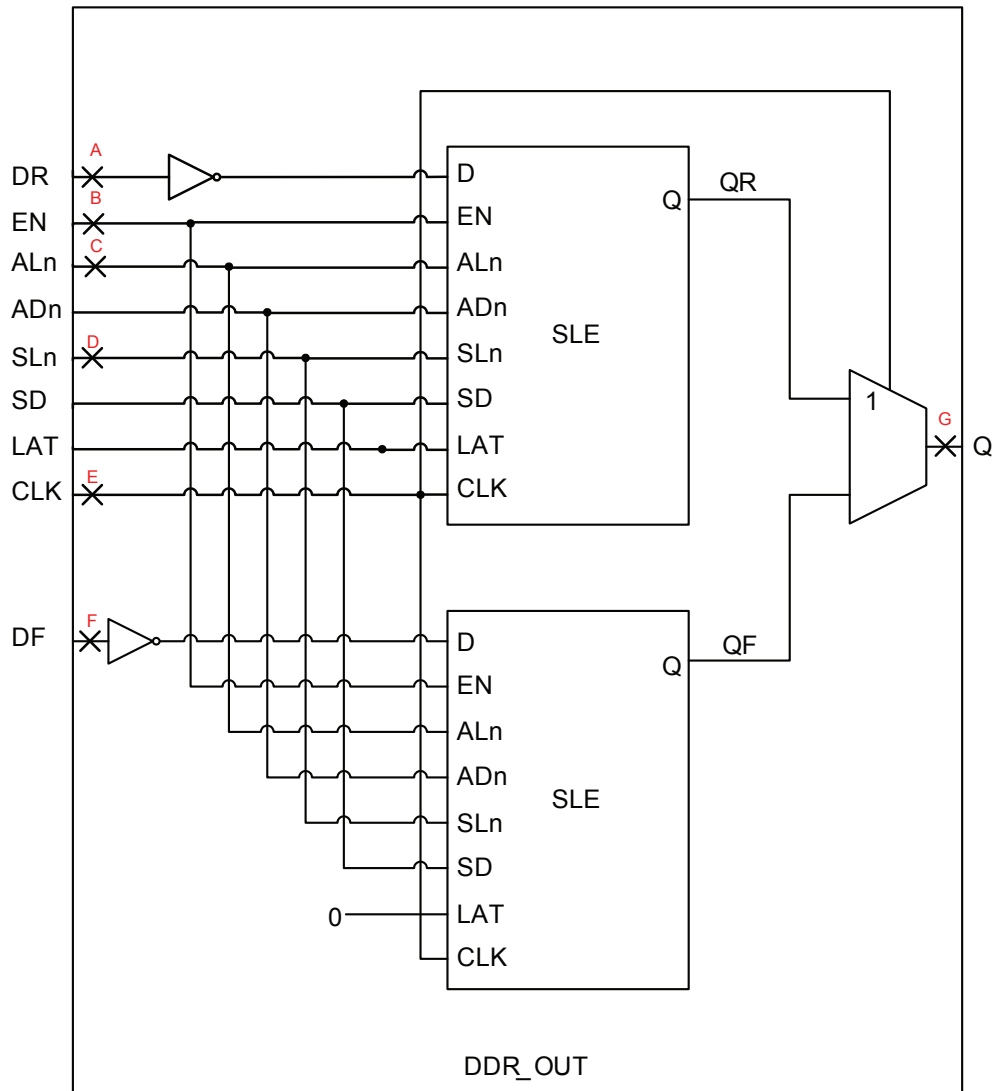


Figure 9 • Output DDR Module

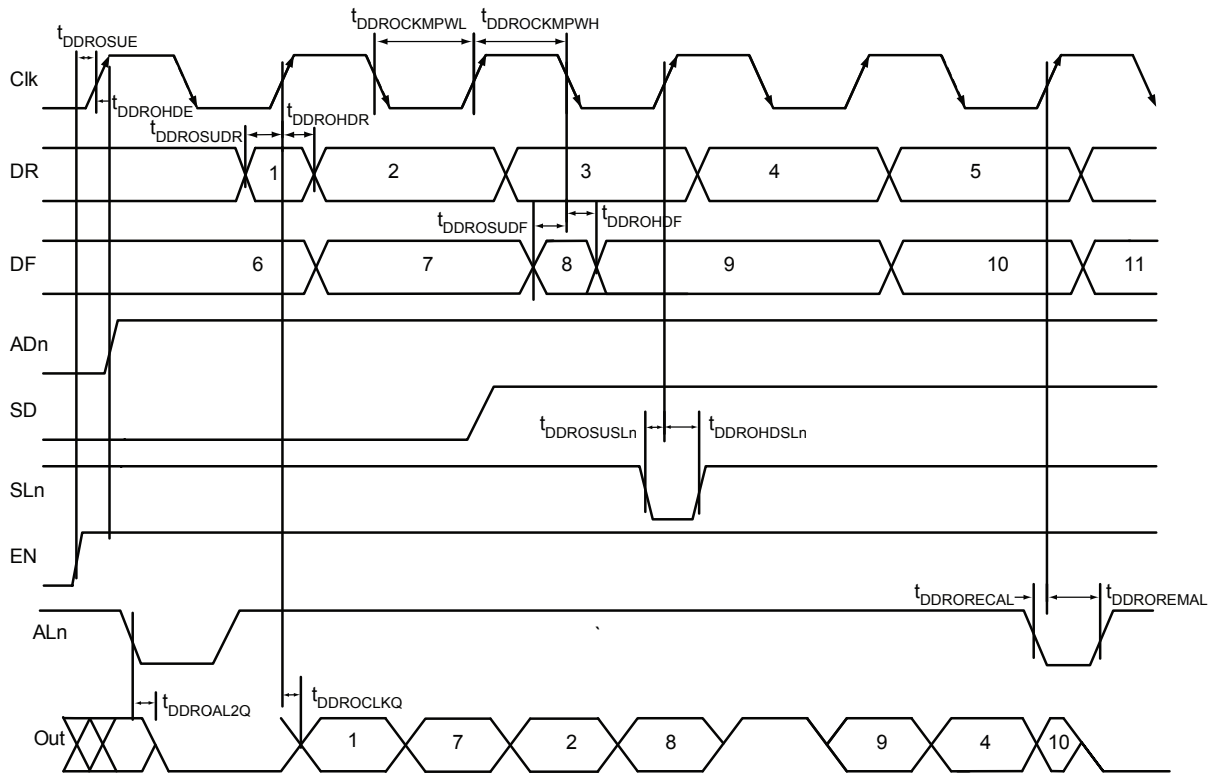


Figure 10 • Output DDR Timing Diagram



Timing Characteristics

Table 91 • Output DDR Propagation Delays

Parameter	Description	Measuring Nodes (from, to)	-1	Std.	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	E, G	0.277	0.326	ns
$t_{DDROSUDF}$	Data_F Data Setup for Output DDR	F, E	0.151	0.177	ns
$t_{DDROSUDR}$	Data_R Data Setup for Output DDR	A, E	0.2	0.235	ns
$t_{DDROHDF}$	Data_F Data Hold for Output DDR	F, E	0	0	ns
$t_{DDROHDR}$	Data_R Data Hold for Output DDR	A, E	0	0	ns
$t_{DDROSUE}$	Enable Setup for Input DDR	B, E	0.441	0.519	ns
t_{DDROHE}	Enable Hold for Input DDR	B, E	0	0	ns
$t_{DDROSUSL_n}$	Synchronous Load Setup for Input DDR	D, E	0.207	0.243	ns
$t_{DDROHSL_n}$	Synchronous Load Hold for Input DDR	D, E	0	0	ns
$t_{DDROAL2Q}$	Asynchronous Load-to-Out for Output DDR	C, G	0.555	0.653	ns
$t_{DDROREMA}$	Asynchronous Load Removal time for Output DDR	C, E	0	0	ns
$t_{DDRORECA}$	Asynchronous Load Recovery time for Output DDR	C, E	0.036	0.042	ns
$t_{DDROWAL}$	Asynchronous Load Minimum Pulse Width for Output DDR	C, C	0.32	0.376	ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width High for the Output DDR	E, E	0.079	0.093	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width Low for the Output DDR	E, E	0.168	0.197	ns

Logic Element Specifications

4-input LUT (LUT-4)

The SmartFusion2 offers a fully permutable 4-input LUT. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *SmartFusion2 Macro Library Guide*.

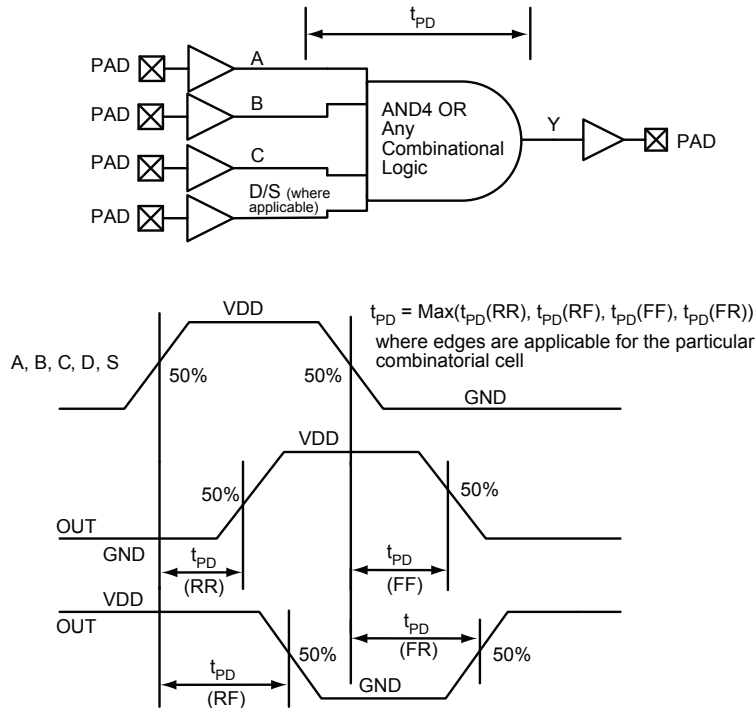


Figure 11 • LUT-4

Timing Characteristics

Table 92 • Combinatorial Cell Propagation Delays

Combinatorial Cell	Equation	Parameter	-1	Std.	Units	Notes
INV	$Y = !A$	t_{PD}	0.108	0.127	ns	
AND2	$Y = A \cdot B$	t_{PD}	0.189	0.222	ns	
NAND2	$Y = !(A \cdot B)$	t_{PD}	0.152	0.178	ns	
OR2	$Y = A + B$	t_{PD}	0.189	0.222	ns	
NOR2	$Y = !(A + B)$	t_{PD}	0.152	0.178	ns	
XOR2	$Y = A \oplus B$	t_{PD}	0.189	0.222	ns	
XOR3	$Y = A \oplus B \oplus C$	t_{PD}	0.24	0.283	ns	
AND3	$Y = A \cdot B \cdot C$	t_{PD}	0.22	0.259	ns	
AND4	$Y = A \cdot B \cdot C \cdot D$	t_{PD}	0.39	0.459	ns	

Sequential Module

SmartFusion2 offers a separate flip-flop which can be used independently from the LUT. The flip-flop can be configured as a register or a latch and has a data input and optional enable, synchronous load (clear or preset), and asynchronous load (clear or preset), and asynchronous load (clear or preset).

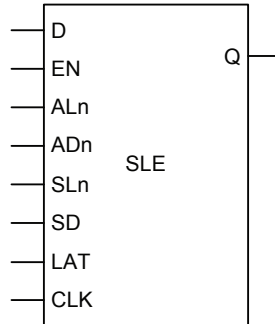


Figure 12 • Sequential Module

Figure 13 shows a configuration with SD = 1 (synchronous preset) and ADn = 1 (asynchronous clear) for a flip-flop (LAT = 0).

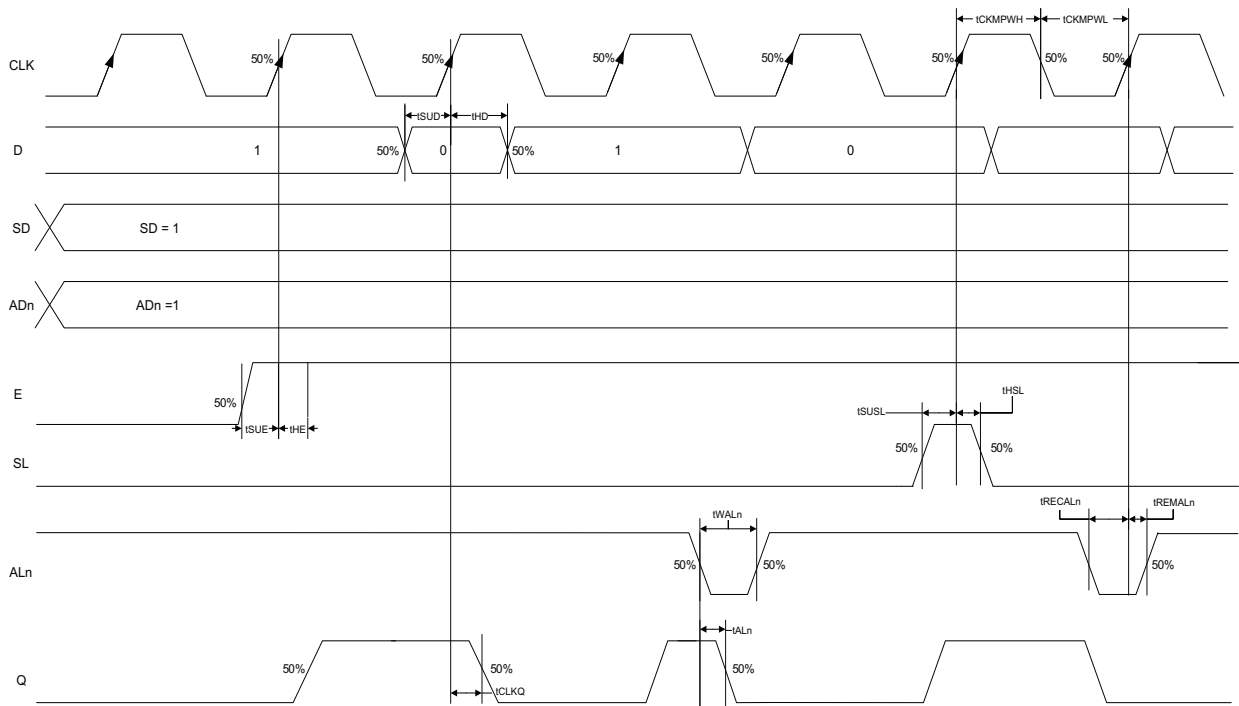


Figure 13 • Timing Diagram

Timing Characteristics

Table 93 • Register Delays

Parameter	Description	-1	Std.	Units	Notes
t_{CLKQ}	Clock-to-Q of the Core register	0.115	0.136	ns	
t_{SUD}	Data Setup Time for the Core register	0.267	0.315	ns	
t_{HD}	Data Hold Time for the Core register	0	0	ns	
t_{SUE}	Enable Setup Time for the Core register	0.357	0.42	ns	
t_{HE}	Enable Hold Time for the Core register	0	0	ns	
t_{SUSL}	Synchronous Load Setup Time for the Core register	0.357	0.42	ns	
t_{HSL}	Synchronous Load Hold Time for the Core register	0	0	ns	
t_{ALn2Q}	Asynchronous Clear-to-Q of the Core register ($ADn = 1$)	0.502	0.591	ns	
	Asynchronous Preset-to-Q of the Core register ($ADn = 0$)	TBD	TBD	ns	
t_{REMAIn}	Asynchronous Load Removal Time for the Core register	0	0	ns	
t_{RECALn}	Asynchronous Load Recovery Time for the Core register	0.373	0.439	ns	
t_{WALn}	Asynchronous Load Minimum Pulse Width for the Core register	0.32	0.376	ns	
t_{CKMPWH}	Clock Minimum Pulse Width High for the Core register	0.079	0.093	ns	
t_{CKMPWL}	Clock Minimum Pulse Width Low for the Core register	0.168	0.197	ns	



Global Resource Characteristics

SmartFusion2 devices offer a powerful, low skew global routing network which provides an effective clock distribution throughout the FPGA fabric. Refer to the [SmartFusion2 FPGA Fabric Architecture User's Guide](#) for the positions of various global routing resources.

Table 94 • M2S050T Global Resource

Parameter	Description	-1		Std.		Units	Notes
		Min.	Max.	Min.	Max.		
t _{RCKL}	Input Low Delay for Global Clock	0.84	0.901	0.838	0.901	ns	
t _{RCKH}	Input High Delay for Global Clock	1.548	1.655	1.82	1.947	ns	
t _{RCKMPWH}	Minimum Pulse Width High for Global Clock					ns	
t _{RCKMPWL}	Minimum Pulse Width Low for Global Clock					ns	
t _{RCKSW}	Maximum Skew for Global Clock		0.107		0.127	ns	

Table 95 • M2S025T Global Resource

Parameter	Description	-1		Std.		Units	Notes
		Min.	Max.	Min.	Max.		
t _{RCKL}	Input Low Delay for Global Clock	0.801	0.844	0.801	0.844	ns	
t _{RCKH}	Input High Delay for Global Clock	1.484	1.563	1.745	1.838	ns	
t _{RCKMPWH}	Minimum Pulse Width High for Global Clock					ns	
t _{RCKMPWL}	Minimum Pulse Width Low for Global Clock					ns	
t _{RCKSW}	Maximum Skew for Global Clock		0.079		0.093	ns	

Table 96 • M2S010T Global Resource

Parameter	Description	-1		Std.		Units	Notes
		Min.	Max.	Min.	Max.		
t _{RCKL}	Input Low Delay for Global Clock	0.769	0.808	0.768	0.808	ns	
t _{RCKH}	Input High Delay for Global Clock	1.465	1.538	1.721	1.81	ns	
t _{RCKMPWH}	Minimum Pulse Width High for Global Clock					ns	
t _{RCKMPWL}	Minimum Pulse Width Low for Global Clock					ns	
t _{RCKSW}	Maximum Skew for Global Clock		0.073		0.089	ns	

FPGA Fabric SRAM

Refer to the *SmartFusion2 FPGA Fabric Architecture User's Guide* for more information.

FPGA Fabric Large SRAM (LSRAM)

Table 97 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 1K × 18

Parameter	Description	-1		Std.		Units
		Min.	Max.	Min.	Max.	
t _{CY}	Clock period	1.981	–	2.33	–	ns
t _{CLKMPWH}	Clock minimum pulse width High	0.823	–	0.968	–	ns
t _{CLKMPWL}	Clock minimum pulse width Low	0.318	–	0.374	–	ns
t _{PLCY}	Pipelined clock period	2.096	–	2.465	–	ns
t _{PLCLKMPWH}	Pipelined clock minimum pulse width High	0.826	–	0.972	–	ns
t _{PLCLKMPWL}	Pipelined clock minimum pulse width Low	0.315	–	0.371	–	ns
t _{CLK2Q}	Read access time with pipeline register	–	0.352	–	0.414	ns
	Read access time without pipeline register	–	2.392	–	2.815	ns
	Access time with feed-through write timing	–	1.609	–	1.893	ns
t _{ADDRSU}	Address setup time	0.457	–	0.538	–	ns
t _{ADDRHD}	Address hold time	0.077	–	0.09	–	ns
t _{DSU}	Data setup time	0.394	–	0.463	–	ns
t _{DHD}	Data hold time	0.113	–	0.133	–	ns
t _{BLKSU}	Block select setup time (with pipelined register enabled)	0.211	–	0.249	–	ns
t _{BLKHD}	Block select hold time (with pipelined register enabled)	0.158	–	0.186	–	ns
t _{BLK2Q}	Block select to out disable time (when pipelined register is disabled)	–	TBD	–	TBD	ns
t _{BLKMPW}	Block select minimum pulse width	0.14	–	0.164	–	ns
t _{RDESU}	Read enable setup time (A_WEN, B_WEN = 0)	0.465	–	0.547	–	ns
t _{RDEHD}	Read enable hold time (A_WEN, B_WEN = 0)	0.21	–	0.247	–	ns
t _{RDPLESU}	Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	0.703	–	0.827	–	ns
t _{RDPLEHD}	Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	–0.053	–	–0.062	–	ns
t _{R2Q}	Asynchronous reset to output propagation delay	–	1.586	–	1.865	ns
t _{RSTREM}	Asynchronous reset removal time	0.532	–	0.626	–	ns
t _{RSTREC}	Asynchronous reset recovery time	0.005	–	0.006	–	ns
t _{RSTMPW}	Asynchronous reset minimum pulse width	0.317	–	0.373	–	ns
t _{PLRSTREM}	Pipelined register asynchronous reset removal time	–0.293	–	–0.345	–	ns
t _{PLRSTREC}	Pipelined register asynchronous reset recovery time	0.344	–	0.405	–	ns
t _{PLRSTMPW}	Pipelined register asynchronous reset minimum pulse width	0.297	–	0.35	–	ns
t _{SRSTSU}	Synchronous reset setup time	0.231	–	0.271	–	ns
t _{SRSTHD}	Synchronous reset hold time	–0.054	–	–0.063	–	ns
t _{WESU}	Write enable setup time (A_WEN, B_WEN = 1)	0.417	–	0.49	–	ns
t _{WEHD}	Write enable hold time (A_WEN, B_WEN = 1)	0.053	–	0.063	–	ns



Table 98 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 2K × 9

Parameter	Description	-1		Std.		Units
		Min.	Max.	Min.	Max.	
t _{CY}	Clock period	1.981	–	2.33	–	ns
t _{CLKMPWH}	Clock minimum pulse width High	0.823	–	0.968	–	ns
t _{CLKMPWL}	Clock minimum pulse width Low	0.318	–	0.374	–	ns
t _{PLCY}	Pipelined clock period	2.096	–	2.465	–	ns
t _{PLCLKMPWH}	Pipelined clock minimum pulse width High	0.826	–	0.972	–	ns
t _{PLCLKMPWL}	Pipelined clock minimum pulse width Low	0.315	–	0.371	–	ns
t _{CLK2Q}	Read access time with pipeline register	–	0.352	–	0.414	ns
	Read access time without pipeline register	–	2.392	–	2.814	ns
	Access time with feed-through write timing	–	1.61	–	1.894	ns
t _{ADDRSU}	Address setup time	0.493	–	0.58	–	ns
t _{ADDRHD}	Address hold time	0.077	–	0.09	–	ns
t _{DSU}	Data setup time	0.388	–	0.456	–	ns
t _{DHD}	Data hold time	0.085	–	0.1	–	ns
t _{BLKSU}	Block select setup time	0.211	–	0.249	–	ns
t _{BLKHD}	Block select hold time	0.158	–	0.186	–	ns
t _{BLK2Q}	Block select to out disable time (when pipelined register is disabled)	–	TBD	–	TBD	ns
t _{BLKMPW}	Block select minimum pulse width	0.14	–	0.164	–	ns
t _{RDESU}	Read enable setup time (A_WEN, B_WEN = 0)	0.503	–	0.592	–	ns
t _{RDEHD}	Read enable hold time (A_WEN, B_WEN = 0)	0.21	–	0.247	–	ns
t _{RDPLESU}	Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	0.703	–	0.827	–	ns
t _{RDPLEHD}	Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	–0.053	–	–0.062	–	ns
t _{R2Q}	Asynchronous reset to output propagation delay	–	1.594	–	1.875	ns
t _{RSTREM}	Asynchronous reset removal time	0.532	–	0.626	–	ns
t _{RSTREC}	Asynchronous reset recovery time	0.005	–	0.006	–	ns
t _{RSTMPW}	Asynchronous reset minimum pulse width	0.317	–	0.373	–	ns
t _{PLRSTREM}	Pipelined register asynchronous reset removal time	–0.293	–	–0.345	–	ns
t _{PLRSTREC}	Pipelined register asynchronous reset recovery time	0.344	–	0.405	–	ns
t _{PLRSTMPW}	Pipelined register asynchronous reset minimum pulse width	0.297	–	0.35	–	ns
t _{SRSTSU}	Synchronous reset setup time	0.231	–	0.271	–	ns
t _{SRSTHD}	Synchronous reset hold time	–0.054	–	–0.063	–	ns
t _{WESU}	Write enable setup time (A_WEN, B_WEN = 1)	0.443	–	0.522	–	ns
t _{WEHD}	Write enable hold time (A_WEN, B_WEN = 1)	0.053	–	0.063	–	ns

Table 99 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 4K × 4

Parameter	Description	-1		Std.		Units
		Min.	Max.	Min.	Max.	
t _{CY}	Clock period	1.981	–	2.33	–	ns
t _{CLKMPWH}	Clock minimum pulse width High	0.823	–	0.968	–	ns
t _{CLKMPWL}	Clock minimum pulse width Low	0.318	–	0.374	–	ns
t _{PLCY}	Pipelined clock period	2.096	–	2.465	–	ns
t _{PLCLKMPWH}	Pipelined clock minimum pulse width High	0.826	–	0.972	–	ns
t _{PLCLKMPWL}	Pipelined clock minimum pulse width Low	0.315	–	0.371	–	ns
t _{CLK2Q}	Read access time with pipeline register	–	0.34	–	0.4	ns
	Read access time without pipeline register	–	2.392	–	2.814	ns
	Access time with feed-through write timing	–	1.591	–	1.872	ns
t _{ADDRSU}	Address setup time	0.564	–	0.664	–	ns
t _{ADDRHD}	Address hold time	0.077	–	0.09	–	ns
t _{DSU}	Data setup time	0.377	–	0.443	–	ns
t _{DHD}	Data hold time	0.085	–	0.1	–	ns
t _{BLKSU}	Block select setup time	0.211	–	0.249	–	ns
t _{BLKHD}	Block select hold time	0.158	–	0.186	–	ns
t _{BLK2Q}	Block select to out disable time (when pipelined register is disabled)	–	TBD	–	TBD	ns
t _{BLKMPW}	Block select minimum pulse width	0.14	–	0.164	–	ns
t _{RDESU}	Read enable setup time (A_WEN, B_WEN = 0)	0.536	–	0.631	–	ns
t _{RDEHD}	Read enable hold time (A_WEN, B_WEN = 0)	0.21	–	0.247	–	ns
t _{RDPLESU}	Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	0.703	–	0.827	–	ns
t _{RDPLEHD}	Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	–0.053	–	–0.062	–	ns
t _{R2Q}	Asynchronous reset to output propagation delay	–	1.587	–	1.866	ns
t _{RSTREM}	Asynchronous reset removal time	0.532	–	0.626	–	ns
t _{RSTREC}	Asynchronous reset recovery time	0.005	–	0.006	–	ns
t _{RSTMPW}	Asynchronous reset minimum pulse width	0.317	–	0.373	–	ns
t _{PLRSTREM}	Pipelined register asynchronous reset removal time	–0.293	–	–0.345	–	ns
t _{PLRSTREC}	Pipelined register asynchronous reset recovery time	0.344	–	0.405	–	ns
t _{PLRSTMPW}	Pipelined register asynchronous reset minimum pulse width	0.297	–	0.35	–	ns
t _{SRSTSU}	Synchronous reset setup time	0.231	–	0.271	–	ns
t _{SRSTHD}	Synchronous reset hold time	–0.054	–	–0.063	–	ns
t _{WESU}	Write enable setup time (A_WEN, B_WEN = 1)	0.489	–	0.575	–	ns
t _{WEHD}	Write enable hold time (A_WEN, B_WEN = 1)	0.053	–	0.063	–	ns



Table 100 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 8K × 2

Parameter	Description	-1		Std.		Units
		Min.	Max.	Min.	Max.	
t _{CY}	Clock period	1.981	–	2.33	–	ns
t _{CLKMPWH}	Clock minimum pulse width High	0.823	–	0.968	–	ns
t _{CLKMPWL}	Clock minimum pulse width Low	0.318	–	0.374	–	ns
t _{PLCY}	Pipelined clock period	2.096	–	2.465	–	ns
t _{PLCLKMPWH}	Pipelined clock minimum pulse width High	0.826	–	0.972	–	ns
t _{PLCLKMPWL}	Pipelined clock minimum pulse width Low	0.315	–	0.371	–	ns
t _{CLK2Q}	Read access time with pipeline register	–	0.337	–	0.397	ns
	Read access time without pipeline register	–	2.392	–	2.814	ns
	Access time with feed-through write timing	–	1.591	–	1.872	ns
t _{ADDRSU}	Address setup time	0.637	–	0.749		ns
t _{ADDRHD}	Address hold time	0.077	–	0.09		ns
t _{DSU}	Data setup time	0.373	–	0.439		ns
t _{DHD}	Data hold time	0.085	–	0.1		ns
t _{BLKSU}	Block select setup time	0.211	–	0.249		ns
t _{BLKHD}	Block select hold time	0.158	–	0.186		ns
t _{BLK2Q}	Block select to out disable time (when pipelined register is disabled)	–	TBD	–	TBD	ns
t _{BLKMPW}	Block select minimum pulse width	0.14	–	0.164	–	ns
t _{RDESU}	Read enable setup time (A_WEN, B_WEN = 0)	0.55	–	0.647	–	ns
t _{RDEHD}	Read enable hold time (A_WEN, B_WEN = 0)	0.21	–	0.247	–	ns
t _{RDPLESU}	Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	0.703	–	0.827	–	ns
t _{RDPLEHD}	Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	–0.053	–	–0.062	–	ns
t _{R2Q}	Asynchronous reset to output propagation delay	–	1.608		1.892	ns
t _{RSTREM}	Asynchronous reset removal time	0.532	–	0.626	–	ns
t _{RSTREC}	Asynchronous reset recovery time	0.005	–	0.006	–	ns
t _{RSTMPW}	Asynchronous reset minimum pulse width	0.317	–	0.373	–	ns
t _{PLRSTREM}	Pipelined register asynchronous reset removal time	–0.293	–	–0.345	–	ns
t _{PLRSTREC}	Pipelined register asynchronous reset recovery time	0.344	–	0.405	–	ns
t _{PLRSTMPW}	Pipelined register asynchronous reset minimum pulse width	0.297	–	0.35	–	ns
t _{SRSTSU}	Synchronous reset setup time	0.231	–	0.271	–	ns
t _{SRSTHD}	Synchronous reset hold time	–0.054	–	–0.063	–	ns
t _{WESU}	Write enable setup time (A_WEN, B_WEN = 1)	0.521	–	0.612	–	ns
t _{WEHD}	Write enable hold time (A_WEN, B_WEN = 1)	0.053	–	0.063	–	ns

Table 101 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 16K × 1

Parameter	Description	-1		Std.		Units
		Min.	Max.	Min.	Max.	
t _{CY}	Clock period	1.981		2.33		ns
t _{CLKMPWH}	Clock minimum pulse width High	0.823		0.968		ns
t _{CLKMPWL}	Clock minimum pulse width Low	0.318		0.374		ns
t _{PLCY}	Pipelined clock period	2.096		2.465		ns
t _{PLCLKMPWH}	Pipelined clock minimum pulse width High	0.826		0.972		ns
t _{PLCLKMPWL}	Pipelined clock minimum pulse width Low	0.315		0.371		ns
t _{CLK2Q}	Read access time with pipeline register		0.337		0.397	ns
	Read access time without pipeline register		2.388		2.809	ns
	Access time with feed-through write timing		1.59		1.87	ns
t _{ADDRSU}	Address setup time	0.652		0.767		ns
t _{ADDRHD}	Address hold time	0.077		0.09		ns
t _{DSU}	Data setup time	0.362		0.426		ns
t _{DHD}	Data hold time	0.085		0.1		ns
t _{BLKSU}	Block select setup time	0.211		0.249		ns
t _{BLKHD}	Block select hold time	0.158		0.186		ns
t _{BLK2Q}	Block select to out disable time (when pipelined register is disabled)	–	TBD	–	TBD	ns
t _{BLKMPW}	Block select minimum pulse width	0.14	–	0.164	–	ns
t _{RDESU}	Read enable setup time (A_WEN, B_WEN = 0)	0.551	–	0.648	–	ns
t _{RDEHD}	Read enable hold time (A_WEN, B_WEN = 0)	0.21	–	0.247	–	ns
t _{RDPLESU}	Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	0.703	–	0.827	–	ns
t _{RDPLEHD}	Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	–0.053	–	–0.062	–	ns
t _{R2Q}	Asynchronous reset to output propagation delay	–	1.628	–	1.916	ns
t _{RSTREM}	Asynchronous reset removal time	0.532	–	0.626	–	ns
t _{RSTREC}	Asynchronous reset recovery time	0.005	–	0.006	–	ns
t _{RSTMPW}	Asynchronous reset minimum pulse width	0.317	–	0.373	–	ns
t _{PLRSTREM}	Pipelined register asynchronous reset removal time	–0.293	–	–0.345	–	ns
t _{PLRSTREC}	Pipelined register asynchronous reset recovery time	0.344	–	0.405	–	ns
t _{PLRSTMPW}	Pipelined register asynchronous reset minimum pulse width	0.297	–	0.35	–	ns
t _{SRSTSU}	Synchronous reset setup time	0.231	–	0.271	–	ns
t _{SRSTHD}	Synchronous reset hold time	–0.054	–	–0.063	–	ns
t _{WESU}	Write enable setup time (A_WEN, B_WEN = 1)	0.485	–	0.57	–	ns
t _{WEHD}	Write enable hold time (A_WEN, B_WEN = 1)	0.053	–	0.063	–	ns



Table 102 • RAM1K18 – Two-Port Mode for Depth × Width C0nfiguration 512 × 36

Parameter	Description	-1		Std.		Units
		Min.	Max.	Min.	Max.	
t _{CY}	Clock period	1.981	–	2.33	–	ns
t _{CLKMPWH}	Clock minimum pulse width High	0.823	–	0.968	–	ns
t _{CLKMPWL}	Clock minimum pulse width Low	0.318	–	0.374	–	ns
t _{PLCY}	Pipelined clock period	2.096	–	2.465	–	ns
t _{PLCLKMPWH}	Pipelined clock minimum pulse width High	0.826	–	0.972	–	ns
t _{PLCLKMPWL}	Pipelined clock minimum pulse width Low	0.315	–	0.371	–	ns
t _{CLK2Q}	Read access time with pipeline register	–	0.35	–	0.41	ns
	Read access time without pipeline register	–	2.37	–	2.79	ns
t _{ADDRSU}	Address setup time	0.207	–	0.244	–	ns
t _{ADDRHD}	Address hold time	0.077	–	0.09	–	ns
t _{DSU}	Data setup time	0.389	–	0.458	–	ns
t _{DHD}	Data hold time	0.117	–	0.138	–	ns
t _{BLKSU}	Block select setup time	0.211	–	0.249	–	ns
t _{BLKHD}	Block select hold time	0.027	–	0.032	–	ns
t _{BLK2Q}	Block select to out disable time (when pipelined register is disabled)	–	TBD	–	TBD	ns
t _{BLKMPW}	Block select minimum pulse width	0.14	–	0.164	–	ns
t _{RDESU}	Read enable setup time (A_WEN, B_WEN = 0)	0.465	–	0.547	–	ns
t _{RDEHD}	Read enable hold time (A_WEN, B_WEN = 0)	0.21	–	0.247	–	ns
t _{RDPLESU}	Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	0.703	–	0.827	–	ns
t _{RDPLEHD}	Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	–0.05	–	–0.06	–	ns
t _{R2Q}	Asynchronous reset to output propagation delay	–	1.59	–	1.87	ns
t _{RSTREM}	Asynchronous reset removal time	0.532	–	0.626	–	ns
t _{RSTREC}	Asynchronous reset recovery time	0.005	–	0.006	–	ns
t _{RSTMPW}	Asynchronous reset minimum pulse width	0.317	–	0.373	–	ns
t _{PLRSTREM}	Pipelined register asynchronous reset removal time	–0.29	–	–0.35	–	ns
t _{PLRSTREC}	Pipelined register asynchronous reset recovery time	0.344	–	0.405	–	ns
t _{PLRSTMPW}	Pipelined register asynchronous reset minimum pulse width	0.297	–	0.35	–	ns
t _{SRSTSU}	Synchronous reset setup time	0.231	–	0.271	–	ns
t _{SRSTHD}	Synchronous reset hold time	–0.05	–	–0.06	–	ns
t _{WESU}	Write enable setup time (A_WEN, B_WEN = 1)	0.417	–	0.49	–	ns
t _{WEHD}	Write enable hold time (A_WEN, B_WEN = 1)	0.053	–	0.063	–	ns

FPGA Fabric Micro SRAM (uSRAM)

Table 103 • uSRAM (RAM64x18) in 64x18 Mode

Parameter	Description	-1		Std.		Units
		Min.	Max.	Min.	Max.	
t _{CY}	Read clock period	0.836	–	0.984	–	ns
t _{CLKMPWH}	Read clock minimum pulse width High	0.296	–	0.348	–	ns
t _{CLKMPWL}	Read clock minimum pulse width Low	0.324	–	0.382	–	ns
t _{PLCY}	Read pipeline clock period	1.989	–	2.34	–	ns
t _{PLCLKMPWH}	Read pipeline clock minimum pulse width High	0.259	–	0.305	–	ns
t _{PLCLKMPWL}	Read pipeline clock minimum pulse width Low	0.296	–	0.348	–	ns
t _{CLPL1}	Minimum pipeline clock low phase in order to prevent glitches with pipeline register in latch mode	TBD	–	TBD	–	ns
t _{CLK2Q}	Read access time with pipeline register	–	0.37	–	0.435	ns
	Read access time with pipeline register in latch mode	–	1.858	–	2.185	ns
	Read access time without pipeline register	TBD	–	TBD	–	ns
t _{ADDRSU}	Read address setup time in synchronous mode	0.294	–	0.345	–	ns
	Read address setup time in asynchronous mode	1.755	–	2.064	–	ns
t _{ADDRHD}	Read address hold time in synchronous mode	0.055	–	0.064	–	ns
	Read address hold time in asynchronous mode	0.035	–	0.041	–	ns
t _{RDENSU}	Read enable setup time	0.245	–	0.289	–	ns
t _{RDENHD}	Read enable hold time	0.074	–	0.087	–	ns
t _{BLKSU}	Read block select setup time (with pipeline register enabled)	1.901	–	2.237	–	ns
t _{BLKHD}	Read block select hold time (with pipelined register enabled)	0.001	–	0.001	–	ns
t _{BLK2Q}	Read block select to out disable time (when pipelined register is disabled)	–	2.173	–	2.556	ns
t _{BLKMPW}	Read block select minimum pulse width	TBD	–	TBD	–	ns
t _{RSTREM}	Read asynchronous reset removal time (pipelined clock)	0	–	0	–	ns
	Read asynchronous reset removal time (non-pipelined clock)	0.03	–	0.036	–	ns
t _{RSTREC}	Read asynchronous reset recovery time (pipelined clock)	0.546	–	0.642	–	ns
	Read asynchronous reset recovery time (non-pipelined clock)	0.085	–	0.099	–	ns
t _{R2Q}	Read asynchronous reset to output propagation delay (with pipelined register enabled)	–	1.05	–	1.236	ns
	Read asynchronous reset to output propagation delay (with pipelined register disabled)	–	0.944	–	1.11	ns
t _{SRSTSU}	Read synchronous reset setup time	0.25	–	0.294	–	ns
t _{SRSTHD}	Read synchronous reset hold time	0.074	–	0.087	–	ns
t _{CCY}	Write clock period	1.49	–	1.752	–	ns
t _{CCLKMPWH}	Write clock minimum pulse width High	0.506	–	0.596	–	ns
t _{CCLKMPWL}	Write clock minimum pulse width Low	0.297	–	0.349	–	ns
t _{BLKCSU}	Write block setup time	0.332	–	0.39	–	ns
t _{BLKCHD}	Write block hold time	–0.009	–	–0.011	–	ns



Table 103 • uSRAM (RAM64x18) in 64x18 Mode (continued)

Parameter	Description	-1		Std.		Units
		Min.	Max.	Min.	Max.	
t _{DINCSU}	Write input data setup time	0.017	–	0.02	–	ns
t _{DINCHD}	Write input data hold time	0.002	–	0.003	–	ns
t _{ADDRCSU}	Write address setup time	0.012	–	0.015	–	ns
t _{ADDRCHD}	Write address hold time	–0.043	–	–0.05	–	ns
t _{WECSU}	Write enable setup time	0.32	–	0.377	–	ns
t _{WECHD}	Write enable hold time	–0.03	–	–0.035	–	ns

Table 104 • uSRAM (RAM64x16) in 64x16 Mode

Parameter	Description	-1		Std.		Units
		Min.	Max.	Min.	Max.	
t _{CY}	Read clock period	0.836	–	0.984	–	ns
t _{CLKMPWH}	Read clock minimum pulse width High	0.296	–	0.348	–	ns
t _{CLKMPWL}	Read clock minimum pulse width Low	0.324	–	0.382	–	ns
t _{PLCY}	Read pipeline clock period	1.989	–	2.34	–	ns
t _{PLCLKMPWH}	Read pipeline clock minimum pulse width High	0.259	–	0.305	–	ns
t _{PLCLKMPWL}	Read pipeline clock minimum pulse width Low	0.296	–	0.348	–	ns
t _{CLPL1}	Minimum pipeline clock low phase in order to prevent glitches with pipeline register in latch mode	TBD	–	TBD	–	ns
t _{CLK2Q}	Read access time with pipeline register	–	0.37	–	0.435	ns
	Read access time with pipeline register in latch mode	–	1.858	–	2.185	ns
	Read access time without pipeline register	TBD	–	TBD	–	ns
t _{ADDRSU}	Read address setup time in synchronous mode	0.294	–	0.345	–	ns
	Read address setup time in asynchronous mode	1.755	–	2.064	–	ns
t _{ADDRHD}	Read address hold time in synchronous mode	0.055	–	0.064	–	ns
	Read address hold time in asynchronous mode	0.035	–	0.041	–	ns
t _{RDENSU}	Read enable setup time	0.245	–	0.289	–	ns
t _{RDENHD}	Read enable hold time	0.074	–	0.087	–	ns
t _{BLKSU}	Read block select setup time (with pipeline register enabled)	1.901	–	2.237	–	ns
t _{BLKHD}	Read block select hold time (with pipelined register enabled)	0.001	–	0.001	–	ns
t _{BLK2Q}	Read block select to out disable time (when pipelined register is disabled)	–	2.173	–	2.556	ns
t _{BLKMPW}	Read block select minimum pulse width	TBD	–	TBD	–	ns
t _{RSTREM}	Read asynchronous reset removal time (pipelined clock)	0	–	0	–	ns
	Read asynchronous reset removal time (non-pipelined clock)	0.03	–	0.036	–	ns
t _{RSTREC}	Read asynchronous reset recovery time (pipelined clock)	0.546	–	0.642	–	ns
	Read asynchronous reset recovery time (non-pipelined clock)	0.085	–	0.099	–	ns
t _{R2Q}	Read asynchronous reset to output propagation delay (with pipelined register enabled)	–	1.044	–	1.228	ns
	Read asynchronous reset to output propagation delay (with pipelined register disabled)	–	0.94	–	1.106	ns
t _{SRSTSU}	Read synchronous reset setup time	0.25	–	0.294	–	ns
t _{SRSTHD}	Read synchronous reset hold time	0.074	–	0.087	–	ns
t _{CCY}	Write clock period	1.49	–	1.752	–	ns
t _{CCLKMPWH}	Write clock minimum pulse width High	0.506	–	0.596	–	ns
t _{CCLKMPWL}	Write clock minimum pulse width Low	0.297	–	0.349	–	ns
t _{BLKCSU}	Write block setup time	0.332	–	0.39	–	ns
t _{BLKCHD}	Write block hold time	–0.009	–	–0.011	–	ns
t _{DINCSU}	Write input data setup time	0.017	–	0.02	–	ns
t _{DINCHD}	Write input data hold time	0.002	–	0.003	–	ns



Table 104 • uSRAM (RAM64x16) in 64x16 Mode (continued)

Parameter	Description	-1		Std.		Units
		Min.	Max.	Min.	Max.	
t _{ADDRCSU}	Write address setup time	0.012	–	0.015	–	ns
t _{ADDRCHD}	Write address hold time	–0.043	–	–0.05	–	ns
t _{WECSU}	Write enable setup time	0.32	–	0.377	–	ns
t _{WECHD}	Write enable hold time	–0.03	–	–0.035	–	ns

Table 105 • uSRAM (RAM128x9) in 128x9 Mode

Parameter	Description	-1		Std.		Units
		Min.	Max.	Min.	Max.	
t _{CY}	Read clock period	0.836	–	0.984	–	ns
t _{CLKMPWH}	Read clock minimum pulse width High	0.296	–	0.348	–	ns
t _{CLKMPWL}	Read clock minimum pulse width Low	0.324	–	0.382	–	ns
t _{PLCY}	Read pipeline clock period	1.989	–	2.34	–	ns
t _{PLCLKMPWH}	Read pipeline clock minimum pulse width High	0.259	–	0.305	–	ns
t _{PLCLKMPWL}	Read pipeline clock minimum pulse width Low	0.296	–	0.348	–	ns
t _{CLPL1}	Minimum pipeline clock low phase in order to prevent glitches with pipeline register in latch mode	TBD	–	TBD	–	ns
t _{CLK2Q}	Read access time with pipeline register	–	0.37	–	0.435	ns
	Read access time with pipeline register in latch mode	–	1.898	–	2.233	ns
	Read access time without pipeline register	TBD	–	TBD	–	ns
t _{ADDRSU}	Read address setup time in synchronous mode	0.294	–	0.345	–	ns
	Read address setup time in asynchronous mode	1.791	–	2.107	–	ns
t _{ADDRHD}	Read address hold time in synchronous mode	0.101	–	0.119	–	ns
	Read address hold time in asynchronous mode	0.082	–	0.096	–	ns
t _{RDENSU}	Read enable setup time	0.245	–	0.289	–	ns
t _{RDENHD}	Read enable hold time	0.074	–	0.087	–	ns
t _{BLKSU}	Read block select setup time (with pipeline register enabled)	1.901	–	2.237	–	ns
t _{BLKHD}	Read block select hold time (with pipelined register enabled)	0.001	–	0.001	–	ns
t _{BLK2Q}	Read block select to out disable time (when pipelined register is disabled)	–	2.211	–	2.601	ns
t _{BLKMPW}	Read block select minimum pulse width	TBD	–	TBD	–	ns
t _{RSTREM}	Read asynchronous reset removal time (pipelined clock)	0	–	0	–	ns
	Read asynchronous reset removal time (non-pipelined clock)	0.03	–	0.036	–	ns
t _{RSTREC}	Read asynchronous reset recovery time (pipelined clock)	0.546	–	0.642	–	ns
	Read asynchronous reset recovery time (non-pipelined clock)	0.085	–	0.099	–	ns
t _{R2Q}	Read asynchronous reset to output propagation delay (with pipelined register enabled)	–	1.042	–	1.226	ns
	Read asynchronous reset to output propagation delay (with pipelined register disabled)	–	0.94	–	1.106	ns
t _{SRSTSU}	Read synchronous reset setup time	0.25	–	0.294	–	ns
t _{SRSTHD}	Read synchronous reset hold time	0.074	–	0.087	–	ns
t _{CCY}	Write clock period	1.49	–	1.752	–	ns
t _{CCLKMPWH}	Write clock minimum pulse width High	0.506	–	0.596	–	ns
t _{CCLKMPWL}	Write clock minimum pulse width Low	0.297	–	0.349	–	ns
t _{BLKCSU}	Write block setup time	0.332	–	0.39	–	ns
t _{BLKCHD}	Write block hold time	–0.009	–	–0.011	–	ns
t _{DINCSU}	Write input data setup time	–0.025	–	–0.03	–	ns
t _{DINCHD}	Write input data hold time	0.002	–	0.003	–	ns



Table 105 • uSRAM (RAM128x9) in 128x9 Mode (continued)

Parameter	Description	-1		Std.		Units
		Min.	Max.	Min.	Max.	
t _{ADDRCSU}	Write address setup time	0.012	–	0.015	–	ns
t _{ADDRCHD}	Write address hold time	0.071	–	0.084	–	ns
t _{WECSU}	Write enable setup time	0.32	–	0.377	–	ns
t _{WECHD}	Write enable hold time	–0.03	–	–0.035	–	ns

Table 106 • uSRAM (RAM128x8) in 128x8 Mode

Parameter	Description	-1		Std.		Units
		Min.	Max.	Min.	Max.	
t _{CY}	Read clock period	0.836	–	0.984	–	ns
t _{CLKMPWH}	Read clock minimum pulse width High	0.296	–	0.348	–	ns
t _{CLKMPWL}	Read clock minimum pulse width Low	0.324	–	0.382	–	ns
t _{PLCY}	Read pipeline clock period	1.989	–	2.34	–	ns
t _{PLCLKMPWH}	Read pipeline clock minimum pulse width High	0.259	–	0.305	–	ns
t _{PLCLKMPWL}	Read pipeline clock minimum pulse width Low	0.296	–	0.348	–	ns
t _{CLPL1}	Minimum pipeline clock low phase in order to prevent glitches with pipeline register in latch mode	TBD	–	TBD	–	ns
t _{CLK2Q}	Read access time with pipeline register	–	0.37	–	0.435	ns
	Read access time with pipeline register in latch mode	–	1.898	–	2.233	ns
	Read access time without pipeline register	TBD	–	TBD	–	ns
t _{ADDRSU}	Read address setup time in synchronous mode	0.294	–	0.345	–	ns
	Read address setup time in asynchronous mode	1.791	–	2.107	–	ns
t _{ADDRHD}	Read address hold time in synchronous mode	0.101	–	0.119	–	ns
	Read address hold time in asynchronous mode	0.082	–	0.096	–	ns
t _{RDENSU}	Read enable setup time	0.245	–	0.289	–	ns
t _{RDENHD}	Read enable hold time	0.074	–	0.087	–	ns
t _{BLKSU}	Read block select setup time (with pipeline register enabled)	1.901	–	2.237	–	ns
t _{BLKHD}	Read block select hold time (with pipelined register enabled)	0.001	–	0.001	–	ns
t _{BLK2Q}	Read block select to out disable time (when pipelined register is disabled)	–	2.211	–	2.601	ns
t _{BLKMPW}	Read block select minimum pulse width	TBD	–	TBD	–	ns
t _{RSTREM}	Read asynchronous reset removal time (pipelined clock)	0	–	0	–	ns
	Read asynchronous reset removal time (non-pipelined clock)	0.03	–	0.036	–	ns
t _{RSTREC}	Read asynchronous reset recovery time (pipelined clock)	0.546	–	0.642	–	ns
	Read asynchronous reset recovery time (non-pipelined clock)	0.085	–	0.099	–	ns
t _{R2Q}	Read asynchronous reset to output propagation delay (with pipelined register enabled)	–	1.042	–	1.226	ns
	Read asynchronous reset to output propagation delay (with pipelined register disabled)	–	0.94	–	1.106	ns
t _{SRSTSU}	Read synchronous reset setup time	0.25	–	0.294	–	ns
t _{SRSTHD}	Read synchronous reset hold time	0.074	–	0.087	–	ns
t _{CCY}	Write clock period	1.49	–	1.752	–	ns
t _{CCLKMPWH}	Write clock minimum pulse width High	0.506	–	0.596	–	ns
t _{CCLKMPWL}	Write clock minimum pulse width Low	0.297	–	0.349	–	ns
t _{BLKCSU}	Write block setup time	0.332	–	0.39	–	ns
t _{BLKCHD}	Write block hold time	–0.009	–	–0.011	–	ns
t _{DINCSU}	Write input data setup time	–0.025	–	–0.03	–	ns
t _{DINCHD}	Write input data hold time	0.002	–	0.003	–	ns



Table 106 • uSRAM (RAM128x8) in 128x8 Mode (continued)

Parameter	Description	-1		Std.		Units
		Min.	Max.	Min.	Max.	
t _{ADDRCSU}	Write address setup time	0.012	–	0.015	–	ns
t _{ADDRCHD}	Write address hold time	0.071	–	0.084	–	ns
t _{WECSU}	Write enable setup time	0.32	–	0.377	–	ns
t _{WECHD}	Write enable hold time	–0.03	–	–0.035	–	ns

Table 107 • uSRAM (RAM256x4) in 256x4 Mode

Parameter	Description	-1		Std.		Units
		Min.	Max.	Min.	Max.	
t _{CY}	Read clock period	0.836	–	0.984	–	ns
t _{CLKMPWH}	Read clock minimum pulse width High	0.296	–	0.348	–	ns
t _{CLKMPWL}	Read clock minimum pulse width Low	0.324	–	0.382	–	ns
t _{PLCY}	Read pipeline clock period	1.989	–	2.34	–	ns
t _{PLCLKMPWH}	Read pipeline clock minimum pulse width High	0.259	–	0.305	–	ns
t _{PLCLKMPWL}	Read pipeline clock minimum pulse width Low	0.296	–	0.348	–	ns
t _{CLPL1}	Minimum pipeline clock low phase in order to prevent glitches with pipeline register in latch mode	TBD	–	TBD	–	ns
t _{CLK2Q}	Read access time with pipeline register	–	0.37	–	0.435	ns
	Read access time with pipeline register in latch mode	–	1.933	–	2.275	ns
	Read access time without pipeline register	TBD	–	TBD	–	ns
t _{ADDRSU}	Read address setup time in synchronous mode	0.294	–	0.345	–	ns
	Read address setup time in asynchronous mode	1.812	–	2.131	–	ns
t _{ADDRHD}	Read address hold time in synchronous mode	0.101	–	0.119	–	ns
	Read address hold time in asynchronous mode	0.082	–	0.096	–	ns
t _{RDENSU}	Read enable setup time	0.245	–	0.289	–	ns
t _{RDENHD}	Read enable hold time	0.074	–	0.087	–	ns
t _{BLKSU}	Read block select setup time (with pipeline register enabled)	1.901	–	2.237	–	ns
t _{BLKHD}	Read block select hold time (with pipelined register enabled)	0.001	–	0.001	–	ns
t _{BLK2Q}	Read block select to out disable time (when pipelined register is disabled)	–	2.249	–	2.646	ns
t _{BLKMPW}	Read block select minimum pulse width	–	–	–	–	ns
t _{RSTREM}	Read asynchronous reset removal time (pipelined clock)	–	–	–	–	ns
	Read asynchronous reset removal time (non-pipelined clock)	–	–	–	–	ns
t _{RSTREC}	Read asynchronous reset recovery time (pipelined clock)	0.546	–	0.642	–	ns
	Read asynchronous reset recovery time (non-pipelined clock)	0.085	–	0.099	–	ns
t _{R2Q}	Read asynchronous reset to output propagation delay (with pipelined register enabled)	–	1.042	–	1.226	ns
	Read asynchronous reset to output propagation delay (with pipelined register disabled)	–	0.94	–	1.106	ns
t _{SRSTSU}	Read synchronous reset setup time	0.25	–	0.294	–	ns
t _{SRSTHD}	Read synchronous reset hold time	0.074	–	0.087	–	ns
t _{CCY}	Write clock period	1.49	–	1.752	–	ns
t _{CCLKMPWH}	Write clock minimum pulse width High	0.506	–	0.596	–	ns
t _{CCLKMPWL}	Write clock minimum pulse width Low	0.297	–	0.349	–	ns
t _{BLKCSU}	Write block setup time	0.332	–	0.39	–	ns
t _{BLKCHD}	Write block hold time	–0.009	–	–0.011	–	ns
t _{DINCSU}	Write input data setup time	–0.025	–	–0.03	–	ns
t _{DINCHD}	Write input data hold time	0.002	–	0.003	–	ns



Table 107 • uSRAM (RAM256x4) in 256x4 Mode (continued)

Parameter	Description	-1		Std.		Units
		Min.	Max.	Min.	Max.	
t _{ADDRCSU}	Write address setup time	0.012	–	0.015	–	ns
t _{ADDRCHD}	Write address hold time	0.088	–	0.103	–	ns
t _{WECSU}	Write enable setup time	0.32	–	0.377	–	ns
t _{WECHD}	Write enable hold time	–0.03	–	–0.035	–	ns

Table 108 • uSRAM (RAM512x2) in 512x2 Mode

Parameter	Description	-1		Std.		Units
		Min.	Max.	Min.	Max.	
t _{CY}	Read clock period	0.836	–	0.984	–	ns
t _{CLKMPWH}	Read clock minimum pulse width High	0.296	–	0.348	–	ns
t _{CLKMPWL}	Read clock minimum pulse width Low	0.324	–	0.382	–	ns
t _{PLCY}	Read pipeline clock period	1.989	–	2.34	–	ns
t _{PLCLKMPWH}	Read pipeline clock minimum pulse width High	0.259	–	0.305	–	ns
t _{PLCLKMPWL}	Read pipeline clock minimum pulse width Low	0.296	–	0.348	–	ns
t _{CLPL1}	Minimum pipeline clock low phase in order to prevent glitches with pipeline register in latch mode	TBD	–	TBD	–	ns
t _{CLK2Q}	Read access time with pipeline register	–	0.37	–	0.435	ns
	Read access time with pipeline register in latch mode	–	1.954	–	2.299	ns
	Read access time without pipeline register	TBD	–	TBD	–	ns
t _{ADDRSU}	Read address setup time in synchronous mode	0.294	–	0.345	–	ns
	Read address setup time in asynchronous mode	1.849	–	2.175	–	ns
t _{ADDRHD}	Read address hold time in synchronous mode	0.131	–	0.154	–	ns
	Read address hold time in asynchronous mode	0.092	–	0.108	–	ns
t _{RDENSU}	Read enable setup time	0.245	–	0.289	–	ns
t _{RDENHD}	Read enable hold time	0.074	–	0.087	–	ns
t _{BLKSU}	Read block select setup time (with pipeline register enabled)	1.901	–	2.237	–	ns
t _{BLKHD}	Read block select hold time (with pipelined register enabled)	0.001	–	0.001	–	ns
t _{BLK2Q}	Read block select to out disable time (when pipelined register is disabled)	–	2.272	–	2.673	ns
t _{BLKMPW}	Read block select minimum pulse width	TBD	–	TBD	–	ns
t _{RSTREM}	Read asynchronous reset removal time (pipelined clock)	0	–	0	–	ns
	Read asynchronous reset removal time (non-pipelined clock)	0.03	–	0.036	–	ns
t _{RSTREC}	Read asynchronous reset recovery time (pipelined clock)	0.546	–	0.642	–	ns
	Read asynchronous reset recovery time (non-pipelined clock)	0.085	–	0.099	–	ns
t _{R2Q}	Read asynchronous reset to output propagation delay (with pipelined register enabled)	–	1.041	–	1.225	ns
	Read asynchronous reset to output propagation delay (with pipelined register disabled)	–	0.937	–	1.102	ns
t _{SRSTSU}	Read synchronous reset setup time	0.25	–	0.294	–	ns
t _{SRSTHD}	Read synchronous reset hold time	0.074	–	0.087	–	ns
t _{CCY}	Write clock period	1.49	–	1.752	–	ns
t _{CCLKMPWH}	Write clock minimum pulse width High	0.506	–	0.596	–	ns
t _{CCLKMPWL}	Write clock minimum pulse width Low	0.297	–	0.349	–	ns
t _{BLKCSU}	Write block setup time	0.332	–	0.39	–	ns
t _{BLKCHD}	Write block hold time	–0.009	–	–0.011	–	ns
t _{DINCSU}	Write input data setup time	–0.025	–	–0.03	–	ns
t _{DINCHD}	Write input data hold time	0.002	–	0.003	–	ns



Table 108 • uSRAM (RAM512x2) in 512x2 Mode (continued)

Parameter	Description	-1		Std.		Units
		Min.	Max.	Min.	Max.	
t _{ADDRCSU}	Write address setup time	0.012	–	0.015	–	ns
t _{ADDRCHD}	Write address hold time	0.098	–	0.115	–	ns
t _{WECSU}	Write enable setup time	0.32	–	0.377	–	ns
t _{WECHD}	Write enable hold time	–0.03	–	–0.035	–	ns

Table 109 • uSRAM (RAM1024x1) in 1024x1 Mode

Parameter	Description	-1		Std.		Units
		Min.	Max.	Min.	Max.	
t _{CY}	Read clock period	0.836	–	0.984	–	ns
t _{CLKMPWH}	Read clock minimum pulse width High	0.296	–	0.348	–	ns
t _{CLKMPWL}	Read clock minimum pulse width Low	0.324	–	0.382	–	ns
t _{PLCY}	Read pipeline clock period	1.989	–	2.34	–	ns
t _{PLCLKMPWH}	Read pipeline clock minimum pulse width High	0.259	–	0.305	–	ns
t _{PLCLKMPWL}	Read pipeline clock minimum pulse width Low	0.296	–	0.348	–	ns
t _{CLPL1}	Minimum pipeline clock low phase in order to prevent glitches with pipeline register in latch mode	TBD	–	TBD	–	ns
t _{CLK2Q}	Read access time with pipeline register	–	0.37	–	0.435	ns
	Read access time with pipeline register in latch mode	–	1.984	–	2.335	ns
	Read access time without pipeline register	TBD	–	TBD	–	ns
t _{ADDRSU}	Read address setup time in synchronous mode	0.294	–	0.345	–	ns
	Read address setup time in asynchronous mode	1.88	–	2.212	–	ns
t _{ADDRHD}	Read address hold time in synchronous mode	0.131	–	0.154	–	ns
	Read address hold time in asynchronous mode	0.092	–	0.108	–	ns
t _{RDENSU}	Read enable setup time	0.245	–	0.289	–	ns
t _{RDENHD}	Read enable hold time	0.074	–	0.087	–	ns
t _{BLKSU}	Read block select setup time (with pipeline register enabled)	1.901	–	2.237	–	ns
t _{BLKHD}	Read block select hold time (with pipelined register enabled)	0.001	–	0.001	–	ns
t _{BLK2Q}	Read block select to out disable time (when pipelined register is disabled)	–	2.299	–	2.705	ns
t _{BLKMPW}	Read block select minimum pulse width	TBD	–	TBD	–	ns
t _{RSTREM}	Read asynchronous reset removal time (pipelined clock)	0	–	0	–	ns
	Read asynchronous reset removal time (non-pipelined clock)	0.03	–	0.036	–	ns
t _{RSTREC}	Read asynchronous reset recovery time (pipelined clock)	0.546	–	0.642	–	ns
	Read asynchronous reset recovery time (non-pipelined clock)	0.085	–	0.099	–	ns
t _{R2Q}	Read asynchronous reset to output propagation delay (with pipelined register enabled)	–	1.041	–	1.225	ns
	Read asynchronous reset to output propagation delay (with pipelined register disabled)	–	0.824	–	0.97	ns
t _{SRSTSU}	Read synchronous reset setup time	0.25	–	0.294	–	ns
t _{SRSTHD}	Read synchronous reset hold time	0.074	–	0.087	–	ns
t _{CCY}	Write clock period	1.49	–	1.752	–	ns
t _{CCLKMPWH}	Write clock minimum pulse width High	0.506	–	0.596	–	ns
t _{CCLKMPWL}	Write clock minimum pulse width Low	0.297	–	0.349	–	ns
t _{BLKCSU}	Write block setup time	0.332	–	0.39	–	ns
t _{BLKCHD}	Write block hold time	–0.009	–	–0.011	–	ns
t _{DINCSU}	Write input data setup time	–0.089	–	–0.104	–	ns
t _{DINCHD}	Write input data hold time	0.002	–	0.003	–	ns



Table 109 • uSRAM (RAM1024x1) in 1024x1 Mode (continued)

Parameter	Description	-1		Std.		Units
		Min.	Max.	Min.	Max.	
t _{ADDRCSU}	Write address setup time	0.012	–	0.015	–	ns
t _{ADDRCHD}	Write address hold time	0.098	–	0.115	–	ns
t _{WECSU}	Write enable setup time	0.32	–	0.377	–	ns
t _{WECHD}	Write enable hold time	–0.03	–	–0.035	–	ns

On-Chip Oscillators

Table 110 through Table 112 on page 102 describe the electrical characteristics of the available on-chip oscillators in SmartFusion2 devices.

Table 110 • Electrical Characteristics of the Crystal Oscillator

Parameter	Description	Condition	Min.	Typ.	Max.	Units	Notes
FXTAL	Operating frequency		–	32	–	KHz	
ACCXTAL	Accuracy	High Gain Mode (20 MHz)			0.0047	%	
		Medium Gain Mode (2 MHz)			0.00105	%	
		Low Gain Mode (32 KHz)			0.000429	%	
CYCXTAL	Output duty cycle	High Gain Mode (20 MHz)		1	3	%	
		Medium Gain Mode (2 MHz)		1	3	%	
		Low Gain Mode (32 KHz)		1	3	%	
JITPERXTAL	Output Period Jitter (peak-to-peak)	High Gain Mode (20 MHz)		200	300	ps	
		Medium Gain Mode (2 MHz)		1	5	ns	
		Low Gain Mode (32 KHz)		150	300	ns	
JITCYCXTAL	Output Cycle-to-Cycle Jitter (peak-to-peak)	High Gain Mode (20 MHz)		200	300	ps	
		Medium Gain Mode (2 MHz)		1	5	ns	
		Low Gain Mode (32 KHz)		150	300	ns	
IDYNXTAL	Operating current	High Gain Mode (20 MHz)			1.5	mA	
		Medium Gain Mode (2 MHz)			0.3	mA	
		Low Gain Mode (32 KHz)			0.044	mA	
PSRRXTAL	Power supply noise tolerance		TBD	TBD	TBD	Vp-p	
VIHXTAL	Input logic level High		0.9 x VPP			V	
VILXTAL	Input logic level Low				0.1 x VPP	V	
SUXTAL	Startup time (w.r.t. stable oscillator output)	High Gain Mode (20 MHz)			0.8	μs	
		Medium Gain Mode (2 MHz)			4.5	μs	
		Low Gain Mode (32 KHz)			115	μs	

Table 111 • Electrical Characteristics of the 50 MHz RC Oscillator

Parameter	Description	Condition	Min.	Typ.	Max.	Units	Notes
F50RC	Operating frequency		–	50	–	MHz	
ACC50RC	Accuracy			1	4	%	
CYC50RC	Output duty cycle			1	3	%	
JIT50RC	Output jitter	Period jitter		200	300	ps	
		Cycle-to-cycle jitter		200	300	ps	
IDYN50RC	Operating current		TBD	6.5	TBD	mA	
PSRR50RC	Power supply noise tolerance		TBD	TBD	TBD	Vp-p	



Table 112 • Electrical Characteristics of the 1 MHz RC Oscillator

Parameter	Description	Condition	Min.	Typ.	Max.	Units	Notes
F1RC	Operating frequency		–	1	–	MHz	
ACC1RC	Accuracy			1	3	%	
CYC1RC	Output duty cycle			1	3	%	
JIT1RC	Output jitter	Period jitter		10	20	ns	
		Cycle-to-cycle jitter		10	20	ns	
IDYN1RC	Operating current		TBD	0.1	TBD	mA	
PSRR1RC	Power supply noise tolerance		TBD	TBD	TBD	Vp-p	
SU1RC	Startup time				17	μs	

Clock Conditioning Circuits (CCC)

Table 113 • SmartFusion2 CCC/PLL Specification

Parameter	Minimum	Typical	Maximum	Units	Notes	
Clock conditioning circuitry input frequency f_{IN_CCC}	1		200	MHz		
Clock conditioning circuitry output frequency f_{OUT_CCC}	20		400	MHz		
Delay increments in programmable delay blocks		75	100	ps		
Number of programmable values in each programmable delay block			64			
Acquisition time		70	100	μ s		
Tracking jitter		TBD		ns		
Output duty cycle	48		52	%		
Feedback delay			8	ns		
CCC output peak-to-peak period jitter F_{CCC_OUT}	Maximum peak-to-peak period jitter					
	SSO = 0	$0 < SSO \leq 2$	$SSO \leq 4$	$SSO \leq 8$	$SSO \leq 16$	
	FG896	FG896	FG896	FG896	FG896	
20 MHz to 100 MHz	110 ps	150 ps				% f_{OUT_CCC}
100 MHz to 400 MHz	120 ps	150 ps		170 ps		% f_{OUT_CCC}
Spread Spectrum Characteristics						
Modulation frequency range			25	35	50	kHz
Modulation depth range			0		1.5	%
Modulation depth control				0.5		%

JTAG

Table 114 • JTAG 1532

Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	-1	Std.	Units	Notes
t_{DISU}	Test data input setup time			ns	
t_{DIHD}	Test data input hold time			ns	
t_{TMSSU}	Test mode select setup time			ns	
t_{TMDHD}	Test mode select hold time			ns	
t_{TCK2Q}	Clock to Q (data out)			ns	
t_{RSTB2Q}	Reset to Q (data out)			ns	
F_{TCKMAX}	TCK maximum frequency			MHz	
$t_{TRSTREM}$	ResetB removal time			ns	
$t_{TRSTREC}$	ResetB recovery time			ns	
$t_{TRSTMPW}$	ResetB minimum pulse			ns	

Note: *For specific junction temperature and voltage supply levels, refer to Table 7 on page 15 for derating values.



Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given are for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_x_CLK. For timing parameter definitions, refer to [Figure 14 on page 105](#).

Table 115 • SPI Characteristics

Commercial Case Conditions: T_J = 85°C, VDD = 1.425 V, –1 Speed Grade

Symbol	Description and Condition	M2S050	M2S025	M2S010	Units	Notes
sp1	SPI_x_CLK minimum period					
	SPI_x_CLK = PCLK/2	12			ns	
	SPI_x_CLK = PCLK/4	24.1			ns	
	SPI_x_CLK = PCLK/8	48.2			ns	
	SPI_x_CLK = PCLK/16	0.1			µs	
	SPI_x_CLK = PCLK/32	0.19			µs	
	SPI_x_CLK = PCLK/64	0.39			µs	
	SPI_x_CLK = PCLK/128	0.77			µs	
sp2	SPI_x_CLK minimum pulse width High					
	SPI_x_CLK = PCLK/2	6			ns	
	SPI_x_CLK = PCLK/4	12.05			ns	
	SPI_x_CLK = PCLK/8	24.1			ns	
	SPI_x_CLK = PCLK/16	0.05			µs	
	SPI_x_CLK = PCLK/32	0.095			µs	
	SPI_x_CLK = PCLK/64	0.195			µs	
	SPI_x_CLK = PCLK/128	0.385			µs	
sp3	SPI_x_CLK minimum pulse width Low					
	SPI_x_CLK = PCLK/2	6			ns	
	SPI_x_CLK = PCLK/4	12.05			ns	
	SPI_x_CLK = PCLK/8	24.1			ns	
	SPI_x_CLK = PCLK/16	0.05			µs	
	SPI_x_CLK = PCLK/32	0.095			µs	
	SPI_x_CLK = PCLK/64	0.195			µs	
	SPI_x_CLK = PCLK/128	0.385			µs	
sp4	SPI_x_CLK, SPI_x_DO, SPI_x_SS rise time (10%-90%)	TBD			ns	1
sp5	SPI_x_CLK, SPI_x_DO, SPI_x_SS fall time (10%-90%)	TBD			ns	1
sp6	Data from master (SPI_x_DO) setup time	1	1	1	pclk cycles	2
sp7	Data from master (SPI_x_DO) hold time	1	1	1	pclk cycles	2

Notes:

1. These values are provided for a load of 5 pF. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: <http://www.microsemi.com/soc/download/ibis/default.aspx>.
2. For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the *SmartFusion2 ARM Cortex-M3 and Microcontroller Subsystem User's Guide*.

Table 115 • SPI Characteristics

Commercial Case Conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.425\text{ V}$, -1 Speed Grade (continued)

Symbol	Description and Condition	M2S050	M2S025	M2S010	Units	Notes
sp8	SPI_x_DI setup time	1	1	1	pclk cycles	2
sp9	SPI_x_DI hold time	1	1	1	pclk cycles	2

Notes:

1. These values are provided for a load of 5 pF. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: <http://www.microsemi.com/soc/download/ibis/default.aspx>.
2. For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the SmartFusion2 ARM Cortex-M3 and Microcontroller Subsystem User's Guide.

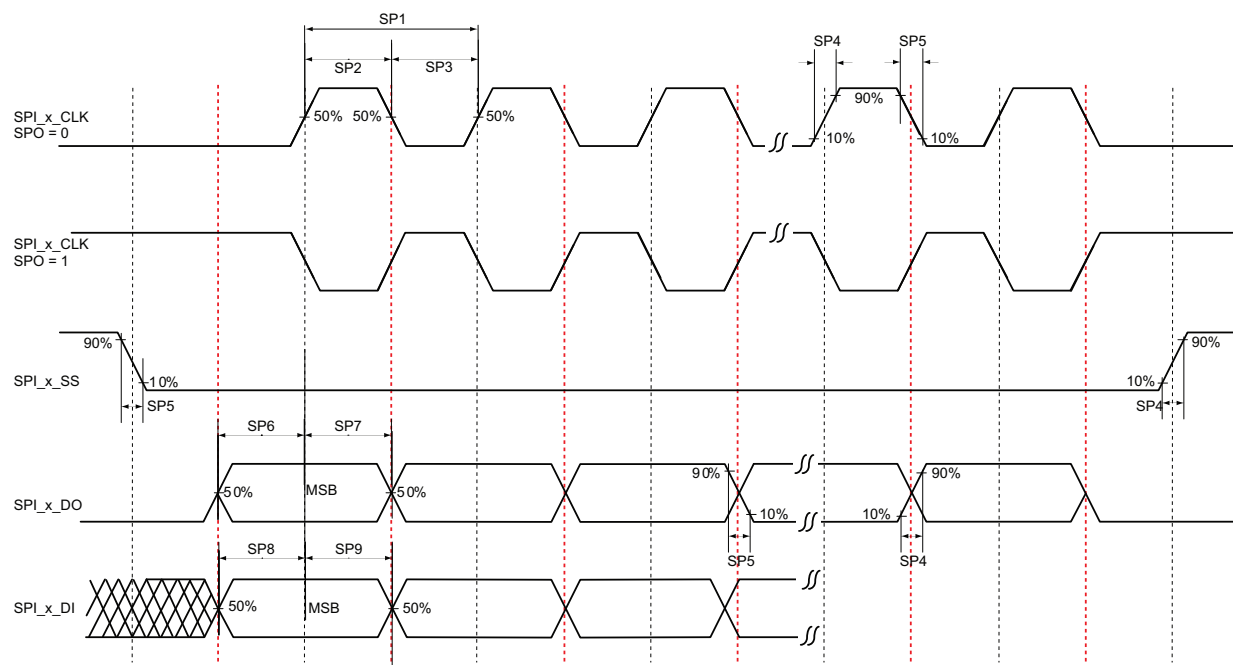


Figure 14 • SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)



Inter-Integrated Circuit (I²C) Characteristics

This section describes the DC and switching of the I²C interface. Unless otherwise noted, all output characteristics given are for a 100 pF load on the pins. For timing parameter definitions, refer to Figure 15 on page 107.

Table 116 • I²C Characteristics

Commercial Case Conditions: T_J = 85°C, VDD = 1.14 V, –1 Speed Grade

Parameter	Definition	Condition	Min.	Typ.	Max.	Units	Notes
VIL	Input low voltage	Refer to the "Single-Ended I/O Standards" section on page 22 for more information. I/O standard used for illustration: MSIO bank – LVTTTL 8 mA low drive.	–0.3	–	0.8	V	
VIH	Input high voltage	Refer to the "Single-Ended I/O Standards" section on page 22 for more information. I/O standard used for illustration: MSIO bank – LVTTTL 8 mA low drive.	2	–	3.45	V	
VHYS	Hysteresis of Schmitt triggered inputs for VDDI > 2 V	Refer to Table 13 on page 21 for more information.	0.05 * VDDI	–	–	V	
IIL	Input current high	Refer to the "Single-Ended I/O Standards" section on page 22 for more information.	–	–	10	μA	
IIH	Input current low	Refer to the "Single-Ended I/O Standards" section on page 22 for more information.	–	–	10	μA	
VOL	Maximum output voltage low (open drain) at 3 mA sink current for VDDI > 2 V	Refer to the "Single-Ended I/O Standards" section on page 22 for more information. I/O standard used for illustration: MSIO bank – LVTTTL 8 mA low drive.	–	–	0.4	V	
Cin	Pin capacitance	VIN = 0, f = 1.0 MHz	–	–	10	pF	
t _{oF}	Output fall time from VIHMin to VILMax	VIHMin to VILMax, Cload = 400 pF	–	–	–	ns	1
t _{oR}	Output rise time from VILMax to VIHMin	VILMax to VIHMin, Cload = 400 pF	–	–	–	ns	1
Rpull-up	Output buffer maximum pull-down resistance		–	–	–	Ohms	2
Rpull-down	Output buffer maximum pull-up resistance		–	–	–	Ohms	2
Dmax	Maximum data rate	Fast mode	–	–	400	Kbps	
		Standard mode	–	–	100	Kbps	
t _{FILT}	Pulse width of spikes which must be suppressed by the input filter	Fast mode	–	50	–	ns	

Notes:

1. These values are provided for a load of 400 pF. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: <http://www.microsemi.com/soc/download/ibis/default.aspx>.
2. These maximum values are provided for information only. Minimum output buffer resistance values depend on VCCxxxIOBx, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: <http://www.microsemi.com/soc/download/ibis/default.aspx>.

Table 117 • I²C Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V

Parameter	Definition	Conditions	-1		Std.		Units	Notes
			Min.	Max.	Min.	Max.		
t _{LOW}	Low period of I2C_x_SCL	–	1	–	1	–	pclk cycles	
t _{HIGH}	High period of I2C_x_SCL	–	1	–	1	–	pclk cycles	
t _{HD;STA}	START hold time	–	1	–	1	–	pclk cycles	
t _{SU;STA}	START setup time	–	1	–	1	–	pclk cycles	
t _{HD;DAT}	DATA hold time	–	1	–	1	–	pclk cycles	
t _{SU;DAT}	DATA setup time	–	1	–	1	–	pclk cycles	
t _{SU;STO}	STOP setup time	–	1	–	1	–	pclk cycles	

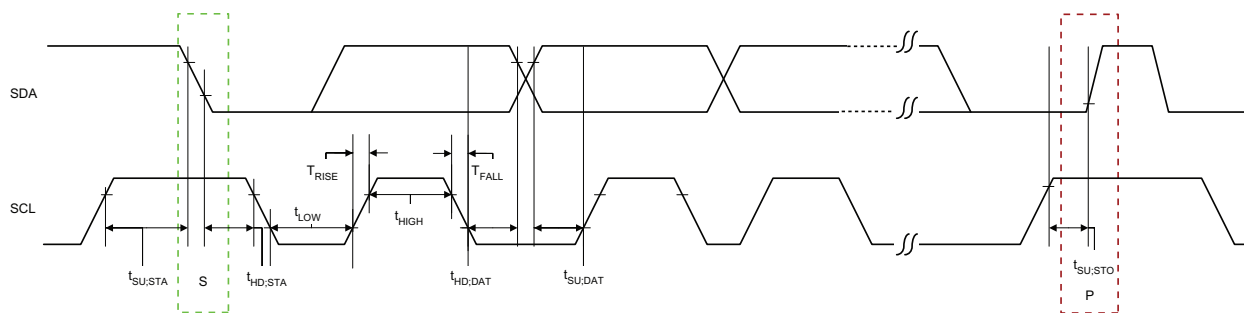


Figure 15 • I²C Timing Parameter Definition



Mathblock Timing Characteristics

The fundamental building block in any digital signal processing algorithm is the multiply-accumulate function. Each SmartFusion mathblock supports 18x18 signed multiplication, dot product, and built-in addition, subtraction, and accumulation units to combine multiplication results efficiently.

Table 118 • Mathblocks with All Registers Used

Parameter	Description	-1		Std.		Units	Notes
		Min.	Max.	Min.	Max.		
t _{MISU}	Input, control register setup time	1.347		1.585		ns	
t _{MIHD}	Input, control register hold time	1.768		2.08		ns	
t _{MOCDINSU}	CDIN input setup time	0.195		0.23		ns	
t _{MOCDINHD}	CDIN input hold time	0.084		0.099		ns	
t _{MSRSTENSU}	Synchronous reset/enable setup time	-0.441		-0.519		ns	
t _{MSRSTENHD}	Synchronous reset/enable hold time	0.012		0.014		ns	
t _{MARSTREM}	Asynchronous reset removal time	0		0		ns	
t _{MARSTREC}	Asynchronous reset recovery time	0.093		0.109		ns	
t _{MOCQ}	Output register clock to out delay		0.244		0.287	ns	
t _{MCLKMP}	CLK minimum period	2.363		2.78		ns	

Table 119 • Mathblock with Input Bypassed and Output Registers Used

Parameter	Description	-1		Std.		Units	Notes
		Min.	Max.	Min.	Max.		
t _{MOSU}	Output register setup time	2.415		2.841		ns	
t _{MOHD}	Output register hold time	1.768		2.08		ns	
t _{MOCDINSU}	CDIN input setup time	0.121		0.143		ns	
t _{MOCDINHD}	CDIN input hold time	-0.467		-0.549		ns	
t _{MSRSTENSU}	Synchronous reset/enable setup time	-0.441		-0.519		ns	
t _{MSRSTENHD}	Synchronous reset/enable hold time	0.012		0.014		ns	
t _{MARSTREM}	Asynchronous reset removal time	0		0		ns	
t _{MARSTREC}	Asynchronous reset recovery time	0.015		0.018		ns	
t _{MOCQ}	Output register clock to out delay		0.244		0.287	ns	
t _{MCLKMP}	CLK minimum period	2.293		2.698		ns	

Table 120 • Mathblock with Input Register Used and Output in Bypass Mode

Parameter	Description	-1		Std.		Units	Notes
		Min.	Max.	Min.	Max.		
t _{MISU}	Input register setup time	0.157		0.185		ns	
t _{MIHD}	Input register hold time	0.195		0.23		ns	
t _{MSRSTENSU}	Synchronous reset/enable setup time	0.084		0.099		ns	
t _{MSRSTENHD}	Synchronous reset/enable hold time	-0.013		-0.015		ns	
t _{MARSTREM}	Asynchronous reset removal time	-0.005		-0.006		ns	
t _{MARSTREC}	Asynchronous reset recovery time	0.093		0.109		ns	
t _{MICQ}	Input register clock to output delay		2.652		3.12	ns	
t _{MCDIN2Q}	CDIN to output delay		2.053		2.416	ns	

Table 121 • Mathblock with Input and Output in Bypass Mode

Parameter	Description	-1		Std.		Units	Notes
		Min.	Max.	Min.	Max.		
t _{MIQ}	Input to output delay		2.704		3.181	ns	
t _{MCDIN2Q}	CDIN to output delay		2.053		2.416	ns	

Table 122 • Flash*Freeze Entry and Exit Times

Symbols	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
TFF_ENTRY	Entry Time	eNVM and MSS PLL=ON			150	us	
		eNVM and MSS PLL=OFF			200	us	
TFF_EXIT	Exit Time with Respect to MSS PLL Lock	eNVM and MSS PLL=ON during F*F			100	us	
		eNVM=ON and MSS PLL=OFF during F*F and MSS PLL turned back on at exit			120	us	
		eNVM and MSS PLL=OFF during F*F and both are turned back on at exit			200	us	
		eNVM=OFF and MSS PLL=ON during F*F and eNVM turned back on at exit			200	us	
	Exit Time with Respect to Fabric PLL Lock	eNVM and MSS PLL=ON during F*F			1.5	μs	
		eNVM and MSS PLL=OFF during F*F and both are turned back on at exit			1.5	μs	
	Exit Time with Respect to Fabric buffer output	eNVM and MSS PLL=ON during F*F			15	us	
		eNVM and MSS PLL=OFF during F*F and both are turned back on at exit			55	us	



PCIe Electrical and Timing AC and DC Characteristics

PCIe is a high speed, packet-based, point-to-point, low pin count, serial interconnect bus. The SmartFusion2 family has two hard high-speed serial interface blocks. Each SERDES block contains a PCIe system block. The PCIe system is connected to the SERDES block.

Table 123 • Transmitter Parameters

Parameter	Description	Min.	Typ.	Max.	Units	Notes
VTX-DIFF-PP	Differential swing PCIe Gen 1 and 2	0.8	–	1.2	mV	
VTX-CM-AC-P	Output common mode voltage PCIe Gen 1	–	–	20	mV	
VTX-CM-AC-PP	Output common mode voltage PCIe Gen 2	–	–	100	mV	
VTX-RISE-FALL	Rise and fall time (20% to 80%) PCIe Gen 1	0.125	–	–	UI	
	Rise and fall time (20% to 80%) PCIe Gen 2	0.15	–	–	UI	
ZTX-DIFF-DC	Output impedance – differential	80	–	120	ohm	
LTX-SKEW	Lane-to-lane TX skew within a SERDES block PCIe Gen 1	–	–	500 ps + 2 UI	ps	
	Lane-to-lane TX skew within a SERDES block PCIe Gen 2	–	–	500 ps +4 UI	ps	
RLTX-DIFF	Return loss differential mode PCIe Gen 1	–10	–	–	dB	
	Return loss differential mode PCIe Gen 2	–10 (min.) 0.05 – 1.25 GHz – 8 (min.) 1.25 – 2.5 GHz			dB	
RLTX-CM	Return loss common mode PCIe Gen 1 and 2	–6	–	–	dB	
	Transmit PLL lock time from reset	–	–	10	µs	

Table 124 • Receiver Parameters

Parameter	Description	Min	Typ	Max	Units	Notes
VRX-DIFF-PP-CC	Input levels PCIe Gen 1	0.175	–	1.2	mV	
	Input levels PCIe Gen 2	0.12	–	1.2	mV	
VRX-CM-DC-P	Input common mode range (DC coupled) Note: PCIe standard mandates AC coupling	NA	NA	NA	-	
VRX-CM-AC-P	Input common mode range (AC coupled)	–	–	150	mV	
VRX-DIFF-PP-CC	Differential input sensitivity PCIe Gen 1	0.175	–	–	mV	
	Differential input sensitivity PCIe Gen 2	0.12	–	–	mV	
ZRX-DIFF-DC	Differential input termination	80	100	120	Ohms	
REXT	External calibration resistor	1,188	1,200	1,212	Ohms	
	CDR relock time from reset	–	–	15	µs	
RLRX-DIFF	Return loss differential mode PCIe Gen 1	–10	–	–	dB	
	Return loss differential mode PCIe Gen 2	–10 (min.) 0.05 – 1.25 GHz – 8 (min.) 1.25 – 2.5 GHz			dB	
RLRX-CM	Return loss common mode PCIe Gen 1 and 2	–6	–	–	dB	
	CID limit (set by 8B/10B coding, not the receiver PLL)			4	UI	
VRX-IDLE-DET-DIFF-PP	Signal detect limit	65		175	mV	

Table 125 • SERDES Reference Clock AC Specifications

Symbols	Description	Conditions	Min.	Typ.	Max.	Units	Notes
FREFCLK	Reference Clock Frequency		100		160	MHz	
TRISE	Reference Clock Rise Time		0.6		4	V/ns	
TFALL	Reference Clock Fall Time		0.6		4	V/ns	
TCYC	Reference Clock Duty Cycle		40		60	%	
Mmrefclk	Reference Clock Mismatch		-300		300	ppm	
SSCref	Reference Spread Spectrum Clock		0		5000	ppm	



Datasheet Information

List of Changes

The following table lists critical changes that were made in each revision of the datasheet.

Revision	Changes	Page
Revision 4 (June 2013)	The M2S050T device status was changed from Advance to Preliminary in the "SmartFusion2 Device Status" table (SAR 47026).	1
	VDD_2V5 and PLL0_PLL1_MDDR_VDDA were added to Table 1 • Absolute Maximum Ratings and Table 2 • Recommended Operating Conditions . The minimum for FDDR_PLL_VDDA was corrected from –0.5 to –0.3 (SARs 47054, 47055, and 48490).	9, 10
	VDD_2V5, PLL0_PLL1_MDDR_VDDA, and programming junction temperature were added to Table 2 • Recommended Operating Conditions (SARs 45620, 47054, 47055).	10
	The "Power Supply Sequencing and Power-On Reset (Commercial and Industrial)" section will become part of a user's guide. The sections "I/O Power", "Power Consumption of Various Internal Resources", and "Power Methodology" were moved to the user's guide (SAR 45904).	N/A
	Information was added to Table 4 • Package Thermal Resistance (SAR 47026).	12
	The Power Methodology section was deleted. This information will become part of a new user's guide (SAR 46973).	N/A
	Table 5 • Quiescent Supply Current Characteristics and Table 6 • Quiescent Supply Current are new (SARs 45673 and 48135).	14
	Updated Figure 1 • Timing Model (SAR 47527).	15
	Values were added to Table 8 • Timing Model Parameters (SAR 47026).	16
	Values were updated for Table 7 • Average Temperature and Voltage Derating Factors for Fabric Timing Delays (SARs 47026 and 48280).	15
	Timing tables in the "User I/O Characteristics" section were updated extensively with available data (SAR 47026).	17
	Updated the Min value of VIH(dc) for the SSTL2 DC Input Voltage Specifications in Table 47 • DDR1/SSTL2 DC Voltage Specification (SAR 48244).	43
	Diagrams in the "I/O Register Specifications" section are new (SAR 47026).	66
	A reference to the <i>SmartFusion2 Macro Library Guide</i> was added.	77
	Updated Table 90 • Input DDR Propagation Delays , Table 91 • Output DDR Propagation Delays , Table 92 • Combinatorial Cell Propagation Delays , and Table 93 • Register Delays (SAR 48280).	73, 76, 77, and 79
	Updated Table 110 • Electrical Characteristics of the Crystal Oscillator and Table 111 • Electrical Characteristics of the 50 MHz RC Oscillator (SAR 44895). Table 111 • Electrical Characteristics of the 50 MHz RC Oscillator was renamed to remove the reference to a 25 MHz oscillator (SAR 44859).	101 and 101
The "Mathblock Timing Characteristics" section and "PCIe Electrical and Timing AC and DC Characteristics" section are new (SARs 40276)	108, 110	
Added Table 122 • Flash*Freeze Entry and Exit Times (SAR 46455) and Table 125 • SERDES Reference Clock AC Specifications .	109	

Revision	Changes	Page
Revision 3 (February 2013)	SmartFusion2 product brief and pin information has been removed from the datasheet and published in separate documents: SmartFusion2 Product Brief and SmartFusion2 Pin Descriptions (SAR 45184).	N/A
Revision 2 (February 2013)	Table 1 • Absolute Maximum Ratings and Table 2 • Recommended Operating Conditions were updated with the new pin names and latest values (SAR 45081).	9, 10
	The storage temperature minimum value was added to Table 1 • Absolute Maximum Ratings , including a note with references to additional tables (SAR 44887).	9
	In EQ 1 , $T_J - \theta_A$ was corrected to $T_J - T_A$ (SAR 44109).	11
	Timing tables were updated with respect to slew and configuration. AC and DC specifications were placed in separate tables. Values were added to replace TBD in a number of tables in the "User I/O Characteristics" section (SAR 44471).	17
	The termination scheme for the differential I/O test setup in the "Output Buffer and AC Loading" section was corrected (SAR 43591).	18
	The worst commercial-case conditions for Table 22 • LVCMOS 2.5 V Receiver Characteristics were changed from VDDI = 3.0 V to VDDI = 2.375 V (SAR 44471).	25
	The following tables were revised to remove typical and minimum Fmax values and change maximum Fmax values (SAR 44471): Table 63 • LVDS DC Voltage Specification Table 77 • Mini-LVDS DC Voltage Specification Table 81 • RSDS DC Voltage Specification	56 61 63
	Table 98 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 2K × 9 through Table 101 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 16K × 1 are new (SAR 44471).	82 to 85
	Table 103 • uSRAM (RAM64x18) in 64x18 Mode through Table 108 • uSRAM (RAM512x2) in 512x2 Mode are new (SAR 44471).	87 to 97
Revision 1 (January 2013)	Table 1 • Absolute Maximum Ratings is new. In Table 2 • Recommended Operating Conditions , the expression "VDDIO" in the values for VREFx was corrected to "VDDIx." VCCENVM was corrected to VPPNVM (SAR 42461). VDDIx was defined differently for different types of I/O banks (SAR 43850).	9, 10
	The "Power Supply Sequencing and Power-On Reset (Commercial and Industrial)" section was revised to correct the available ramp rate options from "50 μ s, 100 μ s, 1 ms, and 100 ms" to "50 μ s, 1 ms, 10 ms, and 100 ms." Each selection represents the maximum ramp rate to apply to VDD and VPP. The user can set the ramp rate setting using Libero SOC (SARs 41970, 42401).	11
	The units for input leakage current (IIL/IIH) were corrected from mA to μ A in the DC voltage tables (SAR 43848).	22 to 34
	A note to reference IBIS models for a detailed I/V curve was added to transmitter drive strength tables for LVTTTL/LVCMOS 3.3 V through LVCMOS 1.2 V (SAR 42171). For more information, refer to the IBIS Models: Background and Usage application note.	23 to 34

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in the "SmartFusion2 Device Status" table on page 1 is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Production

This version contains information that is considered to be final.

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