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# Solid-State Modulator Testing

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## DISCLAIMER



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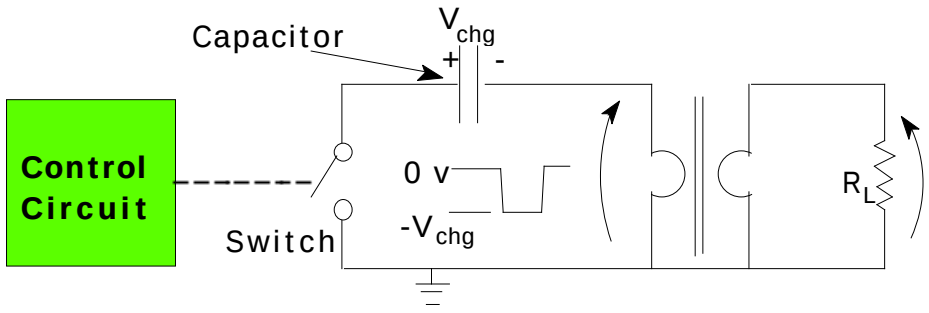
Subject: Solid-State Modulator Testing

In this note is reported the testing of the pre-production version of a solid-state adder type modulator. In this configuration, the adder consists of transformers that are driven by an array of MOSFET switches that are connected in parallel but not in series; i.e. the input voltage on the transformer is limited to the maximum voltage rating on the MOSFETs.

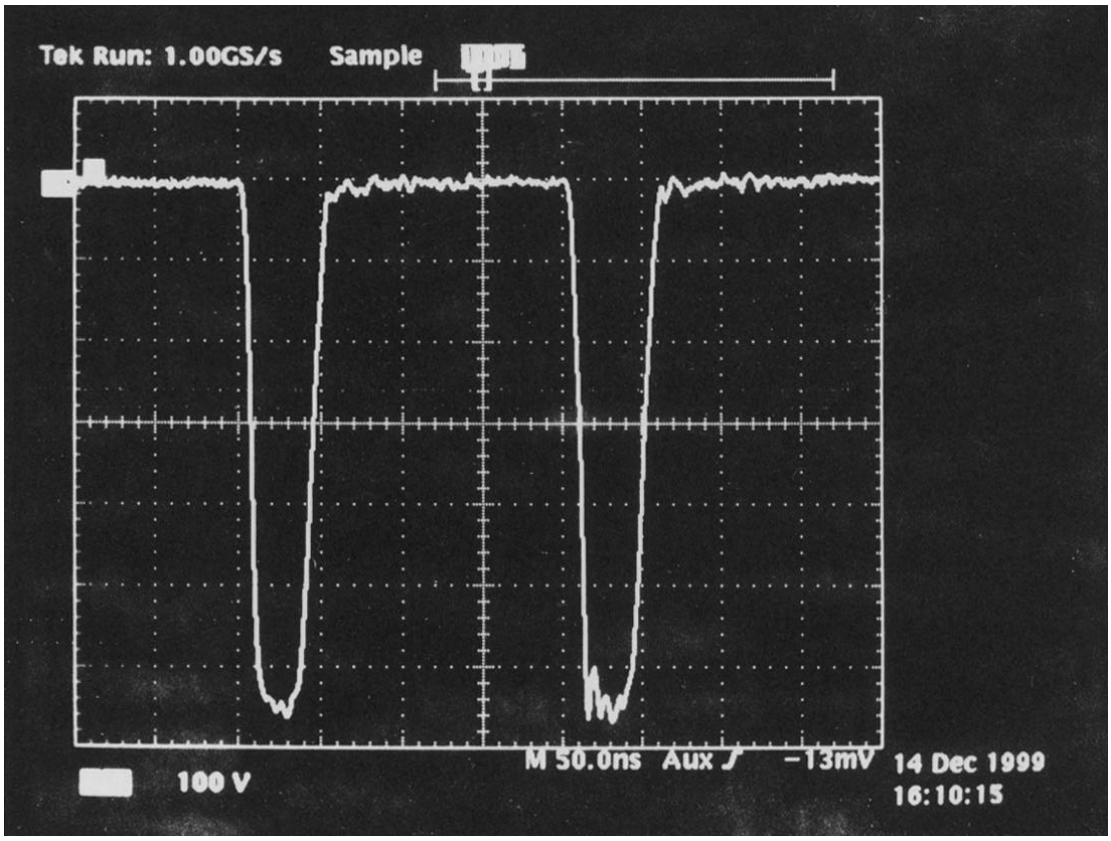
At present, there are only enough printed circuit boards (MOSFET carrier boards) to drive four transformers and two of those are prototypes that are restricted by their gate drive circuits to a minimum output pulse width of ~ 100ns. We also have two pre-production boards that meet all of our requirements for rise and fall-times and minimum pulse width. The remainder of the production boards are due to be delivered in the first week in January and should give us full high voltage capability.

The first data represents test results from a single board. Shown below is a simplified schematic for the MOSFET circuit that consists of the MOSFET, energy storage capacitors, and MOSFET control circuit. We are using 1000V MOSFETS that are rated for ~ 10 amperes average current. This carrier board has twelve such MOSFETS circuits that are electrically connected in parallel at the drain and also share a common ground; all of the capacitors are charged from the same high-voltage source. Each board has a single input trigger pulse that is distributed to each of the control circuits. The carrier board is connected to the single turn transformer in a low inductance manner and the load resistance is connected to the single-turn transformer secondary. At present the load is simply a parallel array of resistors.



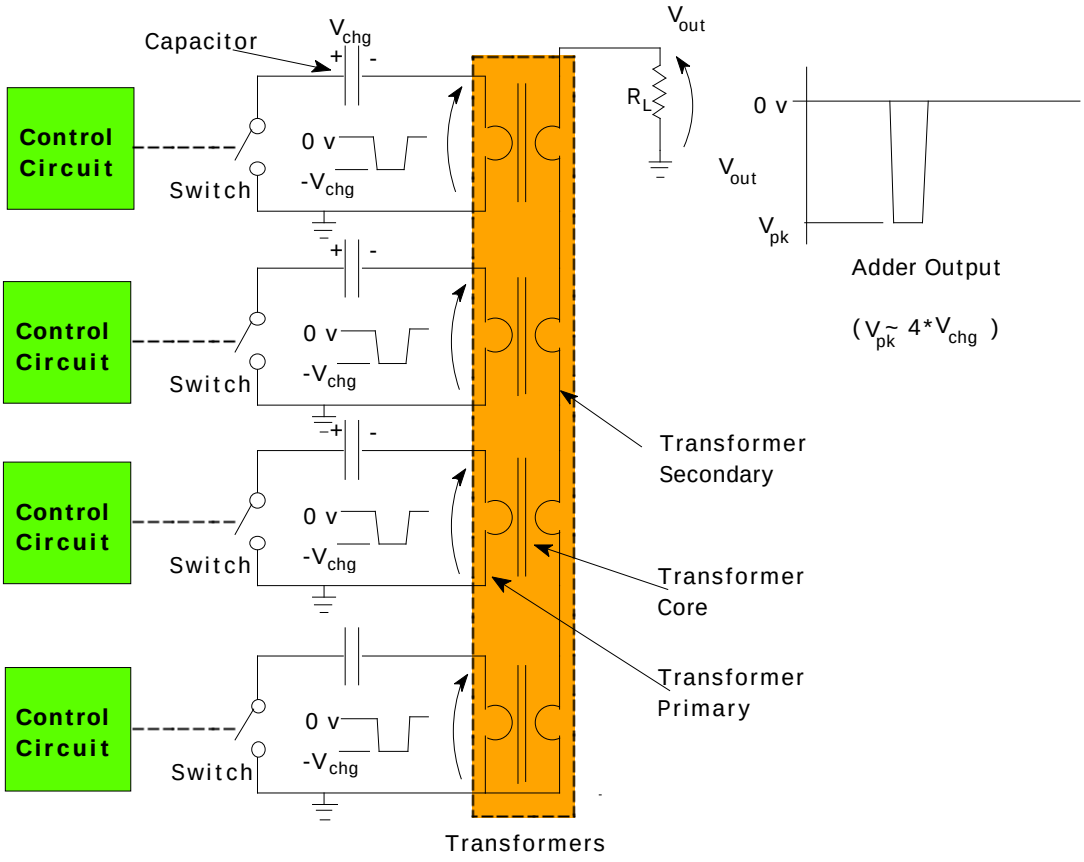

Simplified Schematic of MOSFET Circuit

The individual MOSFETS and their drive circuits have been tested and have demonstrated voltage rise and falltimes of less than 10ns (10-90%) at an operating voltage of ~ 800V and peak current of ~ 25 amperes/device. A pre-production MOSFET carrier board with twelve parallel circuits has demonstrated similar performance. The oscillograph shown below represents a two-pulse burst with a 200ns time interval between leading edges. The load resistance is ~12.5Ω and the capacitor charge voltage is ~ 650 V. In this oscillograph the load current is ~ 50 amperes. The vertical scale is 100V/div and the time scale is 50ns/div. The pulse polarity is negative with ground being one division from the top.



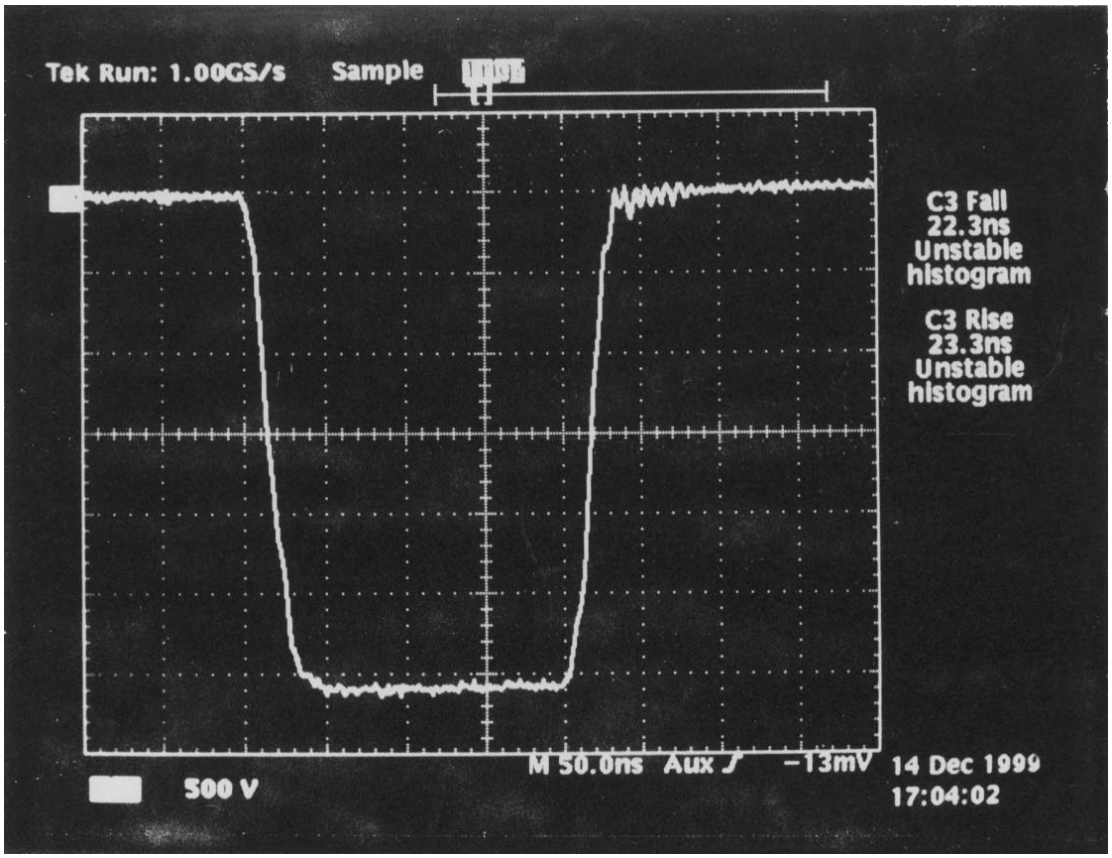

Two Pulse Burst – Single Board into Transformer

Below is the simplified schematic for a four-cell test circuit followed by an oscillograph of the load voltage. In the four-cell test, the transformers are configured in the adder configuration with the transformer primary circuits all being driven by ground referenced circuits and the transformer secondary windings connected in series. Ideally, the output of the secondary winding is simply the sum of the primary inputs.



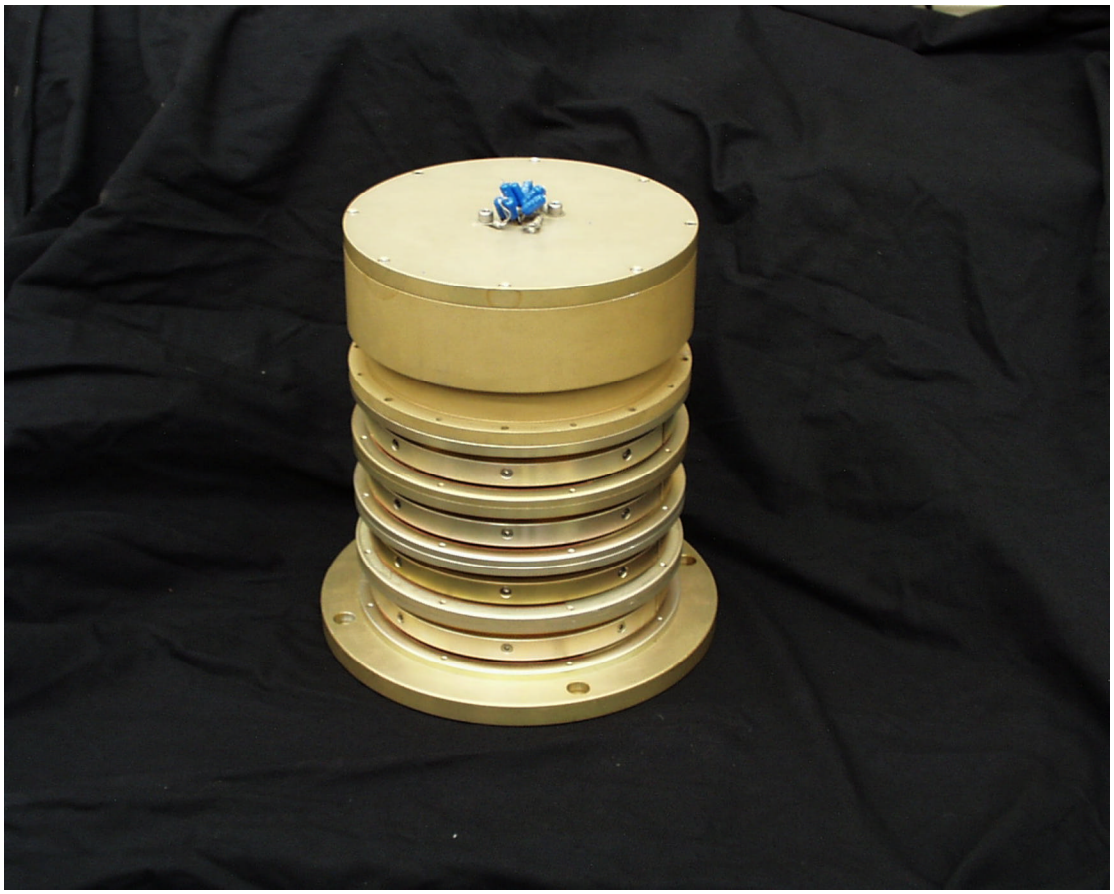

Simplified Electrical Schematic of Adder Concept
(4 Switched Cells)

For testing this configuration, a MOSFET carrier board is connected to each of the transformers. Two of the carrier boards are prototype boards that are limited in their pulsewidth by the control circuit to ~ 150ns. These boards also have rise and fall times that are limited to ~ 20ns. The other two boards are pre-prototype boards and have a performance capability as demonstrated in the first oscillograph. The charge voltage for this test is ~ 800V and the load resistance is 12.5Ω. Peak current in this measurement is ~ 250 amperes. The oscilloscope measures the rise and fall times to be ~23ns (10-90%) but I expect considerably better performance with regard to rise and fall times as well as minimum pulse width when the production boards are available. You can see that the adder is fairly efficient in that the output is ~3100V for a single stage input voltage of ~800V. You will notice from the photographs that we are only using a single MOSFET drive board and that the transformer is designed to accommodate two boards. This gives us a peak current capability in excess of 500 amperes with only a small voltage drop across the MOSFETS. We plan to test this design to determine the peak current limit.



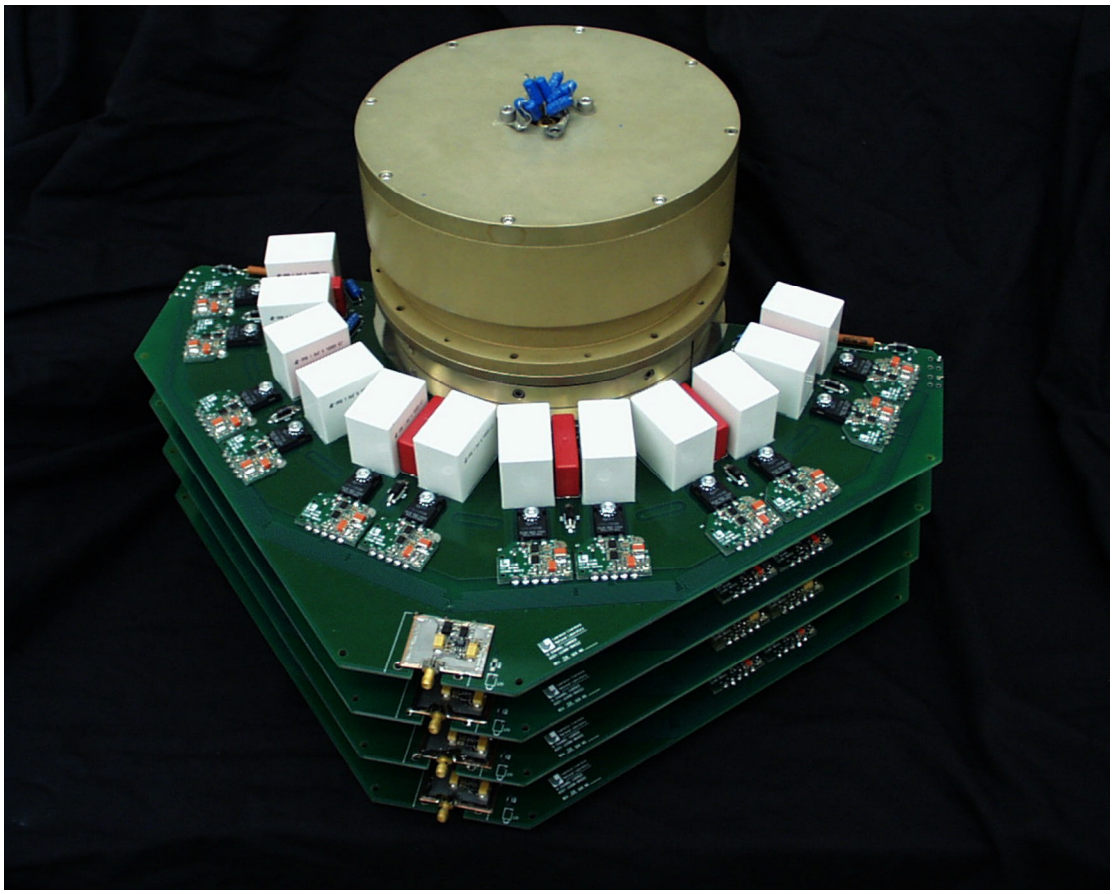

Four Cell Output Voltage – 500V/div into 12.5Ω

Shown in the next photos are the transformer (4-cell stack) with and without boards installed. For scaling purposes, the transformer stack is ~ 8 inches in diameter.



Four Cell Stack

The bottom plate is for mounting. The load resistors (blue) at the top of the structure will eventually be replaced with a 50Ω cable. The boards mount in the slots on the transformers; this makes up the electrical connection as well as supports the boards mechanically.



Four Cell Transformer with MOSFET Carrier Boards Installed

In this photograph, the white blocks are the energy storage capacitors. The red capacitors are part of the snubber circuit and are not shown on the simplified schematic. The small boards and MOSFETS (black devices) can be individually removed and repaired. Utilities power supply connections (high-voltage and housekeeping) are on the back edges of the board. The small board in the front is the trigger module. As you can see the entire structure is very modular which is an asset when servicing is required.