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Space Vector Pulse Width Modulation for Three-Level Converters

- a LabVIEW Implementation

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Abstract

Space Vector Pulse Width Modulation for Three-Level Converters - a LabVIEW Implementation

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This thesis explains the theory and implementation of the Space Vector Pulse Width Modulation (SVPWM) using the graphical programming environment LabVIEW as its basis. All renewable energy sources are in need of multilevel power electronics in form of multilevel inverters. The mind behind the pulses created by the inverters is the SVPWM. This modulation type uses a space vector, referred to as the reference vector, to locate and create the desired sinusoidal-shaped waveform. Using LabVIEW as the software makes it easy to read real-time output from the integrated circuit of the hardware (FPGA). The SVPWM shows good utilization of the DC-link voltage, low current ripple and is relatively easy to implement in the hardware, making it suitable for any high-voltage, high-power application.

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Abbreviations

CM – Common Mode

DA - Digital to Analogue

DSP – Digital Signal Processor

FPGA – Field Programmable Gate Array

IGBT - Insulated Gate Bipolar Transistor

LabVIEW - Laboratory Virtual Instrumentation Engineering Workbench

PWM – Pulse Width Modulation

SVPWM – Space Vector Pulse Width Modulation

THD – Total Harmonic Distortion

WEC – Wave Energy Converter

1. INTRODUCTION

Every project dealing with renewable energy is in need of renewable energy conversion in form of multilevel power electronics. This thesis approaches three-level converters in a wave power conversion point of view and covers the calculation and implementation of a pulse width modulation system using a modulation strategy that uses a space vector as a reference in order to achieve a desired three-level waveform (Space Vector Pulse Width Modulation). The system is specially adapted for three-phase systems that requires high-power and high-voltage and is therefore suitable for all types of renewable energy sources.

1.1 Background: The Lysekil Wave Power Project

The Uppsala University Power Division Department started their wave power project in 2002 and four years later the first wave energy converter (WEC) was tested out at sea. Several WEC's has been tested there since then and the success rate has been high. Most of the converters are grounded with concrete at the bottom of the sea, 25 m below the water surface[1]. The WEC's are conventional point absorbers: They use linear generators to convert the mechanical energy created by the wave motion into electrical energy. A WEC with this form operates in the following way:

- The *buoy* moves along the waves creating a vertical up and down movement.
- This motion is transferred to the *rope* that is connected to the piston.
- The *piston* induces current in the *stator* windings when going up, but with help from the *spring* attached at the bottom, also when going down.

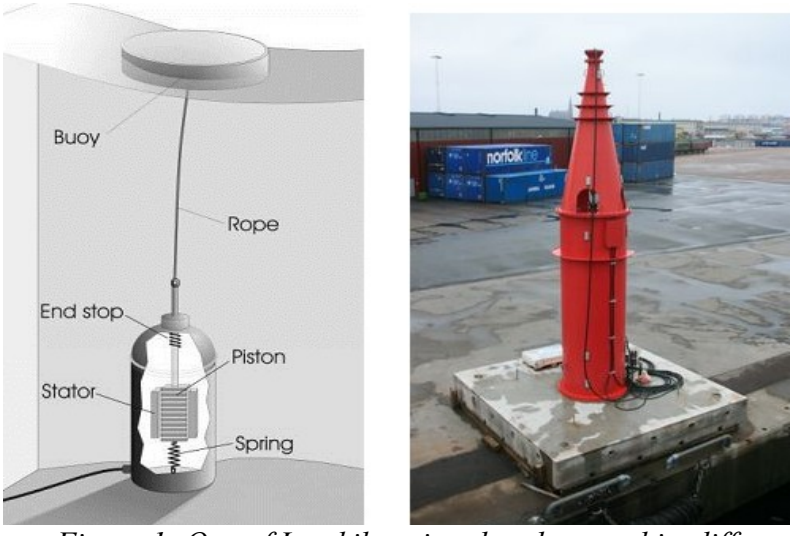


Figure 1: One of Lysekils point absorbers and its different parts

1http://www.el.angstrom.uu.se/forskningsprojekt/WavePower/Lysekilsprojektet_E.html, 10/01/12

1.2 Overview: From Sea to Grid

After successfully achieving the extraction of energy with help from the power converter, the next step is to connect it to the grid. This can not be done directly. The received output from the WEC has to be processed through several systems before it can match the characteristics of the grid (Fig. 2). If the generator is synchronous it has to meet some demands before it can be connected to a strong grid. These requirement has to be fulfilled:

- Same frequency
- Same amplitude
- Same phase and phase shift (three phase)

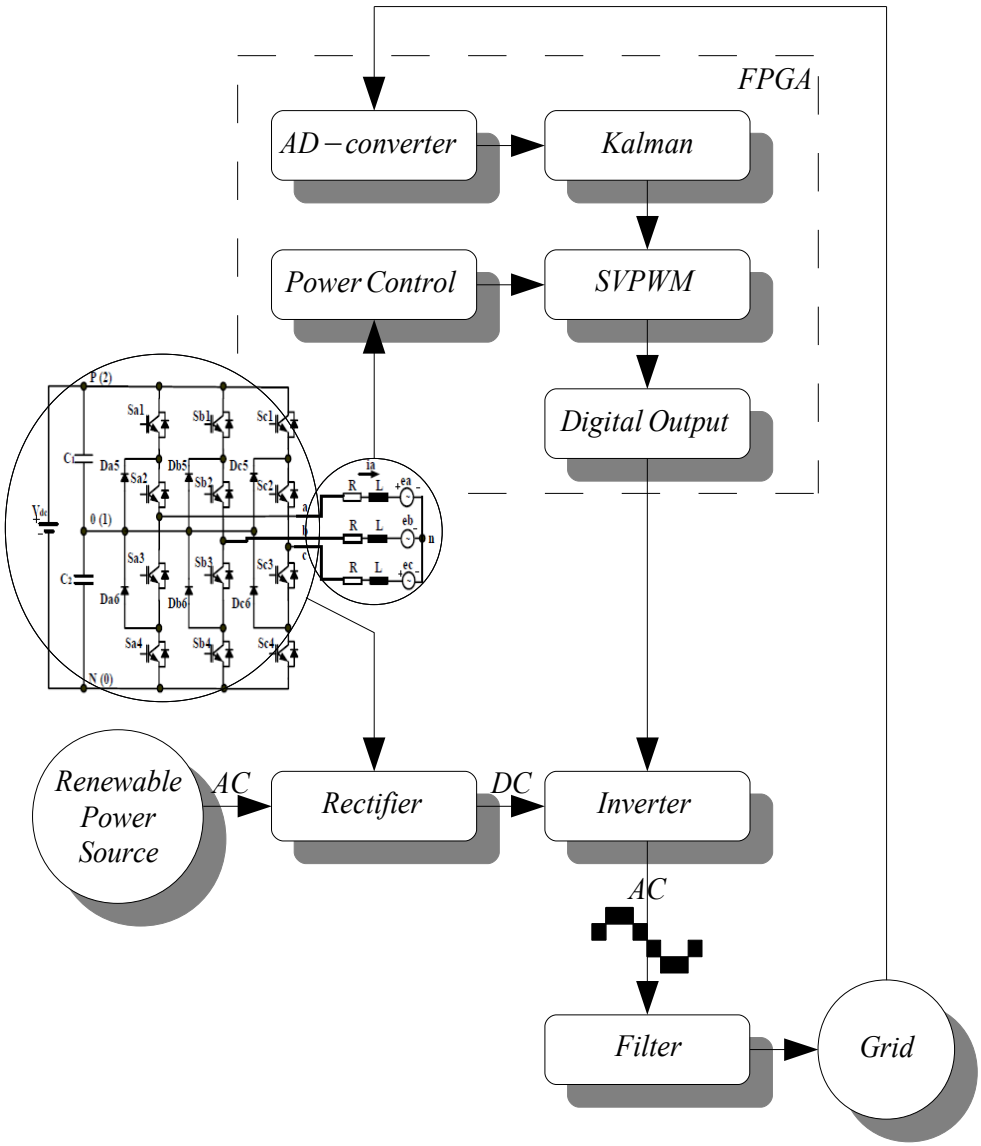


Figure 2: Overview of a Power Converting System: From Source to Grid

This means that the output from the power converter will not be connected to the grid until these requirements are fulfilled. To do this a reference for the grid characteristics is needed. This is done with the Kalman filter. The Kalman filter uses a AD converter to approximate a reference that fits the grid. Its output is based on samples. With this information the inverter can be supplied with switching information. The inverters capability is based on the information given by the space vector modulation algorithm that gives the exact switching time for each switch, creating a stepped output voltage waveform using the DC, supplied by the energy source. This output will then fulfil all the demands mentioned before. Directly connected to the inverter (theoretically to the modulation algorithm) is the current controller, that controls the energy output.

1.3 Multilevel Converters and Modulation Strategies

A DC to AC converter is defined as a inverter. The converter produces sinusoidal output waveform with respect to magnitude [V], frequency [rad/s] and phase [a,b,c] witch help from a DC-power supply. To create this specific waveform the inverter switches has to be turned ON and OFF at certain times, given by the chosen modulation strategy. As seen in Fig. 3b, the output will not be exact as a sinus wave, but the charactaristics will be the same. Fig. 3a shows a typical three-phase two-level inverter with IGBT's (Insulated Gate Bipolar Transistor) as switching devices. The output phases are given as a,b and c.

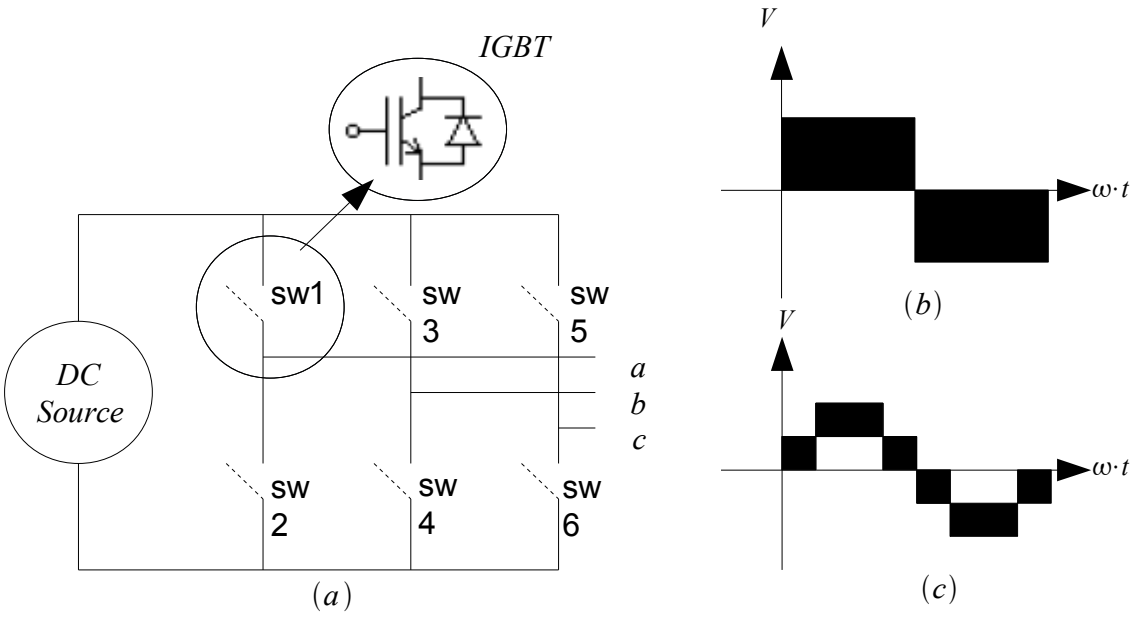


Figure 3: (a) Three-phase two-level inverter with 6 IGBT-switches with the three output phases a,b and c. Output voltage waveform created with PWM: (b) Line-to-line Voltage (c) Line-to-ground Voltage

Inverters are commonly used for medium voltage applications. For high-voltage high-power applications, the inverter also serves as a control mechanism for the reactive power and voltage stabilisation. With the multilevel converter topology the output waveform can be formed with smaller voltage steps (dv/dt), which also decreases the stress on the bearings and winding isolation [7]. It obviously also gives a lower total harmonic distortion (THD) in the output, because of the closer resemblance to the sinusoidal waveform. For multilevel converters, medium voltage semiconductors devices can still be utilized for high-voltage high-power applications. Still standing is the issue with the capacitor voltage balancing problems [15]. However, still the multilevel converter dominates on the power electronic platform. The most studied and tested multilevel types are:

- Cascaded H-Bridge Multilevel Converters
- Flying Capacitor Multilevel Converters
- Diode Clamped Multilevel Converters

For this thesis mainly the diode clamped converter will be discussed and studied. The mind behind the inverters switching combination is the pulse width modulation (PWM). There are several different modulation strategies to approach. One of these is the Space Vector Pulse Width Modulation (SVPWM) and will be the theoretical base of this thesis.

1.4 Guidelines: Purpose and Method

Purpose

The purpose of this project is to design a space vector modulated three-level neutral-point diode-clamped converter that can suit any high power application such as the renewable power generation. Mainly because renewable power resources are unreliable and lacks the form of an even output, regulation and adaptation is needed. This report will discuss the theories behind SVPWM, the implementation of the algorithm, confrontations, conclusions and suggestions for future work.

Method

This project is limited to the analysis of a three-level converter. The tools for realizing this will be the interface program LabVIEW, that will feed the hardware, the FPGA (Field Programmable Gate Array), the information that is needed for the inverters. However, this report only shows the software experiments tested for the hardware output. The output accuracy is confirmed with a digital displayer and will not be tested on the inverters.

2. MULTILEVEL CONVERTERS: TOPOLOGIES, CONTROLES AND DIGITAL COMPONENTS

2.1 Multilevel Strategies

Most of today's power systems need components making higher power operations possible. A concern for the medium voltage grid is the connection with only one semiconductor switch. This limitation became the fuel for pushing researches to develop the multilevel power converters, realizing the combination of high-power and medium-voltage. Except for the increase of power levels, this also opened up opportunities for renewable energy sources, ie multilevel converter systems could easily be attached to it [15].

To understand this project it is necessary to go all the way back to 1981, when it all started: The Multilevel power conversion was introduced for the first time and this was only the first step in what was coming to become a foundation for today's work in power conversion. Until then there was only some studies on PWM in general, but those were not suitable for variable drive-systems and were causing harmonic losses and torque pulsation, resulting in efficiency reduction. With the introduction of three-level converters, instead of two-level, the losses could be reduced [21].

A multilevel inverter works with the usage of several levels of DC-voltages constructing a staircase formed AC-voltage. Capacitors, batteries and renewable energy sources can be used as the DC-source [15]. When the voltage level increases the harmonics decreases. The advantage of this multilevel system is that it induces good power quality, has good electromagnetic compatibility, low switching losses and high capability [6]. There are also several methods in decreasing the switching losses even more [16]. Excepts for these advantages, the multilevel is characterized by low distortion and low dv/dt (voltage variation in time) in the output, low current distortion. It also gives the possibility to terminate common-mode (CM) voltages (and so reducing the stress on the bearings) [7] and is operational with both low and high switching frequencies. High switching frequency means higher efficiency [15]. Unfortunately, multilevel converters do have some disadvantages. One particular disadvantage is the greater number of power semiconductor switches needed. Although lower voltage rated switches can be utilized in a multilevel converter, each switch requires a related gate drive circuit. This may cause the overall system to be more expensive and complex [15]. This chapter will describe the three most common converters: Cascaded H-Bridge Multilevel Converters, Flying Capacitor Multilevel Converters and Diode Clamped Multilevel Converters. Also, voltage control operations will be discussed.

2.1.1 Cascaded H-Bridge Multilevel Converters

A cascaded H-Bridge converter has several H-Bridge conversion cells. These cells are formed as in Fig. 4. It consists of four switches. Each cell is also supplied with a DC-source and is series-connected on the AC side. The whole figure demonstrates one phase leg for the converter. The waveform to the right is the circuits corresponding waveform. Adding V_{C1}, V_{C2}, V_{C3} and V_{C4} gives its 9-level step-shaped waveform [7].

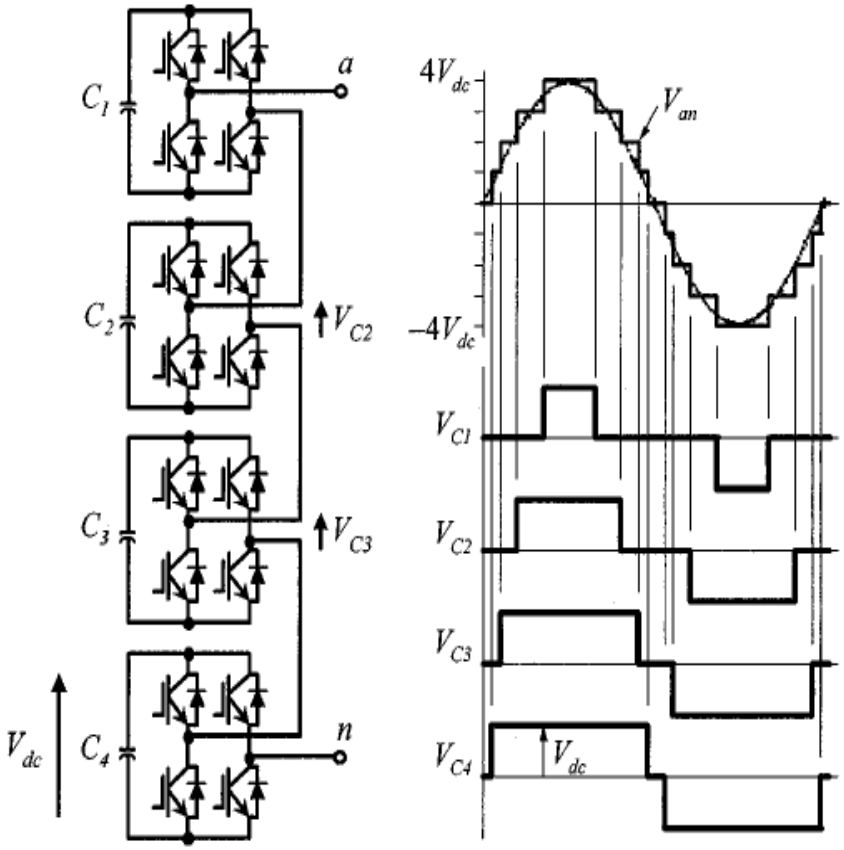


Figure 4: A Cascaded H-Bridge Multilevel Converter (one phase leg) and its 9-level output waveform

Each of these levels can have $+V_{DC}$, 0 and $-V_{DC}$ as their output through different path selections when connecting the DC-source to the AC output, thus assigning different switching patterns for the four switches. Switch 1 and 4 switched ON gives an output of $+V_{DC}$, switch 2 and 3 ON gives $-V_{DC}$ and all the switches ON gives a zero. The series connection between the AC outputs gives then the summation of the outputs creating this waveform.

The advantages with the cascaded H-bridge multilevel converter can be seen in the formula for the calculation of the output phase voltage levels: $m = 2s + 1$. Given that *s* stands for the number of DC-sources needed, the number of voltage levels is more than double than for the sources. Also the

series-connection of the H-bridge form lowers the manufacturing costs, because it shortens the process. The problem remaining is the fact that each H-bridge needs its own DC-source [8]. This means that it can not be connected to products that already have multiple separated DC-sources [15]. One important attribute that a multilevel converter should have is that it can be applied to as many different products as possible. There are however other types of cascaded H-bridge converters that can fit to a wider range of product. This newer type was introduced a decade later and gave form to a converter that only needed one DC-voltage source. In [2] and [27] this type of converter is described and realized as a two cascaded three-phase three-level inverter, as seen in Fig. 5.

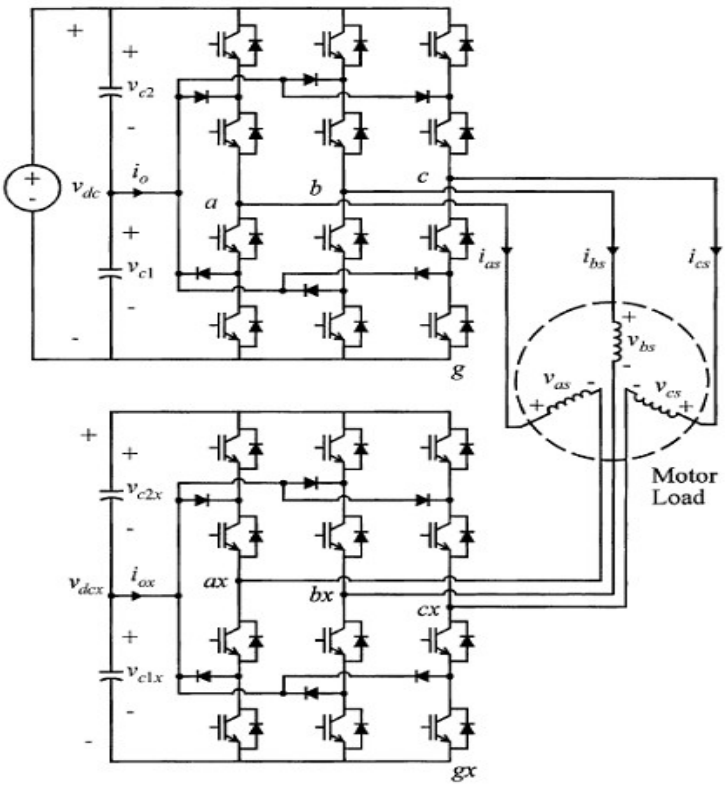


Figure 5: A two cascaded three-phase, three-level inverter

Although several upgraded versions of the cascaded multilevel converter are presented, there still are problems in choosing the number of levels, with respect to the harmonic losses and costs. It is known that higher level means less harmonics and greater output voltage, but with the advantages comes also disadvantages. It is not wisely to use as many levels as theoretically possible just to reduce the harmonics or to increase the output voltage, because more levels also means higher cost, because of more equipment. For this particular 3/3 inverter the most eligible level is the 7-level form. Higher levels does not reduce the harmonics remarkably [4]. There are also several other methods in choosing the level best for the occasion and also methods in reducing the harmonics [3]. However, there has been studies showing that the cascaded multilevel inverter is most efficient for low voltage renewable energy sources [26].

2.1.2 Flying Capacitor Multilevel Converters

In 1992 the Flying capacitor converter was introduced for the first time. The work of Meynard and Foch upgrades the technique where series connection of switches was needed, adapting the system to higher voltage conversions. High-voltage conversion requires semiconductors capable of keeping the desired voltage at a certain level. The paper [5] shows positive results, such as control simplicity and a more desirable output waveform. Other studies also show that the flying capacitor converter shows good performance for high and low modulation index [9].

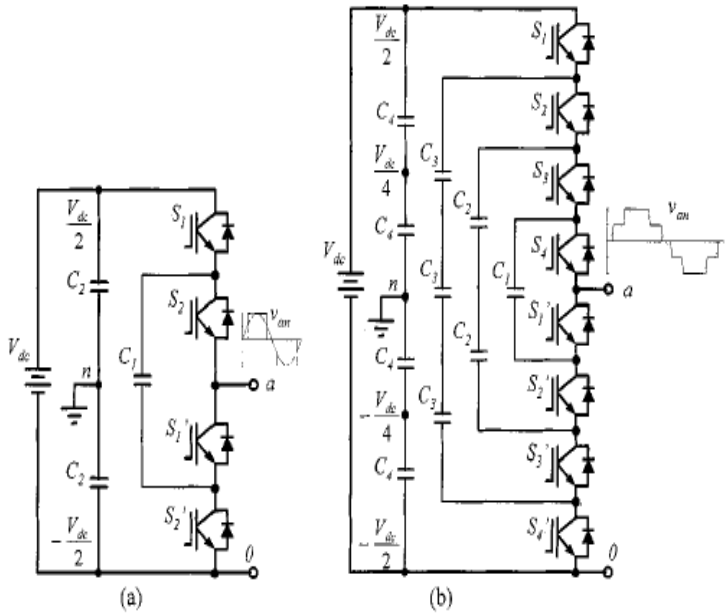


Figure 6: Circuit of a Flying Capacitor (a) two-level converter for one phase leg (b) three-level converter for one phase leg

The flying capacitor is also known as the capacitor clamped inverter, because of its independent capacitors clamping the voltage to one capacitor voltage level [7]. The structure of the system is formed as a ladder and the voltage of each capacitor is different from the other. When the voltage between two side by side placed capacitors increases, it transmits the size of the voltage steps in the output waveform [15].

V_{an}	Switches
$V_{DC}/2$	S1 and S2
0	S1 and S1' or S2 and S2'
$-V_{DC}/2$	S1' and S2'

Table 1: Switching combination for a two-level inverter (one phase leg)

The switching combination for the three-level inverter (Fig. 6a) does not have as many combination states as for the five-level. To get the output voltage V_{an} for the three-level inverter, it has to be regulated with the combination of four switching states, as seen in Table 1.

For the five level system however there are 14 switching states. For an m-level system the required clamping capacitors per phase leg can be described as: $(m-1)*(m-2)/2$, $(m-1)$ designating the required number of DC-bus capacitors.

With the increase of levels, also the amount of some problem factors increases: [15]

- It gets more difficult to control the different voltage levels in each capacitor.
- The increase in capacitors leads to more costs and space.
- The packing stage gets more complex.
- Charging all the capacitors to the same voltage level, makes the whole start-up very complex and the switching utilization and efficiency for the power transmission will not work as expected.

V_{an}	Switches
$\frac{V_{DC}}{4}$	S1,S2,S2,S4
$\frac{V_{DC}}{2}$	S1,S2,S3,S1' or S2,S3,S4,S4' or S1,S3,S4,S3'
0	S1,S2,S1',S2' or S3,S4,S3',S4' or S1,S3,S1',S3' or S1,S4,S2',S3' or S2,S4,S2',S4' or S2,S3,S1',S4'
$\frac{-V_{DC}}{2}$	S1,S1',S2',S3' or S4,S2',S3',S4' or S3,S1',S3',S4'
$\frac{-V_{DC}}{4}$	S1',S2',S3',S4'

Table 2: Switching combination for a three-level inverter (one phase leg)

The flying capacitor also has to deal with voltage unbalance, causing distortion of the output voltage and load current. This might lead to a breakdown of the switching device [28].

However, there are some advantages worth mentioning. Excepts for inverter control of real and reactive power, the inverters phase redundancies balances the voltage levels [15].

2.1.3 Diode Clamped Multilevel Converters

The diode clamped multilevel inverter has almost the same structure as the flying capacitor, but instead of capacitors this inverter type uses diodes as clamping devices, creating the desired output voltage. The voltage across each capacitor is defined as $V_{DC}/(m-1)$, m being the number of levels and $(m-1)$ the amount of capacitors needed. So, for a two-level inverter the voltage is V_{DC} and for that case one capacitor is used. For a three-level inverter the voltage is $V_{DC}/2$ and therefore is in need of two capacitors. This specific design makes it possible to increase the number of levels just by increasing the amount of capacitors. In this context the terminology "neutral point clamped" is often used. It describes the neutral point between two capacitors connected across the DC-bus adding an extra level to the system. If m is an even number, the neutral point is not utilized, so then it is usually called a multiple point clamped converter. Experience show that higher levels than the three-level converter causes voltage balancing problems, so it is common to use the three-level inverter [6], but there are studies demonstrating SVPWMs with self balancing systems [18].

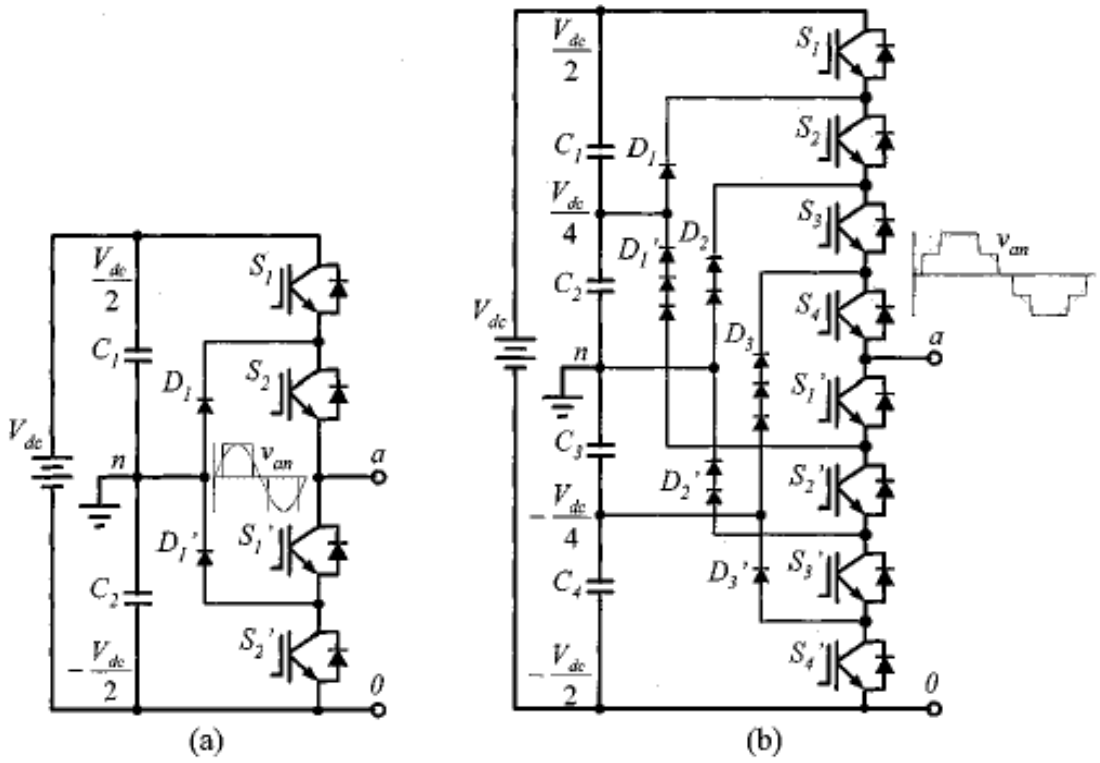


Figure 7: A Diode Clamped converter for a (a) three-level inverter (one phase leg) and for (b) five-level inverter (one phase-leg)

Fig. 7a shows a three-level inverter. Its output voltage V_{an} (one phase leg) has three states: $V_{DC}/2$, 0 and $-V_{DC}/2$. To get $V_{DC}/2$, the two upper switches need to be ON. To get a zero, the two middle switches need to be ON and for $-V_{DC}/2$ the two lower switches need to be ON. One difference between a conventional two-level inverter is the part in Fig. 7a that is called D_1 and D_1', referring to the two diodes. The required amount of diodes can be calculated as $(m-1)*(m-2)$, where *m* stands for amount of levels. So in the three-level case two diodes is needed for each phase. The formula also shows a major increase of the number of diodes when increasing the amount of levels. A three-level inverter needs in a three-phase system 6 diodes, a four-level needs 18, a five-level 36 and at six-levels it already has reached a amount of 60 diodes. This higher level inverters may work in theory but not in practice. The two diodes clamps the switching voltage to half of the DC-bus voltage and the difference between V_{a0} (for an example when S1 and S2 is on, the voltage across *a* and 0 is V_{DC}, giving $V_{a0} = V_{DC}$) and V_{an} gives the voltage across one capacitor ($V_{DC}/2$). It is important to add that the upper and lower switching pairs are complementary. This means that S1 and S1' or S2 and S2' never can be ON at the same time. For the five-level inverter (Fig. 7b) there are five possible voltage outputs (V_{an}): $V_{DC}/2$, $V_{DC}/4$, 0, $V_{DC}/4$ and $V_{DC}/2$ and they operate as seen in Table 3.

V_{an}	Switches (ON)
$V_{DC}/2$	S1-S4
$V_{DC}/4$	S2-S4 and S1'
0	S3,S4,S1',S2'
$-V_{DC}/4$	S4,S1'-S3'
$-V_{DC}/2$	S1'-S4'

Table 3: Duty cycle for the switches in one phase leg (five-level inverter)

Reaching higher levels decreases the lower harmonics and the need for filters, but at the same time it magnifies the need for clamping diodes. Advantages with the diode-clamped inverter is the high efficiency. This because all the devices are switched at the fundamental frequency. The diode-clamped inverter also has a easy reactive power control application, but has difficulties controlling the real power for the individual converters [15].

2.2 Digital Components: Software and Hardware

2.2.1 FPGA

The FPGA (Field Programmable Gate Array) is a integrated circuit configured with a hardware description language. Its unique design allows custom design of the hardware. From a high-level view the FPGA is a programmable silicon chip. It uses logic blocks and programmable routing resources, realizing this tailored version, without physically changing anything in the hardware. The digital computing tasks are developed in the software (ie general-purpose and graphical programming languages) and then compiled down to a configuration file or bit stream, containing information on how the components should be wired together. The FPGA does not require the user to have experience in hardware-design, which broadens the user group.

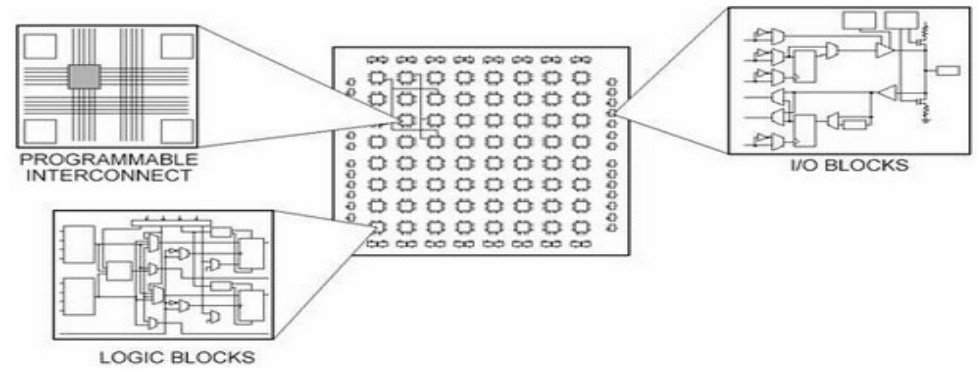


Figure 8: Different parts of the FPGA

Benefits

These kinds of projects require a powerful system considering factors such as efficiency, time and cost. With the FPGA comes several benefits:[2]

- *Performance*: Because of the lack of sequential execution, the FPGA accomplished more per clock cycle. The computing power is higher than for conventional DSP's.
- *Time to market*: Implementing a concept is easier and faster. Instead if weeks it takes hours.
- *Cost*: The programmable silicon eliminates fabrication costs and installation requirements
- *Reliability*: The FPGA does not use operating systems. This minimizes problems, because the communication with the hardware will be directly.
- *Long-term maintenance*: Having the characteristic of being configurable makes it easy to adapt to future modifications.

2http://zone.ni.com/devzone/cda/tut/p/id/6983, 10/01/12

Hardware description

The hardware contains a certain set of configurable logic blocks that can be wired together. Excepts for the logic blocks it also has other specifications such as:

- Flip-Flops: Binary shift registers that synchronizes logics and saves the logic states between clock cycles.
- LUTs (Look Up Table's): All combinations of different logics (AND, OR etc.) are implemented as truth tables in the LUT memory. The output of each unique combination is defined from before.
- Multipliers (Shift-add operation)
- Block RAM

All these part and more are then used and controlled through the chosen programming language connected to it[3].

FPGA type

For this project a Virtex5 LX 50 FPGA is used (Fig. 9). Considering the most common components this version has 28.000 Flip-Flops, 28.000 LUT's, 48 Multipliers and a 1728 kbit BlockRAM (each block having a size of 36 kbit). The combination with a graphical programming language used for this project, LabVIEW, makes the digital computing and compiling quite user-friendly.

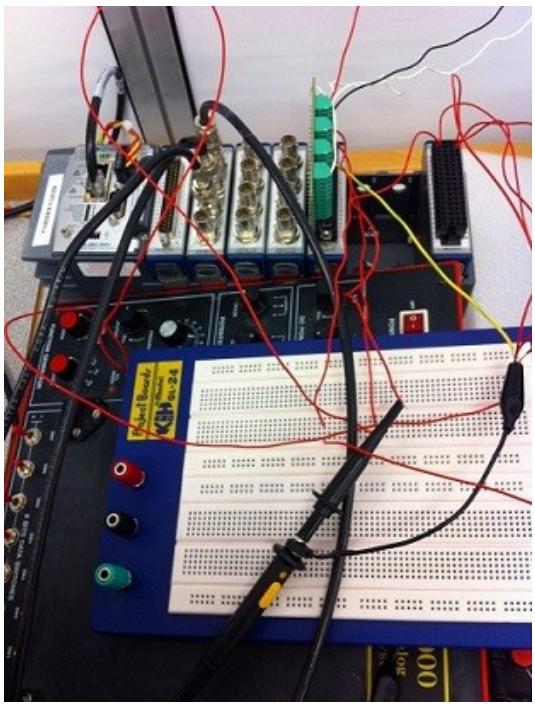


Figure 9: The CompactRIO with the Virtex5 LX 50 FPGA used for the project

3http://zone.ni.com/devzone/cda/tut/p/id/6984, 10/01/12

2.2.2 LabVIEW

LabVIEW (Laboratory Virtual Instrumentation Engineering Workbench) is a graphical programming environment, that, with help from logic blocks and other components, makes it possible to test, simulate and control a flowchart-type model. It is easily integrated with hardware devices such as the FPGA. Mostly the block digram (where the circuit is drawn) and the front panel (the input/output data, but also the programmatic interface) is used when dealing with this program (Fig. 10).

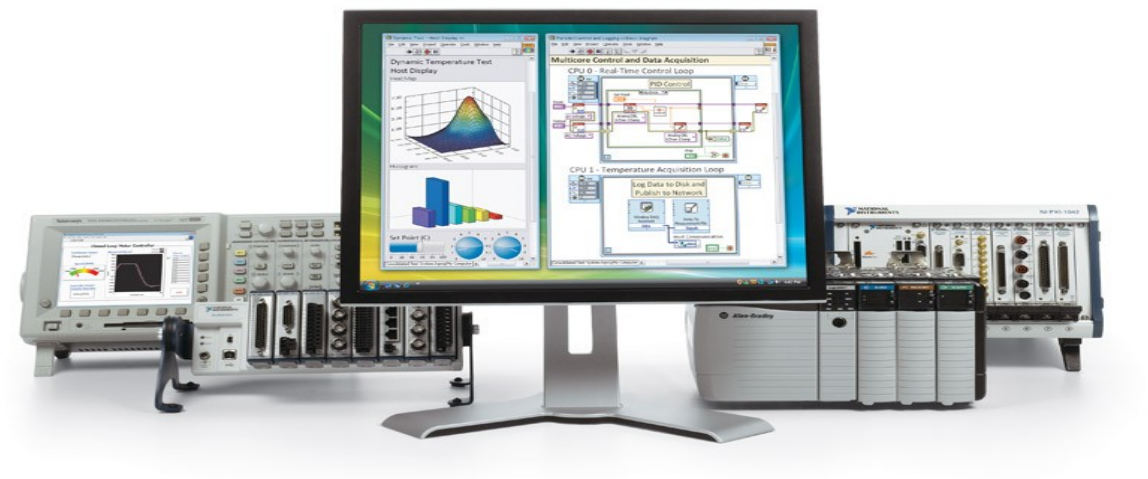


Figure 10: LabVIEW softaware and its interaction devices

Except the fact that a graphical programming language is more pedagogic and user-friendly, the LabVIEW software has benefits considering the following two big differences from other programming languages:[4]

1. Graphical programming is realized with help from graphical icons, combined in a diagram (Fig. 11) and is then directly compiled to machine code, so that the processor can understand and execute the orders created in the diagram.
2. Data flow is transmitted in form of data (not lines of text). This makes it easier to control different executions done separately and consecutively.

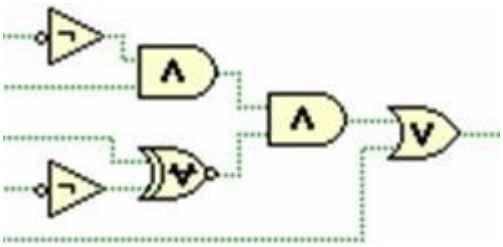


Figure 11:Example of a Logic Operation done in LabVIEW

4http://www.ni.com/labview/whatis/graphical-programming/ , 10/01/12

2.3 Control Algorithm: Predictive Current Controller

The predictive current controller can be used for any multilevel inverter high-voltage, high-power application [25], mainly because it works for long switching periods. This controller is defined as a linear control [12] is based on future values given by the most suitable voltage vector. It has been proofed that the predictive current controller improves the power quality [11]. The inverter in Fig. 12 is a three-level circuit with 19 voltage vectors. The current controller predicts the load current for each of these vectors [14].

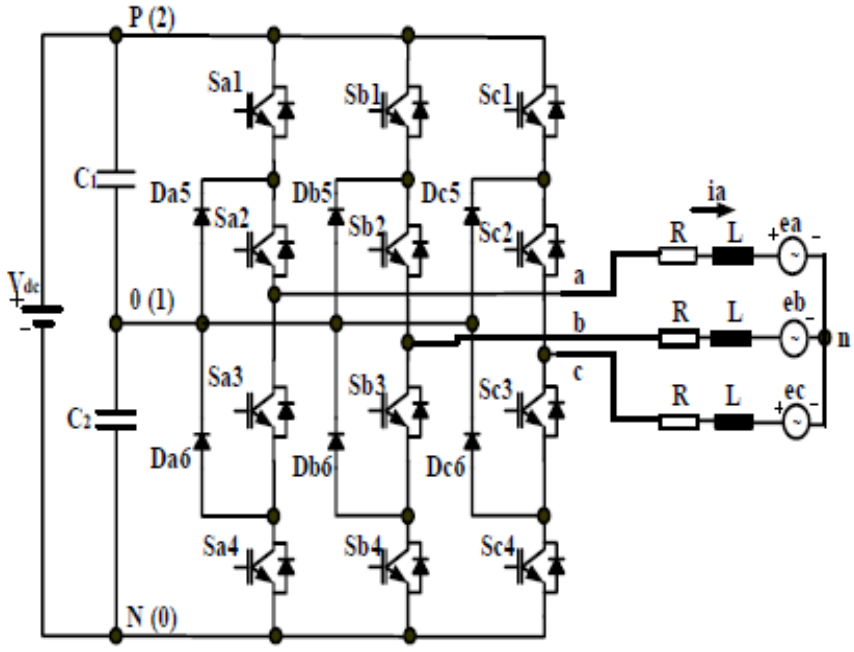


Figure 12: A three-level three-phase neutral point diode clamped converter, with current controller

Each calculation gives an error and the vector that has the smallest error is selected as the inverter voltage for the next sampling time. The involvement of many voltage vectors results in low harmonic distortion. Other advantages with this type of controller are: Fast dynamis respons and fast disconnection between load current components [13].

The current varies with respect to the resistance R and inductans L, but also to the output and grid voltage:

$$\frac{d}{dt}\underbrace{i_{abc}}_{\text{inverter output current}} = -\frac{R}{L} i_{abc} + \frac{1}{L}\left(\underbrace{V_{abc}}_{\text{inverter output voltage}} - \underbrace{e_{abc}}_{\text{grid voltage}}\right)$$

The form abc indicates that the current is given in a three-dimensional plane. To make the calculations easier, the varying parameters can, with help from αβ-transformation (a two dimensioal

complex plane), be changed into stationary values [14]:

$$\frac{d}{dt} i_{d(k)} = -\frac{R}{L} i_{d(k)} + \frac{1}{L}(v_{d(k)} - e_{d(k)}) + w i_{q(k)}$$

$$\frac{d}{dt} i_{q(k)} = -\frac{R}{L} i_{q(k)} + \frac{1}{L}(v_{q(k)} - e_{q(k)}) + w i_{d(k)}$$

The V_{DC} variation is given by:

$$\frac{d}{dt} V_{DC} = \frac{1}{C} \int i_c \, dt$$

2.3.1 The Current as a Reference

The current control is driven with help from future values, calculating the minimum inverter voltage required to make the inductor current follow the current reference as much as possible [14]. Fig. 13 shows the parts that has to be considered calculating the values for the current control.

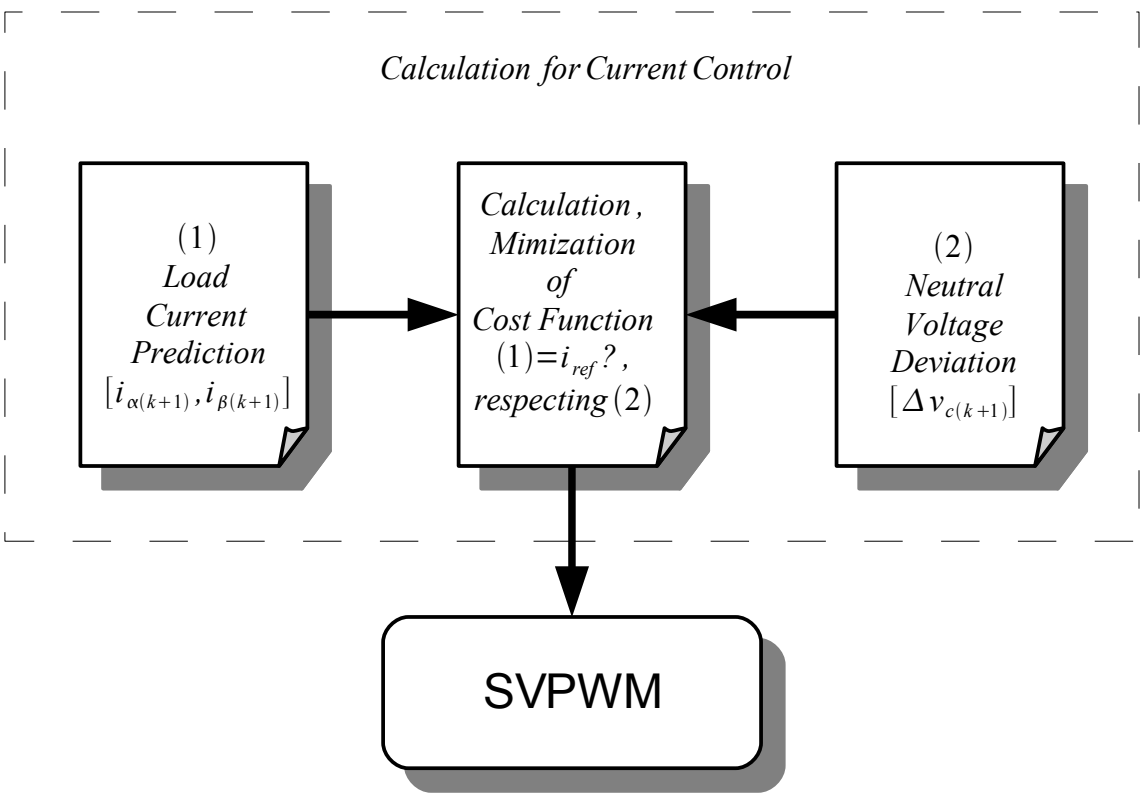


Figure 13: Overview of the Current Cotroller Ccalculations

The load current at $(k+1)th$ instant is given in the formula for the instant output voltage. These are the instant output voltage parameters in the complex αβ-plane:

$$v_{d(k+1)} = R i_{d(k+1)} + L \frac{d}{dt} i_{d(k+1)} - w i_{d(k+1)} + e_{d(k+1)}$$

$$v_{q(k+1)} = Ri_{q(k+1)} + L\frac{d}{dt}i_{q(k+1)} - wi_{q(k+1)} + e_{q(k+1)}$$

The currents varying in time is defined as:

$$\frac{d}{dt}i_{d(k+1)} = \frac{i_{d(k+1)} - i_{d(k)}}{T_s}, \frac{d}{dt}i_{q(k+1)} = \frac{i_{q(k+1)} - i_{d(k)}}{T_s}$$

Finally giving the load current at $(k+1)th$ instant:

$$i_{d(k+1)} = \frac{1}{(RT_s + L)}[Li_{d(k)} + wT_s Li_{q(k+1)} + Ts(V_{d(k+1)} - e_{d(k+1)})]$$

$$i_{q(k+1)} = \frac{1}{(RT_s + L)}[Li_{q(k)} + wT_s Li_{q(k+1)} + Ts(V_{q(k+1)} - e_{q(k+1)})]$$

Prediction for the grid voltage values can be calculated with the "Lagrange extrapolation method", a process that constructs new data points that are not included in the range of the measurements. This may not be appropriate for unpredictable functions, however if the sampling is low, extrapolation can be avoided [1].

Most control systems need a cost function that can determine if the required criterion is achieved or not. The cost function compares the calculated predicted current with the current reference. A low value for the cost calculation is to desire. It is given as: $c_1 = \lambda_1 |i_{d(k+1)ref} - i_{d(k+1)}| + \lambda_2 |i_{q(k+1)ref} - i_{q(k+1)}|$, where λ_1 and λ_2 are weighting factors, the weighting factor being a number between 0-1. The weighting factor λ_2 also determines the accuracy of the reactive power control, thus compensating for the power factor variation. The instantaneous reactive power can be predicted just like for the current: $Q(k) = e_{q(k)}i_{d(k)} - e_{d(k)}i_{q(k)}$ [14]

2.3.2 DC Voltage unbalance

The problem is caused by uneven charging/discharging of the DC-link capacitors when the output is connected to the zero-point. Each output terminal (V_{a0}, V_{b0}, V_{c0}) can be connected to this point and delivers in that case 0V. When that is the case, the neutral point current, i_0, causes this uneven charging pattern. It is known that multilevel neutral point clamped inverter has a DC-balancing problem. The reason for the unbalance lies in the capacitors. When a output phase voltage is shorted to the capacitor middle point, the corresponding phase current is transferred to the neutral point. To prevent this the neutral point current values should be zero. The solution to this problem is the regulation of the switching of the capacitors [14]. The DC-link currents are:

$$i_s = i_{c1} + i_1$$
$$i_{c1} = i_0 + i_{c2}$$
$$i_{c2} = i_s + i_{-1}$$

If the system is balanced the following relation is valid: $i_1+i_0+i_{-1}=0$ and gives the currents:

$$i_1=(s_{a1}\cdot s_{a2})i_a+(s_{b1}\cdot s_{b2})i_b+(s_{c1}\cdot s_{c2})i_c$$
$$i_0=(s_{a2}\cdot s_{a3})i_a+(s_{b2}\cdot s_{b3})i_b+(s_{c2}\cdot s_{c3})i_c$$
$$i_{-1}=(s_{a3}\cdot s_{a4})i_a+(s_{b4}\cdot s_{b4})i_b+(s_{c4}\cdot s_{c4})i_c$$

This gives the current flowing through capacitor c_1 and c_2:

$$\begin{pmatrix} i_{c1} \\ i_{c2} \end{pmatrix}=\begin{pmatrix} 1 & 1 & 1 \\ 1 & 1 & 0 \end{pmatrix}\cdot\begin{pmatrix} i_s \\ i_1 \\ i_{-1} \end{pmatrix}$$

With this also the DC-link voltage can be calculated:

$$c_2=\mu \underbrace{|\Delta v_{c(k+1)}|}_{voltage\ difference\ between\ c_1 \wedge c_2}$$

This is the key when minimizing the voltage unbalance. Another way of decreasing the unbalancing problem is through regulation of the energy:

$$E_{p(k+1)}=\frac{1}{2}C(\Delta v_{c1}^2)=\frac{1}{2}C(\Delta v_{c1(k)}+\frac{T_s}{C}\cdot i_{c1})^2$$
$$E_{n(k+1)}=\frac{1}{2}C(\Delta v_{c2}^2)=\frac{1}{2}C(\Delta v_{c2(k)}+\frac{T_s}{C}\cdot i_{c2})^2$$

In the same way as for the capacitor voltage-comparison:

$$c_2=\mu[E_{p(k+1)}-E_{n(k+1)}],\ \mu=determines\ the\ allowed\ neutral\ voltage\ variation$$

2.4 Conclusions

There are several differnt types of multilvel converters on the market and the most studied converters has been described in this chapter: Cascaded H-Bridge Multilevel Converters, Flying Capacitor Multilevel Converters and Diode Clamped Multilevel Converters. Choosing the right converter it is important to consider the voltage level to implement. High-level converters gives low distortion but higher voltage unbalance, so there has to be a compromise between those two factors, but also other issues such as increase of equipment for higher levels. For high-voltage high-power applications the inverter also can be used as a control for the voltage and reactive power regulation. This is done when the inverter is connected to a RL-load, a current controller. Designing the multilevel application a software (LabVIEW) directly connected to the hardware (FPGA) will be used for this project.

3. SPACE VECTOR MODULATION ALGORITHM FOR MULTILEVEL CONVERTERS IN THEORY AND IN PRACTICE

If the signal, received from the output of the power converter, is going to be connected to the grid it has to be synchronized with it. The inverters provide for this with help from the PWM switching information. The inverters will get the switching information from the calculations made by the modulation formed in LabVIEW. There are several different types of modulation strategies. This chapter will present the most common modulation strategies, the theory behind two-, and three-level SVPWM, and also the implementation done in Simulink and LabVIEW.

3.1 Modulation Topologies

The basic structure of a multilevel power converter is formed by small discrete DC-voltage sources [10]. The modulation strategies can be divided into two parts: Fundamental switching frequency and high switching frequency PWM. The latter part is the main focus in this chapter, because this is the part that is relevant for high voltage conversion. There are several different PWM methods. Here, some of the most common modulation topologies will be discussed.

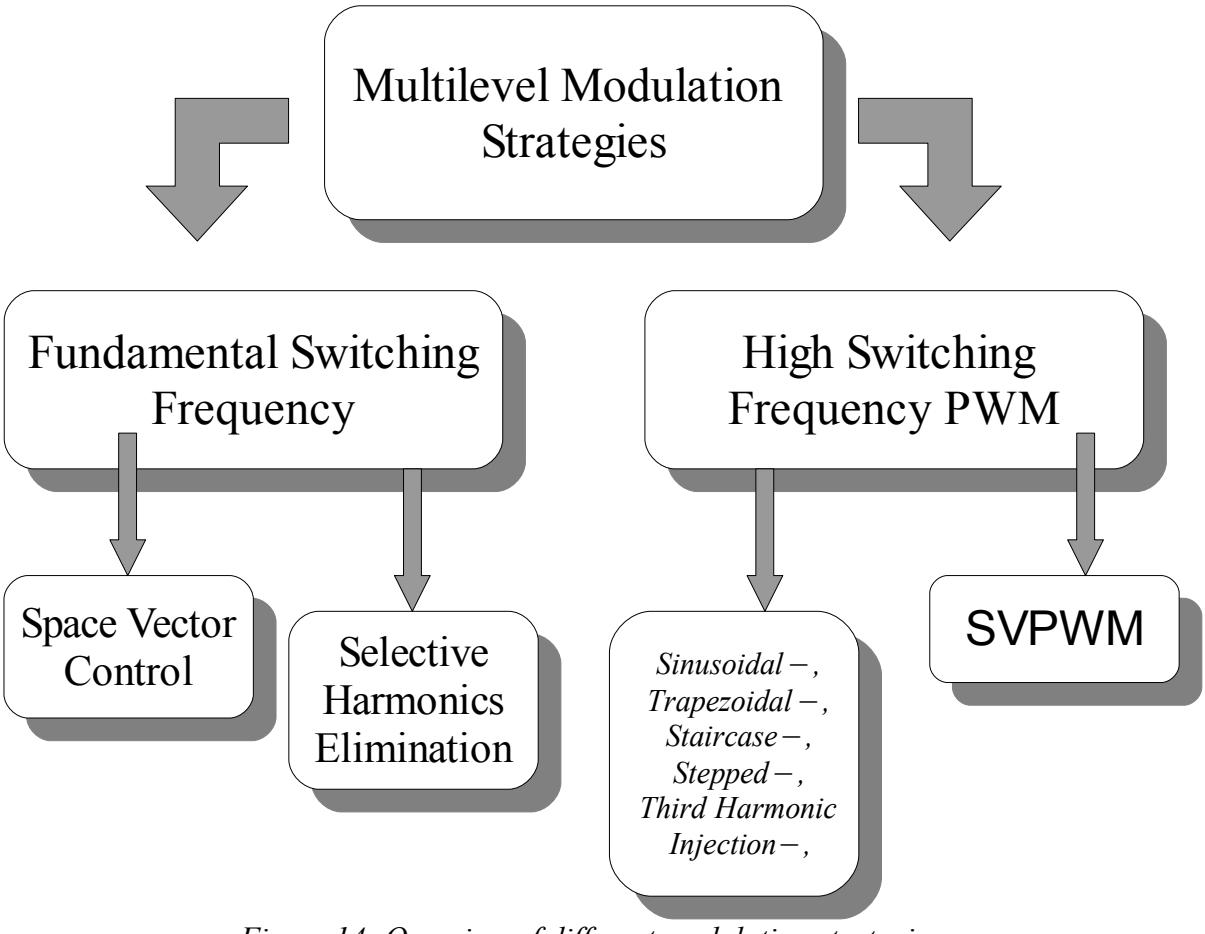


Figure 14: Overview of different modulation strategies

Choosing the modulation it is important to consider following things:

- Minimization of load current harmonics and switching frequency
- Providing uniform switching frequency for all switching devices and a balanced DC capacitor voltage [10]

Different PWM - approaches have the same goal: To reduce the THD of the current. Increasing the switching frequency reduces the lower-harmonics, which contributes to a lower THD, achieving the goal of a voltage output waveform with the requested rms values and frequency and a sinusoidal waveform resemblance [6].

Turning the switches ON and OFF creates pulses with the same amplitude but with different width. These pulses are generated in the output to replace the sinusoidal waveform [20]. The easiest way of creating this is by using a intersection method, ie comparison with a sawtooth/triangle waveform (carrier wave). When the reference wave (sinus) is larger than the triangular waveform, the PWM signal is switched ON (value: 1) and when it is smaller it is switched OFF (value: 0).

The most common method is called the **Sinusoidal PWM**. Although it is commonly used it has a big disadvantage – it has low output voltage, which also can be seen in Table 4. There are however other methods that can meet these demands in a better way, using similar carrier-based systems with different forms:

- **Trapezoidal modulation**: Comparison of a triangular wave and a modulating trapezoidal wave.
- **Staircase modulation**: The modulation signal is formed as a stair, the levels being calculated to eliminate certain harmonics. Not recommended for cycles that have less than 15 pulses.
- **Stepped modulation**: Each step being a certain time portion (in degrees) which is individually controling the amplitude and is used to elimate harmonics. Gives low distortion, but high amplitude.
- **Third harmonic injected PWM**: Implementation in the same way as for the SPWM, but the references signal is not a sinusoidal wave. It consists of a 1) fundamental component 2) Third harmonic component. This method gives higher amplitude and a better utilization of the DC-source.

Space Vector Pulse width Modulation (SVPWM) generates the appropriate gate drive waveform for each PWM cycle. The inverter is treated as one single unit and can combine different switching states (number of switching states depends on levels). The SVPWM provides unique switching time

calculations for each of these states [6]. This technique can easily be changed to higher levels and works with all kinds of multilevel inverters (cascaded, capacitor clamped, diode clamped). The three vectors that form one triangle will provide duty cycle time for each, giving the desired voltage vector (V_{ref}). This can be described with the formula: $V = (T_1 V_1 + T_2 V_2 + T_3 V_3)/Tc$

Modulation Technique	Line Voltage THD	Stator Current THD	Fundamental Voltage (Volt)
SPWM	44.3%	4.03%	269,9
Trapizoidal	40.08%	2.55%	299,8
Staircase	44.53%	2.55%	302,8
Stepped	36.68%	2.08%	317,6
Third Harmonic	35.62%	1.38%	332,6
Offset Voltage	34.84%	1.23%	346,3

Table 4: Different Modulation Techniques and their THD

SVPWM also have good utilization of the DC link voltage, low current ripple and relative easy hardware implementation. Compared to the SPWM, the SVPWM has a 15% higher utilization ratio of the voltage [22][24]. This features makes it suitable for high voltage high power applications, such as renewable power generation. As the number of level increase the redundant switching states increases and also the complexity of selection of the switching states [7]. So, deciding which level is right for a certain application it is important to find a balance between losses and specification of the positioning of the reference vector.

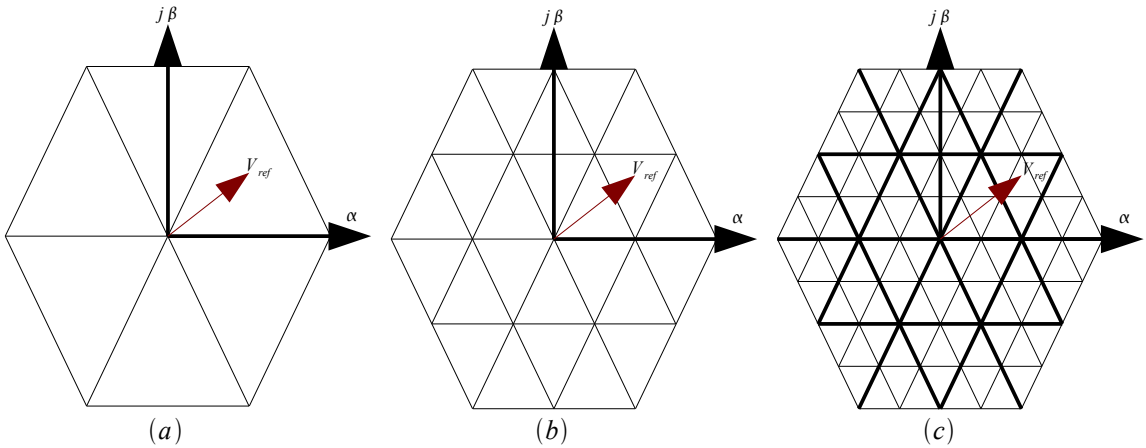


Figure 15: Space Vector diagram of a (a) two-level inverter (b) three-level inverter (c) five-level inverter

3.2 Space Vector Pulse Width Modulation for two-level converters

The circuit in Fig. 16 demonstrates the foundation of a two-level voltage source converter. It has six switches (sw1-sw6) and each of these are represented with an IGBT switching device. A, B and C represents the output for the phase shifted sinusoidal signals. Depending on the switching combination the inverter will produce different outputs, creating the two-level signal. The biggest difference from other PWM methods is that the SVPWM uses a vector as a reference. This gives the advantage of a better overview of the system.

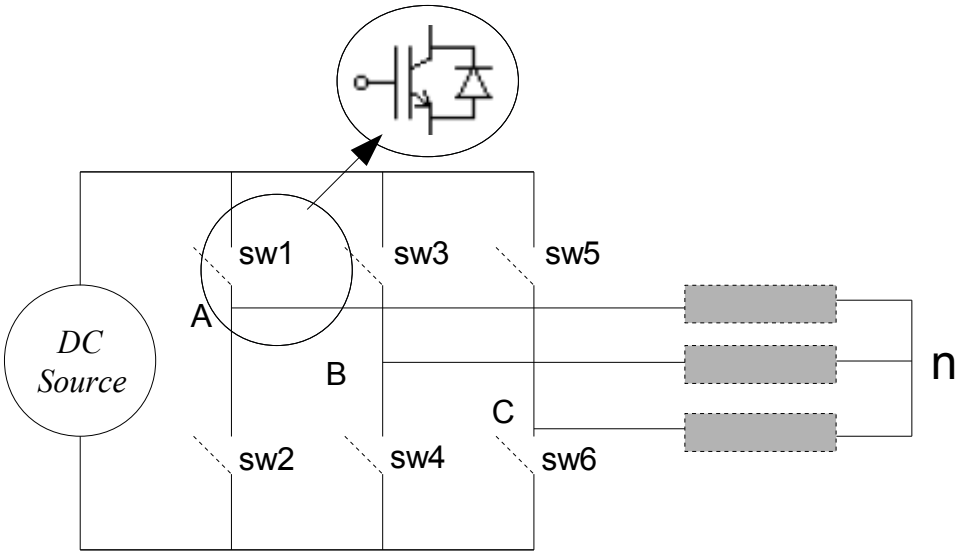


Figure 16: Three-level three-phase inverter, with a load and neutral point

3.2.1 Reference Vector

The reference vector is represented in a αβ-plane. This is a two-dimensional plane transformed from a three-dimensional plane containing the vectors of the three phases. The switches being ON or OFF is determined by the location of the reference vector on this αβ-plane.

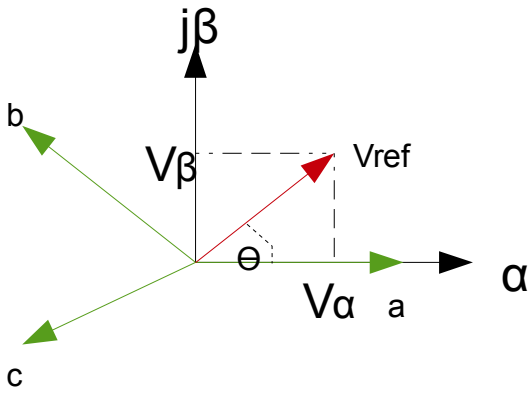


Figure 17: The reference vector in the two and three dimensional plane

Table 5 shows that the switches can be ON or OFF, meaning 1 or 0. The switches 1,3,5 are the upper switches and if these are 1 (separately or together) it turns the upper inverter leg ON and the terminal voltage (V_a, V_b, V_c) is positive ($+V_{DC}$). If the upper switches are zero, then the terminal voltage is zero).

Switching	***a***			***b***			***c***		
states	S1	S2	V_{an}	S3	S4	V_{bn}	S5	S6	V_{cn}
1	ON	OFF	V_{DC}	ON	OFF	V_{DC}	ON	OFF	V_{DC}
0	OFF	ON	0	OFF	ON	0	OFF	ON	0

Table 5: Switching states for each phase leg

The lower switches are complementary to the upper switches, so the only possible combinations are the switching states: 000, 001, 010, 011, 100, 110, 110, 111. This means that there are 8 possible switching states, for which two of them are zero switching states and six of them are active switching states. These are represented by active (V_1-V_6) and zero (V_0) vectors. The zero vectors are placed in the axis origin (Fig, 18).

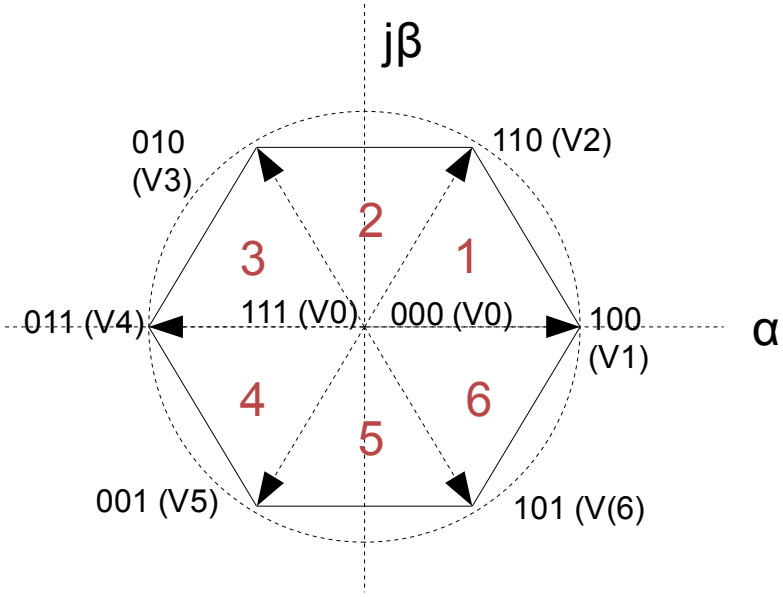


Figure 18: Space voltage vectors in different sectors

It is assumed that the three-phase system is balanced:

$$V_{a0}+V_{b0}+V_{c0}=0$$

These are the instantaneous phase voltages:

$$V_a=Vsin(\theta t)$$

$$V_b=Vsin(\theta t+\frac{2\pi}{3})$$

$$V_c=Vsin(\theta t+\frac{4\pi}{3})$$

When the three phase voltages are applied to a AC machine a rotating flux is created. This flux is

represented as one rotating voltage vector. The magnitude and angle of this vector can be calculated with Clark's Transformation:

$V_{ref} = V_\alpha + jV_\beta = \frac{2}{3}(V_a + aV_b + a^2 V_c)$, a is given by

$a = e^{j\frac{2\pi}{3}}$

The magnitude and angle (determining in which sector the reference vector is in) of the reference vector is:

$|V_{ref}| = \sqrt{V_\alpha^2 + V_\beta^2} \qquad \theta = \tan^{-1}(\frac{V_\beta}{V_\alpha})$

The reference voltage can then be expresses as:

$V_\alpha + jV_\beta = \frac{2}{3}(V_a + e^{j\frac{2\pi}{3}} V_b + e^{-j\frac{2\pi}{3}} V_c)$

Inserting the phase shifted values for Va, Vb and Vc gives:

$$V_\alpha + jV_\beta = \underbrace{\frac{2}{3}(V_a + \cos(\frac{2\pi}{3})V_b + \cos(\frac{2\pi}{3})V_c)}_{V_\alpha} + j\underbrace{\frac{2}{3}(\sin(\frac{2\pi}{3})V_b - \sin(\frac{2\pi}{3})V_c)}_{V_\beta}$$

The voltage vectors on the alpha and beta axis can then be described as:

$$\begin{pmatrix} V_\alpha \\ V_\beta \end{pmatrix} = \frac{2}{3} \cdot \begin{pmatrix} 1 & \cos(\frac{2\pi}{3}) & \cos(\frac{2\pi}{3}) \\ 0 & \sin\frac{2\pi}{3} & -\sin(\frac{2\pi}{3}) \end{pmatrix} \cdot \begin{pmatrix} V_a \\ V_b \\ V_c \end{pmatrix} = \frac{2}{3} \cdot \begin{pmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{(3)}}{2} & -\frac{\sqrt{(3)}}{2} \end{pmatrix} \cdot \begin{pmatrix} V_a \\ V_b \\ V_c \end{pmatrix}$$

$V_\alpha = \frac{2}{3}(V_a - \frac{1}{2}V_b - \frac{1}{2}V_c)$

$V_\beta = \frac{2}{3}(\frac{\sqrt{(3)}}{2}V_b - \frac{\sqrt{(3)}}{2}V_c)$

Having calculated V_α, V_β, V_{ref} and the reference angle,the first step is taken. The next step is to calculate the duration time for each vector V_1-V_6.

3.2.2 Time Duration

V_{ref} can be found with two active and one zero vector. For sector 1 (0 to $\pi/3$): V_{ref} can be located with V_0, V_1 and V_2. V_{ref} in terms of the duration time can be considered as:

$V_{ref} \cdot T_c = V_1 \cdot \frac{T_1}{T_c} + V_2 \cdot \frac{T_2}{T_c} + V_0 \cdot \frac{T_0}{T_c}$

$$V_{ref} = V_1 \cdot T_1 + V_2 \cdot T_2 + V_0 \cdot T_0$$

The total cycle is given by:

$$T_c = T_1 + T_2 + T_0$$

The position of V_{ref}, V_1, V_2 and V_0 can be described with its magnitude and angle:

$$V_{ref} = V_{ref}\, r^{j\theta},\ V_1 = \frac{2}{3} V_{DC},\ V_2 = \frac{2}{3} V_{DC} e^{j\frac{\pi}{3}},\ V_0 = 0$$

$$T_c \cdot V_{ref} \cdot \begin{pmatrix} \cos(\theta) \\ \sin(\theta) \end{pmatrix} = T_1 \cdot \frac{2}{3} V_{DC} \cdot \begin{pmatrix} 1 \\ 0 \end{pmatrix} + T_2 \cdot \frac{2}{3} \cdot V_{DC} \cdot \begin{pmatrix} \cos(\frac{\pi}{3}) \\ \sin(\frac{\pi}{3}) \end{pmatrix}$$

Dividing these in real and imaginary parts simplifies the calculation for each duration time:

$$\text{Real part}: T_c \cdot V_{ref} \cdot \cos(\theta) = T_1 \frac{2}{3} V_{DC} + T_2 \frac{1}{3} V_{DC}$$

$$\text{Imaginary part}: T_c \cdot V_{ref} \cdot \sin(\theta) = T_2 \frac{1}{\sqrt{(3)}} V_{DC}$$

T_1 and T_2 is then given by:

$$T_1 = T_c \underbrace{\frac{\sqrt{3} \cdot V_{ref}}{V_{DC}}}_{\text{modulationindex a}} \sin(\frac{\pi}{3} - \theta) = T_c \cdot a \cdot \sin(\frac{\pi}{3} - \theta)$$

$$T_2 = T_c \underbrace{\frac{\sqrt{3} \cdot V_{ref}}{V_{DC}}}_{\text{modulationindex a}} \sin(\theta) = T_c \cdot a \cdot \sin(\theta) \qquad 0 < \theta < \frac{\pi}{3}$$

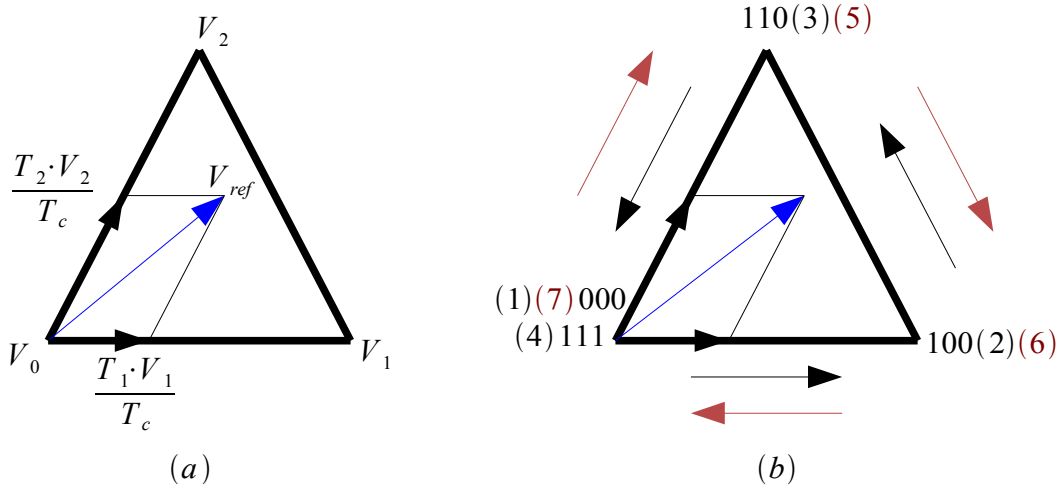


Figure 19: Space vector diagram for Sector 1 (a) described with the duty cycle for each vector (b) described with it switching states

The general calculation to receive the duty times in the rest of the sectors is given by:

$$T_1 = T_c \cdot a \cdot \sin\left(\frac{\pi}{3} - \theta + \frac{n-1}{3} \cdot \pi\right) = T_c \cdot a\left[\sin\left(\frac{n}{3}\pi\right)\cos(\theta) - \cos\left(\frac{n}{3}\pi\right)\sin(\theta)\right]$$

$$T_2 = T_c \cdot a \cdot \sin\left(\theta - \frac{n-1}{3}\pi\right) = T_c \cdot a\left[-\cos(\theta)\sin\left(\frac{n-1}{3}\pi\right) + \sin(\theta)\cos\left(\frac{n-1}{3}\pi\right)\right]$$

$$T_0 = T_c - T_1 - T_2$$

Choosing n as the number of the sector (n=1,2,3,4,5,6) the calculations for the time duration in each sector can be calculated.

Sw states			***Corresponding Voltage Vectors***		
a	***b***	***c***	***Vector***	***Magnitude***	***Angle***
0	0	0	V_0	0	0
1	1	1			
1	0	0	V_1	$\frac{2}{3}V_{DC}$	0
1	1	0	V_2	$\frac{2}{3}V_{DC}$	$\frac{\pi}{3}$
0	1	0	V_3	$\frac{2}{3}V_{DC}$	$\frac{2\pi}{3}$
0	1	1	V_4	$\frac{2}{3}V_{DC}$	π
0	0	1	V_5	$\frac{2}{3}V_{DC}$	$\frac{4\pi}{3}$
1	0	1	V_6	$\frac{2}{3}V_{DC}$	$\frac{5\pi}{3}$

Table 6: All switching states and its corresponding voltage vectors

Sector	***Duration times***		
	T_1	T_2	T_0
1	$T_c \cdot a \cdot \sin\left(\frac{\pi}{3} - \theta\right)$	$T_c \cdot a \cdot \sin(\theta)$	$T_c - T_1 - T_2$
2	$T_c \cdot a \cdot \sin\left(\frac{2\pi}{3} - \theta\right)$	$T_c \cdot a \cdot \sin\left(\theta - \frac{\pi}{3}\right)$	$T_c - T_1 - T_2$
3	$T_c \cdot a \cdot \sin(\pi - \theta)$	$T_c \cdot a \cdot \sin\left(\theta - \frac{2\pi}{3}\right)$	$T_c - T_1 - T_2$
4	$T_c \cdot a \cdot \sin\left(\frac{4\pi}{3} - \theta\right)$	$T_c \cdot a \cdot \sin(\theta - \pi)$	$T_c - T_1 - T_2$
5	$T_c \cdot a \cdot \sin\left(\frac{5\pi}{3} - \theta\right)$	$T_c \cdot a \cdot \sin\left(\theta - \frac{4\pi}{3}\right)$	$T_c - T_1 - T_2$
6	$T_c \cdot a \cdot \sin(2\pi - \theta)$	$T_c \cdot a \cdot \sin\left(\theta - \frac{5\pi}{3}\right)$	$T_c - T_1 - T_2$

Table 7: Duration time for each sector

3.2.3 Switching Time

Duty Cycle

For each sector there are 7 switching states for each cycle. It always starts and ends with a zero vector. This also means that there is no extra switching state needed when changing the sector. The uneven numbers travel counter clockwise in each sector and the even sectors travel clockwise.

Duty cycle for sector 1

For sector 1 it goes through these switching states: 000-100-110-111-110-100-000, one round and then back again. This is during the time T_c and it has to be divided amongst the 7 switching states, three of them being zero vectors:

$$T_c = \frac{T_0}{4} + \frac{T_1}{2} + \frac{T_0}{2} + \frac{T_2}{2} + \frac{T_1}{2} + \frac{T_0}{4}$$

This can be calculated for all the sectors (Fig. 21). There are different kinds of waveforms: centre aligned and edge aligned. Edge align waveforms makes it easier when comparing with the carrier wave, but the centre aligned has the advantage of reducing the harmonics and also reducing noise[5].

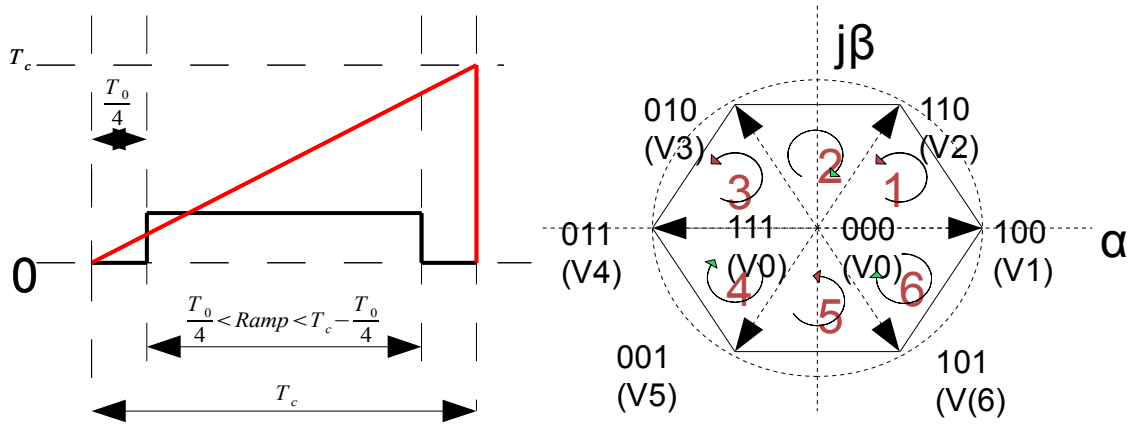


Figure 20: (a) Illustration ramp (b) Space vector diagram with every switching state and sequence

Sequencing of Switching States in Sector 1-6

Following the pattern for each sector results in a ON/OFF waveform for each sector and phase. Each switch has it switching information depending on where the reference vector is located. The waveforms are shown in the Fig. 22. For Sector 1, the switch is ON between $T_0/4$ and T_c-$T_0/4$ in the first phase, between $T_0/4+T_1/2$ and T_c-($T_0/4+T_1/2$) for the second phase and so on. For the switch to know that it should be switched ON at these specific times requires a timer that can give this information. Something like a ramp or a repeated sequence can be used as a reference (Fig. 20a), so the ramp indicates that the switches should be ON/OFF at specific times.

5 http://www.freescale.com/webapp/sps/site/overview.jsp?code=WBT_MOTORPWMTUT_WP 10/01/12

Sector	*Duty Time Upper Switches*		*Duty Time Lower Switches*	
1	S1	$T_1+T_2+\frac{T_0}{2}$	S2	$\frac{T_0}{2}$
	S3	$T_2+\frac{T_0}{2}$	S4	$T_1+\frac{T_0}{2}$
	S5	$\frac{T_0}{2}$	S6	$T_1+T_2+\frac{T_0}{2}$
2	S1	$T_2+\frac{T_0}{2}$	S2	$T_1+\frac{T_0}{2}$
	S3	$T_1+T_2+\frac{T_0}{2}$	S4	$\frac{T_0}{2}$
	S5	$\frac{T_0}{2}$	S6	$T_1+T_2+\frac{T_0}{2}$
3	S1	$\frac{T_0}{2}$	S2	$T_1+T_2+\frac{T_0}{2}$
	S3	$T_1+T_2+\frac{T_0}{2}$	S4	$\frac{T_0}{2}$
	S5	$T_2+\frac{T_0}{2}$	S6	$T_1+\frac{T_0}{2}$
4	S1	$\frac{T_0}{2}$	S2	$T_1+T_2+\frac{T_0}{2}$
	S3	$T_2+\frac{T_0}{2}$	S4	$T_1+\frac{T_0}{2}$
	S5	$T_1+T_2+\frac{T_0}{2}$	S6	$\frac{T_0}{2}$
5	S1	$T_2+\frac{T_0}{2}$	S2	$T_1+\frac{T_0}{2}$
	S3	$\frac{T_0}{2}$	S4	$T_1+T_2+\frac{T_0}{2}$
	S5	$T_1+T_2+\frac{T_0}{2}$	S6	$\frac{T_0}{2}$
6	S1	$T_1+T_2+\frac{T_0}{2}$	S2	$\frac{T_0}{2}$
	S3	$\frac{T_0}{2}$	S4	$T_1+T_2+\frac{T_0}{2}$
	S5	$T_2+\frac{T_0}{2}$	S6	$T_1+\frac{T_0}{2}$

Table 8: Duty time for each sector

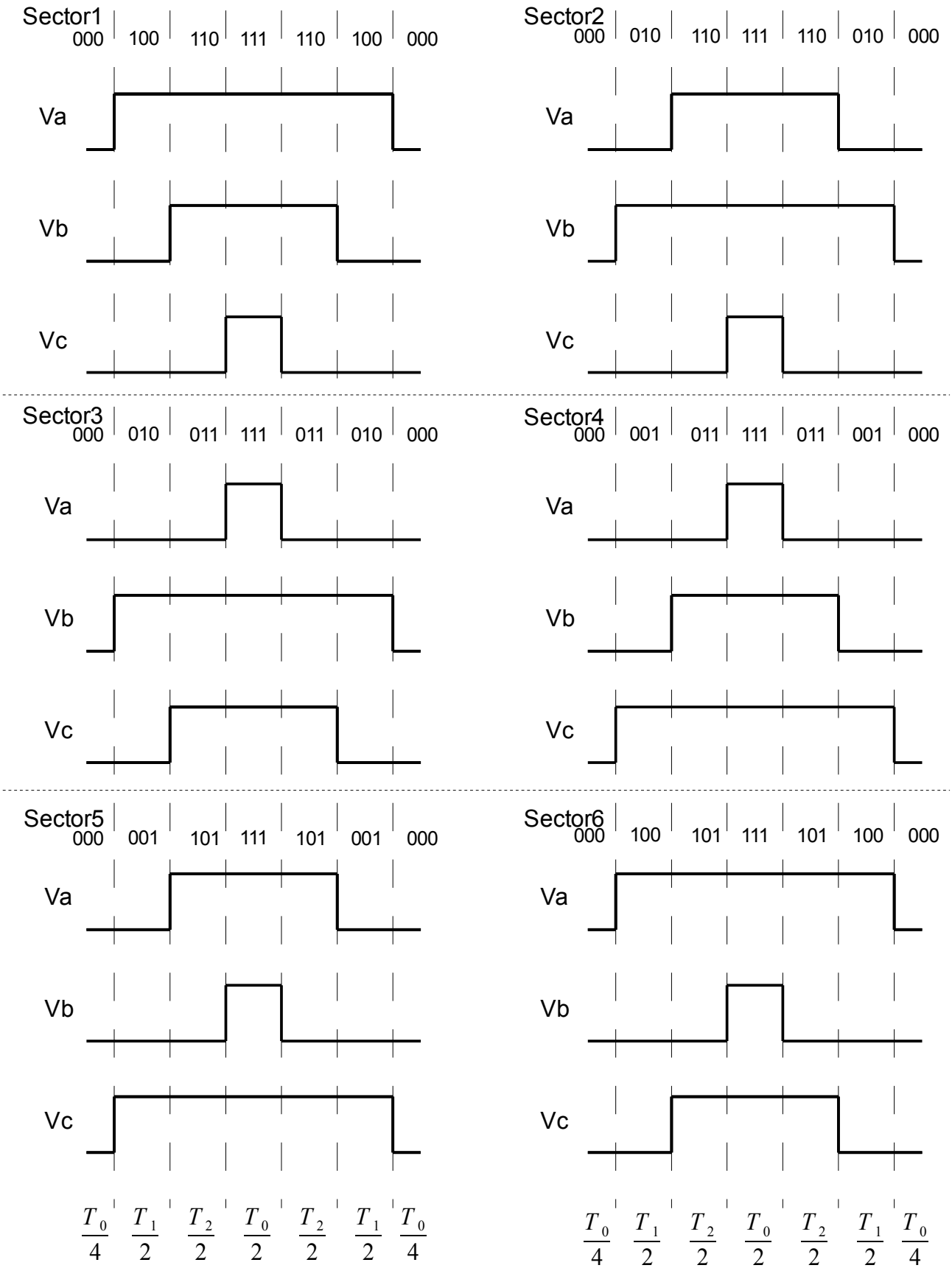


Figure 21: Waveform showing sequencing of switching states for all the regions

3.2.4 Implementation in Matlab/Simulink

To test the theory the calculations from 3.2.2 and 3.2.3 has been simulated using Matlab/Simulink. Some specifications: Amplitude and DC-voltage has been chosen as 1V, sampling time T_s = 1/10000s, cycle time for the ramp T_c = 1/1000s, the three phases are phase sifted 120 degrees apart and have the frequency of a typical Swedish grid, $2\pi 50$ rad/s. Values for the ramp (Part IV): Period $T_r = T_c$ = 1/1000s, ramp amplitude is 1/1000V. Fig. 22 shows a overview of the block diagram in Simulink and the different parts where each calculatation is done:

- Part I – $\alpha\beta$ -Transformation
- Part II – Reference voltage vector V_{ref}, angle θ , modulationindex a
- Part III – Sector Selection (Appendix 1)
- Part IV – Switching Times Calculation
- Part V – Inverter Output

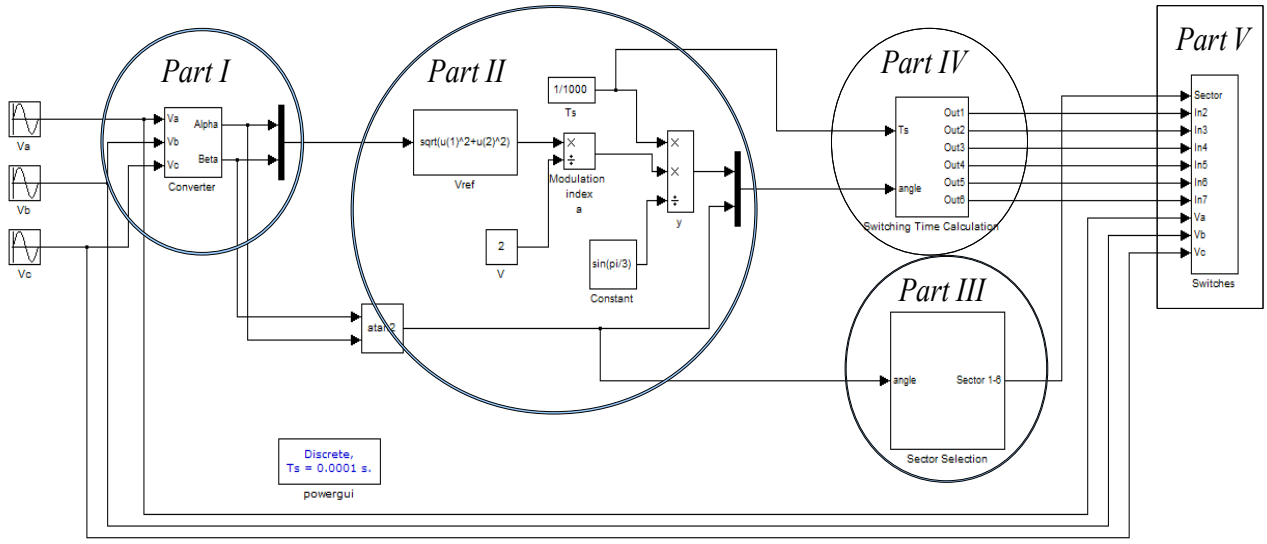


Figure 22: Overview of the two-level inverter made in Simulink and the different calculation parts

Part I

The voltage vectors: V_a, V_b, V_c is replaced with V_α and V_β. As seen in Fig. 17, V_a and V_α have the same direction, but different magnitude. The same expression is seen in Fig. 23 as a amplitude difference. With the αβ-transformation the signals are demonstrated in a two-dimensional plane, making it easier to use in the calculations done in the other parts.

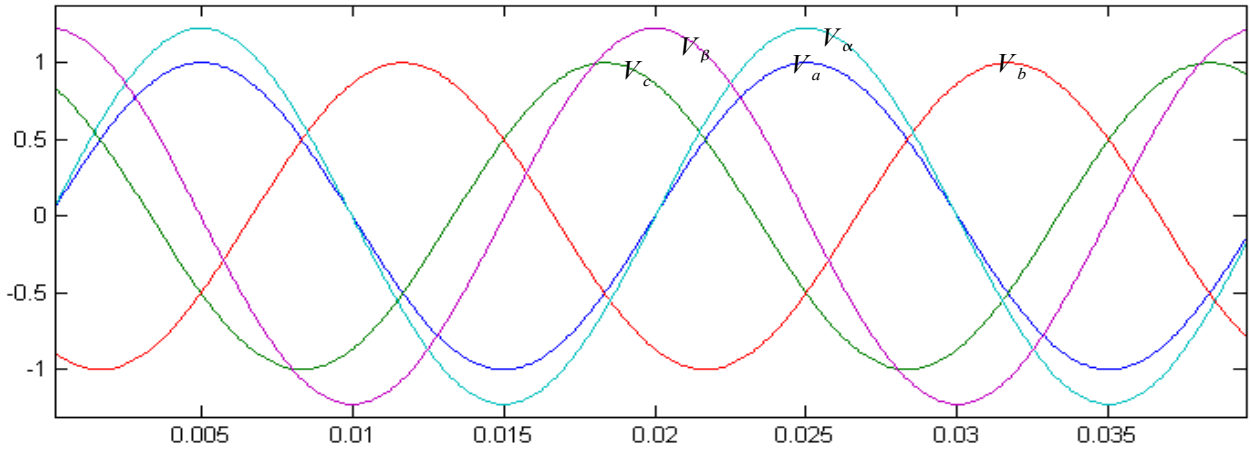


Figure 23: αβ-transformation

Part II

The reference voltage vector V_{ref}, angle θ and modulationindex a is calculated as shown in chapter 3.2.

Part III

Appendix 1 shows the block diagram made in Simulink. The calculations are based on the vector reference angle. If V_{ref} is between 0 and $\pi/3$ it is in sector 1, if it is between $\pi/3$ and $2pi/3$ it is in sector 2 and so on.

Part IV

Fig. 24 gives one example of one time calculation compared with the ramp. If the signal is greater then the ramp the value one is given, else zero.

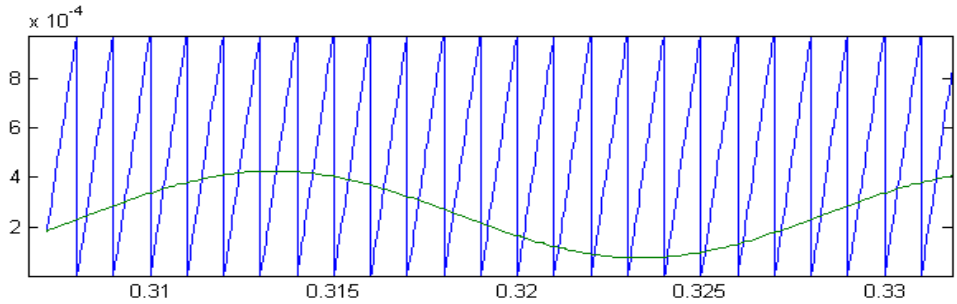


Figure 24: Time signal compared with a ramp

Part V

In Part V the switching information is fed to a Universal Bridge (representing the inverters), that is connected to three loads and a neutral point between them (Fig. 23). The DC-voltage source is set to 1 V. To get the phase voltage, for example V_{ab}: Substract V_b from V_a. The output for V_{ab}, V_{bc}, V_{ac} is shown in Fig. 24 and also compared to the input sinusoidal waves. Appendix 4 shows the output for all three phases.

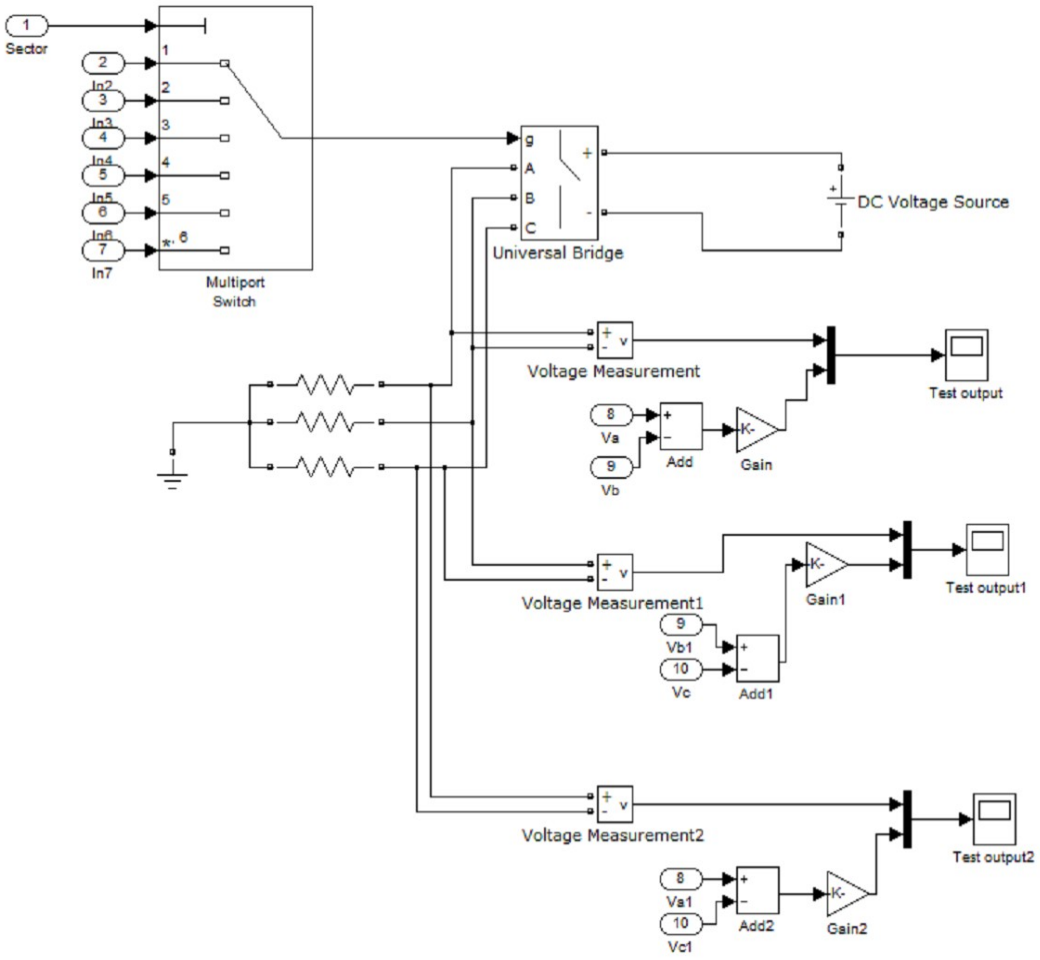


Figure 25: Inverter ouput scheme

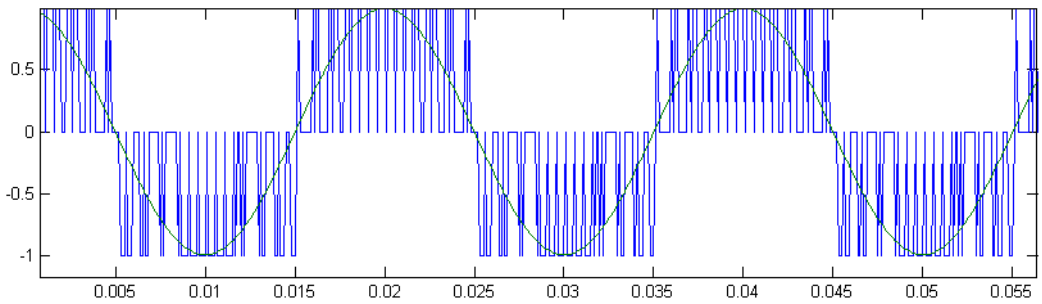


Figure 26: Two-level voltage ouput V_{bc}, compared to input signal V_{bc}

3.2.5 Conclusions

In chapter 3.2 the SVPWM for a two-level neutral-point-clamped voltage source inverter has been presented. The two voltage level ($0V_{DC}$ and $1V_{DC}$) can with help from the inverter switches create the two levels in the inverter output (one level for line-to-nutral voltage). Calculating the duty cycle (the switches ON-time) for each switch, gives a sinusoidal resembling waveform in the output.

3.3 Space Vector Pulse Width Modulation for three-level converters

Fig. 27 shows a three-level neutral point clamped inverter. It contains 12 switching devices and also supplied with two capacitors connected in series. Both are charged with V_{DC}. The point between these capacitors is the DC-voltage neutral point. Each phase leg consists of 4 series-connected switching devices (IGBT's) and two clamping diodes. Their job is to clamp the six middle switches potential to the DC-link point at zero. Specific combinations of the twelve switches gives the three-level output voltage.

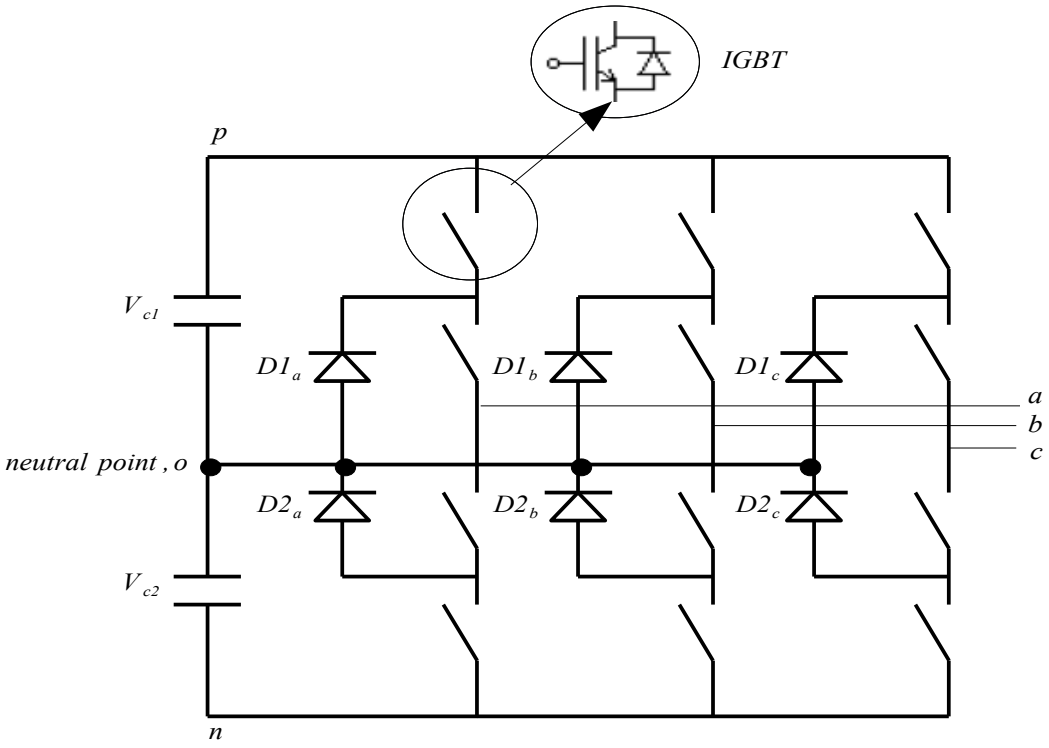


Figure 27: A three-level, three-phase neutral point clamped inverter

The four switches in one phase leg can only be turned on two at a time and so be connected to the DC-link points p, o, n. These are represented with the switching states P, O and N. This means that three voltage levels can be created using O as the reference.

The advantages of three-level converters instead of two-level:

- Higher levels means that the output waveform resembles the sinusoidal waveform more. This also means that the harmonic distortion is decreased.
- Smaller voltage levels are used. This means smaller ΔV , which means reduced stress on the motor bearings.
- The clamping diodes limits the voltage across the OFF-state switching devices to one capacitor voltage level (half of the DC-link voltage). This reduces the voltage, so medium rated semiconductor devices can be used for high-voltage high-level applications.

One big downside of the higher level inverter is the neutral point balancing problem.

S_{1x}	ON	OFF	OFF
S_{2x}	ON	ON	OFF
S_{3x}	OFF	ON	ON
S_{4x}	OFF	OFF	ON
V_{x0}	V_{DC}	0	$-V_{DC}$
Switching State	P	O	N

Table 9: Switching combination and switching states for a three-level inverter (one phase-leg)

3.3.1 Switching States

For a three-level three-phase inverter there are 27 switching states (Fig. 26). These states represent the connection to the different DC-link points. If there is a load connected to the output of these states the inverter will generate a output phase voltage. This can be calculated as follows:

$$V_{a0}=(2S_{1a}-S_{1b}-S_{1c})+(2S_{2a}-S_{2b}-S_{2c})$$
$$V_{b0}=(2S_{1b}-S_{1a}-S_{1c})+(2S_{2b}-S_{2a}-S_{2c})$$
$$V_{c0}=(2S_{1c}-S_{1b}-S_{1a})+(2S_{2c}-S_{2b}-S_{2a})$$

These are the line-to-neutral voltages. To receive the line-to-line voltage:

$$V_{ab}=V_{a0}-V_{b0}$$
$$V_{bc}=V_{b0}-V_{c0}$$
$$V_{ca}=V_{c0}-V_{a0}$$

There is requested to generate five levels of outputs, so the three-level can be created. These levels are $2V_{DC}$, V_{DC}, 0, $-V_{DC}$ and $-2V_{DC}$ (for the line-to-line voltage). All 27 switching states and 19 voltage vectors and the generated output voltage is shown in Table 11.

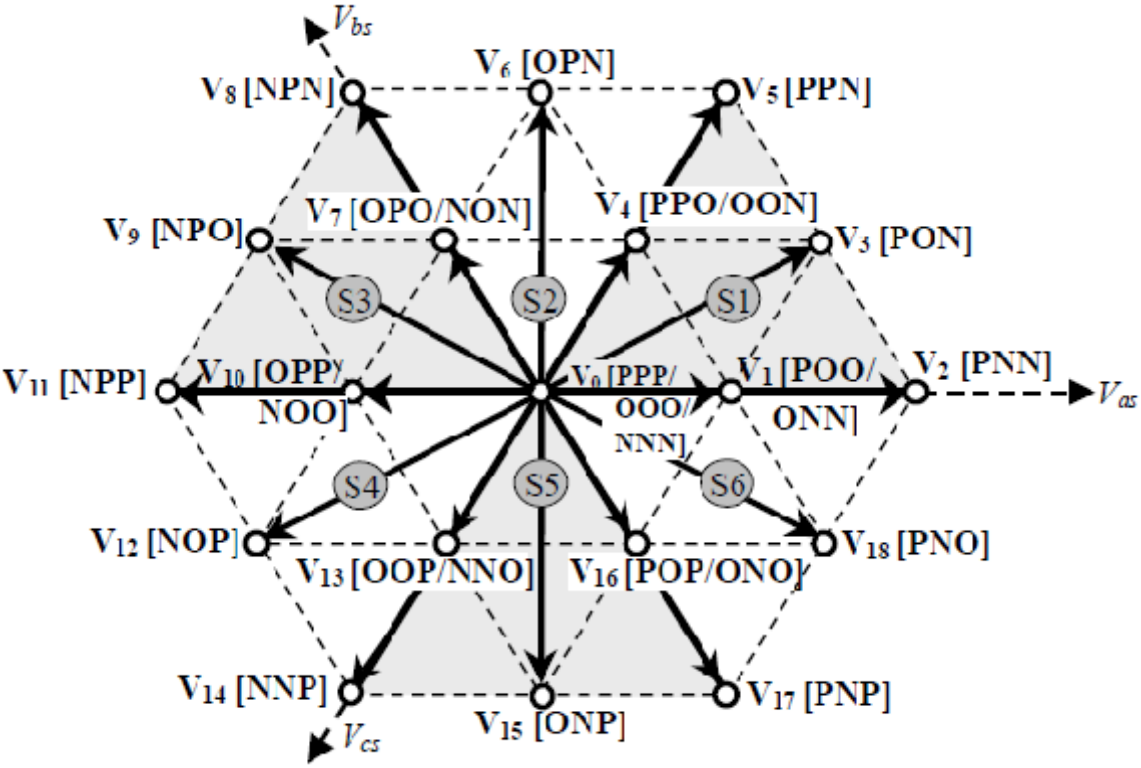


Figure 28: Space vector diagram for a three-level inverter demonstrating 19 voltage vectors and 27 switching states

As for the two-level inverter the reference vector is given with the help from three voltage vectors. For the three-level converter each sector also is divided into 4 regions, specifying the output even more. Based on the magnitude the voltage vectors can be defined as:

- Zero Voltage Vectors (ZVV): V=0 (redundant sw states)
- Small Voltage Vectors (SVV): V1,4,7,10,13,16 (redundant sw states)
- Medium Voltage Vectors (MVV): V3,6,9,12,15,18
- Large Voltage Vectors (LVV): V2,5,8,11,14,17

3.3.2 Time Duration

To describe the reference voltage vector V_{ref}, the space vector transformations comes in handy:

$$V_{ref} = \frac{2}{3}(V_{a0} + V_{b0} \cdot e^{j\frac{2}{3}\pi} + V_{c0} \cdot e^{-j\frac{2}{3}\pi})$$

$$V_{ref} = V \cdot e^{j(\omega_0 t - \gamma_0)} = V < \theta_0$$

V_{ref} can be described with the three nearest voltage space vectors. This selection is based on the magnitude of the V_{ref} and its angle. For one cycle:

$$V_{ref} = T_1 V_x + T_2 V_y + T_3 V_z$$

Ta, Tb and Tc for Sector 1, Region 3 (Fig. 29b)

If V_2 Is chosen as the reference axis (maximum magnitude as units) the voltage vectors on the axis can be described as:

$$V_x = V_1 = \frac{1}{2},\ V_y = V_3 = \frac{\sqrt{3}}{2} \cdot e^{j\frac{\pi}{6}},\ V_z = V_4 = \frac{1}{2} \cdot e^{j\frac{\pi}{3}}$$

and the reference vector as:

$$V_{ref} = \underbrace{V_u}_{V} \cdot e^{j\theta} \Big/ \frac{4}{3} V_{DC}$$

V_{ref} in forms of the real and imaginary axis:

$$V_u(\cos(\theta) + j\sin(\theta)) = \frac{1}{2} T_1 + \frac{\sqrt{3}}{2}[\cos(\frac{\pi}{6}) + j\sin(\frac{\pi}{6})] T_2 + \frac{1}{2}[\cos(\frac{\pi}{3}) + j\sin(\frac{\pi}{3})] T_3$$

Dividing the formula in real and imaginary part eases the calculations for the duty cycles:

$$Real\ part: \frac{1}{2} T_1 + \frac{\sqrt{3}}{2} \cos(\frac{\pi}{6}) T_2 + \frac{1}{2} \cos(\frac{\pi}{3}) T_3 = V_u \cdot \cos(\theta)$$

$$Imaginary\ part: \frac{\sqrt{3}}{2} \sin(\frac{\pi}{6}) T_2 + \frac{1}{2} \sin(\frac{\pi}{3}) T_3 = V_u \cdot \sin(\theta)$$

The duty cycles is then given in form of:

$$T_1 = 1 - 2 \underbrace{(\frac{2V_u}{\sqrt{3}})}_{modulation\ index\ a} \sin(\theta) = 1 - 2 \cdot a \cdot \sin(\theta)$$

$$T_2 = 2 \cdot a \cdot \sin(\theta + \frac{\pi}{3}) - 1$$

$$T_3 = 2 \cdot a \cdot \sin(\theta - \frac{\pi}{3}) + 1$$

In similar way the calculations for every sector and region can be calculated (Table 10). Having the duration time for the vectors will give information about the duty cycle for each switch.

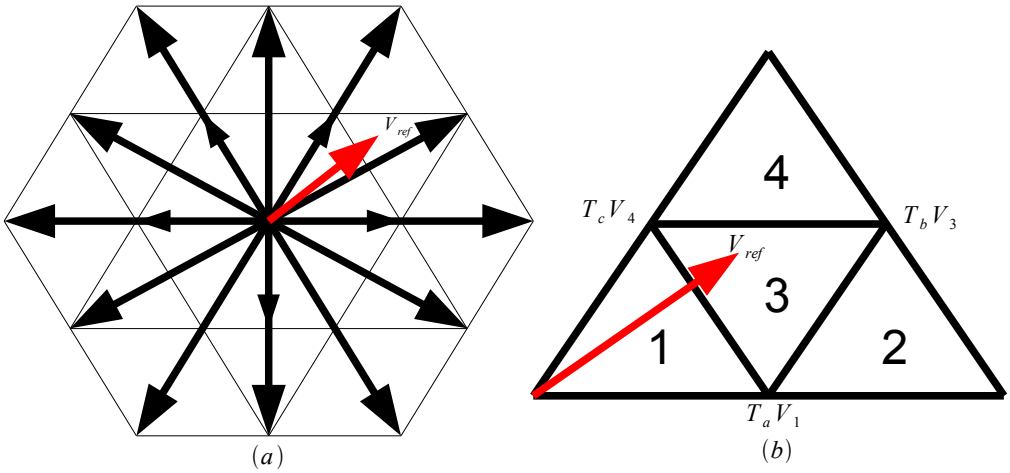


Figure 29: Space vector diagram for (a) all sectors (b) sector 1

Region Selection

The region selection is done as in [17]. The regions are given as:

$V_\alpha + \frac{\sqrt{3}}{3} V_\beta - \frac{V_{DC}}{3} < 0$ for sector 1. If this is not fulfilled, the vector is in region 2:

$V_\alpha - \frac{\sqrt{3}}{3} V_\beta - \frac{V_{DC}}{3} > 0$ If none of the above are true, the vector is in region 3:

$V_\alpha - \frac{\sqrt{3}}{6} V_{DC} < 0$. If none of these are fulfilled the vector is in region 4.

Sector	Region 1	Region 2	Region 3	Region 4
1	$aT_c\sin(\frac{\pi}{3}-\theta)$ $\frac{T_c}{2}[1-2\text{asin}(\theta+\frac{\pi}{3})]$ $aT_c\sin(\theta)$	$T_c[1+a\sin(\theta-\frac{\pi}{3})]$ $-aT_c\sin(\theta)$ $\frac{-T_c}{2}[2a\sin(\theta+\frac{\pi}{3})-1]$	$\frac{T_c}{2}[1-2\text{asin}(\theta)]$ $\frac{T_c}{2}[2\text{asin}(\theta+\frac{\pi}{3})-2]$ $\frac{T_c}{2}[1+2\text{asin}(\theta-\frac{\pi}{3})]$	$\frac{T_c}{2}[2\text{asin}(\theta)-1]$ $aT_c\sin(\frac{\pi}{3}-\theta)$ $T_c[1-asin(\theta+\frac{\pi}{3})]$
2	$aT_c\sin(\frac{\pi}{3}-\theta)$ $\frac{T_c}{2}[1-2\text{asin}(\theta+\frac{\pi}{3})]$ $aT_c\sin(\theta)$	$\frac{T_c}{2}[2a\sin(\theta+\frac{\pi}{3})-1]$ $-aT_c\sin(\frac{\pi}{3}-\theta)$ $aT_c[1-\sin(\theta)]$	$\frac{T_c}{2}[1-2\text{asin}(\theta+\frac{\pi}{3})]$ $\frac{T_c}{2}[2\text{asin}(\theta)-1]$ $\frac{T_c}{2}[2\text{asin}(\frac{\pi}{3}-\theta)+1]$	$T_c[1-asin(\theta)]$ $aT_c\sin(\theta+\frac{\pi}{3})$ $\frac{T_c}{2}[2\text{asin}(\theta-\frac{\pi}{3})-1]$
3	$aT_c\sin(\theta)$ $\frac{T_c}{2}[1-2\text{asin}(\theta-\frac{\pi}{3})]$ $-aT_c\sin(\theta+\frac{\pi}{3})$	$T_c[1-a\sin(\theta-\frac{\pi}{3})]$ $-aT_c\sin(\theta+\frac{\pi}{3})$ $\frac{-T_c}{2}[2a\sin(\theta)-1]$	$\frac{T_c}{2}[2\text{asin}(\theta+\frac{\pi}{3})+1]$ $-\frac{T_c}{2}[1+2\text{asin}(\frac{\pi}{3}-\theta)]$ $\frac{T_c}{2}[1-2\text{asin}(\theta)]$	$\frac{-T_c}{2}[1-asin(\theta)]$ $aT_c\sin(\theta+\frac{\pi}{3})$ $\frac{T_c}{2}[2\text{asin}(\theta-\frac{\pi}{3})-1]$
4	$-aT_c\sin(\theta)$ $\frac{T_c}{2}[1+2\text{asin}(\theta+\frac{\pi}{3})]$ $aT_c\sin(\theta-\frac{\pi}{3})$	$\frac{T_c}{2}[2a\sin(\theta-\frac{\pi}{3})-1]$ $-aT_c\sin(\theta)$ $aT_c[1+\sin(\theta+\frac{\pi}{3})]$	$\frac{T_c}{2}[2\text{asin}(\frac{\pi}{3}-\theta)-1]$ $-\frac{T_c}{2}[1+2\text{asin}(\theta+\frac{\pi}{3})]$ $\frac{T_c}{2}[1+2\text{asin}(\theta)]$	$\frac{T_c}{2}[1+2\text{asin}(\theta+\frac{\pi}{3})]$ $aT_c\sin(\theta)$ $T_c[1+asin(\frac{\pi}{3}-\theta)]$
5	$-aT_c\sin(\theta+\frac{\pi}{3})$ $\frac{T_c}{2}[1+2\text{asin}(\theta)]$ $aT_c\sin(\frac{\pi}{3}-\theta)$	$T_c[1+a\sin(\theta)]$ $aT_c\sin(\pi\ pver\ 3-\theta)$ $\frac{-T_c}{2}[2a\sin(\theta+\frac{\pi}{3})+1]$	$\frac{T_c}{2}[2\text{asin}(\theta-\frac{\pi}{3})+1]$ $-\frac{T_c}{2}[2\text{asin}(\theta)+1]$ $\frac{T_c}{2}[2\text{asin}(\theta+\frac{\pi}{3})+1]$	$\frac{T_c}{2}[2\text{asin}(\frac{\pi}{3}-\theta)-1]$ $-aT_c\sin(\theta+\frac{\pi}{3})$ $T_c[1+asin(\theta)]$
6	$aT_c\sin(\theta+\frac{\pi}{3})$ $\frac{T_c}{2}[1+2\text{asin}(\theta-\frac{\pi}{3})]$ $-aT_c\sin(\theta)$	$-T_c[1+2a\sin(\theta)]$ $aT_c\sin(\theta+\frac{\pi}{3})$ $\frac{T_c}{2}[a\sin(\theta-\frac{\pi}{3})+1]$	$\frac{T_c}{2}[2\text{asin}(\theta)+1]$ $\frac{T_c}{2}[1-2\text{asin}(\theta+\frac{\pi}{3})]$ $\frac{T_c}{2}[2\text{asin}(\frac{\pi}{3}-\theta)-1]$	$T_c[1+a\sin(\theta-\frac{\pi}{3})]$ $-aT_c\sin(\theta)$ $\frac{-T_c}{2}[2\text{asin}(\theta+\frac{\pi}{3})-1]$

Table 10: Time expressions of voltage vectors in different sectors and regions

Switching States			Corresponding Voltage Vectors		
a	***b***	***c***	***Vector***	***Magnitude***	***Angle***
P	P	P	V_0	0V	0
O	O	O			
N	N	N			
P	O	O	V_1	$\frac{2}{3}V_{DC}$	0
O	N	N			
P	N	N	V_2	$\frac{4}{3}V_{DC}$	0
P	O	N	V_3	$\frac{2}{\sqrt{3}}V_{DC}$	$\frac{\pi}{6}$
P	P	O	V_4	$\frac{2}{3}V_{DC}$	$\frac{\pi}{3}$
O	O	N			
P	P	N	V_5	$\frac{4}{3}V_{DC}$	$\frac{\pi}{3}$
O	P	N	V_6	$\frac{2}{\sqrt{3}}V_{DC}$	$\frac{\pi}{2}$
O	P	O	V_7	$\frac{2}{3}V_{DC}$	$\frac{2\pi}{3}$
N	O	N			
N	P	N	V_8	$\frac{4}{3}V_{DC}$	$\frac{2\pi}{3}$
N	P	O	V_9	$\frac{2}{\sqrt{3}}V_{DC}$	$\frac{5\pi}{6}$
O	P	P	V_{10}	$\frac{2}{3}V_{DC}$	π
N	O	O			
N	P	P	V_{11}	$\frac{4}{3}V_{DC}$	π
N	O	P	V_{12}	$\frac{2}{\sqrt{3}}V_{DC}$	$-\frac{5\pi}{6}$
O	O	P	V_{13}	$\frac{2}{3}V_{DC}$	$-\frac{2\pi}{3}$
N	N	O			
N	N	P	V_{14}	$\frac{4}{3}V_{DC}$	$-\frac{2\pi}{3}$
O	N	P	V_{15}	$\frac{2}{\sqrt{3}}V_{DC}$	$-\frac{\pi}{2}$
P	O	P	V_{16}	$\frac{2}{3}V_{DC}$	$-\frac{\pi}{3}$
O	N	O			
P	N	P	V_{17}	$\frac{4}{3}V_{DC}$	$-\frac{\pi}{3}$
P	N	O	V_{18}	$\frac{2}{\sqrt{3}}V_{DC}$	$-\frac{\pi}{6}$

Table 11: All Switching states with their corresponding voltage vectors: magnitude and angle

3.3.3 Sequencing of Switching States

In the same way as for the two-level inverter each switch in each phase leg has its own output waveform. Each sector has 4 regions, meaning there will be: 6(sectors)*4(regions)*3(phases)*4(switches) = 288 waveforms. For the two-level there are 72 waveforms. However only 144 of these has to be calculated, because the lower switches in each phase leg are complementary to the upper switches.

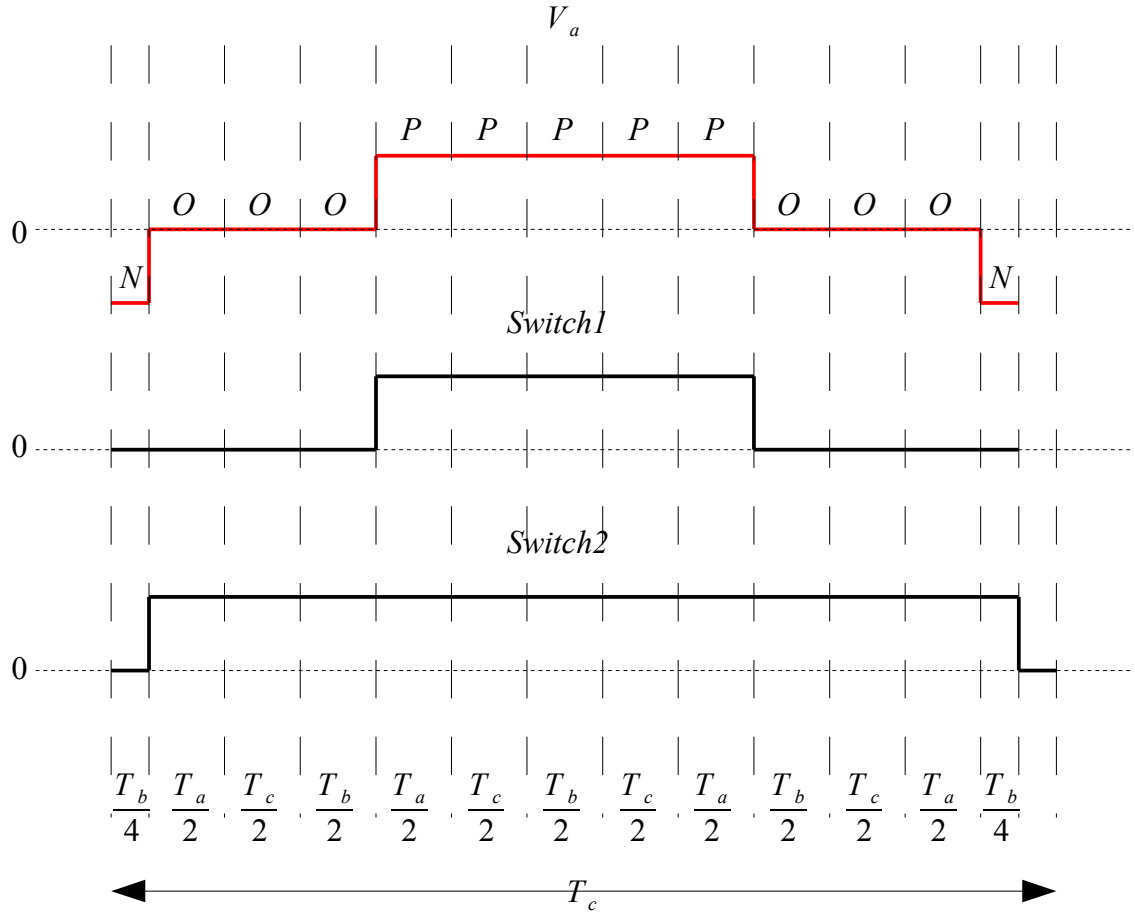


Figure 30: Waveform showing sequence of switching states for switch 1 and 2 in sector 1, region 1, phase a

Sequencing for even sectors

Sequencing for switch 1 and 2 in even sectors, ie 2,4 and 6, gives a opposite (begins with 1 to 0 to 1) waveform and cannot be compared with the ramp in the same way. For these sectors the waveform for switch 3 and 4 are used instead, because they give the complementary waveform of switch 1 and 2. Later, after the waveform is compared with the ramp, the output information can be inverted, giving switching information for switch 1 and 2 in the even sectors.

3.3.4 SVPWM of Higher Levels and Overmodulation

Higher levels

This report only covers inverters up to three levels of voltage output and the space vector modulation is designed as in Fig. 29a. It is important to add that this only is one way of calculating the three-level modulation. The sectionalizing of the sectors in the shape of these 4 regions can be done in different ways. This is only one of them. With this type of segmentation it is easier to follow the same pattern, as Fig. 29b is for Fig. 29a. This way seems however to be the easiest one, because of its symmetrical dimensions.

Overmodulation

Another factor that has not been considered in this study is the overmodulation of the space vector modulation. Overmodulation is when the reference voltage can be considered outside the diagram. Fig. 29 shows the reference signal inside the diagram. Calculations and implementation on overmodulation techniques has shown positive results as in good performance [23], but is however a very complex method to realise.

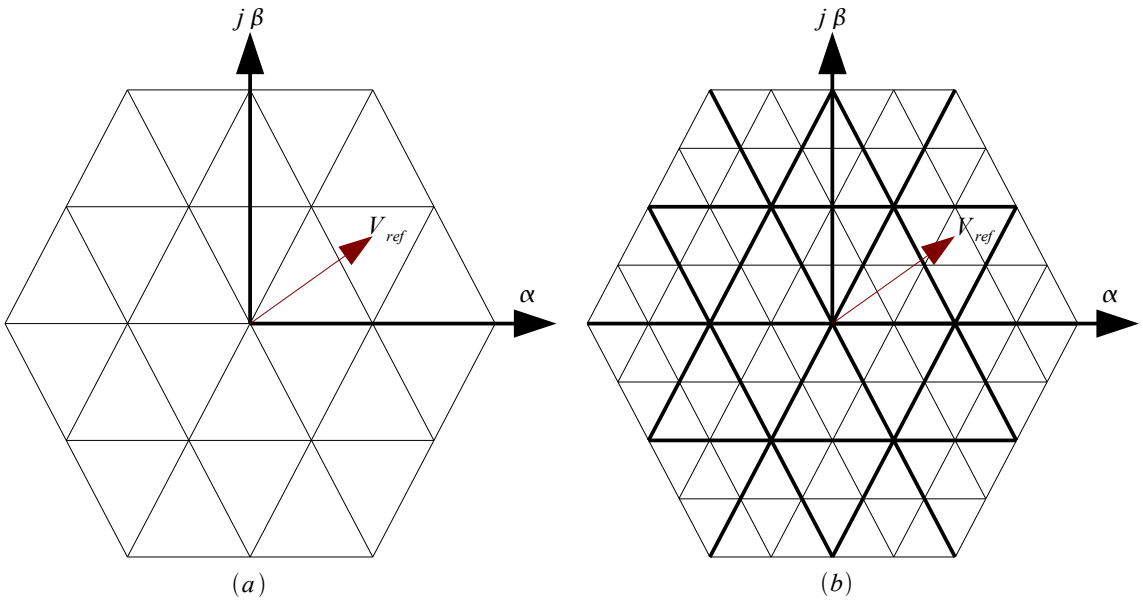


Figure 31: Space vector diagram for a (a) three-level inverter (b) five-level inverter

3.3.5 Implementation in Simulink and LabVIEW

Simulink output

The theoretical three-level calculations has been realised using Simulink. Fig. 30 shows the output voltage waveform for V_{bc} (line-to-line voltage). Some specifications: Amplitude and DC-voltage has been chosen as 1V, sampling time T_s = 1/10000, cycle time for the ramp T_c =1/1000, the three phases are phase shifted 120 degrees apart and have the frequency of a typical Swedish grid, $2\pi 50$ rad/s. The frequency being 50Hz gives T = 1/50 = 0.02s, which can be seen in Fig. 32. Values for the ramp: Period $T_r = T_c$ = 1/1000s, each period built up by 400 samples. The ramp amplitude is 1/1000V. The amplitude is 2V, because capacitor voltage is V_c = 2V, the first level producing $V_c/2$ = 1 V, the second level producing 2V.

The output is received through the steps:

- Calculations for Sector Selection and Region Selection (Appendix 2)
- Duty cycles T_a, T_b, T_c for each sector and region (Appendix 2)
- Switching time for all phases in every sector and region (Appendix 2)
- Comparison with the ramp (Appendix 3)
- Designing for line-to-line voltage (Appendix 3)

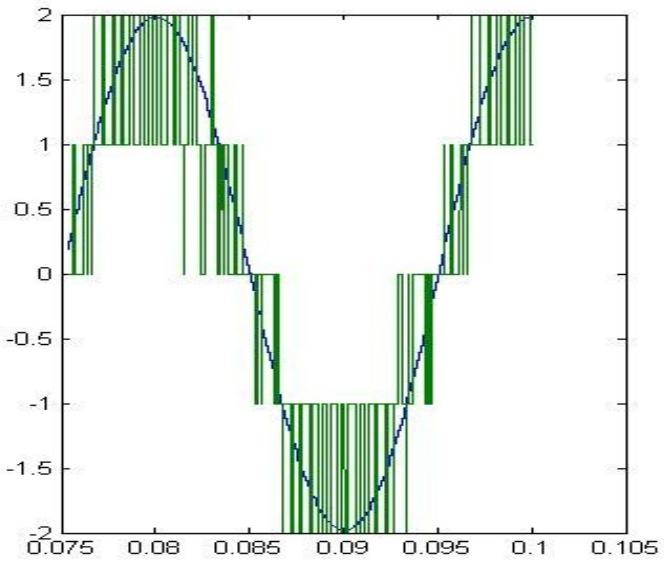


Figure 32: Output voltage waveform for V_{bc}

LabVIEW output

Fig. 33 shows the line-to-line voltage output for a three-level inverter. The implementation is done in LabVIEW. Some specifications: Amplitude and DC-voltage has been chosen as 1V, sampling time T_s = 0.02s, cycle time for the ramp T_c = 0.0005s (occurs 40 times for one T_s), the three phases are phase sifted 120 degrees apart and have the frequency of a typical Swedish grid, $2\pi 50$ rad/s. The frequency being 50Hz gives the period T = 1/50Hz = 0.02s = 20ms, which can be seen in Fig. 33. The five-level line-to-neutral voltage waveform is shown in Fig. 34.

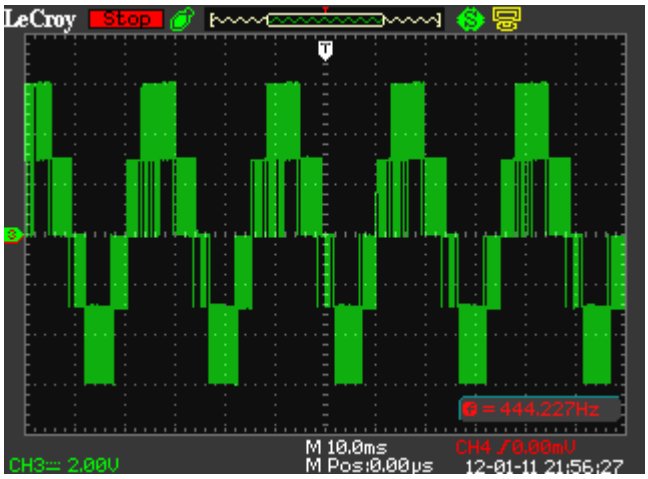


Figure 33: Output voltage waveform for V_{bc} (line-to-line)

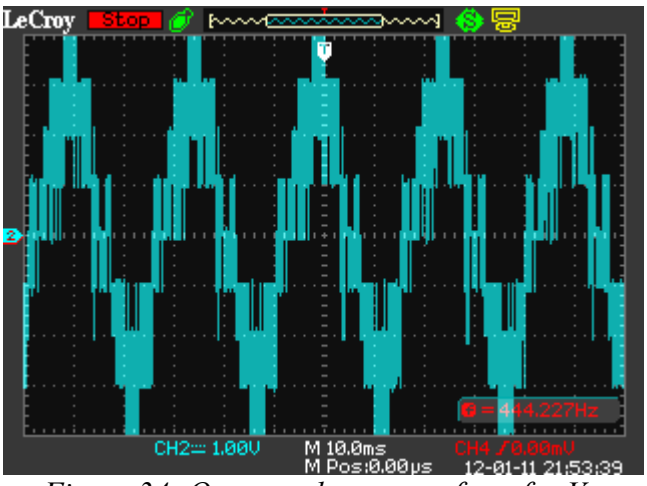


Figure 34: Output voltage waveform for V_{b0} (line-to-neutral)

LabVIEW adaptation

Simulink and LabVIEW are very different software programs. The simulations done in Simulink are not realistic or useful when using together with the FPGA. The sample time in Simulink can be chosen as high as wanted, in this case $T_s = 1/10000$, which is far to complicated to produce in reality using LabVIEW. This three-level converter is adapted to the Kalman filter that produces sinusoidal waves formed by 400 samples/period, each sample being 50µs. The T_s is then 20ms = 0.02s. Having less samples weakens the accuracy of the output.

FPGA adaptation

Also, the FPGA limits the full usage of LabVIEW. It is almost impossible to use the calculated duty cycles for each vector T_a, T_b and T_c in the form it is presented in Table 10. Each time is presented in forms of a sinus. To create this in LabVIEW would take too much memory from the FPGA. Instead the times can be presented in form of the three phases V_a, V_b and V_c:

$$V_a = \sin(\theta)$$

$$V_b = \sin(\theta + \frac{2\pi}{3}) = \sin(\theta)\cos(\frac{2\pi}{3}) + \cos(\theta)\sin(\frac{2\pi}{3}) = \sin(\theta)(-\frac{1}{2}) + \cos(\theta)(\frac{\sqrt{3}}{2}) = \sin(\frac{\pi}{3} - \theta)$$

$$V_c = \sin(\theta + \frac{4\pi}{3}) = \sin(\theta)\cos(\frac{4\pi}{3}) + \cos(\theta)\sin(\frac{4\pi}{3}) = \sin(\theta)(-\frac{1}{2}) + \cos(\theta)(-\frac{\sqrt{3}}{2}) = -\sin(\theta + \frac{\pi}{3})$$

Each of these calculations then give form to six different forms (Table 12), describing the times in Table 10. This gives new exprsession in form of Table 13.

V_a	$\sin(\theta)$	$-V_a$	$-\sin(\theta)$
V_b	$\sin(\frac{\pi}{3} - \theta)$	$-V_b$	$-\sin(\frac{\pi}{3} - \theta) = \sin(\theta - \frac{\pi}{3})$
V_c	$-\sin(\theta + \frac{\pi}{3})$	V_c	$\sin(\theta + \frac{\pi}{3})$

Table 12: The different sinusoidal waveforms represented as the three inputs: Va, Vb and Vc

Output error

As seen in Fig. 32, Fig. 33 and Fig. 34 some errors are occurring. These are specified to a certain sector (the sector being one 60º piece of the waveform in one period) and can be looked up for modification. Each individual change in the input calculations (over 200) contributes to a small change in the output. Although achieve a somehow distinct three-level form is desired, these few deviations will not affect the usage of the waveform when connecting it to the grid (after filtering).

Sector	Time	Region 1	Region 2	Region 3	Region 4
1	T_a T_b T_c	V_b $\frac{1}{2}+V_c$ V_a	$1+V_c$ V_a $V_b-\frac{1}{2}$	$\frac{1}{2}-V_a$ $-V_c-\frac{1}{2}$ $\frac{1}{2}-V_b$	$V_a-\frac{1}{2}$ V_b $1+V_c$
2	T_a T_b T_c	$-V_b$ $\frac{1}{2}-V_a$ $-V_c$	$-V_c-\frac{1}{2}$ $-V_b$ $1-V_a$	$\frac{1}{2}+V_c$ $V_a-\frac{1}{2}$ $\frac{1}{2}+V_b$	$1-V_a$ $-V_c$ $-V_b-\frac{1}{2}$
3	T_a T_b T_c	V_a $\frac{1}{2}+V_b$ V_c	$1+V_b$ V_c $V_a-\frac{1}{2}$	$\frac{1}{2}-V_c$ $-V_b-\frac{1}{2}$ $\frac{1}{2}-V_a$	$V_c-\frac{1}{2}$ V_a $1+V_b$
4	T_a T_b T_c	$-V_a$ $\frac{1}{2}-V_c$ $-V_b$	$-V_b-\frac{1}{2}$ $-V_a$ $1-V_c$	$V_b-\frac{1}{2}$ $V_c-\frac{1}{2}$ $\frac{1}{2}+V_a$	$\frac{1}{2}-V_c$ $-V_b-\frac{1}{2}$ $\frac{1}{2}-V_a$
5	T_a T_b T_c	V_c $\frac{1}{2}V_a$ V_b	$1+V_a$ V_b $V_c-\frac{1}{2}$	$\frac{1}{2}-V_b$ $-V_a-\frac{1}{2}$ $\frac{1}{2}-V_c$	$V_b-\frac{1}{2}$ V_c $1+V_a$
6	T_a T_b T_c	$-V_c$ $\frac{1}{2}-V_b$ $-V_a$	$-\frac{1}{2}-V_a$ $-V_c$ $1-V_b$	$\frac{1}{2}+V_a$ $\frac{1}{2}+V_c$ $V_b-\frac{1}{2}$	$1-V_b$ $-V_a$ $-V_c-\frac{1}{2}$

Table 13: Duration time described with the phase voltages Va, Vb and Vc

3.3.6 Conclusions

In chapter 3.3 the SVPWM for a three-level neutral-point-clamped voltage source inverter has been presented. The three voltage levels ($0V_{DC}$, $1V_{DC}$ and $2V_{DC}$) can with help from the inverter switches create the three levels in the inverter output. Calculating the duty cycle for each switch, gives a sinusoidal resembling waveform in the output. Higher level means lower distortion, but at the same time the problem with the neutral point unbalance is attending. Realising the three-level converter in LabVIEW requires adaptation to the FPGA, in form of memory storage and sample time selection.

4. CONCLUSIONS

This thesis has presented the theories behind multilevel converters, using the neutral point diode clamped converter as a basis. Advantages with the diode-clamped inverter is the high efficiency. The modulation chosen for the project, the space vector pulse width modulation, has good utilization of the DC link voltage, low current ripple and is relative easy to implement in the hardware. These features makes it suitable for high-voltage high-power applications, such as renewable power generation. This specific design makes it possible to increase the number of levels just by increasing the amount of capacitors. It also works with all kinds of multilevel inverters. Increasing the voltage levels decreases the harmonic distortion, because it resembles the desired sinusoidal output more, but is also increases the voltage unbalancing problems. Also, the system becomes more complex, both in theory (more calculations) and reality (more equipment). For this reason many prefer to work with the three-level converter. For high-voltage high-power applications the inverter also is used as a control for the voltage and reactive power regulation. This is done when the inverter is connected to a RL-load, a current controller. It is however not suitable for active power control. Testing the theories of the three-level converter in Simulink can be useful when making small changes in the code, because it does not take as much time as in LabVIEW, but there are no guaranties that it will work with other sample times than the idealistic ones in Simulink. Implementing the ideas behind the SVPWM in LabVIEW, requires adaptation to the FPGA. The memory is not endless and each of the memories, logic blocks etc used in LabVIEW are carefully chosen so it will not take up all the space in the FPGA. It is also important to consider that it is not only the space vector modulation algorithm that will take space in the FPGA, also the Kalman filter

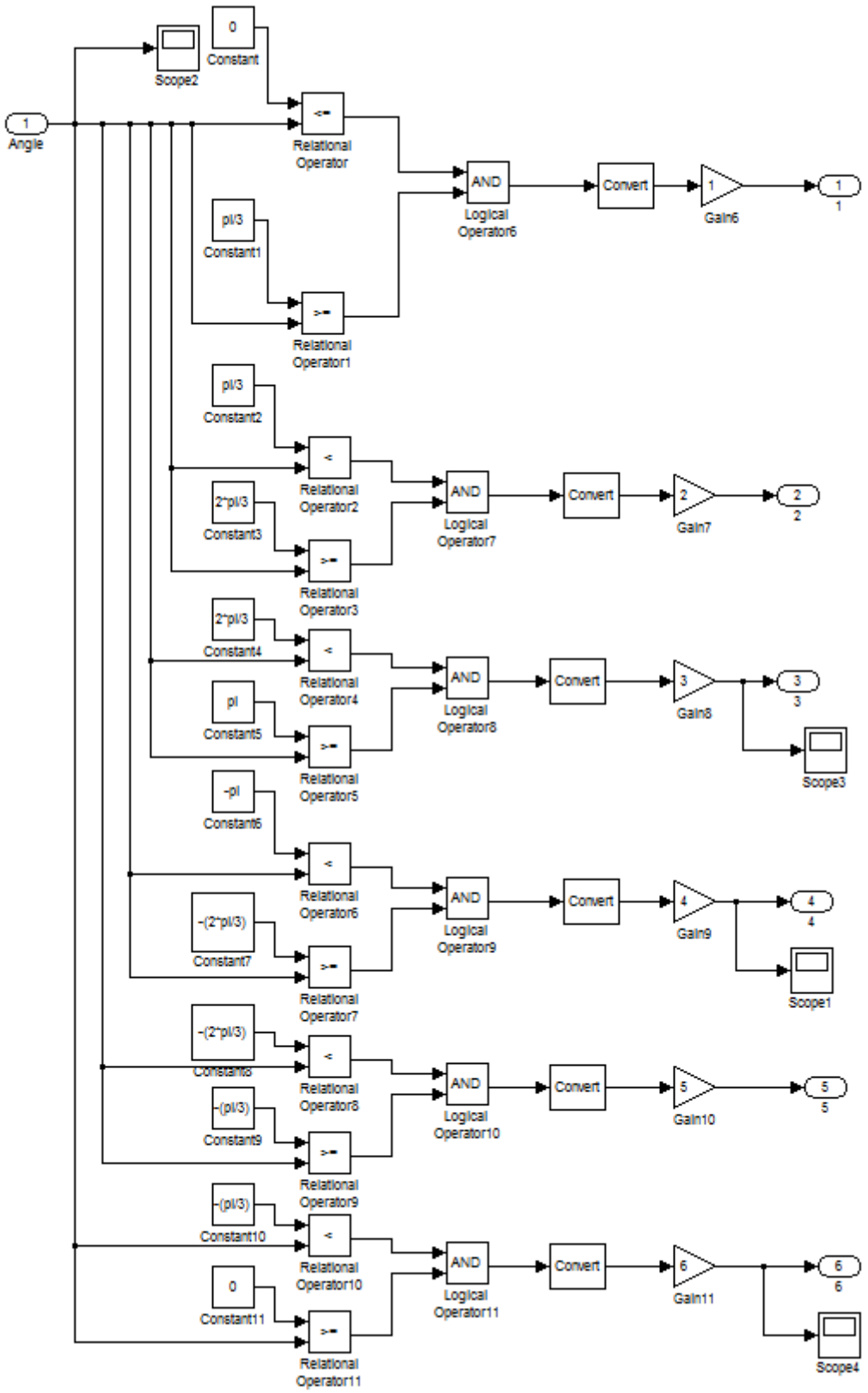
and the current controller algorithm has to fit in there. In conclusion, some errors in the voltage waveform output has been noticed: Deviations causing uneven pattern. This does however not intrude with the final stage of grid-connection, because of the filtering done in the end.

5. FUTURE WORK

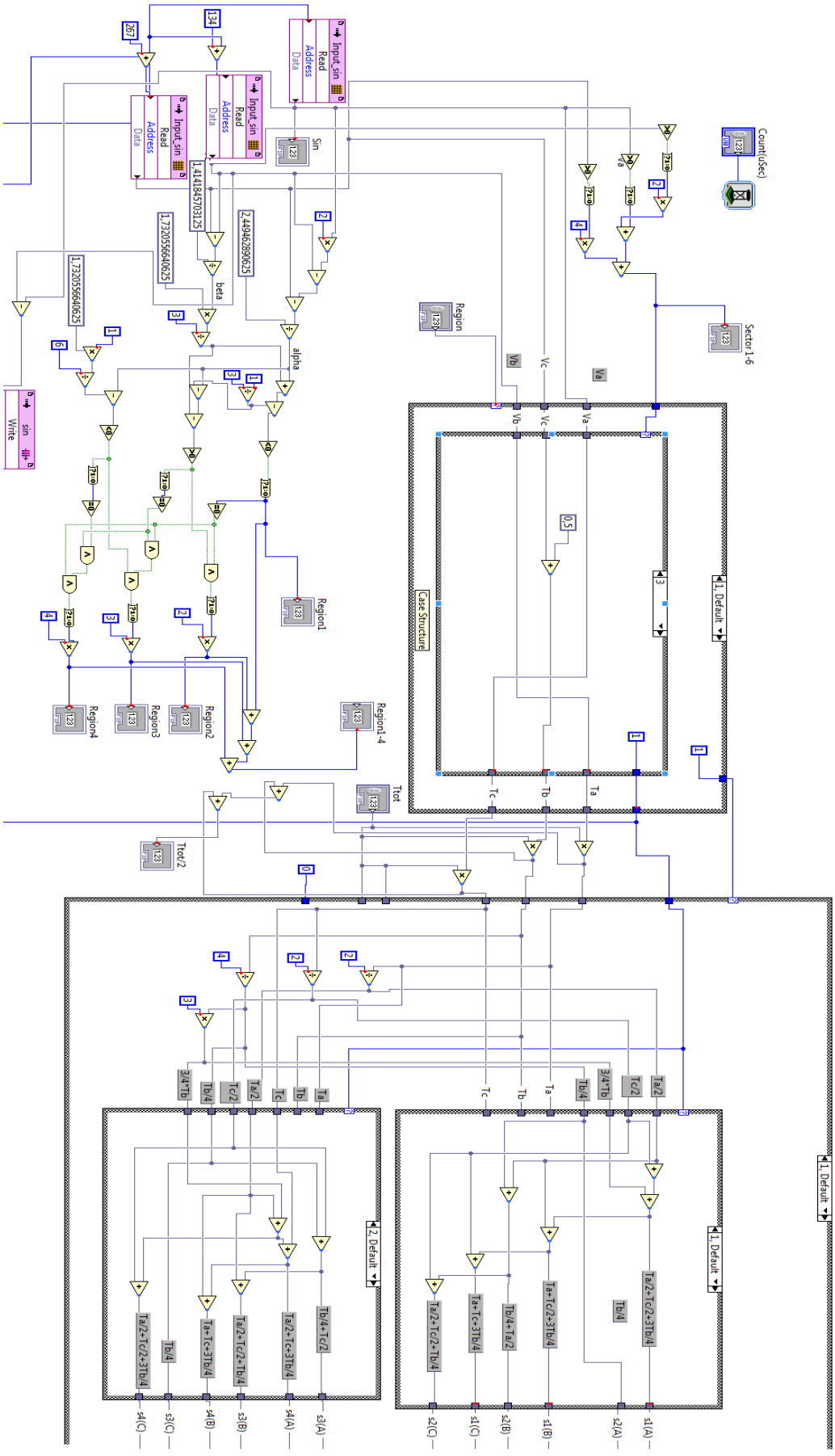
Where this project ends a new begins. There are several ideas that can be analysed and implemented. These are some of the suggestions for future work:

- Connect the FPGA to the three-level inverter and test the modulation algorithm created in LabVIEW.
- Try the space vector modulation strategy with a unbalanced system: $V_{a0}+V_{b0}+V_{c0}\neq 0$
- Improve the three-level SVPWM: Reduce losses with a filtering system within LabVIEW

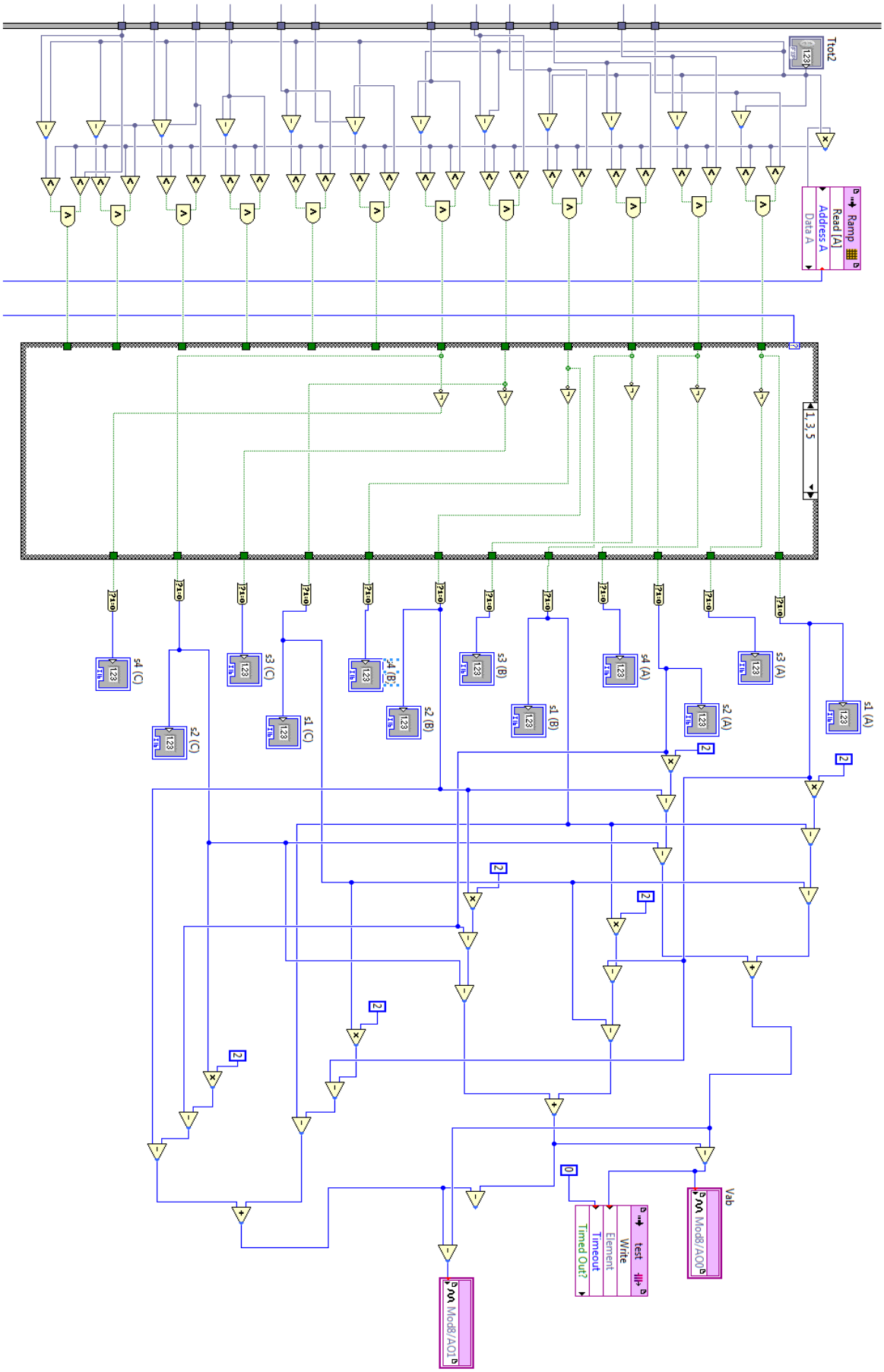
6. APPENDICES



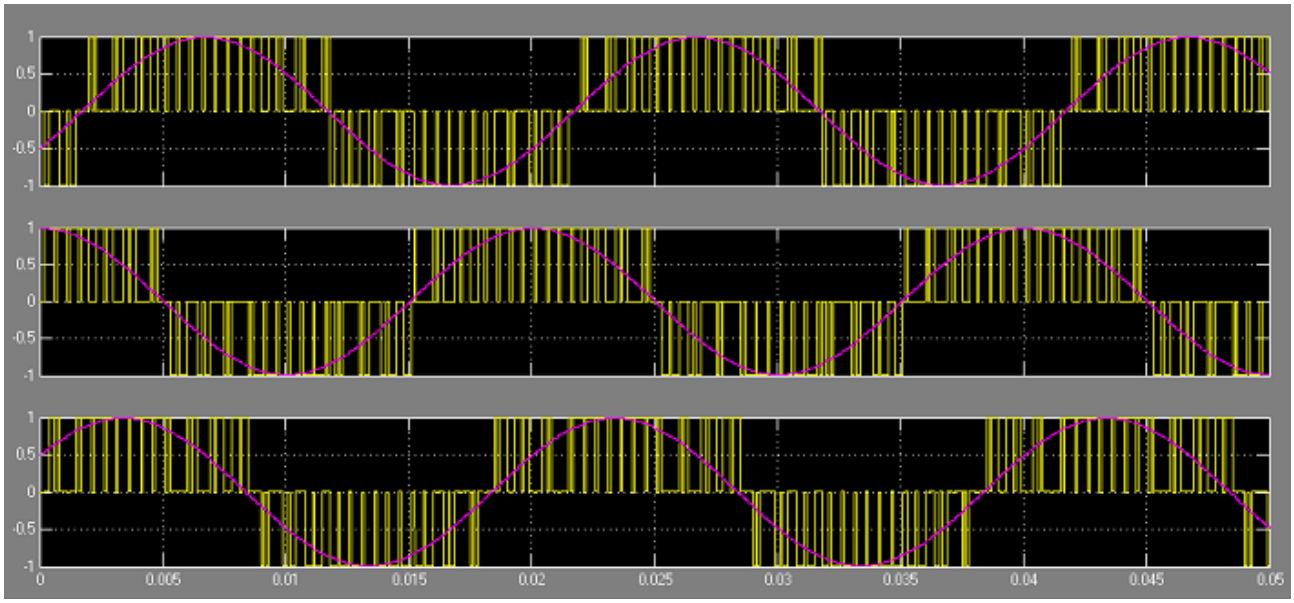
Appendix 1: Space vector modulation in Simulink: Block showing calculation for sector selection



Appendix 2: Space vector modulation in LabVIEW, part 1: Sector selection, region selection, duty time calculation and sequencing of switching states



Appendix 3: Space vector modulation in LabVIEW, part 2: Comparison with ramp and line-to-line phase voltage calculation



Appendix 4: Two-level output line-to-line voltage for each phase

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