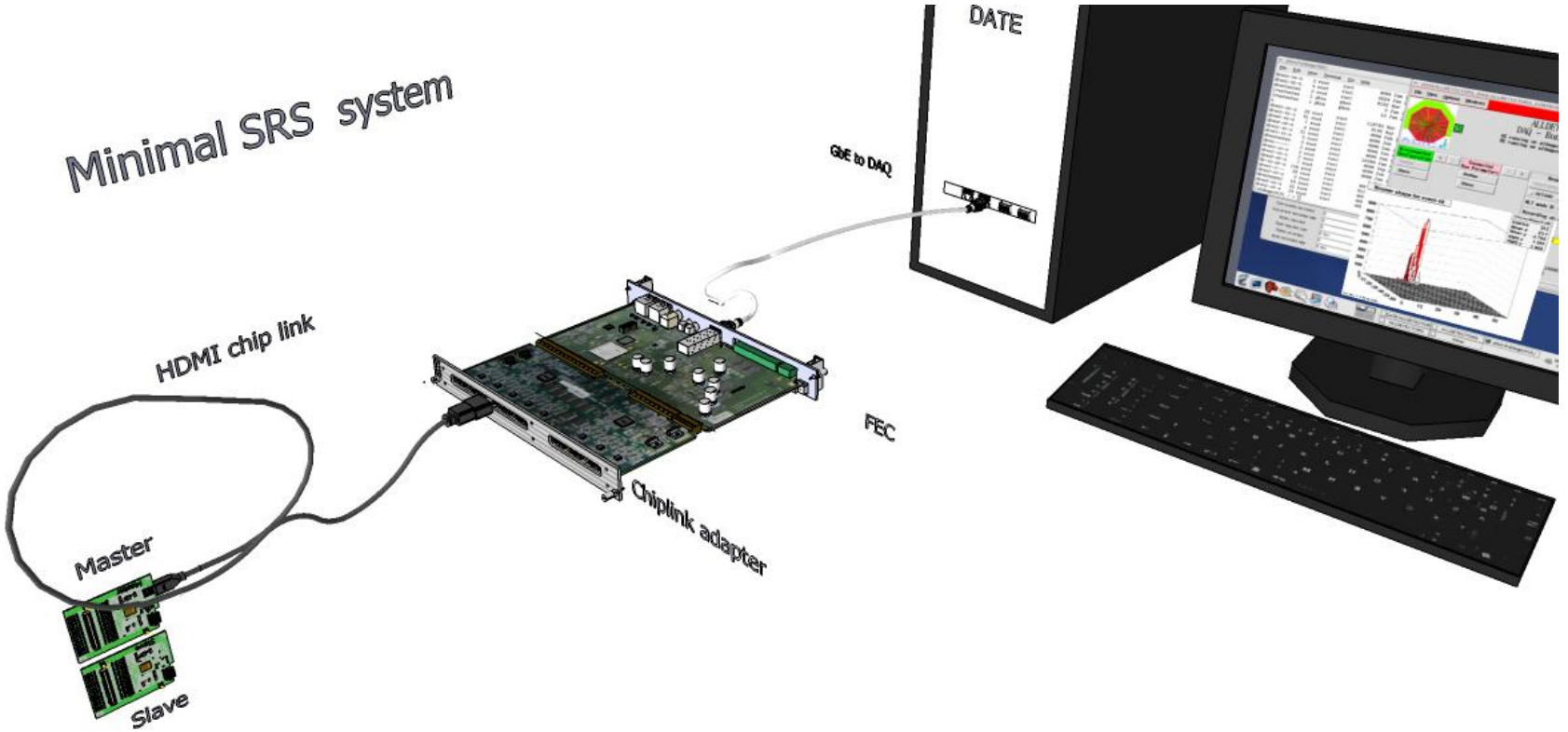
SRS Readout architectures

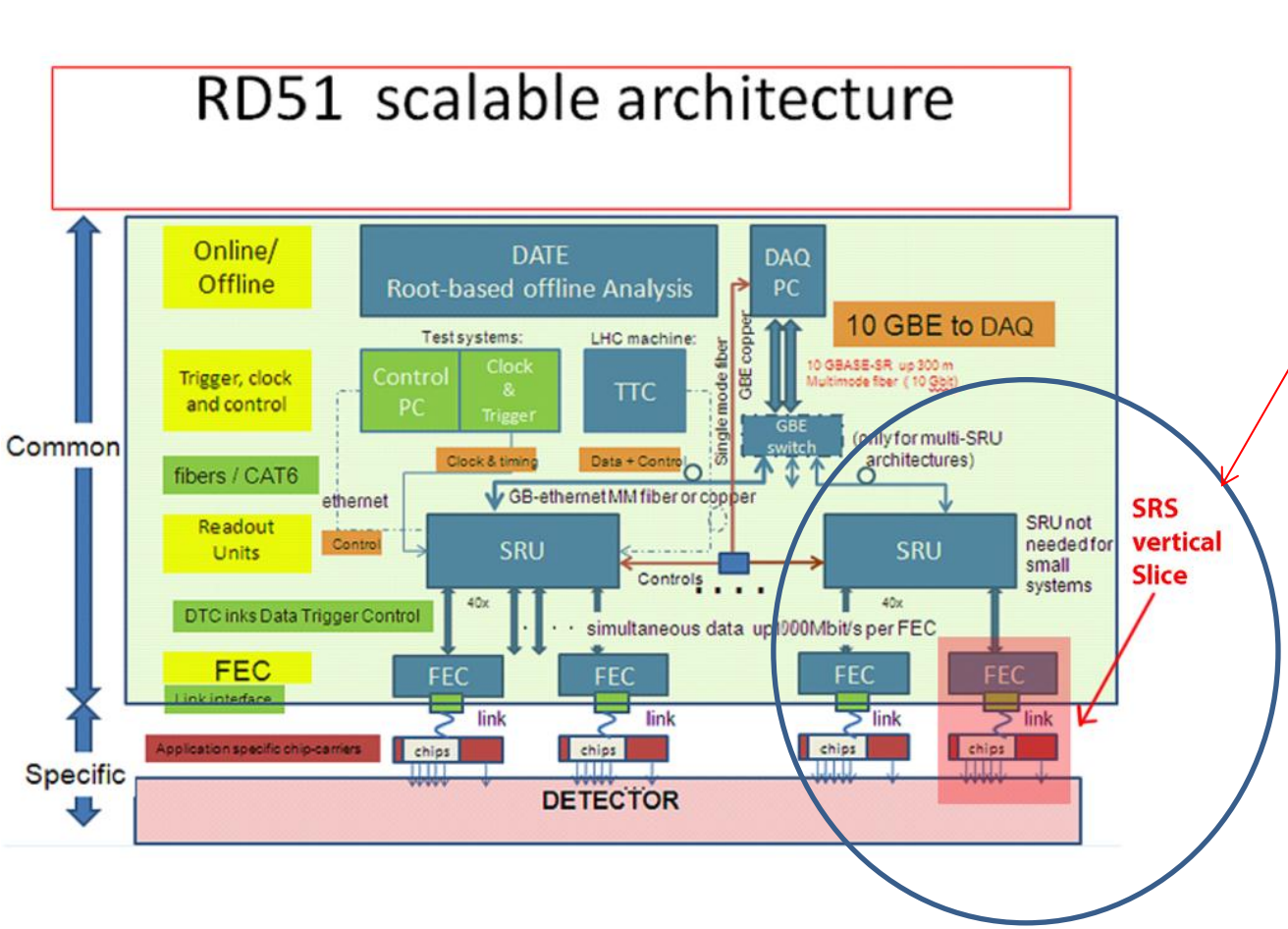
Hans Muller, CERN PH

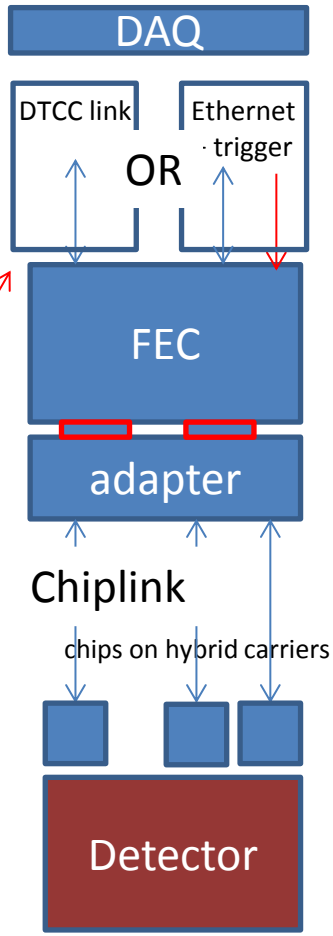
The SRS idea (2009)

- **choose the frontend (ASIC, hybrid) that fits your detector**
- **have a common readout backend with standard DAQ Software**
- **start from a minimal systems - > scale to large system**



SRS = vertical slice LHC architecture

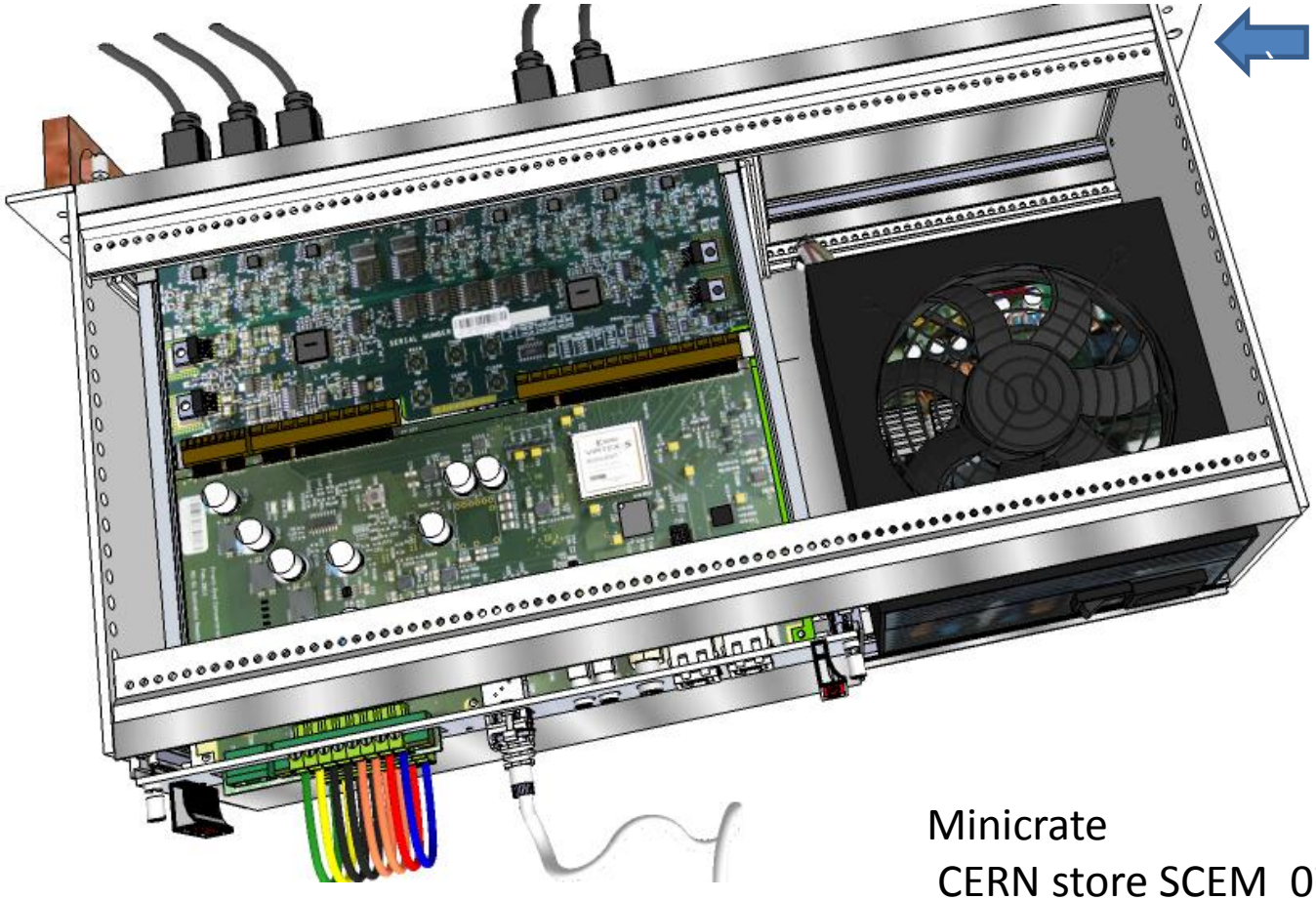




1 single vertical slice is a independent, small SRS system
the addition of vertical slices is a scalable architecture
SRU needed for larger systems for Data , Trigger, Slow Controls, Clock

SRS Minicrate

a portable solution for up to 4k channels



1 x FEC -ADC card Combo

CERN store items
SCEM 07.89.00.100.1 (FEC)
SCEM 07.89.00.105.6 (ADC)

Minicrate
CERN store SCEM 07.89.00.020.0

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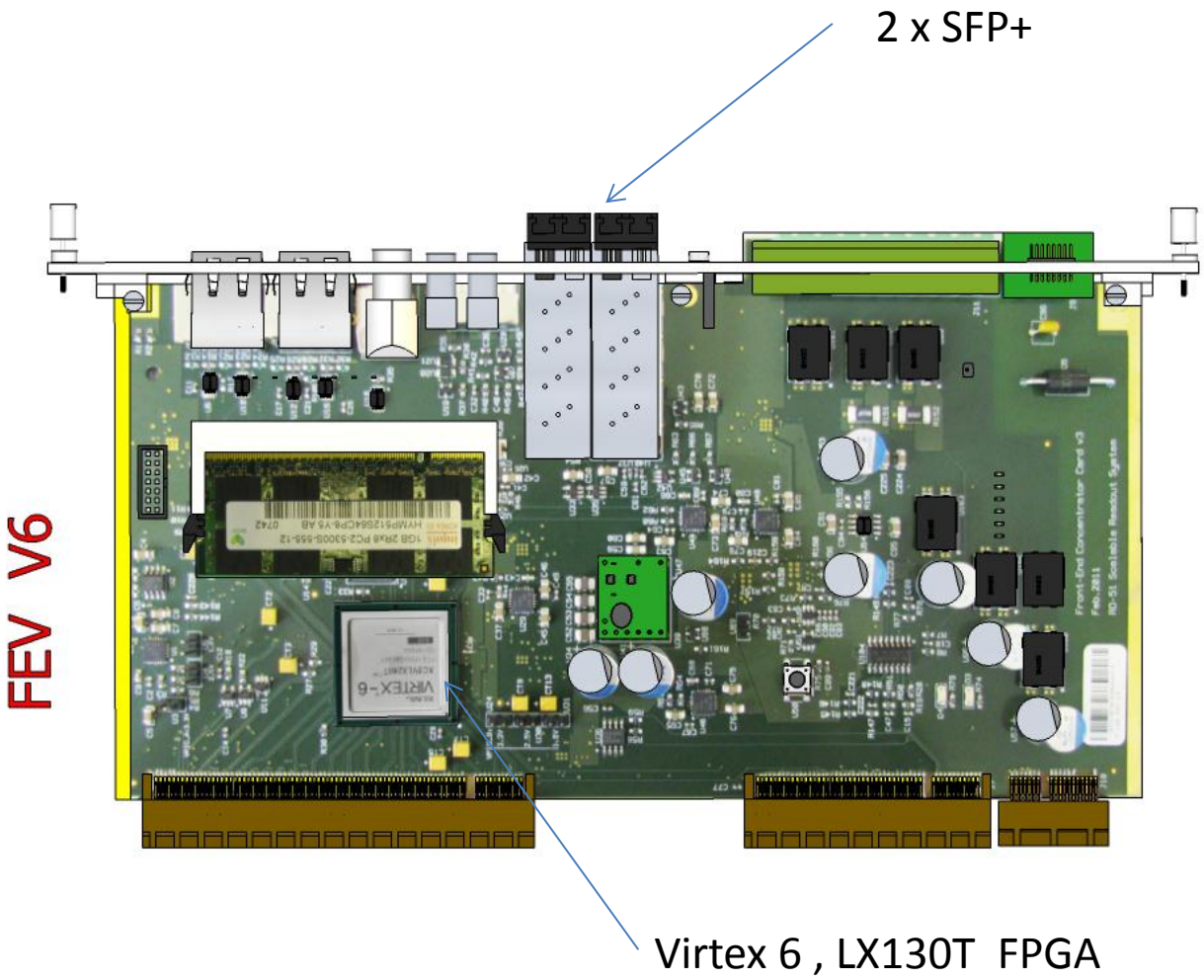
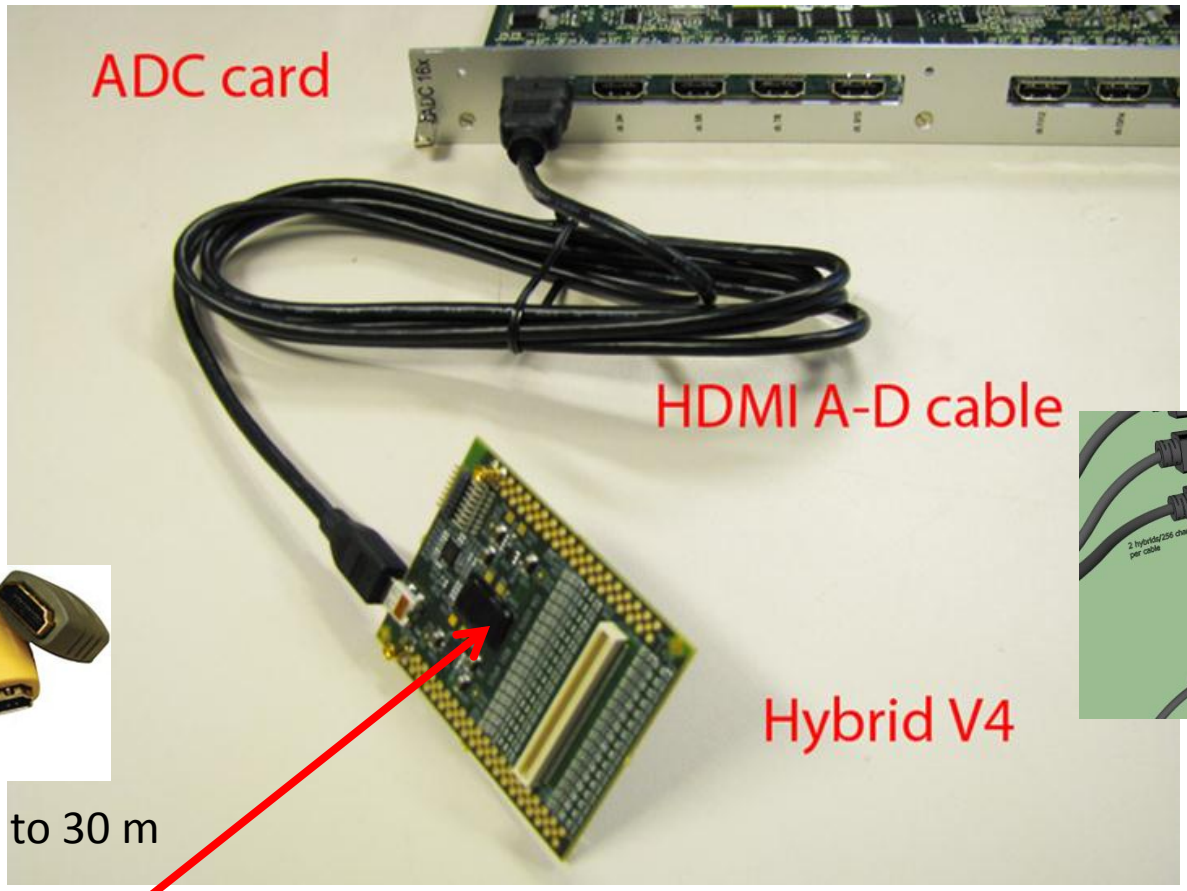
FEC V6 hardware



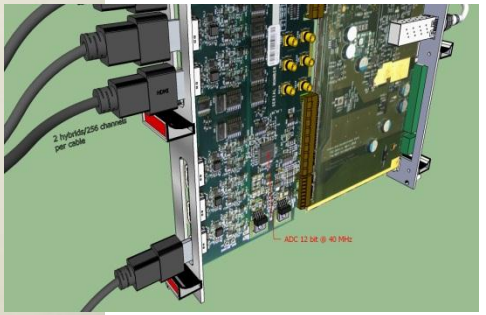
SRS: 1st chip –link: HDMI

cheap, v. high quality , 3Gbit/s, power for hybrid, works very well



Extension up to 30 m

ADC FEC

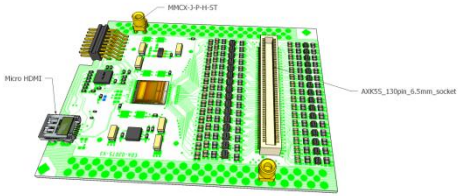


16 hybrids/FEC
2048 channels

128 channel readout chip (APV, Beetle, VFAT, VMM1)

APV hybrid SRS

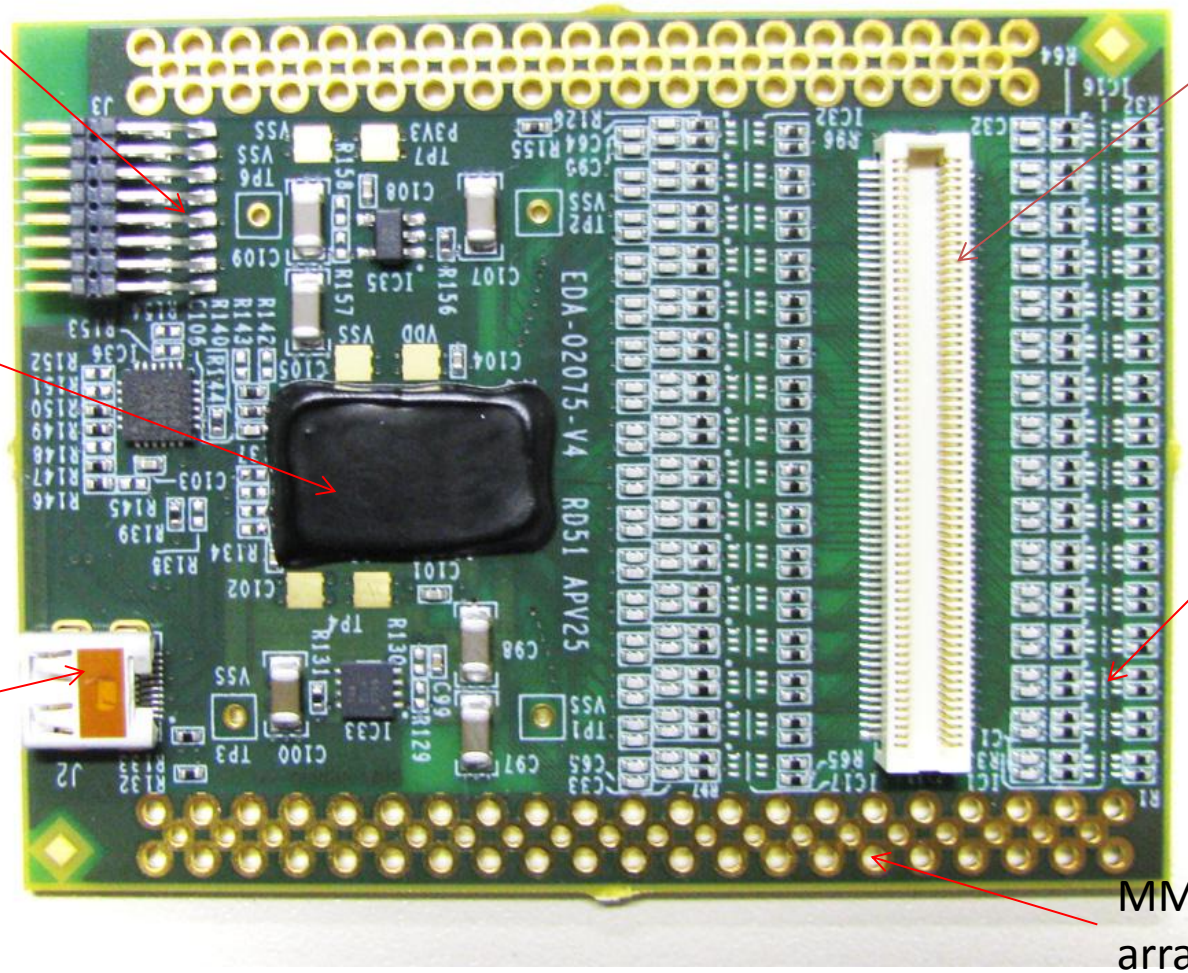
(CERN store SCEM 07.89.00.005.9)



Master-Slave Cable connector

Wire –bonded APV 25 chip Analogue 128 channels below globtop

Micro HDMI readout plug for SRS



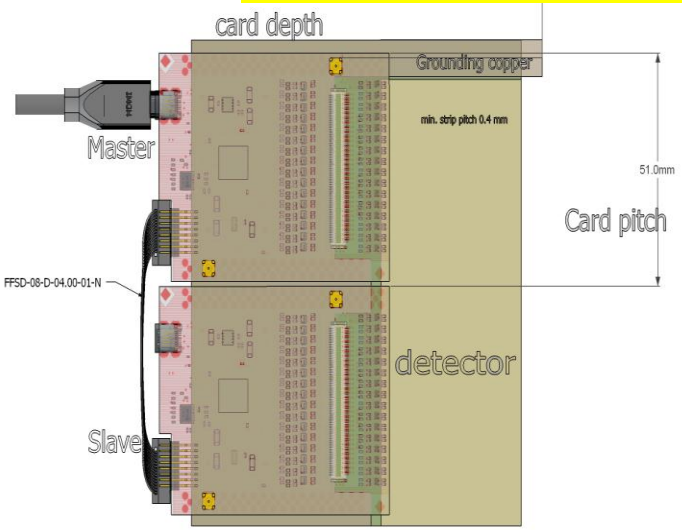
Standard connector RD51 Detectors (128 channels)

IEC-61000 Level-4 spark protection

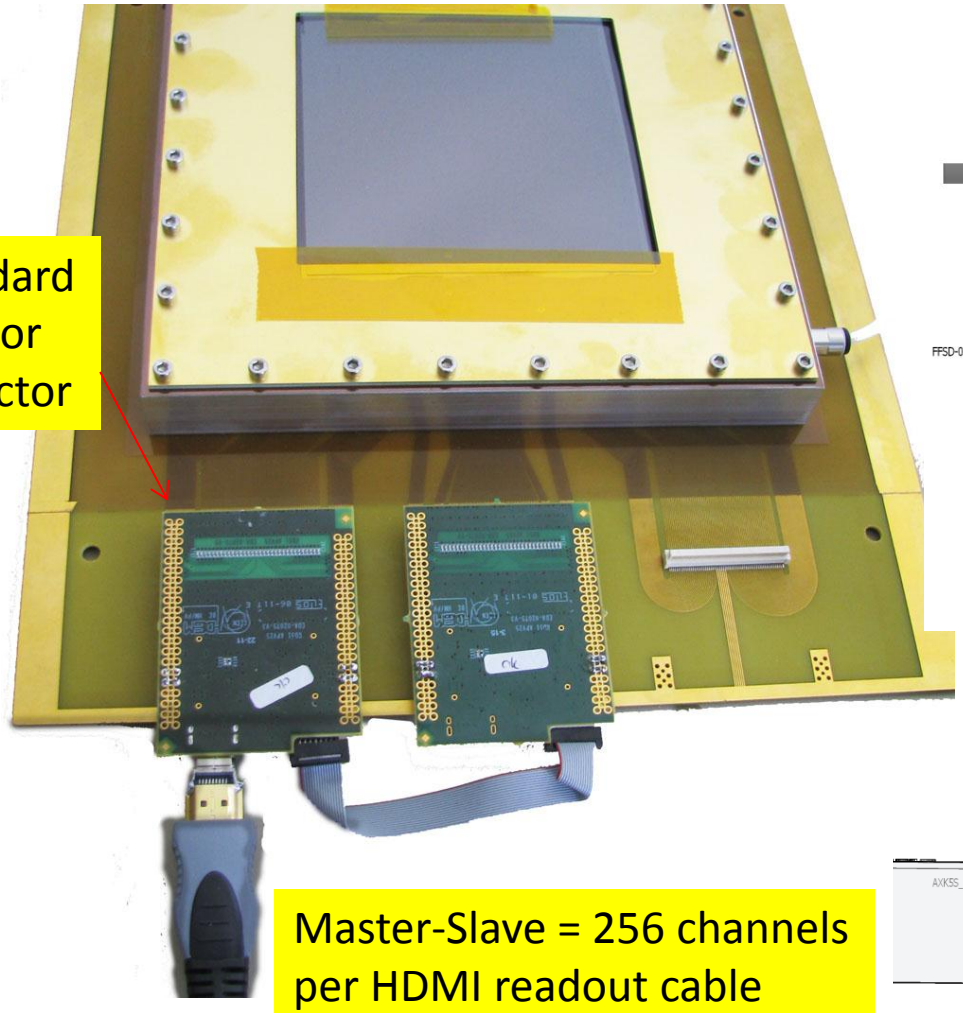
MMCX connector array (GND,PWR)

SRS hybrids on a Detector

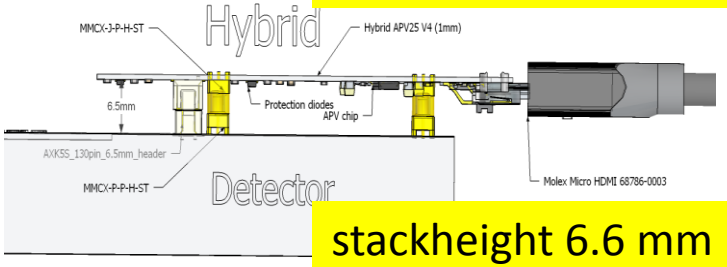
128 channels for 0.4 mm continuous pitch



Fit standard connector on detector



uses 9 mm above detector detector plane



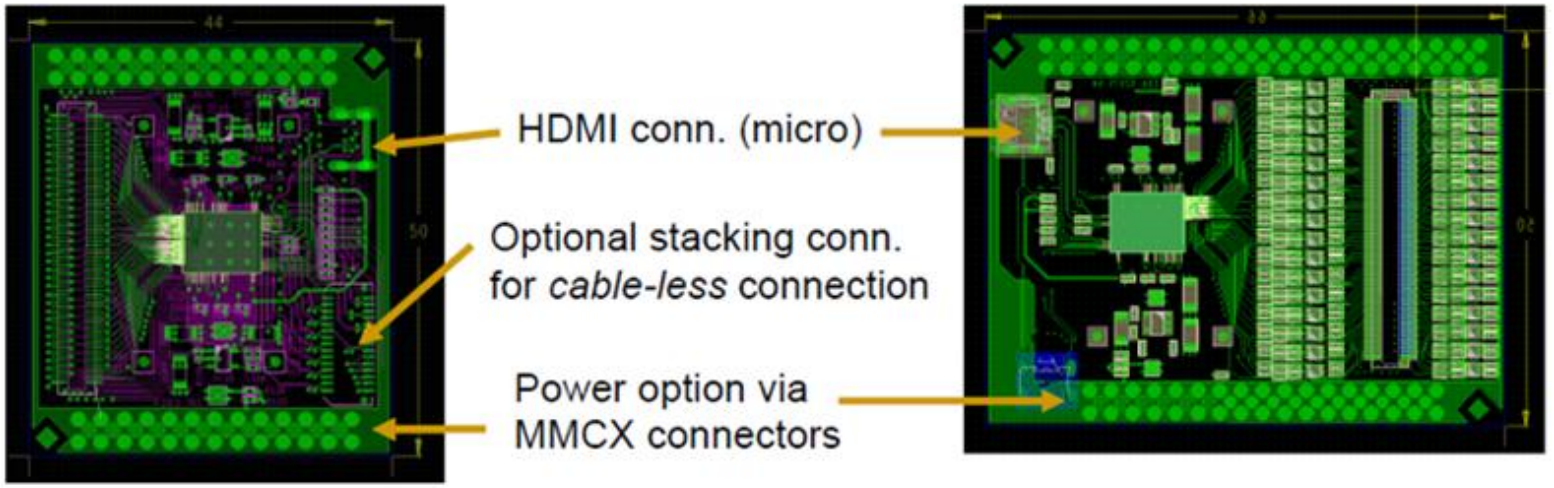
stackheight 6.6 mm

Master-Slave = 256 channels per HDMI readout cable
Power via HDMI

New VFAT2 hybrid design*

Short version – no input protection

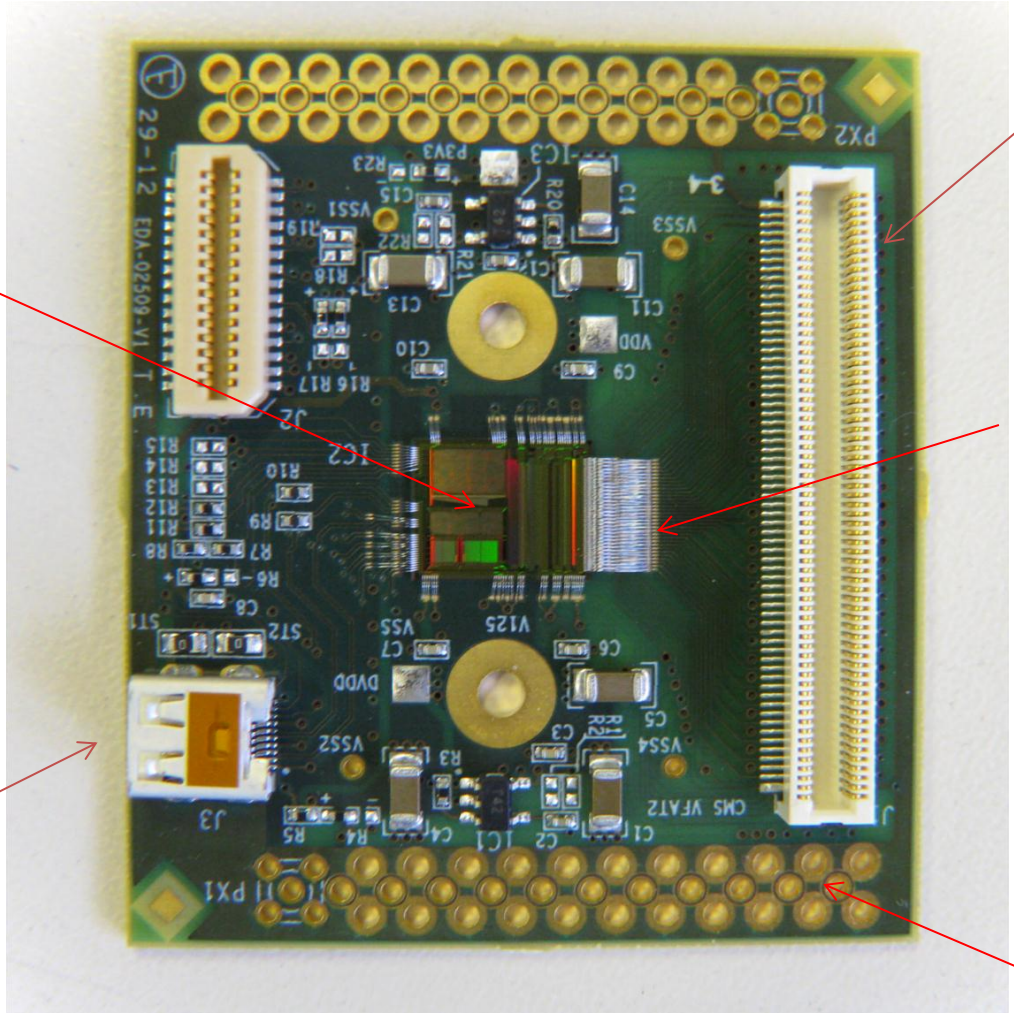
Long version – full RD51 compatibility



* Sorin Martoiu /RD51 for CMS GEM collaboration

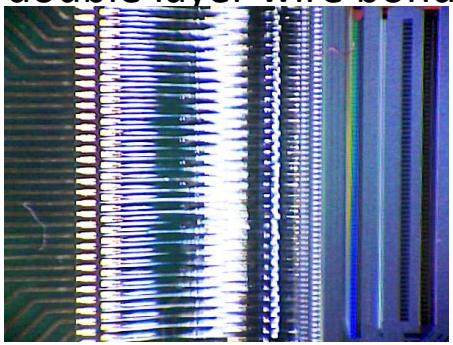
photo of 1st VFAT SRS hybrid

wire –bonded
VFAT chip



Standard
connector
RD51 Detectors
(128 channels)

double layer wire bonds



Micro HDMI
readout plug
for SRS

MMCX connector
array for
Ground and power

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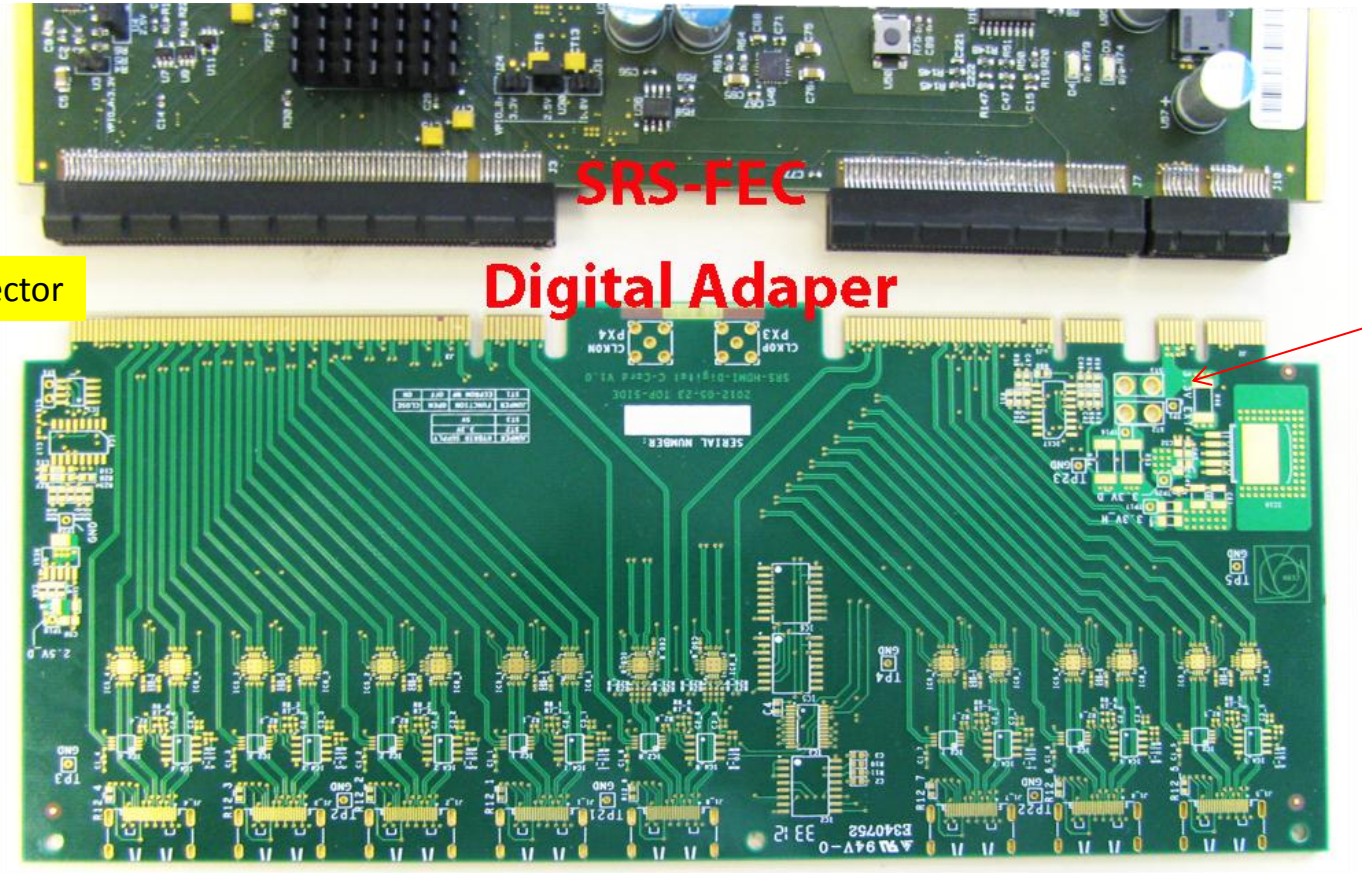
New: SRS adapter for digital chips

(VFAT readout CMS GEM collaboration*)



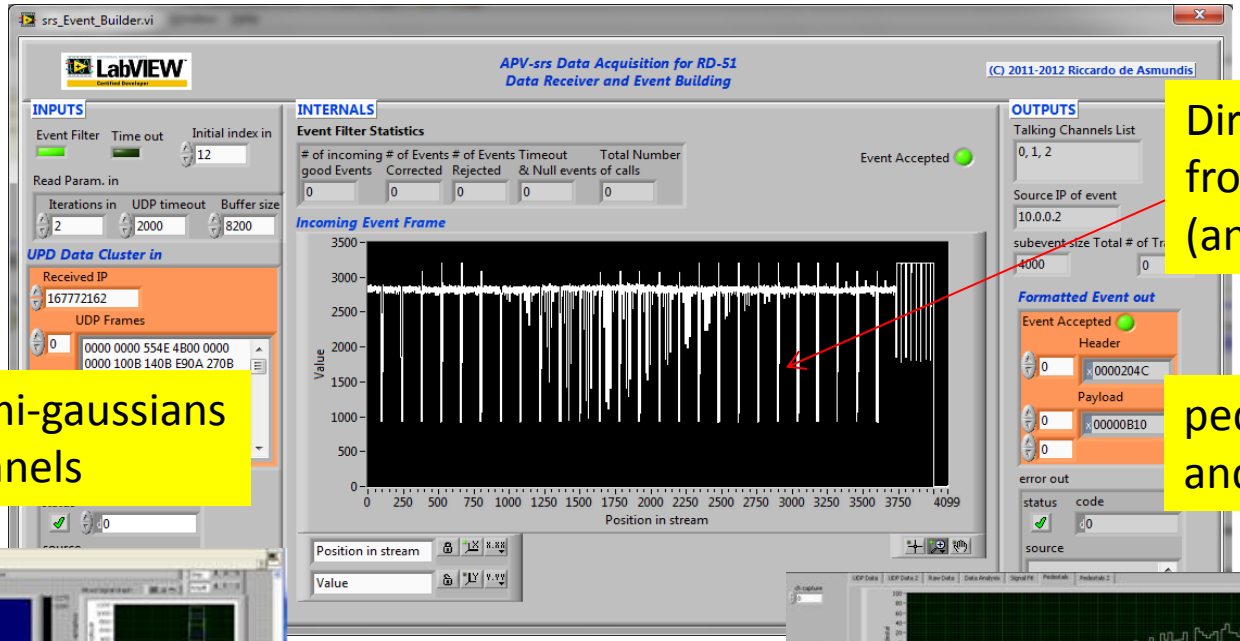
PCIe connector

Digital
C-card
Adapter
PCB
(just arrived)

*collaboration on VFAT readout via SRS being set up. participation welcome

APV-srs DAQ (Labview 2011*)

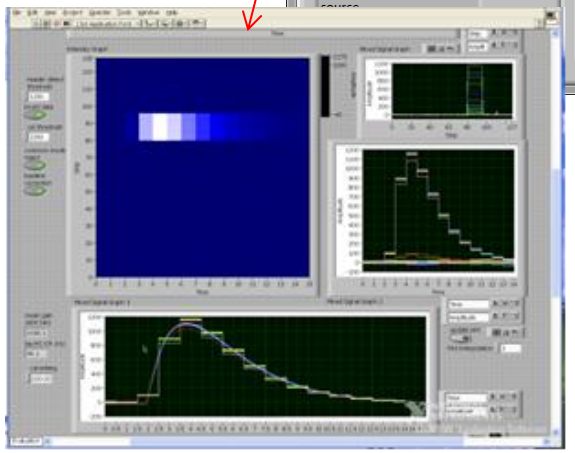
like a 128- channel oscilloscope

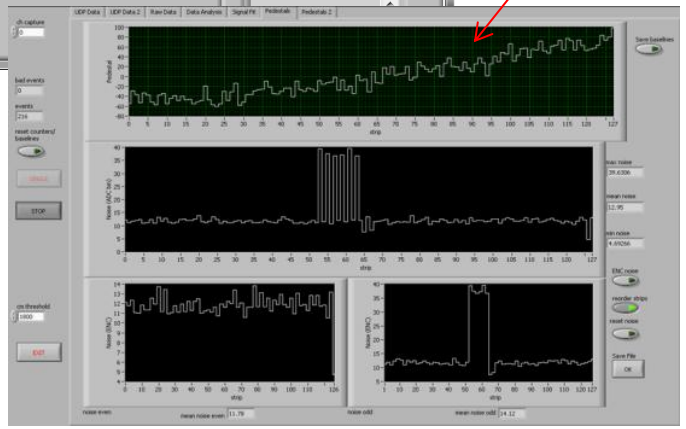


Direct signals from APV (analogue, serial)

single ch. semi-gaussians and 128 channels

pedestals and RMS noise





Direct signal viewing
Data quality monitoring
Channel mapping
etc..

** Riccardo de Asmundis INFN Naples with monitoring modules by Sorin Martoiu INFN Bucharest*

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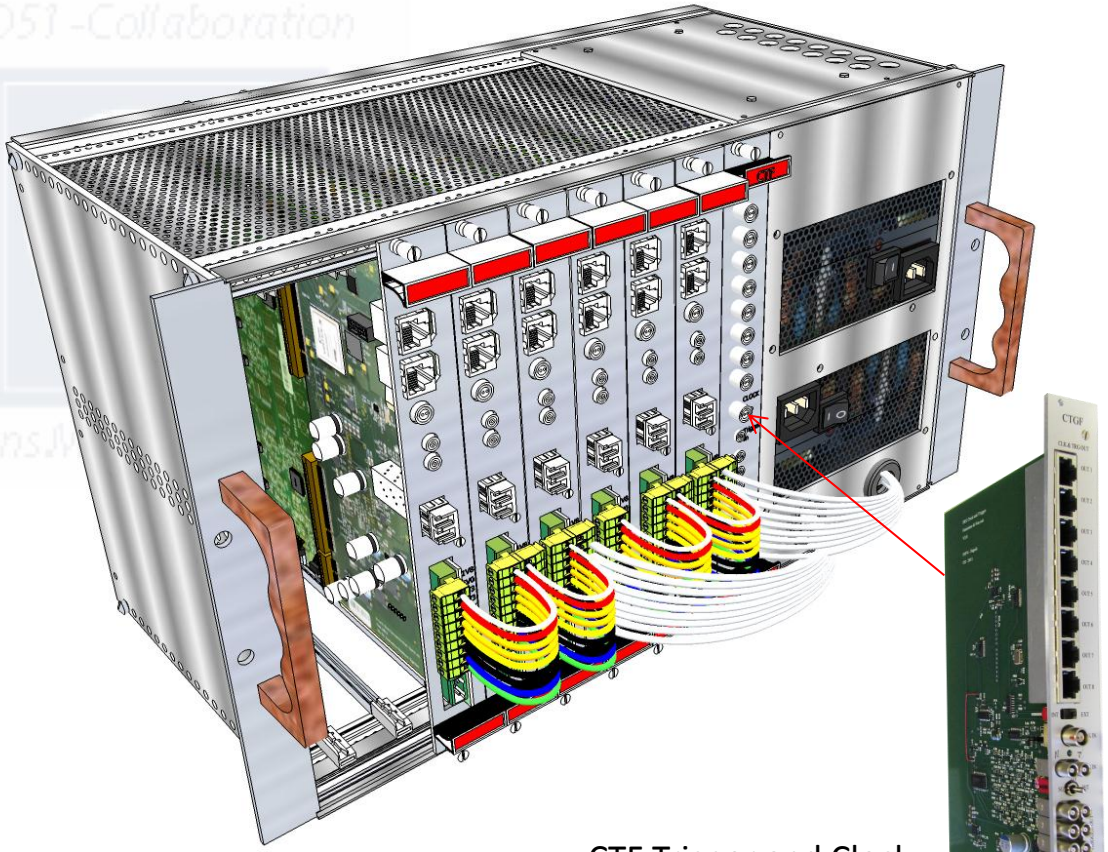
Eurocrate

a scalable solution for up 16 k channels/crate

HP version: up 4 FECs, 1 ATX, incl. power for 64 hybrids
FP version: up 8 FECs, 2 ATX, incl. power for 128 hybrids

CERN Store SCEM 07.89.00.030.8



CTF Trigger and Clock
Fanout in SRS slot 9

8 x ADC card
from backside

8 x FEC card
from frontside

Channel cost small SRS systems

Example RD51, CERN store order

	ATX	FEC	ADC	CrateHP	MiniCrate	APV-M	APV-S	HDMI cable	Flat cable	TBASE-1000	MMCX pair	ATX Pack	other	Fs	Eu
RD51, CERN		2	2	1		16	16	16	16	1	32	0	0	10602	8835

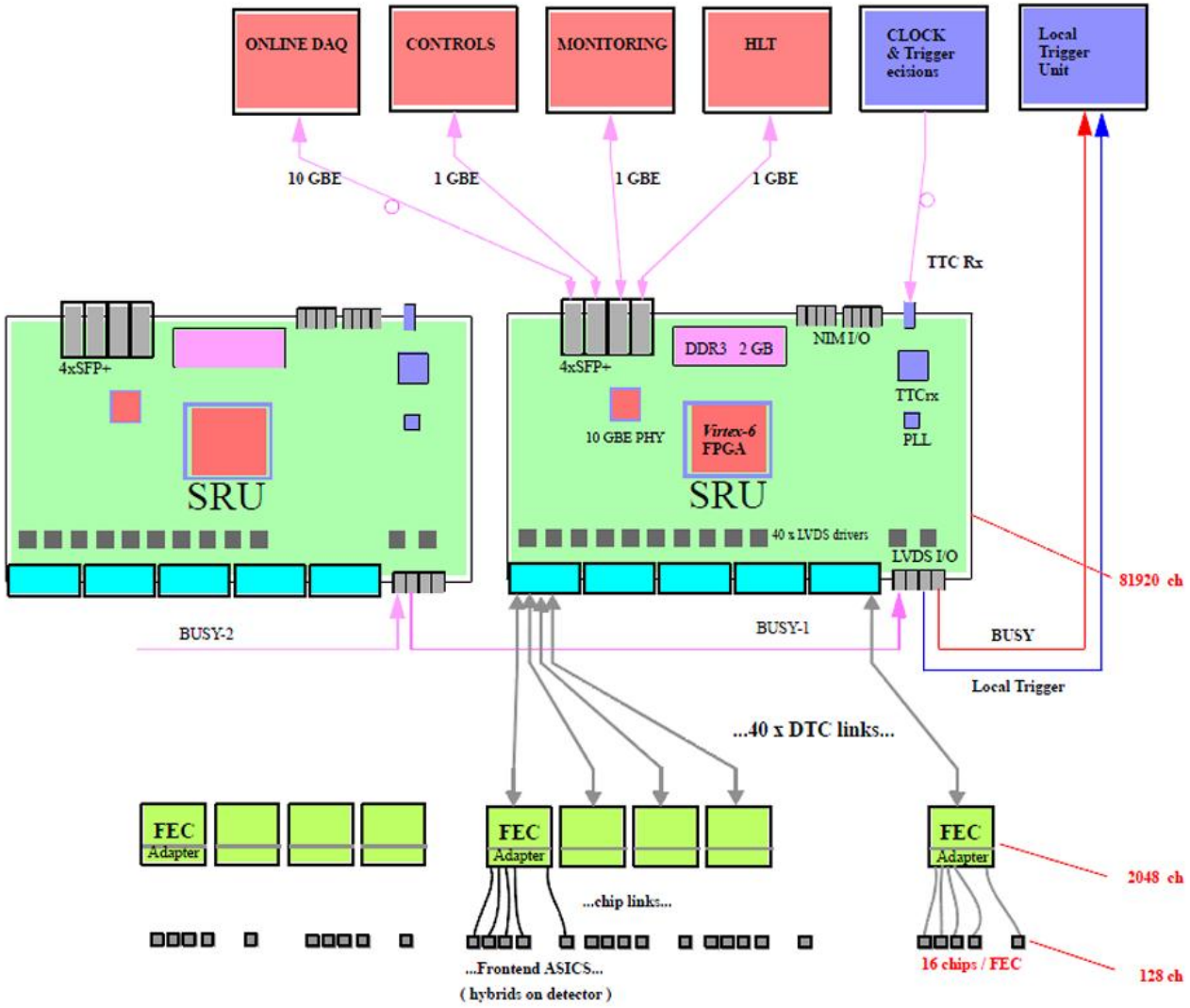
1 Eurocrate, 2 FEC, 2 ADC, 16 Master, 16 Slaves, 16 HDMI cables,
16 Flat cables, 2 TBASE-1000 plugins, 32 MMCX pairs = 10.602 Fs

32 hybrids = 4096 channels

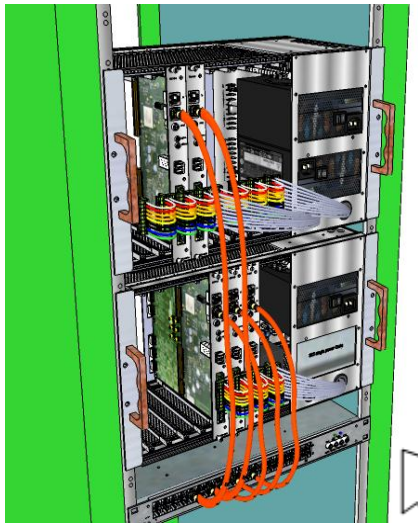
10.602/4096 = 2.6 Fs per channel

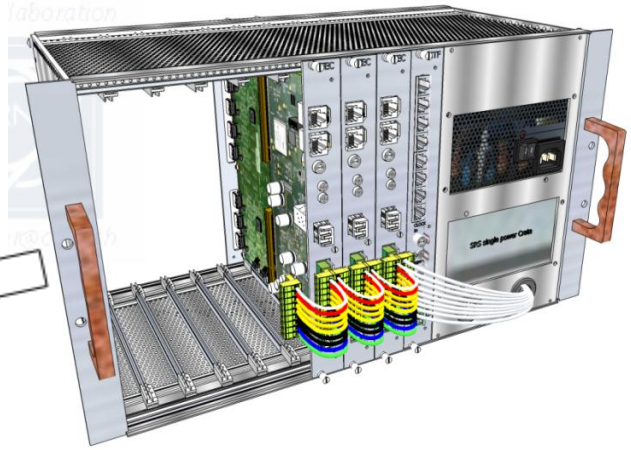
For larger, multi-crate systems channels cost is ~ 2 Eu
Including 1 SRU (~ 3kFs) per 40 FEC cards

Large SRS system architecture



SRS 19” rack environment





Rack for up to 82k channels
distributed over 5 SRS crates + 1 SRU

DTCC links

Max 92 k channels / Rack

Scalable Readout Unit (SRU)

25 SRU's produced for ALICE EMCal, being installed for upgrade
10 produced for RD51 users

designed for use in magnetic field:
Alu chassis, no transformers, no DC-DC

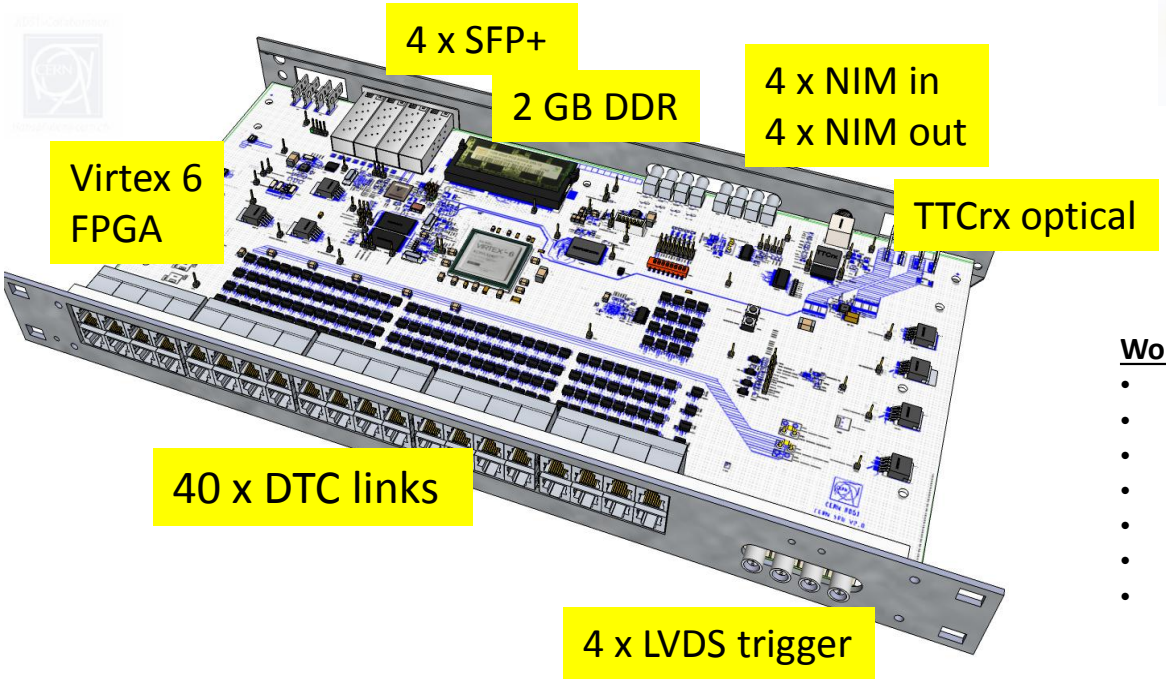


PHOTO SRU

Working so far:

- DTCC links
- TTCrx receiver
- Slink
- 1 Gbit ethernet
- 10 Gbit Ethernet
- Slow controls via IP
- Software triggers

Being worked on

- DDR3 event buffer
- Jitter cleaner
- Subevent building
- remote configuration
- SEU reconfiguration

Planned

- TTC via SFP
- Event Multicast
- Busy handling
- ….

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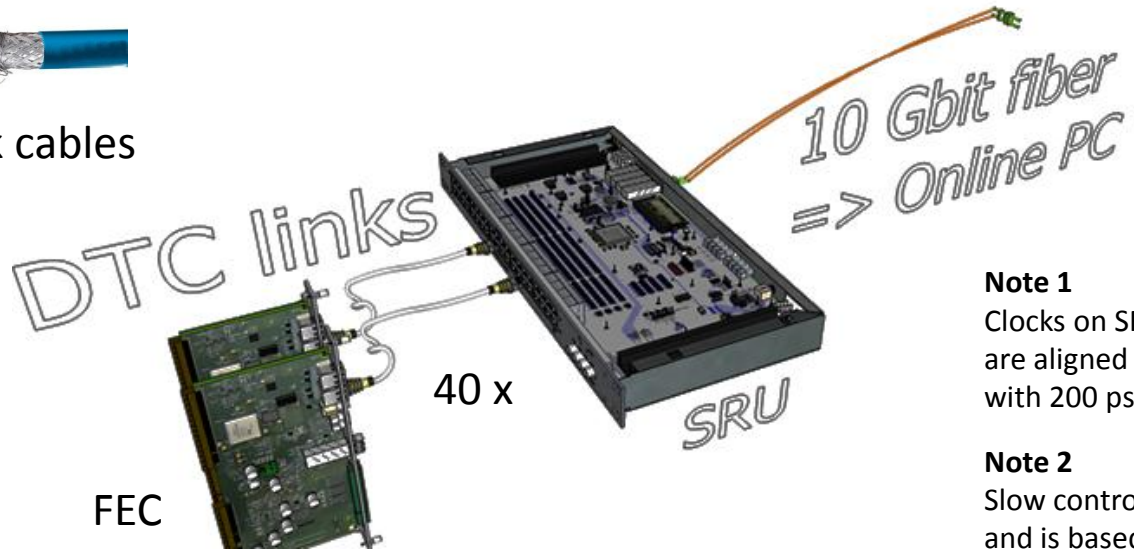
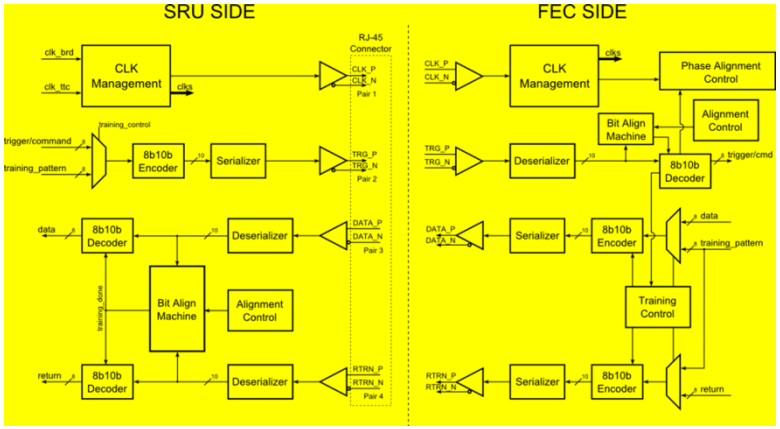
DTCC links*

network cables



Note 1
Clocks on SRU and FEC cards
are aligned to exactly same phase
with 200 ps jitter over 5 m cable

Note 2
Slow controls needs no hardware (!)
and is based on control commands
from host PC to IP ports in FEC or SRU



DTCC protocol (based on 8b/10b)

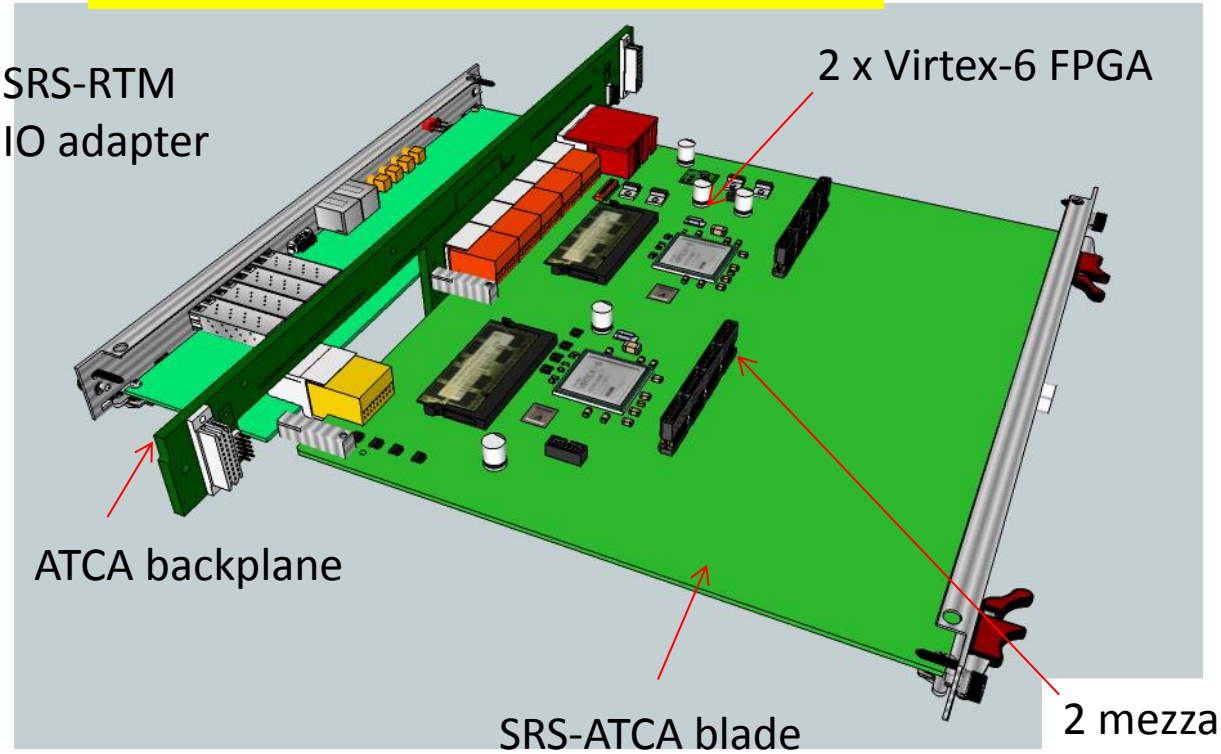
Clock ← clk (from TTC or other source)
Data → data a (1 Gbit upstream)
Trigger ← Trigger & Slow Control
Clock Sync → Slow Control & data b

*Alfonso Tarazona, ALICE

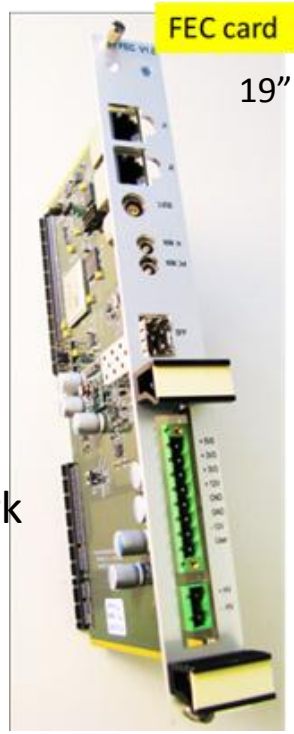
Future of large SRS : ATCA*

ATCA blade = FEC equivalent with dual FPGA

NEW for large, rack-based RO systems



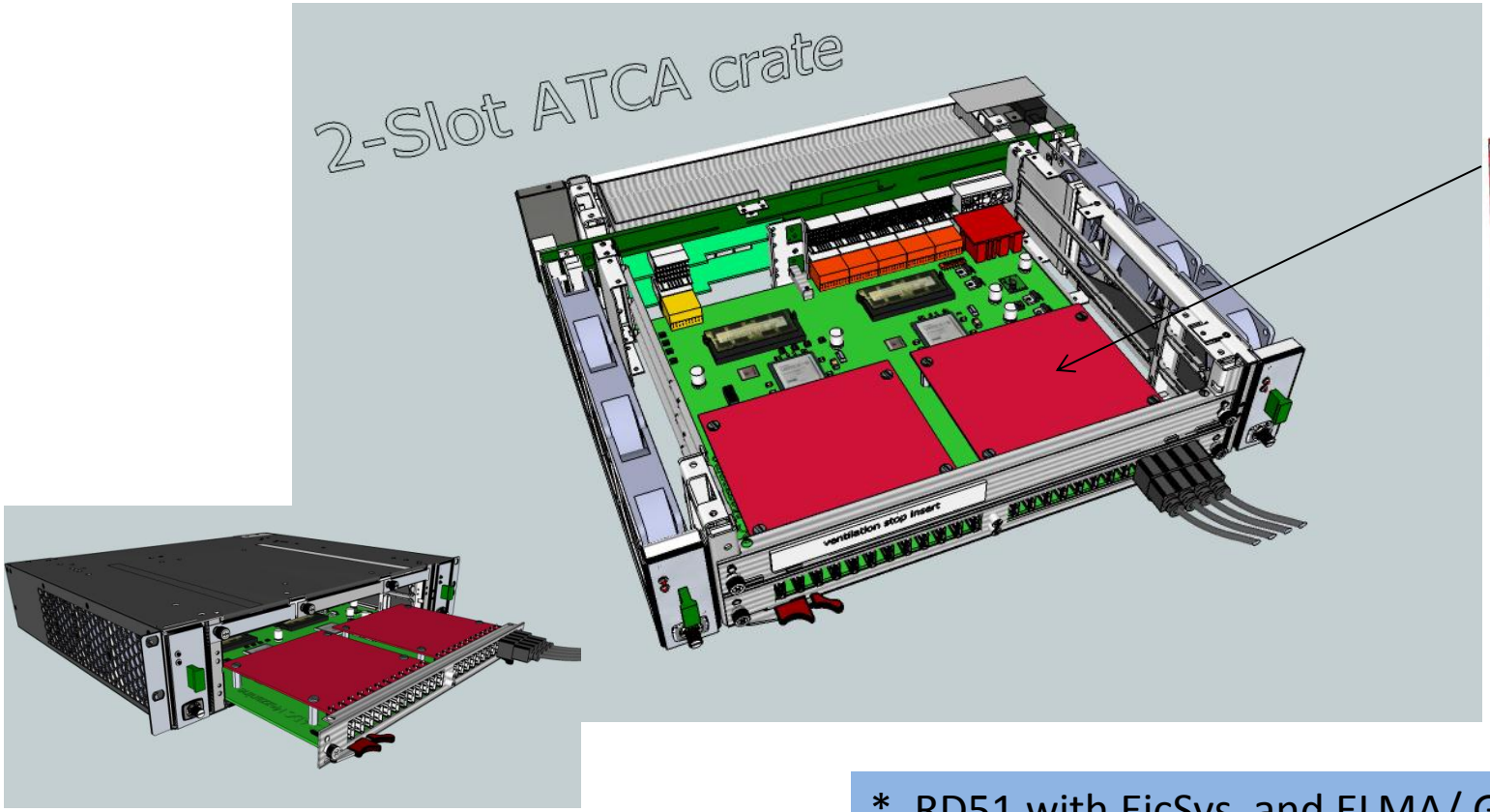
3x more channels per card In ATCA framework



*AdvancedTCA (Adcanced Telecommunication Computing Architecture)
an open industry standard developed by PICMG 3.0

SRS - ATCA*

1.) higher channel integration => reduce cost/channel for large systems
2.) certified crate standard 3.) replace DTCC cables by ATCA backplane
4.) start with 2-slot ATCA crate that can be read out via SRU



SRS adapter mezzanines
- analogue
or
- digital

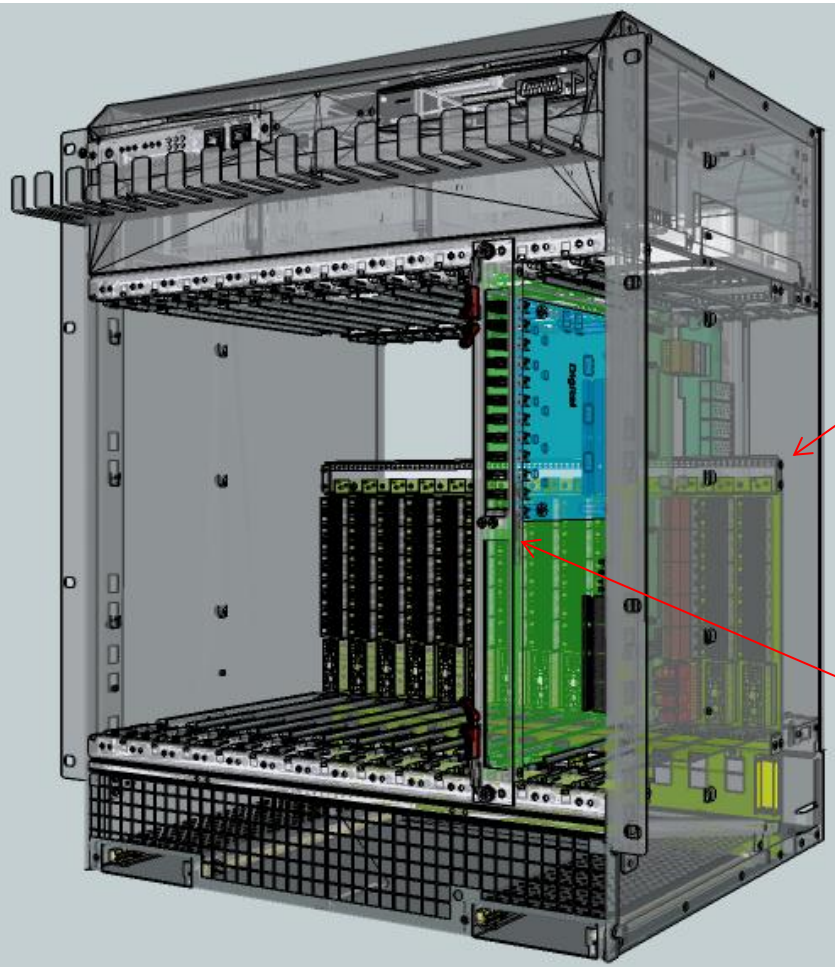
* RD51 with EicSys and ELMA/ Grmany

Large SRS systems: ATCA crate (13U)

3 crates per rack (max. 190 k channels)

SRU will become
slot-1 card
DTCC -> mesh fabric
channel cost ~ 2Eu

Photo of ELMA crate



ATCA full mesh backplane

SRS-ATCA card

SRS User Status 9/2012*

CERN experiments

- ATLAS CSC upgrade MMegas (8kch APV-SRS systems, 1st SRS testbeams, MMDAQ developer)
- ATLAS CSC upgrade MMegas, (VMM1 readout chip developer, SRS Adapter by Arizona Univ, MMDAQ)
- ALICE EMCaL + FOCAL, SRU-based backend (50 kHz upgrade via SRS, DATE, new: Focal readout via SRS-Beetle)
- ALICE TPC upgrade, SRS readout electronics with DATE backend ?
- NA62 ref. tracker with Micro-Megas (1kCH-SRS Minicrate, MMDAQ)
- CMS high Eta GEM collaboration (VFAT hybrid and VFAT SRS adapter, in prep.)
- Totem upgrade R&D , SRS VFAT readout, DATE ?

HEP experiments

- NEXT Coll., dual Beta decay, SiPM, PM (Collaboration on SRS HW & FW, FEC cards, DATE)
- BNL GEM detector readout (2kCH. APV Minicrate, PHENIX SRDAQ porting to SRS)
- Jeff. Lab Virginia Univ. GEM prototyping, (Minicrate , Offline Data evaluation via AMORE + DATE)

Applications with Cosmic Tomography

- FIT Florida, Muon Tompography for homeland security, GEMs (1st 16K SRS application, DATE)
- Geoscienes CRNS- Waterquality in Rocks, MMegas (5kCh SRS Crate , DATE + Labview)

R&D with MPGD's (small systems)

- Bonn/Mainz Univ, Timepix readout (SRS- Timepix adapter card)
- Helsinki HIP, GEM-MMega (SRS evaluation, Trigger pickup box via CSP)
- MEXICO UNAM, THGEM 2x (SRS Minicrate, DATE)
- C.E. Saclay, Micromegas MMegas (2k Ch SRS Minicrate , MMDAQ)
- WIS Israel, THGEM 3x (Minicrate, Beetle hybrid, SRS- Labview Beta tester
- INFN Naples (Minicrate, Labview for SRS developer, CTF card , Zero-supression code)

New SRS system deliveries (orders via CERN store)

- RD51 lab, Radcore, LMU Munich, WIS, USTC, SAHA, INFN Bari, INFN Naples, Stony Brook, Yale Univ, J-Parc-RIKEN,
- East Carol. Univ., Jeff-Lab, Tsinghua Univ, Univ Texas,

* in red: SRS developers in green: to be confirmed in blue: USER

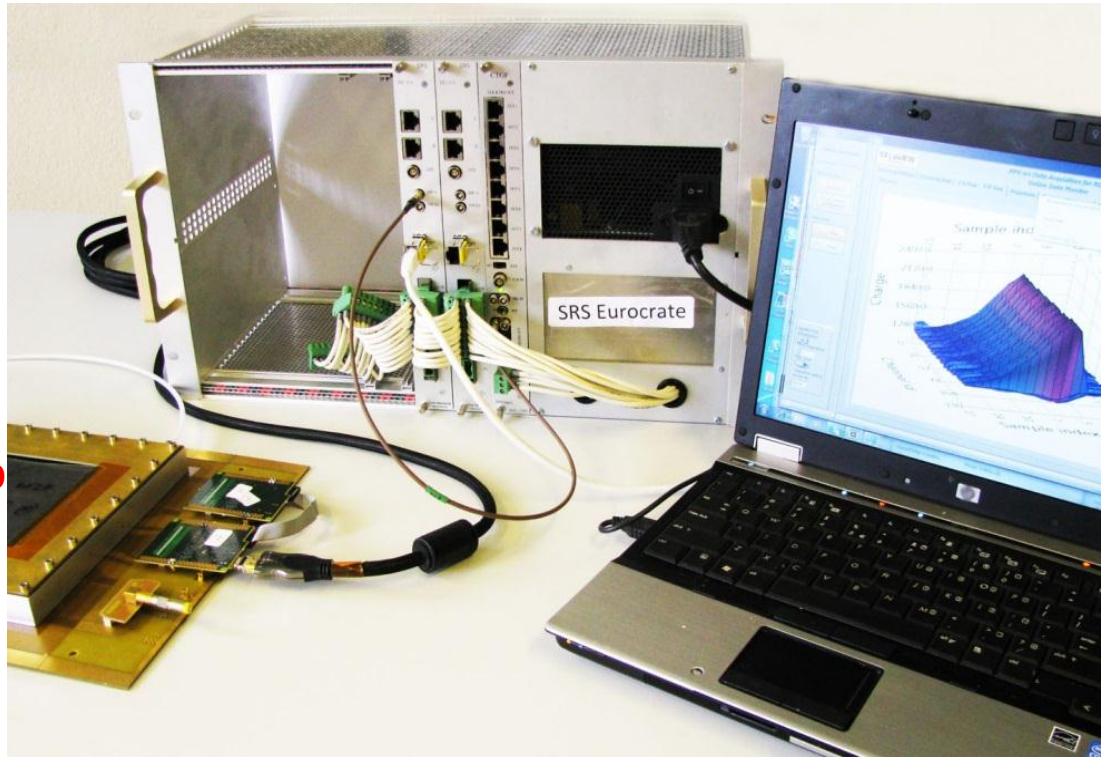
Summary

- SRS , a complete DAQ from frontend chip to Online
- minimal SRS = vertical slice of a LHC architecture
- APV frontend well established, next is VFAT, Beetle
- VFAT frontend launched, CMS invites participation
- Channel cost around 2 Eu above 4k channel
- Various SRS compatible Online systems
- SRU needed for larger systems
- DTCC links for STAR interconnection 40x FEC-> SRU
- Online connected via Slink, Ethernet and 10 GBE
- TTC and Slow controls included w.out extra hardware
- SRS moves towards commercial ATCA for large systems

photo of a table-top SRS system

(= 1 vertical slice)

SRS Electronics up 16 k channels in a 19" Eurocrate (no bus)



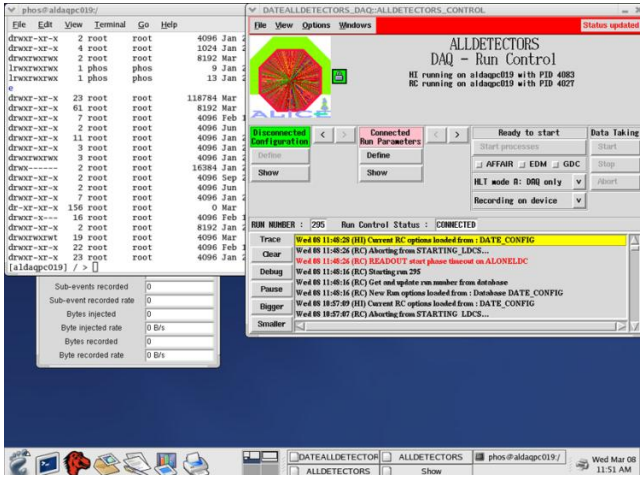
readout chip on hybrids attached to detector

SRS-compatible DAQ software and slow controls SW

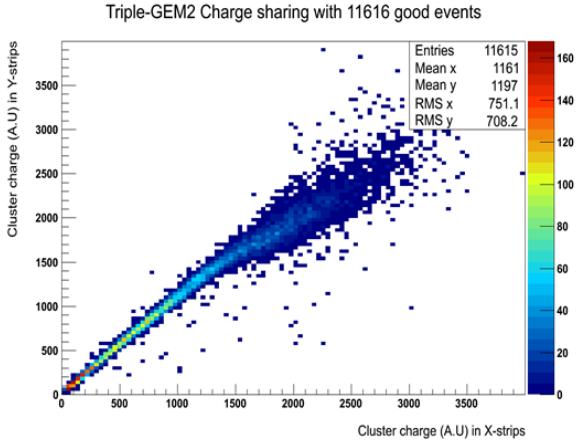
-Labview gen.purpose
-DATE (ALICE)
-MMDAQ (ATLAS)
-RCDAQ (RHIC)

Online DAQ systems

DATE , MMDAQ , RCDAQ (Linux based)

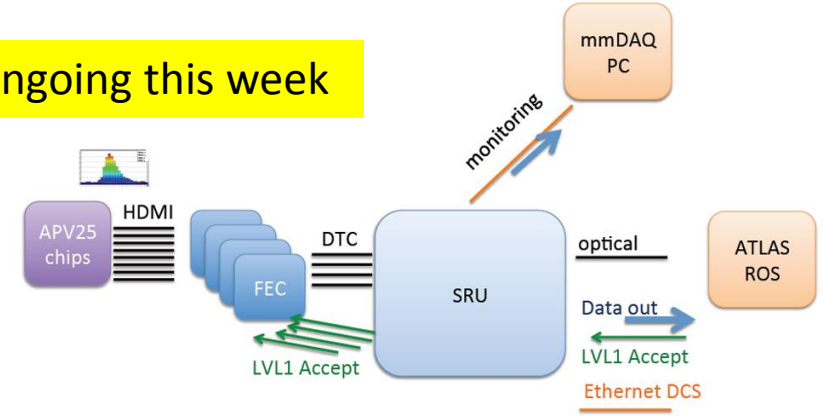


Root Analysis: Event statistics, distributions, cuts and fits

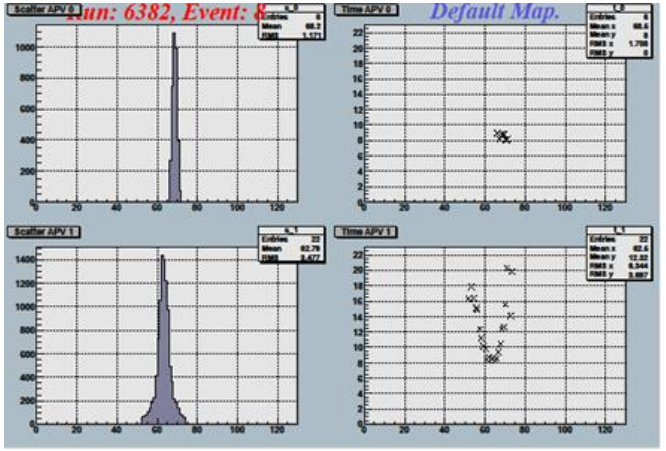


Integration into ATLAS DAQ

Ongoing this week



Testbeam data



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