

STATCOM as a Solution to Improve the Voltage Profile of a Power Grid

(Master Thesis Extended Abstract)

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Abstract— The aim of this dissertation is to propose and evaluate a power electronics based system, using reactive shunt compensation to guarantee a better voltage profile at the MV/HV grid, thus allowing a better use of the line capacities.

An H-bridge Static Synchronous Compensator (STATCOM) is developed using a star configured Cascaded Multilevel Converter (CMC). The system is designed for a 10 kV application, with seven modules and a Phase-Shifted Pulse Width Modulation (PS-PWM) strategy, in which a phase shift of the carrier waveforms is used in order to obtain the desired AC output voltage from the converters. PI controllers are used for the grid side currents and voltages and a voltage balancing technique for the DC capacitors is also designed to guarantee that the voltages in the DC link do not diverge significantly.

The developed system is tested, using an equivalent model of a MV line. Several simulation scenarios are tested and the obtained results show that the proposed system allows for the regulation of reactive power injected/consumed in the network, guaranteeing the regulation of the voltage at the point of common coupling (PCC).

Index Terms— Flexible Alternating Current Transmission Systems (FACTS), Static Synchronous Compensator (STATCOM), Cascaded Multilevel Converter (CMC), Phase Shifted Pulse Width Modulation (PS-PMW).

I. INTRODUCTION

Since the introduction of electrical energy in the 19th century, there have been significant technological developments and the modern day electric power systems have been built. These systems have grown in complexity and nowadays are constituted by a vast network of transmission interconnections, multiple types of generation resources and loads. Due to these technological advancements and many other scientific achievements, in the last century the quality of life for most people has increased significantly. However, the rapid growth of the population, the development of industry, the increase of generation sources at the load and the networks underlying unpredictability, are starting to strain the power generation systems. This means that the added load demands, growth of interconnections, economic restrictions, and factors such as global warming, that is a leading concern in the

scientific field, and is slowly starting to pressure governments to turn to renewable energy systems as a means of replacing old and cheap energy productions methods that produce a significant amount of greenhouse gas, are starting to create balancing issues in the delivery systems.

Imbalances in the voltage profile along the electric network are one of the biggest challenges for system operators. Therefore if the voltage and reactive power are not controlled, then the difference in voltage between the generation source and the load can lead to voltage instabilities or even voltage collapse.

A solution using Flexible AC Transmission Systems (FACTS) can overcome some of these issues. This solution is extremely important in overcoming limitations in the static and dynamic transmission capabilities of electrical networks.

The aim of this dissertation is to propose and evaluate a power electronics based system that is able to guarantee a stable voltage profile in the HV/MV grid for the transmissible power along the power lines to be increased, using reactive shunt compensation, allowing for system operators to have a better use of line capacity without needing to build new lines, and new generation sources which are a costly endeavour and represent a mid to long term strategy. It is important to acknowledge that the use of FACTS will not solve all the existing problems, which means that although extending the lines capacity can bring benefits, sometimes it is necessary to build new lines or upgrade current and voltage capabilities of existing lines and corridors. What FACTS system can provide is an alternative to some of these problems.

The present paper is organized as follows: Section II: The designed H-bridge STATCOM is explained. Section III: Controllers design. Section IV: The PS-PWM strategy and the balancing technique for the CMC are described. Section V: In this section the simulation results for the constructed H-bridge STATCOM in the Simulink environment are presented. Section VI: This section summarizes all the achieved results.

II. MODEL

A STATCOM using a Cascade Multilevel Converter (CMC) with a star configuration, is designed in this paper. The H-

bridge STATCOM has been receiving increased attention in recent years, as well as being implemented in various markets, [1]. This sort of configurations allows for the control of the reactive power in the system, attenuation of voltage flicker, regulation of voltage in distribution lines among others. Another advantage in a cascaded H-bridge STATCOM results from the use of CMC, which offers the system added modularity and an increased number of levels for the voltage output, this will allow for a generated output voltage with less harmonics. Another advantage from using this configuration is direct connection to the grid without the need of a bulky step-up transformer, thanks to each converter being connected to a galvanic isolated DC capacitor, [1], reducing the weight added to the system by the transformer and also removing its costs and reducing losses.

Fig. 1 illustrates the system being implemented in this paper. At the point of common coupling (PCC) where the connection between the system and the STATCOM takes place a reactor is required, which serves as a current smoother to attenuate the high frequency current harmonics that the STATCOM generates, [2].

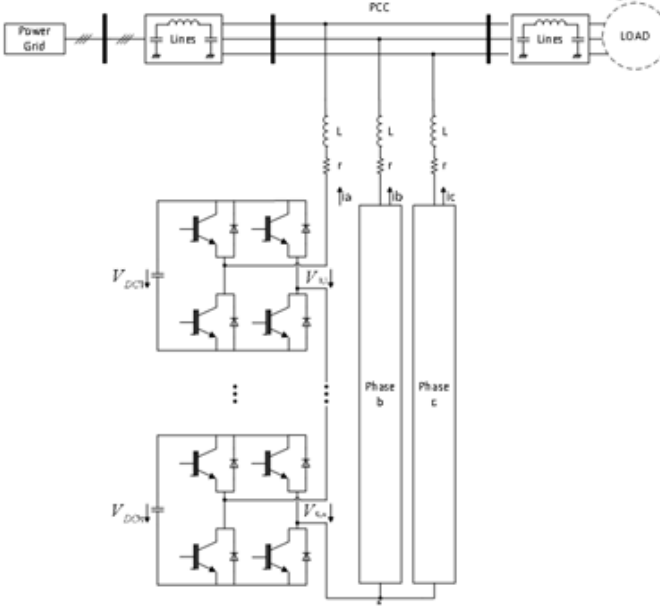


Fig. 1 – Model of an H-bridge STATCOM

A. Converter

The proposed H-bridge STATCOM uses a modular solution which results from the application of n single phase converters in series, per phase, connected in a star configuration.

The single phase converter is comprised of two arms, each with two semiconductors with turn OFF capability, with two freewheeling diodes connected in anti-parallel. The semiconductors with turn OFF capability can be either IGBTs, MOSFETs and GTOs, [3].

$$\begin{aligned} V_{DC_o} &= \sum_{i=1}^n V_i \\ Levels &= 2N + 1 \\ N_c &= 2^{N+1} - 1. \end{aligned} \quad (II.1)$$

By utilising a CMC topology the voltage output, number of levels and number of operation modes can be expressed by (II.1), where N stands for the number of modules in use.

From the analysis of Fig. 2 the STATCOM state space equations (II.2) are obtained, where $V_{PCC_{a,b,c}}$ represents the grid voltages at the PCC, $V_{o_{a,b,c}}$ is the three-phase output voltage from the CMC, and $i_{a,b,c}$ is the three-phase balanced current flowing from the STATCOM.

$$\begin{cases} V_{PCC_a} = L \frac{di_a}{dt} + Ri_a + V_{o,a} \\ V_{PCC_b} = L \frac{di_b}{dt} + Ri_b + V_{o,b} \\ V_{PCC_c} = L \frac{di_c}{dt} + Ri_c + V_{o,c} \end{cases} \quad (II.2)$$

Using the Clarke and Park transformations the system is represented in a dq coordinate synchronous reference, equation (II.3). In this equation, ωLi_d and ωLi_q represent the cross coupling terms.

$$\begin{cases} V_{PCC_d} = Ri_d + L \frac{di_d}{dt} - \omega Li_q + V_{o,d} \\ V_{PCC_q} = Ri_q + L \frac{di_q}{dt} + \omega Li_d + V_{o,q} \end{cases} \quad (II.3)$$

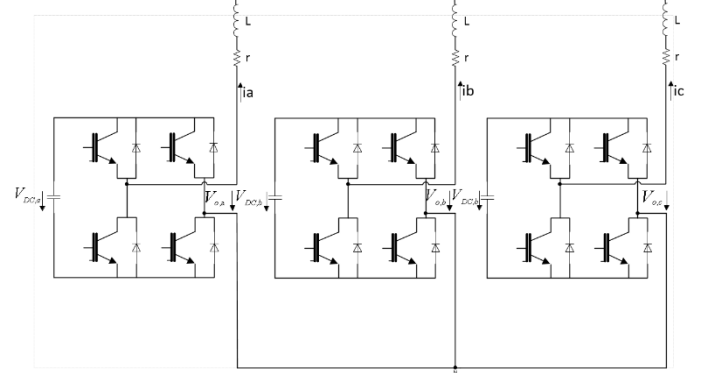


Fig. 2 – Simple representation of the system in study

Under balanced conditions, the coordinates of the voltage and current vectors in the synchronous reference frame are constant quantities. This feature is useful for analysis for decoupled control of the two current components, [3], [4], [5]. The power decoupling control, allows for separate active and reactive power control. With this information at hand the controllers needed can be designed using a decoupled methodology. Which allows for reactive power to be controlled by adjusting I_q and for active power to be controlled adjusting I_d . The active power in the STATCOM serves to compensate the voltages in the DC capacitors.

$$\begin{cases} P = V_d I_d \\ Q = -V_d I_q \end{cases} \quad (II.4)$$

The modularity that is introduced with a cascaded multilevel topology is a great advantage, as it will provide the system with added flexibility. As a result, when a module is damaged during the course of the STATCOM operation time, if the converters are correctly sized, and therefore there are extra modules, than the STATCOM can continue to operate normally, by simply bypassing the faulty modules. This will allow a faulty module to be removed without affecting the overall functioning of the

STATCOM.

The developed system is sized for a 10 kV application.

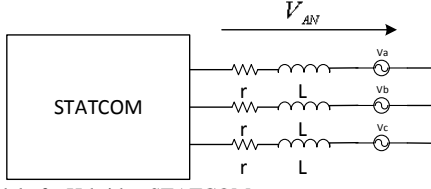


Fig. 3 – Model of a H-bridge STATCOM

The number of modules in use by the developed system, needs to guarantee that the voltage on the DC side is higher than the voltage in the AC side, to ensure that the VSC converters work adequately. The minimum number of modules, N , that the system needs can be approximately calculated from equation (II.5), where V_{DCn} is the voltage of a single DC capacitor:

$$N > \frac{\frac{\sqrt{2}V_{Sph}}{\sqrt{3}}}{V_{DCn}} \quad (II.5)$$

From the analysis of Fig. 3, the single phase voltages are:

$$\begin{cases} V_{AN} = \frac{2}{3}V_{AB} + \frac{1}{3}V_{BC} \\ V_{BN} = \frac{2}{3}V_{BC} + \frac{1}{3}V_{AC} \\ V_{CN} = \frac{2}{3}V_{CA} + \frac{1}{3}V_{AB} \end{cases} \quad (II.6)$$

With $V_{AN_{RMSmax}}$ is defined as:

$$V_{AN_{RMSmax}} \approx \frac{V_{DCo}}{\sqrt{2}} \quad (II.7)$$

To guarantee the adequate operation of the converter the value of $V_{AB_{RMSmax}}$, represented in (II.8), should be higher than the output voltage of the converter, (II.9), where i_{max} is the maximum current that is supplied by the STATCOM.

$$V_{AB_{RMSmax}} = \sqrt{3}V_{AN_{RMSmax}} \quad (II.8)$$

$$V_{DC_{omax}} \Rightarrow \sqrt{\left(\frac{\sqrt{2}V_{Sph}}{\sqrt{3}}\right)^2 + (\omega_0 L i_{max})^2} \quad (II.9)$$

The number of modules that will be used in the simulation in this dissertation is 7, with a total DC voltage capacity of 11.7 kV, that is, 1.671 kV in each capacitor, which will guarantee the correct operation of the converter and its modularity.

B. Sizing of the filtering inductors in the connection to the grid

In a converter with a high number of modules, when compared to other topologies, a connection filter with a lower value can be used, as the harmonic contents decrease for higher number of levels.

To calculate the filter, equation (II.10) is used where V_{DCk} represents the output voltage of one module, f_c is the switching frequency, and ΔI_{Lmax} is maximum ripple of the current.

$$L = \frac{V_{DCk} T_c}{2 \cdot \Delta I_{Lmax}} = 13mH \quad (II.10)$$

The internal resistance of the inductor r_L can be estimated

from (II.11), where P_d is the dissipated power.

$$r_L = \frac{P_d}{I_{cmax}^2} = 5 m\Omega \quad (II.11)$$

C. Sizing of the DC capacitors

The design of the DC capacitors starts with studying the relation of the DC voltage and the AC voltage. Also, the capacitors should be able to supply power for a certain duration without discharging below an established value that would compromise the normal operation of the converter. Another factor that needs to be taken into account is that a voltage fault consists in an abrupt loss of voltage that can go from ninety to five percent of the nominal value for a duration that can last from a few milliseconds to a minute [6]. Interruptions have three classifications: momentary (few ms to 3 seconds), temporary (lasting 3 seconds to 1 minute) and sustained (lasting more than 1 minute), [7].

$$W_c = \frac{1}{2} CV^2 \quad (II.12)$$

$$C = \frac{2P\Delta t}{V_{initial}^2 - V_{final}^2} = 0.1516 F \quad (II.13)$$

Using equation (II.13) the capacitance of the DC converters can be obtained. To create a STATCOM model as close as possible to reality, each capacitor will be considered to have a slight deviation from the calculated value from (II.13).

D. Semiconductors

In this work the chosen semiconductors are Insulated Gate Bipolar Transistor (IGBT), [8], which are usually preferred for applications with low duty cycle, low frequency (<20kHz), high voltage and current applications, high output powered demands. It should be noted that when choosing an IGBT the highest voltage the IGBT should block, should be no higher than eighty percent of the V_{CES} rating, amongst other more technical reasons.

In the present work the voltage per DC capacitor is:

$$V_{DCn} = \frac{11.7}{7} kV = 1.671 kV \quad (II.14)$$

To guarantee the safety margin the semiconductor should be sized to be able to block a voltage of:

$$V_{CES} = 2500 V \quad (II.15)$$

Which guarantees a safety margin of 50%.

The maximum value of the RMS current in the semiconductors is:

$$i_{rms} = \frac{i_{ac}}{\sqrt{2}} = \frac{350}{\sqrt{2}} = 247.49 A \quad (II.16)$$

To determine the average value of the current it is necessary to use the relation between the power of the DC side and AC side. Therefore, from equation (III.8) the DC current i_{DC} in the capacitors can be obtained, and then the average value of the current in each semiconductor can be calculated using from (II.17).

$$i_{av} = \frac{i_{dc}}{2} = 63.45 A \quad (II.17)$$

The IGBT used in this work should be able to block a voltage of 2.5 kV and a maximum current of 400 A.

III. CONTROLLERS DESIGN

A. Control Method

The proposed feedback decoupled control scheme is presented in Fig. 4. For both the voltage and current loop, Proportional-Integral (PI) controllers are designed, with its components defined in rotating *synchronous coordinates* dq , [3], [4], [9]. The use of PI compensators is a common choice, as they guarantee fast responses times and zero tracking error to the step response.

The proposed control scheme uses four PI compensators and the coordinates transformations described in the previous chapter, will be an integral part of the controllers designed in this dissertation. The PI compensator that allows for the DC capacitors to be balanced controls the active power that results from the power losses in each converter. The output of this PI compensator is the current reference for the grid i_d current.

The PI controller that outputs the reactive current reference uses the information of the d component voltage at the PCC in order to determine the necessary reactive compensation to keep a stable voltage profile along the line. In the current control stage, the reference voltages for the modulating wave are obtained, which are then used for the gating signals.

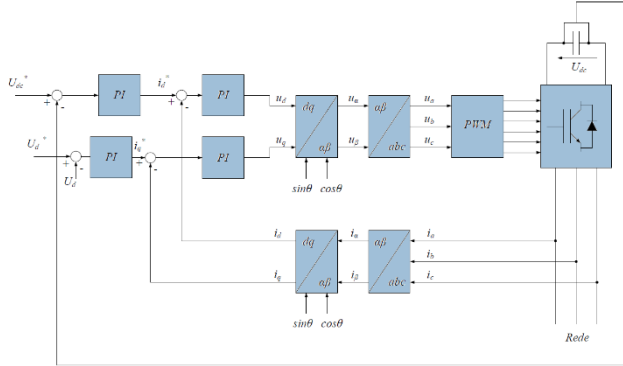


Fig. 4 - Control Scheme

B. Current Control loop

The inner control loop, otherwise known as the current controller, is designed as a PI controller, so that a fast response and a zero steady-state error to step response can be obtained. From Fig. 2 the following equations are obtained:

$$\begin{cases} i_a = \frac{V_{DCo,a} - V_{aN}}{R + sL} \\ i_b = \frac{V_{DCo,b} - V_{bN}}{R + sL} \\ i_c = \frac{V_{DCo,c} - V_{cN}}{R + sL} \end{cases} \quad (III.1)$$

The compensator and the converter will be described as follows:

$$C(s) = K_p + \frac{K_i}{s} = \frac{sT_z + 1}{sT_p} \quad (III.2)$$

$$G(s) \approx \frac{K_D}{1 + sT_d} \quad (III.2)$$

The gain K_D is obtained from the ratio between the voltage in the DC side and the maximum voltage of the carrier wave:

$$K_D = \frac{V_{DCo,max}}{V_p} \quad (III.3)$$

The delay used in this sort of endeavours can be a value belonging to the interval $[0, T_c]$, therefore it will be defined to be half of the commutation time.

$$T_d = \frac{T_c}{2} \quad (III.4)$$

Solving the closed loop system present in Fig. 5 will yield (III.5), which is then solved as a second order system to obtain the values of K_p and K_i in (III.6).

$$H(s) = \frac{i}{i_{ref}} = \frac{\frac{K_D}{T_p T_d R}}{s^2 + \frac{s}{T_d} + \frac{K_D}{T_p T_d R}} \quad (III.5)$$

$$\begin{cases} T_z = \frac{L}{R} \\ T_p = \frac{2T_d K_D}{R} \end{cases} \Rightarrow \begin{cases} K_p = \frac{T_z}{T_p} = 0.0056 \\ K_i = \frac{1}{T_p} = 53.420 \end{cases} \quad (III.6)$$

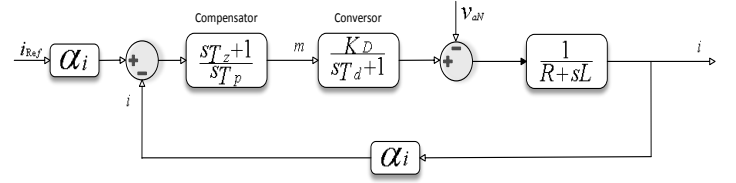


Fig. 5 - Current Control

C. Voltage Control loop

The outer control loop, otherwise known as voltage controller, is designed as a PI controller, this controller will have a slower time than the current controller.

The relation between the current the flows from the STATCOM and the voltage of the converter is obtained from:

$$i_c = C \frac{dv_{DC}}{dt} \Rightarrow i_c = sCv_{DC} \Leftrightarrow v_{DC} = \frac{1}{sC} i_c \quad (III.7)$$

The relation between the DC capacitors charging/discharging current and the current that flows out in the AC side. This can be done using the relationship between the input/output power (III.8).

$$P_{DC} = P_{AC} \Leftrightarrow V_{DC} i_{DC} = 3V_{ef} I_{ef} \quad (III.8)$$

With the following relationship of the Power at the AC side and DC side the voltage control loop can be built, as illustrated in Fig. 6.

The gain K , represents the coefficient between the DC and AC side of the converter.

$$K = \frac{i_{DC}}{I_{ef}} = \frac{3V_{ef}}{V_{DC}} \quad (III.9)$$

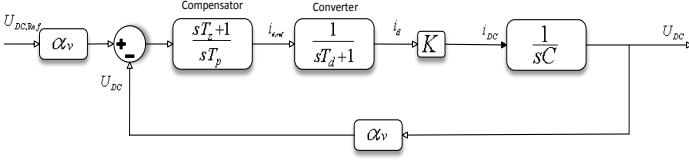


Fig. 6 - Voltage Control Loop

From Fig. 6, the voltage response of the system to the load can be acquired, which is presented in (III.10).

$$\left. \frac{V_{DC}}{V_{DC,ref}} \right| = \frac{(sT_z + 1) \frac{\alpha_v K_i K}{CT_d}}{s^3 + \frac{s^2}{T_d} + \frac{s \alpha_v K_p K}{CT_d} + \frac{\alpha_v K_i K}{CT_d}} \quad (\text{III.10})$$

The next step consists in taking into account the final value theorem (III.11).

$$\lim_{s \rightarrow 0} \frac{V_{DC}}{V_{DC,ref}} = 1 \quad (\text{III.11})$$

In order to calculate the PI controller parameters, the denominator of equation (III.11), in canonical form, must be compared to the third order polynomial present in equation (III.12), [6].

$$P_3(s) = s^3 + 1.75\omega_0 s^2 + 2.15\omega_0^2 s + \omega_0^3 \quad (\text{III.12})$$

Following these steps allow for the conclusions presented in (III.13) to be taken.

$$\begin{cases} 1.75\omega_0 = \frac{1}{T_d} \\ 2.15\omega_0^2 = \frac{\alpha_v K_p K}{T_d C} \\ \omega_0^3 = \frac{\alpha_v K_i K}{T_d C} \end{cases} \Leftrightarrow \begin{cases} K_p = \frac{2.15C}{1.75^2 \alpha_v T_d K} \\ K_i = \frac{C}{1.75^3 \alpha_v T_d K} \end{cases} \Leftrightarrow \begin{cases} K_p = 106.7498 \\ K_i = 2837.2 \end{cases} \quad (\text{III.13})$$

IV. PS-PWM AND DC VOLTAGE BALANCING TECHNIQUE

A. PS-PWM

This solution was chosen due to it having dynamic performance, being more robust in line disturbances and faults, and more flexible in applications, compared to the staircase solutions [7], as well as minimizing the outputs total harmonic distortion, the application of this strategy to a CMC enhances output voltages, reduces voltage stress on semiconductor switches and lowers acoustic noise and electromagnetic interference (EMI), [8], [9], [10]. The solution is also an important part in the correct operation of the STACOM system, as it will allow for some degree of control in the individual DC capacitor voltages, because it will operate by distributing an equal workload among the modules, guaranteeing the minimization of the error in the total average voltage of the DC

capacitors.

When implementing a PS-PWM technique, it is necessary to create a phase difference in the triangular carrier waves. This means each phase will receive the modulation waveforms from the controller, but in each module of the system, there will be a phase difference in the triangular carrier waveforms in order to correctly send the signals to the gates, which will allow for the correct operation of the CMC and will produce the maximum number of levels in the output.

The developed system is operated at $f_c = 5 \text{ kHz}$ and the number of modules in each phase is $N = 7$. Therefore, the phase shift of the triangular carrier waveforms will be given by (IV.1), that is: they will be shifted ϕ_{ps} , where n represents the index of the module.

$$\phi_{ps} = n \frac{T_c}{N} \quad (\text{IV.1})$$

B. Capacitors Voltage Balancing

The implementation of a PS-PWM technique, provides the system with a reasonable control over the voltage profile of the DC capacitors, but due to the existence of losses from the systems components which aren't equal for all the converters allied with the fact that the control method implemented with PS-PWM is made taking into account the average value of the various capacitors and that these capacitors aren't all used in the same fashion [7], there will be a divergent behaviour of the various voltages when the need to transfer power occurs. It becomes necessary to implement a second system, with a slower reaction time to the first, otherwise some conflicts may occur. If the voltages are not balanced it may affect the voltage output of the convert which can lead to the system not working as it was designed to.

The voltage balancing technique is developed taking advantage of the systems redundant levels. These redundant levels can be used by taking a configuration that produces the same voltage output, but allows for the charging or discharging of a capacitor whose voltage needs to be compensated.

The current CMC is being developed to have 7 modules, which means it has $2N + 1 = 15$ levels and $2^{N+1} - 1 = 255$ combinations to produce said levels.

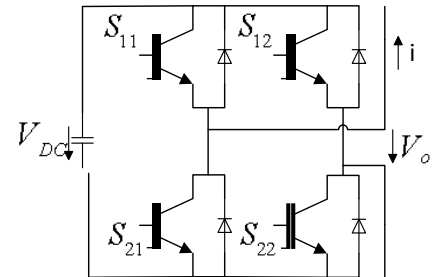


Fig. 7 - Single Converter

From Fig. 7 it can be seen that when the converter is producing a voltage of $+V_{DC}$, that is S_{11} and S_{22} are ON while S_{12} and S_{21} are OFF, and the current is positive then the capacitor will start discharging, on the other hand, if the current is negative than the capacitor will be charged. If the converter

is producing a voltage of $-V_{DC}$, that is S_{12} and S_{21} are ON while S_{11} and S_{22} are OFF, than with a positive current the capacitor will be charged, and with a negative current the voltage will be discharged. In the case that the output voltage from the converter is 0 then independently of the current there will be no change to the capacitors voltage. With this information it is possible to build Table 1.

Table 1 - Capacitor Behaviour

i_a	S_{11}	S_{12}	S_{21}	S_{22}	V_{PWM}	V_{DC}
>0	1	0	0	1	$+V_{DC}$	\downarrow
<0	1	0	0	1	$+V_{DC}$	\uparrow
>0	1	0	1	0	0	\rightarrow
<0	1	0	1	0	0	\rightarrow
>0	0	1	0	1	0	\rightarrow
<0	0	1	0	1	0	\rightarrow
>0	0	1	1	0	$-V_{DC}$	\uparrow
<0	0	1	1	0	$-V_{DC}$	\downarrow

The Algorithm used for the capacitors balancing works as follows:

1. The DC capacitor reference, $V_{DC,ref}$, the voltage level of individual capacitors, the intended voltage output, and the sign of the AC currents are acquired and analysed.
2. The voltages deviation from their reference $\Delta V_{DC,i} = V_{DC,ref} - V_{DC,i}$, where i represents the index of the module, are calculated.
3. With the information provided by the PWM, the voltage level that is to be implemented is determined. From this information the number of redundant levels is known.
4. Arranging $\Delta V_{DC,i}$:
 - When the applied voltage level output is positive and the AC current sign is higher than zero, than $\Delta V_{DC,i}$ should be sorted from smallest to biggest, as the capacitors will discharge. On the other hand if the current sign is negative then $\Delta V_{DC,i}$ should be sorted from biggest to smallest, as in this case the capacitors will charge.
 - When the applied voltage level output is negative, and the AC current sign is higher than zero, than $\Delta V_{DC,i}$ should be sorted from biggest to smallest, as the capacitors will charge. On the other hand if the current has a negative signal then $\Delta V_{DC,i}$ should be sorted from smallest to biggest, and in this case the capacitors will discharge.
 - If the current is zero than the algorithm should be exited and the original signals will be sent with no changes.
5. With $\Delta V_{DC,i}$ ordered, each element will be attributed a weight value. The first element of the array will be given the highest weight value, and from there each element will be given subsequently lower weight values until the last element receives the smallest weight value.

6. It is determined which is the combination from the possible redundancies that has the highest weight value.
7. With the information obtained in the last step, it is necessary to send the driving signals to the switches in order to apply the desired AC voltage level with the desired combination of modules.

V. SIMULATION RESULTS

This section will test the designed systems capabilities to perform the various tasks needed.

A. Capacitive Compensation

For this simulation the system starts in rated conditions and at $t = 80 \text{ ms}$ a step is applied to $I_{q,ref}$, as illustrated in Fig. 8. This will lead to a change in the modulation index, as the system reacts to the current controller, thus changing the driving signals sent to the semiconductors of the numerous modules in the STATCOM.

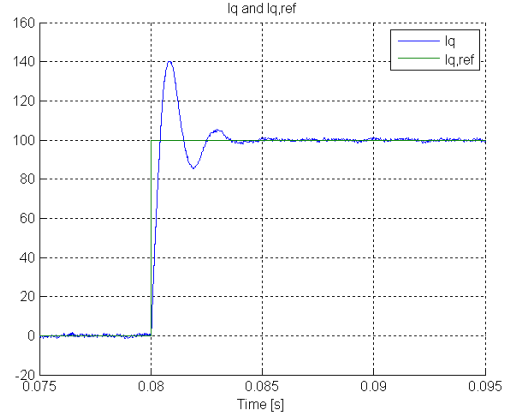


Fig. 8 - I_q and $I_{q,ref}$

The effects of this step in the $I_{q,ref}$, current are illustrated in Fig. 9, where the voltage and current that flow from the STATCOM at the PCC are represented. When the step is applied to $I_{q,ref}$ there is a transition period, as the system responds to the controllers, after which the current will lead the voltage by approximately 90° , which is an indicative that the STATCOM is operating in capacitive mode, and therefore the STATCOM will provide the system with reactive power.

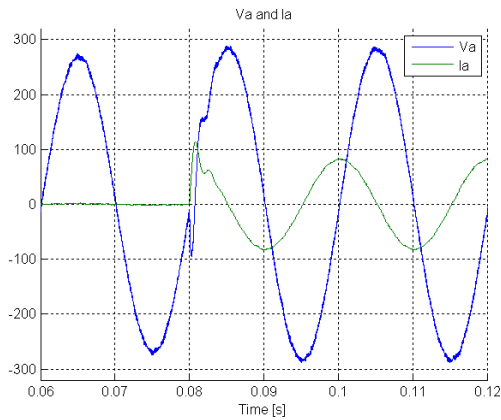


Fig. 9 - Voltage and current of phase A at the PCC

When working in capacitive mode the STATCOM will increase the voltage at the PCC. This is directly caused by the increase in the voltage output of the CMC, as seen in Fig. 10, which means that in order to have the STATCOM working in capacitive mode the voltage level of the CMC needs to be increased, and therefore the voltage of the DC side is higher than the AC side. As a result, a leading current is then produced and the STATCOM enters capacitive mode as previously shown.

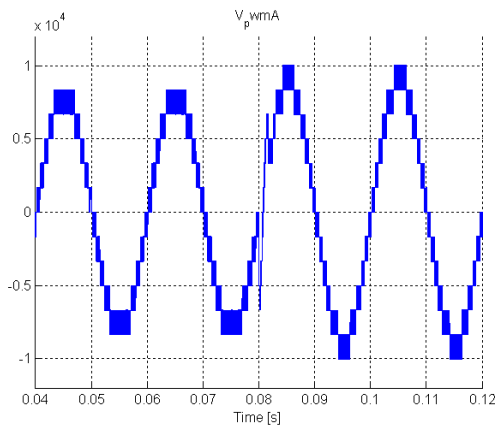


Fig. 10 – Voltage output of the CMC in phase A

B. Inductive Compensation

This section will continue evaluate several scenarios of operation, but this time it will focus on the inductive behaviour of the STATCOM.

As the simulation starts, the system is working in rated conditions. At $t = 80\text{ ms}$ a negative step is applied to the reference current $I_{q,ref}$, as shown in Fig. 11. This will lead to a response from the controllers, where the system adapts to the new operation conditions, and the STATCOM switches to inductive mode, which means that the STATCOM will now consume reactive power from the grid.

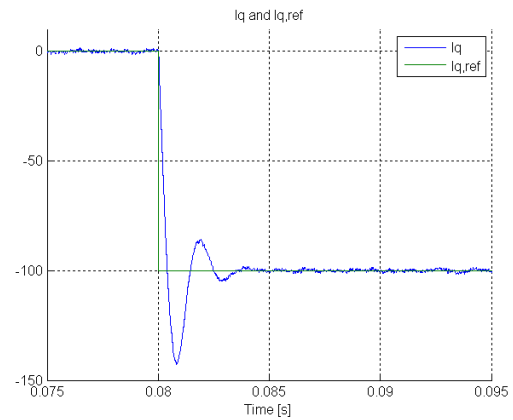


Fig. 11 - I_q and $I_{q,ref}$

From Fig. 12, it is possible to analyse the behaviour of the voltage and current, that is to say, it is possible to see how the current will respond to the STATCOM operated in inductive mode. The analysis is done at the PCC, from which it is possible to see that after $t = 80\text{ ms}$ the voltage will lead the current by approximately 90° , as would be expected.

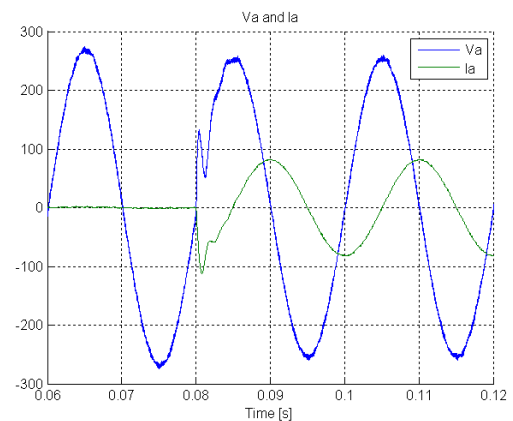


Fig. 12 - Voltage and current of phase A at the PCC

When operating in inductive mode the STATCOM will lower the voltage at the PCC. This is directly caused by a decrease in the voltage output of the CMC, as seen in Fig. 13.

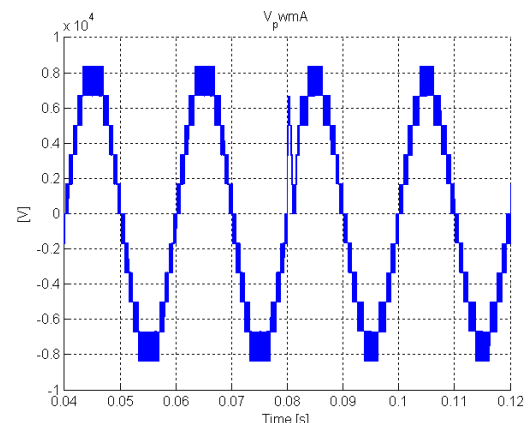


Fig. 13 - Voltage output of the CMC in phase A

C. Compensation a Capacitive Load

A capacitive load is connected to the system with $C = 7.79 \mu F$ and will cause the current to lead the voltage by approximately 17.46° , as demonstrated in the beginning of Fig. 14.

At $t = 100 \text{ ms}$ the STATCOM has a negative step is applied to the reference current, $I_{q,ref}$, as illustrated in Fig. 15. The inductive current produced by the STATCOM successfully counters the effects of a capacitive load, as demonstrated in Fig. 14.

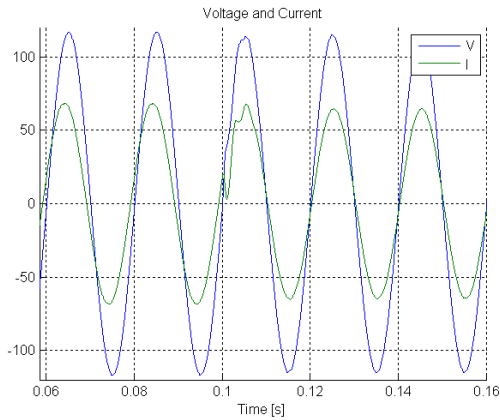


Fig. 14 - Voltage and current of phase A at the PCC

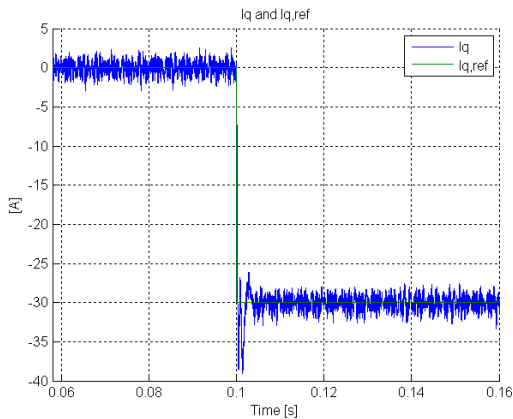


Fig. 15- I_q and $I_{q,ref}$

D. Voltage Balancing at the DC Level

To demonstrate the developed voltage balancing technique, the voltages in the DC level of phase A will be unbalanced. The results show that without the use of the balancing technique, Fig. 16, the system will not try to stabilize the individual voltages of the DC capacitors, to the value of $V_{DC,ref}$, but will ensure that the average value in the DC level is in fact $V_{DC,ref}$. Whilst with the balancing technique, Fig. 17, the voltages are successfully balanced leaving a smaller margin of error between the various voltages in the DC level.

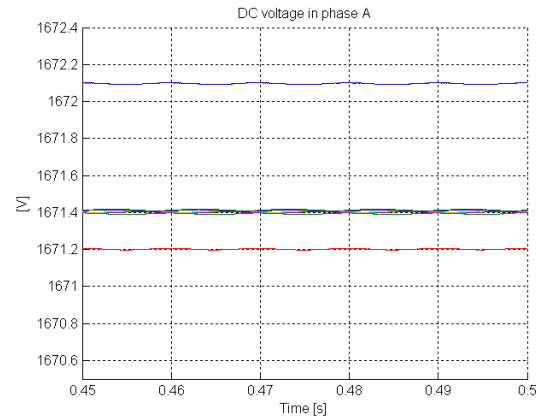


Fig. 16 - DC voltages without compensation system

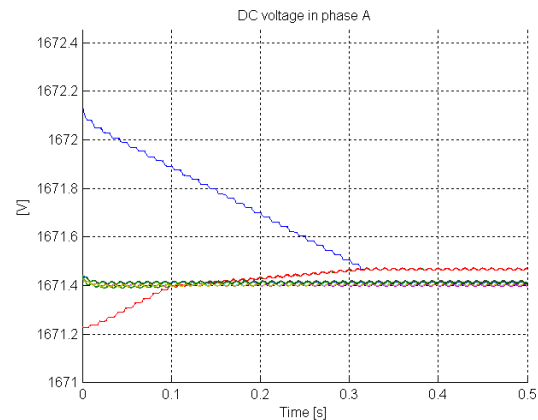


Fig. 17 - DC voltage with compensation system

E. Voltage sags

A voltage sag at the source is analysed. A voltage drop of 25% occurs at the source. In order to compensate this voltage dip, the STATCOM needs to enter capacitive mode. From the analysis of the voltage at the PCC a positive step is applied to the reference current, $I_{q,ref}$, which is illustrated by Fig. 18. When the STATCOM functioning in capacitive mode it will supply a current that will be ahead of the voltage, Fig. 19.

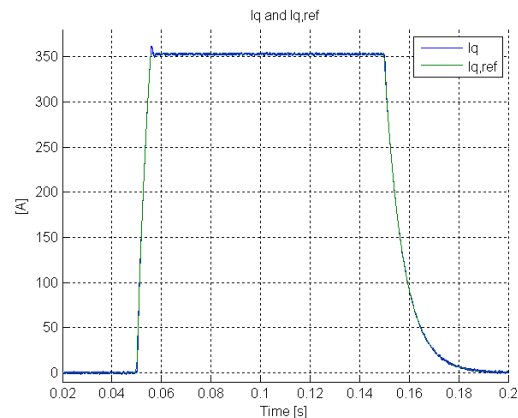


Fig. 18 - I_q and $I_{q,ref}$

The STATCOM successfully compensates the fault which can be seen in Fig. 20, where the voltage profile is maintained at the

desired value. In order to enter a capacitive mode the voltage level used in the DC side is elevated as seen in Fig. 21

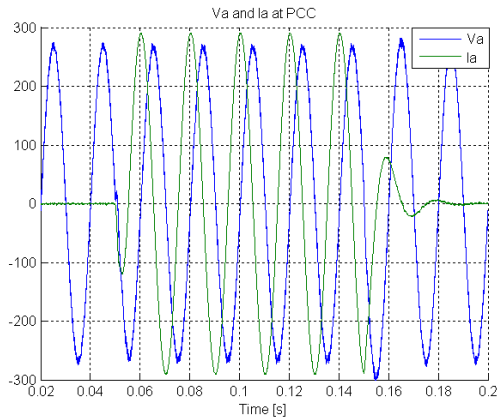


Fig. 19 - Voltage and current of phase A at the PCC

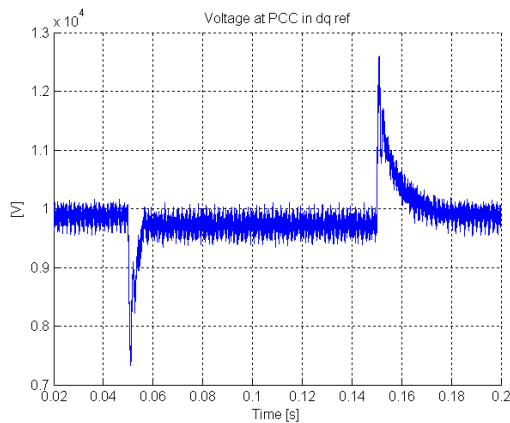


Fig. 20 - Voltage at the PCC

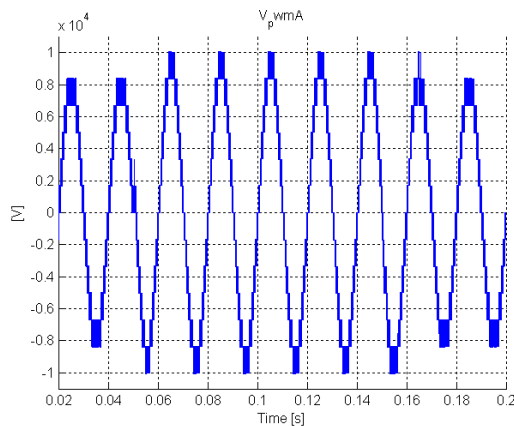


Fig. 21 - Voltage output of the CMC in phase A

F. Modularity

To simulate the modularity of the STATCOM, and showcase the systems stability, the following simulation was done. At $t = 50 \text{ ms}$ one module, per phase, is going to be disconnected from the STATCOM, this means that the STATCOM will go from functioning with seven modules and fifteen levels to functioning with six modules and thirteen levels, per phase. When the command is sent to disconnect the modules it is

important that the system is capable of adjusting the phase shift parameters to suit the new conditions of the system. A simple recalculation during the simulation takes place, using equation (IV.1), with the new number of modules, for the updated phase shift to be implemented.

From Fig. 22 the modulation wave can be seen to suffer an increase with the loss of the modules which will result in a higher voltage level applied by the CMC, as shown in Fig. 23, this occurs due to the converter having a lower number of levels to present whilst performing the same task. From Fig. 24 it can be seen that the STATCOM continues to perform its task of maintaining the voltage at the load, without any issues.

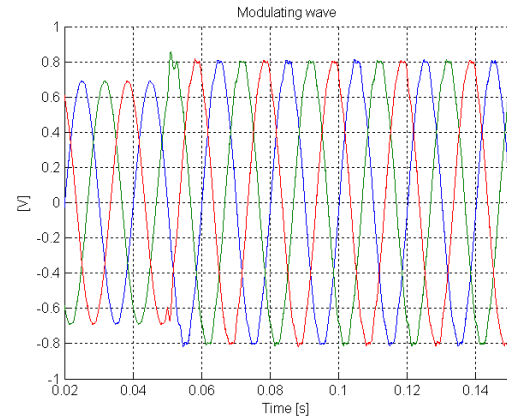


Fig. 22 - Modulation wave

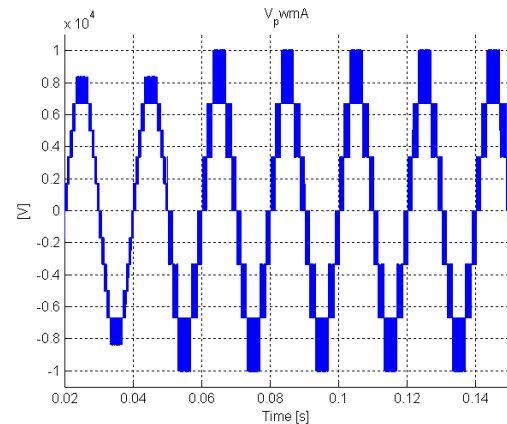


Fig. 23 - Voltage output of the CMC in phase A

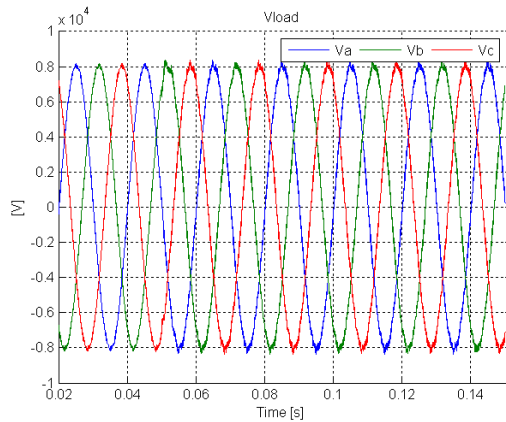


Fig. 24 - Voltage at Load

VI. CONCLUSION

An H-bridge STATCOM using a star CMC configuration has been presented. The implemented solution proved that it could provide both capacitive and inductive compensation, as well as maintaining the voltage profile at the load in the eventuality of a voltage sag or overvoltage. The DC voltage balancing technique was successfully implemented, and showed that the utilization of redundancies is viable. The modular approach showed its benefits by enabling the system to work, even in the eventuality that the system would lose few modules.

Future work that can be done includes::

- Design the system to take into account non balanced faults, which can be quite prevalent.
- Comparison to other CMC configurations, one example of this would be the use of a triangle configuration.
- Adding more modules to the converter, and in this way building the system up so that it could be implemented in High Voltage systems.
- Testing the designed model in a lab implementation.
- Comparing the obtained DC voltage balancing technique to other techniques.

• REFERENCES

- [1] H. Akagi, S. Inoue and T. Yoshii, "Control and Performance of a Transformerless Cascade PWM STATCOM With Star Configuration," *IEEE Trans. On Industry App.*, vol. 43, no. 4, pp. 1041-1049, 2007.
- [2] X. Xiang-lian, Z. Yun-ping, W. Cheng-zhi e H. Hong-yuan, "Research on cascaded multilevel inverter and its application in STATCOM," *Front. Electr. Electron. Eng. China*, pp. 390-395, February 2006.
- [3] F. A. Silva, J. J. Santana and S. F. Pinto, *Conversores Comutados para Energias Renováveis*, vol. 45, Instituto Superior Técnico, 2012.
- [4] J. F. Silva e S. F. Pinto, "Advanced Control of Switching Power Converters," em *Power Electronics Handbook*, Burlington, Buterworth-Heinemann, 2011, pp. 1037-1113.
- [5] C. Schauder e H. Mehta, "Vector Analysis and Control of Advanced Static Var Compensators," *Electric Power Research Institute*, pp. 266-272.
- [6] E. 50160, *Voltage Characteristics of Electricity Supplied by Public Electricity Networks*, Standard EN 50160, 2010.
- [7] UST, "Utility Systems Technologies, Inc.," [Online]. Available: <http://www.ustpower.com/power-quality-glossary/>.
- [8] C. Blake e C. Bull, *IGBT or MOSFET: Choose Wisely*, International Rectifier.
- [9] C. T. Rim, N. S. Choi, G. C. Cho e G. H. Cho, "A complete DC and AC analysis of three-phase controlled-current PWM rectifier using circuit D-Q transformation," *IEE Trans. Power Electron*, vol. 9, pp. 390-396, 1994.
- [10] S. Pinto, J. F. Silva, F. Silva e P. Frade, "Design of a Virtual Lab to Evaluate and Mitigate Power Quality Problems Introduced by Microgeneration," *Instituto Superior Técnico*, 2011.
- [11] T. Yoshii, S. Inoue e H. Akagi, "Control and Performance of a Medium Voltage Transformerless Cascade PWM STATCOM with Star-Configuration," *IEEE*, 2006.
- [12] P. Palanivel e S. Dash, "Phase Shifted Carrier Pulse Width Modulation for Three Phase Multilevel Inverter to Minimize THD and Enhance Output Voltage Performance," *J. Eletrical Systems*.
- [13] R. Naderi e A. Rahmati, "Phase-Shifted Carrier PWM Technique for General Cascaded Inverters," *IEEE Trans. Power Electron*, vol. 23, pp. 1257-1269, 2008.
- [14] C. Boonmee e Y. Kumsuwan, "A Phase-shifted Carrier-Based PWM Technique for Cascaded H-bridge Inverters Application in Standalone PV System," em *Rec. IEEE EPE-PEMC'12*, Novi Sad, 2012.
- [15] S. Paiva, *Redes de Energia Electrica: uma análise sistémica*, vol. 60, Instituto Superior Técnico, 2007, pp. 1286 - 1299.