Three Phase Load Balancing and Power Factor Correction Using a Pulse Width Modulated Static Compensator

by

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A thesis

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requirement for the degree of

Master of Science

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THREE PHASE LOAD BALANCING AND POWER FACTOR CORRECTION USING A PULSE WIDTH MODULATED STATIC COMPENSATOR

BY

CHRISTOPHER ANDREW STRUTHERS

A Thesis/Practicum submitted to the Faculty of Graduate Studies of The University of

Manitoba in partial fulfillment of the requirement of the degree

of

MASTER OF SCIENCE

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ABSTRACT

The purpose of this thesis is to demonstrate that a pulse-width-modulated static compensator is capable of performing three-phase load balancing and power factor correction. An unbalanced load is analysed using sequence component theory and a mathematical solution found to satisfy the load balancing and power factor correction requirements. Two types of pulse-width modulation to implement this theory are investigated - sinusoidal pulse width modulation and current reference pulse width modulation. Control systems have been developed for both methods. Both methods have then been simulated using PSCAD / EMTDC software with the results analysed for dynamic response, steady state response and harmonic content.

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LIST OF SYMBOLS

Abbreviations and symbols used in this thesis are tabulated below:

Α	Amperes
α	Complex Constant - 1 at 120 degrees.
AC	Alternating Current
COMP	Compensator
COS	Cosine Function
CRPWM	Current Reference Pulse Width Modulation
DC	Direct Current
DVR	Dynamic Voltage Regulator
FACTS	Flexible AC Transmission Systems
FFT	Fast Fourier Transform
GTO	Gate Turn-Off Thyristor
HVDC	High Voltage DC
HZ	Hertz
IMAG	Imaginary Part of Complex Number
KW	Kilowatts
KA	Kilo-amps
KVA	Kilovolt-amps
KVAR	Kilovolt-amp Reactive
L-L	Line to Line
L-G	Line to Ground
MVA	Megavolt-amps
MVAR	Megavolt-amps Reactive
MW	Megawatts
PI	Proportional Integral Controller
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
REF	Reference

SIN	Sine Function
SPWM	Sinusoidal Pulse Width Modulation
STATCOM	Static Synchronous Compensator
SVC	Static Var Compensator
TCR	Thyristor Controlled Reactor
TSC	Thyristor Switched Capacitor
UPFC	Unified Power Flow Controller
uS	Microsecond
VSI	Voltage Source Inverter

Chapter 1

INTRODUCTION TO STATCOM AND LOAD BALANCING APPLICATIONS

Ongoing developments in solid-state power electronic devices have paved the way for extensive progress in the field of power quality. Faster, more reliable and more easily controlled power electronic devices have allowed the development of Static Var Compensators (SVC's), Dynamic Voltage Regulators (DRV's), Static Synchronous Compensators (STATCOM's), Unified Power Flow Controllers (UPFC's) among other Flexible AC Transmisison System (FACTS) devices. [1]

These devices can be applied to provide power factor correction, three phase load balancing, voltage regulation, flicker control, harmonic elimination, increased network stability and better control of power flow.

The main objective of this investigation is to provide three-phase load balancing and power factor correction using a Pulse Width Modulated (PWM) STATCOM.

1.1 The Need for Compensation

Certain industrial loads do not draw equal load currents from all three phases. Single phase railway loads and electrical arc furnaces are the two most common examples. Large unbalanced loads often result in a voltage imbalance in the power system, which thereby affects other customers. Cage induction motors are affected by even a minor voltage imbalance, which results in additional heating and unbalanced mechanical torque. Thus is it desirable to compensate a highly unbalanced load, so that the network does not suffer the effects of imbalance.

Loads with large reactive power requirements draw a lot of reactive current from the network which leads to poor voltage regulation and limits the controllability and the amount of real power that can be delivered. Thus it is also desirable to provide reactive power compensation to a highly inductive load.

1.2 Traditional Solution

Both of these compensation requirements have traditionally been satisfied using SVC's. [2]. SVC's generally consist of thyristors controlled reactors (TCR's), and thyristor switched capacitors (TSC's). A typical single-phase of a shunt-connected SVC is shown in Figure 1.1 below:



Figure 1.1: Example of TCR / TSC.

The TCR valves are fired every cycle between 90° and 180° to allow a variable amount of reactive current flow. Figure 1.2 below shows the TCR currents for firing angles 105°, 120° and 160°.



Figure 1.2: Current Flow in TCR.

A firing angle of 90° allows maximum reactive current flow, while an angle approaching 180° results in zero current flow.

The TSC does not have this variable property however. Capacitor current is proportional to the derivitive of the voltage. Switching during the cycle creates a discontinuous voltage. Differentiation of the discontinuity creates unacceptable current transients. Therefore, both valves are switched either on or off completely throughout every cycle.

However, several TSC's switched on or off in parallel can be used to give some variation in

capacitive current. In conjunction with a large enough TCR the net current can be varied over the entire capacitive/inductive range.

For example, two TSC's each with ratings of 50KVAR, in conjunction with a TCR of 50KVAR will provide full reactive power compensation anywhere from 100KVAR capacitive to 50KVAR inductive.

Load balancing and power factor correction can be provided by connecting these branches into a three-phase delta configuration, and then controlling the required reactive currents on each branch.

1.3 Static Synchronous Compensators

The advent of the Gate Turn Off (GTO) thyristor has allowed the development of a highly flexible STATCOM.



GTO Voltage Source Inverter

Figure 1.3: Single Phase Model of STATCOM.

Fig 1.3 above shows a single phase STATCOM, with the GTO's modelled as ideal switches.

The two capacitors are charged to equal voltages in opposing polarities (+Vcap, -Vcap). When switch A is closed, the output voltage, *Vout*, is equal to +Vcap. When switch B is closed, *Vout* is equal to -Vcap. Switch A and B are never closed at the same time.

These switches, when opened and closed in a periodic manner, will create an output voltage that is effectively sinusoidal. The switching method of interest for this research is pulse-width modulation. The two modulation methods of interest in this research are Sinusoidal Pulse Width Modulation (SPWM) and Current Reference Pulse Width Modulation (CRPWM). These will be described further in chapters 3 and 4.

Altering the modulation of the switching signals allows control of the magnitude and phase of the output voltage which thereby controls the real and reactive current flows to the system. Figure 1.4 below shows a three phase load balancing STATCOM in greater detail. This is the model analysed throughout this investigation.



Figure 1.4: STATCOM Used for Load Balancing and Power Factor Correction.

STATCOM's are ordinarily used for balanced three-phase reactive power compensation or balanced three-phase voltage regulation. In balanced operation, GTO pairs on each phase receive the same switching signals, 120° out of phase. The capacitor voltage is varied to provide different amounts of balanced three phase reactive currents.

For a load balancing application however, differing amounts of real and reactive current are required on each phase. One way of achieving this is by fixing the capacitor voltage at a certain level and providing three different modulation signals to each GTO pair.

STATCOM's have proven to be faster and more effective than SVC's for power factor correction and flicker elimination in rapidly changing arc furnace loads [3]. It will be shown that they can also be effective for load balancing applications.

1.4 Research Objectives

The main objective of this research is to design and successfully simulate a three phase load balancing STATCOM, as shown in figure 1.4.

Two methods of pulse width modulation will be investigated, voltage controlled sinusoidal pulse width modulation and current reference pulse width modulation. They will be compared in terms of dynamic performance, harmonic analysis and steady state performance.

The additional property of active filtering [4] will be applied to the current reference pulse width modulation.

Chapter 2

LOAD BALANCING THEORY

2.1 NOTATION

Two different frames of reference for real and imaginary parts of phasor quantities are used throughout this thesis. To avoid confusion, strict notation to differentiate between the two has been adopted.

The first reference frame will be referred to as the standard phasor form. This is where real and imaginary parts of each phase are in the same plane, so they may be added or subtracted from one another. All phasors in the standard form can therefore be used in Kirchoffs current and voltage laws. The standard form, with real and imaginary parts will be denoted as follows:

$$\vec{la} = Ia_{re} + jIa_{im} \qquad \vec{lb} = Ib_{re} + jIb_{im} \qquad \vec{lc} = Ic_{re} + jIc_{im} \quad (2.1)$$

The second reference frame will be referred to as the rotated form, whereby phases B and C have been rotated by $+120^{\circ}$ and -120° respectively. This means that vectors associated with phase B will use the voltage phasor of phase B as the real axis, and likewise for phase C.

The constant α will be used to denote $1 \ge 120^{\circ}$ and α^2 for $1 \ge -120^{\circ}$. Multiplication of phasors by this constant performs the required rotations. The ' α ' and ' α^2 ' symbols will always appear in the notation for the rotated reference frame to differentiate from the standard frame.

Notation for the rotated form is shown as follows:

$$\vec{Ia} = Ia_{re} + jIa_{im} \qquad \alpha \vec{Ib} = [\alpha Ib]_{re} + j[\alpha Ib]_{im} \qquad \alpha^2 \vec{Ic} = [\alpha^2 Ic]_{re} + j[\alpha^2 Ic]_{im} \quad (2.2)$$

Note that phase A does not change. Both the values and notation remain identical.

When describing real and reactive currents on each phase, the rotated form is more useful. A real or imaginary value in the rotated form corresponds exactly to a real or reactive current value, with respect to the individual phase voltage.

Take for example, a selection of balanced three phase currents:

 $Ia = 3.16\sin(\omega t + 18^\circ)$ $Ib = 3.16\sin(\omega t - 102^\circ)$ $Ic = 3.16\sin(\omega t + 138^\circ)$ (2.3) In standard phasor form, they will be expressed as follows:

$$\vec{Ia} = 3.16 \angle 18^{\circ} \qquad \vec{Ib} = 3.16 \angle -102^{\circ} \qquad \vec{Ic} = 3.16 \angle 138^{\circ} \\ = 3 + j 1 \qquad = -0.634 - j 3.098 \qquad = -2.366 + j 2.098 \qquad (2.4)$$

With the real and imaginary parts being:

$$Ia_{re} = 3$$
 $Ib_{re} = -0.634$ $Ic_{re} = -2.366$
 $Ia_{im} = 1$ $Ib_{im} = -3.098$ $Ic_{im} = 2.098$ (2.5)

In rotated phasor form, where phases B and C are shifted by α and α^2 , they will be expressed as:

$$\vec{Ia} = 3.16 \angle 18^{\circ}$$

= 3 + j 1
 $\alpha \vec{Ib} = 3.16 \angle 18^{\circ}$
= 3 + j 1
 $\alpha^{2}\vec{Ic} = 3.16 \angle 18^{\circ}$
= 3 + j 1
(2.6)

With the real and imaginary parts being:

$$\begin{aligned} Ia_{re} &= 3 & [\alpha Ib]_{re} &= 3 & [\alpha^2 Ic]_{re} &= 3 \\ Ia_{im} &= 1 & [\alpha Ib]_{im} &= 1 & [\alpha^2 Ic]_{im} &= 1 & (2.7) \end{aligned}$$

This allows us to see immediately that the currents all consist of real current, magnitude 3, plus reactive current, magnitude 1. Figure 1.5 below shows this graphically.



Standard Phasor Form

Rotated Phasor Form



2.2 SEQUENCE TRANSFORMATIONS

Sequence transformations are an exceptionally useful tool for analysing unbalanced loads and formulating a solution to them [5].

Given three phasor quantities for currents in standard form $(\vec{Ia}, \vec{Ib}, \vec{Ic})$, the positive negative and zero sequences $(\vec{I_1}, \vec{I_2}, \vec{I_0})$ can be calculated using the following relation:

$$\begin{vmatrix} \vec{I}_1 \\ \vec{I}_2 \\ \vec{I}_0 \end{vmatrix} = \frac{1}{3} \begin{bmatrix} 1 & \alpha & \alpha^2 \\ 1 & \alpha^2 & \alpha \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} \vec{I} & \vec{I} \\ \vec{I} & \vec{I} \\ \vec{I} & \vec{I} \end{bmatrix}$$
 Where $\alpha = 1 \angle 120^\circ$ (2.8)

The relation can be inverted as follows:

$$\begin{bmatrix} \vec{I} \vec{a} \\ \vec{I} \vec{b} \\ \vec{I} \vec{c} \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ \alpha^2 & \alpha & 1 \\ \alpha & \alpha^2 & 1 \end{bmatrix} \begin{bmatrix} \vec{I}_1 \\ \vec{I}_2 \\ \vec{I}_0 \end{bmatrix} \qquad \text{Where } \alpha = 1 \angle 120^\circ \qquad (2.9)$$

2.3 ANALYSIS OF UNBALANCED LOAD

2.3.1 Sequence Transformation of Unbalanced Load

A perfectly balanced load current will contain no negative sequence component and no zerosequence component. The ultimate goal of a load-balancer is to remove these components. Note that this thesis is concerned only with star-ungrounded or delta-connected loads, so zero sequence is not a concern.

Positive sequence current of a load at unity power factor will contain no imaginary component. The load-balancer can be altered to also remove the positive sequence imaginary component of the load current to provide power factor correction.

Fig 2.1 shows examples of various delta-connected resistive loads, real-time currents and the cor-

responding sequence components $(\vec{I_1}, \vec{I_2}, \vec{I_0})$ of the load currents.



Figure 2.2: Examples of Unbalanced Loads

2.3.2 Power Oscillations of Unbalanced Loads

Instantaneous power of a balanced load is a constant non-sinusoidal value equal to the RMS power. However, instantaneous power of an unbalanced delta-connected load will oscillate at twice the system frequency, similar to that in a single-phase load.

This phenomena is best understood in terms of sequence components. Assuming a perfectly balanced source voltage, positive sequence currents provide constant power with a value equal to the total RMS power. Negative sequence currents cause the oscillations in power. The average value of these oscillations is zero. This means that negative sequence currents do not alter the total net energy flow to the load.

Equation 2.1 shows the relationship between instantaneous power (P(t)), RMS Line to Ground Voltage (V_{LG}) and sequence components of the load currents ($\vec{I_1}, \vec{J_2}$). Refer to Appendix A for the

derivation.

$$\vec{I}_1 = I_1 REAL + j \cdot I_1 IMAG \qquad \vec{I}_2 = I_2 REAL + j \cdot I_2 IMAG \qquad (2.10)$$

$$P(t) = 3V_{LG}(I_{1}REAL - I_{2}REAL\cos(2\omega t) + I_{2}IMAGsin(2\omega t))$$
(2.11)

The oscillations in instantaneous power become important when determining the energy ratings of the compensator. The storage capacitor must be large enough to absorb these energy oscillations without any detriment to performance. This will be discussed further in chapter 5.

2.4 ANALYSIS OF LOAD-BALANCER

2.4.1 Sequence Components of Load Balancer

As mentioned previously, a balanced load will contain only positive sequence currents. This can be achieved by having the load-balancer produce negative sequence currents which are exactly opposite to those in the unbalanced load.

For example, if the load contains negative sequence currents of $0.33pu \ge 60^{\circ}$ then the compensator must provide negative sequence currents of $-0.33pu \ge 60^{\circ}$.

Only three-wire loads are being considered for this research, so zero sequence is ignored. However, it is possible to develop a more complicated four wire STATCOM that is capable of compensating for zero sequence [6].

2.4.2 Power Factor Correction

Power factor correction can be added to the controls of a load-balancer fairly easily. It is simply a matter of removing the imaginary part of the positive sequence load current as well as the negative sequence. This will however require a load-balancer of higher rating.

2.4.3 Real and Imaginary Parts of Load Balancer Currents

Once the current sequence components required from the load balancer have been calculated, it is advantageous to convert these into individual per-phase current orders. These orders are best expressed in real and imaginary (reactive) parts.

Matrices (2.2) - (2.3) below show the relationship between compensator current sequence components $(\vec{I_1}, \vec{J_2})$ and the corresponding phase currents in rotated form $(\vec{Ia}, \alpha \vec{Ib}, \alpha^2 \vec{Ic})$. The term "ICHARGE" is the net real current required to keep the capacitor charged to the reference voltage. This value will be close to zero during steady state. Refer to appendix B for the derivation.

$$\begin{bmatrix} Ia_{re} \\ [\alpha Ib]_{re} \\ [\alpha^2 Ic]_{re} \end{bmatrix} = \begin{bmatrix} \frac{1}{3} & 0 & 1 & 0 \\ \frac{1}{3} & 0 & -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{3} & 0 & -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} I_{CHARGE} \\ I_{1im} \\ I_{2re} \\ I_{2im} \end{bmatrix} = \begin{bmatrix} Ia_{im} \\ [\alpha Ib]_{im} \\ [\alpha^2 Ic]_{im} \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 & 1 \\ 0 & 1 & -\frac{\sqrt{3}}{2} & -\frac{1}{2} \\ 0 & 1 & \frac{\sqrt{3}}{2} & -\frac{1}{2} \\ I_{2im} \end{bmatrix} \begin{bmatrix} I_{CHARGE} \\ I_{1im} \\ I_{2re} \\ I_{2im} \end{bmatrix}$$
(2.12)

2.5 Example of Load Balancing Solution

Take for example a single phase load of 10MW, 8MVAR on phase BC, where the line voltage is 10KV RMS.

Line to ground voltages are:

$$\overrightarrow{Va} = 5.77 \angle 0^{\circ} \qquad \overrightarrow{Vb} = 5.77 \angle -120^{\circ} \qquad \overrightarrow{Vc} = 5.77 \angle 120^{\circ} \qquad (2.13)$$

So line-line voltage on phase BC is:

$$\overrightarrow{Vbc} = \overrightarrow{Vb} - \overrightarrow{Vc} = 10 \angle -90^{\circ}$$
(2.14)

Load currents can now be solved using the relation $I = (S/V)^*$:

$$\overrightarrow{Ibc_L} = \left(\frac{\overrightarrow{Sbc}}{\overrightarrow{Vbc}}\right)^* = \left(\frac{10+j8}{-10j}\right)^* = -0.8-j1$$
(2.15)

$$\overrightarrow{Ia_L} = 0$$
 $\overrightarrow{Ib_L} = -0.8-j1$ $\overrightarrow{Ic_L} = 0.8+j1$ (2.16)

Now it is possible to calculate the sequence components of the load currents:

$$\begin{bmatrix} \overrightarrow{I}_{1L} \\ \overrightarrow{I}_{2L} \\ \overrightarrow{I}_{0L} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & \alpha & \alpha^2 \\ 1 & \alpha^2 & \alpha \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} \overrightarrow{Ia_L} \\ \overrightarrow{Ib_L} \\ \overrightarrow{Ic_L} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & (-\frac{1}{2} + j\frac{\sqrt{3}}{2}) & (-\frac{1}{2} - j\frac{\sqrt{3}}{2}) \\ 1 & (-\frac{1}{2} - j\frac{\sqrt{3}}{2}) & (-\frac{1}{2} + j\frac{\sqrt{3}}{2}) \\ 1 & (-\frac{1}{2} - j\frac{\sqrt{3}}{2}) & (-\frac{1}{2} + j\frac{\sqrt{3}}{2}) \\ 0 & (-\frac{1}{2} + j\frac{\sqrt{3}}{2}) \end{bmatrix} \begin{bmatrix} 0 \\ -0.8 - j1 \\ 0.8 + j1 \end{bmatrix} = \begin{bmatrix} -0.577 - j0.462 \\ -0.577 + j0.462 \\ 0 \end{bmatrix}$$

$$(2.17)$$

As expected, there is no zero sequence. The compensator will be required to provide opposing negative sequence real and imaginary currents for load balancing, in addition to positive sequence imaginary currents for power factor correction:

$$\begin{vmatrix} \overrightarrow{I}_{1C} \\ \overrightarrow{I}_{2C} \\ \overrightarrow{I}_{0C} \end{vmatrix} = \begin{bmatrix} j0.462 \\ 0.577 - j0.462 \\ 0 \end{bmatrix}$$
(2.18)

Equation (2.12) can then be used to find the real and imaginary parts of the required compensator currents. Capacitor charging current is assumed to be negligible (0):

$$\begin{bmatrix} Ia_{Cre} \\ [\alpha Ib_{C}]_{re} \\ [\alpha^{2}Ic_{C}]_{re} \end{bmatrix} = \begin{bmatrix} \frac{1}{3} & 0 & 1 & 0 \\ \frac{1}{3} & 0 & -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{3} & 0 & -\frac{1}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} I_{CHARGE} \\ I_{1im} \\ I_{2re} \\ I_{2im} \end{bmatrix} = \begin{bmatrix} \frac{1}{3} & 0 & 1 & 0 \\ \frac{1}{3} & 0 & -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{3} & 0 & -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} 0 \\ 0.462 \\ 0.577 \\ -0.462 \end{bmatrix} = \begin{bmatrix} 0.577 \\ -0.689 \\ 0.111 \end{bmatrix}$$
(2.19)

$$\begin{bmatrix} Ia_{Cim} \\ [\alpha Ib_{C}]_{im} \\ [\alpha^{2}Ic_{C}]_{im} \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 & 1 \\ 0 & 1 & -\frac{\sqrt{3}}{2} & -\frac{1}{2} \\ 0 & 1 & \frac{\sqrt{3}}{2} & -\frac{1}{2} \end{bmatrix} \begin{bmatrix} I_{CHARGE} \\ I_{1im} \\ I_{2re} \\ I_{2im} \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 & 1 \\ 0 & 1 & -\frac{\sqrt{3}}{2} & -\frac{1}{2} \\ 0 & 1 & \frac{\sqrt{3}}{2} & -\frac{1}{2} \end{bmatrix} \begin{bmatrix} 0 \\ 0.462 \\ 0.577 \\ -0.462 \end{bmatrix} = \begin{bmatrix} 0 \\ 0.193 \\ 1.193 \end{bmatrix}$$
(2.20)

This shows that in order to balance the load and correct the power factor, the compensator must do the following:

Draw 0.577KA and 0.111KA real current from phases A and C respectively, and deliver the sum, 0.689KA, to phase B

Draw 0.193KA and 1.193KA of leading reactive current from phases B and C.

Net real power transfer is zero.

The sum of the reactive currents is 1.386KA. Multiplication by the line voltage, 5.77KV, shows the net reactive power transfer is 8 MVAR capacitive, the same quantity consumed by the load.

This solution can be proved by rotating the compensator currents back to standard phasor form:

$$\begin{bmatrix} \overrightarrow{Ia_C} \\ \overrightarrow{Ib_C} \\ \overrightarrow{Ib_C} \\ \overrightarrow{Ic_C} \end{bmatrix} = \begin{bmatrix} Ia_{Cre} + jIa_{Cim} \\ \alpha^2([\alpha/b_C]_{re} + j[\alpha/b_C]_{im}) \\ \alpha([\alpha^2/c_C]_{re} + j[\alpha^2/c_C]_{im}) \end{bmatrix} = \begin{bmatrix} 0.577 \\ (-\frac{1}{2} - j\frac{\sqrt{3}}{2})(-0.689 + j0.193) \\ (-\frac{1}{2} + j\frac{\sqrt{3}}{2})(0.111 + j1.193) \end{bmatrix} = \begin{bmatrix} 0.577 \\ 0.512 + j0.5 \\ -1.089 - j0.5 \end{bmatrix}$$
(2.21)

Then summated with the load currents to find the total system currents:

$$\begin{bmatrix} \overrightarrow{Ia_S} \\ \overrightarrow{Ib_S} \\ \overrightarrow{Ic_S} \end{bmatrix} = \begin{bmatrix} \overrightarrow{Ia_C} \\ \overrightarrow{Ib_C} \\ \overrightarrow{Ic_C} \end{bmatrix} + \begin{bmatrix} \overrightarrow{Ia_L} \\ \overrightarrow{Ib_L} \\ \overrightarrow{Ic_L} \end{bmatrix} = \begin{bmatrix} 0.577 \\ 0.512 + j0.5 \\ 1.089 + j0.5 \end{bmatrix} + \begin{bmatrix} 0 \\ -0.8 - j1 \\ 0.8 + j1 \end{bmatrix} = \begin{bmatrix} 0.577 \\ -0.288 - j0.5 \\ -0.288 + j0.5 \end{bmatrix} = \begin{bmatrix} 0.577 \angle 0^\circ \\ 0.577 \angle -120^\circ \\ 0.577 \angle 120^\circ \end{bmatrix}$$
(2.22)

The solution shows that all three system currents are of identical magnitude, and perfectly in phase with their respective voltages.

Load balancing and power factor correction will therefore be accomplished if the compensator can provide the required currents to the load.

Chapter 3

LOAD BALANCING AND POWER FACTOR CORRECTION USING SINUSOIDAL PWM

3.1 MATHEMATICAL ANALYSIS OF STATCOM

3.1.1 Sequence Components

The clearest method of analysing unbalanced currents and voltages in the system is to use superposition of sequence components. Figure 3.1 below shows the single line diagram of the STAT-COM system in terms of positive and negative sequence components. The STATCOM is modelled as a voltage source with both real and imaginary parts making up the positive and negative sequence components.

The source voltage is assumed to be balanced and set as the reference phase. Thus it contains only a positive sequence real part. Zero sequence is ommitted due to the assumed delta windings.



Figure 3.1: Single Line Diagram of STATCOM / Voltage Source Sequences

Using Ohms law and superposition, the sequence components of the output currents can be calculated in the standard non-rotated form as follows:

$$I_{1}RE = \frac{V_{C1}IM}{X_{L}} \quad I_{1}IM = \frac{V_{S1}RE - V_{C1}RE}{X_{L}} \quad I_{2}RE = \frac{V_{C2}IM}{X_{L}} \quad I_{2}IM = \frac{-V_{C2}RE}{X_{L}}$$
(3.1)

Breaking down the equations into these real and imaginary sequence components will prove to be necessary when analysing the control system.

3.1.2 DC Transients

One aspect which must be considered when using voltage control are the undesirable DC transients that occur in the output current. The output current is related to the integral of the voltage across the transformer leakage reactange. This results in a constant of integration whenever a change is made to the voltage.

$$i_{L}(t) = \frac{1}{L} \int [v_{C}(t) - v_{S}(t)] dt + c \qquad (3.2)$$

Figure 3.2 below illustrates the DC Transient in a worst-case scenario where the inductor voltage (STATCOM voltage minus system voltage) undergoes a 180° phase shift at a current maximum. Left alone this DC transient will follow an exponential decay depending on the damping within the circuit. It is preferable, however, to remove this DC much faster using controls



Figure 3.2: Worst Case DC Transient in STATCOM Current

3.1.3 Modulation of Output Voltage

The firing pulses to the GTO's are constructed using a reference sinusoid compared against a triangular wave. This technique is commonly known as sinusoidal pulse width modulation (SPWM) [1]. Figure 3.3 below shows the basic control diagram for a single phase SPWM system.

A voltage reference signal is constructed using three components. The first component is a sinusoid directly in phase with the source voltage to control the real current flow. The second component is a sinusoid in quadrature with the source voltage to control the reactive current flow. Lastly, a DC component may be necessary for removing DC transients in the output current.

This reference sinusoid is compared against a triangular wave. Whenever the reference sinusoid is greater than the triangular wave, the VSI is fired to switch a positive output. Vice-versa for a negative output. Figure 3.4 overleaf shows an example of these three components, the resulting reference sinusoid, and the output voltage produced from the compensator.



Figure 3.3: Control Diagram for Sinusoidal Pulse Width Modulation



Figure 3.4: Sinusoidal Pulse Width Modulation Signals

It can be seen that the fundamental component of the resulting output voltage (Vc) is equal to the reference sinusoid (*Ref*) multiplied by half of the VSI's capacitor voltage (VCap). The RMS relationship is given by:

$$\overrightarrow{Vc} = \overrightarrow{Ref} \cdot \frac{VCap}{2\sqrt{2}}$$
(3.3)

The peak-value of the reference sinusoid, not including the DC component, will be referred to as the "modulation index". The ratio of triangular wave frequency to reference sinusoid frequency will be referred to as the "modulation ratio".

3.2 CONTROL SYSTEM

The requirements of the control system are as follows:

- To satisfy a load-balancing solution, different real and reactive currents are required from each phase. Therefore, each GTO pair in the STATCOM must be fired differently.
- The capacitor voltage must be maintained at a constant value. This implies that the net real power flow to the circuit should only be the amount required to cover losses.
- DC transients must be damped as quickly as possible.

Inputs to the control system will be the measured load currents, measured compensator currents and measured capacitor voltage.

Outputs from the control system will be three different reference sinusoids, used for the pulse width modulation on each phase of the STATCOM.

This general format is shown below in figure 3.5. For ease of understanding, the control system will be broken into subections and explained separately.



Figure 3.5: General Format of Control System.

3.2.1 Reactive Current Control

Reactive Currents must be controlled individually on each phase to achieve load-balancing. As described in section 3.1.3, the reactive current output of the compensator can be controlled by adjusting the magnitudes of the direct component of the reference sinusoids.

The controller subsection which controls the reactive currents has the load currents and compensator currents as inputs, with three scalar values representing the direct component magnitude of the final reference sinusoids as the outputs.



Figure 3.6: Control of Reactive Currents.

The first task that this controller subsystem must perform is to convert the input sinusoids into phasor quantities. The realtime current waveforms are not useful to the controller. The controller needs these inputs to be expressed as phasors, in real and reactive parts.

This can be done using an online Fast-Fourier-Transform (FFT) component. The FFT continously buffers a 'snapshot' of the last cycle of each waveform. Fourier analysis is continously performed on these snapshots to extract the fundamental harmonic. This analysis provides the magnitudes of the real and imaginary (reactive) parts of the fundamental phasor quantity, as scalar values. The process is fast, with an output delay of only one cycle, and a meaningful output is usually available within half a cycle.

Some additional logic in the FFT component can also provide the real and imaginary parts of the

positive and negative sequence phasors as scalar values.



A more detailed control diagram can be seen below in Figure 3.7

Figure 3.7: Detailed Control of Reactive Currents.

Measured load currents are first passed through an FFT to calculate the real and imaginary parts of the sequence components. These are multiplied by the reactive current solution matrix (2.12) to provide the reactive current references. These three output values indicate the magnitudes of the compensator reactive currents which are required to balance the load.

Measured compensator currents are also passed through an FFT to extract the fundamental phasor, from which the magnitude of the reactive currents being produced by the compensator can be found. Error signals are generated by subtracting these measured reactive currents from the reference signals. When steady state is reached, these error signals will be equal to zero.

The error signals are fed into identical PI controllers, which produce the preliminary magnitudes of the direct in-phase components of the preliminary reference sinusoids used in PWM.

Note that an alternative definition for generation of the error signals, shown below, substitutes the

current sequence components in place of the reactive currents. This is useful when analysing the controls.



Figure 3.8: Alternative Definition of Error Signals.

3.2.2 Real Current Control

Two possibilities arise when formulating the real current control system. The first option is to explicitly control all three real currents in a similar manner to the method used in 3.2.1. This method would however require an additional branch to maintain capacitor charge. Fig 3.9 shows this first possibility:



Figure 3.9: Possible Solution for Control of Real Currents

This is not a preferred method as there are two levels of PI control - the output from the capacitor voltage PI controller is eventually fed to the input of the three real-current PI controllers. This makes for poor control as the two controllers fight each other during transients.

The alternative to this option, is to make use of implicit control. A zero-sequence filter on the reference sinusoids will provide the required quadrature components for load-balancing purposes while capacitor voltage feedback with PI control provides the quadrature component required to maintain capacitor charge. This will be discussed further in section 3.2.5.

Preliminary simulations showed that explicit control was extremely difficult to stabilise and had very poor dynamic performance. Implicit control, shown to work well, was therefore chosen as the control system for this research.





Figure 3.10: Capacitor Voltage / Real Current Control Subsystem.

The measured capacitor voltage is filtered through an FFT which extracts the DC component of the voltage waveform. This ensures that the 120Hz ripple due to negative sequence and switching harmonics do not interfere with the controller outputs.
3.2.3 DC Transient Control

As mentioned in 2.1.2, DC transients can appear in the STATCOM current output.

These are controlled by adding opposing DC components to the reference sinusoids.

Firstly, the compensator currents are fed through an FFT to extract the DC component from the waveforms. These DC components are multiplied by -1, to ensure negative feedback. The feedback signals are then put through a PI controller before being added to the reference sinusoids.

Figure 3.11 below demonstrates this.



Figure 3.11: DC Transient Removal Subsystem.

3.2.4 Construction of the Reference Sinusoids

So far, three control subsystems have been described. These provide the magnitudes of the desired direct, quadrature and DC components of the reference sinusoids. The next step is to construct the realtime reference sinusoids from these scalar values.

The output sinusoids must be able to stay synchronised with the source-voltage and quickly keep up with external phase-shifts or frequency variations. A phase-locked-loop is used [7] to find the angular displacements (θ_a , θ_b , θ_c) of the source voltage, from which the reference sinusoids can be constructed. Figure 3.5 overleaf shows the outputs of this phase-locked-loop.



Figure 3.12: Output Signals from Phase Locked Loop

Taking the sine and cosine of these angular displacements provides realtime sinusoids of magnitude 1, which are directly in phase or in quadrature with each phase voltage.

These direct and quadrature sinusoids are multiplied by the outputs from the real and reactive control subsystems, then summated with the DC output of the DC control subsystem to provide the preliminary reference sinusoids.

This can be seen in figure 3.13 overleaf.



Figure 3.13: Construction of Reference Sinusoids.

Expressions for these sinusoids, assuming Va,Vb,Vc are at 0,-120°,+120°, are as follows:

$$RefO_{A}(t) = da \cdot \sin(\omega t) + qabc \cdot \cos(\omega t) + DCa$$
(3.4)

$$RefO_B(t) = db \cdot \sin(\omega t - 120^\circ) + qabc \cdot \cos(\omega t - 120^\circ) + DCb$$
(3.5)

$$RefO_C(t) = dc \cdot \sin(\omega t + 120^\circ) + qabc \cdot \cos(\omega t + 120^\circ) + DCc$$
(3.6)

During steady-state, when all DC transients have been eliminated, the standard form phasor quantities can be found:

$$RefO_A = da + j \cdot qabc \tag{3.7}$$

$$\overrightarrow{RefO}_B = \alpha^2 (db + j \cdot qabc) = \left[-\frac{1}{2}db + \frac{\sqrt{3}}{2}qabc \right] + j \left[-\frac{1}{2}qabc - \frac{\sqrt{3}}{2}db \right]$$
(3.8)

$$\overrightarrow{RefO_C} = \alpha(dc + j \cdot qabc) = \left[-\frac{1}{2}dc - \frac{\sqrt{3}}{2}qabc\right] + j\left[-\frac{1}{2}qabc + \frac{\sqrt{3}}{2}dc\right]$$
(3.9)

3.2.5 Zero Sequence Filter

The control solution thus far will provide the necessary reactive currents for partial load balancing and the required amount of balanced real current for maintaining the capacitor voltage. However, it does not provide the required different real currents to perform full load balancing.

The preliminary reference sinusoids can be manipulated via a zero sequence filter in order to provide these required real currents.

This works by taking advantage of an interesting mathematical property of a three wire system. A three wire system is not capable of containing any zero sequence currents. By ordering only the reactive current parts of a load balancing solution, the system is ordering currents that include zero sequence - a request which is impossible to implement. The restriction of no zero-sequence will only be satisfied if the real parts of the load balancing solution are also included.

In other words, a three wire system may not contain one half of a current balancing solution without the other. The delta winding will force a full solution if only the real or reactive half is ordered.

However, allowing the delta winding in the power system to do this is not the most efficient solution. Instead, a forcing action similar to that of the delta winding can be applied to the three reference sinusoids in the control system with the use of a zero sequence filter.

The three preliminary reference sinusoids (RefO(t)) are summated to find the zero sequence component. This is then divided by three and subtracted from each reference sinusoid. The result being that the outputs (Ref(t)) now contain no zero sequence This filtering procedure is accomplished with the use of the following matrix:

$$\begin{bmatrix} Ref_A(t) \\ Ref_B(t) \\ Ref_C(t) \end{bmatrix} = \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ -\frac{1}{3} & \frac{2}{3} & -\frac{1}{3} \\ -\frac{1}{3} & -\frac{1}{3} & \frac{2}{3} \end{bmatrix} \begin{bmatrix} RefO_A(t) \\ RefO_B(t) \\ RefO_C(t) \end{bmatrix}$$
(3.10)

The resulting output sinusoids now provide the required real currents necessary for load-balancing. The net real current being ordered still matches that required for capacitor voltage control.

3.2.6 Mathematical Proof of Control System

An extended control block diagram is shown overleaf for this analysis.

Steady state is assumed so DC components have been ignored.

The first step is to begin with the phasor expressions of the preliminary reference sinusoids, given in section 3.2.4:.

$$\overline{RefO_A} = da + j \cdot qabc \tag{3.11}$$

$$\overrightarrow{RefO_B} = \alpha^2 (db + j \cdot qabc) = \left[-\frac{1}{2}db + \frac{\sqrt{3}}{2}qabc \right] + j \left[-\frac{1}{2}qabc - \frac{\sqrt{3}}{2}db \right]$$
(3.12)

$$\overrightarrow{RefO_C} = \alpha(dc + j \cdot qabc) = \left[-\frac{1}{2}dc - \frac{\sqrt{3}}{2}qabc\right] + j\left[-\frac{1}{2}qabc + \frac{\sqrt{3}}{2}dc\right]$$
(3.13)





These reference phasors can be expressed as real and imaginary parts in matrix form as follows:

$$\begin{bmatrix} RefO_A RE\\ RefO_A IM\\ RefO_B RE\\ RefO_B IM\\ RefO_C RE\\ RefO_C IM \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0\\ 0 & 0 & 0 & 1\\ 0 & -\frac{1}{2} & 0 & \frac{\sqrt{3}}{2}\\ 0 & \frac{-\sqrt{3}}{2} & 0 & -\frac{1}{2}\\ 0 & 0 & -\frac{1}{2} & -\frac{\sqrt{3}}{2}\\ 0 & 0 & -\frac{1}{2} & -\frac{\sqrt{3}}{2}\\ 0 & 0 & \frac{\sqrt{3}}{2} & -\frac{1}{2} \end{bmatrix} \begin{bmatrix} da\\ db\\ dc\\ gabc \end{bmatrix}$$
(3.14)

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The preliminary reference sinusoids are then passed through the zero-sequence filter matrix. Note that real and imaginary parts are now being expressed as scalar values in seperate rows, so the zero sequence filtering matrix is somewhat different from the form previously shown.

$$\begin{bmatrix} Ref_{A}RE\\ Ref_{B}IM\\ Ref_{B}RE\\ Ref_{B}IM\\ Ref_{C}RE\\ Ref_{C}IM \end{bmatrix} = \begin{bmatrix} \frac{2}{3} & 0 & -\frac{1}{3} & 0 & -\frac{1}{3} & 0\\ 0 & \frac{2}{3} & 0 & -\frac{1}{3} & 0 & -\frac{1}{3} & 0\\ -\frac{1}{3} & 0 & \frac{2}{3} & 0 & -\frac{1}{3} & 0\\ 0 & -\frac{1}{3} & 0 & \frac{2}{3} & 0 & -\frac{1}{3} & 0\\ 0 & -\frac{1}{3} & 0 & \frac{2}{3} & 0 & -\frac{1}{3} & 0\\ -\frac{1}{3} & 0 & -\frac{1}{3} & 0 & \frac{2}{3} & 0\\ 0 & -\frac{1}{3} & 0 & -\frac{1}{3} & 0 & \frac{2}{3} & 0\\ 0 & -\frac{1}{3} & 0 & -\frac{1}{3} & 0 & \frac{2}{3} \end{bmatrix} \begin{bmatrix} RefO_{A}RE\\ RefO_{A}IM\\ RefO_{B}RE\\ RefO_{B}IM\\ RefO_{C}RE\\ RefO_{C}IM \end{bmatrix}$$
(3.15)

Using formula (3.3) it is now possible to calculate the real and imaginary parts of the compensator output voltage.

$$\begin{bmatrix} Vc_{A}RE \\ Vc_{A}IM \\ Vc_{B}RE \\ Vc_{B}IM \\ Vc_{C}RE \\ Vc_{C}IM \end{bmatrix} = \frac{VCap}{2\sqrt{2}} \begin{bmatrix} Ref_{A}RE \\ Ref_{B}IM \\ Ref_{B}RE \\ Ref_{B}IM \\ Ref_{C}RE \\ Ref_{C}IM \end{bmatrix}$$
(3.16)

For load-balancing analysis, this is best expressed as sequence components. Multiplication by a sequence transformation matrix yields the desired result:

~

$$\begin{bmatrix} Vc_{1}RE \\ Vc_{1}IM \\ Vc_{2}RE \\ Vc_{2}IM \\ Vc_{0}RE \\ Vc_{0}IM \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 0 & -\frac{1}{2} & -\frac{\sqrt{3}}{2} & -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ 0 & 1 & \frac{\sqrt{3}}{2} & -\frac{1}{2} & -\frac{\sqrt{3}}{2} & -\frac{1}{2} \\ 1 & 0 & -\frac{1}{2} & \frac{\sqrt{3}}{2} & -\frac{1}{2} & -\frac{\sqrt{3}}{2} \\ 0 & 1 & -\frac{\sqrt{3}}{2} & -\frac{1}{2} & -\frac{\sqrt{3}}{2} \\ 0 & 1 & -\frac{\sqrt{3}}{2} & -\frac{1}{2} & \frac{\sqrt{3}}{2} & -\frac{1}{2} \\ 1 & 0 & 1 & 0 & 1 \\ 0 & 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} Vc_{A}RE \\ Vc_{A}IM \\ Vc_{B}RE \\ Vc_{B}IM \\ Vc_{C}RE \\ Vc_{C}IM \end{bmatrix}$$
(3.17)

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Multiplication and simplification of steps (3.14) to (3.17) provides the STATCOM voltage sequence components in terms of the PI controller outputs:

As expected, due to the zero-sequence filter, the compensator output contains no zero sequence. The bottom two rows of the above matrix can therefore be dropped. The compensator voltage sequence components can also be substituted with current sequence components formulae, (3.1).

-

$$\begin{bmatrix} Vs_{1RE} - X_{L} \cdot I_{1}IM \\ X_{L} \cdot I_{1}RE \\ -X_{L} \cdot I_{2}IM \\ X_{L} \cdot I_{2}RE \end{bmatrix} = \frac{VCap}{6\sqrt{2}} \begin{bmatrix} 1 & 1 & 1 & 0 \\ 0 & 0 & 0 & 3 \\ 1 & -\frac{1}{2} & -\frac{1}{2} & 0 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} & 0 \end{bmatrix} \begin{bmatrix} da \\ db \\ dc \\ qabc \end{bmatrix}$$
(3.19)

-

This solution can be readily inverted to prove that a specific combination of controller outputs

exists for any given combination of required output currents:

$$\begin{bmatrix} da \\ db \\ dc \\ qabc \end{bmatrix} = \frac{2\sqrt{2}}{VCap} \begin{bmatrix} 1 & 0 & 2 & 0 \\ 1 & 0 & -1 & \sqrt{3} \\ 1 & 0 & -1 & -\sqrt{3} \\ 0 & 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} Vs_1RE - X_L \cdot I_1IM \\ X_L \cdot I_1RE \\ -X_L \cdot I_2IM \\ X_L \cdot I_2RE \end{bmatrix}$$
(3.20)

Cross-checking this solution against Figure 3.7 verifies that this control system will converge to the desired outputs. The error signals that are fed to the da, db and dc PI controllers contain the same variables that outputs da, db and dc directly control, and they are all of opposing sign.

Positive sequence real current is controlled separately by qabc, which in turn has no effect on positive sequence imaginary current or negative sequence current. Variable qabc is calculated from PI control of the DC capacitor voltage error.

It is interesting to note that the zero-sequence filter is a singular matrix and cannot be directly inverted. This means that given an output from the zero sequence filter is it impossible to reconstruct the input, as any arbitrary amount of zero sequence may have existed before the filter.

However, by restricting the input variables to four scalar values (da, db, dc and qabc) the degrees of freedom for the input are reduced to the same number of degrees of freedom that exist in the output (real and imaginary parts of positive and negative sequence). This allows direct inversion of the zero-sequence filter to be bypassed, as shown above, and a specific input solution to be found.

3.3 SWITCHING

The number of switchings per-cycle is a constant predictable value with the voltage controlled PWM. This number is determined by the ratio of triangle-wave modulation frequency to system frequency, or modulation ratio.

Number of On or Off Switchings per Valve per Cycle
$$=$$
 $\frac{\text{Triangular Wave Frequency}}{\text{System Frequency}}$ (3.21)

The shortest switching time will always occur at the peaks of the reference sinusoid. The closer the modulation index is to one, the shorter this switching time will be, assuming over-modulation does not occur. Figure 3.9 below demonstrates this property.

Shortest On/Off Switching Period
$$\approx \frac{1 - \text{Modulation Index}}{\text{Triangular Wave Frequency}}$$
 (3.22)



Figure 3.15: Effect of Modulation Index on Switching Times.

The modulation index can be reduced by increasing the capacitor voltage, thereby increasing the minimum switching time.

Modulation Index
$$\propto \frac{1}{\text{Capacitor Voltage}}$$
 Under Steady-State (3.23)
Conditions

3.4 HARMONICS

The characteristic current harmonics produced from this type of voltage-controlled PWM are predictable [1]. The order of the harmonics are odd numbers clustered around multiples of the modulation ratio.

Higher modulation ratio generally reduces the total harmonic distortion, but this must be traded off against switching losses and limitations of the valves.

Some non-characteristic harmonics may appear during transients or due to imperfections and delays in the control circuitry. This is discussed further in chapter 6.

Chapter 4

LOAD BALANCING AND POWER FACTOR CORRECTION USING CURRENT REFERENCE PWM

Current reference PWM provides an alternative method of modulation which has different control properties and responses to those of sinusoidal PWM. With voltage-controlled sinusoidal PWM, the output currents are controlled indirectly through modulation of the output voltage because the inverter acts as a voltage source. In current reference PWM, however, the inverter is controlled as a current source and the output currents are manipulated directly.

4.1 CURRENT ANALYSIS OF STATCOM

4.1.1 Real and Reactive Current Flows

Figure 4.1 below shows the current source model of the current-controlled STATCOM.



Figure 4.1: Single Phase of STATCOM / Current Source

Real and imaginary parts of the compensator sequence currents are simply determined by the current source.

 $IL_1RE = Icomp_1RE \quad IL_1IM = Icomp_1IM \quad IL_2RE = Icomp_2RE \quad IL_2IM = Icomp_2IM$ (4.1)

4.1.2 Dynamic Performance

A STATCOM operated as a current source should have negligible DC transients.

With an ideal control system, the current-controlled STATCOM will have ideal dynamic performance. It will be shown however, that control limitations and measurement delays make a significant difference.

4.2 CONTROL SYSTEM

Firing of the VSI is determined using hysteresis-based current control. [1] Figure 4.2 below shows the block diagram of this control method:



Figure 4.2: Block-Diagram of Control for Voltage PWM

If the measured current is below the lower hysteresis limit of the reference current, the VSI will switch high, causing the current to rise. When it eventually hits the upper hysteresis limit it will switch low again. Figure 4.3 shows how this generates the required PWM current.



Figure 4.3: Example of current-hysteresis PWM.

4.2.1 Generation of the Reference Currents

The unbalanced load will contain positive and negative sequences with real and imaginary parts.

To balance the load, the compensator will have to negate the negative sequence components. To provide additional power factor correction, it will also have to negate the positive sequence imaginary components. The net system current will then be identical to only the positive sequence real component of the load.

In practice, some additional positive sequence real current will be needed for control of the capacitor voltage. The order for this current will be provided by a PI controller, similar to that used in the voltage-controlled STATCOM.

Thus it is possible to produce three real-time reference system-currents using reverse sequence transformation of the real positive sequence load current added to the required charging current. The reverse sequence transformation will require inputs from the phase-locked-loop that tracks the system voltage, to ensure that the outputs are of correct phase and frequency.

From these reference system-currents, the measured load currents are subtracted to reveal the required real-time reference load-balancer currents.

If power-factor correction is not required, the positive sequence imaginary component can be added to the reverse transformation. By leaving the reactive currents in the reference system-currents, the load balancer will not act to remove them.

Figure 4.4 overleaf shows the control-diagram of the reference current generator.



Figure 4.4: Generation of reference currents for current controlled PWM.

This method has the additional benefit of allowing the load-balancer to also filter lower order harmonics from the load which will be described further in sections 4.4.1 and 6.3.5.

This is similar to previous research [6] where a CRPWM STATCOM was used for load balancing and active filtering.

4.3 SWITCHING

The exact number of switchings per valve per cycle is impractical to predict using current hysteresis PWM, as it is significantly load dependent.

Using a larger hysteresis band results in longer switching times and therefore less switching per cycle.

Trial and observation was used to find a hystersis band size that gave the approximate number of desired switchings per cycle. More complex methods may be used to better regulate the switching frequency [8] but are beyond the scope of this thesis.

4.4 HARMONICS

The CRPWM method is capable of actively filtering harmonics which are less than half the switching frequency. However, higher order harmonics will be introduced due to the PWM switching.

4.4.1 Active Filtering

Elimination of lower-order harmonics from the load currents is an additional useful property which can only be done with current-controlled PWM.

The control method described in 4.2 will compensate a current waveform of almost any shape to provide a closely sinusoidal output.

Figure 4.5 below shows a single phase square-wave load-current and the resulting reference and output currents from a single-phase compensator. It can be seen that the output current is very close to the real fundamental component of the load current.



Figure 4.5: Harmonic Elimination using Current Controlled PWM

Note the higher-order harmonics introduced due to the nature of PWM.

In a three-phase case the compensator current would be a slightly different shape as the system current would be phase-shifted by 30° .

4.4.2 PWM Generated Harmonics

It is not practical to predict exactly the high order harmonics generated from current-controlled PWM. They will comprise of many assorted frequencies and will not be exact multiples of the system frequency. However, most of them will be clustered below twice the average switching frequency.

A smaller hysteresis band will therefore result in a higher switching frequency with higher order harmonics of smaller magnitudes.

Chapter 5

MODELLING OF THE SYSTEM IN PSCAD/EMTDC

So far the theory for a load balancing STATCOM has been developed. Two different methods of pulse width modulation have been designed and analysed.

The next half of this research is the simulation of these designs on the PSCAD/EMTDC simulation software. The designs will be evaluated in terms of steady-state performance, dynamic response and harmonic analysis.

Firstly, the parameters of the system must be selected - what power ratings will be simulated ? Voltage and current ratings ? How big should the components be ?

It was decided that the load balancing model should be required to balance a delta connected inductive load, where each branch can draw up to 10MW, 8MVAR on a 10KV line to line bus.

Secondly, a number of new simulation components will need to be programmed in order to implement the designed systems.

5.1 SELECTION OF SYSTEM PARAMETERS

5.1.1 Leakage Reactance

Conventional transformers are designed with around 5 - 10% leakage reactance. HVDC and FACTS transformers however, are usually designed with a higher leakage reactance of 15 - 20%. [9] The higher leakage reactance in these cases is used to reduce the system fault currents should a short appear across the valves.

Given that the unit load is 10MW p.u. on a 10kV L-L bus, leakage reactance was chosen to be 15%, or 1.5Ω

5.1.2 Capacitor Voltage

Selection of the capacitor voltage and leakage reactance are co-dependent. In this case, a specific

leakage reactance has been chosen and the required capacitor voltage must be calculated from this. It is possible to choose parameters in the reverse order, or iterate between selections as required.

For this analysis, it is only necessary to look at a single phase, phase A being the least complex in the mathematical sense. The basic relationship between leakage reactance (X_L) , source voltage (Vlg), compensator voltage (V_Ca) and compensator current $(I_Ca_{RE}+jI_Ca_{IM})$ is as follows:

$$\overrightarrow{V_C a} = [Vlg - I_C a_{IM} \cdot X_L] + j[I_C a_{RE} \cdot X_L]$$
(5.1)

To find out what the maximum compensator voltage must be, the largest negative value of $I_C a_{IM}$ must be found. This is done using the formula derived in Appendix C:

$$\overrightarrow{I_Ca} = \frac{[Pab+2Pbc-Pca-\sqrt{3}(Qab-Qca)]+j[\sqrt{3}(Pab-Pca)-3(Qab+Qca)]}{6Vlg}$$
(5.2)

It can be seen by inspection that maximum real and reactive loads on phases AB and CA will provide the largest negative reactive compensator current. Substituting 10MW for Pab and Pca, 8MVAR for Qab, Qca, the numerical solution is found:

$$\overrightarrow{I_Ca}(Max) = -0.578 - j1.387 \quad kA$$
 (5.3)

This is substituted into the above voltage formula (5.1) along with Vlg=5.77 kV, X_L =1.5 Ω to find the maximum required compensator voltage:

$$\overrightarrow{V_C a} = 7.90 \angle -6.3^\circ \quad kV \tag{5.4}$$

To generate this maximum voltage, the sinusoidal reference wave would be magnitude 1 at -6.3° . Choosing the maximum reference sinusoid to be magnitude 1 allows minimum capacitor voltage without any overmodulation.

Using the relationship between compensator voltage, reference wave and capacitor voltage, the

minimum required capacitor voltage can then be found:

$$VCap_{min} = \frac{2\sqrt{2} \cdot V_C a_{max}}{\overrightarrow{Refa_{max}}} \cong 22.5 \quad kV \tag{5.5}$$

5.1.3 Capacitor Size

The main factor for determining capacitor size is the 120Hz energy oscillations caused by the negative sequence compensation currents. These oscillations cause a ripple on the capacitor voltage, and the capacitor must be of sufficient size that the ripples do not adversely effect the performance.

The formula for real-time power of the compensator, derived in Appendix A, is a as follows:

$$Pa(t) + Pb(t) + Pc(t) = 3V_{LG} \cdot [I_{1re} - I_{2re}\cos(2\omega t) + I_{2im}\sin(2\omega t)]$$
(5.6)

The oscillating component, which the compensator must supply in order to perform load balancing, is therefore:

$$Posc(t) = 3V_{LG} \cdot |I_2| \cdot \cos(2\omega t + \phi)$$
(5.7)

Note that only the size and frequency of this oscillation are important, so ' ϕ ' will be omitted from further calculations.

The formula for energy stored (W) in a capacitor (size C) at a given voltage (V) is also equal to the time-integral of the real power.

$$W(t) = \frac{C \cdot V(t)^2}{2} = \int P(t) dt \qquad (5.8)$$

This expression is then rearranged in terms of V(t), with the oscillating power expression substituted for P(t) and then integrated:

$$V(t) = \sqrt{\frac{2}{C}} \int Posc(t) dt = \sqrt{\frac{3V_{LG} \cdot |I_2|}{\omega \cdot C}} \sin(2\omega t) + k$$
(5.9)

It can be seen that 'k', the constant of integration, is very close to the nominal capacitor voltage, squared.

$$V(t) = \sqrt{\frac{3V_{LG} \cdot |I_2|}{\omega \cdot C}} \sin(2\omega t) + (V_{nom})^2 = V_{nom} \sqrt{\frac{3V_{LG} \cdot |I_2|}{\omega \cdot C \cdot (V_{nom})^2}} \sin(2\omega t) + 1 \quad (5.10)$$

The following mathematical approximation (5.11) can be used to simplify (5.10):

$$\sqrt{\delta+1} \cong 1 + \frac{\delta}{2}$$
 Where $\delta << 1$ (5.11)

$$V(t) \cong V_{nom} \sqrt{\frac{3V_{LG} \cdot |I_2|}{\omega \cdot C \cdot (V_{nom})^2}} \sin(2\omega t) + 1 \cong V_{nom} + \frac{3V_{LG} \cdot |I_2|}{2\omega \cdot C \cdot V_{nom}} \sin(2\omega t)$$
(5.12)

Now, given a maximum allowable 120Hz, ripple amplitude (*RipMax*) it is possible to calculate a minimum required capacitor size:

$$C = \frac{3V_{LG} \cdot |I_2|}{2\omega \cdot V_{nom} \cdot RipMax}$$
(5.13)

Using the negative sequence formula derived in Appendix C, the maximum negative sequence current magnitude is calculated to be 776 A.

Nominal voltage has already been selected at 22.5kV.

It now becomes a design trade-off between capacitor size and allowable ripple. Capacitor cost rises dramatically as size increases. Further studies will be required to determine exactly what levels of capacitor ripple have significant effect compensator performance and current harmonics.

As a basic estimate, it was chosen that the 120Hz ripple amplitude be no more than 1% of the nominal voltage. This equates to a Ripmax of 2.25 kV.

Substitution of the above numerical values into the capacitance formula reveals the desired capacitor size:

$$C \cong 3500 \mu F$$

5.1.4 Complete System



Figure 5.1 below shows the complete model for the load, STATCOM and source voltage.

Figure 5.1: System Parameters Used for Simulation

The schematic used in PSCAD/EMTDC can be seen overleaf in Figure 5.2. See section 5.3 for the controls.



Figure 5.2: PSCAD Schematic of Main System

5.2 NEW COMPONENTS

Several new simulation components must be programmed in order to implement the designed control system. These components are programmed using FORTRAN.

5.2.1 Interpolated Switching Delay

The PSCAD / EMTDC simulation software runs using discrete time-steps. When high-frequency PWM is used, these time-steps can cause significant errors in the simulation.

Small timing errors on the firing signals due to the discretization of time can compound themselves into significant control problems and inaccurate output results. This is likely to be a problem in a real system if digital control with a low clocking frequency is used.

Much of these errors can be overcome using interpolated firing signals. The firing signals change only at discrete time-steps, but changes are accompanied with an interpolation signal which reveals the exact time at which the transition occurred. [10]





Simulation Variables Sampled at Discrete Time-Steps, Δ

Figure 5.3: Interpolation of Firing Signal from SPWM

The valve components used in the main circuit are already programmed to take interpolated firing signals, so no additional changes are required here. However, a delay is required between switching signals, and a new component which provides an interpolated delay must be programmed.

Real values do not switch off instanteneously, there is a natural delay that occurs due to charge removal in the semiconductor material [1]. It is important that value pairs be given a short delay period between switching so that they do not mistakenly short the capacitor.

This delay period must take into account the interpolation signals described in 5.2. A new component was designed to produce a switch-on delay.



Figure 5.4: Operation of New Switch-Delay Component

Note that the interpolation is not shown in the above figure.

Length of the delay must be greater than or equal to one time step.

5.2.2 Power to Resistance / Inductance Calculators

The delta-connected load used in this simulation must be variable in order to test a full range of real and reactive load currents. This is acheived using variable resistor/inductor components. The required values of these variable components are calculated from real and reactive power orders

specified by the user. The calculations are performed by two new components 'P2R' and 'Q2L'.

Variable parameters within the blocks are the base MVA and base voltage. System frequency is also a variable parameter for the 'Q2L' block. The required MW / MVAR is specified as an input. Fig 5.3 shows how this is used to create the variable load.



Figure 5.5: EMTDC / PSCAD Simulation of Variable Load

Note that additional resistance has been added in series with the inductor to damp DC transients. This resistance is approximately 10% of the inductor reactance, and has only a small effect on the total real and reactive power.

The inductor and associated resistor have hard-limits set to them, as a zero MVAR request will result in an excessively large inductor, causing large DC transients.

5.2.3 3x3 Computation Matrix

A 3x3 computation matrix has been designed, where all nine elements can be entered by the user.

Figure 5.4 below shows how this new component allows the simulator to calculate the required reactive currents, using matrix (2.3). Power-factor correction is made optional using a switch. This switch output is multiplied with the positive sequence imaginary component, enabling it to

be to set it to zero if power-factor correction is not required.



Figure 5.6: 3x3 Computation Matrix Used to Calculate Reactive Current Orders

This same computation matrix component is also used as the zero sequence filter for the reference sinusoids.

5.2.4 Polar to Rectangular Transformation

Many of the vector measurements made in PSCAD/EMTDC are in polar co-ordinates. The designed control system requires rectangular real and imaginary co-ordinates. A simple polar to rectangular block was programmed for this purpose.



Figure 5.7: Polar to Rectangular Transformation Block

5.3 Complete Control System

Figures 5.8 to 5.10 on the following three pages show the PSCAD/EMTDC implementation of the entire control system.

Part one shows the Fast Fourier Transform components used for measuring system variables. Note the additional FFT for measurement of the phases of the source voltage. Subtraction of these values from all other phase measurements allows calibration of the phasors in rotated form.

Part two contains the real, reactive and DC current controller subsystems, construction of the reference sinusoids, zero sequence filter and triangular wave generator.



Part three contains the PWM comparitor and switching delay components.

Figure 5.8: PSCAD/EMTDC Implementation of Controls, Part 1 - FFT Measurements



Figure 5.9: PSCAD/EMTDC Implementation of Controls, Part 2 - Main



Figure 5.10: PSCAD/EMTDC Implementation of Controls, Part 3 - PWM Firing

Chapter 6 PSCAD/EMTDC SIMULATION RESULTS

6.1 SINUSOIDAL PULSE WIDTH MODULATION

6.1.1 Optimal Control Settings

The voltage controlled PWM method requires seven Proportional-Integral (PI) controllers which can be grouped into three sets. The first set of three are from the DC transient control subsystem. The second set of three are from the reactive current control subsystem, and last single PI controller is from the capacitor voltage control subsystem.

The proportional gain and integral time-constant of each of these controllers were set by manual adjustment. System outputs were observed and the gains adjusted accordingly until a reasonable response was found.

Gains were then further optimised using the multiple-run facility in EMTDC. The multiple-run facility automatically performs a number of simulations over a range of input variables and records the final output variables. The optimal input variables can then be found.

Proportional gains and integral time constants were specified as the input variables. Integral squared DC errors, negative sequence errors and capacitor voltage errors were specified as outputs, when step changes were applied to the system.

This allowed the control variables to be optimised to the best all-round values. The process was iterated a number of times, as all of the PI controllers are somewhat coupled to each other. No strict mathematical procedure was followed. Result observation and human intuition played a large part of this optimisation.

Figure 6.3 overleaf shows the results from optimisation of the DC removal controls. It was noticed that by using high gains on the reactive current controls, less gains were required for DC removal.



Figure 6.1: Contour Plots of DC Errors Used to Find Optimal PI Gains

It can be seen that for these cases even zero gains provided acceptable control of the DC transients. However, for compensations currents with higher reactive content and less imbalance, the higher gains were required.

After a number of iterations, it was found that best response for all three controllers was achieved by forcing the strongest control from the reactive current controller. The gains for DC transient control and capacitor voltage control were then lowered to stop the controllers fighting.



Figure 6.2: Contour Plots of Negative Sequence Errors Used to Find Optimal PI Gains

Finally, the capacitor voltage control was optimised. For this control, steady-state error of the capacitor voltage was not as important. Overdamped control was preferred to underdamped control because oscillations on the capacitor voltage caused problems with the other two control systems.



Figure 6.3: Contour Plots of Capacitor Voltage Errors Used to Find Optimal PI Gains

6.1.2 Simulation Outputs

In a typical power system PWM application, switching frequency will often be as high as 2 - 5 KHz. For rapid simulation however, modulation ratio was chosen to be slightly lower, at 21 times the system frequency, or 1260Hz. Switching delay was equal to one simulation time-step, which was 5 microseconds.

Shown below is a step change in the load from no-load to 10MW, 8MVAR on phase BC:



Figure 6.4: Simulation Outputs, Step Change from no-load to 10MW, 8 MVAR phase BC

It can be seen that 90% of the negative sequence is removed and power factor correction is achieved within 2.5 cycles. Steady-state is achieved within 4 cycles. Note the introduced 120Hz ripple on the capacitor due to the negative sequence power fluctuation. The magnitude of this ripple is very close to that designed for in 5.1.3.

Shown below is a step-change from 10 MW, 8 MVAR phase BC to 10 MW, 8 MVAR on phased AB and CA. Phase BC contains no load.



Figure 6.5: Simulation Outputs, Step Change from 10 MW, 8 MVAR phase BC to 10 MW, 8 MVAR on phases AB and CA.

Again, 90% of the negative sequence is removed and power factor correction is achieved within
A third step-change from 10MW, 8MVAR on phases AB and CA to no-load is shown below.



Figure 6.6: Simulation Outputs, Step Change from 10MW, 8MVAR on phases AB and CA to no-load.

Compensator currents are reduced to 10% of their initial magnitudes within 2.5 cycles. Steady state is achieved within 4 cycles. In a real system, the controls could be modified to simply block all valves when zero currents are required.

6.1.3 Harmonic Analysis

Figure 6.9 below shows the fourier analysis of the total system currents which have been balanced. It can be seen that the 19th, 21st, 23rd, 41st and 43rd harmonics are the most significant. Some third harmonic is also present. The delta winding does not completely eliminate the thirdharmonic, as the harmonics are not equally balanced between all three phases.



Figure 6.7: Fourier Analysis of Balanced System Currents

6.1.4 Effects of Switching Delay

As described in section 5.3.1, a delay is required between valve switchings to avoid short-circuit conditions. If the delay becomes significantly large, the output of the PWM circuit will be affected. The simulation showed that increasing the switching delay affected the current wave-shape. Most notable was the increase in the 3rd harmonic component. Shown below is the fourier analysis of system currents where the switching delay has been increased from 15 up to 35 uS.



Figure 6.8: Fourier Analysis of Balanced System Currents with Switching Delay



Figure 6.9: Fourier Analysis of Balanced System Currents with Switching Delay



Figure 6.10: Distorted Current Waveforms due to Switching Delay

The introduced third harmonic component is not evenly distributed between the three phases. The delta winding will only pass unbalanced third harmonics.

The effect of the switching delay also depends on the modulation frequency. If the modulation frequency is higher, the switching delay will have more effect.

Shown below is the output waveform when the modulation frequency is increased to 33 times the fundamental, with the 35uS switching delay.



Figure 6.11: Fourier Analysis of Balanced System Currents with Switching Delay



Figure 6.12: Distorted Current Waveforms due to Switching Delay

It can be seen that increasing the modulation frequency from 21 to 33 times increases the negative sequence third harmonic component from 8% to 11% when a switching delay of 35uS is present. Higher order harmonics are reduced due to higher switching frequency.

The reverse is true for a lower switching frequency. Less lower order harmonics are induced due

to switching delay, but more PWM harmonics will be present.

Shown below is the effect of reducing modulation ratio to 13 times the fundamental, with the 35uS switching delay.



Figure 6.13: Fourier Analysis of Balanced System Currents with Switching Delay



Figure 6.14: Distorted Current Waveforms due to Switching Delay

It can be seen that reducing the modulation ratio from 21 to 13 reduces the negative sequence third harmonic component from 8% to 5% when a switching delay of 35uS is present. Higher order harmonics are increased due to lower switching frequency.

6.1.5 Effects of Source Voltage Impedance

In a real power system the source voltage impedance is highly complex and time-varying as network conditions continually change [11]. The source voltage impedance was altered to monitor the effects this may have on compensator performance.

The nominal examples above use a source impedance of 0.2Ω at 80° .

A variation, shown below, uses a source impedance of 1.0Ω at 80° .



Figure 6.15: Simulation Outputs, Step Change from no Load to 10 MW, 8 MVAR on phase BC. Source Voltage Impedance = 1.0Ω at 80°

It can be seen that the output of the compensator is still satisfactory. However, two distinct differences are noticed.

Firstly, the capacitor voltage takes a longer time to settle. Response is slower and there is considerably more overshoot. It is still within acceptable limits however, and the effect on output currents is barely noticable.

Secondly, the load currents contain a significant amount of harmonics. The higher source impedance causes a much greater harmonic distortion on the source voltage which is then reflected in the harmonic content of the load.

Harmonic filtering should be applied to the system.

6.2 CURRENT REFERENCE PULSE WIDTH MODULATION

6.2.1 Optimal Control Settings

The current controlled PWM method requires only a single PI controller, the purpose of which is to maintain capacitor voltage. The same optimisation procedure as described in 6.2.1 was followed. The end result was similar, with overdamped control preferred to underdamped control to ensure smooth as possible current waveforms.



Figure 6.16: Contour Plots of Negative Sequence Errors Used to Find Optimal PI Gains

6.2.2 Simulation Outputs

The hysteresis band was chosen to be 20 A. This provided between 15 to 30 switchings per valve per cycle. Switching delay was 5 microseconds, equal to one simulation time-step.

Shown below is a step change in the load from no-load to 10 MW, 8 MVAR on phase BC:



Figure 6.17: Simulation Outputs, Step Change from no-load to 10 MW, 8 MVAR phase BC.

The system currents are at unity power factor and contain no negative sequence at all times. However, they take around four full cycles before settling at steady-state. This is mainly due to delays in measurements fed to the control system.

The correct reference currents are not generated for the first cycle, because it takes the FFT com-

ponent approximately a cycle to measure the change in load. During this cycle the capacitor is effectively feeding the entire load, as the compensator is still enforcing zero system currents. This is why the capacitor significantly discharges during the first cycle. The FFT component which samples the capacitor voltage also has some delay. The result being that the capacitor is forced to recharge for the next three cycles, causing increased system currents.



Figure 6.18: Simulation Outputs, Step Change from 10MW, 8 MVAR phase BC to 10MW, 8 MVAR on Phases AB and CA.

The response to this step change is similar to the previous. The system currents stay continuously balanced at unity power factor, but steady state takes around four cycles. The capacitor voltage drops significantly during the first one to two cycles and requires another two cycles to recharge.



Figure 6.19: Simulation Outputs, Step Change from 10MW, 8 MVAR on Phases AB and CA to no-load.

The effects of measurement delay can again be seen in this response. For the first cycle immediately after the load is switched off, the FFT does not register this change, so the compensator continues to maintain the system currents of the previous cycle. This results in the capacitor being overcharged, as it absorbs the power that was previously being consumed by the load.

The capacitor voltage measurement is also delayed slightly, so it takes another three cycles to discharge back to 22.5 kV.

6.2.3 Harmonic Analysis

Figure 6.2 below shows the fourier analysis of the total system currents which have been balanced. It can be seen that the harmonics follow no strict pattern, although most are clustered around twice the average switching frequency (20 switchings per cycle). Note that this analysis is for only a single cycle - actual harmonic orders change continuously and are not necessarily multiples of the fundamental frequency.



Figure 6.20: Fourier Analysis of Balanced System Currents

6.2.4 Effects of Switching Delay / Minimum Switching Time

Increasing the switching delay small amounts (up to 100uS) has no noticeable effect on the harmonics or performance.

Very large switching delays, however, will increase all lower harmonics, especially the third. Shown below is the fourier analysis and current waveforms for a switching delay of 250uS while the STATCOM is balancing and power-factor correcting a 10 MW, 8 MW load on phase BC. The hysteresis band is exactly the same for previous examples - set at ± 0.2 kA.



Figure 6.21: Fourier Analysis of Balanced System Currents with Switching Delay



Figure 6.22: Distorted Current Waveforms due to Switching Delay

6.2.5 Lower Harmonic Filtering

A square-wave load was connected to phase BC to test the harmonic filtering of the current controlled method. The load consisted of a commutation inductance, diode bridge and current source. This is a typical model for a highly inductive DC motor [1]. Figure 6.25 shows the circuit used.



Figure 6.23: Bridge Circuit Used to Draw Square-Wave Load Currents

Figure 6.26 below shows that the compensator was capable of providing balanced, roughly sinusoidal output currents at unity power factor. Note that the waveshapes differ slightly from those shown in section 4.4.1. This is due to the current phase shift in a three phase system.



Figure 6.24: Compensation of Single Phase Square Wave Load

Fourier analysis of the waveforms, shown below, verifies that all lower-order harmonics below the 18th order are significantly reduced. Some higher order harmonics are introduced due to the PWM process,.



Figure 6.25: Fourier Analysis of Square Wave Compensation

6.2.6 Effects of Source Voltage Impedance

The source voltage impedance was increased from 0.2Ω at 80° to 1.0Ω at 80° and a step change from no-load to 10MW, 8MVAR phase BC was made.



Figure 6.26: Simulation Outputs, Step Change from no-load to 10MW, 8 MVAR phase BC.

The increased source resistance had a pronounced effect on harmonics in the load current, even moreso than the voltage controlled method.

Capacitor voltage control did not differ markedly, although it did take a slightly longer time to settle.

Otherwise the STATCOM perfomed satisfactorily.

Chapter 7 CONCLUSIONS

7.1 CONCLUSIONS

It has been shown through EMTDC/PSCAD simulations that a pulse width modulation static compensator is capable of providing fast-acting three-phase load-balancing and power factor correction.

This has been mathematically proven using sequence component theory. A perfectly balanced load at unity power factor contains only positice sequence real components. By removing the negative sequence real and reactive components from the load, the compensator is able to provide load balancing. By removing the positive sequence reactive component from the load, the compensator is also able to provide power factor correction.

This can be implemented using either of two different types of pulse width modulation. Sinusoidal pulse width modulation is the first option, whereby the STATCOM is controlled as a voltage source to provide the required compensator currents. Current reference pulse width modulation is the second option, whereby the STATCOM is controlled directly as a current source.

The first type of PWM, sinusoidal pulse width modulation, provides a good steady-state solution for constant unbalanced currents such as single phase railway loads. The GTO switchings are at a constant frequency and the output harmonics are limited and predictable. The dynamic response is good, with 90% compensation achieved within two cycles and steady state achieved within four cycles. DC transients are eliminated using negative feedback.

The control system for SPWM was developed using an interesting mathematical property of a three wire system. By controlling only the negative sequence reactive currents and using a zero-sequence filter, the system is forced to compensate the required negative sequence real currents without the need for additional control.

Sinusoidal pulse width modulation requires seven PI controllers in the control system and is not the preferred method for continuously changing loads.

Current reference pulse width modulation, however, provides a good dynamic solution for continually changing unbalanced loads such as arc furnaces. The net system currents are protected from most irregular transients due to the load.

Another advantage of current reference pulse width modulation is that all lower order harmonics are actively filtered out. This is also a useful property for square-wave or other nonlinear loads such as single-phase DC motors.

Note that for arc-furnace compensation the capacitor voltage controls would be need to be modified so that the charging time-constants do not clash with the rate of current changes in the arc furnace load.

The drawback of the current controlled method is the unpredictable switching frequency and the large range of output harmonics.

For both types of pulse width modulation, a delay must be introduced between valve switchings to allow plasma discharge in the semiconductor material and avoid a short-circuit condition. With sinusoidal PWM, the length of this delay can have a significant effect on the output harmonics of the compensator. Current reference PWM, however is largely unaffected.

Both types of modulation were shown to be fairly independent from the power system impedance.

7.2 FUTURE WORK

The main disadvantage of both PWM schemes is the high number of valve switchings required to overcome harmonics in the output currents. This results in a significant amount of switching losses and lowers the energy efficiency of the system.

Future work would include looking at alternative switching methods to reduce the number of switchings per cycle while maintaining an acceptable level of switching harmonics.

Satisfactory solutions could be found using selective harmonic elimination or multiple-level STATCOM's. In either case, the control methodology shown in this investigation would remain largely the same.

Another use of the three phase PWM STATCOM is voltage regulation. In this investigation it was assumed that the source voltage was balanced, and the only requirement was compensation of the load currents. Rather than provide power-factor correction, the STATCOM could provide voltage regulation, including balancing and regulation of an unbalanced source voltage.

This could be achieved by modifying the reactive current controls so that they satisfied the required level of voltage regulation instead of power factor correction.

Lastly, and most importantly, future work would include the building of a prototype. All of the analysis and testing in this investigation has been performed using the PSCAD/EMTDC simulation package. Design of a real system would need a very high performance digital signal processor to perform the required online fast fourier transforms.

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APPENDIX A - INSTANTANEOUS POWER OF THREE-PHASE DELTA-CONNECTED LOADS

The following derivation calculates the instantaneous power of a three-phase delta-connected load from the sequence components of the load currents and the source voltage. Zero sequence is ignored as it does not exist in a delta-connected load. The source voltage is assumed to be perfectly balanced..

Given that: $\alpha = 1 \angle 120^{\circ}$

Phase Currents are reconstructed from sequence components.:

$$\vec{Ia} = \vec{I_1} + \vec{I_2} \qquad \vec{Ib} = \alpha \vec{I_1} + \alpha^2 \vec{I_2} \qquad \vec{Ic} = \alpha^2 \vec{I_1} + \alpha \vec{I_2}$$

Then broken into real and imaginary parts:

$$\vec{Ia} = I_{1re} + jI_{1im} + I_{2re} + jI_{2im}$$

$$\vec{Ib} = \alpha^{2}(I_{1re} + jI_{1im}) + \alpha(I_{2re} + jI_{2im})$$

$$\vec{Ic} = \alpha(I_{1re} + jI_{1im}) + \alpha^{2}(I_{2re} + jI_{2im})$$

Vector quantities are then converted to instantaneous values:

$$Ia(t) = \sqrt{2}(I_{1re}\sin(\omega t) + I_{1im}\cos(\omega t) + I_{2re}\sin(\omega t) + I_{2im}\cos(\omega t))$$

$$Ib(t) = \sqrt{2}(I_{1re}\sin(\omega t - 120^\circ) + I_{1im}\cos(\omega t - 120^\circ) + I_{2re}\sin(\omega t + 120^\circ) + I_{2im}\cos(\omega t + 120^\circ))$$

$$Ic(t) = \sqrt{2}(I_{1re}\sin(\omega t + 120^{\circ}) + I_{1im}\cos(\omega t + 120^{\circ}))$$

...+ $I_{2re}\sin(\omega t - 120^{\circ}) + I_{2im}\cos(\omega t - 120^{\circ}))$

Given that the instantaneous line-ground voltages are:

$$Va(t) = \sqrt{2}V_{LG}\sin(\omega t)$$
$$Vb(t) = \sqrt{2}V_{LG}\sin(\omega t - 120^{\circ})$$
$$Vc(t) = \sqrt{2}V_{LG}\sin(\omega t + 120^{\circ})$$

Multiplication of instantaneous voltage and current provides instantaneous power:

$$Pa(t) = 2V_{LG}(I_{1re}sin^{2}(\omega t) + I_{1im}sin(\omega t)\cos(\omega t))$$
$$\dots + I_{2re}sin^{2}(\omega t) + I_{2im}sin(\omega t)\cos(\omega t))$$

$$Pb(t) = 2V_{LG}(I_{1re}sin^{2}(\omega t - 120^{\circ}) + I_{1im}sin(\omega t - 120^{\circ})cos(\omega t - 120^{\circ})$$

... + $I_{2re}sin(\omega t + 120^{\circ})sin(\omega t - 120^{\circ}) + I_{2im}sin(\omega t - 120^{\circ})cos(\omega t + 120^{\circ}))$

$$Pc(t) = 2V_{LG}(I_{1re}sin^{2}(\omega t + 120^{\circ}) + I_{1im}sin(\omega t + 120^{\circ})cos(\omega t - 120^{\circ})$$

... + $I_{2re}sin(\omega t + 120^{\circ})sin(\omega t - 120^{\circ}) + I_{2im}sin(\omega t + 120^{\circ})cos(\omega t - 120^{\circ}))$

These expressions can be altered using trigonmetric identities:

$$Pa(t) = V_{LG}(I_{1re}[1 - \cos(2\omega t)] + I_{1im}sin(2\omega t)$$

... + $I_{2re}[1 - \cos(2\omega t)] + I_{2im}sin(2\omega t))$

$$Pb(t) = V_{LG}(I_{1re}[1 - \cos(2\omega t + 120)] + I_{1im}sin(2\omega t + 120)$$
$$\dots + I_{2re}\left[-\cos(2\omega t) - \frac{1}{2}\right] + I_{2im}\left[sin(2\omega t) + \frac{\sqrt{3}}{2}\right]$$

$$Pc(t) = V_{LG}(I_{1re}[1 - \cos(2\omega t - 120)] + I_{1im}sin(2\omega t - 120)$$
$$\dots + I_{2re}[-\cos(2\omega t) - \frac{1}{2}] + I_{2im}[sin(2\omega t) - \frac{\sqrt{3}}{2}])$$

Summation of the three results in the cancellation of many terms and reveals the total instantaneous power:

$$Pa(t) + Pb(t) + Pc(t) = 3V_{LG}(I_{1re} - I_{2re}\cos(2\omega t) + I_{2im}\sin(2\omega t))$$

APPENDIX B - REAL AND REACTIVE PARTS OF LOAD BALANCER CURRENTS

The following derivation allows conversion from current sequence components to real and reactive parts of each phase current. This is used when ordering phase currents from a load balancer, given the sequence components of the unbalanced and/or uncompensated load.

Beginning with the same instantaneous current values as in Appendix A:

$$Ia(t) = \sqrt{2}(I_{1re}\sin(\omega t) + I_{1im}\cos(\omega t) + I_{2re}\sin(\omega t) + I_{2im}\cos(\omega t))$$

$$Ib(t) = \sqrt{2}(I_{1re}\sin(\omega t - 120^{\circ}) + I_{1im}\cos(\omega t - 120^{\circ}))$$

... + $I_{2re}\sin(\omega t + 120^{\circ}) + I_{2im}\cos(\omega t + 120^{\circ}))$

$$Ic(t) = \sqrt{2}(I_{1re}\sin(\omega t + 120^{\circ}) + I_{1im}\cos(\omega t + 120^{\circ}))$$

... + $I_{2re}\sin(\omega t - 120^{\circ}) + I_{2im}\cos(\omega t - 120^{\circ}))$

Phases B and C are time-shifted by $+120^{\circ}$ and -120° respectively:

$$Ia(t) = \sqrt{2}(I_{1re}\sin(\omega t) + I_{1im}\cos(\omega t) + I_{2re}\sin(\omega t) + I_{2im}\cos(\omega t))$$

$$Ib\left(t-\frac{120^{\circ}}{\omega}\right) = \sqrt{2}(I_{1re}\sin(\omega t) + I_{1im}\cos(\omega t))$$
$$\dots + I_{2re}\sin(\omega t-120^{\circ}) + I_{2im}\cos(\omega t-120^{\circ}))$$

$$Ic\left(t + \frac{120^{\circ}}{\omega}\right) = \sqrt{2}(I_{1re}\sin(\omega t) + I_{1im}\cos(\omega t))$$
$$\dots + I_{2re}\sin(\omega t + 120^{\circ}) + I_{2im}\cos(\omega t + 120^{\circ}))$$

Further deconstruct the negative sequence components of Phases B and C:

$$Ia(t) = \sqrt{2}(I_{1re}\sin(\omega t) + I_{1im}\cos(\omega t) + I_{2re}\sin(\omega t) + I_{2im}\cos(\omega t))$$

$$Ib\left(t - \frac{120^{\circ}}{\omega}\right) = \sqrt{2}(I_{1re}\sin(\omega t) + I_{1im}\cos(\omega t))$$
$$\dots + I_{2re}\left[-\frac{1}{2}\sin(\omega t) - \frac{\sqrt{3}}{2}\cos(\omega t)\right]$$
$$\dots + I_{2im}\left[\frac{\sqrt{3}}{2}\sin(\omega t) - \frac{1}{2}\cos(\omega t)\right]$$

$$Ic\left(t + \frac{120^{\circ}}{\omega}\right) = \sqrt{2}(I_{1re}\sin(\omega t) + I_{1im}\cos(\omega t))$$
$$\dots + I_{2re}\left[-\frac{1}{2}\sin(\omega t) + \frac{\sqrt{3}}{2}\cos(\omega t)\right]$$
$$\dots + I_{2im}\left[-\frac{\sqrt{3}}{2}\sin(\omega t) - \frac{1}{2}\cos(\omega t)\right]$$

Gather like terms:

$$Ia(t) = \sqrt{2}([I_{1re} + I_{2re}]\sin(\omega t) + [I_{1im} + I_{2im}]\cos(\omega t))$$

$$Ib(t - \frac{120^{\circ}}{\omega}) = \sqrt{2} \left(\left[I_{1re} - \frac{1}{2} I_{2re} + \frac{\sqrt{3}}{2} I_{2im} \right] \sin(\omega t) + \left[I_{1im} - \frac{\sqrt{3}}{2} I_{2re} - \frac{1}{2} I_{2im} \right] \cos(\omega t) \right)$$

$$Ic\left(t + \frac{120^{\circ}}{\omega}\right) = \sqrt{2}\left(\left[I_{1re} - \frac{1}{2}I_{2re} - \frac{\sqrt{3}}{2}I_{2im}\right]\sin(\omega t)\right)$$
$$\dots + \left[I_{1im} + \frac{\sqrt{3}}{2}I_{2re} - \frac{1}{2}I_{2im}\right]\cos(\omega t)\right)$$

These expressions can be readily converted back to phasors:

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$$\vec{Ia} = [I_{1re} + I_{2re}] + j[I_{1im} + I_{2im}]$$

$$\vec{Ib} = [I_{1re} - \frac{1}{2}I_{2re} + \frac{\sqrt{3}}{2}I_{2im}] + j[I_{1im} - \frac{\sqrt{3}}{2}I_{2re} - \frac{1}{2}I_{2im}]$$

$$\vec{Ic} = [I_{1re} - \frac{1}{2}I_{2re} - \frac{\sqrt{3}}{2}I_{2im}] + j[I_{1im} + \frac{\sqrt{3}}{2}I_{2re} - \frac{1}{2}I_{2im}]$$

Ignoring the I_{1re} term, these are converted into matrix form for calculating the required real and reactive current flows of a load-balancer:

$$\begin{bmatrix} Ia_{re} \\ Ib_{re} \\ Ic_{re} \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 0 & -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ 0 & -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} I_{1im} \\ I_{2re} \\ I_{2im} \end{bmatrix} \qquad \begin{bmatrix} Ia_{im} \\ Ib_{im} \\ Ic_{im} \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 \\ 1 & -\frac{\sqrt{3}}{2} & -\frac{1}{2} \\ 1 & \frac{\sqrt{3}}{2} & -\frac{1}{2} \\ 1 & \frac{\sqrt{3}}{2} & -\frac{1}{2} \end{bmatrix} \begin{bmatrix} I_{1im} \\ I_{2re} \\ I_{2im} \end{bmatrix}$$

This provides us with a solution that has no net real current flow. In practice, however, some net real current flow will be required to keep the storage element charged.

$$la_{re} + Ib_{re} + Ic_{re} = I_{CHARGE}$$

This expression can easily be added to the real power matrix in place of the I_{1im} term:

$$\begin{bmatrix} Ia_{re} \\ Ib_{re} \\ Ic_{re} \end{bmatrix} = \begin{bmatrix} \frac{1}{3} & 1 & 0 \\ \frac{1}{3} & -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{3} & -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} I_{CHARGE} \\ I_{2re} \\ I_{2im} \end{bmatrix} \qquad \begin{bmatrix} Ia_{im} \\ Ib_{im} \\ Ic_{im} \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 \\ 1 & -\frac{\sqrt{3}}{2} & -\frac{1}{2} \\ 1 & \frac{\sqrt{3}}{2} & -\frac{1}{2} \\ 1 & \frac{\sqrt{3}}{2} & -\frac{1}{2} \end{bmatrix} \begin{bmatrix} I_{1im} \\ I_{2re} \\ I_{2im} \end{bmatrix}$$

If load-balancing is the only goal, and power-factor correction is not required, the I_{lim} term can be set to zero.

APPENDIX C - REQUIRED COMPENSATOR CURRENTS FROM LOAD POWERS

The following derivation allows the calculation of required compensator currents using phase-tophase load powers. This is useful when determining the ratings of the compensator components.

The problem is approached using superposition. Three single line-load loads are analysed and the solution currents are summated to provide the final solution.

Single Line-Line Loads:



Total Solution:



$$I_L a = I_L a' + I_L a'' + I_L a'''$$
$$I_L b = I_L b' + I_L b''' + I_L b'''$$
$$I_L c = I_L c' + I_L c''' + I_L c'''$$

Firstly, the load on phase AB is analysed:

$$\overrightarrow{Vab} = \overrightarrow{Va} - \overrightarrow{Vb}$$

$$= Vlg - \alpha^{2}Vlg$$

$$= Vlg \left[\frac{3+j\sqrt{3}}{2}\right]$$

$$\overrightarrow{I_{L}a'} = \left(\frac{\overrightarrow{Sab}}{\overrightarrow{Vab}}\right)^{*} \qquad \overrightarrow{I_{L}b'} = -\overrightarrow{I_{L}a'}$$

$$= \left(\frac{Pab+jQab}{Vlg}\left[\frac{2}{3+j\sqrt{3}}\right]\right)^{*} \qquad = \frac{-\left[Pab+\frac{Qab}{\sqrt{3}}\right] + -j\left[\frac{Pab}{\sqrt{3}} - Qab\right]}{2Vlg}$$

$$= \frac{\left[Pab+\frac{Qab}{\sqrt{3}}\right] + j\left[\frac{Pab}{\sqrt{3}} - Qab\right]}{2Vlg} \qquad \overrightarrow{I_{L}c'} = 0$$

Next, the load on phase BC is analysed:

$$\overrightarrow{Vbc} = \overrightarrow{Vb} - \overrightarrow{Vc}$$
$$= \alpha^2 V lg - \alpha V lg$$
$$= -j \sqrt{3} V lg$$

$$\vec{I_L b''} = \left(\frac{\overrightarrow{Sbc}}{\overrightarrow{Vbc}}\right)^* \qquad \qquad \vec{I_L c''} = -\overrightarrow{I_L b''} \\ = \left(\frac{Pbc + jQbc}{-j\sqrt{3}Vlg}\right)^* \qquad \qquad = \frac{[Qbc] + j[Pbc]}{\sqrt{3}Vlg} \\ = \frac{[-Qbc] + j[-Pbc]}{\sqrt{3}Vlg} \qquad \qquad \overrightarrow{I_L a''} = 0$$

Thirdly, the load on phase CA is analysed:

$$\overrightarrow{Vca} = \overrightarrow{Vc} - \overrightarrow{Va}$$

$$= \alpha V lg - V lg$$

$$= V lg \left[\frac{-3 + j\sqrt{3}}{2} \right]$$

$$\overrightarrow{I_Lc'''} = \left(\frac{\overrightarrow{Sca}}{\overrightarrow{Vca}} \right)^* \qquad \overrightarrow{I_La'''} = -\overrightarrow{I_Lc'''}$$

$$= \left(\frac{Pca + jQca}{Vlg} \left[\frac{-3 + j\sqrt{3}}{2} \right] \right)^* \qquad = \frac{\left[\frac{Pca - Qca}{\sqrt{3}} \right] + j \left[-\frac{Pca}{\sqrt{3}} - Qca \right]}{2V lg}}{2V lg}$$

$$= \frac{\left[-Pca + \frac{Qca}{\sqrt{3}} \right] + j \left[\frac{Pca}{\sqrt{3}} + Qca \right]}{2V lg} \qquad \overrightarrow{I_Lb'''} = 0$$

Single load currents are then summated to find total load currents:

$$\overrightarrow{I_La} = \overrightarrow{I_La'} + \overrightarrow{I_La''} + \overrightarrow{I_La''} = \frac{\left[\frac{Pab + Pca + (Qab - Qca)}{\sqrt{3}}\right] + j\left[\frac{(Pab - Pca)}{\sqrt{3}} - Qab - Qca\right]}{2Vlg}$$
$$\overrightarrow{I_Lb} = \overrightarrow{I_Lb'} + \overrightarrow{I_Lb''} + \overrightarrow{I_Lb'''} = \frac{\left[-Pab - \frac{(Qab + 2Qbc)}{\sqrt{3}}\right] + j\left[\frac{-(Pab + 2Pbc)}{\sqrt{3}} + Qab\right]}{2Vlg}$$

$$\overrightarrow{I_L c} = \overrightarrow{I_L c'} + \overrightarrow{I_L c''} + \overrightarrow{I_L c'''} = \frac{\left[-Pca + \frac{(Qca + 2Qbc)}{\sqrt{3}}\right] + j\left[\frac{(Pca + 2Pbc)}{\sqrt{3}} + Qca\right]}{2Vlg}$$

Now it is possible to find the positive and negative sequence load currents:

$$\vec{I_L 1} = \vec{I_L a} + \alpha \cdot \vec{I_L b} + \alpha^2 \cdot \vec{I_L c}$$

$$= \frac{[Pab + Pbc + Pca] + [jQab + Qbc + Qca]}{3Vlg}$$

$$\vec{I_L 2} = \vec{I_L a} + \alpha^2 \cdot \vec{I_L b} + \alpha \cdot \vec{I_L c}$$

$$= \frac{[Pab + Pca - 2Pbc + \sqrt{3}(Qab - Qca)] + j[-Qab - Qca + 2Qbc + \sqrt{3}(Pab - Pca)]}{2Vlg}$$

The required system currents (I_s) are the sum of load (I_L) and compensator (I_C) currents and should contain only the positive sequence component of the load current as follows:

$$\overrightarrow{I_Sa} = \overrightarrow{I_La} + \overrightarrow{I_Ca} = \overrightarrow{I_L1}$$
$$\overrightarrow{I_Sb} = \overrightarrow{I_Lb} + \overrightarrow{I_Cb} = \alpha^2 \cdot \overrightarrow{I_L1}$$
$$\overrightarrow{I_Sc} = \overrightarrow{I_Lc} + \overrightarrow{I_Cc} = \alpha \cdot \overrightarrow{I_L1}$$

These expressions can be rearranged with compensator currents as the subject:

$$\overrightarrow{I_C a} = \overrightarrow{I_L 1} - \overrightarrow{I_L a}$$
$$\alpha \overrightarrow{I_C b} = \overrightarrow{I_L 1} - \alpha \overrightarrow{I_L b}$$
$$\alpha^2 \overrightarrow{I_C c} = \overrightarrow{I_L 1} - \alpha^2 \overrightarrow{I_L c}$$

These equations can now be solved for I_Ca , I_Cb , I_Cc in terms of Pab, Pbc, Pca, Qab, Qbc, Qca:

$$\overrightarrow{I_Ca} = \frac{[Pab+2Pbc-Pca-\sqrt{3}(Qab-Qca)]+j[\sqrt{3}(Pab-Pca)-3(Qab+Qca)]}{6Vlg}$$

$$\alpha \cdot \overrightarrow{I_Cb} = \frac{[Pbc+2Pca-Pab-\sqrt{3}(Qbc-Qab)]+j[\sqrt{3}(Pbc-Pab)-3(Qbc+Qab)]}{6Vlg}$$

$$\alpha^2 \cdot \overrightarrow{I_Cc} = \frac{[Pca+2Pab-Pbc-\sqrt{3}(Qca-Qbc)]+j[\sqrt{3}(Pca-Pbc)-3(Qca+Qbc)]}{6Vlg}$$

Note that these solutions are given in rotated form. Refer to chapter 2.1 for more details.



Rotated (form shown above)