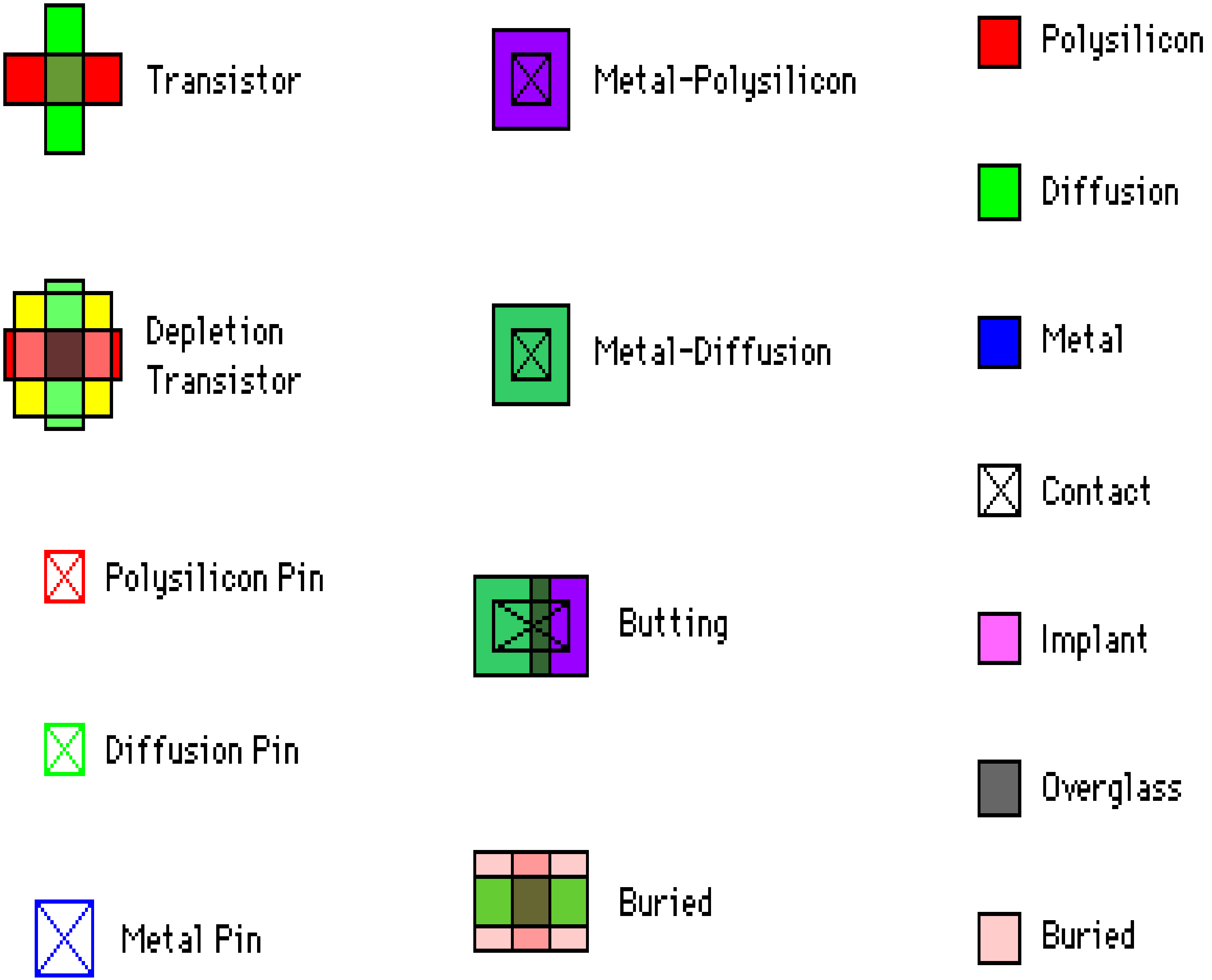
Stick diagram and Layout Diagram

INTRODUCTION

- Objectives:
  - To know MOS layers
  - To understand the stick diagrams
  - To learn design rules
  - To understand layout and symbolic diagrams

- Outcome:
  - At the end of this, will be able draw the stick diagram, layout and symbolic diagram for simple MOS circuits

MOS LAYERS


Transistor
Metal-Polysilicon
Polysilicon
Diffusion
Depletion Transistor
Metal-Diffusion
Metal
Contact
Polysilicon Pin
Butting
Implant
Diffusion Pin
Overglass
Metal Pin
Buried
Buried

STICK DIAGRAMS

- Objectives:
  - To know what is meant by stick diagram.
  - To understand the capabilities and limitations of stick diagram.
  - To learn how to draw stick diagrams for a given MOS circuit.

- Outcome:
  - At the end of this module the students will be able draw the stick diagram for simple MOS circuits.

STICK DIAGRAMS

- VLSI design aims to translate circuit concepts onto silicon.
- Stick diagrams are a means of capturing topography and layer information using simple diagrams.
- Stick diagrams convey layer information through color codes (or monochrome encoding).
- Acts as an interface between symbolic circuit and the actual layout.

STICK DIAGRAMS

- Does show all components/vias.
  - Via is used to connect higher level metals from metal connection
- It shows relative placement of components.
- Goes one step closer to the layout
- Helps plan the layout and routing

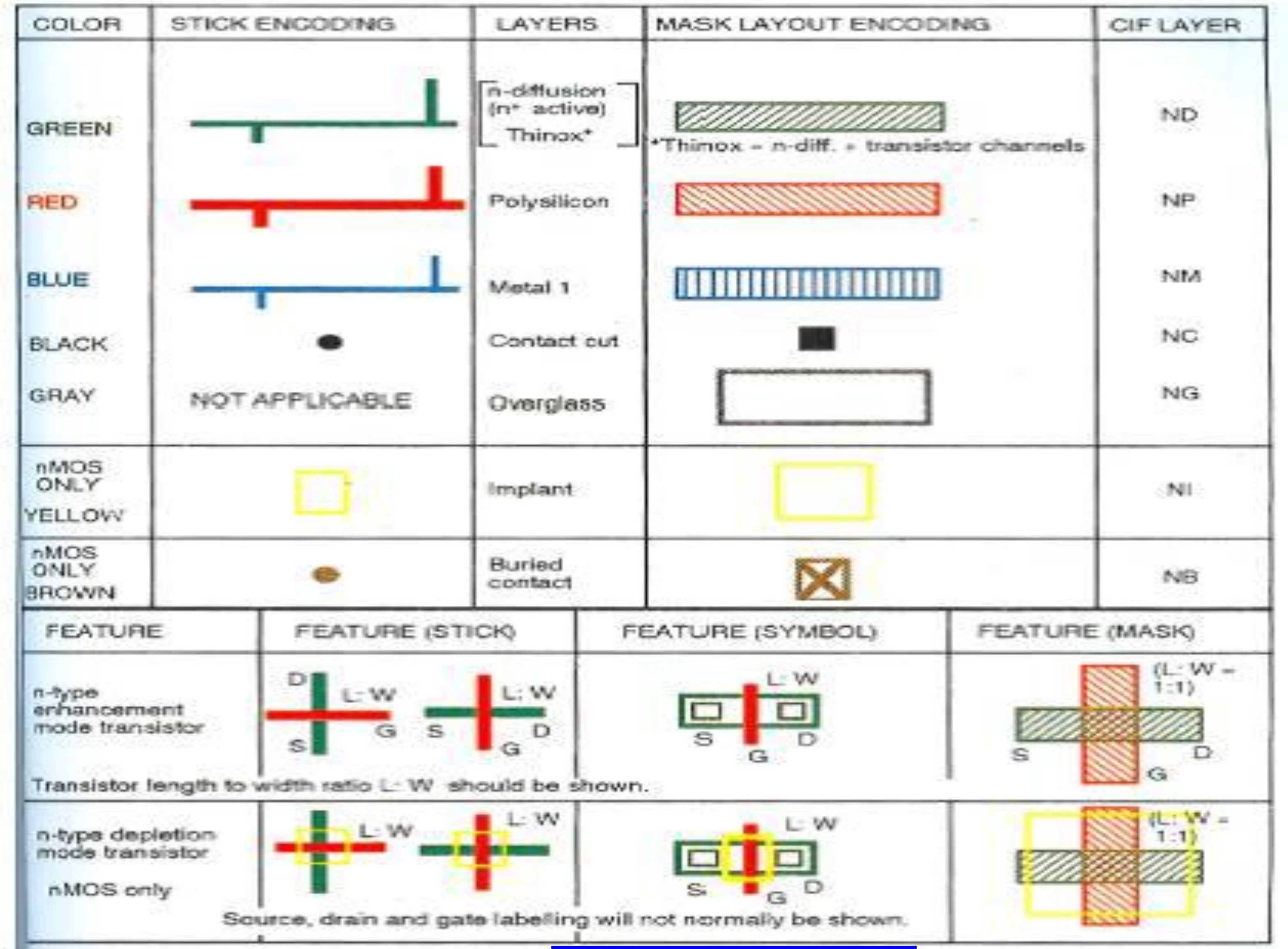
A stick diagram is a cartoon of a layout.

STICK DIAGRAMS

- Does ***not*** show
  - Exact placement of components
  - Transistor sizes
  - Wire lengths, wire widths, tub boundaries
  - Any other low level details such as parasitics

Stick Diagrams – Notations

STICK DIAGRAMS

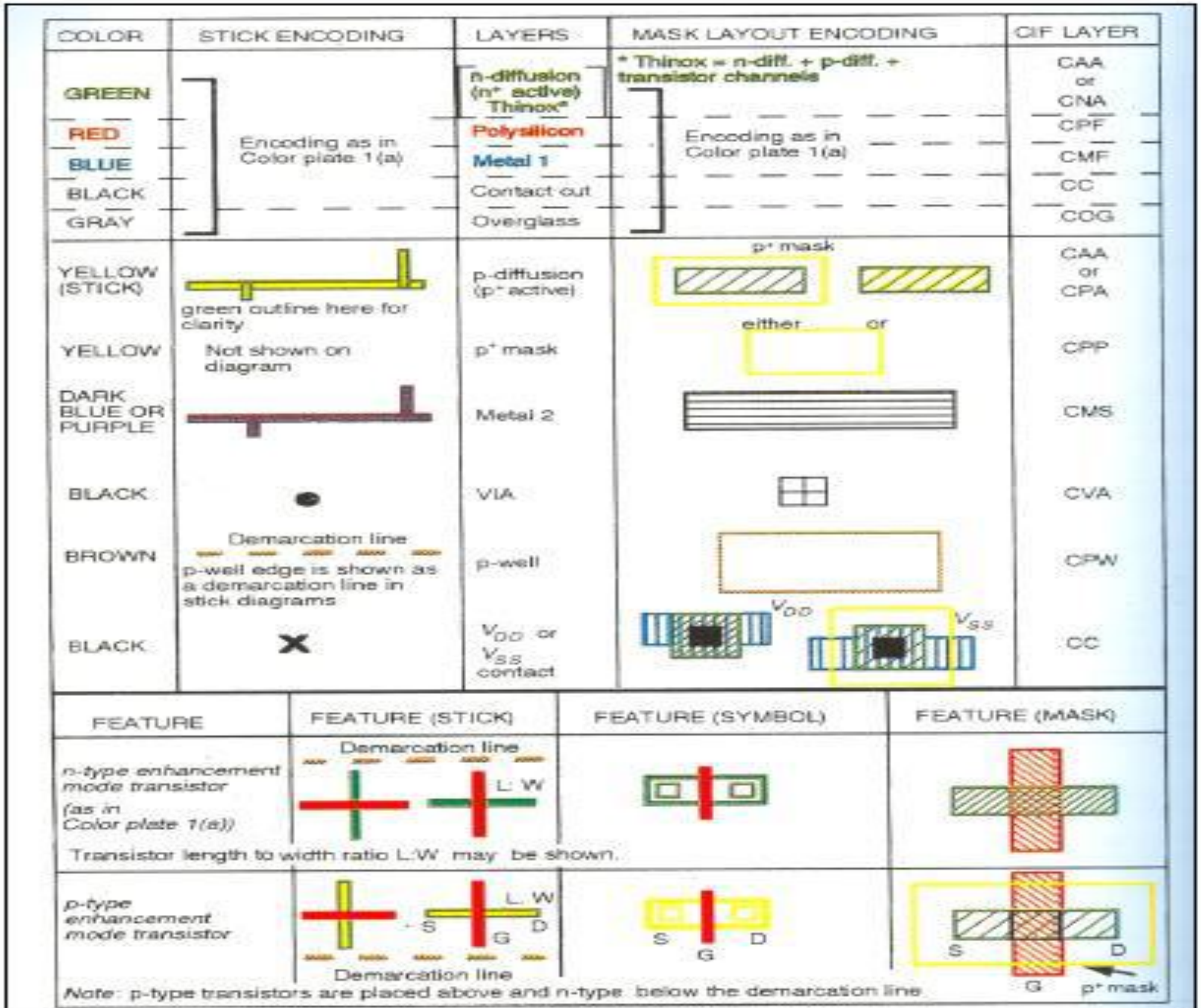


COLOR	STICK ENCODING	LAYERS	MASK LAYOUT ENCODING	CIF LAYER
GREEN		n-diffusion (n^+ active) Thinox*	*Thinox = n-diff. + transistor channels	ND
RED		Polysilicon		NP
BLUE		Metal 1		NM
BLACK		Contact cut		NC
GRAY	NOT APPLICABLE	Overglass		NG
nMOS ONLY YELLOW		Implant		NI
nMOS ONLY BROWN		Buried contact		NB

FEATURE	FEATURE (STICK)	FEATURE (SYMBOL)	FEATURE (MASK)
n-type enhancement mode transistor	D L:W G S; L:W S D G	L:W S G D	(L:W ~ 1:1) S D G
Transistor length to width ratio L:W should be shown.			
n-type depletion mode transistor nMOS only	L:W; L:W	L:W S G D	(L:W ~ 1:1)
Source, drain and gate labelling will not normally be shown.			

NMOS ENCODING

STICK DIAGRAMS

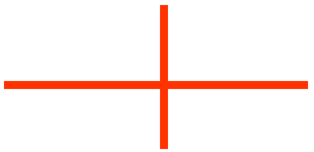


CMOS ENCODING

Stick Diagrams – Some Rules

Rule 1:

When two or more ‘sticks’ of the same type cross or touch each other that represents electrical contact.

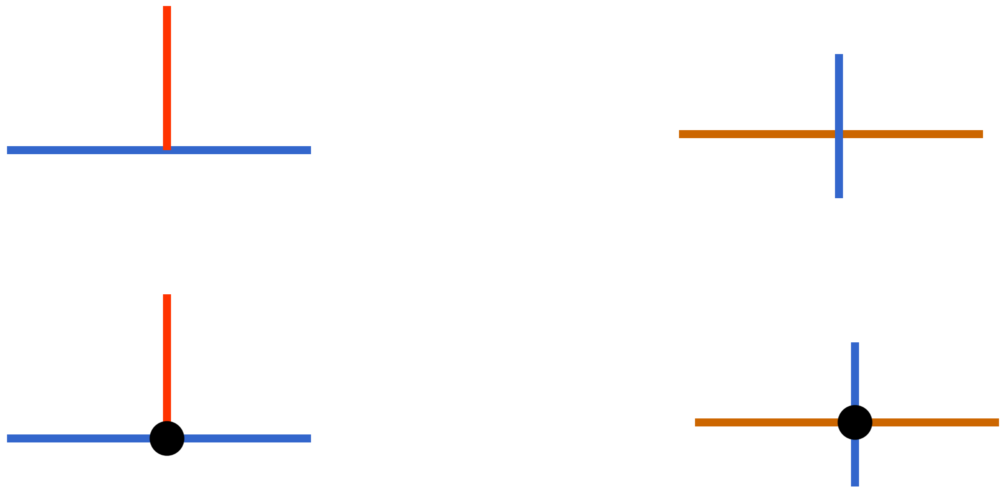


Stick Diagrams – Some Rules

Rule 2:

When two or more 'sticks' of different type cross or touch each other there is no electrical contact.

(If electrical contact is needed we have to show the connection explicitly)



Stick Diagrams – Some Rules

Rule 3:

When a poly crosses diffusion it represents a transistor.

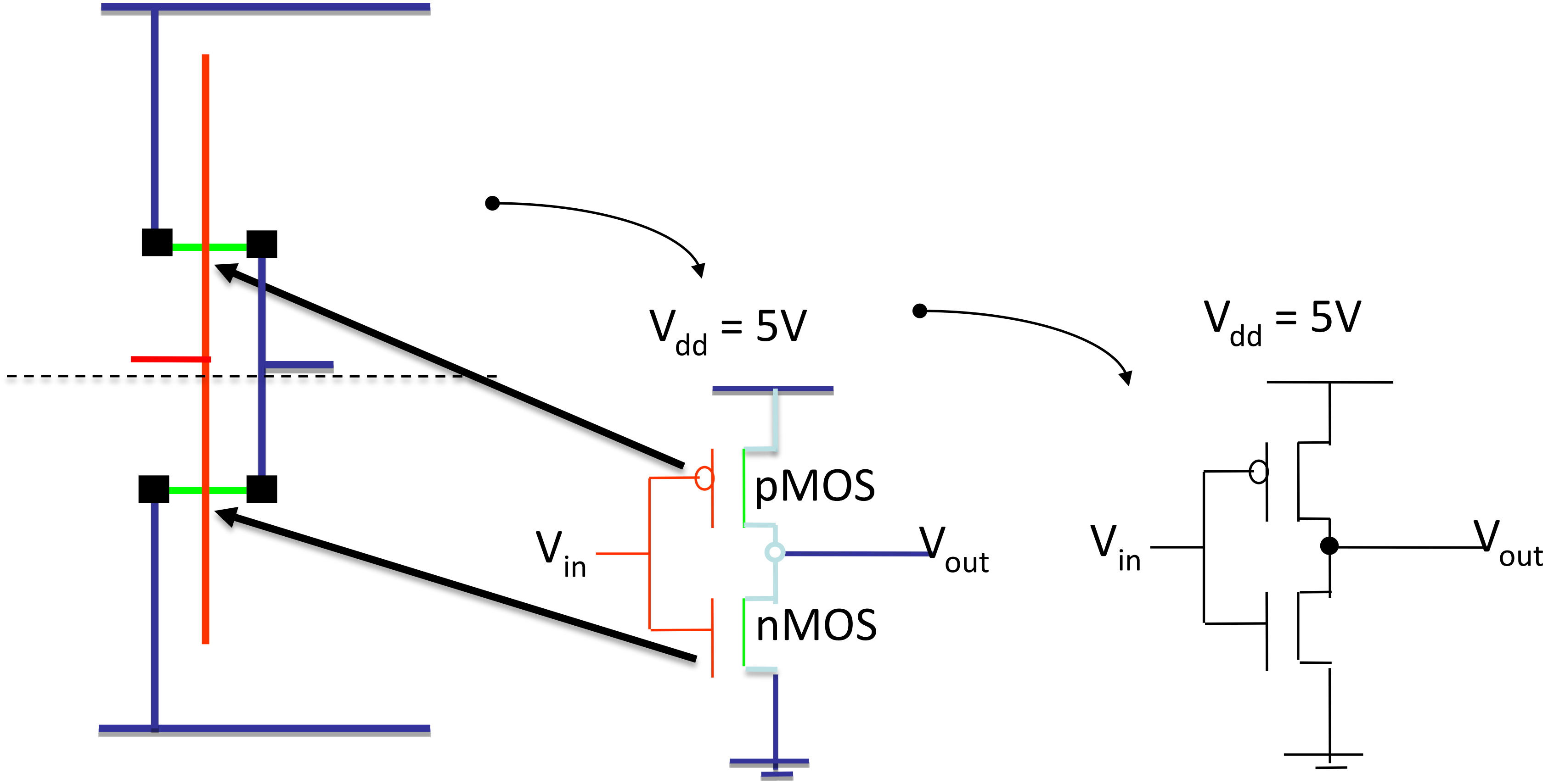
Note: If a contact is shown then it is ***not*** a transistor.

Stick Diagrams – Some Rules

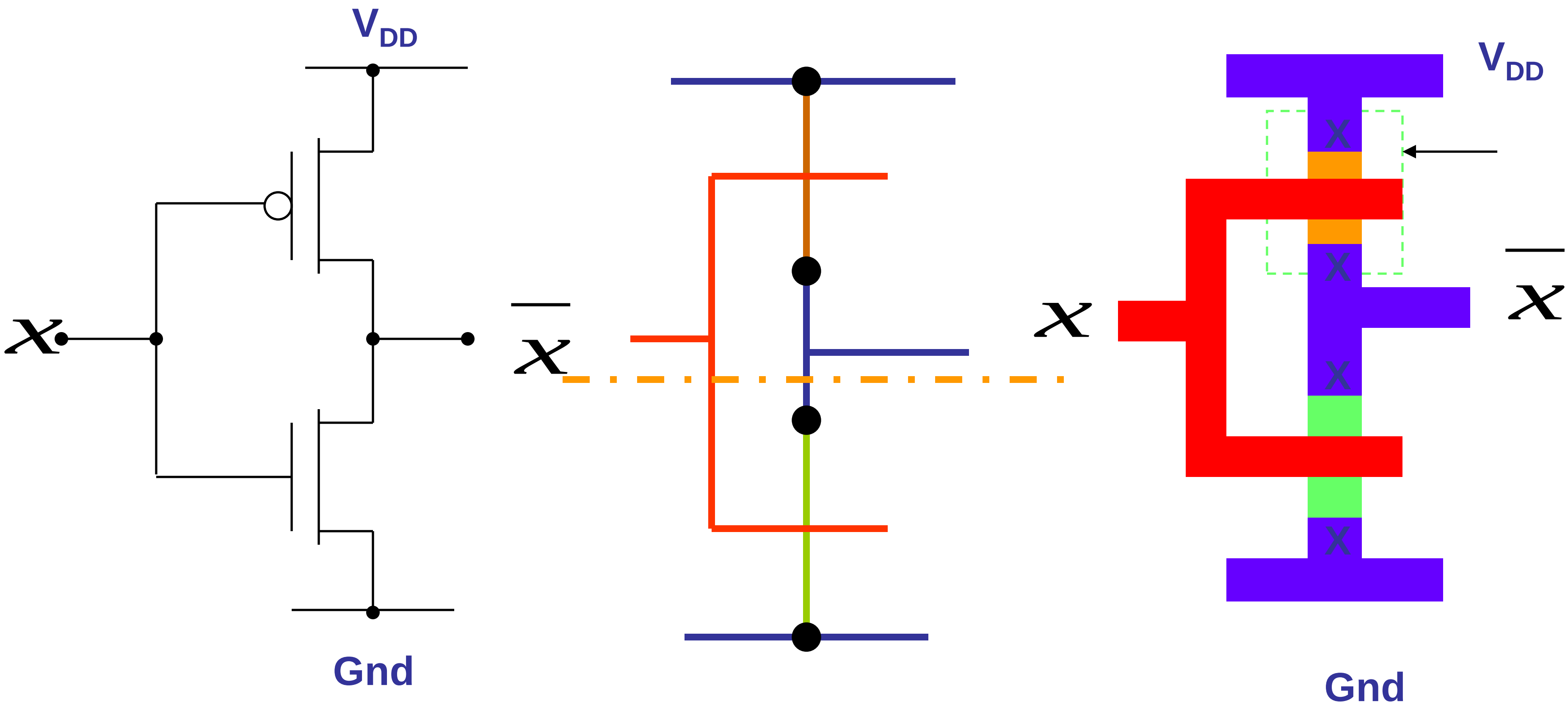
Rule 4:

In CMOS a demarcation line is drawn to avoid touching of p-diff with n-diff. All PMOS must lie on one side of the line and all NMOS will have to be on the other side.

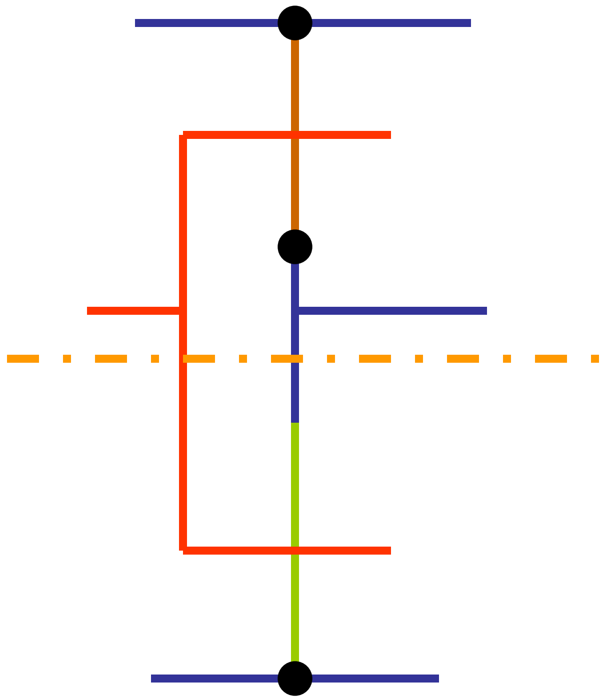
Examples of Stick Diagrams

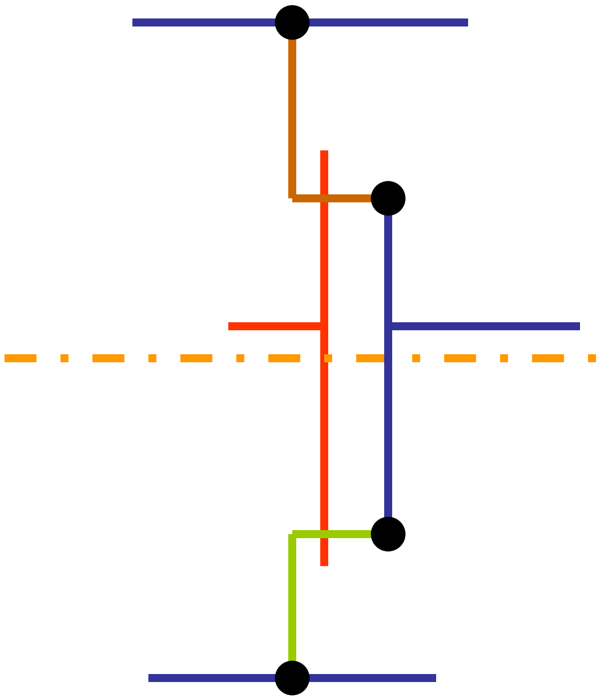


Examples of Stick Diagrams

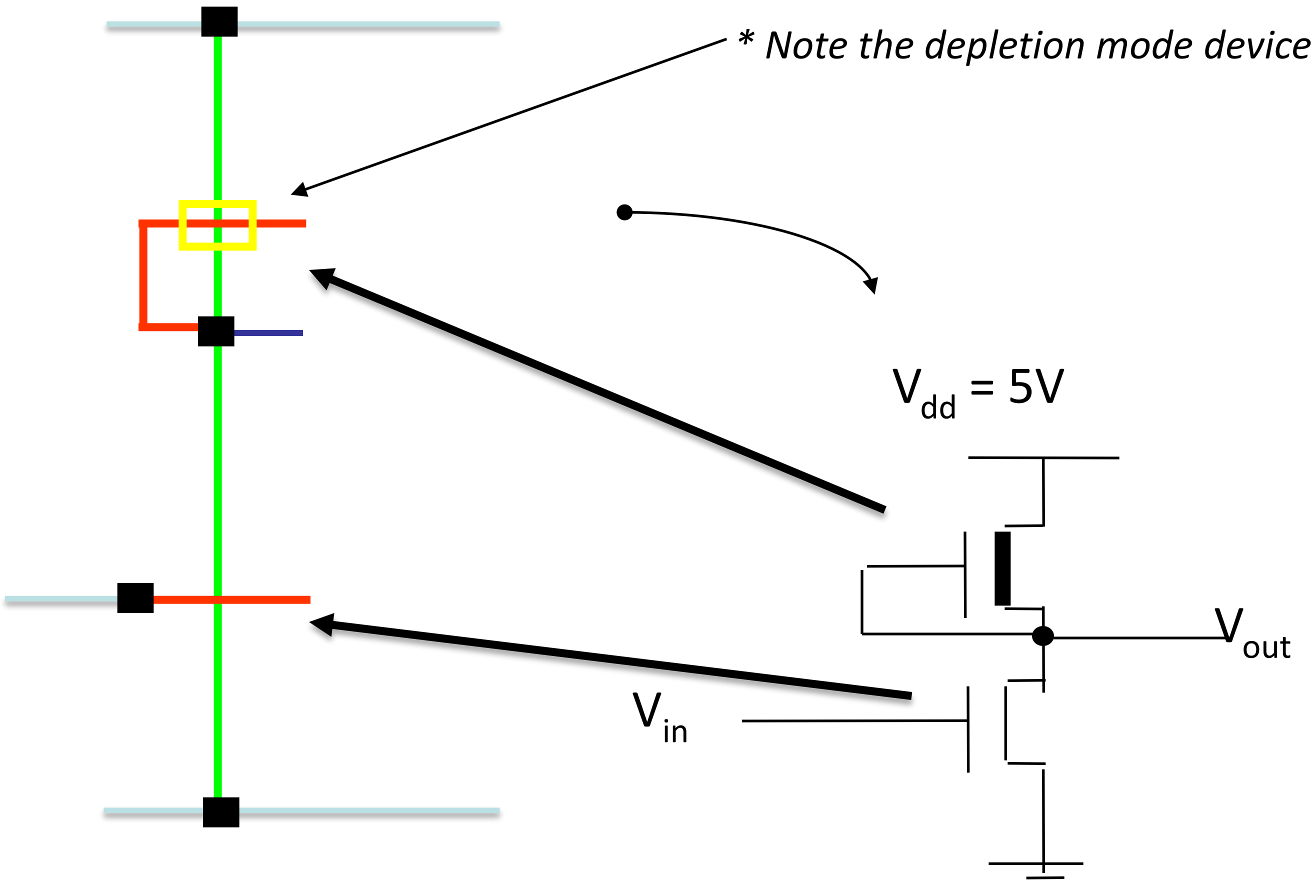


Examples of Stick Diagrams

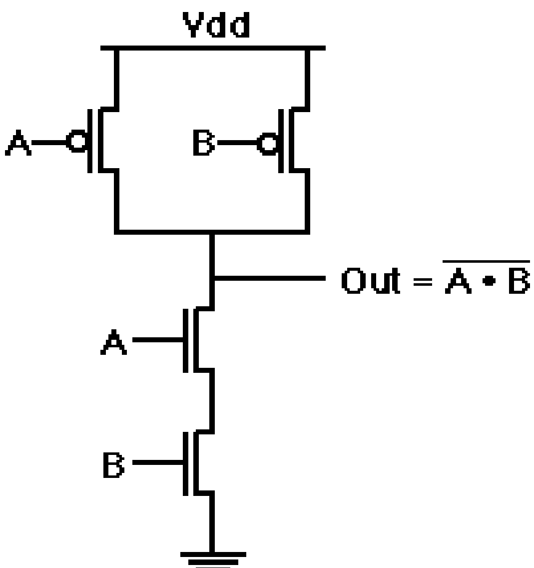




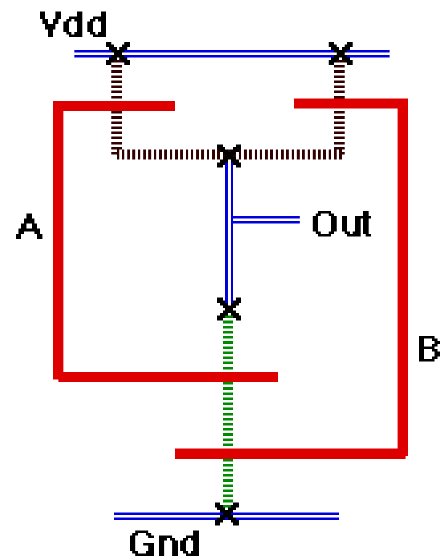
Examples of Stick Diagrams



Examples of Stick Diagrams



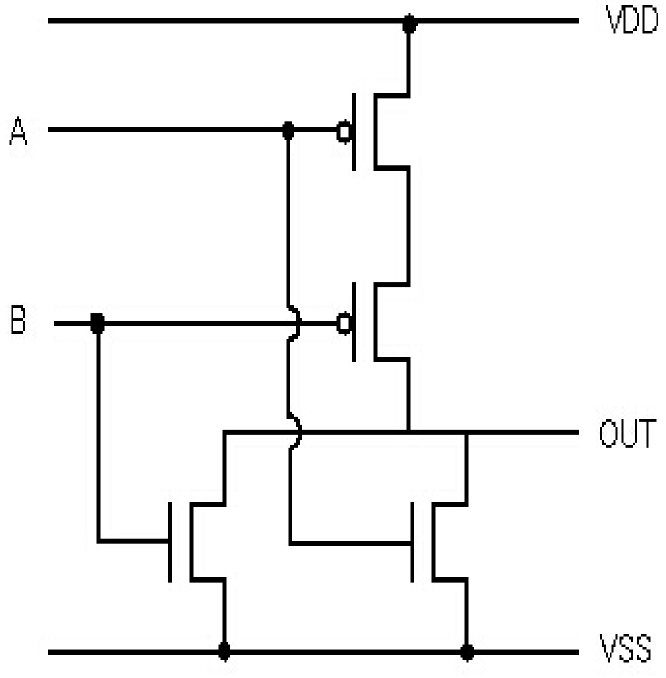
A	B	$\overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0



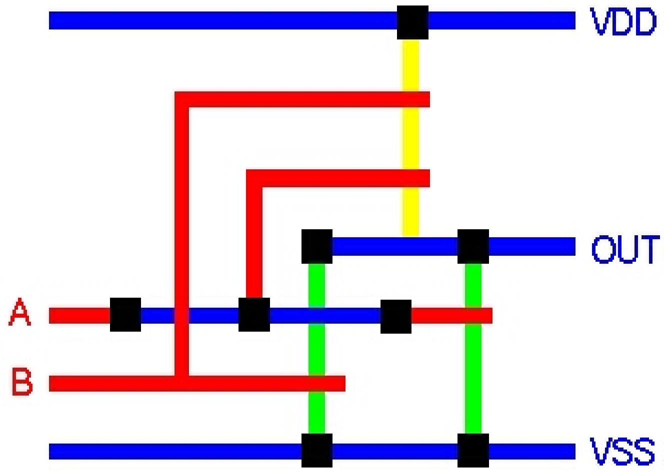
1. Pull-down: Connect to ground If A=1 AND B=1

2. Pull-up: Connect to Vdd If A=0 OR B=0

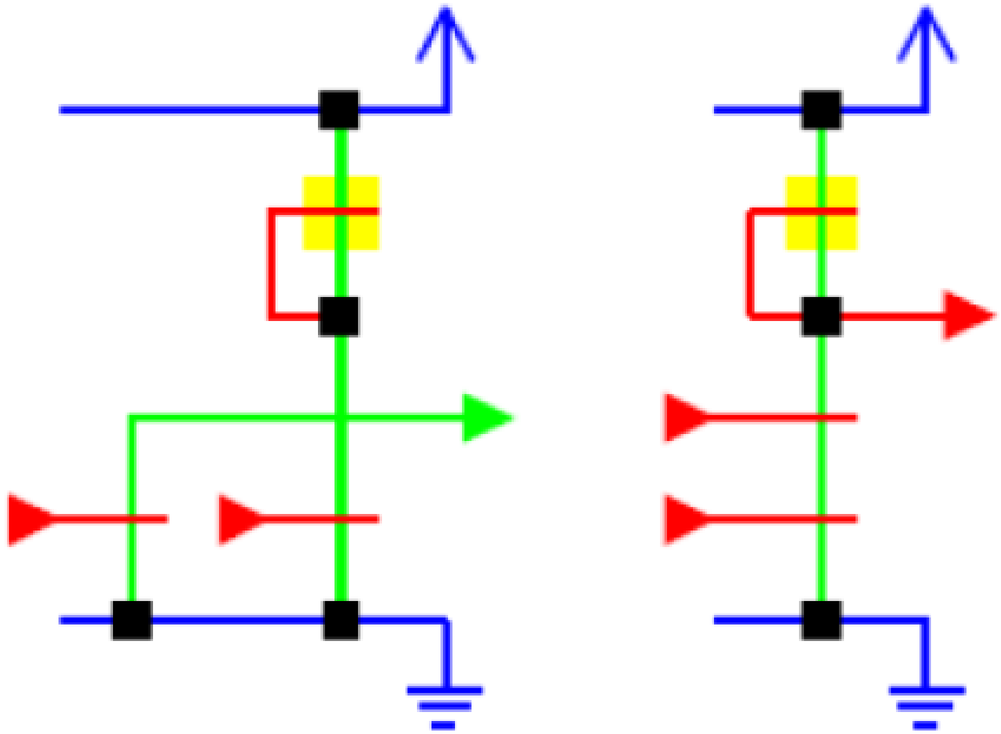
Examples of Stick Diagrams



NOR gate in CMOS

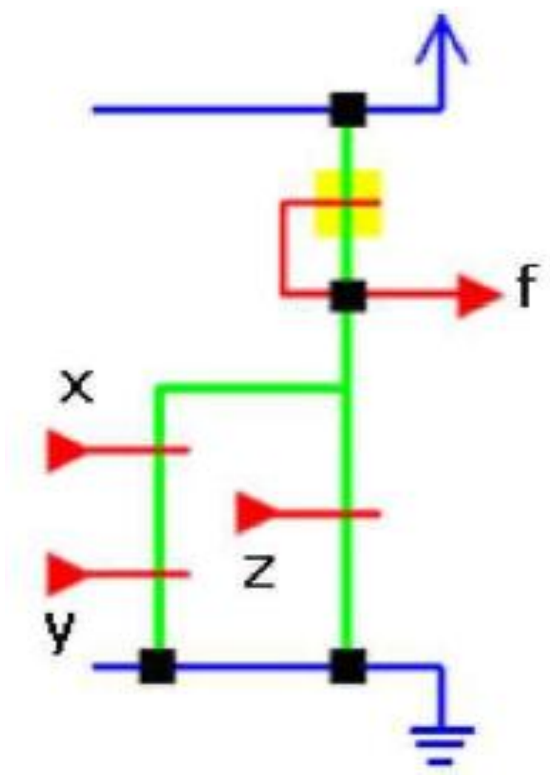


Examples of Stick Diagrams



NOR gate and NAND using NMOS Transistors

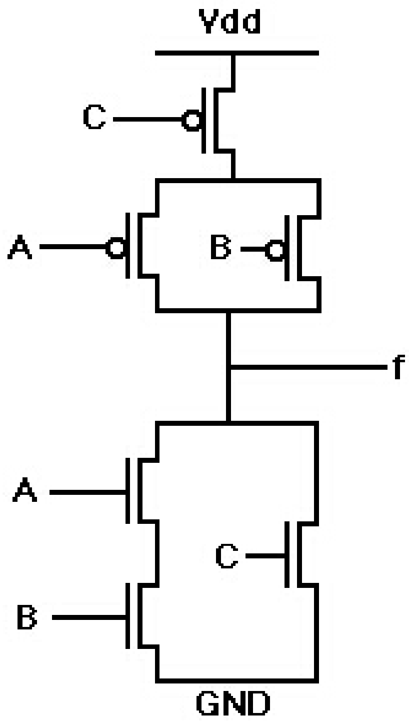
Examples of Stick Diagrams

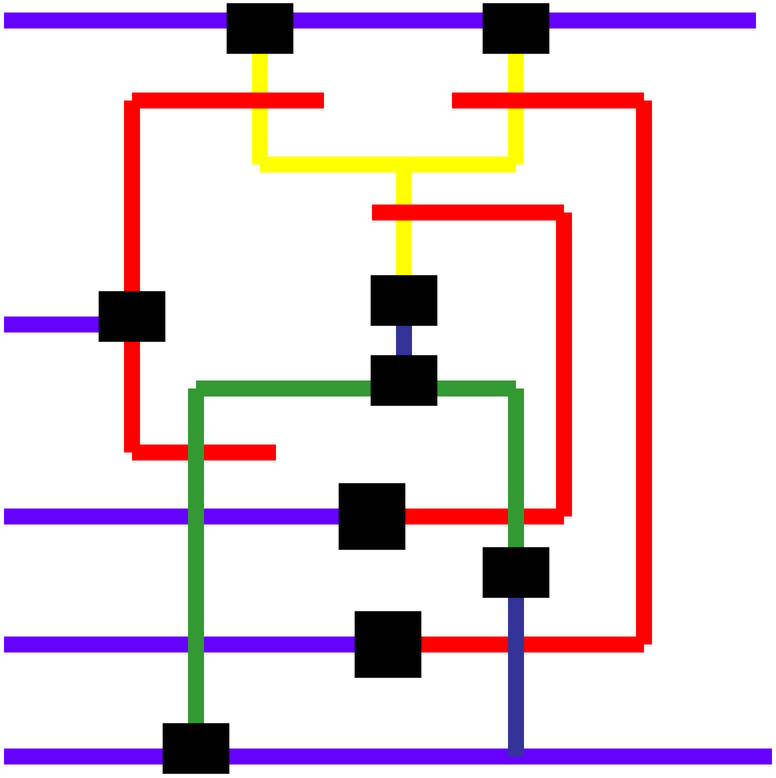


f= [(xy) +z]' using NMOS Transistors

Examples of Stick Diagrams

Example: $f = \overline{(A \bullet B) + C}$





DESIGN RULES

- **Why we use design rules?**
  - Interface between designer and process engineer

- Historically, the process technology referred to the length of the silicon channel between the source and drain terminals in field effect transistors.
- The sizes of other features are generally derived as a ratio of the channel length, where some may be larger than the channel size and some smaller.
  - For example, in a 90 nm process, the length of the channel may be 90 nm, but the width of the gate terminal may be only 50 nm.

DESIGN RULES

Semiconductor manufacturing processes

- 10 µm — 1971
- 3 µm — 1975
- 1.5 µm — 1982
- 1 µm — 1985
- 800 nm (0.80 µm) — 1989
- 600 nm (0.60 µm) — 1994
- 350 nm (0.35 µm) — 1995
- 250 nm (0.25 µm) — 1998
- **180 nm** (0.18 µm) — 1999
- 130 nm (0.13 µm) — 2000
- 90 nm — 2002
- 65 nm — 2006
- 45 nm — 2008
- 32 nm — 2010
- 22 nm — approx. 2011
- 16 nm — approx. 2018
- 11 nm — approx. 2022

DESIGN RULES

- Allow translation of circuits (usually in stick diagram or symbolic form) into actual geometry in silicon
- Interface between circuit designer and fabrication engineer
- Compromise
  - designer - tighter, smaller
  - fabricator - controllable, reproducible

DESIGN RULES

- Design rules define ranges for features
  - Examples:
    - min. wire widths to avoid breaks
    - min. spacing to avoid shorts
    - minimum overlaps to ensure complete overlaps
  - Measured in microns
  - Required for resolution/tolerances of masks
- Fabrication processes defined by minimum channel width
  - Also minimum width of poly traces
  - Defines "how fast" a fabrication process is

DESIGN RULES

- **Two major approaches:**
  - **"Micron" rules: stated at micron resolution.**
  - **λ rules: simplified micron rules with limited scaling attributes.**
- **Design rules represents a tolerance which insures very high probability of correct fabrication**
  - scalable design rules: lambda parameter
  - absolute dimensions (micron rules)

"Micron" rules

- All minimum sizes and spacing specified in microns.
- Rules don't have to be multiples of λ.
- Can result in 50% reduction in area over λ based rules
- Standard in industry.

Lambda-based Design Rules

- *Lambda-based* (scalable CMOS) design rules define scalable rules based on λ (which is half of the minimum channel length)
  - classes of MOSIS SCMOS rules: SUBMICRON, DEEPSUBMICRON
- Stick diagram is a draft of real layout, it serves as an abstract view between the schematic and layout.

Lambda-based Design Rules

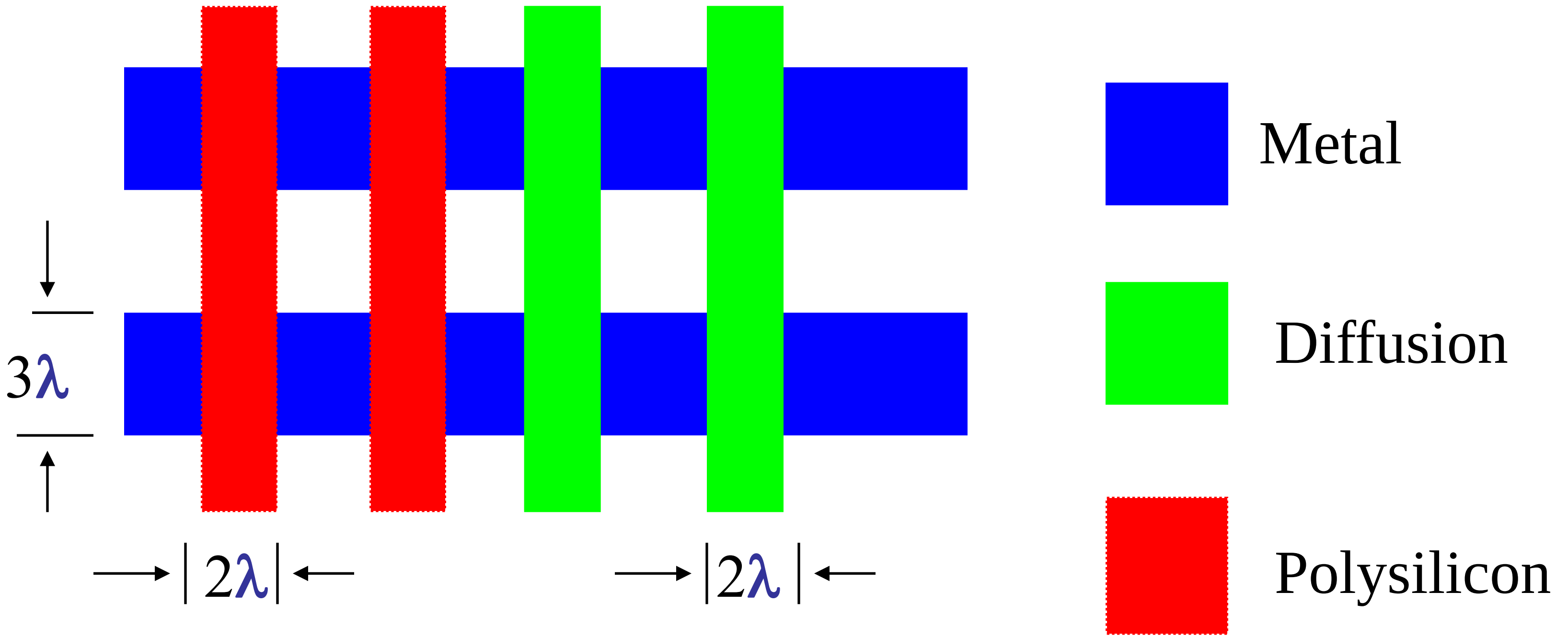
- Circuit designer in general want tighter, smaller layouts for improved performance and decreased silicon area.
- On the other hand, the process engineer wants design rules that result in a controllable and reproducible process.
- Generally we find there has to be a compromise for a competitive circuit to be produced at a reasonable cost.
- All widths, spacing, and distances are written in the form
- λ = 0.5 X minimum drawn transistor length

Lambda-based Design Rules

- Design rules based on single parameter, λ
- Simple for the designer
- Wide acceptance
- Provide feature size independent way of setting out mask
- If design rules are obeyed, masks will produce working circuits
- Minimum feature size is defined as 2 λ
- Used to preserve topological features on a chip
- Prevents shorting, opens, contacts from slipping out of area to be contacted

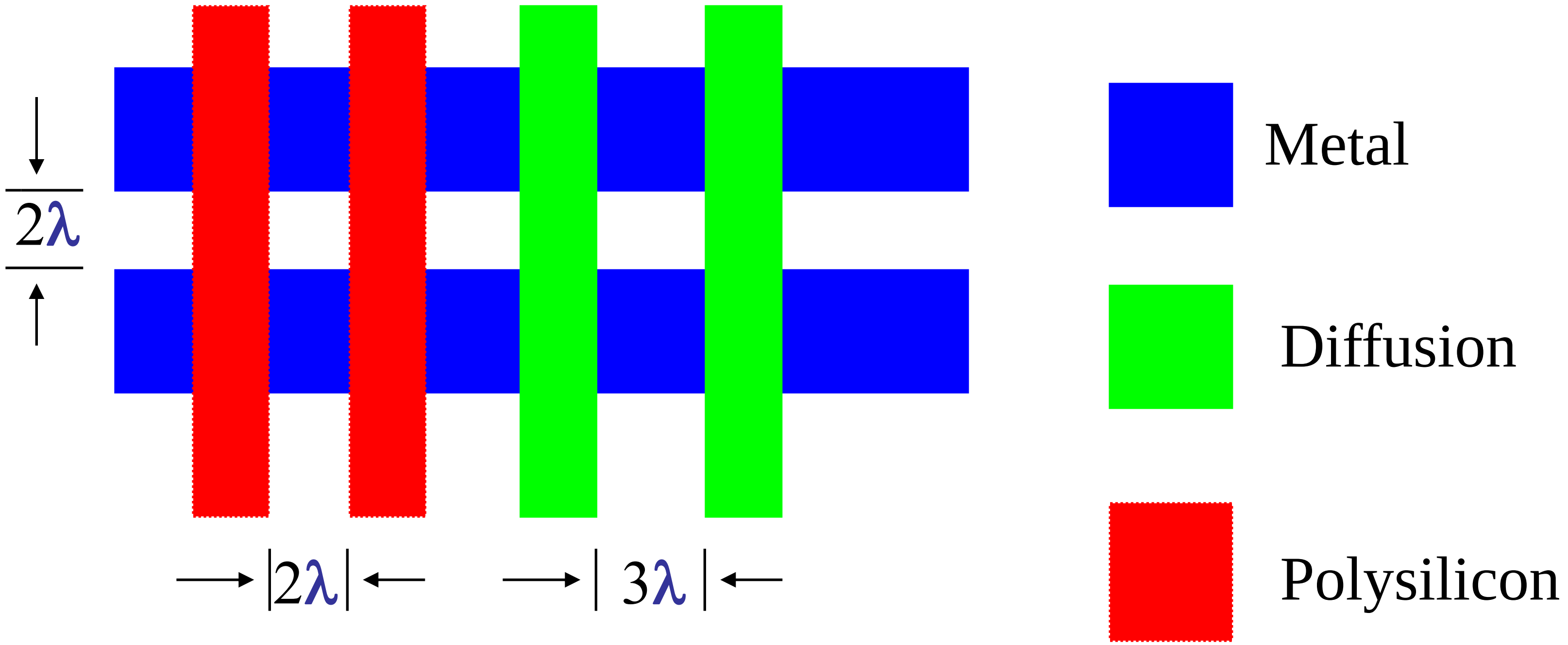
DESIGN RULES

- Minimum width of PolySi and diffusion line **2λ**
- Minimum width of Metal line **3λ** as metal lines run over a more uneven surface than other conducting layers to ensure their continuity



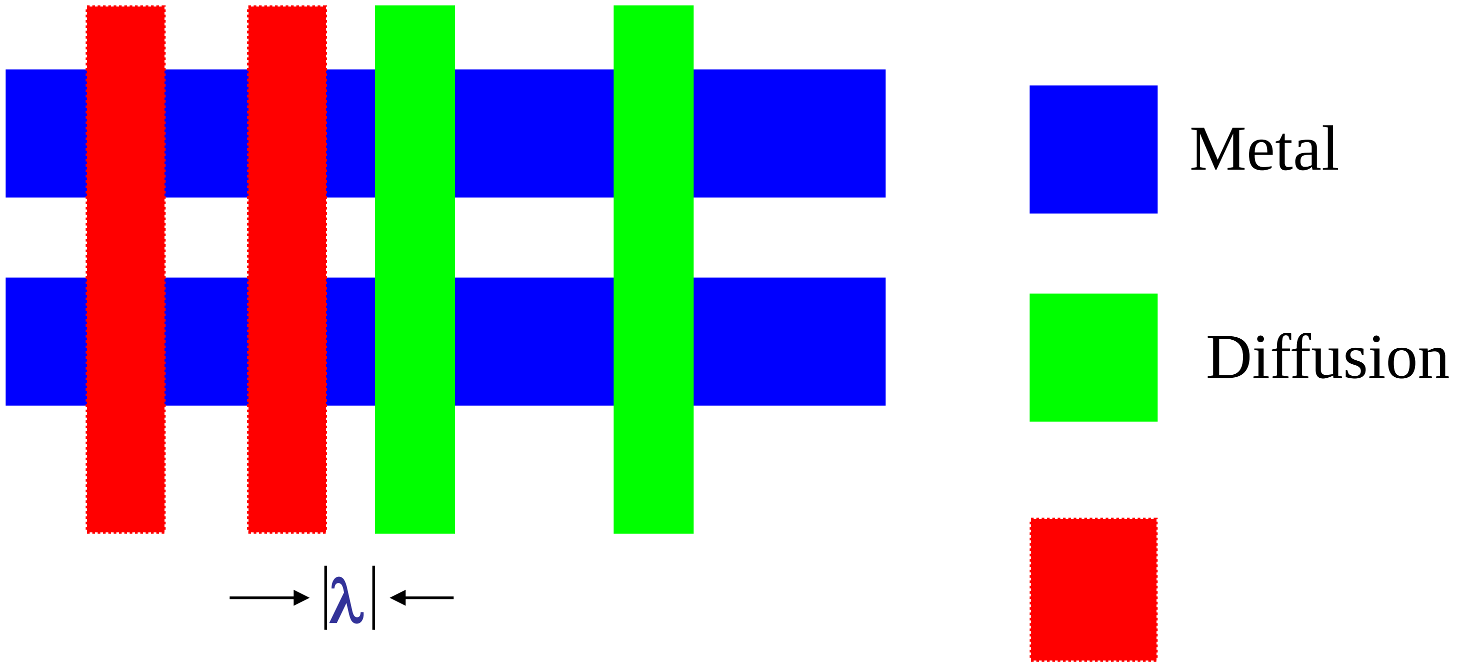
DESIGN RULES

- **PolySi – PolySi space 2λ**
- **Metal - Metal space 2λ**
- **Diffusion – Diffusion space 3λ To avoid the possibility of their associated regions overlapping and conducting current**



DESIGN RULES

- **Diffusion – PolySi space λ To prevent the lines overlapping to form unwanted capacitor**
- **Metal lines can pass over both diffusion and polySi without electrical effect. Where no separation is specified, metal lines can overlap or cross**



DESIGN RULES

- **Metal lines can pass over both diffusion and polySi without electrical effect**
- **It is recommended practice to leave λ between a metal edge and a polySi or diffusion line to which it is not electrically connected**

- **Recall**
  - **poly-poly spacing** **2λ**
  - **diff-diff spacing** **3λ (depletion regions tend to spread outward)**
  - **metal-metal spacing** **2λ**
  - **diff-poly spacing** λ

Butting Contact

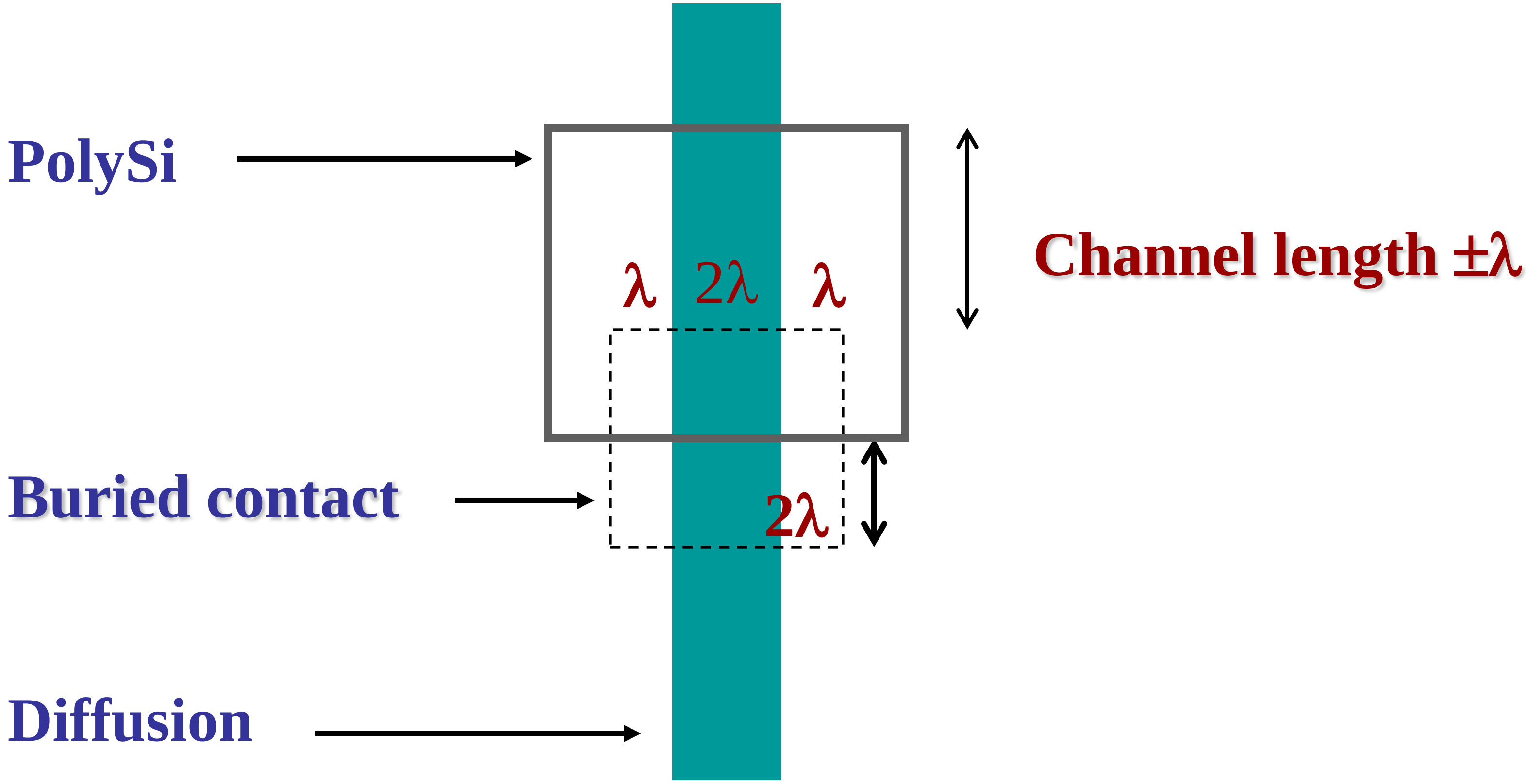
The gate and source of a depletion device can be connected by a method known as **butting contact.** Here metal makes contact to both the diffusion forming the source of the depletion transistor and to the polySi forming this device's gate.

Advantage:

No buried contact mask required and avoids associated processing.

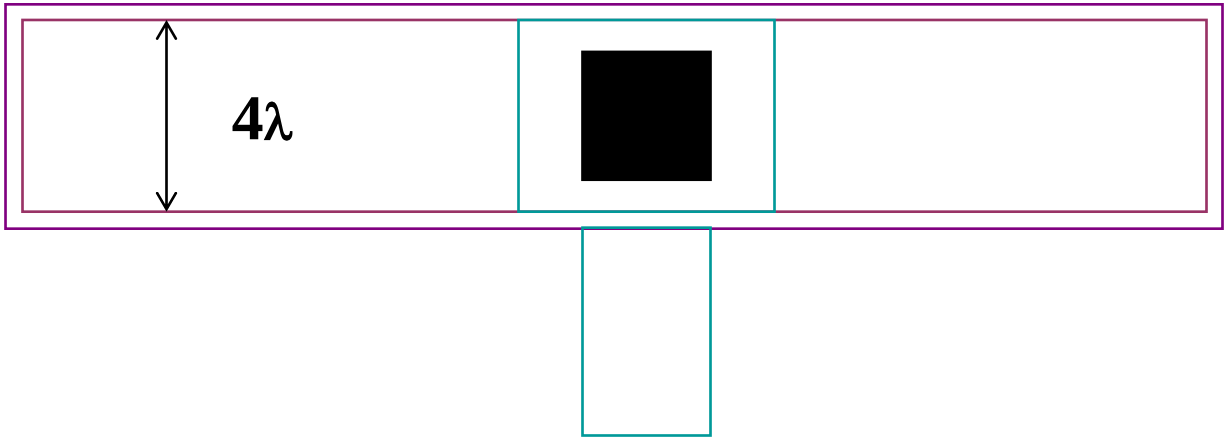
Buried Contact

Here gate length is depend upon the alignment of the buried contact mask relative to the polySi and therefore vary by ±λ.



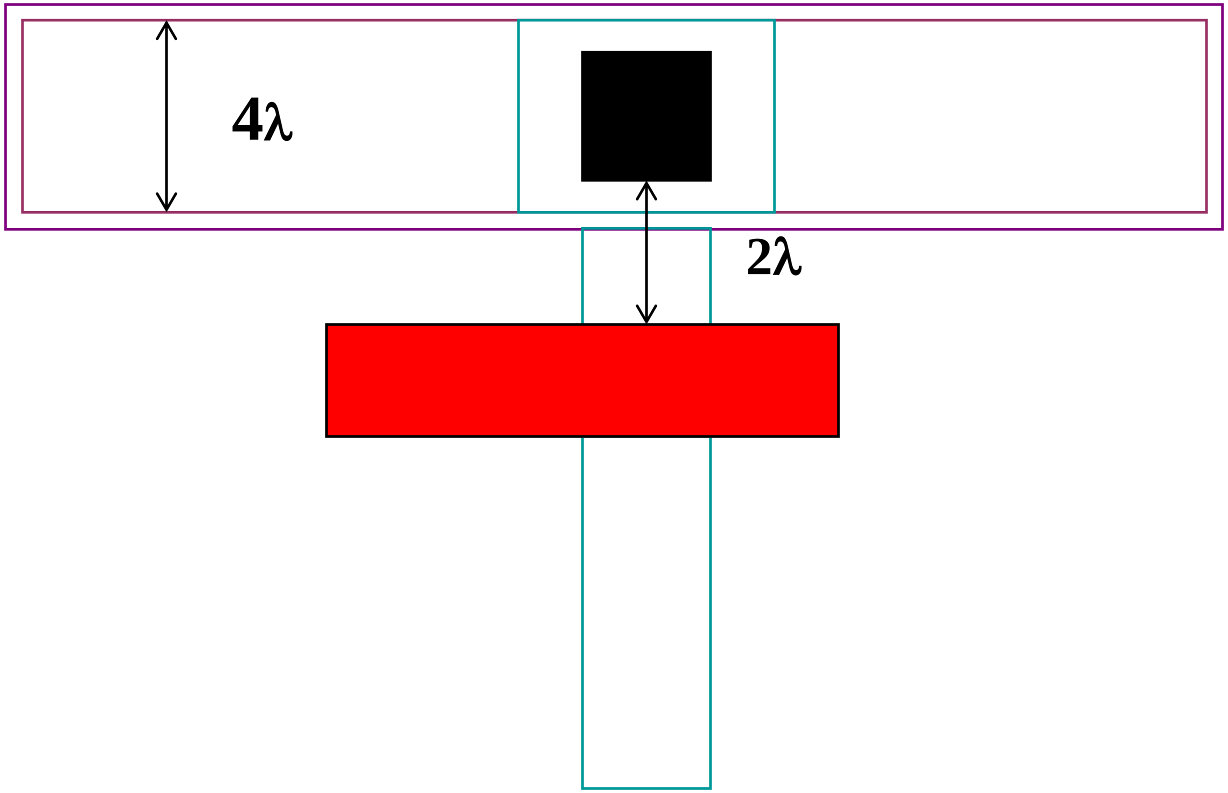
Contact Cut

- **Metal connects to polySi/diffusion by contact cut.**
- **Contact area: 2 λ X 2 λ**
- **Metal and polySi or diffusion must overlap this contact area by l so that the two desired conductors encompass the contact area despite any mis-alignment between conducting layers and the contact hole**



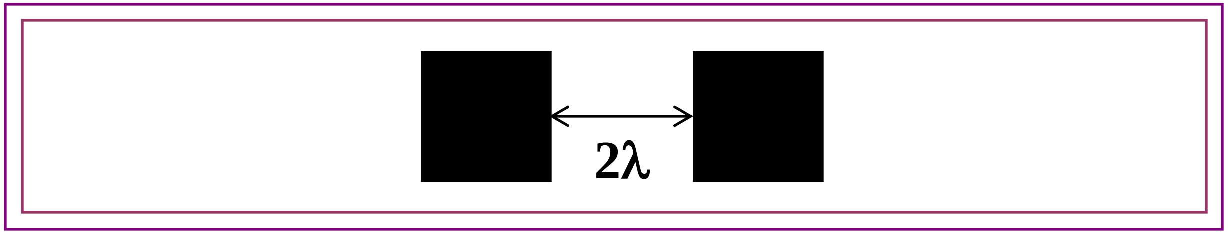
Contact Cut

- **Contact cut – any gate: 2 λ apart**
- **Why? No contact to any part of the gate.**

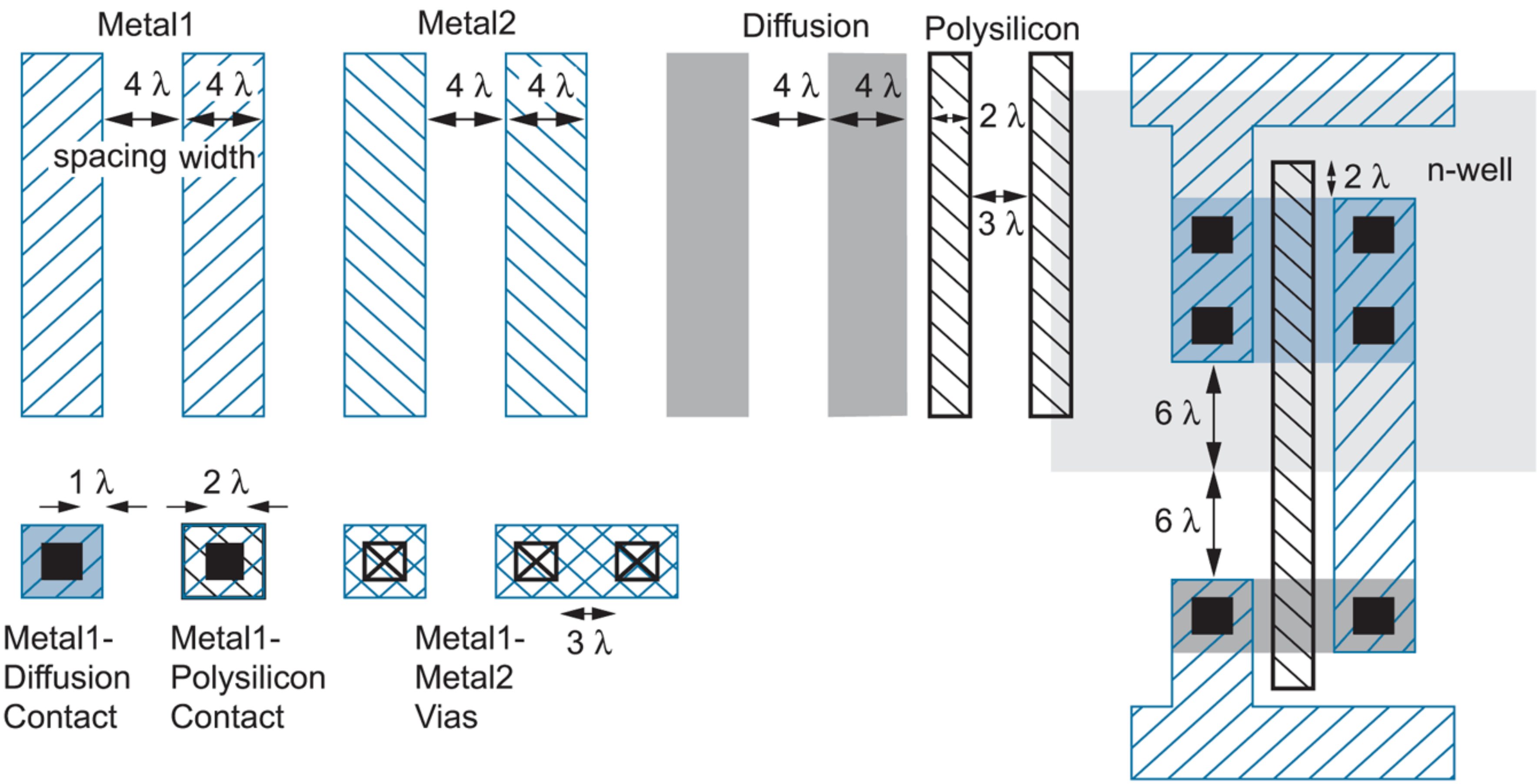


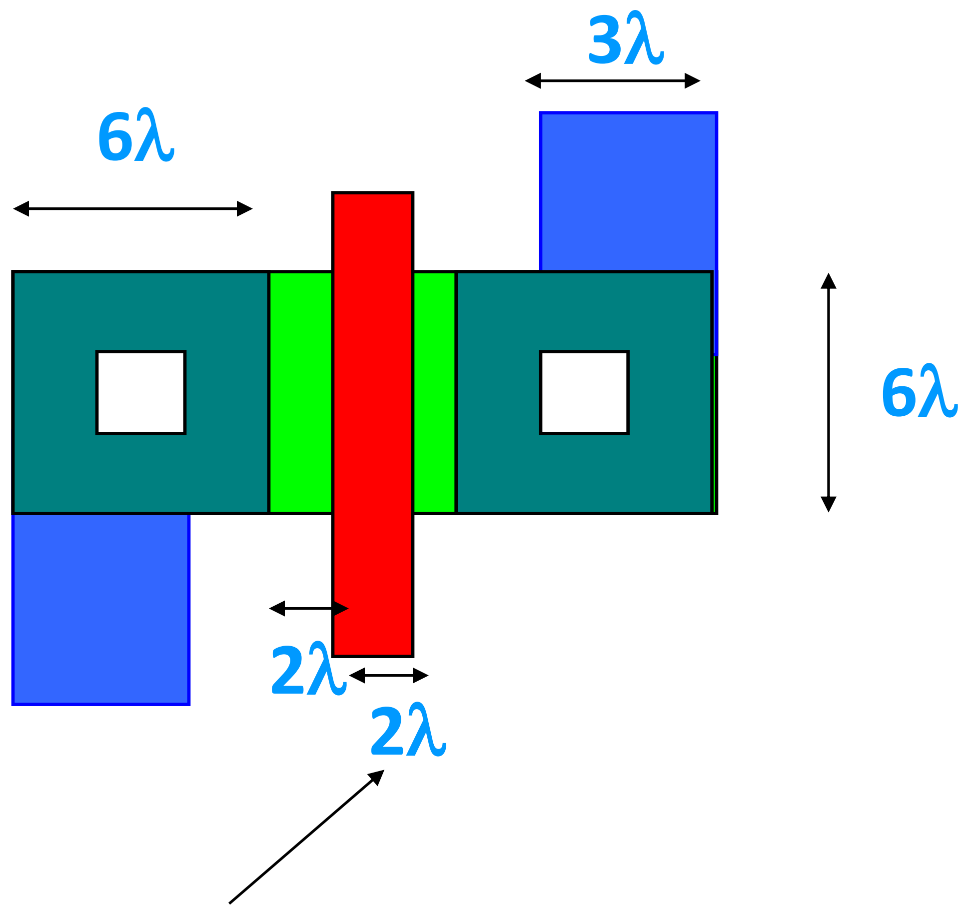
Contact Cut

- Contact cut – contact cut: 2 λ apart
- Why? To prevent holes from merging.



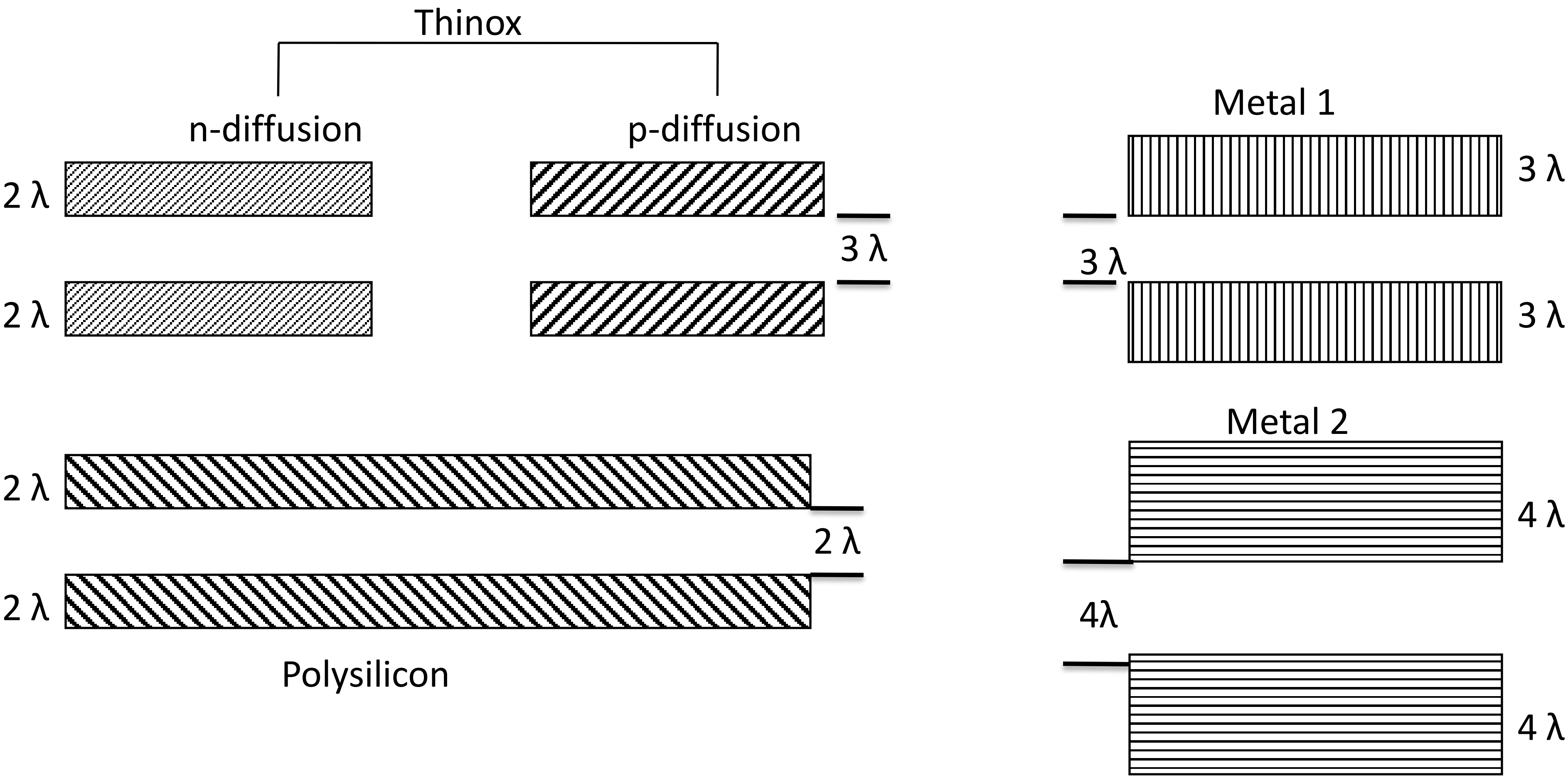
DESIGN RULES





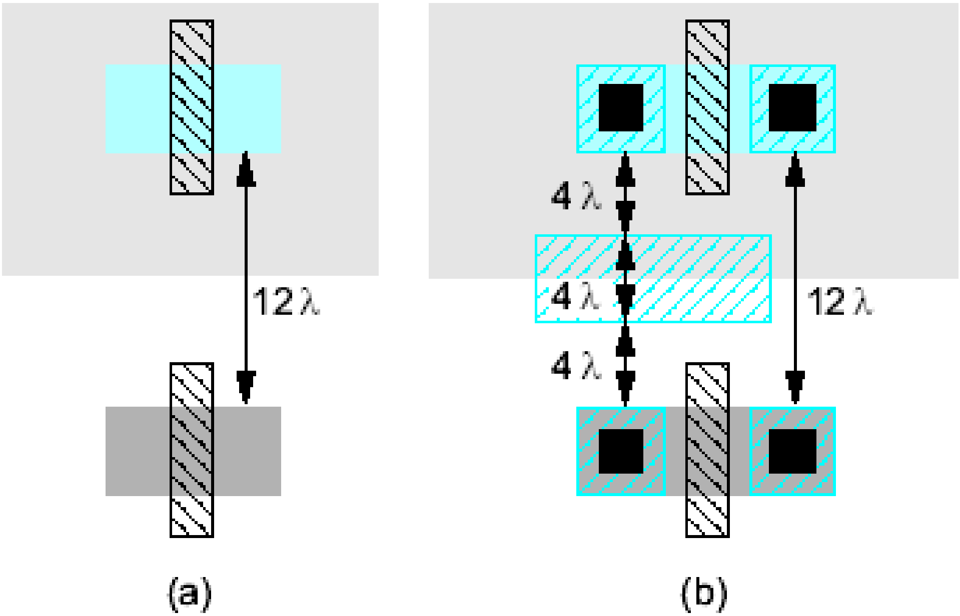
All device mask dimensions are based on multiples of λ, e.g., polysilicon minimum width = 2λ. Minimum metal to metal spacing = 3λ

DESIGN RULES



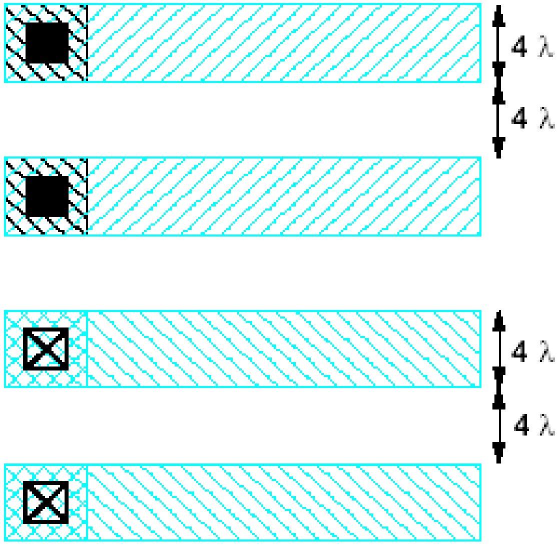
DESIGN RULES

- Wells must surround transistors by 6 λ
  - Implies 12 λ between opposite transistor flavors
  - Leaves room for one wire track

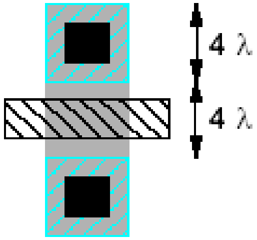


DESIGN RULES

- A *wiring track* is the space required for a wire
  - 4 λ width, 4 λ spacing from neighbour = 8 λ pitch
- Transistors also consume one wiring track



(a)

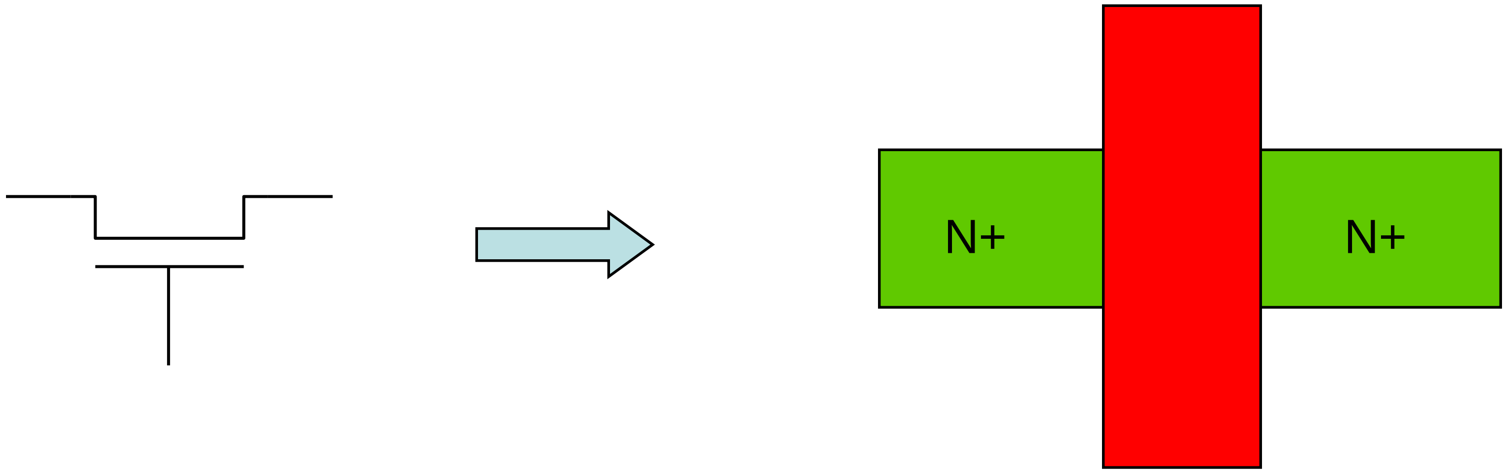


(b)

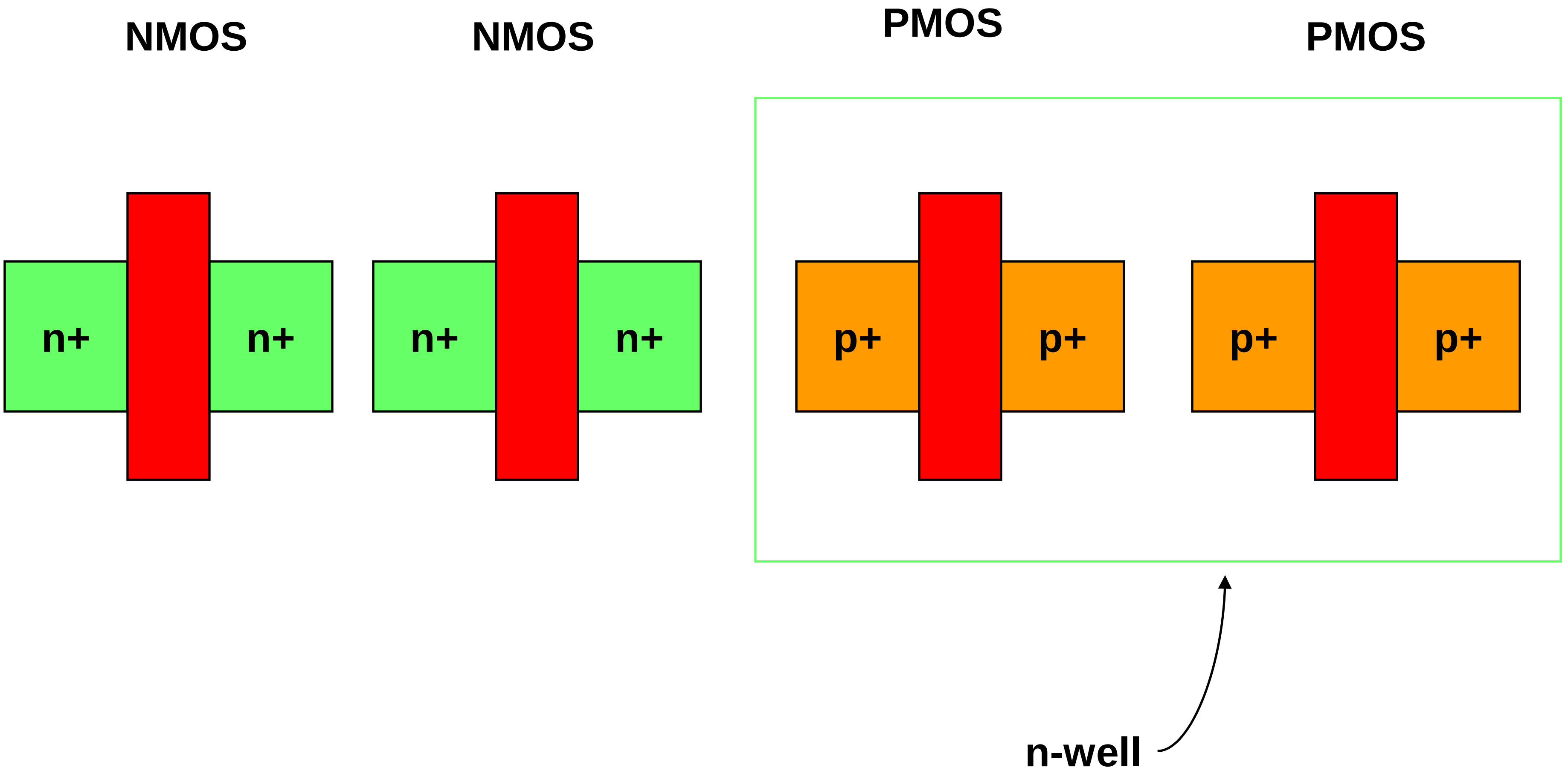
LAYOUTS

- **Layer Types**
  - p-substrate
  - n-well
  - n+
  - p+
  - Gate oxide
  - Gate (polysilicon)
  - Field Oxide
    - Insulated glass
    - Provide electrical isolation

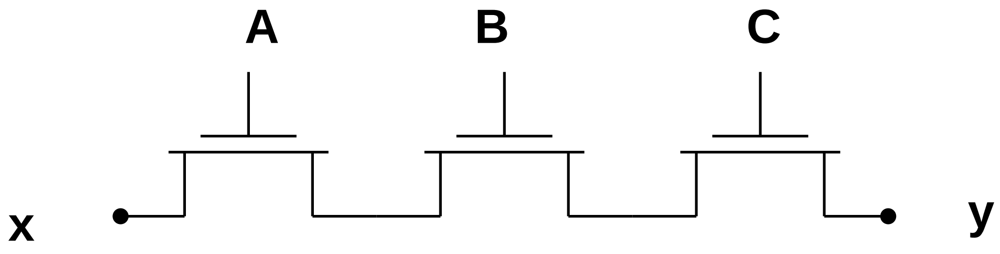
LAYOUTS

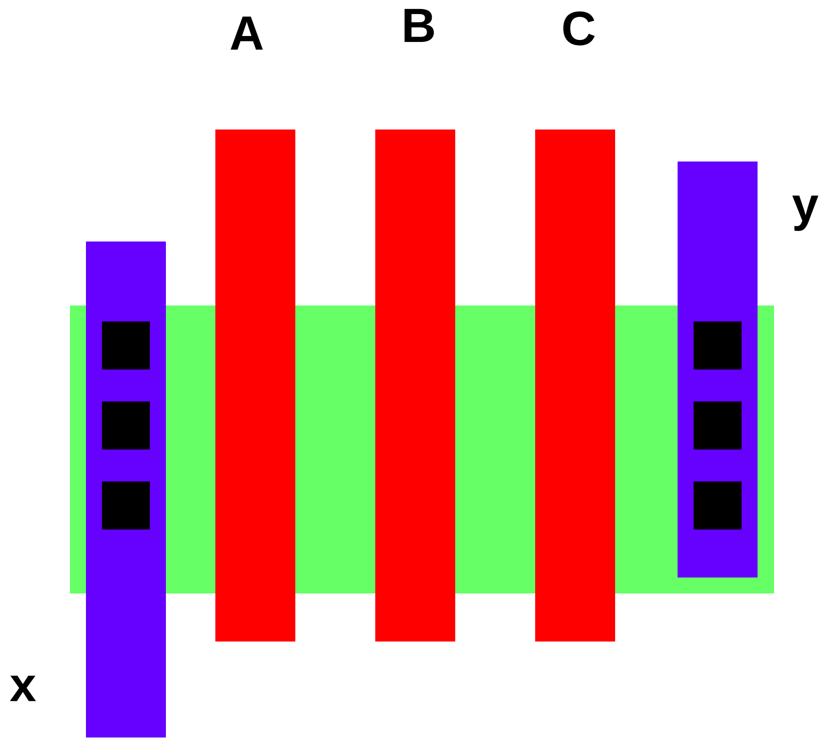


Top view of the FET pattern

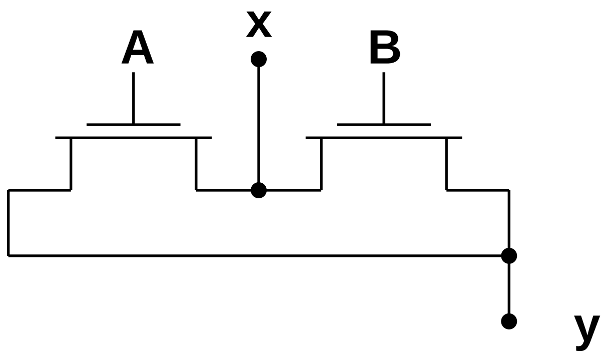


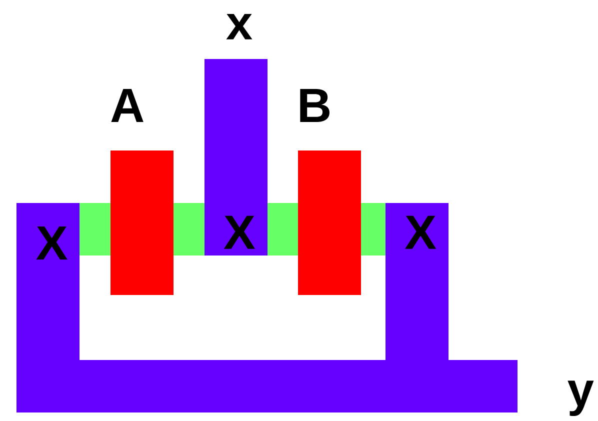
Designing MOS Arrays

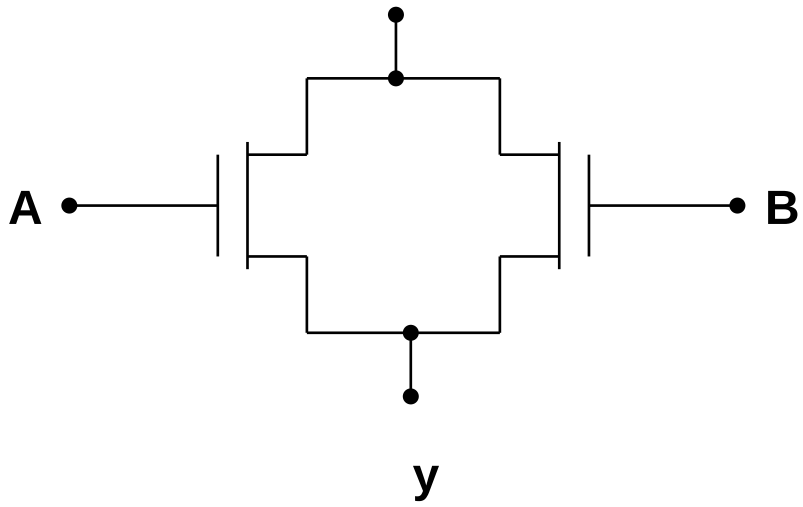


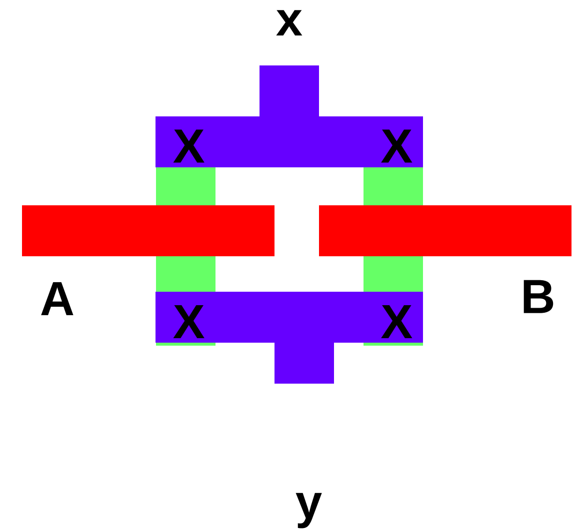


Parallel Connected MOS Patterning

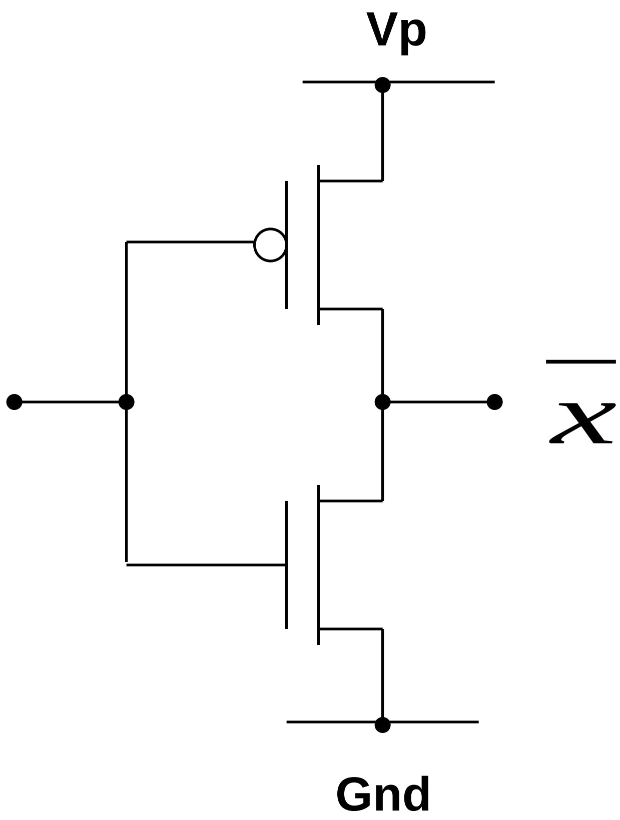


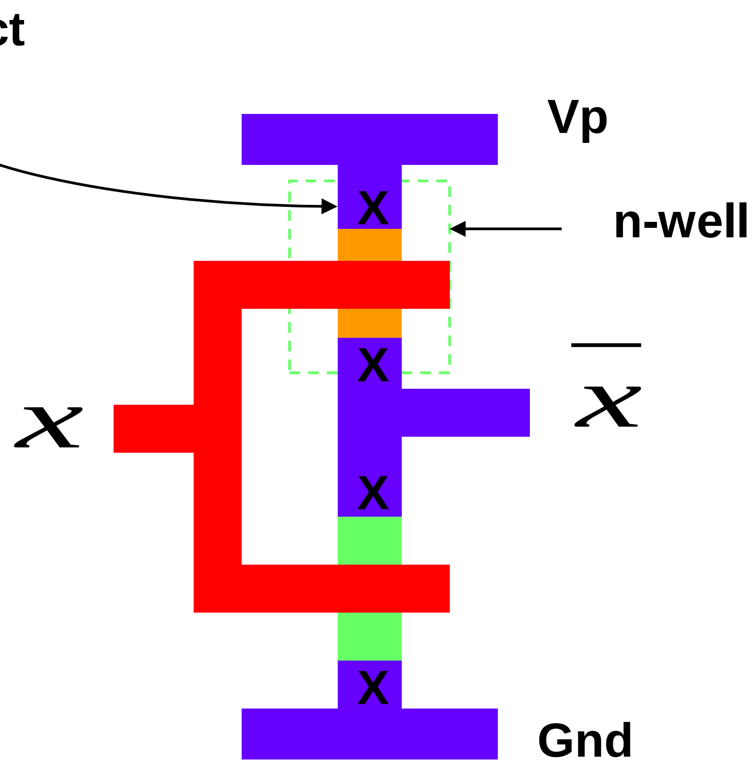




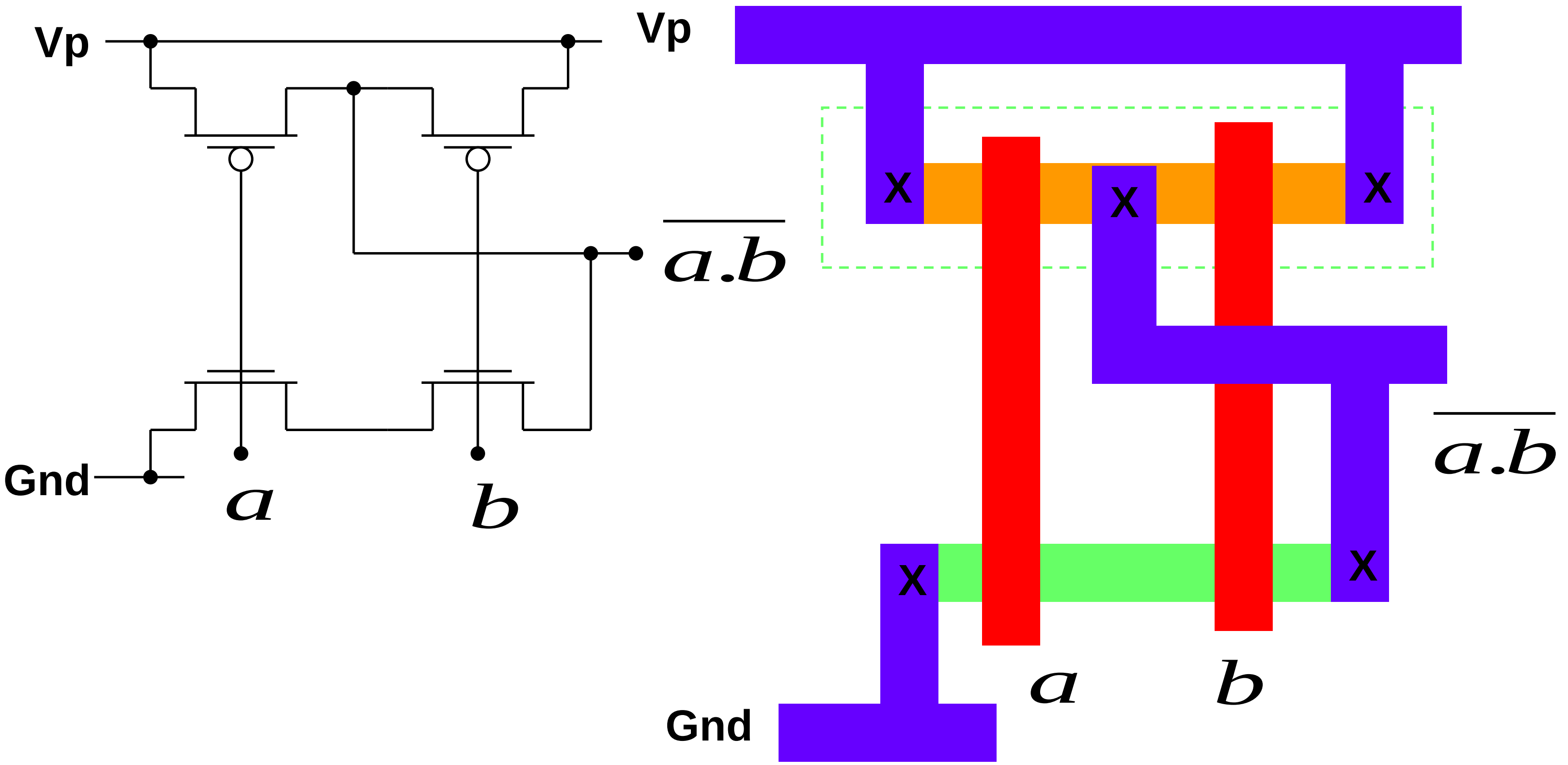


The CMOS NOT Gate

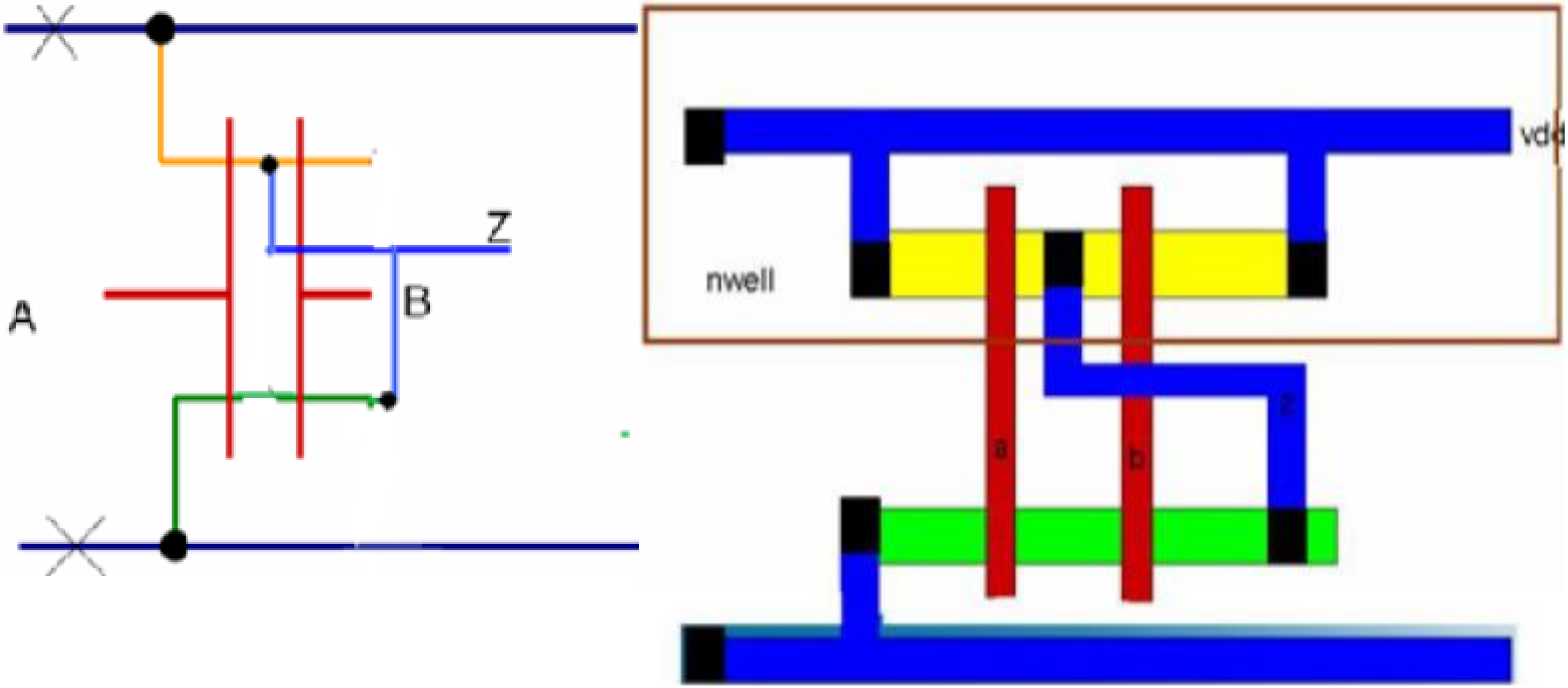




The CMOS NAND Gate



The CMOS NAND Gate



The CMOS NOR Gate