



STONERIDGE ELECTRONICS PCB REQUIREMENTS

Doc. no: 1124-P01582 15

Document number: 1124-P01582 15

Date: 2 January 2020

Document issued by: Lars Wahlstrom / Approved by: Stefan Olofsson

PROCUREMENT DOCUMENTATION

This document is the property of STONERIDGE ELECTRONICS division.

It is owned, maintained, updated and approved by the Procurement Department of Stoneridge Electronics division. Stoneridge Electronics PCB Requirements is reviewed and validated by Stoneridge Electronics PCB Commodity Team.

These requirements are valid, globally, for Stoneridge Electronics divisions Printed Circuit Boards. Certain designs may need AABUS (As Agreed between User and Supplier).

Document overview, contents and revision history:

Chapter:	Title:	Document number:	Revision:
1.	Valid documents	1124-P01582	15
2.	PCB manufacturer – requirements	-"-	-"-
3.	Tolerance requirements for PCBs	-"-	-"-
4.	Laminate & Solder mask	-"-	-"-
5.	Surface treatment (HASL, ENIG etc.)	-"-	-"-
6.	Via hole filling and cover	-"-	-"-
7.	Carbon print – characteristics	-"-	-"-
8.	Etching, Plating, Pattern	-"-	-"-
9.	AOI and Electrical test	-"-	-"-
10.	Repair (rework, touch up)	-"-	-"-
11.	Cleanliness and Surface Isolation Resistance	-"-	-"-
12.	Inspection	-"-	-"-
13.	Moisture and Outgassing	-"-	-"-
14.	Packaging and marking	-"-	-"-
15.	Documentation	-"-	-"-
Appendix 1:	Description of 1076 specification file	-"-	-"-
Appendix 2:	ISO2409 - Adhesion test method	-"-	-"-
Appendix 3:	Revision history	-"-	-"-



STONERIDGE ELECTRONICS PCB REQUIREMENTS

Doc. no: 1124-P01582 15

Document number: 1124-P01582 15

Date: 2 January 2020

Document issued by: Lars Wahlstrom / Approved by: Stefan Olofsson

PROCUREMENT DOCUMENTATION

ABSTRACT

This document is a part of Stoneridge Electronics PROCUREMENT DOCUMENTATION. It specifies general requirements for manufacturing of rigid and flexible PCB's for Stoneridge Electronics.

The PCBs are intended for automotive use and may contain advanced surface- and hole mounted components, press fit connectors and pins as well as riveted, bolted and snap-fit components as well as HDI design.

The document is valid for STONERIDGE ELECTRONICS, their subsidiaries and PCB manufacturers used by STONERIDGE ELECTRONICS.

Manufacturers and distributors of STONERIDGE ELECTRONICS PCB's shall conform to what is stated in this document and documents and standards referred to.

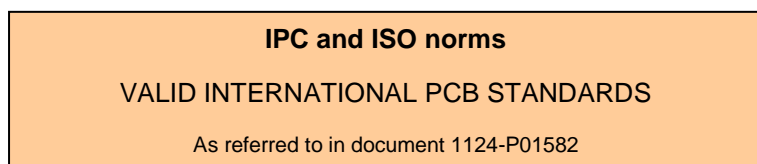
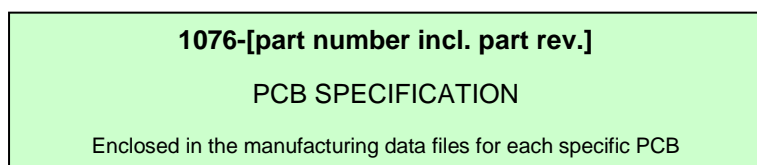
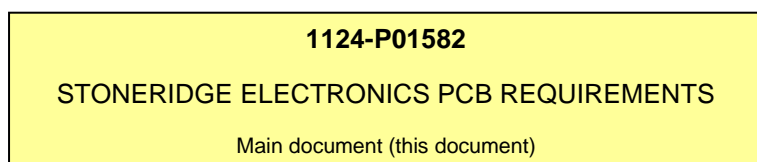
1 VALID DOCUMENTS

1.1 STONERIDGE ELECTRONICS documents:

1124-P01582 STONERIDGE ELECTRONICS PCB REQUIREMENTS (this document)

1076-[part number incl. revision status]+[revision status on document] Part number specification and info. This document is included as a text file in the manufacturing data files for each specific PCB.

1.2 Document structure





STONERIDGE ELECTRONICS PCB REQUIREMENTS

Doc. no: 1124-P01582 15

Document number: 1124-P01582 15

Date: 2 January 2020

Document issued by: Lars Wahlstrom / Approved by: Stefan Olofsson

1.3 Valid standards (latest editions):

IPC 6011	Generic Performance Specification for Printed Boards
IPC 6012D	Qualification and Performance Specifications Rigid
IPC 6012DA	Automotive Supplement to IPC 6012D
IPC 6012D-AM1	Qualification and Performance Specification for Rigid Printed Boards (class 3)
IPC 6013	Qualification and Performance Specifications - Flex
IPC 6016	Qualification and Performance Specifications for High Density Interconnect (HDI) Layers and Boards
IPC-A-600	Acceptability of PCBs
IPC-SM-840	Qualification and Performance Specification of Permanent Solder mask
IPC 4101	Specification for Base Materials for Rigid and Multilayer Printed Boards
IPC 4104	Specification for High Density Interconnect (HDI) Layers and Boards
IPC 4552	ENIG
IPC 4553	Immersion SILVER
IPC 4554	Immersion TIN
IPC 9252	Electrical test
IPC-TM-650	Test methods
IPC J-STD-001	Requirements for Soldered Electrical and Electronic Assemblies
ISO 2409	Adhesion

NB! All references to IPC standards refer to latest revisions and amendments

[HOME](#)



STONERIDGE ELECTRONICS PCB REQUIREMENTS

Doc. no: 1124-P01582 15

Document number: 1124-P01582 15

Date: 2 January 2020

Document issued by: Lars Wahlstrom / Approved by: Stefan Olofsson

PROCUREMENT DOCUMENTATION

2. PCB MANUFACTURER – REQUIREMENTS

2.1 General

These requirements are valid, whether the Supplier is the manufacturer of the PCB's, or act as a distributor (retailer/representative). Suppliers acting as distributors are responsible for the implementation and understanding of these requirements at their contracted suppliers.

2.2 Stoneridge Electronics as your customer

Stoneridge Electronics shall be classified by their manufacturing suppliers and distributors as an **automotive tier one customer**. Parts delivered to Stoneridge Electronics shall meet applicable automotive standards. It is therefore expected and required that the manufacturer and distributor have a thorough understanding and knowledge of the quality and reliability demands placed on PCB's used in automotive applications.

2.3 Manufacturing sites and sub-contractors

The Supplier is not allowed to manufacture parts to the Stoneridge Electronics at any other manufacturing site/sites than those audited and approved by Stoneridge Electronics 2nd party auditor. The use of sub-contractors for major manufacturing processes is not allowed without permission by Stoneridge Electronics. Stoneridge Electronics will only permit sub-contractors that are IATF16949 certified, and fully conforms to Stoneridge Electronics requirements and that receive at least B-rating in Stoneridge Electronics supplier audit.

2.4 Manufacturing capability and critical parameters

Critical dimensions/parameters will be indicated in drawings and this document and conformity shall be proven in PPAP or AABUS.

2.5 UL Approval

All Stoneridge Electronics PCB manufacturers shall be **recognized in the UL Online Certification Database (UL file number) and shall have appropriate UL approvals corresponding to the technology and materials in use**. All Stoneridge Electronics PCB's shall be **manufactured with UL94-V0 approved materials**.

Customer critical parameter: Shall be proven in PPAP by copies of appropriate UL cards.

2.6 Design review

The PCB manufacturer shall perform a design review of all new and revised PCBs.

In the case of a deviation between requirements, specification and manufacturing documentation the manufacturer is responsible for informing Stoneridge Electronics and await instruction.

The manufacturer shall, after inspection of the specification and manufacturing data, and before manufacturing starts, take exception in writing of the cases where pertinent norms cannot be applied. In such case, the manufacturer shall await instruction from Stoneridge Electronics. The design review requires the manufacturer to be in possession of state of the art DFM tools



STONERIDGE ELECTRONICS PCB REQUIREMENTS

Doc. no: 1124-P01582 15

Document number: 1124-P01582 15

Date: 2 January 2020

Document issued by: Lars Wahlstrom / Approved by: Stefan Olofsson

2.7 Gerber data preparation v.s. panelized PCB

When a printed circuit board need to be panelized, Stoneridge Electronics will provide the panelized Gerber data. This must be used by the PCB manufacturer.

PCB manufacturers are not allowed to make their own panelized versions.

2.8 Workmanship

PCBs shall be professionally manufactured and also meet demands that are not specifically stated but may be regarded to be the common practice. PCB's shall meet the acceptance criteria in **IPC-A-600**.

2.9 Material shelf life

The PCB manufacturer shall guarantee a shelf life of minimum 1 year, from manufacturing date, for HASL, LF HASL and ENIG. The PCB manufacturer shall guarantee a shelf life of minimum 6 month, from manufacturing date, for Immersion Ag and Immersion Sn.

2.10 Non-conforming material

The PCB manufacturer is not allowed to send any non-conforming material to Stoneridge Electronics without requesting a written approval. A reliability analysis and a description of the consequences shall follow this request. Cross out (X-out) boards in panels are not allowed.

2.11 IPC Class 3 PCB's

PCB's specified as IPC class 3 shall be manufactured and documented according to **IPC-6012 D, IPC 6012D-AM1 and IPC-6012 DA**. Manufacturers shall have a valid **IPC 6012/IPC-A-600 Qualified Manufacturers Listing**, issued by IPC.

[HOME](#)

PROCUREMENT DOCUMENTATION

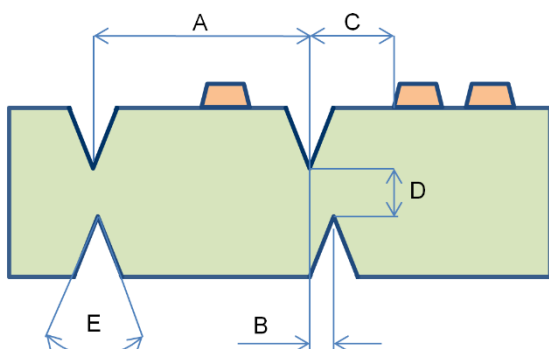
3. TOLERANCE REQUIREMENTS

3.1 Outline and cut out dimensions:

Required tolerance: $\pm 0,10$ mm for routing and punching.

For outlines and cut-outs, routing or punching may be used according to what is most cost efficient. AABUS = Stoneridge Electronics Procurement PCB commodity manager.

3.2 Scoring (V-cut) for aluminium laminate:



Feature type		Nom (mm)	Min (mm)	Tolerance +/- (mm)
Score line and spacing	A	5	3	0.10
Blade offset	B	/	/	0.10
Keep out area	C	/	0.45	0.15
Web	D	0.20	/	+/-0.10
Angle	E	45° - 60°	/	+/-5°
Min board thickness:		0.60mm		
Max board thickness:		3.50mm		

3.3 Scoring (V-cut) for IPC-4101 (FR4) laminate:

Feature type		Nom (mm)	Min (mm)	Tolerance +/- (mm)
Score line	A	5	3	0.10
Blade offset	B	/	/	0.10
Keep out area	C	/	0.45	0.15
Web	D	0.50	/	+/-0.10
Angle	E	30 or 45°	30°	+/-5°
Min board thickness:		1.00mm		
Max board thickness:		3.50mm		



STONERIDGE ELECTRONICS PCB REQUIREMENTS

Doc. no: 1124-P01582 15

Document number: 1124-P01582 15

Date: 2 January 2020

Document issued by: Lars Wahlstrom / Approved by: Stefan Olofsson

3.4 Hole and surface plating

Plating thickness for surface, via holes and through holes shall be minimum average **25 μ m** (according to IPC-6012D Table 3-4 Class 3). *Customer critical parameter: PPAP sample measurements + each manufacturing batch.*

Surface and Hole Copper Plating Minimum Requirements for Micro via (Blind and Buried) shall be minimum average **12 μ m** (according to IPC-6012D Table 3-5 Class 3). *Customer critical parameter: PPAP sample measurements + each manufacturing batch.*

3.5 Hole dimensions

Default tolerance plated/non-plated: $\pm 0,10$ mm

Tolerance for non-plated steering holes: $\pm 0,05$ mm. NB! Maximum hole size is 6,0 mm.

Tolerance $\pm 0,05$ mm for specified ENIG plated holes (including press fit pin holes). NB! Only for ENIG finish, **not** HASL *Customer critical parameter: PPAP Cpk studies with target 1,67*

Tolerance for plated holes with HASL, when specifically specified: $\pm 0,076$ mm

NB! Definition of hole types and sizes as per Stoneridge Electronics:

- Via hole size is the drill size that *shall* be used (manufacturers standard tolerance).
- Plated through hole is the size of the finished hole including specified tolerances.
- Non-plated hole is the size of the finished hole including specified tolerances.

3.6 Hole positions

Default tolerance: $\pm 0,10$ mm.

Specified holes for press fit pins, steering pin holes and micro-via holes: $\pm 0,05$ mm. *Customer critical parameter: PPAP Cpk studies with target 1,67*

Hole to hole tolerance: Required tolerance: $\pm 0,10$ mm

3.7 Micro-via holes

Micro-via holes must be laser drilled.

Default tolerance: $\pm 0,05$ mm. *Customer critical parameter: PPAP Cpk studies with target 1,67*

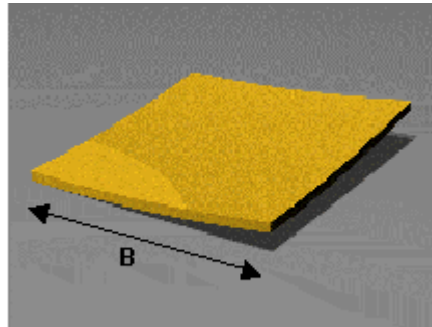
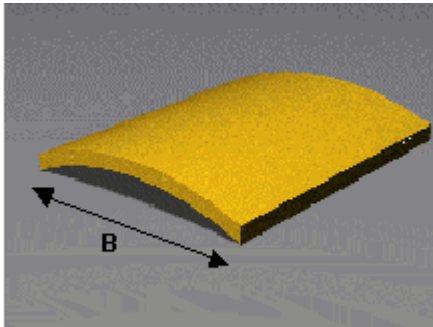
3.8 Pattern registration

Required tolerance: $\pm 0,10$ mm

3.9 Solder mask registration

Default tolerance: $\pm 0,076$ mm. For HDI designs: $\pm 0,050$ mm

3.10 Bow and twist



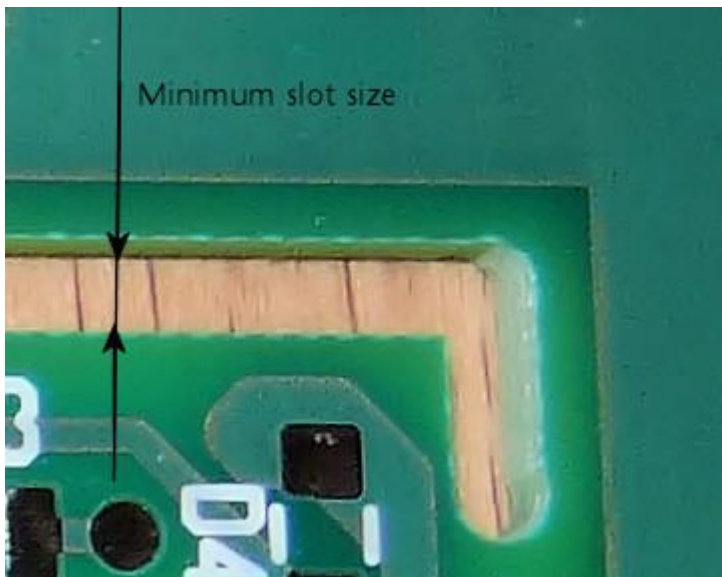
Bow and twist shall not exceed 0,75% (B) for SMD PCBs (measuring method according to IPC-A600 chapter 2.11).

Bow and twist shall not exceed 1,50% (B) for hole mounted PCBs (measuring method according to IPC-A600 chapter 2.11).

3.11 Minimum slot-size

Minimum slot-size for punching: Same as PCB thickness (e.g. 1,6 mm PCB thickness = 1,6 mm punching slot).

Minimum slot-size for routing: 1,2 mm





STONERIDGE ELECTRONICS PCB REQUIREMENTS

Doc. no: 1124-P01582 15

Document number: 1124-P01582 15

Date: 2 January 2020

Document issued by: Lars Wahlstrom / Approved by: Stefan Olofsson

PROCUREMENT DOCUMENTATION

4. LAMINATE, SOLDER MASK, SILK SCREEN AND PEELABLE MASK

4.1 Laminate - general

Laminate used in Stoneridge Electronics PCB's shall meet the specifications and requirements in **IPC-4101**. Laminate and pre-peg for all Stoneridge Electronics PCB's shall meet the flammability requirements according to **UL94-V0**.

4.1.1 Specified laminate

All laminates used for Stoneridge Electronics PCB's shall be classified according to IPC4101 ("slash designations").

For lead free products, **IPC-4101/99 (min. Tg 150)** shall be used. If higher Tg is required **IPC-4101/126 (min. Tg 170)** shall be used.

For non-lead free products, **IPC-4101/21** shall be used.

For HDI designs, the pre-preg should be either a fine mesh or laser drillable pre-preg. NB! Non glass fibre reinforced isolation material (such as RCC) is not allowed.

NOTE: The lead free laminates are chosen for its content of inorganic fillers which is considered to improve not only the CTE value but mechanical stability in general, a characteristic beneficial for reliability in automotive applications.

4.2 Solder mask - general

Solder masks applied on Stoneridge Electronics PCB's shall meet the requirements in **IPC-SM-840 Class H**. Solder masks applied on Stoneridge Electronics PCB's shall meet the flammability requirements according to **UL94-V0**. *Customer critical parameter: Shall be proven in PPAP by copies of appropriate UL cards.*

4.2.1 Adhesion

Adhesion of the solder mask to the PCB shall be according to **ISO 2409** grading 0 or 1. *Customer critical parameter: PPAP sample measurement.*

Adhesion tests according to ISO 2409 shall be performed by AQL on each production batch delivered to STONERIDGE ELECTRONICS.

See [Appendix 3](#) for a description of ISO2409. Proof of adhesion conformity according to ISO2409 shall be included in PPAP documentation.

4.2.2 Approved solder masks

There are three solder mask series approved by STONERIDGE ELECTRONICS, however, **only sub-types complying to IPC-SM-840 Class H**:

- Taiyo PSR4000 series
- Coates/Huntsman PR77 series
- Sun Chemicals XV-501 series

The individual part specification will define if the solder mask shall be matte or glossy.

Once a solder mask version and a solder mask sub-type have been chosen, a change cannot be made without a PCN approval from STONERIDGE ELECTRONICS.

4.2.4 Solder mask thickness

Solder mask thickness shall be as follows:

In accordance with 3.7.3 Solder Mask Thickness in Table 1 in IPC-6012DA.

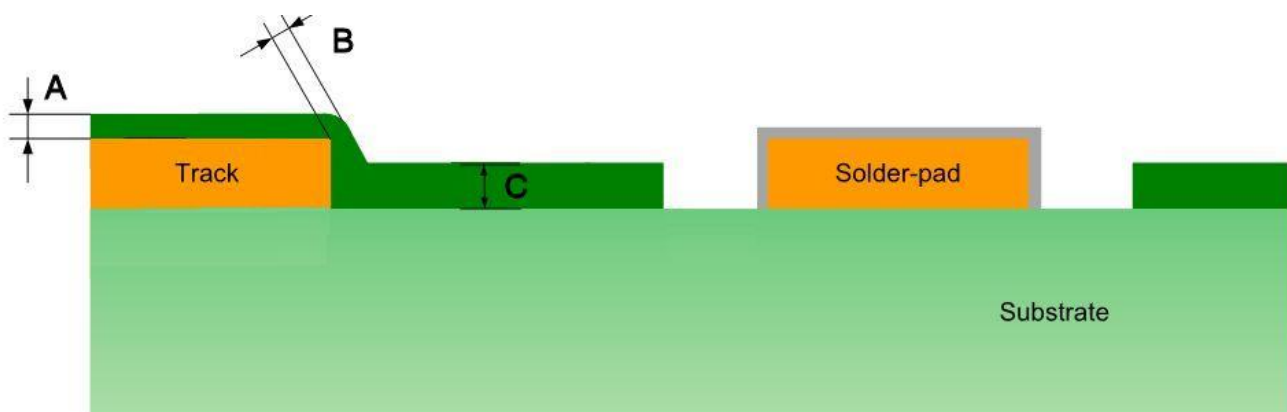
For 18 μ m (1/2 oz.) base copper thickness (/35 μ m finished Cu), Level A in Table 2 is valid.

For 35 μ m (1oz) and 53 μ m (1,5 oz.) base copper thickness (/70 μ m finished Cu), the specification and figure below shall be used:

Minimum thickness over conductor (A): **8 μ m**

Minimum thickness over conductor edge (B): **8 μ m**

Maximum thickness over dielectric area with respect to the surface of SMD land (C): **35 μ m**



For base copper thickness > 70 μ m (2 oz.) /105 μ m finished the solder mask thickness shall be AABUS.

4.2.5 Solder mask hardness

Solder mask shall have a minimum pencil hardness of **5H** (IPC-TM-650 test 2.4.27.2.)

4.2.6 Solder mask colour

Solder mask shall have green colour, unless otherwise specified.

4.3 Peelable Masks

4.3.1 Characteristics:

Characteristics shall have equal characteristics to Lackwerke Peters SD2954 or SD2955.

For lead free PCB's only SD2955 or equivalent is allowed.

4.3.2 Thickness

Minimum thickness: 350 μ m



STONERIDGE ELECTRONICS PCB REQUIREMENTS

Doc. no: 1124-P01582 15

Document number: 1124-P01582 15

Date: 2 January 2020

Document issued by: Lars Wahlstrom / Approved by: Stefan Olofsson

4.4 Silk Screen Print (Legend Print)

Special requirements: The silk screen ink shall withstand the heat from two SMD reflow processes and one wave/selective-solder process without any significant change in colour or texture.

It is common practice to use white silk screen as a light reflector on Stoneridge Electronics instrument panel PCB's. For this reason it is essential that the legend ink does have enough amount of pigment and the print deposit is thick enough to not appear dull due to the underlying green solder mask.

4.5 UL Maximum Operating Temperature (MOT)

UL Maximum Operating Temperature (MOT), unless otherwise specified in the Stoneridge Electronics production drawing, the UL Maximum Operating Temperature (MOT) shall be:

- Minimum 105°C for IPC-4101/99 and IPC 4101/21
- Minimum 130°C for IPC-4101/126

[HOME](#)

PROCUREMENT DOCUMENTATION

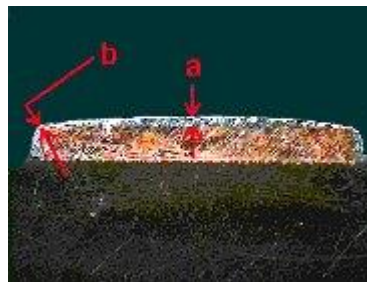
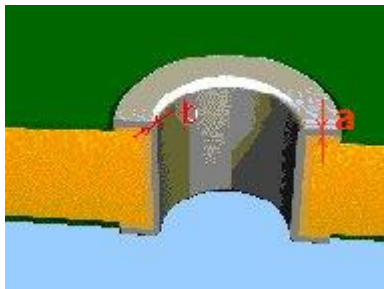
5. SURFACE TREATMENT

5.1 HASL

HASL may be specified as lead free or tin/lead. Lead free HASL shall be SN100C or equivalent.

5.1.1 HASL thickness - Tin/lead and Lead Free

The thickness of the HASL layer shall be within **1 -20 μ m typical** (a) measured on top of the SMD land patterns, For hole mounted components and other types of land patterns the thickness shall be within 1 - 50 μ m (a). HASL plating on hole edges and SMD land pattern edges shall be more than 1 μ m (b) to avoid inter-metallic. See illustrations below. *Customer critical parameter: Shall be proven in PPAP by sample measurements.*



5.1.2 Solder ability and appearance

Solder wetting of the HASL treated surfaces shall be at least 95% of each soldering surface.

5.1.3 Process control

Leaded HASL: Maximum contamination of copper: 0,3%.

Lead free HASL: Maximum contamination of copper: 1%.

Solder-ability tests shall be performed routinely. Solder bath contamination analysis shall be performed on weekly basis as a minimum.

5.2 ENIG (ELECTRO-LESS GOLD PLATING WITH A BARRIER OF CHEMICAL NICKEL)

5.2.1 Applicable standard

ENIG surfaces (including manufacturing processes and testing) shall conform to the standard **IPC-4552**.

Customer critical parameter: Shall be proven in PPAP by sample measurements.

5.2.2 Metal content

The nickel layer shall have a nickel content of at least 99,7%

The gold layer shall have a gold content of at least 99,9%

5.2.3 Age of ENIG PCB's

ENIG PCB's shall not be more than 3 month old when delivered to Stoneridge Electronics.



STONERIDGE ELECTRONICS PCB REQUIREMENTS

Doc. no: 1124-P01582 15

Document number: 1124-P01582 15

Date: 2 January 2020

Document issued by: Lars Wahlstrom / Approved by: Stefan Olofsson

5.3 Immersion SILVER

5.3.1 Applicable standard

Immersion SILVER surfaces (including manufacturing processes and testing) shall conform to the standard **IPC-4553**.

Immersion thickness shall be within the range of **0, 05 to 0, 40µm** *Customer critical parameter: Shall be proven in PPAP by sample measurements.*

5.3.2 Age of Immersion SILVER plated PCB's

Immersion SILVER PCB's shall not be more than 3 month old when delivered to Stoneridge Electronics.

5.4 Immersion TIN

5.4.1 Applicable standard

Immersion TIN surfaces (including manufacturing processes and testing) shall conform to the standard **IPC-4554**.

Immersion thickness shall be minimum **1µm** *Customer critical parameter: Shall be proven in PPAP by sample measurements.*

5.4.2 Age of Immersion TIN plated PCB's

Immersion TIN PCB's shall not be more than 3 month old when delivered to Stoneridge Electronics.

5.5 HARD GOLD (electro plated - for contact areas)

5.5.1 Plating thickness

Nickel: 3 – 10 µm *Customer critical parameter: Shall be proven in PPAP by sample measurements.*

Gold: Minimum 0, 80 µm *Customer critical parameter: Shall be proven in PPAP by sample measurements.*

5.5.2 Metal content

The plated nickel layer shall have a nickel content of at least 99,5%

The plated gold layer shall have a gold content of at least 99,7%

5.5.3 Quality expectations

Cleanliness: No residues or oxides of whatever kind are permitted on the outer surface or between the copper/nickel/gold/silver layers.

[HOME](#)



STONERIDGE ELECTRONICS PCB REQUIREMENTS

Doc. no: 1124-P01582 15

Document number: 1124-P01582 15

Date: 2 January 2020

Document issued by: Lars Wahlstrom / Approved by: Stefan Olofsson

PROCUREMENT DOCUMENTATION

6. VIA HOLE FILLING AND COVER

6.1 Via hole filling

Via hole filling shall conform to **IPC-4761 Type VI b "Filled and Covered Via hole"**. *NB! When the term "Plugged" is used in certain Stoneridge Electronics documentation, it is equal to "Filled" (IPC designation).*

6.1.1 Default filling material

Default filling material for Stoneridge Electronics PCB's is **Taiyo PF9** or a filling material with the same chemical/mechanical/electrical characteristics (AABUS).

NB! It is not allowed to use solder mask ink for IPC-4761 Type VI fillings. Solder mask ink will not create appropriate quality for automotive applications (problems with cracking and leaking plugs and obstacles).

6.1.2 Special filling material

All micro via holes (laser drilled blind and buried) should be copper filled.

Some designs may require epoxy filling, such as: Drilled blind via holes and PTH via holes that are located in thermal pads which in such cases will be indicated and specified on the Stoneridge Electronics production drawings. As a consequence of this type of design, such via hole fillings shall conform to either IPC-4761 Type VI-a (when a pad is located only on one end of the via hole) or IPC-4761 Type V (when a pad is located on both ends of the via hole).

6.1.3 Application of filling materials

Epoxy fillings shall always be vacuum treated to avoid air encapsulations.

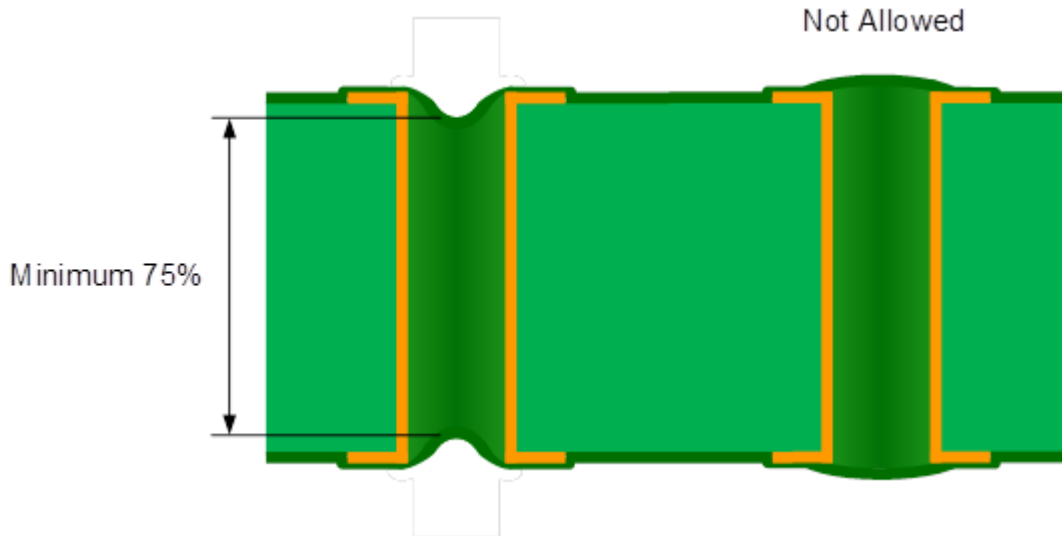
Printing: Selective printing shall be performed by use of steel/aluminum stencils.

Mixing of different filling material on outer layers is not allowed. Filling material applied to cores and inner layers shall always be epoxy.

6.1.4 Appearance and performance of via hole fillings

The filling compound shall not cause bumps or obstacles on the PCB surface that can jeopardize Stoneridge Electronics production processes such as solder paste printing.

The via hole plug filling shall be minimum 75%.



The via filling material should be in the hole only and the thickness of any plugging material over the pads should be minimal.

The PCB manufacturer is allowed to make necessary aperture modifications in order to fulfil design rules. For HASL (including lead free HASL) designs, via hole filling shall be performed before HASL. Rework of via hole filling after HASL is not allowed.

6.2 Tenting

Older PCB specification may indicate "Tenting", the via holes shall than be **filled IPC-4761 Type VI b "Filled and Covered Via hole"**.

6.3 Gerber aperture data

The PCB manufacturer is allowed to make necessary aperture modifications in order to fulfil design rules for via hole filling and cover.

6.4 Copper capped via holes

Copper capped PTH and copper capped buried via holes shall be manufactured according to IPC-4761 Type VII and IPC-6012D Table 3-11 Class 3.

6.5 Copper filled micro via

The maximum allowed depression on a copper filled micro via shall be 15µm, $A \leq 15\mu\text{m}$ in the figure.



PROCUREMENT DOCUMENTATION

7. CARBON PRINT

7.1 CARBON PRINT CHARACTERISTICS

Resistivity ¹⁾: < 20 Ω□

Sheet resistance ²⁾: < 25 Ω□

Solder wetting resistance: min 260 C / 10 seconds

Number of hits: >1 million

Hardness: minimum 4H

Thickness of carbon print: Min 20 um

Insulation resistance: >10MΩ. Test shall be performed at a voltage of 500V DC. N.B. Measurements shall be made with blunted test probes.

¹⁾ Resistivity (Ω□ = ohms/square 4 x 4 mm) : The degree to which the flow of electrical current is opposed using a four point probe.

²⁾ Sheet resistance (Ω□ = ohms/square 4 x 4 mm): Direct (surface) resistance measure using a four point probe.

7.2 Carbon print dimensions for key pads

NB! Notice about dimensions:

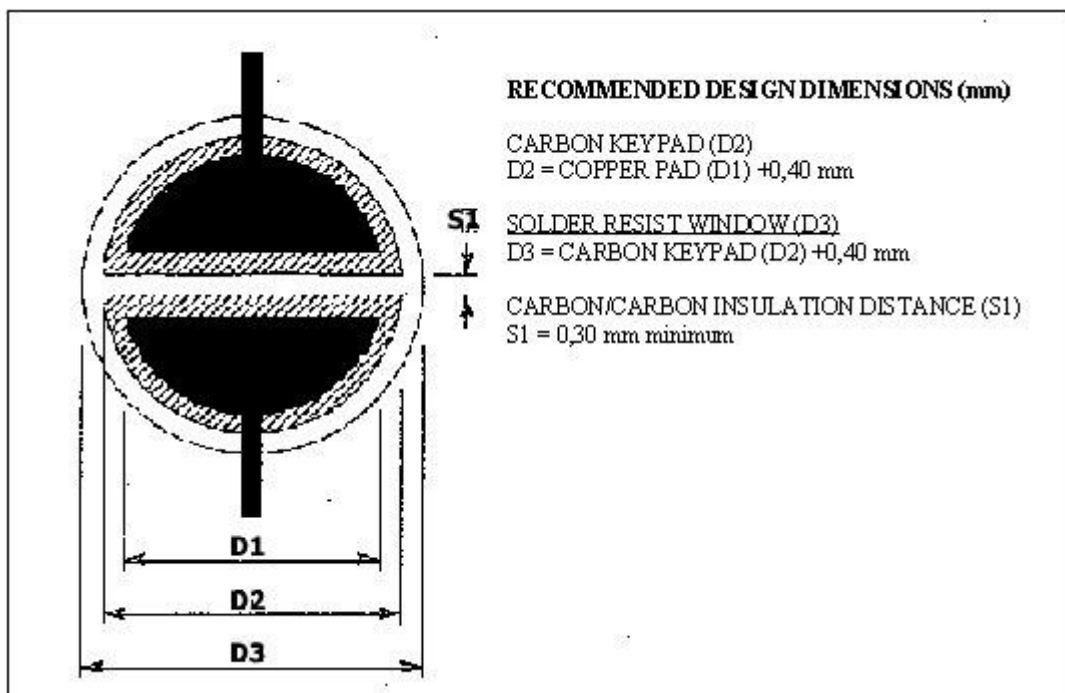
Minimum isolation between carbon printed areas: 0,30 mm.

Minimum isolation between carbon printed area and solder mask: 0,20 mm.

Minimum overlap for carbon over copper pad/pattern: 0,20 mm.

Minimum width for copper track: 0,25 mm.

Please see illustrations below:



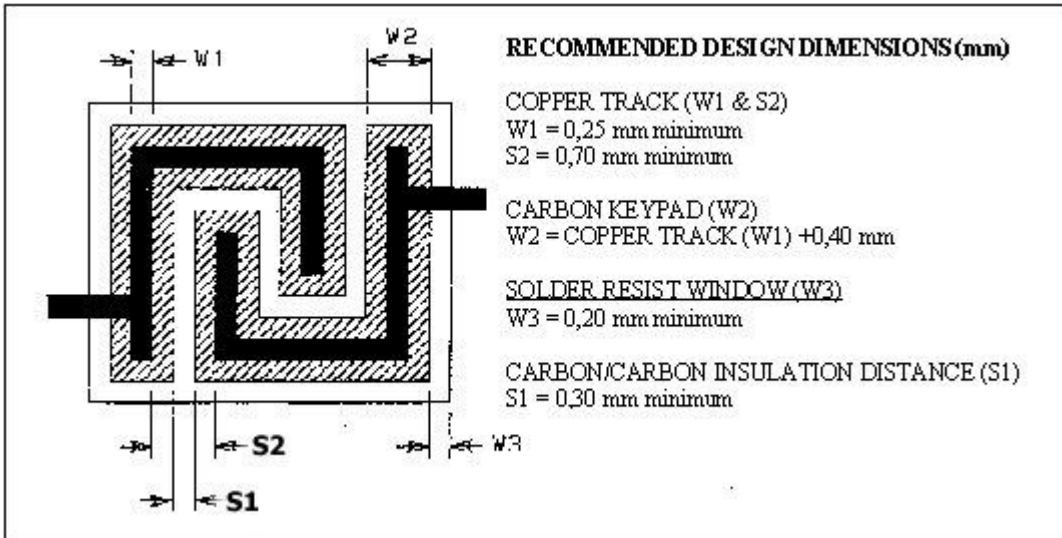
STONERIDGE ELECTRONICS PCB REQUIREMENTS

Doc. no: 1124-P01582 15

Document number: 1124-P01582 15

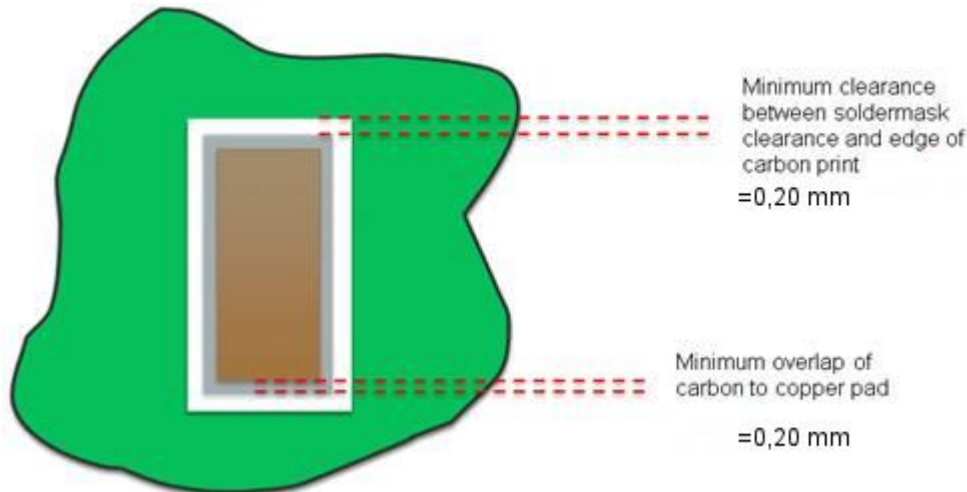
Date: 2 January 2020

Document issued by: Lars Wahlstrom / Approved by: Stefan Olofsson



PCB manufacturers may modify layout AABUS in order to fulfil dimension requirements.

7.3 Carbon print dimensions for zebra strip contact pads



PCB manufacturers may modify layout AABUS in order to fulfil dimension requirements.

7.4 Carbon print conditions

Carbon print must be rich enough to fully cover the underlying tracks.
Please see **NOT OK** vs **OK** examples below:

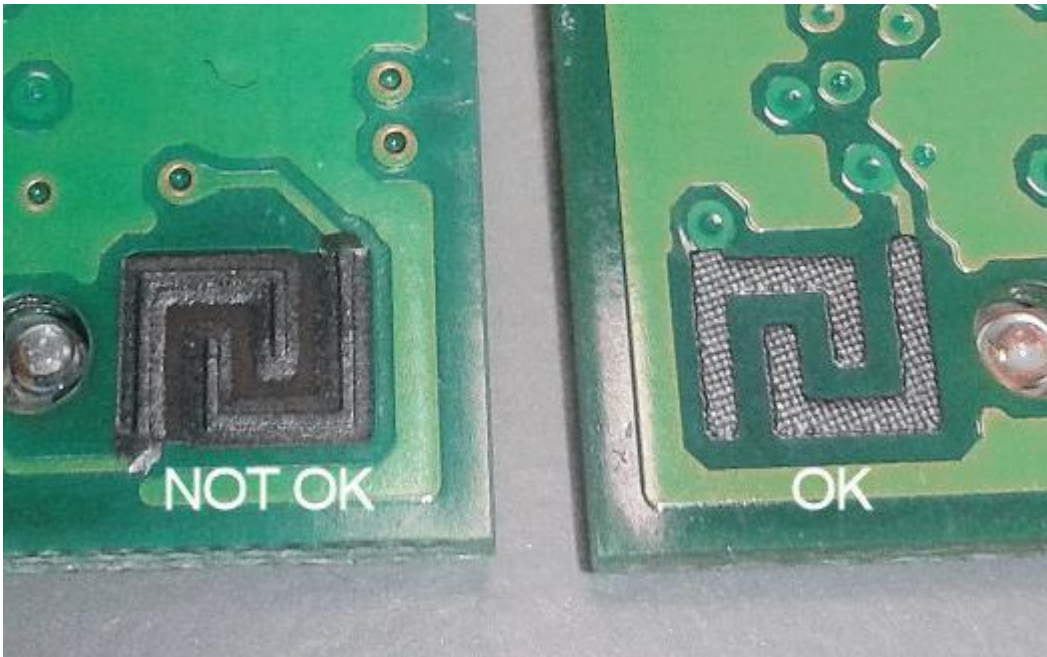
STONERIDGE ELECTRONICS PCB REQUIREMENTS

Doc. no: 1124-P01582 15

Document number: 1124-P01582 15

Date: 2 January 2020

Document issued by: Lars Wahlstrom / Approved by: Stefan Olofsson



[HOME](#)



STONERIDGE ELECTRONICS PCB REQUIREMENTS

Doc. no: 1124-P01582 15

Document number: 1124-P01582 15

Date: 2 January 2020

Document issued by: Lars Wahlstrom / Approved by: Stefan Olofsson

PROCUREMENT DOCUMENTATION

8. ETCHING, PLATING, PATTERN

8.1 Etch factor tolerance

The etch factor shall be minimum 1:1 as defined by IPC-2221B Figure 10-1.

8.2 Pattern - annular rings

Non-function annular rings must not be removed.

[HOME](#)



STONERIDGE ELECTRONICS PCB REQUIREMENTS

Doc. no: 1124-P01582 15

Document number: 1124-P01582 15

Date: 2 January 2020

Document issued by: Lars Wahlstrom / Approved by: Stefan Olofsson

PROCUREMENT DOCUMENTATION

9. AOI - ELECTRICAL TEST - CROSS OUT BOARDS

9.1 AOI test

All STONERIDGE ELECTRONICS PCBs shall be 100% AOI tested. **NB! The AOI test shall be performed on both inner and outer layers.**

Deviation from this demand is AABUS. *Customer critical parameter: AOI test protocols shall be saved for a minimum of five years.*

9.2 Electrical test of PCB's

All STONERIDGE ELECTRONICS PCBs shall be 100% electrically tested according to IPC 9252, the common used parameters to the normal E-test fixture shall be:

Test voltage: 200V~250V

Isolation resistance: 10 Ω ~20 M Ω

Continuity resistance: 30~50 Ω .

Electrical test shall be performed on all types of PCBs, single-sided, PTH and ML. The electrical test shall include **all** nets (tracks and connections).

9.2.1 Marking of electrically tested PCBs

Electrically tested PCBs shall be marked when passing the electrical test. A system of automatic marking in the test fixture is preferred. Type of marking and location of the marking shall be AABUS.

9.3 Cross out boards

STONERIDGE ELECTRONICS does **not** accept cross out boards in panels.

[HOME](#)



STONERIDGE ELECTRONICS PCB REQUIREMENTS

Doc. no: 1124-P01582 15

Document number: 1124-P01582 15

Date: 2 January 2020

Document issued by: Lars Wahlstrom / Approved by: Stefan Olofsson

PROCUREMENT DOCUMENTATION

10. REPAIR (Touch up and rework)

10.1 Tracks and isolation gaps

Welding of open tracks, or tracks with reduced track width, are **not** allowed. These PCBs shall be scrapped.

10.2 Solder mask

Blisters in solder mask and flaked off solder mask are not allowed for repair. Blisters and flaked off solder mask indicate process problems and such affected parts shall be scrapped.

[HOME](#)



STONERIDGE ELECTRONICS PCB REQUIREMENTS

Doc. no: 1124-P01582 15

Document number: 1124-P01582 15

Date: 2 January 2020

Document issued by: Lars Wahlstrom / Approved by: Stefan Olofsson

PROCUREMENT DOCUMENTATION

11. CLEANLINESS AND SURFACE ISOLATION RESISTANCE

11.1 Cleanliness on finished board

Cleaning of the PCB's shall be performed prior to delivery and shall meet the requirements specified in IPC-6012D chapter 3.9

11.2 Cleanliness prior to solder resist application

According to IPC-6012D chapter 3.9.1 (1.56 μ g NaCl/cm²)

11.3 Cleanliness after solder resist, HASL or alternative surface coating application

According to IPC-6012D chapter 3.9.2 (1.56 μ g NaCl/cm²). Proof for ionic contamination test must be indicated in outgoing inspection/audit report and in PPAP documentation. PCB's should be free from dust and routing/scoring debris.

11.4 Moisture and Surface insulation resistance (MIR)

PCBs for PPAP qualification shall be tested according to IPC-6012D chapter 3.8.4 and table 3-17 class 3 (>500 M Ω).

When a MIR test pattern is designed by the customer on the part, the manufacturer shall also measure and specify surface isolation measurement in PPAP documentation.

[HOME](#)



STONERIDGE ELECTRONICS PCB REQUIREMENTS

Doc. no: 1124-P01582 15

Document number: 1124-P01582 15

Date: 2 January 2020

Document issued by: Lars Wahlstrom / Approved by: Stefan Olofsson

PROCUREMENT DOCUMENTATION

12. INSPECTION

12.1 General

All Stoneridge Electronics PCBs shall be inspected before delivery. Inspection shall be performed according to the specification and standards described in this document and according to good workmanship and praxis.

12.2 Operators

Inspectors shall be educated on IPC6012D+DA and IPC-A-600 acceptance criteria. Inspectors shall be educated on Stoneridge Electronics custom specific requirements. Documentation regarding Stoneridge Electronics customer specific requirements shall be available on operator work stations.

12.3 Gloves

Clean gloves shall be used at all time during inspection of Stoneridge Electronics PCBs.

12.4 Documentation

Documentation describing specific demands and characteristics for Stoneridge Electronics PCB's shall be available at inspector work stations.

Inspection reports and statistics shall be presented to Stoneridge Electronics if requested.

[HOME](#)



STONERIDGE ELECTRONICS PCB REQUIREMENTS

Doc. no: 1124-P01582 15

Document number: 1124-P01582 15

Date: 2 January 2020

Document issued by: Lars Wahlstrom / Approved by: Stefan Olofsson

PROCUREMENT DOCUMENTATION

13. MOISTURE & OUTGASSING

13.1 Moisture

The supplier should arrange necessary baking procedures for pre-peg prior to manufacturing and final product before delivery.

13.2 Requirements

The moisture content in the PCB's shall be kept at a level that meets the delivery conditions stated in IPC-6012D chapter 3.8.4 *Moisture and Insulation Resistance* and 3.10.1 *Outgassing*.

[HOME](#)

PROCUREMENT DOCUMENTATION



STONERIDGE ELECTRONICS PCB REQUIREMENTS

Doc. no: 1124-P01582 15

Document number: 1124-P01582 15

Date: 2 January 2020

Document issued by: Lars Wahlstrom / Approved by: Stefan Olofsson

14. PACKAGING AND MARKING

14.1 Packing

PCBs shall be packed in sealed and tight plastic (blister plastic preferred). Individual packages shall normally not contain more than 20 PCBs or panels. Individual packages shall be packed in damage-proof boxes. PCB's transported by sea freight shall have reinforced packages to withstand moisture, heat and salt conditions.

14.1.1 Marking of packages

All individual packages shall have labels and the information on the labels shall contain: STONERIDGE ELECTRONICS part number (including the revision status), number of PCBs in the package, batch number, production year and week.

Main packages shall include information about STONERIDGE ELECTRONICS part number (including the revision status), order number and the amount of PCBs in the package.

14.2 Marking of PCB's

Individual PCBs shall be marked with: Manufacturers ID, production year and week, UL 94V-0 approval and electrical test proofing.

14.3 Marking of lead free PCB's and packages

When PCB's are specified as "Lead Free" (see note below) in the 1076- SPECIFICATION TEXT FILE, PCB's as well as packages (individual and main packages) shall be marked with the following symbol:



Other lead free symbols AABUS.

Note: Lead Free at levels defined by the RoHS 2 Directive (Directive 2011/65/EU + latest amendments) and the ELV Directive (Directive 2000/53/EC + latest amendments).

[HOME](#)



STONERIDGE ELECTRONICS PCB REQUIREMENTS

Doc. no: 1124-P01582 15

Document number: 1124-P01582 15

Date: 2 January 2020

Document issued by: Lars Wahlstrom / Approved by: Stefan Olofsson

PROCUREMENT DOCUMENTATION

15. DOCUMENTATION

15.1 PPAP:

PPAP level 3 shall be submitted in electronic format. PPAP documentation and samples shall be submitted according to PPAP Standard Fourth Edition. All PPAP documentation concerning STONERIDGE ELECTRONICS PCBs shall be stored for a minimum of 5 years. All PPAP documentation shall be written in English language. All dimensions and measurement results shall be indicated by metric values. Indications like "Passed" or "OK" are not acceptable in measurement protocols, real values shall be indicated.

15.2 Storage of results, reports, micro sections and similar:

All documents and other properties as a result of test and inspection of STONERIDGE ELECTRONICS PCBs shall be stored for a minimum of 5 years.

15.3 Manufacturing capability results:

Results of capability measurements within the production processes shall be stored for a minimum of 5 years.

15.4 Records of material:

The PCB supplier need to keep records of the following material traceable to produced batches of STONERIDGE ELECTRONICS PCBs:

Laminate: supplier and type, batch #

Solder mask: supplier and type, batch #

Legend ink: supplier and type, batch #

Records shall be stored for a minimum of 5 years.

15.5 Availability of results:

Results of tests and controls made on STONERIDGE ELECTRONICS PCBs as well as manufacturing capability data in connection with the actual PCBs shall be made available to STONERIDGE ELECTRONICS if requested.

[HOME](#)



STONERIDGE ELECTRONICS PCB REQUIREMENTS

Doc. no: 1124-P01582 15

Document number: 1124-P01582 15

Date: 2 January 2020

Document issued by: Lars Wahlstrom / Approved by: Stefan Olofsson

APPENDIX 1:

DESCRIPTION OF 1076- SPECIFICATION TEXT FILE (mainly used by Stoneridge Electronics in Europe and Asia Pacific)

Each PCB file-set contains one specification file that describes the data files and important manufacturing data. These files have the extension **.txt** or **.inf** and are written in plain text format. This document (file) shall always be read before preparing and manufacturing the PCB. Below is an example of the file:

(C) Copyright STONERIDGE ELECTRONICS AB, Sweden
for template change history see section after "end of relevant information"

Document name : PCB SPECIFICATION AND INFORMATION
File name : 1076_400zzzRyy_01_info.txt
Document class : 1076
Part number : 400zzzRyy
Document revision : 01
Date : 20aa-bb-cc
Prepared : TBD
Layout design : TBD
Title: TBD

Please read: STONERIDGE ELECTRONICS PRINTED BOARDS REQUIREMENTS document
1124-P01582 for information of valid documents, general information and
specific demands

This printed board must conform to IPC A 600 except for specific demands
stated in document 1124-P01582

File format: RS274X

FILE DESCRIPTION:
=====

Files for PCB Manufacturer



STONERIDGE ELECTRONICS PCB REQUIREMENTS

Doc. no: 1124-P01582 15

Document number: 1124-P01582 15

Date: 2 January 2020

Document issued by: Lars Wahlstrom / Approved by: Stefan Olofsson

PATTERN

Layer 1 : filename.GBR

Layer 2 : filename.GBR

Layer 3 : filename.GBR

Layer 4 : filename.GBR

Layer 5 :

Layer 6 :

SOLDER MASK

Layer 1 : filename.GBR

Layer 2 : filename.GBR

SILKSCREEN

Layer 1 :

Layer 2 :

PEEL OFF MASK

Layer 1 :

Layer 2 :

CARBON PRINT

Layer 1 : filename.GBR

Layer 2 :

VIA HOLE FILLING

Layer 1 : filename.GBR

OUTLINE AND HOLES (full Board/Panel)

Layer 1 : filename.GBR

COMPONENT PLACEMENT (full Board/Panel)

Layer 1 : filename.GBR

Layer 2 : filename.GBR

Files for Internal Stoneridge Use

SOLDER PASTE

Layer 1 : filename.GBR

Layer 2 : filename.GBR

PROTECTIVE COATING

Layer 1 : filename.GBR

Layer 2 :



STONERIDGE ELECTRONICS PCB REQUIREMENTS

Doc. no: 1124-P01582 15

Document number: 1124-P01582 15

Date: 2 January 2020

Document issued by: Lars Wahlstrom / Approved by: Stefan Olofsson

GLUING DATA

Layer 1 :

Layer 2 :

File format: ASCII

FILE DESCRIPTION:

=====

Files for PCB Manufacturer

DRILL (full Board/Panel)

Layer P-S : filename.DRL

ROUTING (for Panel only)

Layer P-S : filename.ROU

NETLIST

IPC-D-356A : filename.IPC

Files for Internal Stoneridge Use

PICK&PLACE

Layer 1 : filename.PP

Layer 2 : filename.PP

TESTPOINTS

Layer 1 : filename.TP

Layer 2 :

NETLIST

User Friendly : filename.WIR

TECHNICAL SPECIFICATION:

" X " means choice



STONERIDGE ELECTRONICS PCB REQUIREMENTS

Doc. no: 1124-P01582 15

Document number: 1124-P01582 15

Date: 2 January 2020

Document issued by: Lars Wahlstrom / Approved by: Stefan Olofsson

1. BOARD SIZE

No. of boards per panel: ____

Panel size: ____ mm x ____ mm

2. RF OR HIGH FREQUENCY

There will be High Frequency or RF function on the PCB and the PCB shall be manufactured accordingly.

Please see the Outlines and Holes drawing 1077-
 No High Frequency or RF requirements.

3. BOARD TYPE

Single sided

Double Sided

Multilayer: ____ Layers

HDI: ____ + ____ + ____ Layers

Other:

4. MATERIAL

FR-4 IPC-4101/21

FR-4 IPC-4101/99

FR-4 IPC-4101/126

Other:

5. THICKNESS

1.2 mm +/-10%

1.6 mm +/-10%

2.0 mm +/-10%

Other:

6. STACK-UP / BUILD

Free, no specific requirements

Please see the Outlines and Holes drawing 1077-

Signal Impedance ____ ohm at Frequency range ____ Hz *

* Impedance tolerance: +/-10%

7. SURFACE TREATMENT

HASL (Hot Air Level Soldering with Pb) *

HASL SN100C (Lead-free Hot Air Level Soldering) *

ENIG, "soft Gold" (Electroless Gold) *

Immersion Ag, (Immersion Silver) *

Other *

* According to document 1124-P01582



STONERIDGE ELECTRONICS PCB REQUIREMENTS

Doc. no: 1124-P01582 15

Document number: 1124-P01582 15

Date: 2 January 2020

Document issued by: Lars Wahlstrom / Approved by: Stefan Olofsson

8. SOLDER MASK TYPE

- Soldermask according to document 1124-P01582
- Soldermask finish: matte
- Soldermask finish: glossy
- Soldermask finish: not defined
- Soldermask colour: Green

9. SILKSCREEN

- No Print
- White
- Yellow

10. PATTERN

- Max conductor width:
 - Min conductor width: 0.2mm
 - Max spacing:
 - Min spacing: 0.2mm
- Electrical distribution centres (total CU-thickness min 115um):
NB! Isolation width between conductors: 0.60mm +0.08/-0.08mm
- Electrical distribution centres (total CU-thickness min 140um):
NB! Isolation width between conductors: 0.76mm +0.08/-0.08mm

11. CU-THICKNESS

- 35um Finish, include Cu plating (1oz).
- 70um Finish, include Cu plating (2oz).
- 105um Finish, include Cu plating (3oz).
- 140um Finish, include Cu plating (4oz).
- Other:

12. CU-THICKNESS INNER LAYER (Only multi layer)

- 35um (1oz)
- 70um (2oz)
- Other:

13. CONNECTING SURFACES

- none
 - Gold Plated, "hard gold", Au (Electro Plated Gold)
 - Carbon *)
 - Other:
- *) See document 1124-P01582 for specification on carbon print

14. LAY-UP SEQUENCE OUTER LAYER (multi layer only)

- Outerlayer: 1 and 4 / 1 and 6 etc.
- Layer sequence: 1,2,3,4 / 1,2,3,4,5,6 etc.



STONERIDGE ELECTRONICS PCB REQUIREMENTS

Doc. no: 1124-P01582 15

Document number: 1124-P01582 15

Date: 2 January 2020

Document issued by: Lars Wahlstrom / Approved by: Stefan Olofsson

15. DEFAULT HOLE TOLERANCES

x +/- 0.10 mm

_ Other:

16. QUALITY STANDARD

x According to document 1124-P01582

x Class 2 according to IPC-6012D+DA

_ Class 3 according to IPC-6012D+DA

17. WARP AND TWIST TOLERANCES

x According to document 1124-P01582

18. OTHER INFORMATION

x UL-Approval 94V-0

_ MIL-Approval

19. OUTLINES

x Routing or Punching *

_ Scoring (V-cut) *

* According to document 1124-P01582

20. PEEL OFF MASK

_ Yes *

x No

* According to document 1124-P01582

21. VERIFICATION

x Gerber and CAD Netlist comparison, Input-data verification

x Electrical Open- and Short-test, PCB Manufacturing test

_ Other:

22. CLEANLINESS REQUIREMENTS

x According to document 1124-P01582

_ Other:

23. PTH VIA HOLE FILLING AND COVERING *

x Taiyo PF9 filling paste

_ Epoxy filling (e.g. for use with Thermal-via in Solder-pad)

_ Capped PTH via (Thermal-via or Via In Pad), outer layer(s): _____

_ No filling or covering

According to Via Hole Filling file. Supplier is allowed to make necessary aperture modifications in order to fulfil design rules.



STONERIDGE ELECTRONICS PCB REQUIREMENTS

Doc. no: 1124-P01582 15

Document number: 1124-P01582 15

Date: 2 January 2020

Document issued by: Lars Wahlstrom / Approved by: Stefan Olofsson

* According to document 1124-P01582

24. DRYING PRIOR TO PACKING

x According to document 1124-P01582

25. PRESS-FIT PINS

_ Handling of Press-fit pins on holes that are defined in the Panel drawing; 1079-

x No requirement on Press-fit pins

26. PLACEMENT OF MANUFACTURER AND UL MARKING

_ Location is defined in the Component Placement files and identified as "PCB Manufacturing Logo"

x No defined placement, Manufacturer is free to choose area

27. HDI VIA HOLES / IPC-2226 TYPES

x No microvias or buried vias

_ HDI board

Type I

_ Standard microvia, outer layers

_ Microvia in pad, outer layer(s): _____

_ Cu-filled microvia, outer layer(s): _____

Type II

_ Buried via

_ Capped buried via

_ Microvia on capped buried via pad

Type III

_ Cu-filled microvia, inner layer(s): _____

_ Buried microvia, inner layers

_ Staggered microvia

_ Stacked microvia with the capturing microvia Cu-filled

NB! Specifications made by Stoneridge Electronics North America may look different and may be in AutoCad and/or Gerber format, sometimes included as drawing information.

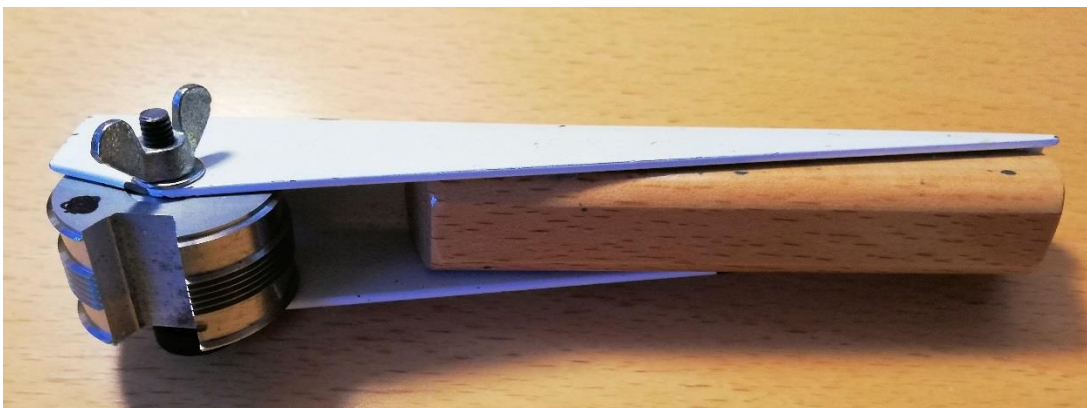
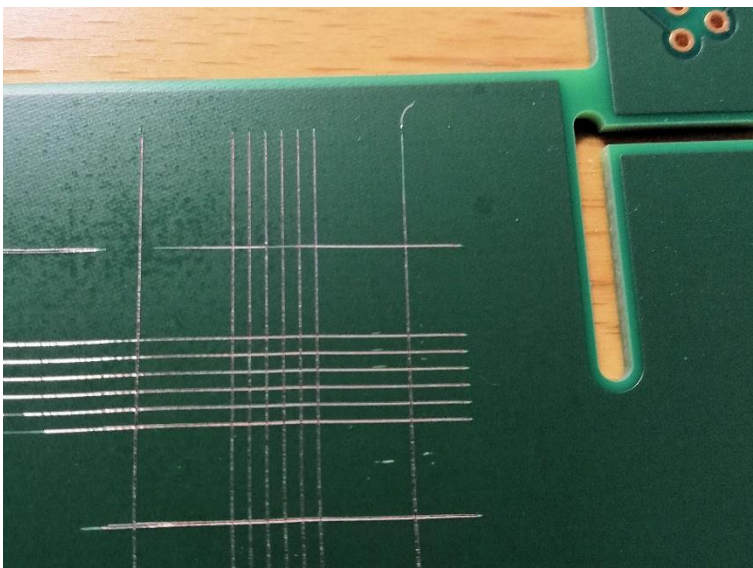
[HOME](#)

PROCUREMENT DOCUMENTATION

APPENDIX 2:

ADHESION TESTS ACCORDING TO ISO 2409

Adhesion tests shall be made according judgement criteria grade 0 or 1 in ISO 2409 or equivalent standard please see pictures below.





STONERIDGE ELECTRONICS PCB REQUIREMENTS

Doc. no: 1124-P01582 15

Document number: 1124-P01582 15

Date: 2 January 2020

Document issued by: Lars Wahlstrom / Approved by: Stefan Olofsson

PROCUREMENT DOCUMENTATION

APPENDIX 3:

Latest revision history for previous revisions of STONERIDGE ELECTRONICS PCB REQUIREMENTS

Doc. nr: 1124-P01582

Rev. 15

Valid from: 2 January 2020

Chapter:	Type of change
All	Document format changed to PDF
1	1.3 IPC standards updated
2	2. General PCB requirements removed
2	2.11 IPC Class 3 requirements added
3	3.2 Aluminums scoring tolerances added
4	4.2.4: Solder mask thickness updated
4	4.3 4.4 New chapters about silk screen and peel able mask
6	Chapter about via hole filling and cover re-written
8	8. New chapter added: Plating, Etching and Pattern
9	9:3 Cross out boards added
Appendix 2	Re-named chapter Adhesion test according to ISO2409
Appendix 3	Re-named chapter Revision history
Appendix gen.	Appendix about PPAP and environmental testing has been removed

[HOME](#)