STRUCTURED ANALOG CMOS DESIGN

Based on the Device Inversion Level

Danica Stefanovic

STATE OF THE ART

→ No general analog design methodology.

→ No general **design approach**.

→ **CAD tools** for simulation, layout generation and post layout verification.

→ Large number of **analog design automation** tools,

but only in the university domain!

→ Few analog design automation tools in industry.

HOW TO

→ Deal with increasing circuit **complexity** ?

→ Deal with very **demanding specifications** sets ?

→ Estimate **technology limits** ?

→ Bridge the gap between **hand-calculations** and simulations ?

→ Use the **device physics understanding** for analog design ?

→ Optimize analog circuits and find the best **trade-offs** ?

→ Develop CAD tools for **analog design assistance** ?

→ **Encapsulate** analog design knowledge ?

THIS WORK

Analog design approach

→ Structured analog design

→ Procedural design

Transistor level design

→ the device inversion level as a key variable

CAD tool for analog design assistance

→ PAD tool

→ BSIM2EKV converter

BASIC CONCEPT

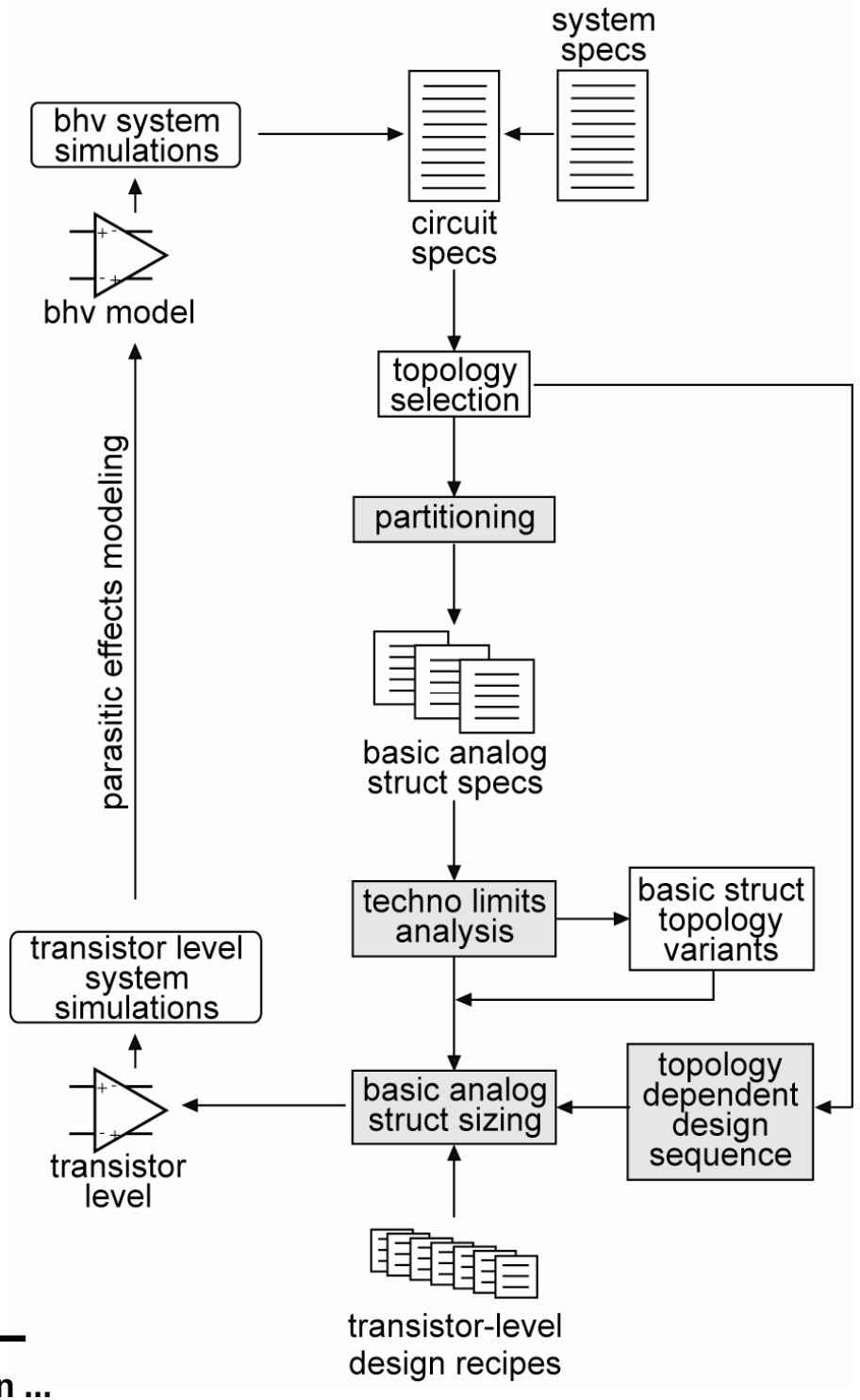
→ **Circuit-level specifications from system-level simulations**

→ **Basic analog structures library**

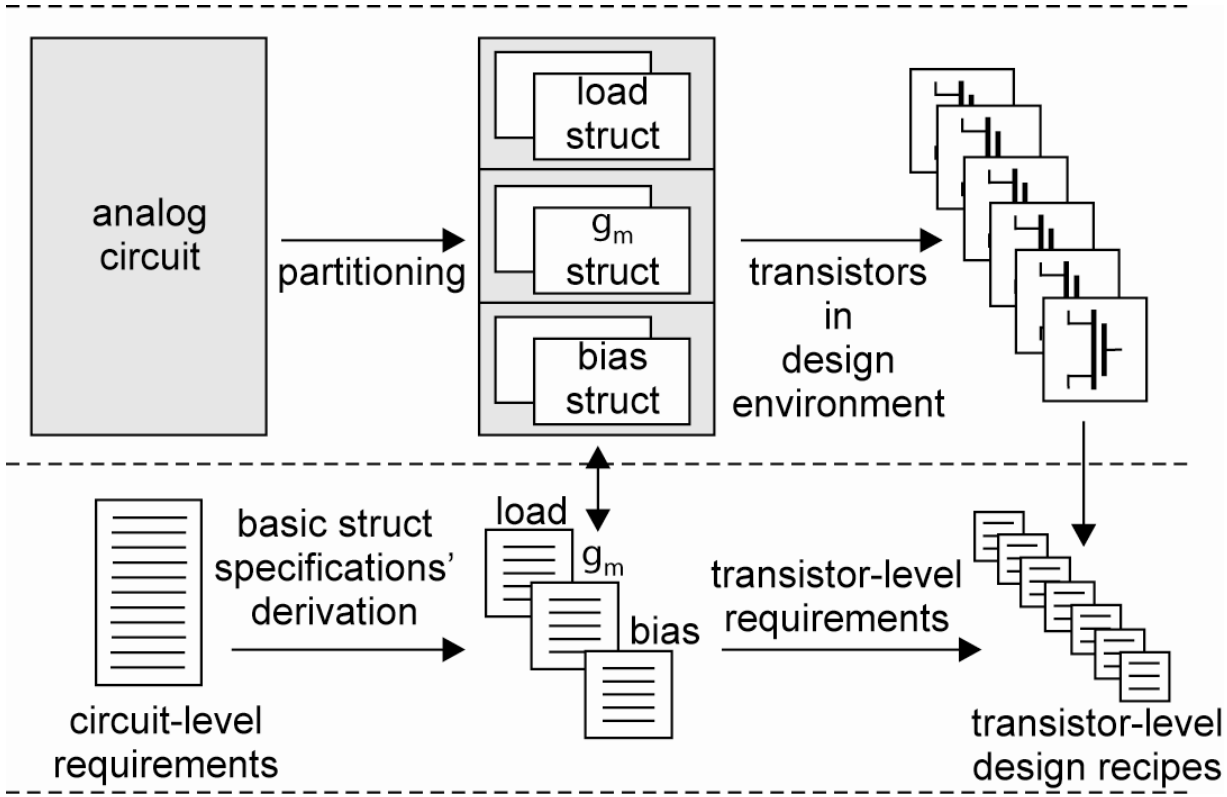
→ **Procedural design scenarios**

→ **Sizing and optimization on the level of basic analog structures**

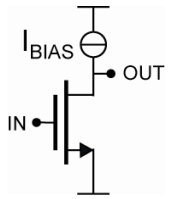
→ **Topology variants**

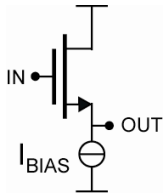


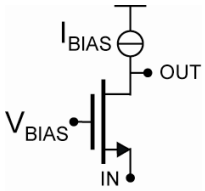
STRUCTURED ANALOG DESIGN

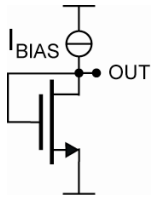


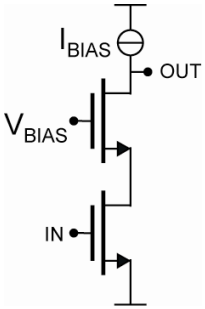
BASIC ANALOG STRUCTURES LIBRARY

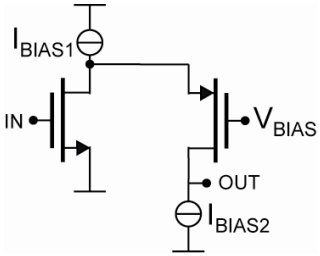


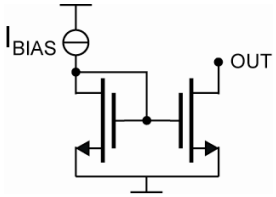


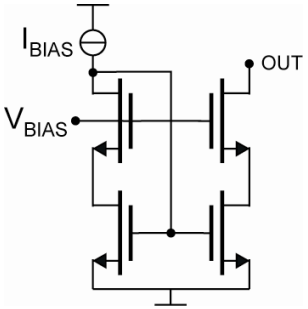


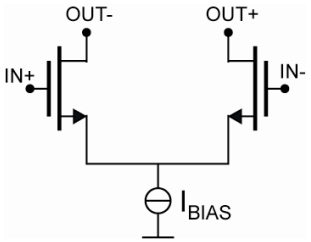


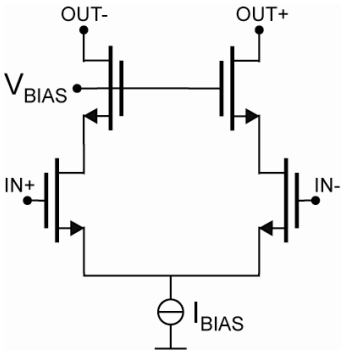


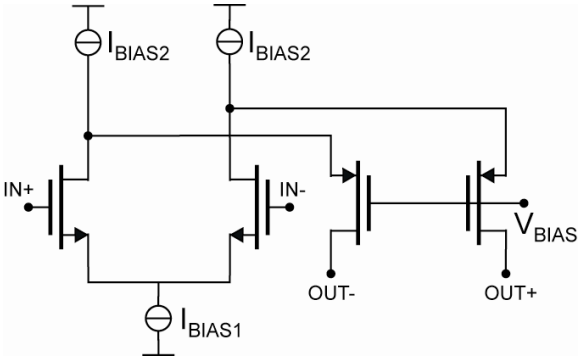












BASIC ANALOG STRUCTURES LIBRARY

→ Classification

Transconductance structures:

CS, CD, CG, cascode, differential pair

Load structures:

simple and cascode current mirror

Bias structures:

simple and cascode current mirror

BASIC ANALOG STRUCTURES LIBRARY

→ **Design parameters**

Transconductance structures:

transconductance, input range, noise,
voltage mismatch (offset)
output resistance, output swing, parasitic capacitances

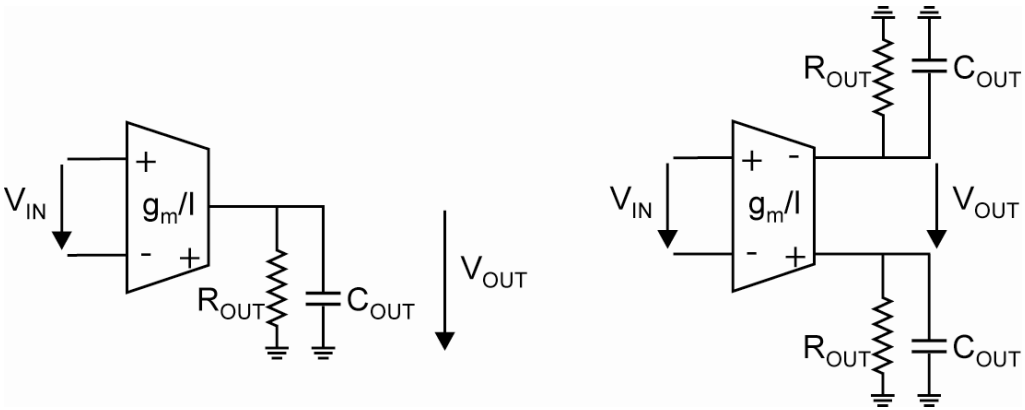
Load structures:

output resistance, saturation voltage,
parasitic capacitances, noise, current mismatch

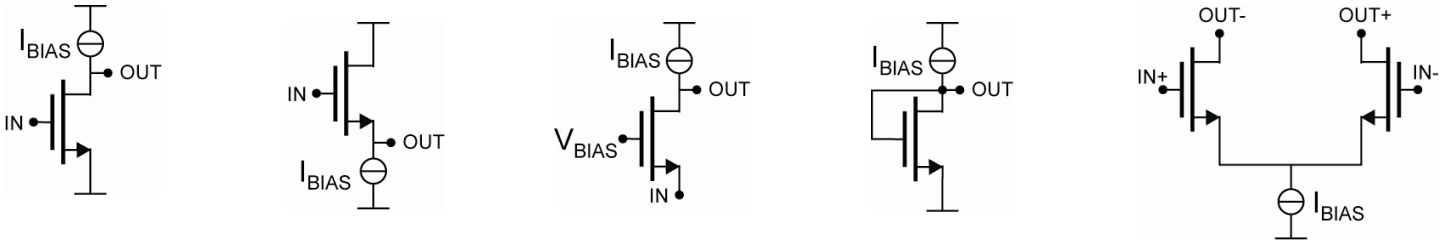
Bias structure:

output resistance, saturation voltage, current mismatch

BEHAVIORAL MODEL OF ANALOG CELL



TRANSISTOR DESIGN CASES



→ Good MOS model

- → Based on physical behavior
- → Covers all significant physical effects
- → Global, compact, accurate
- → Covers all geometry ranges
- → Correct I-V characteristics, correct current derivatives
- → Accurate modeling of the intrinsic capacitances
- → Simple and fast extraction procedure
- → Easy implementation, no convergence problems

TRANSISTOR LEVEL DESIGN

→ MOS model dedicated to analog design

→ **Small number of parameters** with physical meaning

→ **Hierarchical structure**

→ Model equations **approximations** without a great loss of accuracy

→ Accurate modeling of **weak and moderate inversion** behavior

→ **Continuous expressions** of current derivatives

→ EKV MOS model → its basic concept makes it possible to develop a design approach at the transistor level

(http://legwww.epfl.ch/ekv/)

TRANSISTOR LEVEL DESIGN

→ Design parameters vs. design variables

saturation voltage V_{DSsat}	saturation current I_{Dsat}
transconductance g_m	inversion factor *IF*
output conductance g_{DS}	transistor width *W*
parasitic capacitances	transistor length *L*
intrinsic gain A_i	ratio *W/L*
transition frequency f_t	area *WL*
equivalent noise	

TRANSISTOR LEVEL DESIGN

→ Design variables

$$I_{pol} = I_{Dsat} = 2nKP\left(\frac{W}{L}\right)V_t^2 \cdot IF$$

$$\rightarrow \quad \frac{W}{L} = \frac{I_{Dsat}}{2nKPV_t^2 \cdot IF}$$

$$\rightarrow \quad W = \left(\frac{W}{L}\right) \cdot L = \frac{I_{Dsat}}{2nKPV_t^2 \cdot IF} \cdot L$$

$$\rightarrow WL = \left(\frac{W}{L}\right) \cdot L^2 = \frac{I_{Dsat}}{2nKPV_t^2 \cdot IF} \cdot L^2$$

inversion factor *IF*

transistor length *L*

TRANSISTOR LEVEL DESIGN

→ Design parameters

$$V_{DSsat} = V_t \cdot (2\sqrt{IF} + 4)$$

$$\frac{g_m}{I_{Dsat}} = \frac{1}{nV_t} \cdot \frac{1}{\frac{1}{2} + \sqrt{IF + \frac{1}{4}}}$$

$$g_{DS} = \frac{I_{Dsat}}{L \cdot V_a}$$

$$A_i = \left(\frac{g_m}{I_{Dsat}}\right) \cdot L \cdot V_a$$

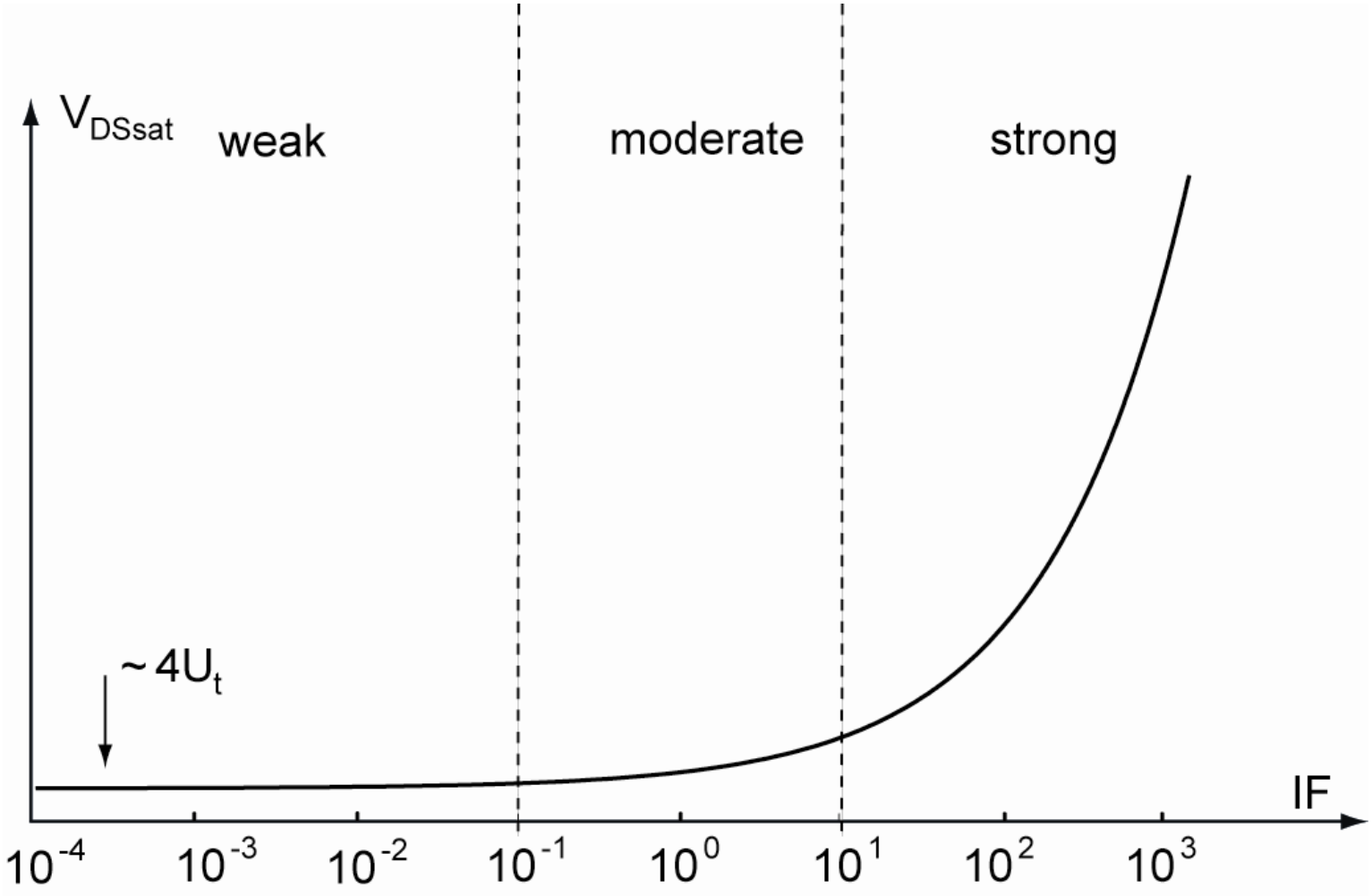
$$(\Sigma C_i)_{MAX} = C_{ox} \cdot \frac{I_{Dsat}}{2nKPV_t^2 \cdot IF} \cdot L^2$$

$$f_t = \frac{g_m}{2\pi(\Sigma C_i)_{MAX}} = \left(\frac{g_m}{I_{Dsat}}\right) \cdot \frac{nKPV_t^2 \cdot IF}{\pi C_{ox} \cdot L^2}$$

$$v_{n,th}^2 = \frac{4KT \cdot n \cdot \frac{1}{1+IF} \cdot \left(\frac{1}{2} + \frac{2}{3}IF\right)}{\left(\frac{g_m}{I_{Dsat}}\right) \cdot I_{Dsat}}$$

$$v_{n,fl}^2 = \frac{2nKPV_t^2 \cdot KF \cdot IF}{L^2 C_{ox} f^{AF} \cdot I_{Dsat}}$$

→ Design parameters vs. variables



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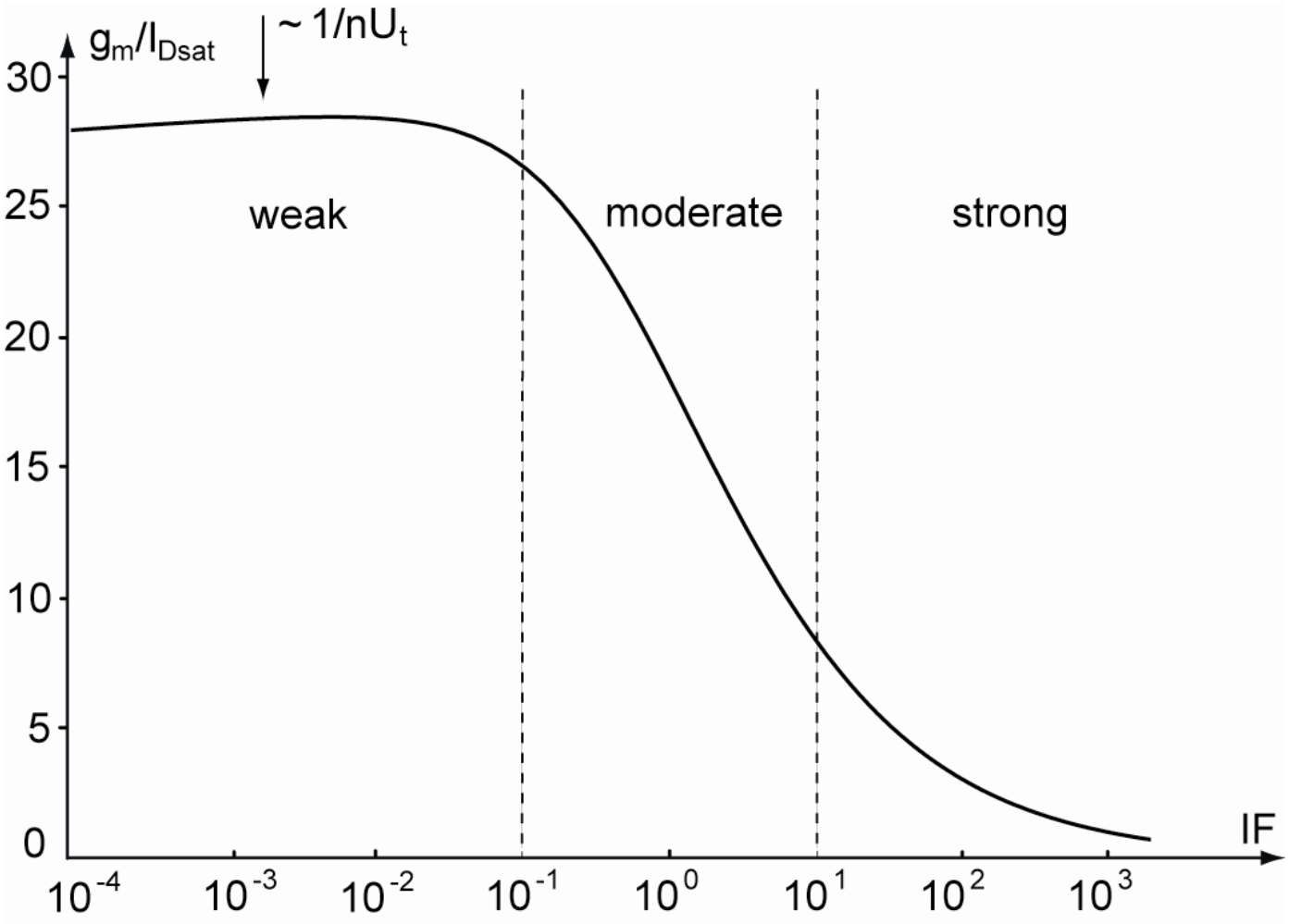

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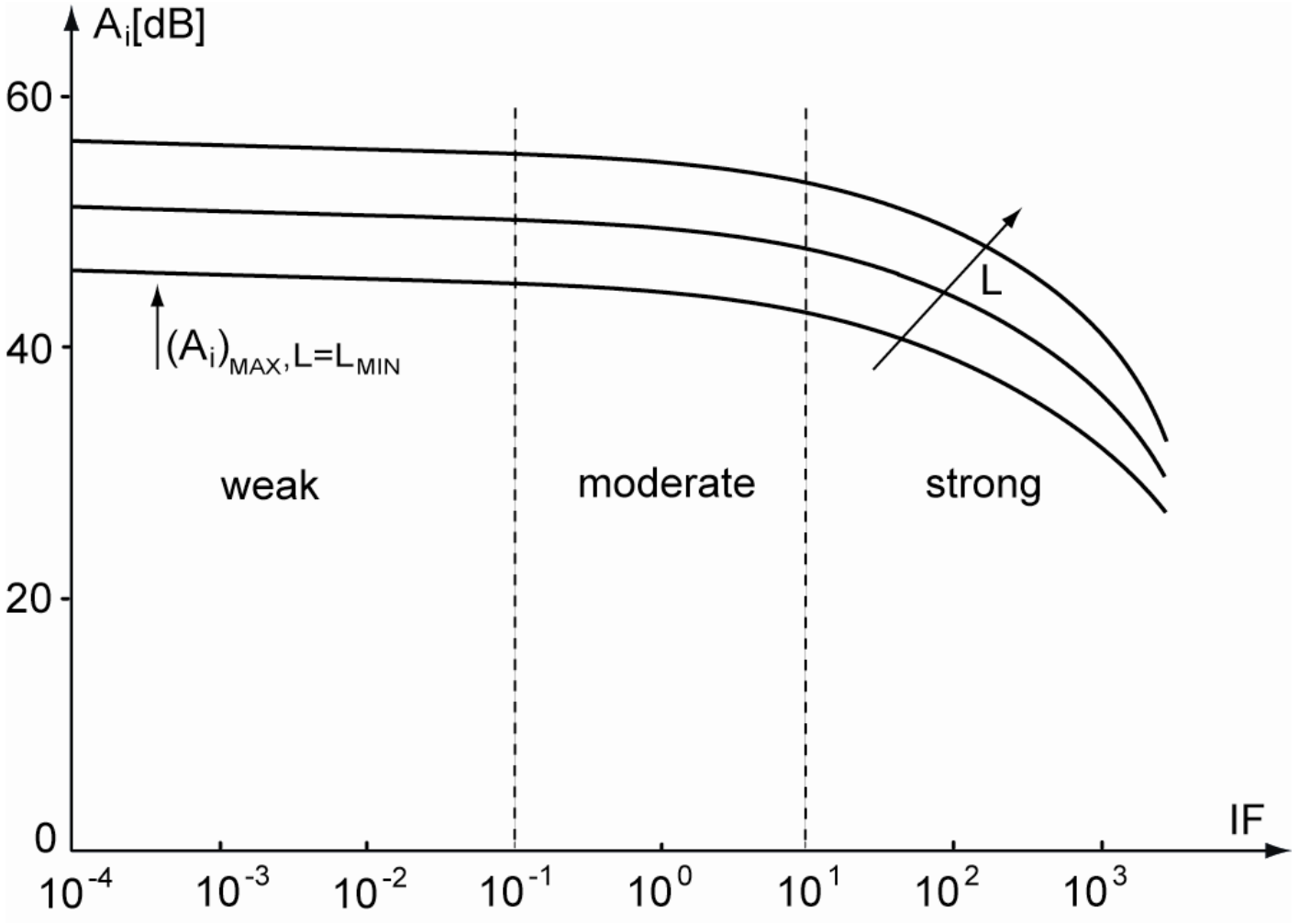

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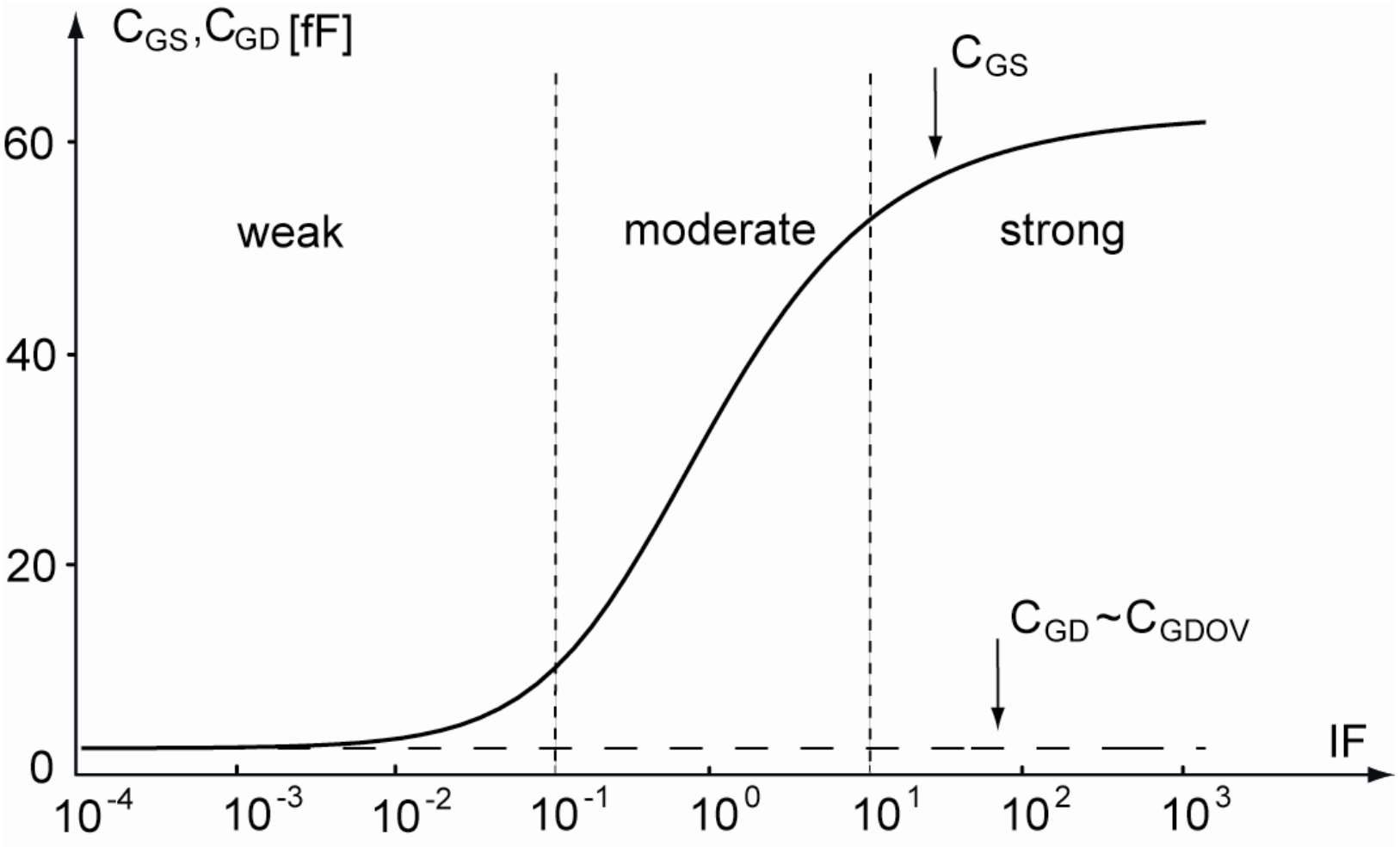

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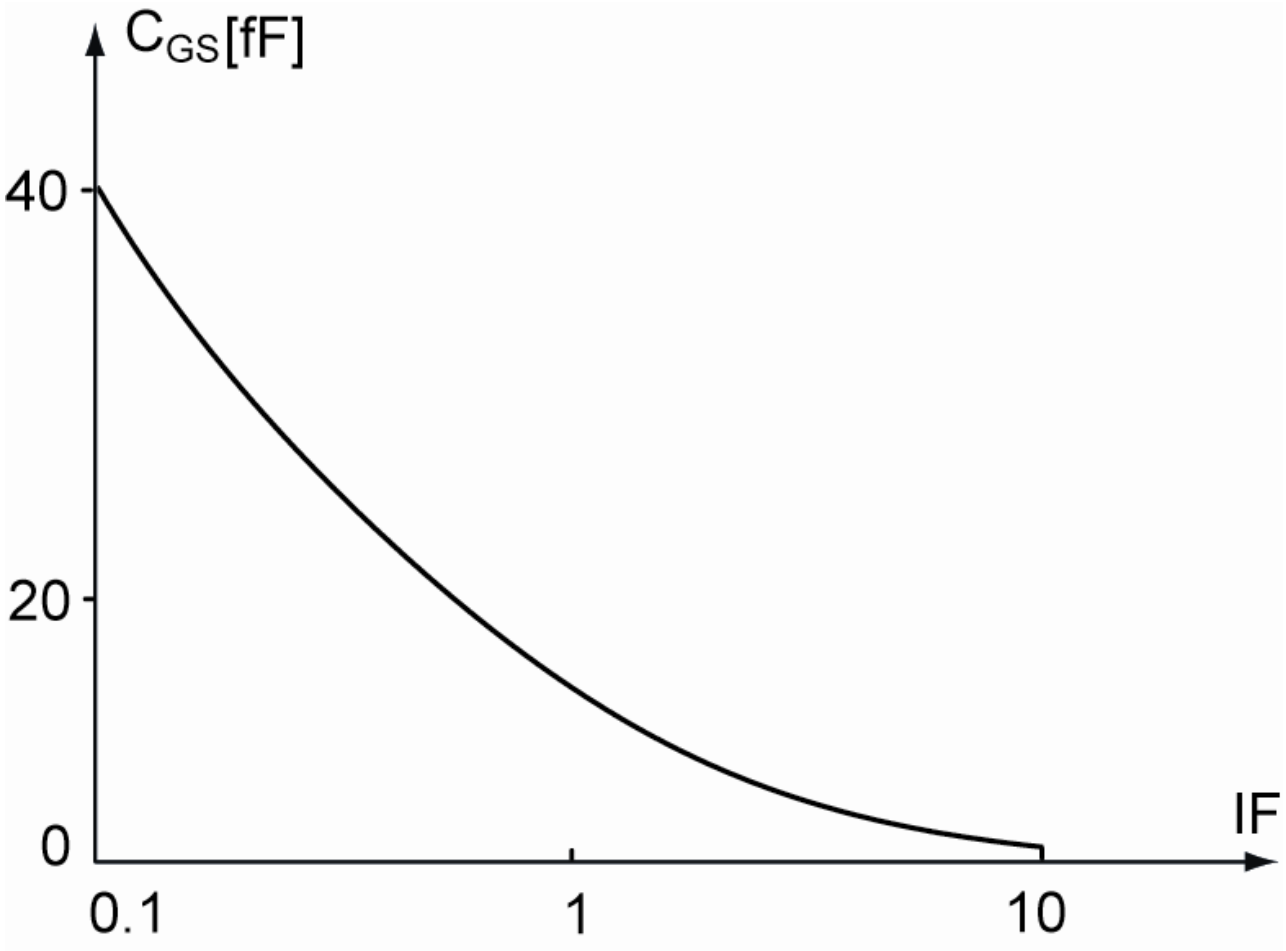

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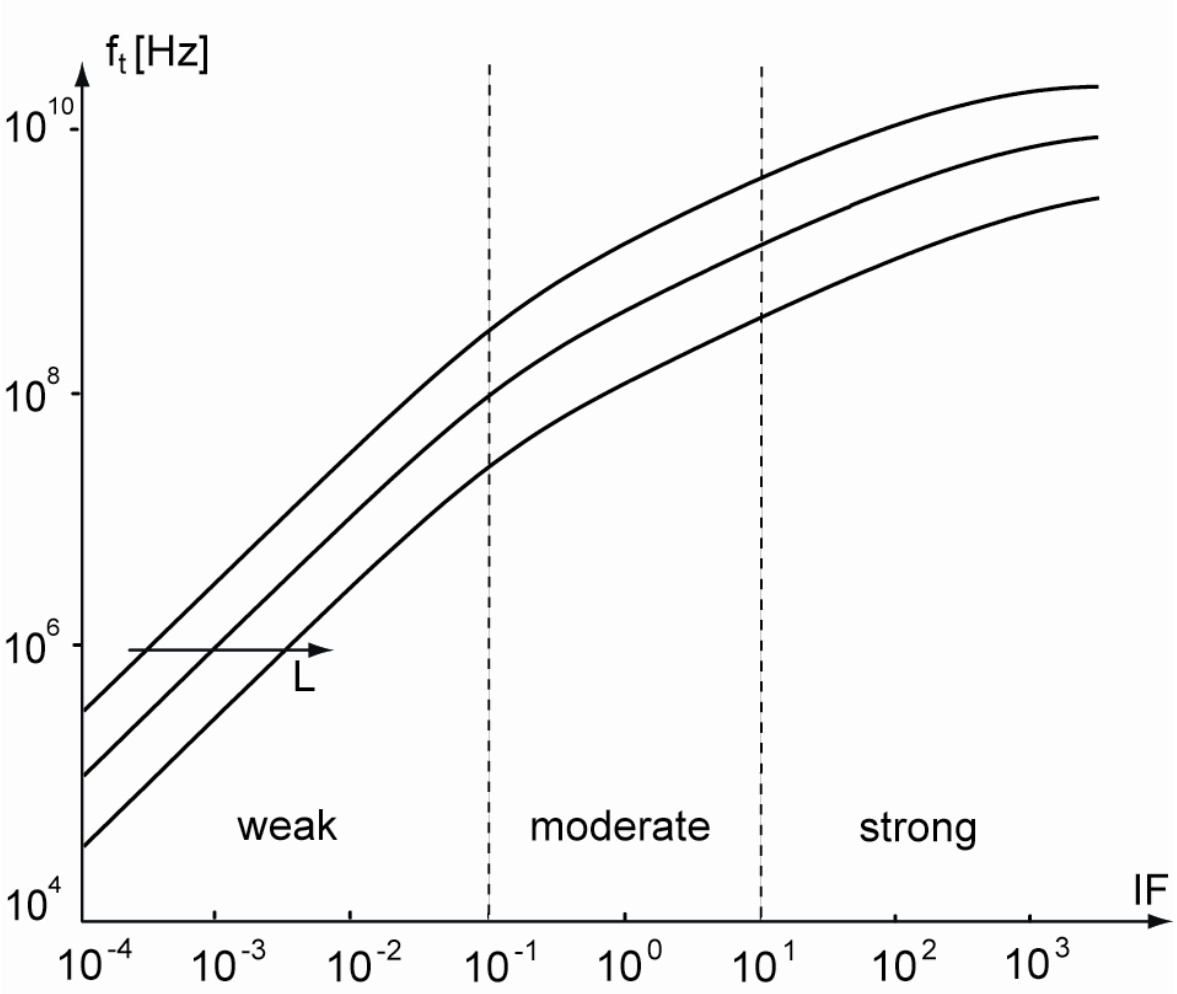

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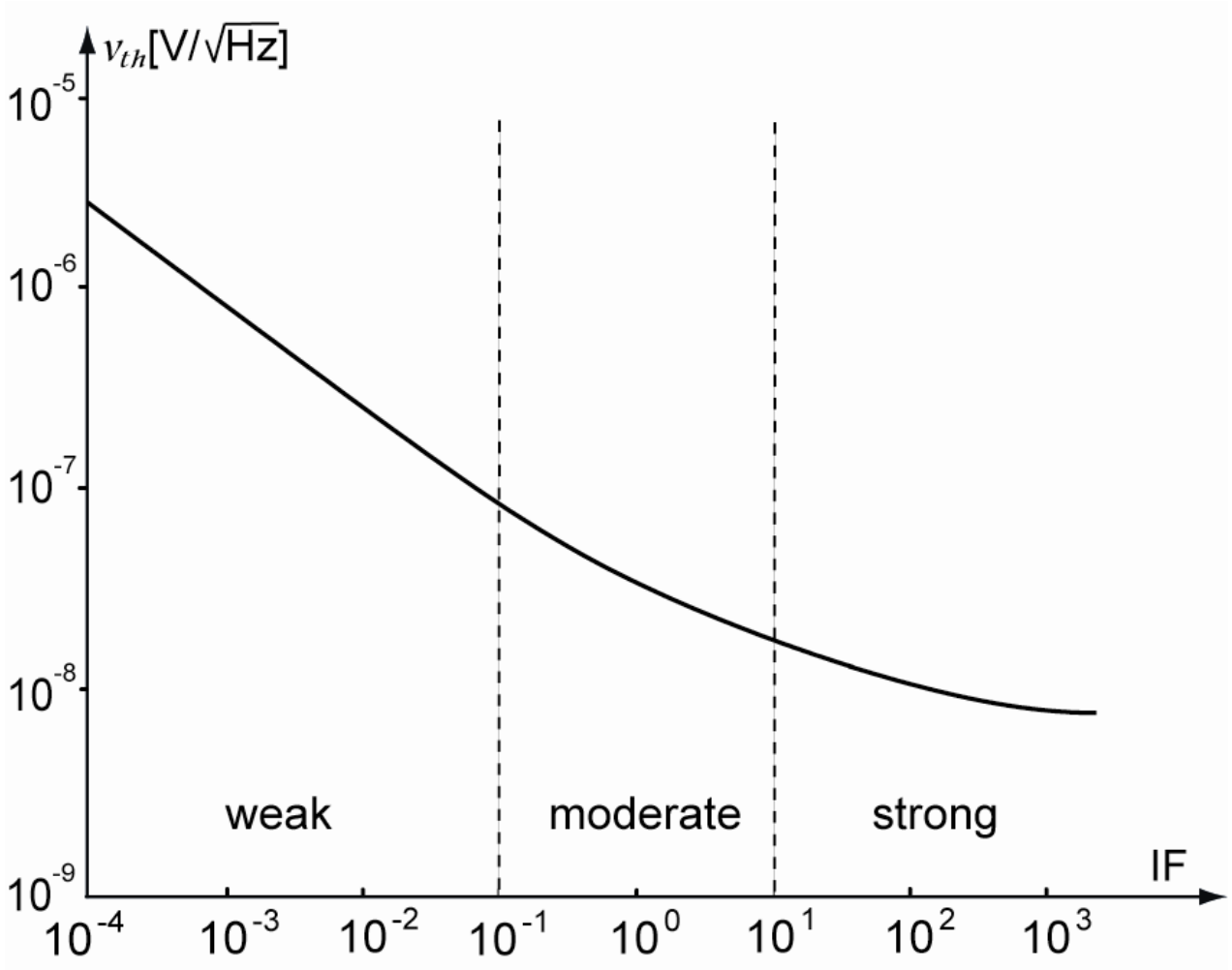

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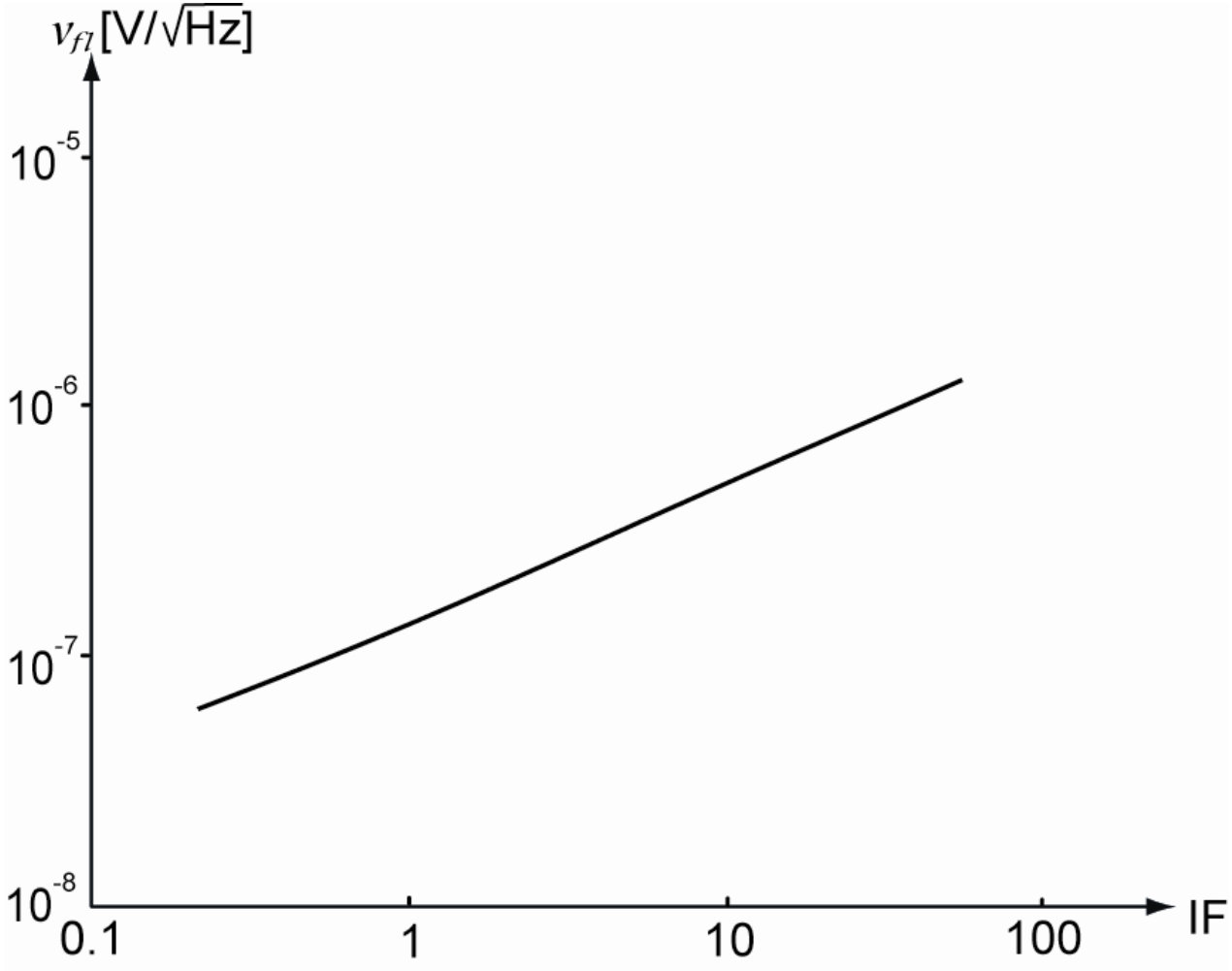


TRANSISTOR LEVEL DESIGN

→ Design cases :

output conductance + saturation voltage

output conductance + transconductance

saturation voltage + gain

gain + sum of par. caps

transconductance + sum of par. caps

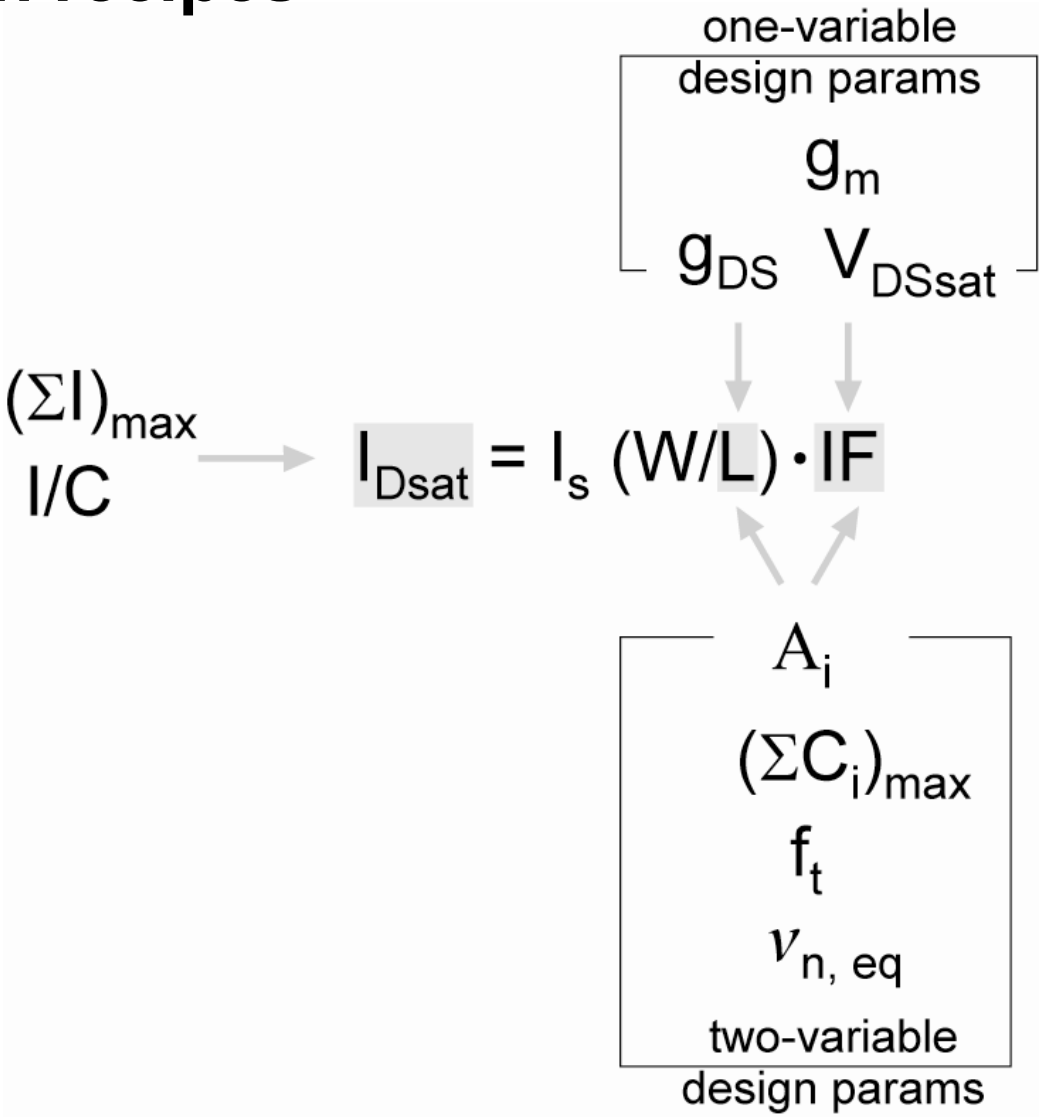
transconductance + equiv. noise

gain + transition frequency

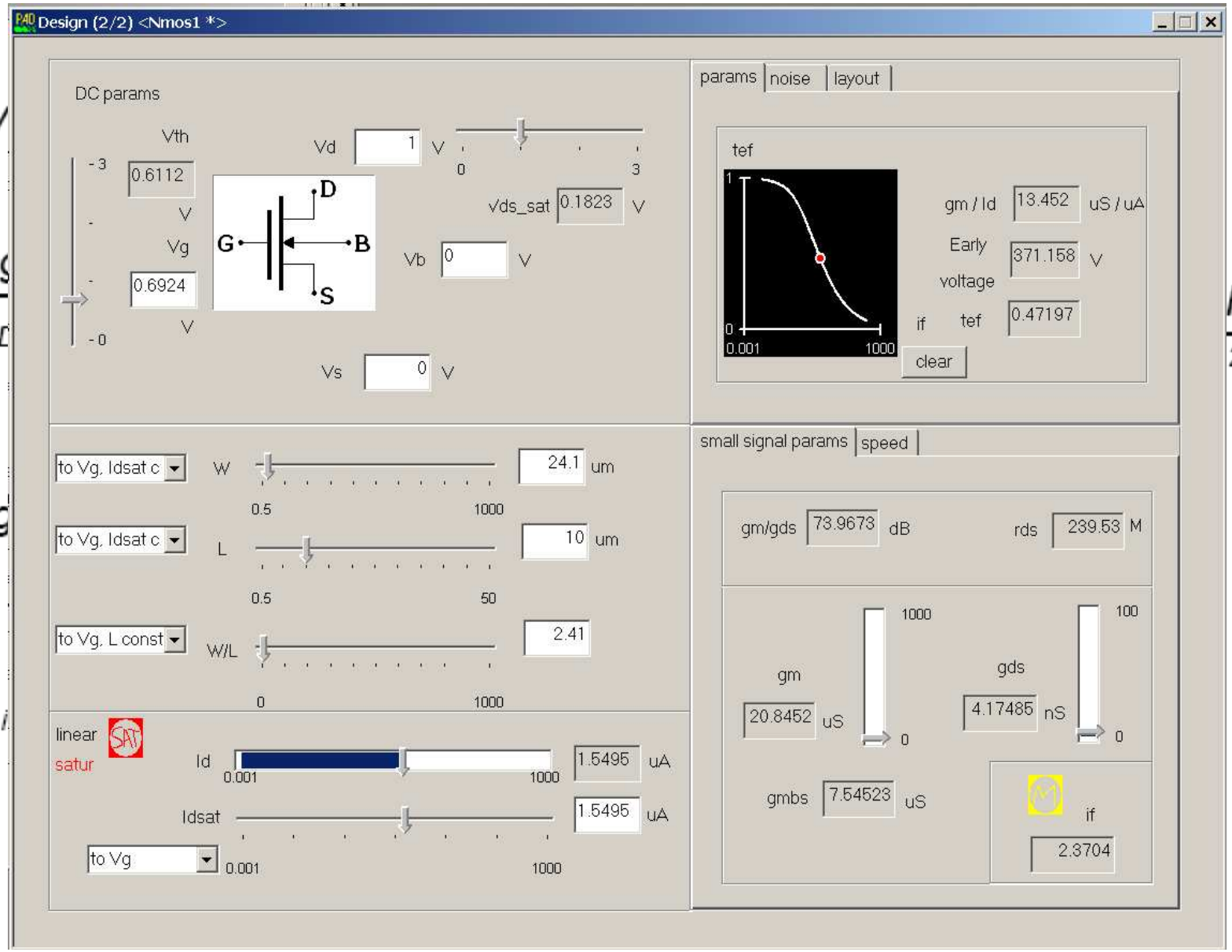
transconductance + voltage mismatch

saturation voltage + current mismatch

→ Design recipes



DESIGN CHARTS

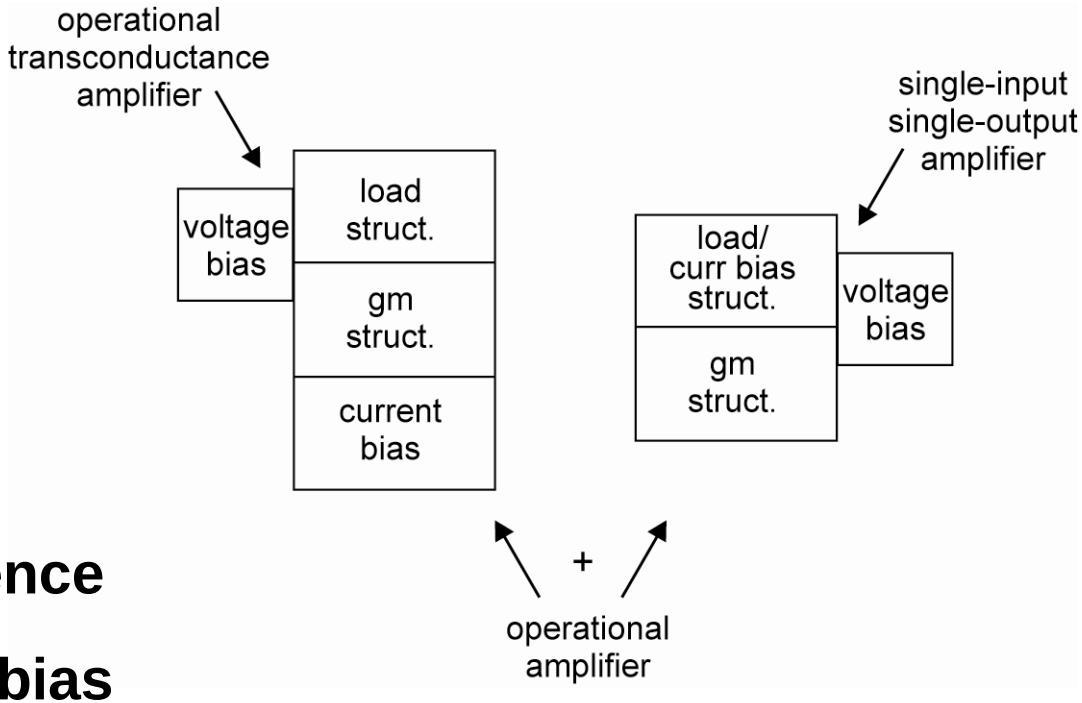


PROCEDURAL DESIGN

→ **Circuit partitioning**

→ **Basic analog structures specifications derivation**

→ **Step-by-step design sequence in transconductance-load-bias structure order**



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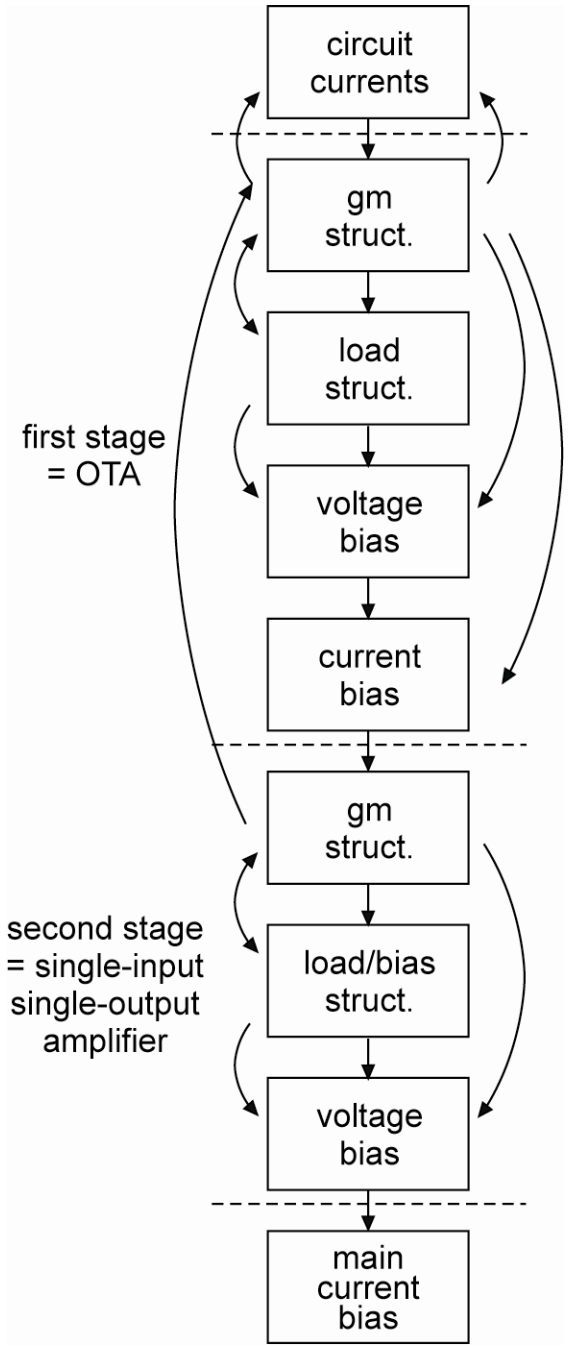
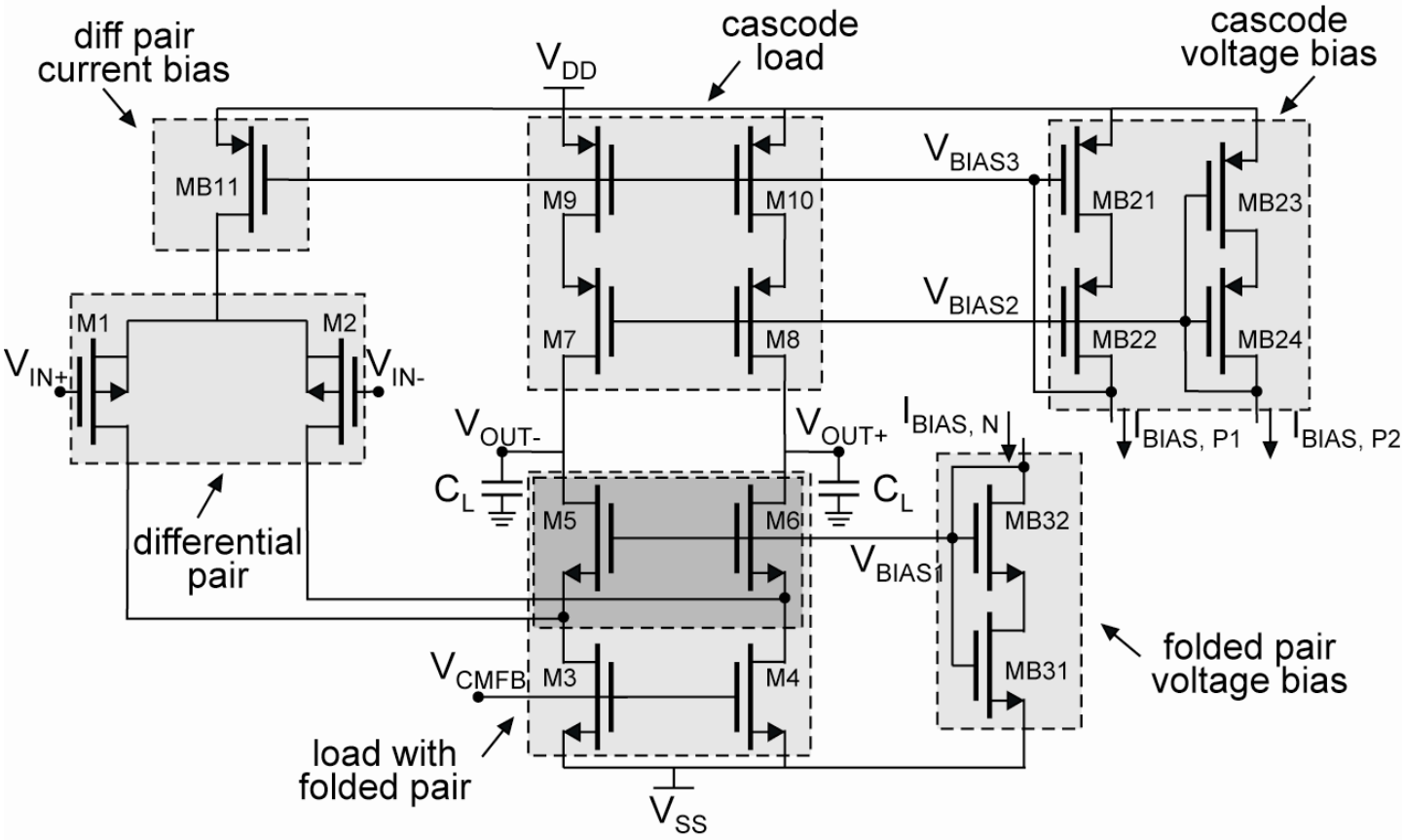


PROCEDURAL DESIGN

→ Circuit partitioning → example: fully-differential folded cascode OTA



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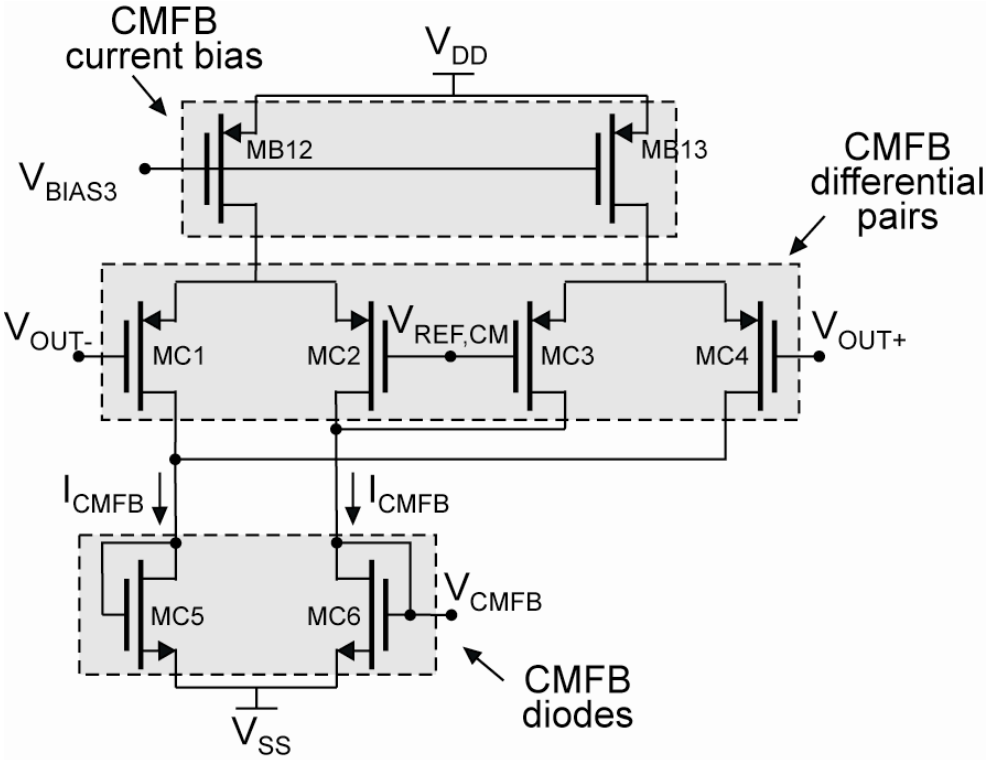

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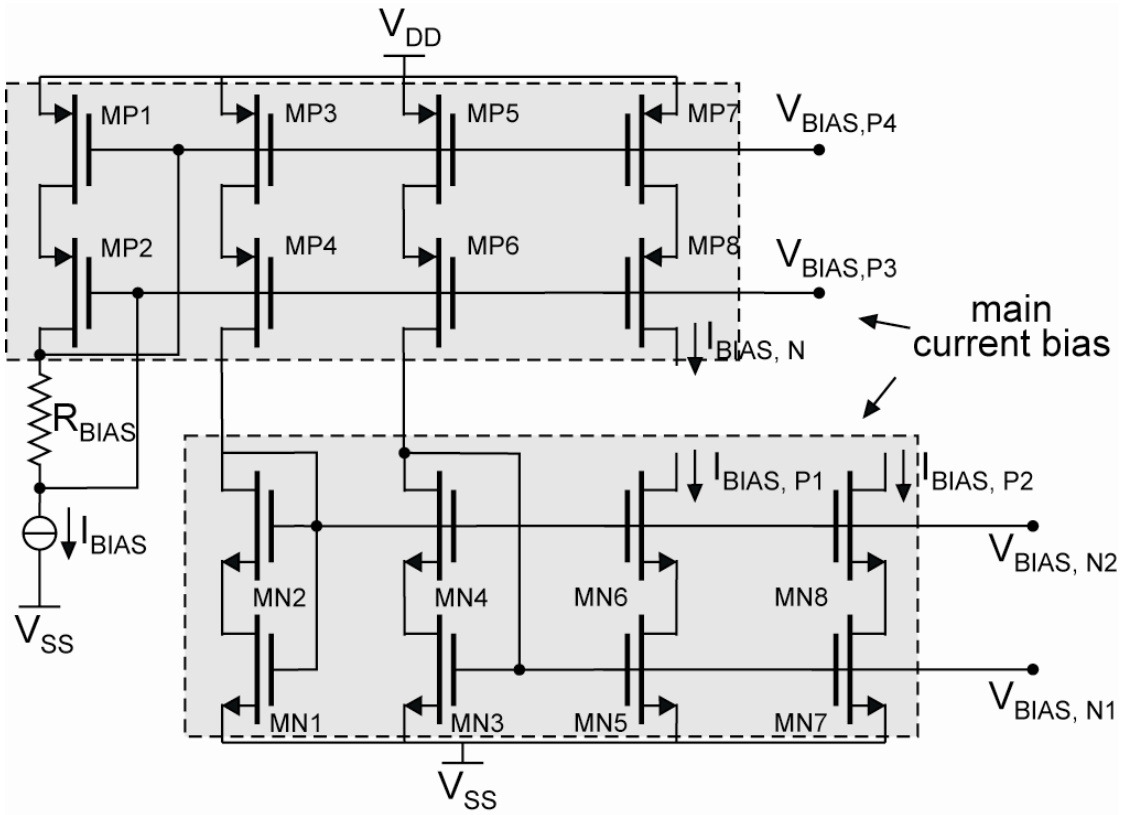

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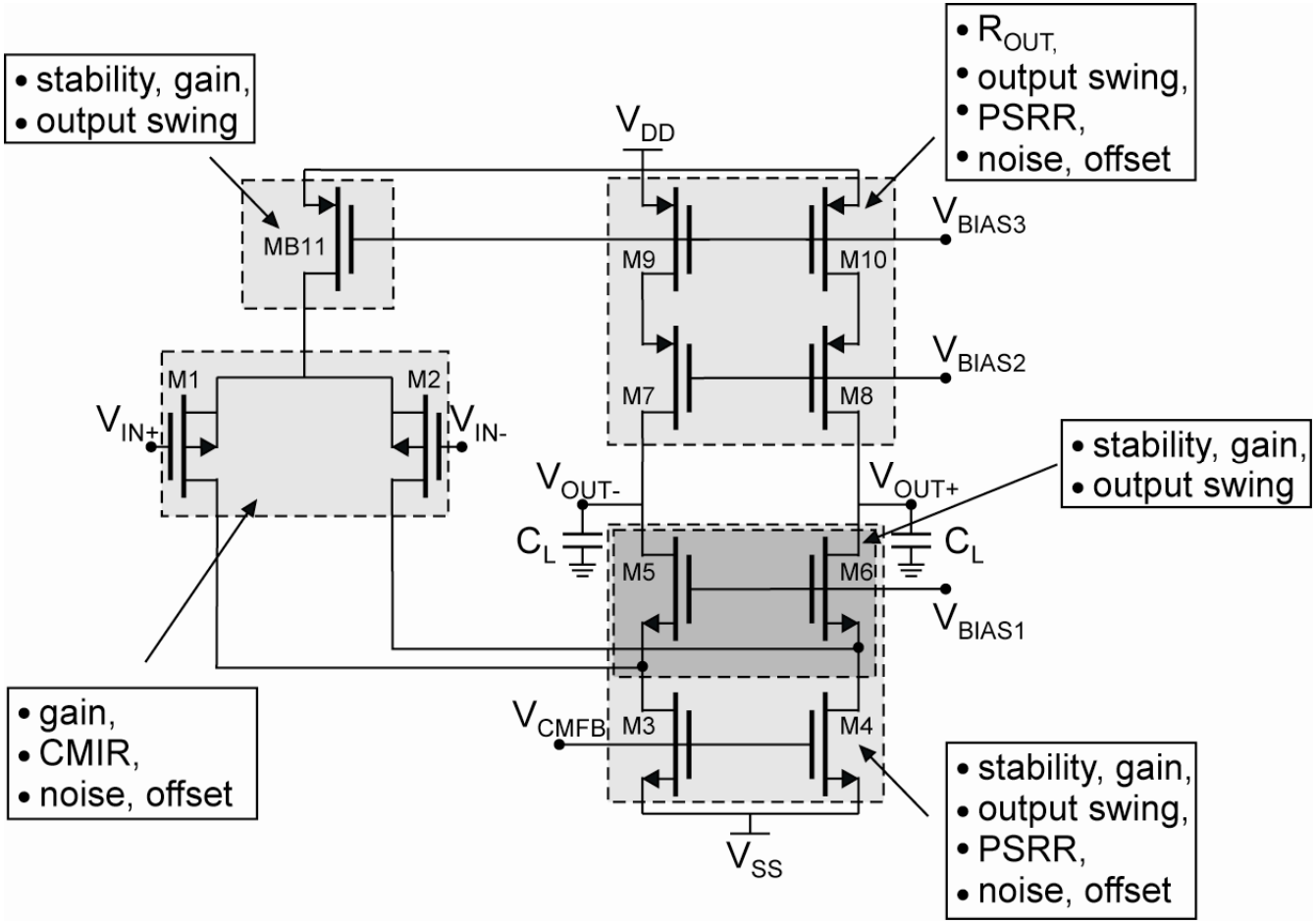

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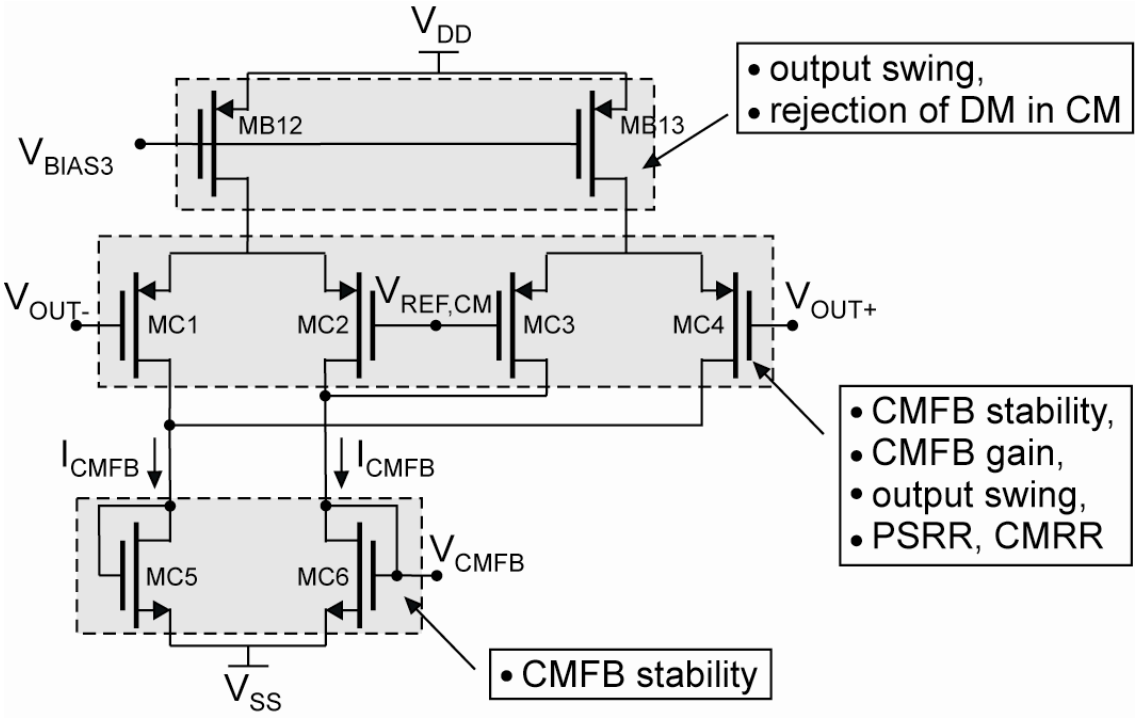


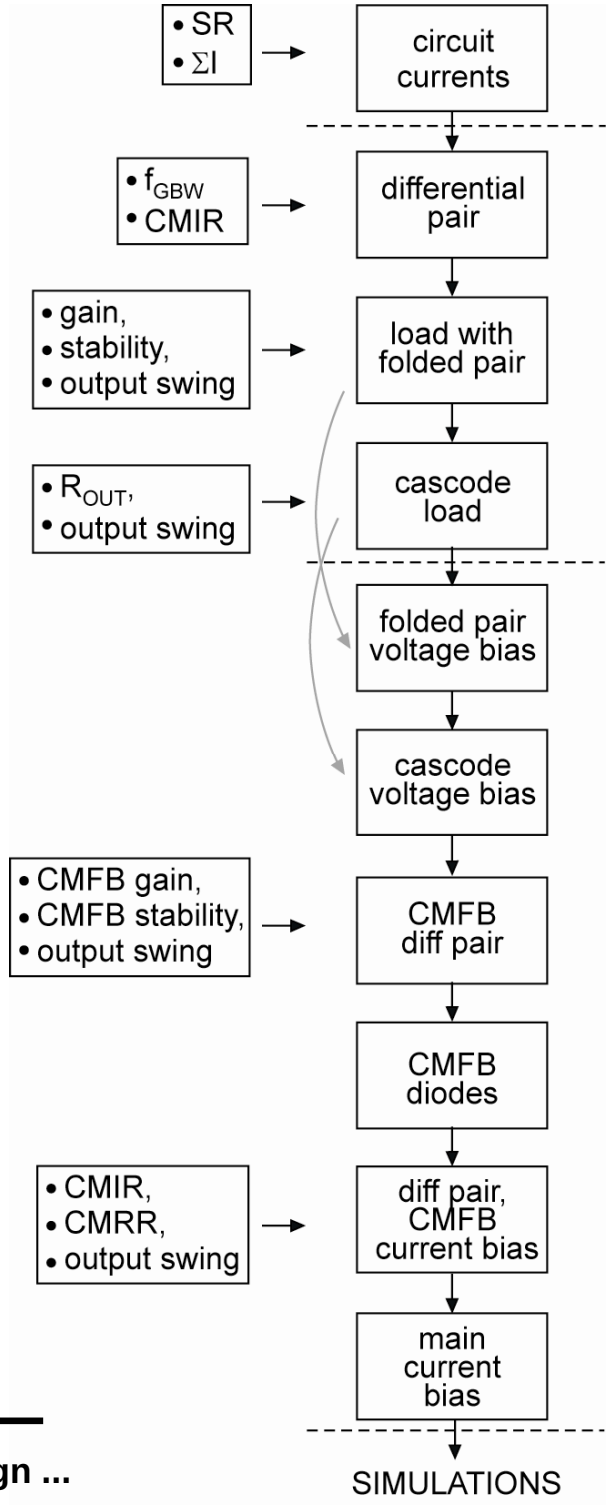
PROCEDURAL DESIGN

→ Design sequence

$$\frac{g_m}{I_{Dsat}} = \frac{1}{nV_t} \cdot \frac{1}{\frac{1}{2} + \sqrt{IF + \frac{1}{4}}}$$

$$V_{DSsat} = V_t \cdot (2\sqrt{IF} + 4)$$

$$g_{DS} = \frac{I_{Dsat}}{L \cdot V_a}$$



PROCEDURAL DESIGN

→ **Design optimization**

→ **Specification propagation**

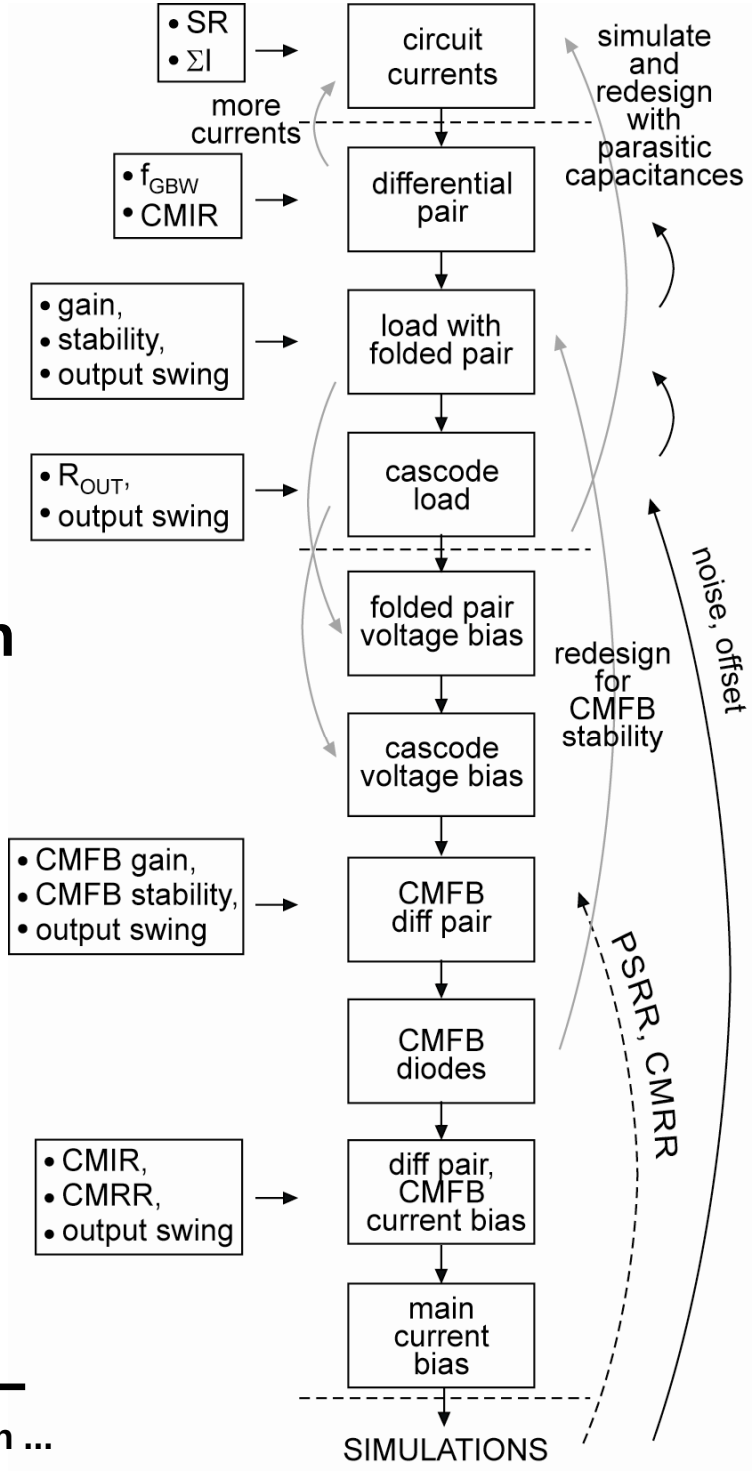
→ **Parameters' bounds verification**

example:

$$\frac{f_{GBW}}{SR} = \frac{g_m/(2\pi C_L)}{I_{OUT}/C_L} = \frac{g_m}{2\pi I_{OUT}}$$

$$= \frac{g_m}{2\pi I_{Dsat}} = \frac{1}{2\pi}\cdot\left(\frac{g_m}{I_{Dsat}}\right)$$

→ **Topology variants**



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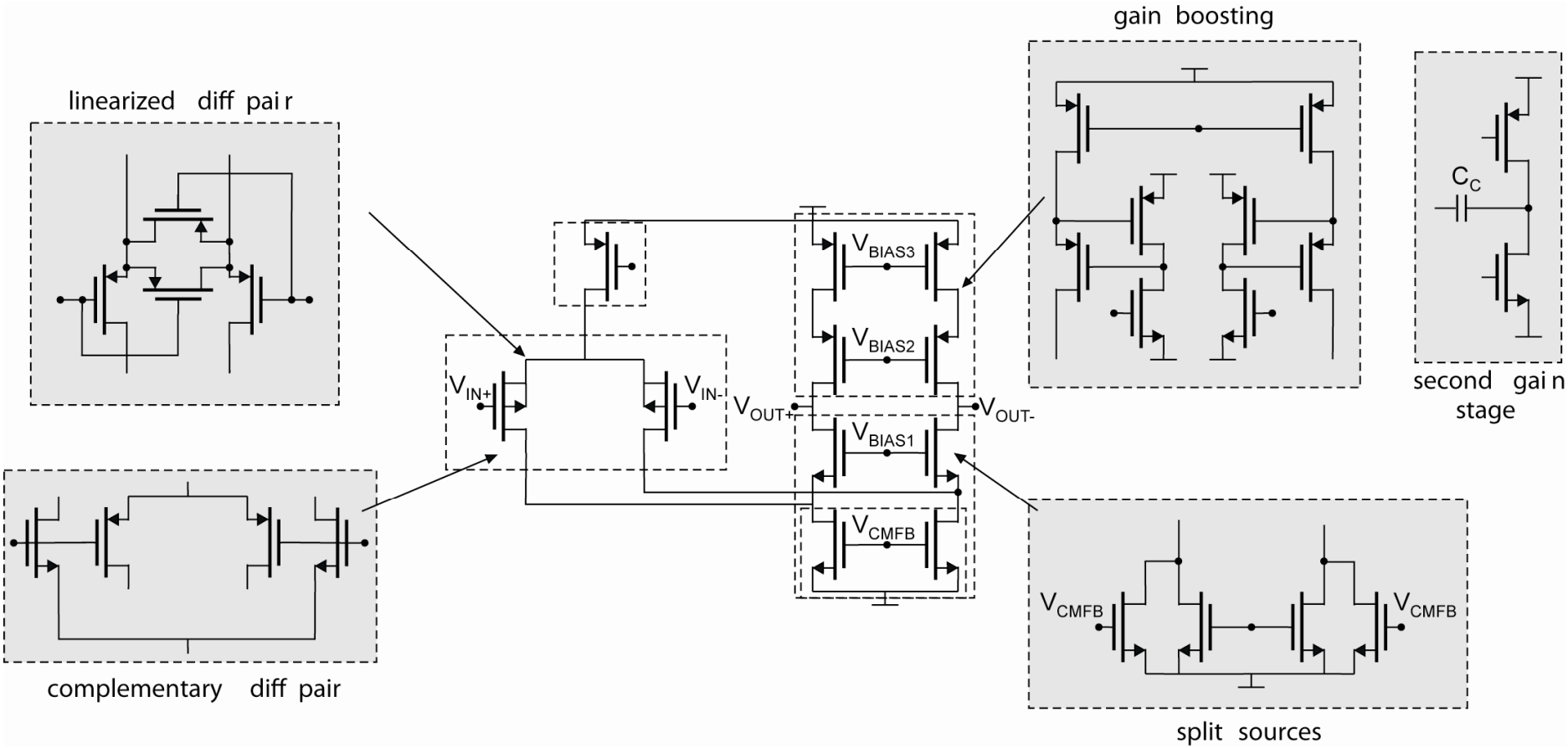

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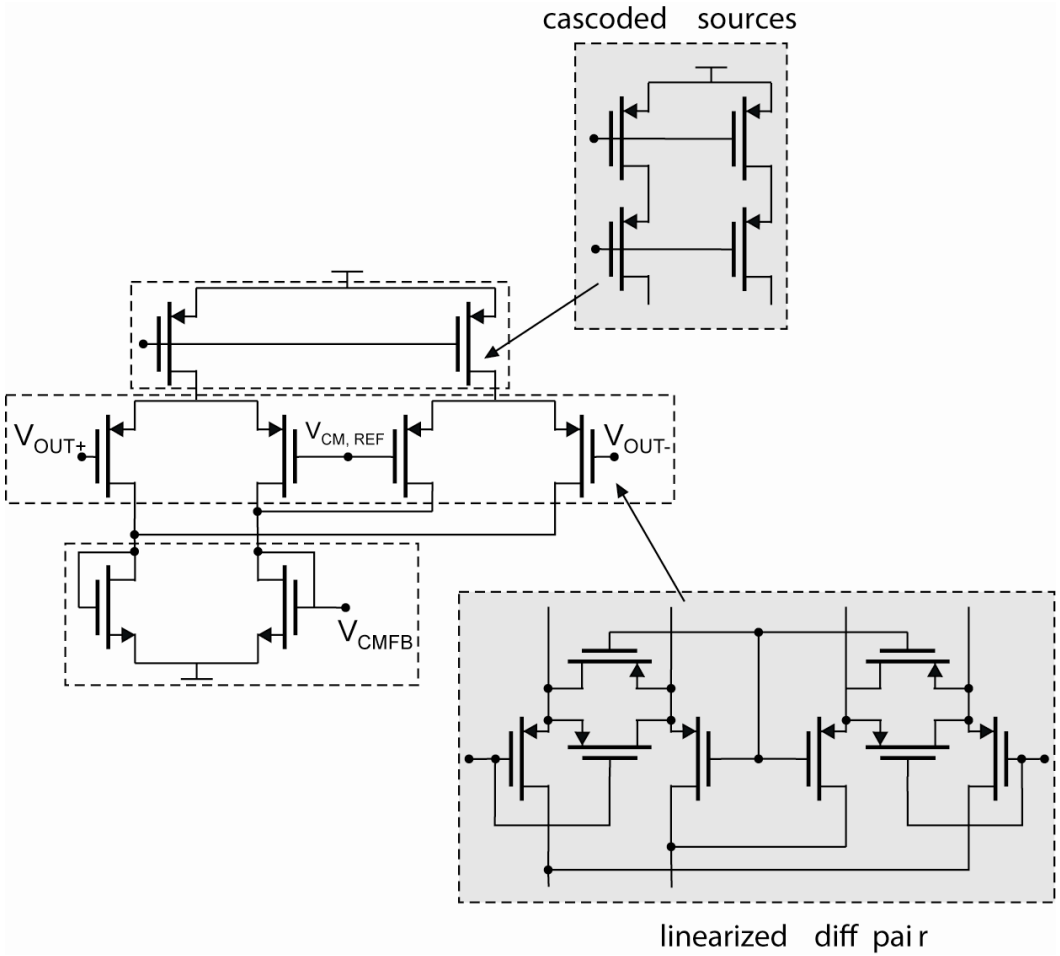


PAD tool (http://analog.epfl.ch/)

→ Basic features

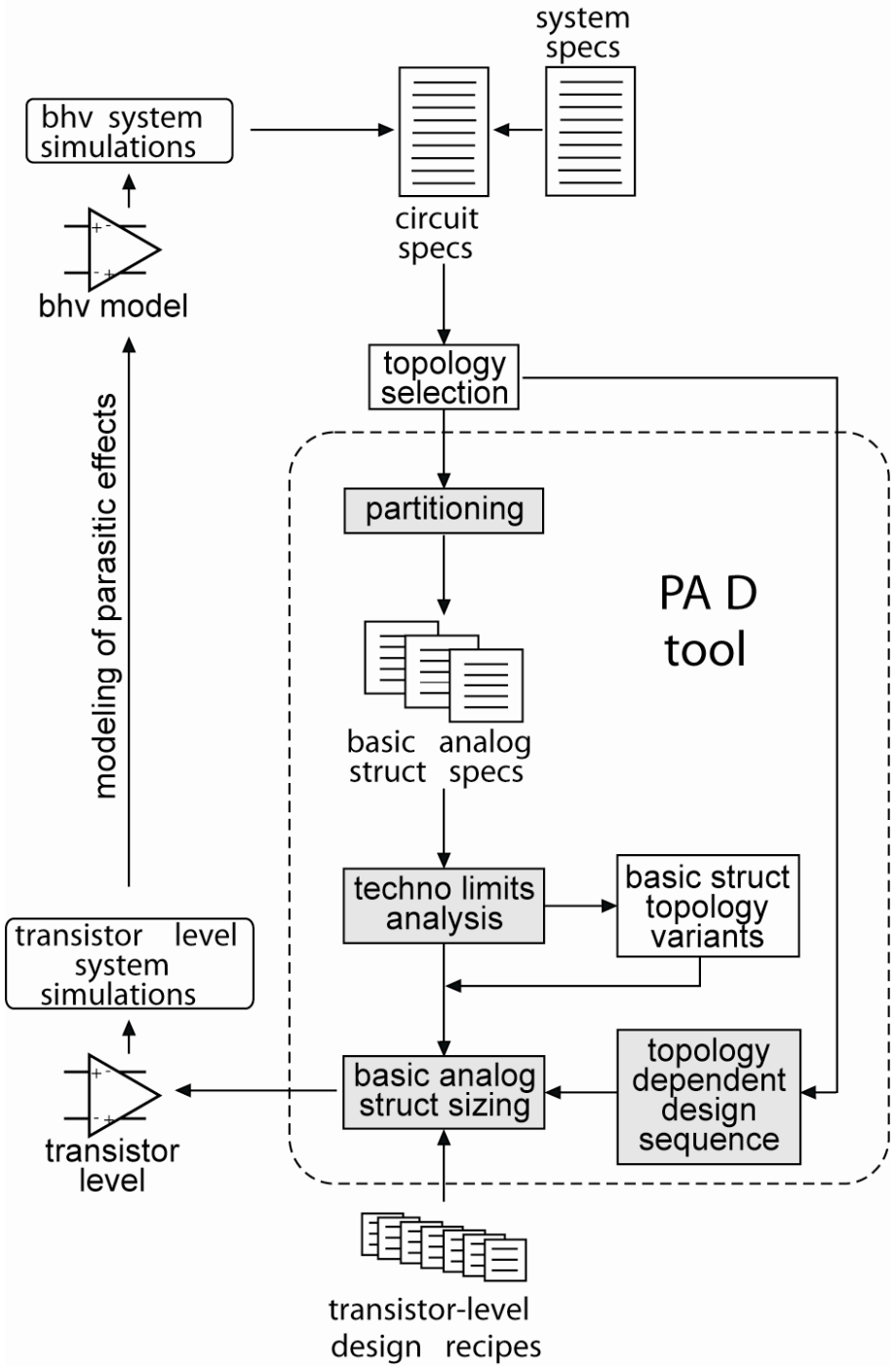
→ Analog design **assistance**

→ **Interactive interface**

→ Step-by-step design of analog cells

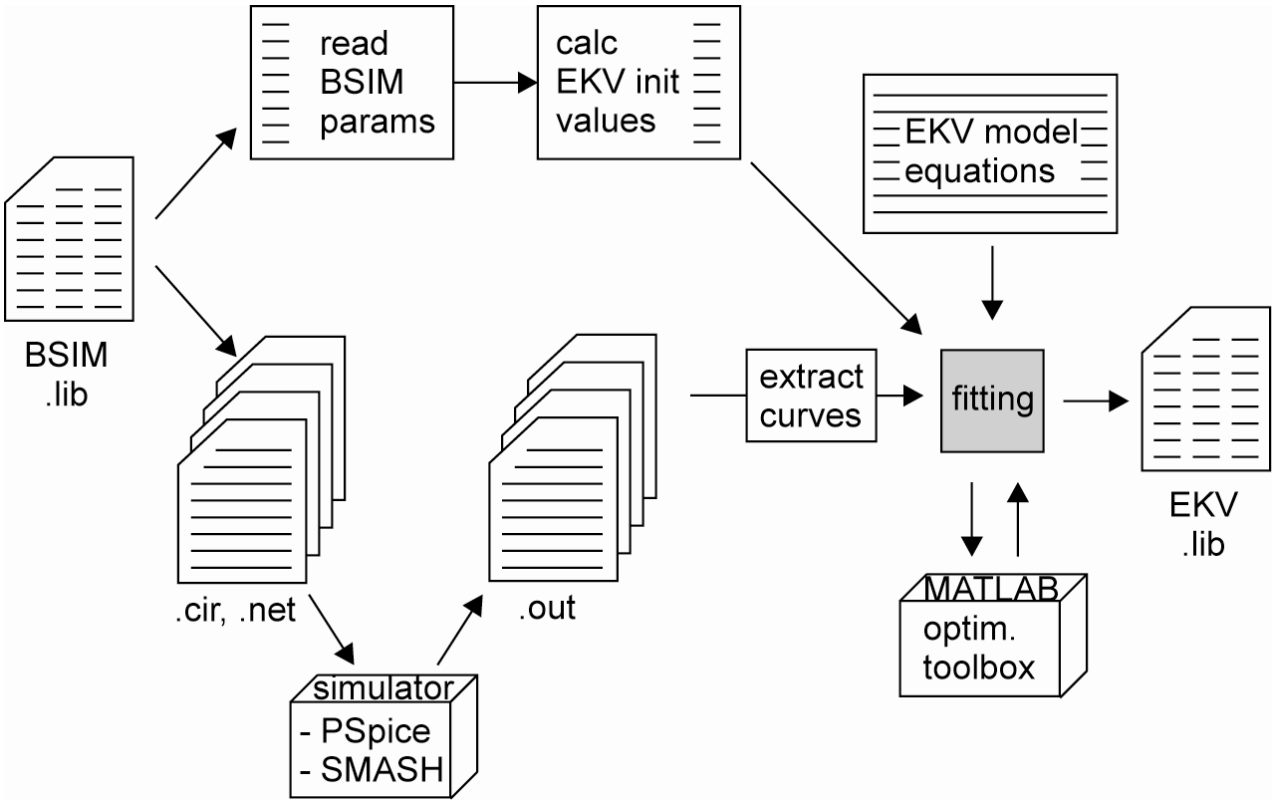
→ **Sizing and optimization**

→ Intuitive understanding



BSIM2EKV tool (http://analog.epfl.ch/)

→ Conversion concept



CONCLUSION

→ Simplify complex analog design problems by partitioning of analog cells into basic analog structures

→ Size each basic analog structure in the environment imposed by the circuit

→ Look for the design trade-offs on both circuit level and transistor level

→ Use the inversion level as a key design variable

STRUCTURED ANALOG CMOS DESIGN

Based on the Device Inversion Level

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