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Study of Current Density Influence on Bond Wire Degradation Rate in SiC MOSFET Modules

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***Abstract* – This paper proposes a separated test method for studying the current effect on the ageing process of wire-bonded Silicon Carbide (SiC) MOSFET module under power cycling test (PCT). The separated test method enables to test SiC MOSFET with different load current densities, but under the same temperature swing and average temperature conditions. By analyzing the output characteristics in the linear region, the relations among the gate voltage, on-state voltage and junction temperature are revealed. Then, the one-to-one correspondence between gate voltage and conduction power loss can be used to adjust the current density with the same temperature conditions. Two six-pack SiC modules (1200V/20A) are tested under 12A and 24A conditions to experimentally verify the proposed method. The ageing curves show that the higher current can speed up the ageing rate of bond wires even under the same temperature conditions (65°C ~ 125°C). Moreover, the high current density also has an impact on the solder layer degradation as well as the temperature conditions. Finally, power device analyzer B1506A and Scanning Acoustic Microscopy (SAM) are used to investigate the degradation of electrical parameter and solder layer, respectively. The final summary of analytical results shows that the input current has a non-negligible impact on the degradation process of power module.**

***Index Terms* – Silicon carbide MOSFET, power cycling test, separated test, adjustable gate voltage, and package degradation.**

I. INTRODUCTION

High-power Silicon Carbide (SiC) MOSFET modules have begun to enter the market [1], [2]. Since the characteristics of SiC dies are quite different from the Si-based devices in terms of smaller dies, higher temperature tolerance and higher switching frequency, the conventional package techniques developed for Si-based semiconductor inevitably bring new obstacles to SiC dies [3]. With the advantages of mature package techniques and low cost, the conventional wire-bonded packages are usually employed in the existing commercial SiC power modules [4]–[7]. Hence, how to evaluate the reliability level for the combination of emerging SiC dies and the conventional wire-bonded package becomes a real problem.

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Accelerated power cycling test (PCT) is often used for the package-level failure mechanism evaluation of power modules. So far, many PCT works have been done to evaluate the package reliability issues on the conventional wire-bonded power modules and discrete devices [8]–[11]. In the late 90's, the experimental test time (or power cycles) to failure as a function of temperature swing (ΔT_j) and average temperature (T_{avg}) under PCT were published in the LESIT Study [12]. It is concluded that the both ΔT_j and T_{avg} dominate for the number of cycles to the end of life. Finally, due to the mismatch of Coefficient of Thermal Expansions (CTE) between different materials, the temperature swing is regarded as the main decisive cause for the package wear-out degradation [13], [14].

However, according to the extensive statistical test results, the correlations between the number of power cycles and the temperature swing are associated with many test conditions [15]–[17]. Apart from the typical ΔT_j and T_{avg}, both the amplitude of load current I_{load} and pulse duration ton also have a great impact on the final power cycles and lifetime estimation of power modules [15], [18], [19]. In order to investigate the effect of different test conditions on the ageing process, the separate control strategies have been developed for the conventional PCT, such as constant t_{on}, constant power loss methods. In [18], [20], the influence of different t_{on} duration on the number of power cycles is studied. A similar test idea is performed in AC-based PCT platform [21], where the fundamental frequency effect on the lifetime and failure mechanism of IGBT modules are also studied. However, the aforementioned separation test methods do not take into account the current effect individually in the tests.

Usually, the current effect is mixed with temperature factors for the bond wire degradation evaluation because the temperature swing is adjusted by the load current [8], [22]. In the standard PCT process, both large temperature swing and current are imposed on the module. Since the desired temperature swing is mainly proportional to the input current, the influence of current cannot be separated from ΔT_j when using the standard PCT principle. In the case of different load currents, the pulse duration time should be adjusted accordingly for the required temperature swings. If so, the total test time spend on the same number of cycles would be completely different. As a result, the effect of different current densities on the module degradation cannot be compared fairly due to the different test time and power cycles. So far, the PCT standard formulated in IEC 60749-34 specifies the operation rules only with regard to the desired ΔT_j and how to avoid thermal runaway failure [23]. The load current is not treated as a quantitative factor in PCT principle, which could cause deviations to the lifetime model and the reliability evaluation.

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To overcome the above problems, a power cycling test method for investigating the current density effect individually on the wire-bonded SiC module is proposed. By controlling the gate voltage V_{gs}, the conduction loss of SiC MOSFET can be adjusted instead of the load current. Therefore, the SiC module can be tested under the same T_j requirements (ΔT_j and T_{avg}) and pulse duration t_{on}, but with the different load current in PCT. The package reliability evaluation, especially the bond wire and solder layer, can be investigated without the coupling effect of temperature factors (ΔT_j and T_{avg}).

This paper is organized as follows: In Section II, the problems in the conventional PCT method is introduced firstly, and then the failure mechanisms for bond wires and solder layer are reviewed. In Section III, on the basis of linear region characteristics of SiC MOSFET, an equivalent power loss control method by means of gate voltage adjustment is described. The experimental results confirm the feasibility of the proposed method, and the corresponding analysis and discussion are shown in Section IV and Section V, respectively. Finally, the findings form the conclusion.

II. Current Effect on Wire-bonded Package Degradation

Because of the CTE mismatches among SiC die (2.77 ppm/K), Aluminum wires (23.5 ppm/K), solder material (15~30 ppm/K), wire bond interconnection and die attach solder layer are regarded as the weakest parts in the wire-bonded modules [24]. Extensive research demonstrated that several typical categories of failure mechanisms which are mainly dependent on the locations where the failure occurs [9], [24], [25]. The typical failure and fatigue modes and the corresponding parasitic resistance dependence are depicted in Fig.1.

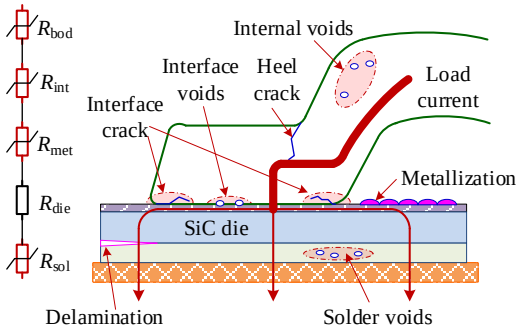

Fig.1. Fatigue modes in bond wires after power cycling test.

Accordingly, the parasitic resistance from bond wire to the copper layer consists of bond wire resistance (R_{bod}), interconnection resistance (R_{int}), Aluminum pad resistance (R_{met}), SiC die resistance (R_{die}) and die attach solder layer resistance (R_{sol}) [26]. Among them, R_{die} can be treated as constant without taking into account threshold voltage shift.

Due to the accumulative plastic strains caused by the large temperature extrusion, the cracks are most likely to occur at the tail of bond wires [21]. Moreover, the heel parts as well as the body part are also prone to cracks. With the increase of power cycles, the interface cracks could propagate inwards until the bond wire eventually lifts off. When the heel and body part of bond wires suffer from the temperature extrusion, especially from the ohmic self-heating, heel cracks are easy to occur because of the thermal expansion and contraction [27]. Recently, in the case of low ΔT_j tests, many interfacial voids and some random voids have been widely observed during both the thermal and power cycling tests [28], [29]. It is studied that the appearance of interfacial voids can be attributed to the oxide debris and particles among the interfaces. Due to the dislocation density of the atoms, these voids continue to develop and expand along with the number of power cycles.

Concerning the fatigue occurring throughout the bond wire body, some of them are far away from the interconnection part. For example, the top part of bond wires are less affected by the temperature swing than the self-heating which are related to the current density. Due to the existence of cracks, voids, and slip bands, an inhomogeneous current density would flow though the bond wires and lead to the uneven self-heating effect on them [30]. This uneven self-heating effects will get worse and worse with the growth of cracks and voids. The bond wire fatigue modes and the related dependences are listed in Table I.

Table I. Fatigue modes and ageing dependences of bond wires.

Fatigue modes in bond wires	Stress types	Major factors
Heel cracks	Mean T_j, T_j variation, t_{on}/t_{off}	Mismatch of CTE at the interface between bond wire and chip. It mainly depends on the ΔT_j related CTE mismatch
Interface voids	Mean T_j, T_j variation, t_{on}/t_{off}	
Interface cracks	Mean T_j, T_j variation, t_{on}/t_{off}	
Internal voids far away from interface	Mean T_j, T_j variation, current density induced self-heating and electron migration	Bond wire ohmic self-heating effects. It depends on parasitic resistance and current density
Internal cracks far away from interface	Mean T_j, T_j variation, current density induced self-heating and electron migration	

As shown in Table I, on the foundation of the physics-of-failure mechanisms, the reliability-related thermomechanical stresses, plastic strain and elastic energy stored in the bonding wire loop can also be affected by the current density and the related electromigration effect [31], [32]. The metal reconstruction is the most typical fatigue mode for the aluminium metallization. The reconstruction of surface would make uneven current distribution to the SiC die cells and also increase both R_{int} and R_{met}. Usually, the metallization fatigue is also mainly attributable to the high current density [33]. With regard to the second weakest part, the solder layer degradation rarely cause the notorious open-circuit failure in the tests. As depicted in Fig.1, delamination and voids are the main fatigue modes on the die-attach solder layer, which can also be attributable to both CTE mismatch and the current density effect.

In Table II, the ageing dependences about the die attach solder layer fatigues shown in Fig.1 are listed. The delamination usually starts at the edge and corner of the chip, and then continues to propagate from the outside to the centre of the chip [34], [35]. Theoretically, electromigration is the self-diffusion of metal (e.g. Aluminium) induced by the electric current, which can lead to the generation of voids and interconnect failure on the solder layer [36]–[38]. Recently, the electron migration related reliability issue has been taken into consideration at package-level as well as chip-level [37], [39]–[41].

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Table II. Fatigue modes and ageing dependences of die attach solder layer.

Fatigue modes in solder layer	Stress types	Major factors
Delamination	T_j variation, t_{on}/t_{off}, current density induced electron migration	Mismatch of CTE at the edge and corner of the die attach solder layer; Electron migration effect would accelerate the delamination under high current density
Interface voids	t_{on}/t_{off} duration, current density induced electron migration	Electron migration effect induced self-diffusion of Aluminium metal; T_j variation could accelerate the void expansion

Generally, the current density and the related electromigration effect have impact for both the degradation of bond wire and solder layer. In traditional PCT, since the temperature variation is proportional to the input current, the effect of current density and the temperature swing related CTE mismatch are coupled together. Hence, it is necessary to separate the current density effect on the failure mechanism of package degradation.

III. Constant Temperature Swing Control Method With Different Current Conditions

A. Problem statement in conventional DC-based PCT

In the conventional PCT methods, the SiC MOSFETs are usually driven with standard gate voltages, +18V or +20V. Then, the ΔT_j is obtained by the on-state conduction power losses using second-scale duration. The related temperature variation control method is plotted in Fig.2. To obtain the desired ΔT_j, the conduction power loss P_{cs} usually can be controlled by two control variables, the on-state period (t_{on}/t_{off}) and load current I_{load}. An external heat plate is used to control the case temperature (T_{case}). As long as the PCT system reaches a thermal equilibrium, the minimum junction temperature (T_{min}) falls back to the case temperature T_{case} at the end of t_{off} pulse. As shown in Fig.2, the effect of different temperature variation intertwine with the duty cycle and I_{load}. In the case of fixed t_{on}, the desired ΔT_j can only be adjusted by the input I_{load}. In order to investigate the current density effect on the bond wires independently, the temperature factors ΔT_j and T_{avg} should be separated from the load current.

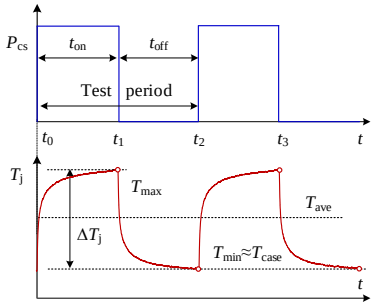

Fig.2. Conduction power loss and junction temperature swing pattern in DC-based tests.

B. Proposed test method

The appearance and equivalent circuits of single SiC MOSFET die are depicted in Fig.3. Thanks to the 4-terminal package with a Kelvin-source terminal (s), the gate loop does not contain the parasitic bond wire resistance R_{bw}. As a result, the increase of R_{bw} has no effect on the gate voltage V_{gs} during the long-term PCT process.

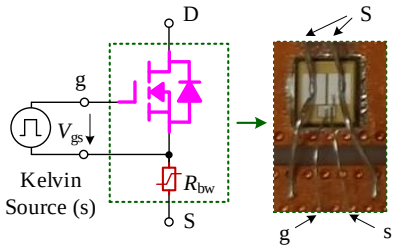

Fig.3. Commercial 4-terminal MOSFET containing a Kelvin-source terminal.

Unlike conventional test method with the fixed SiC gate voltages (+18V or +20V), a large V_{gs} adjustment control strategy is proposed to achieve the desired ΔT_j under different load current. In DC-based PCT, the power MOSFETs are operated in the linear region with relatively low drain voltage V_{DS}. Under fixed duty ratio (t_{on}/t_{off}) and base plate temperature, the expected ΔT_j in Fig.2 is proportional to the conduction loss P_{cs}, as expressed in

$$\Delta T_j \propto P_{cs} = \int_{t_2}^{t_3} V_{cp} I_{load} dt \quad (1).$$

Assuming the gate overdrive (V_{gs}-V_{th}) is larger than the Drain-to-source voltage V_{DS}, the Drain current I_D can be calculated by

$$I_{load} = I_D = \frac{Z\mu_{in}C_{ox}}{L_{CH}}\left[\left(V_{gs} - V_{th}\right)V_{DS}\right] \text{ for } |V_{DS}| << V_{gs} - V_{th} \quad (2).$$

Then V_{DS} can be expressed as

$$V_{DS} = \frac{I_{load}L_{CH}}{Z\mu_{in}C_{ox}}\frac{1}{\left(V_{gs} - V_{th}\right)} \text{ for } |V_{DS}| << V_{gs} - V_{th} \quad (3).$$

Where L_{CH} is the length of channel, Z is the width of channel, C_{ox} is the specific capacitance of the gate oxide layer and μ_{in} is the electron mobility in the inversion layer. Furthermore, the μ_{in} is temperature-dependent parameter, which can be obtained by

$$\mu_{in} = \mu_0\left(\frac{T_j + 273}{300}\right)^{-k} \quad (4).$$

Where μ_0 is constant related to the electron mobility and semiconductor processing and the exponent k varies from 1 to 2.5 [42]. Hence, the die voltage V_{cp} is a function of gate voltage V_{gs} and load current I_{load} under given T_j, as shown below

$$\Delta T_j \propto P_{cs} = \int_{t_2}^{t_3} \frac{I_{load}L_{CH}}{Z\mu_{in}C_{ox}}\frac{1}{\left(V_{gs} - V_{th}\right)} I_{load} dt \quad (5).$$

From (4) and (5), the ΔT_j related conduction loss P_{cs} can be expressed as

$$\Delta T_j \propto P_{cs} = \frac{I_{load}^2 L_{CH}}{Z\mu_0 C_{ox}}\int_{t_2}^{t_3} \frac{(T_j + 273)^k}{\left(V_{gs} - V_{th}\right)} dt \quad (6).$$

Assuming T_j increases from t_2 to t_3, the desired ΔT_j can be adjusted by both I_{load} and V_{gs} for the given MOSFET. In order to achieve the same ΔT_j under different load current, V_{gs} should be calculated and adjusted correspondingly. The typical output characteristics of SiC MOSFETs under different V_{gs} in the linear region are plotted in Fig.4. Besides, the related definitions labeled in Fig.4 are listed in Table III. For the higher load current Iload1, the voltage difference (V_{cp2}-V_{cp1}) under desired

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ΔT_j (T_{jH}-T_{jL}) should be limited in a relatively low value. In the case of fixed ton, the desired ΔT_j under different load current can be achieved by the law of equivalent area

$$I_{load1}(V_{cp2}-V_{cp1})\Big|_{V_{gs1}} = I_{load2}(V_{cp4}-V_{cp3})\Big|_{V_{gs2}} \quad (7).$$

By means of the quantitative V_{gs} adjustment, the on-state power losses under different I_{load} can be equal.

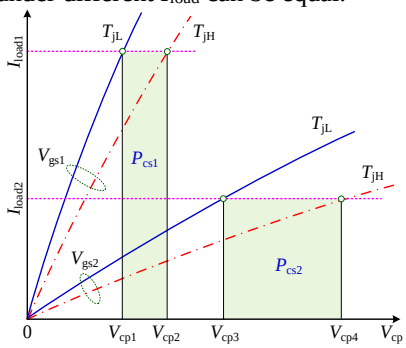

Fig.4. SiC MOSFET Output characteristics under different temperatures and gate voltages.

TABLE III. ELECTRICAL DEFINITIONS UNDER DIFFERENT V_{GS} AND TEMPERATURES

Notification	Condition 1	Condition 2
Planned load current	I_{load1}	I_{load2}
Gate voltage	V_{gs1}	V_{gs2}
Maximum T_j	T_{jH}	T_{jH}
Minimum T_j	T_{jL}	T_{jL}
Conduction power loss	P_{cs1}	P_{cs2}

IV. EXPERIMENTAL PLATFORM AND TEST CONDITIONS

A. Module Under Test

The devices under test are two six-pack modules (CREE CCS020M12CM2). The module consists of three identical half-bridge substrates. The maximum allowable operation T_j is 150 °C, and the internal layouts of the six SiC dies are depicted in Fig.5. For each SiC die, there are two bond wires used to carry the load current and another two thinner bond wires for the gate driver loop.

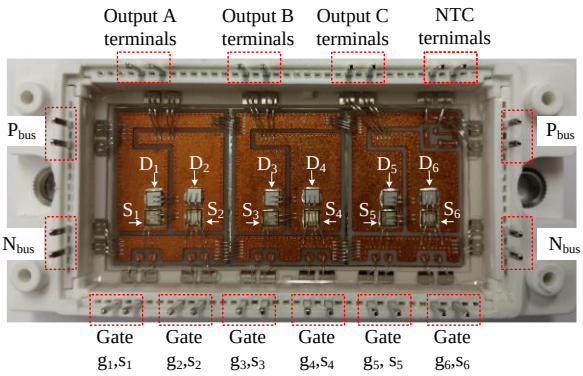

Fig.5. Layouts for the module under test (CREE CCS020M12CM2).

The half-bridge schematic and the measurement proposal are depicted in Fig.6. The independent measurement method for the bond wire and die resistances proposed in [43] is applied to the dies under test. Taking the first die S_1 as an example, its bond wire voltage V_{bw1} can be measured by the gate auxiliary terminal s_1 and the output power terminal T_{OA}. Meanwhile, the die voltage V_{cp1} under constant I_{load} can be measured by the positive bus terminal P_{bus} and the gate auxiliary terminal s_1. During the test, both the die voltage and bond wire voltage are measured and recorded simultaneously, and the increased V_{bw1} can be attributed to the bond wire R_{bw1} degradation.

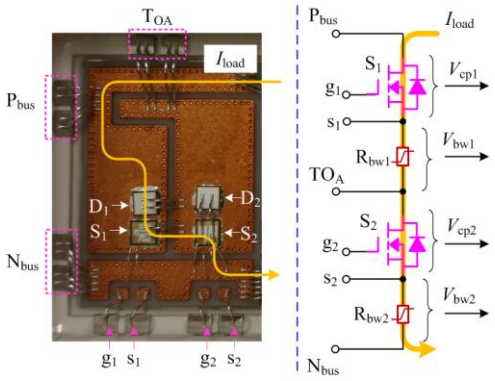

Fig.6. Half-bridge schematic and bond wire voltage measurement.

For S_1 in Module A, the output characteristic curves under different junction temperatures are plotted in Fig.7. Since the electron mobility varies inversely with the temperature, the on-state voltage V_{DS} increases with the increasing T_j under fixed I_{DS}. Assuming the desired ΔT_j ranges from 25°C to 175°C, the average power loss Pcs under I_{DS}=24 A is around 73.2W while Pcs equals to 11.3W at 12 A condition. It is also proved that the conduction power loss is proportional to fixed I_{DS} within the given turn-on duration. In order to get the same T_j swing under different I_{DS}, the gate voltage is required to be adjusted accordingly.

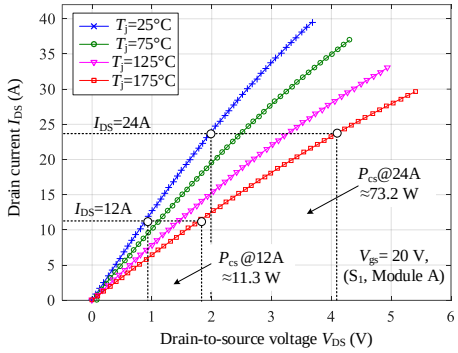

Fig.7. Output characteristic curves under different junction temperature.

B. On-line T_j measurement

The on-line T_j measurement without gel removal is achieved by the isolated optical fibers from Opsens and the implementation is depicted in Fig.8. The part number of optical fiber is OTG-F-10 with 5 ms response time, as shown in Fig.8 (a) [44]. In order to hold the optical fiber during operation, a precision manipulator is applied to the optical fiber. It is worth noting that the measured T_j merely represents the temperature of the contact point. In practice, the sensor of optical fiber is placed at the center of the inspected SiC die.

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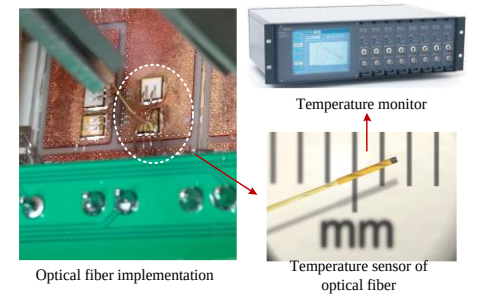


Fig.11. Online junction temperature measurement implementation using optical fiber.

C. Test conditions and experimental results

In order to investigate the current density effects on the bond wires, two SiC modules (labeled Module A and Module B) were tested. The desired ΔT_j for both modules are controlled in the range of 65°C to 125°C with the same test conditions except for the Drain current injection. The test conditions for the two SiC-MOSFET modules are listed in Table IV.

TABLE IV. TEST CONDITIONS FOR CREE MODULES.

Parameters	Module A	Module B
Maximum T_j	125 °C	125 °C
Minimum T_j	65 °C	65 °C
ΔT_j	60 °C	60 °C
t_{on}/t_{off}	2s / 4s	2s / 4s
Load current	24 A	12 A

The output characteristics of Module A under different gate voltages are plotted in Fig.9. Because of the discrepancies in the manufacturing process, the six dies present different output characteristics under the same static test conditions. Therefore, six independent gate drivers with adjustable output voltages were used in the tests.

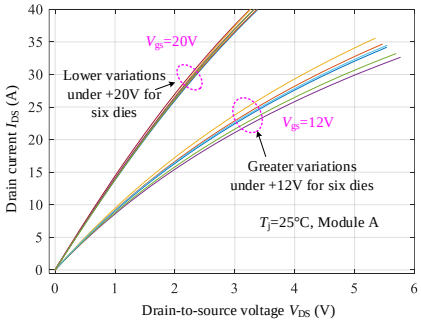


Fig.9. Output characteristic curves for six dies for module A.

In Table V, the practical gate voltages for the constant ΔT_j under two load current conditions are recorded.

TABLE V. GATING VOLTAGES FOR CREE MODULES.

Gate voltage adjustment	S_1	S_2	S_3	S_4	S_5	S_6
Module A: +24A, 65°C~125°C	18.9 V	19.6V	21.1V	19.7V	21.4V	20.6V
Module B: +12A, 65°C~125°C	7.9 V	7.9V	8.0V	8.0V	8.1V	7.9V

The temperature variations for the high-side three dies of Module A at the beginning of the test are depicted in Fig.10. The measured T_j swings are in the range of 65°C~125°C.

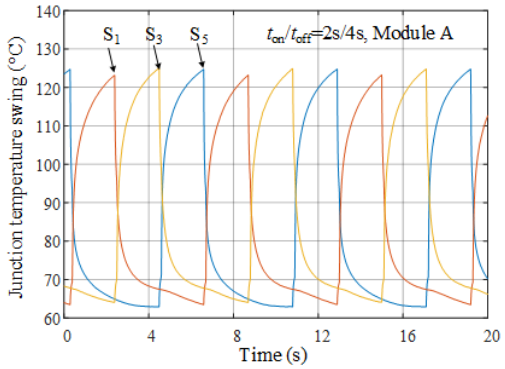
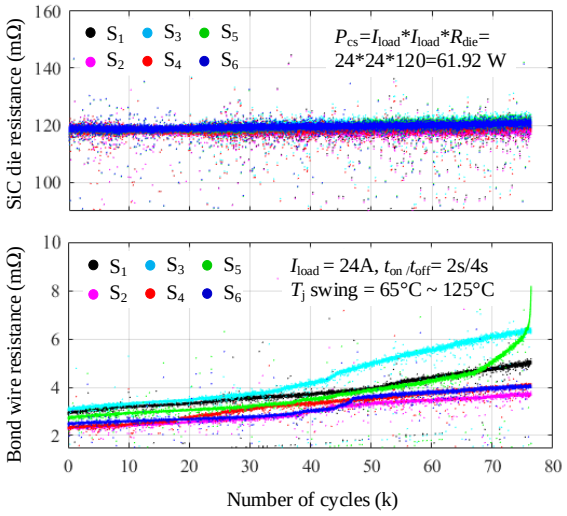


Fig.10. Online junction temperature measurements for high-side three dies of Module A.

In Fig.11.(a) and (b), the on-line record for SiC die and bond wire resistances under two current conditions are depicted, respectively. Due to the layout differences, the initial bond wire resistances are not the same [45]. In this study, the measured high-side bond wire resistances are higher than the low-side bond wire resistances, which are consistent with the load current path depicted in Fig.6. As shown in Fig.11 (a), the die resistances for six dies of Module A remain around 120 mΩ throughout the test. The corresponding conduction power loss P_{cs} is around 61.92W. After 76k power cycles (N_{cyc}), the R_{bw} of S_1 increased by 300% and then the test was stopped. This excess R_{bw} increase implies the contact area between bond wire and SiC die is dramatically reduced.



(a)

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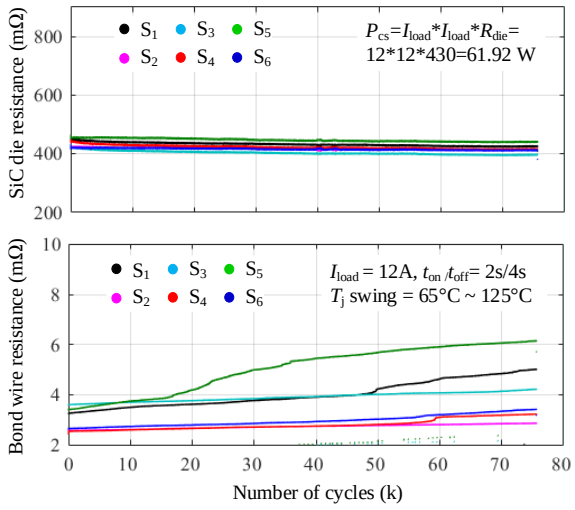


(b)

Fig.11. Online measurement and record for bond wire and die resistances (a) I_{load}=24A and end-of-test N_{cyc} ≈76 k. (b) I_{load}=12A and end-of-test N_{cyc} ≈76 k.

In order to make a better comparison, the Module B is also stopped after 76k cycles' test. The ageing curves for Module B (I_{load} = 12A) are depicted in Fig.11 (b). It is shown that the average die resistance for the six SiC dies is around 430 mΩ under lower gate voltages. Even though the load current is 12A, the conduction power loss Pcs could also be kept around 61.92W for the same T_j swing.

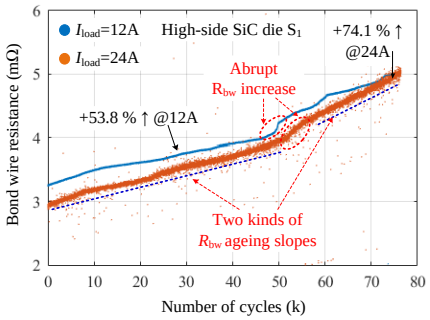
V. Comprehensive Analysis and Discussion

A. Ageing process comparison

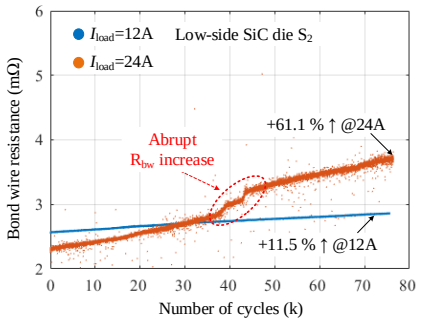
The online bond wire resistance measurements under two current conditions after 76k power cycles are compared individually and plotted in Fig.12. Considering the layout difference among the six dies, the ageing curves are only compared for the dies with the same layout in the module. Fig.12 illustrates two kinds of ageing trend in the test, one is the linear growth with N_{cyc} increase, and the other is step R_{bw} increase along with a subsequent steeper linear growth.

As can be seen from all the sub figures, there is a linear ageing process under fixed test conditions in the beginning stages. It is shown that the higher the load current, the steeper the ageing slope. The typical linear ageing process can be found in Figs.12 (b), (c) and (f) under I_{load}=12A condition (see blue curves). These linear ageing processes indicate that the constant temperature stresses (ΔT_j and T_{avg}) have uniform degradation effect on the bond wire resistance. Before stopping the test of Module B, the measured bond wire resistances for S_2, S_3, and S_6 are increased by 11.5%, 17.2% and 28.7%, respectively. In this scenario, the follow-up R_{bw} increase can be easily estimated by an approximate linear model.

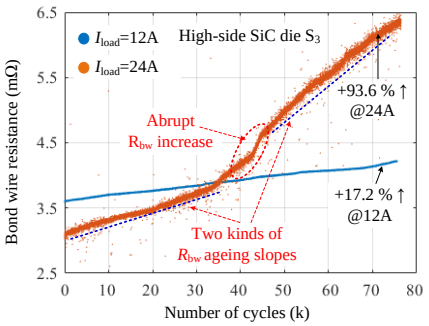
For the second ageing trend, this kind of abrupt R_{bw} increase is usually present at the end of test. Once the abrupt R_{bw} increase occurs, the bond wires under test start to get into an accelerated process, and the bond wires would lift off the die within a short period. The increased bond wire resistance under high current could lead to a higher self-heat effect and then accelerate the follow-up bond wire degradation, as demonstrated in Figs.12 (a), (c) and (f). Notably, in the case of I_{load}=24A, the bond wires continue to keep almost the same ageing pace after the sudden R_{bw} increase, as shown in Fig.12 (b) and Fig.12 (f). The significant abrupt increases can be attributable to the cracks and sudden delamination, which are related to high current density rather than CTE mismatch. However, in the case of low current density (I_{load}=12A), such as Figs.12 (b), (c) and (f) do not show significant sudden R_{bw} step increase in the tests. Since the two modules experienced the same T_j conditions and power cycles, Module A has higher ageing speed and more abrupt R_{bw} increases than Module B due to the higher current density.



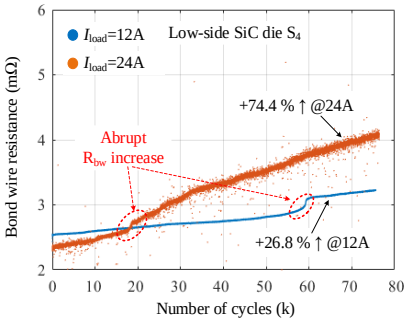
(a)



(b)



(c)



(d)

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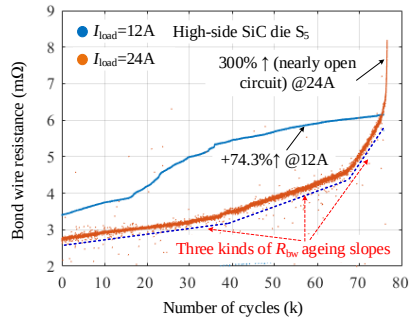
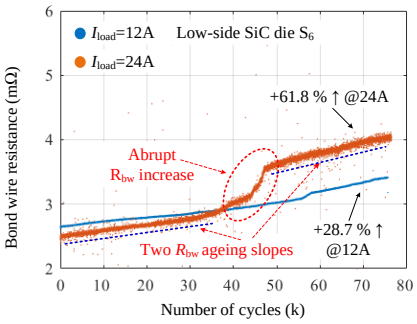


(e)



(f)

Fig.12. Comparisons of online bond wire resistance measurements under different current conditions after 76k cycles. (a) die S1, (b) die S2 (c) die S3 (d)S4 (e) die S5(f) die S6.

In particular, a variable ageing rate process without any abrupt R_{bw} increase is shown in Fig.12 (e). In Fig.12 (e), there are three kinds of straight ageing slope under I_{load}=24 A condition. After 38k cycles, the ageing rate starts to increase for the first time. Then, it changes the ageing rate again after 67k cycles. The measured R_{bw} increases quickly and the bond wire appears lift off behavior within 10k cycles. The ageing curve plotted in Fig.12 (e) implies that the higher current density can change and accelerate the ageing slope even without the sudden R_{bw} increase.

Generally, compared with the ageing processes under low current conditions, the modules under high current tests shown higher ageing rate in terms of abrupt R_{bw} increase and variable ageing rate. For an overall comparison, the ageing speed can be evaluated by using increase rate R_{rate}

$$R_{rate} = \left(\frac{R_{end}}{R_{ini}} - 1 \right) 100\% \qquad (8).$$

Where R_{end} is measured bond wire resistance at the end of test, R_{int} is the initial measured resistance. The increase rates for the six SiC dies after 76k cycles are summarized in Fig.13. It is shown that all the increase rates under I_{load}=24A are higher than the increase rates under I_{load}=12A. In the case of higher current density, the wire bonded packages are subjected to higher self-heating and electro-migration effect. As a result, the bond wires degrade faster even under the same temperature swings.

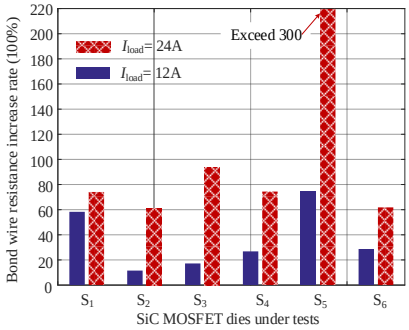
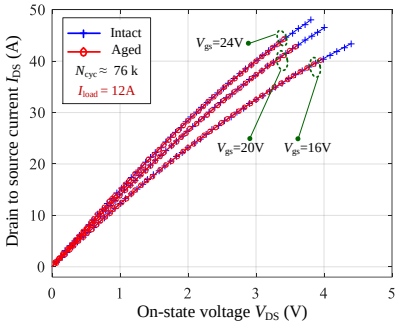


Fig.13. Comparisons of bond wire resistance increase rates for six SiC dies at different current conditions.

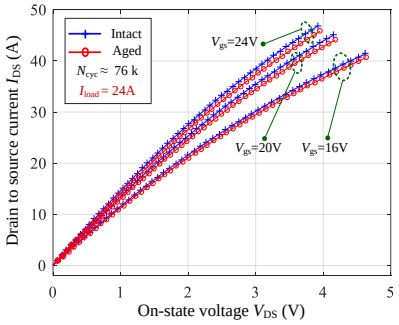
B. Ageing process comparison

By means of the B1506A power device analyzer, three kinds of electrical parameters are selected and compared: output characteristic, transfer characteristic and on-state resistance. All the static tests are conducted under constant temperature room environment, and the room temperature is around 25 °C.

In Fig.14, the measured output characteristic comparisons before and after the tests are depicted. As shown in Fig.14 (a), there is almost no obvious degradation in the output characteristic curves under different gate voltages. In the case of 24A, the slopes of output characteristic curves for the aged die are lower than the initial measurements. This lower slope means that the conduction losses would increase during the ageing process even under the same working conditions. According to the comparisons, the die S_3 shows significant degradation under I_{load}=24A condition and these results are consistent with the ageing curves plotted in Fig.12 (c).



(a)



(b)

Fig.14. Output characteristic curve comparisons before and after power cycling tests for S_3: (a) I_{load}=12A and T_j=25°C, (b) I_{load}=24A and T_j=25°C.

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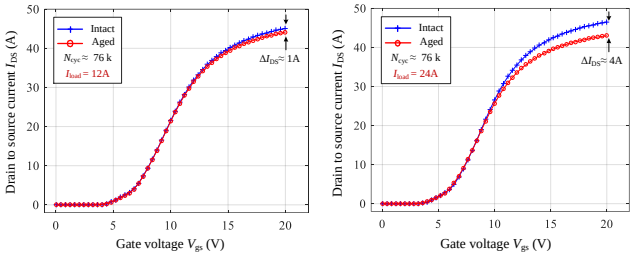
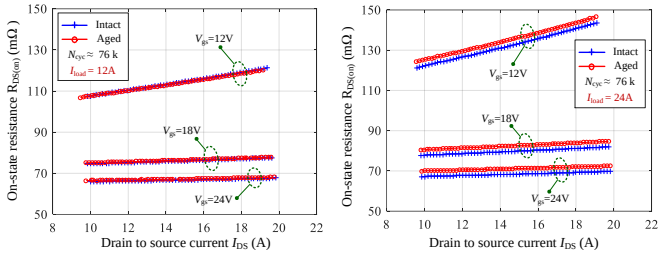
In Fig.15, the transfer characteristic curves before and after tests are compared and plotted. Theoretically, transfer characteristic curve indicates how drain current increases with gate voltage under a given Drain-to-source voltage V_{DS}. Moreover, the slope of transfer characteristic curve is the trans-conductance of the device. Compared with the initial curves, both two dies show the evidence of degradation. However, in the case of V_{gs}=20V, the measured drain current I_{DS} under I_{load}=24A decreased by 4A, which is greater than the results under I_{load}=12A. The slight negative slopes imply that switching speed would become slower under V_{gs}=20V after the power cycling tests.



(a) (b)

Fig.15. Transfer characteristic curve comparisons before and after power cycling tests for S_3: (a) I_{load}=12A and T_j=25°C, (b) I_{load}=24A and T_j=25°C.

In Fig.16, the measured on-state device resistances before and after the power cycling test are plotted and compared. It is worth noting that the measured on-state resistance $R_{DS(on)}$ from B1506A is a combination of die resistance and parasitic resistances including bond wire resistance, copper layer resistance and Aluminum pad resistance.

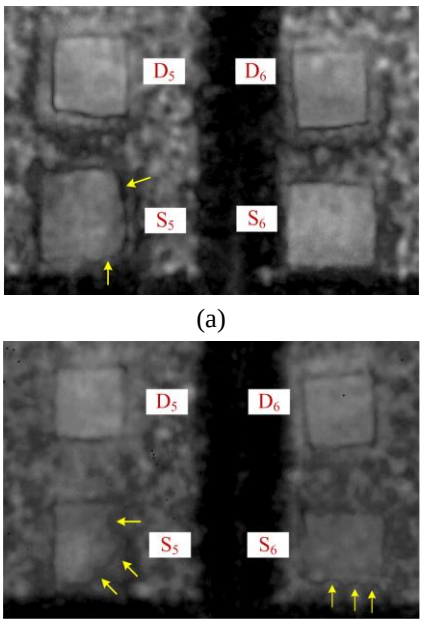


(a) (b)

Fig.16. Measured on-state resistance comparisons before and after power cycling tests for S_3: (a) Module A, I_{load}=12A and T_j=25°C, (b) Module B, I_{load}=24A and T_j=25°C.

Referring to Fig.11 (a), the measured $R_{DS(on)}$ do not significantly change after power cycling tests. According to the results in Fig.12 (e), the bond wire increase is less than 1 mΩ, which can hardly affect $R_{DS(on)}$. However, in the case of I_{load}=24A shown in Fig.16.(b), the visible changes about 3.3 mΩ increase can be detected, and the measured results are consistent with the recorded curve in Fig.12 (e).

In Fig.17, the Scanning Acoustic Microscopy (SAM) images for die attach solder degradation are shown. The freewheeling diodes D_5 and D_6 have not been tested, so the diode SAM image can be regarded as reference compared with SiC dies. In Fig.17 (a), there are no visible degradations on D_5, D_6 and S_6 under I_{load}=12A conditions. For S_5, there is a slight delamination on the right side and the bottom-right corner. In general, the die attach solder layer maintain a healthy state of interconnection. However, in the case of I_{load}=24A shown in Fig.17 (b), the delamination on S_5 is worse than the die under lower current condition. More significant delamination can be found from the right side and the bottom-right corner. Besides, a slight delamination can be observed on the bottom side on S_6.



(a)

(b)

Fig.17. SAM images of die attach solder layer after 76k temperature cycles (a) Module A, I_{load}=12A, T_j=65 °C~125 °C (b) Module B, I_{load}=24A, T_j=65 °C~125 °C.

It is confirmed that different current conditions have a great impact on the die attach solder layer degradation even under the same T_j swing conditions. Compared with the typical Si-based semiconductor die (13 mm^2), the active area of SiC die (4.2 mm^2) is smaller in the SiC MOSFET modules [46]. In order to alleviate the high current density effect on the package of SiC modules, the number of bond wire needs to be increased from the manufacturing point of view. Moreover, in a real application using SiC modules, the duration time of over-current operation should be limited, which would also accelerate the bond wire degradation in SiC MOSFET power modules.

VI. Conclusion

This paper has presented a separate test method for SiC MOSFET modules in power cycling test. Through adjusting the gate voltage, the on-state die resistance can be adjusted under the given current. Therefore, the conduction losses and related temperature swing can be changed accordingly by using gate voltage rather than load current. The SiC MOSFET modules with wire-bonded package can be tested under different current densities but with the same temperature conditions. Hence, the current density effect can be evaluated separately under the framework of conventional PCT standards. Results shown that different current densities have different impacts on both the bond wire resistance and die-attach solder layer. The module under higher current test condition shown faster ageing speed. Besides, more abrupt degradation can be found in the bond wire resistances in the case of higher current. It is experimentally validated that the package degradation rate is related to the current effect as well as the temperature swing and average

temperature. By using a power device analyzer, the static parameters were measured and compared before and after power cycling tests. The analysis and comparisons are consistent with the PCT monitoring measurement results. With the help of scanning acoustic microscopy, a delamination effect can be observed and confirms the involvement of current in the aging effect. Finally, the experimental results and analysis validated the effectiveness of proposed method.

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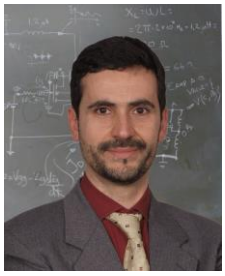

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