Study of Various Faults on Physical Level using Microwind2

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ABSTRACT
In this contribution, we present microwind2 based fault simulation environment. Many faults may occur on the circuit level as well as physical level. To fulfill our goal, the layout design of BCD to Excess-3 code converter is taken and the effect of various faults such as latchup, distribution of RC effect, input waveform slope and bridging fault are seen. The effect of these faults are examined on the various foundries of cmos: 0.12 μm, 0.18 μm, 0.25 μm and 0.8 μm. Experimental and simulation results show the effect of faults on layout design.

KEYWORDS
DSCH2, microwind2, latchup fault, input waveform slope, RC effect, bridging fault.

1. INTRODUCTION
CMOS (Complementry Metal Oxide Silicon) technology played a significant role in the global integrated circuit industry, because it has several advantages i.e. low power dissipation, excellent noise immunity, high packing density and a wide range of supply voltages. But, during the operation of circuitry, versatile faults take place which result degradation in cmos parameters.

In a conventional silicon gate process an MOS device requires a gate-forming region and a source/drain-forming region, which consists of diffusion, polysilicon and metal layers separated by insulating layers.

Many faults have detected on the circuit level in previous year papers. Transient bit-flip faults detected in sequential elements of a digital design[1], the effect of faults is seen on cryptographic design. The speed of fault detection is also important parameter. The effect of open switch fault is seen on the five-leg converter [2] where converter has five legs before the fault occurrence and after fault occurrence the converter continues function with four legs. When any device is in process, then its speed should be controllable, the modeling and FPGA implementation of a PMSM speed controller is done [3]. Ionizing radiation has also major effect on digital electronics [4], which causes of logical faults. Faults may occur on the on- chip design substations due to the power consumption.

In this paper, we design the BCD to excess-3 code converter and determine the effect of various faults on layout design. Because occurence of faults is responsible for more power consumption which is the most important parameter of cmos. Power consumption is calculated on various foundries.

In section 2, design of bcd to excess-3 code converter is shown with its timing diagram. In section 3, the impact and analysis of various type of faults are presented on layout design. Section 4 reveals the effect using experimental results. Section 5 gives the conclusion.

2. DESIGN OF BCD TO EXCESS-3 CODE CONVERTER
Here design of BCD to excess-3 code converter is shown in which four bits a, b, c, d are taken to represent input signal and corresponding bits w, x, y, z show the behaviour with respect to the bits.

Table.1 Truth Table

BCD				Excess-3			
a	b	c	d	w	x	y	z
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0

Now, we shall study about the impact of faults on the layout design, we see that how power consumption parameter is affected from the faults in section 3.

3. IMPACT OF FAULTS
Complementry MOS circuits take advantage of the fact that both n-channel and p-channel devices can be fabricated on the same substrate. CMOS circuits consist of both types of MOS devices interconnected to form logic functions [6]. In either logic state, one MOS transistor is on while the other is off, the dc power dissipation of the CMOS circuit is extremely low, usually on the order of 10 nW.

3.1 Latch up fault
The source of the latch up effect can be explained by examining the process cross section of a CMOS inverter [7].

The schematic depicts, in addition to the expected nmos and pmos transistors, a circuit composed of an npn-transistor, a pnp- transistor and resistors connected between the power and ground rails. This parasitic circuit draws a large current above some critical voltage. This results in a short circuit.

For latch up to occur, the parasitic npn- pnp circuit has to be triggered. Two distinct methods of triggering are possible:-

(1) Lateral triggering

(2) Vertical triggering

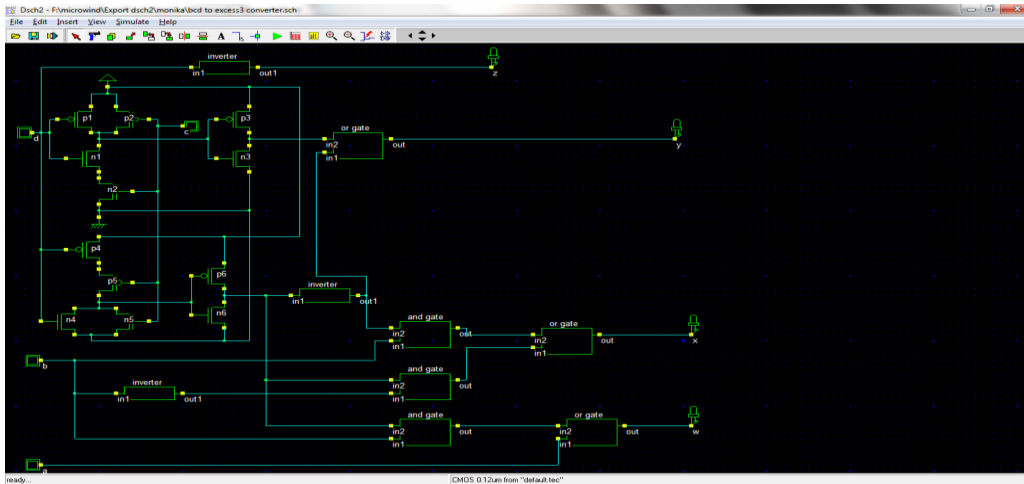

Fig. 1 Circuit design of BCD to Excess-3 code converter

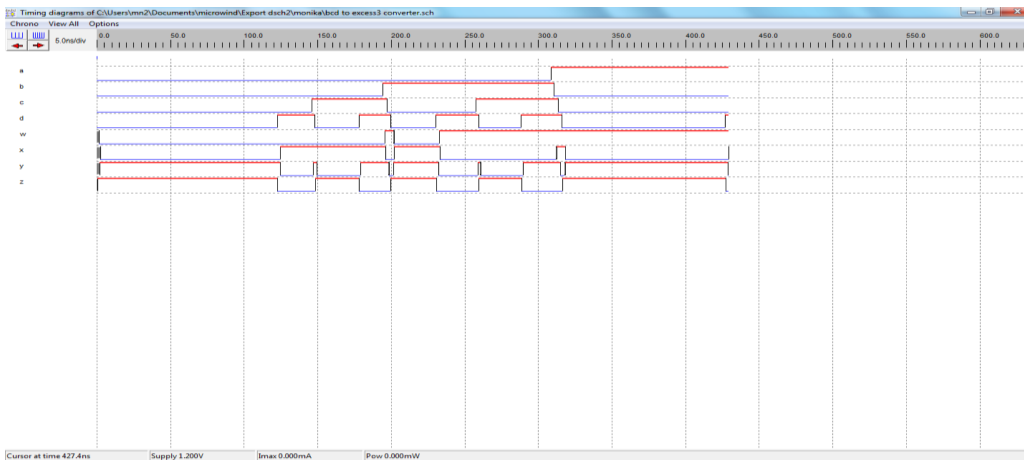

Fig. 2 Timing diagram

$$I_{ntrigger} \approx \frac{V_{pnp-on}}{\alpha_{npn} R_{well}}$$

V_{pnp-on} = 0.7V

α_{npn} = common base gain

R_{well} = well resistance

From above, we can see that if R_{well} resistance increases triggering current becomes small and at the small value of $I_{ntrigger}$, parasitic transistor is triggered. To examine the effect of this fault, we take the value of R_{well} $100\,\Omega$.

Vertical triggering occurs when a sufficient current is injected into the emitter of the vertical pnp- transistor.

Lateral triggering occurs when a current flows in the emitter of the lateral npn- transistor. The static trigger point is set by

Latch up depends on the pulse widths, speed of the transistor.

For latch up condition

$$\alpha_{npn} + \alpha_{pnp} = 1$$

Where, $\alpha_{npn} = \frac{I_{cn}}{I_{en}}$, $\alpha_{pnp} = \frac{I_{cp}}{I_{EP}}$

3.2 Distributed RC effects

The propagation of a signal along a wire depends on many factors, including the distributed resistance and capacitance of the wire, the impedance of the driving source and the load impedance [7].

For very long wires, propagation delays caused by distributed resistance capacitance (RC) in the wiring layer can dominate. This transmission line effect is particularly severe in poly wires because of the relatively high resistance of this layer.

A long wire can be represented in terms of several RC sections. The response at node V_j with respect to time is then given by

$$C\frac{dV_j}{dt} = (I_{j-1} - I_j)$$

$$= \frac{(V_{j-1} - V_j)}{R} - \frac{(V_j - V_{j+1})}{R}$$

If the number of sections in the network becomes large, the above expression reduces to the differential form:

$$rc\frac{dV}{dt} = \frac{d^2V}{dx^2}$$

Where x= distance from input

r= resistance per unit length

c= capacitance per unit length

a discrete analysis of the circuit shown in figure gives an approximate signal delay of

$$t_n = 0.7 \times \frac{RCn(n+1)}{2}$$

Where n= number of sections

As n becomes very large, this reduces to $t_1 = 0.7\frac{rcl^2}{2}$

Where r= resistance per unit length

c= capacitance per unit length

l= length of the wire

The l^2 term in equation shows that signal delay will be totally dominated by this RC effect for very long signal paths.

To examine this effect, we take the value of R is 50 Ω and C is 0.05 pf.

3.3 Input waveform slope

If any circuit consists of many inputs, then different slope of the input waveforms can modify the delay of a gate. When the input rises or falls rapidly, the delay of the charge or discharge path is determined by the rate at which the transistors in the path can charge or discharge the capacitors in the tree. When the input changes slowly, it will contribute to the output delay. The rise time is given by

$$t_{dr} = t_{dr-step} + \frac{t_{input-fall}}{6}(1-2p)$$

Where

$t_{dr-step}$ = the step-input rise time calculated in equation

$t_{input-fall}$ = the input fall time

$$p = \frac{V_{tp}}{V_{DD}}$$

$$t_{dr-step} = A_p\frac{C_L}{\beta_p}$$

A_p = process constant for a specific supply voltage.

$$A_p = \frac{1}{V_{DD}(1+p)}\left[\frac{-2p}{1+p} + \ln\left(\frac{2(1+p)-V_0}{V_0}\right)\right]$$

Similarly,

$$t_{df} = t_{df-step} + \frac{t_{input-rise}}{6}(1+2n)$$

$$n = \frac{V_{tn}}{V_{DD}}$$

This is valid for input rise or fall times that satisfy the following criteria:

$$\frac{t_{input-rise}\beta_p V_{DD}}{C_L} < \frac{6p}{(1-p)^3}$$

and

$$\frac{t_{input-fall}\beta_n V_{DD}}{C_L} < \frac{6n}{(1-n)^3}$$

Three factors on which delay time depends:

(1) t_d is directly proportional to load capacitance (C_L).

(2) t_d is inversely proportional to supply voltage (V_{DD}).

(3) t_d is inversely proportional to β.

To examine this fault we give the different time to the all input signals like low time (t_l) 0.775 ns for input ‘d’, 1.540 ns for input ‘c’, 2.975 ns for input ‘b’ and 7.975 ns for input ‘a’ . μm

3.4 Bridging fault

With the increase in the number or devices on the VLSI chips, the probability of shorts between two or more signal lines has been significantly increased. Unintended shorts between the lines form a class of permanent faults, known as bridging faults [8]. It has been observed that physical defects in MOS (Metal oxide semiconductor) circuits are created as bridging faults more than as any other type of fault. Bridging faults can be categorized into three groups:

Input bridging

Feedback bridging

Non feedback bridging

The probable bridging fault in the circuit (or in any other CMOS circuit) can be grouped into four categories.

Metal poly silicon short

(2) Poly silicon n-diffusion short

(3) Poly silicon p-diffusion short

To examine the effect of this fault, we take metal poly silicon shorting. Here four layout designs are shown below.

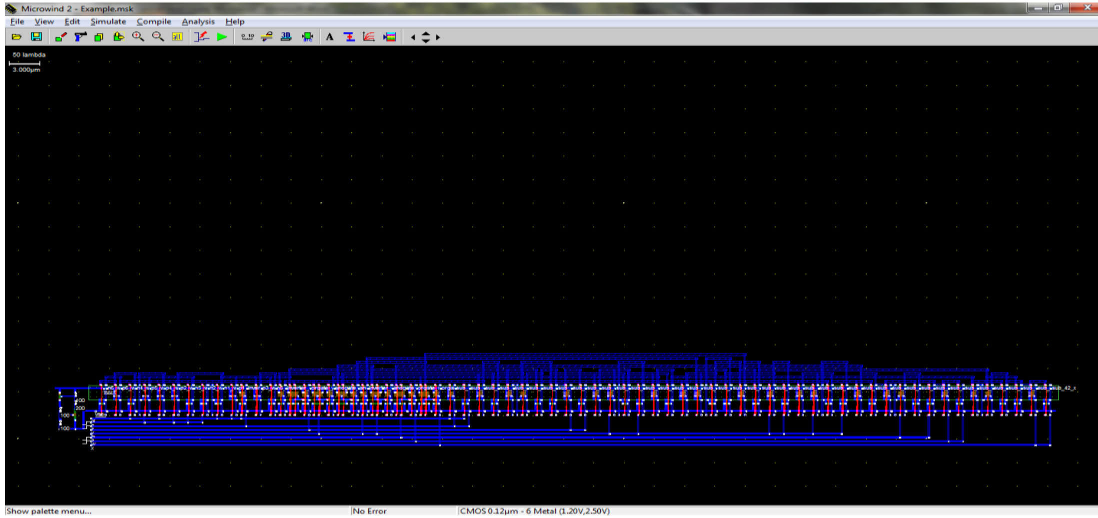

Fig. 3 Layout design of latch up fault

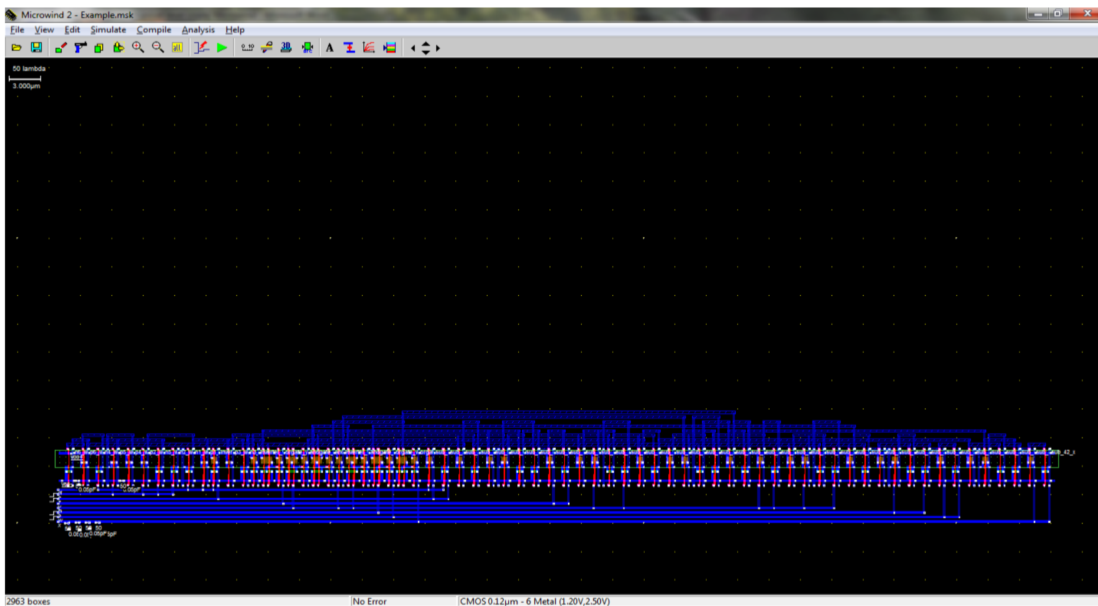

Fig.4 Layout design of distributed RC effect

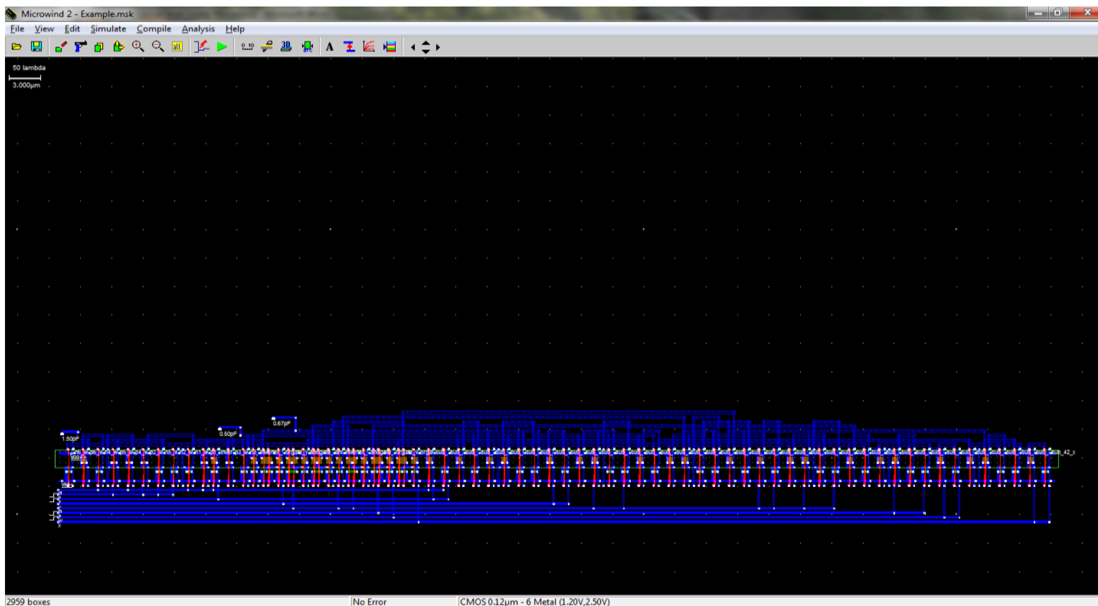

Fig.5 Layout design of input waveform slope

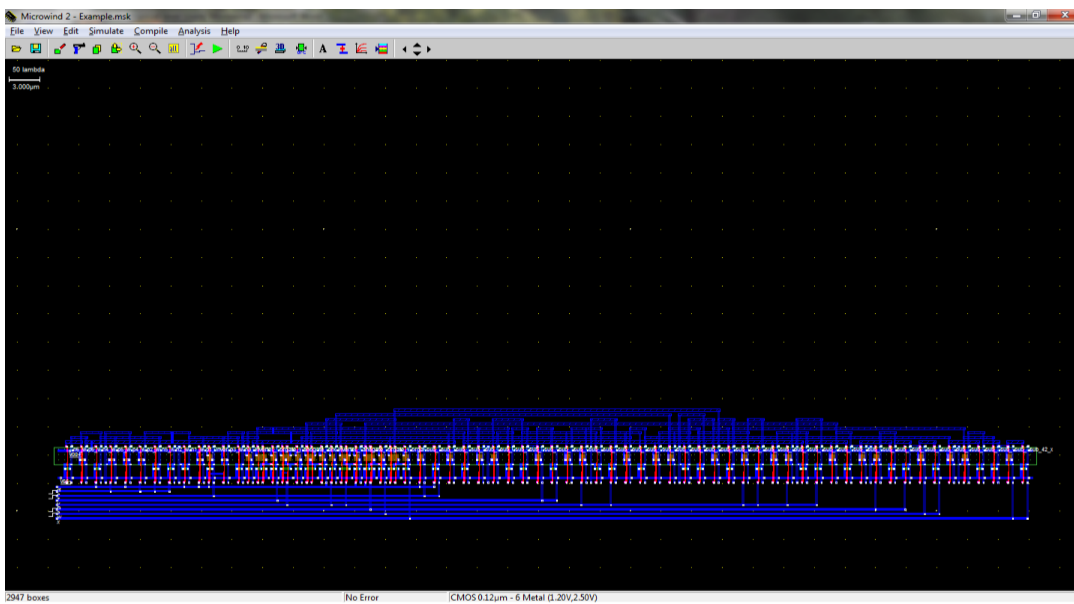

Fig.6 Layout design of bridging fault

4. EXPERIMENT RESULTS

Cmos foundry	Without fault(mW)	Latch up fault (mW)	RC-effect (mW)	Input waveform slope (mW)	Bridging fault (mW)
0.12 μm	0.767	0.801	0.932	0.766	1.105
0.18 μm	0.418	0.424	0.738	0.412	0.801
0.25 μm	0.924	0.877	1.011	0.924	1.175
0.8 μm	0.370	0.698	0.368	0.365	0.424

5. CONCLUSION

Here we see that the various faults influence the different foundry in a different manner.

We saw the effect of faults that are following:

(a) Latch up

(b) Distributed RC effect

(c) Delay fault on the input waveform

(d) Bridging fault

Power consumption plays widespread role on any level design. In order to proper operation of any circuit, it requires that it gives desired output at the low power consumption. But during the process, many faults occur which are responsible to enhance the power consumption.

So, if we use optimization of the parameters, we can control the power consumption.

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