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# Sub-10 nm Carbon Nanotube Transistor

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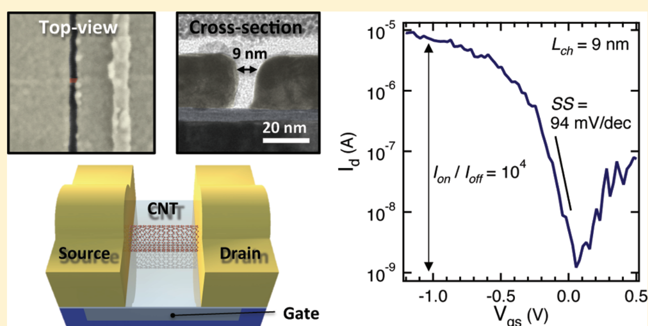
S *Supporting Information*

**ABSTRACT:** Although carbon nanotube (CNT) transistors have been promoted for years as a replacement for silicon technology, there is limited theoretical work and no experimental reports on how nanotubes will perform at sub-10 nm channel lengths. In this manuscript, we demonstrate the first sub-10 nm CNT transistor, which is shown to outperform the best competing silicon devices with more than four times the diameter-normalized current density (2.41 mA/μm) at a low operating voltage of 0.5 V. The nanotube transistor exhibits an impressively small inverse subthreshold slope of 94 mV/decade—nearly half of the value expected from a previous theoretical study. Numerical simulations show the critical role of the metal−CNT contacts in determining the performance of sub-10 nm channel length transistors, signifying the need for more accurate theoretical modeling of transport between the metal and nanotube. The superior low-voltage performance of the sub-10 nm CNT transistor proves the viability of nanotubes for consideration in future aggressively scaled transistor technologies.




**KEYWORDS:** *Carbon nanotube, field-effect transistor, sub-10 nm, transistor scaling, CNTFET*

Within the next decade, computing technology will require transistors with channel lengths ($L_{ch}$) below 10 nm.[1,2] In Si metal-oxide-semiconductor field-effect transistors (MOSFETs), the workhorse of integrated circuits, as $L_{ch}$ shrinks, the ability to effectively control electrical current in the transistor diminishes, a cost known as short-channel effects. It has been known for some time that the bulk-Si MOSFET will not perform reliably at sub-10 nm gate lengths.[1] Potential solutions to enable continued MOSFET scaling are to modify the Si device structure, as with the recently unveiled fins for the 22 nm technology node,[3] or incorporate a new channel geometry/material.[2,4,5] For years, single-walled carbon nanotubes (CNT) have been promoted as a replacement for Si owing to their superior electrical properties and ultrathin body.[4−10] Nanotubes are comprised of a single atomic layer of graphene rolled into a 1−2 nm diameter seamless cylinder and have exhibited ideal, ballistic carrier transport.[6,7] Because of their ultrathin body, the ability to maintain gate control of the current in a CNT transistor—thus avoiding short-channel effects—should be better than for other competing structures, such as realizable nanowires or fins.

Despite the considerable motivation over the years for transistors with ultrathin CNT channels, the available theoretical projections suggest a severe increase in inverse subthreshold slope ($SS = (d(\log_{10} I_d)/dV_{gs})^{-1}$) at $L_{ch} < 15$ nm.[11,12] Increased $SS$ denotes a loss of gate control, which is primarily a result of weakened electrostatics in the scaled channel and/or quantum mechanical tunneling of carriers through the channel energy barrier. Such source-drain tunneling is considered especially damaging in CNTs because the carrier effective masses can be substantially lower than in other semiconductors. Also anticipated from theory is a loss of drain current ($I_d$) saturation in the output characteristics.[11] The experimental results herein defy both of these projections. In this work, by fabricating several transistors on the same nanotube, the scaling performance of CNTs is unveiled, showing switching behavior that is comparable to the best Si devices. Furthermore, the sub-10 nm CNT transistor provides low voltage operation that is superior to any similarly scaled device to date, a result that shows promise for further optimization of CNT transistors for future applications.

In a 200 mm wafer fab, metal local bottom gates capped with a 3 nm $HfO_2$ gate dielectric (equivalent oxide thickness, EOT ≈ 0.65 nm) were fabricated. Nanotubes were transferred onto the gates[7] followed by a two-step source/drain metallization to form transistors with $L_{ch}$ ranging from sub-10 nm to greater than 300 nm on the same CNT channel (Figure S1, Supporting Information). A schematic of the device structure is shown in

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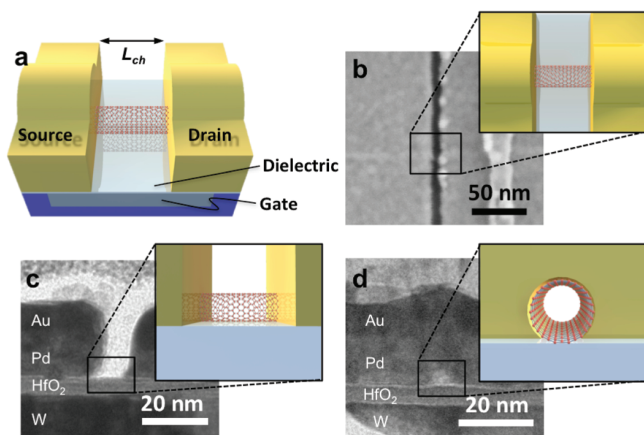


**Figure 1.** Sub-10 nm carbon nanotube transistor configuration with electron microscope images. (a) Schematic illustration showing the local bottom gate device structure, with W gate, 3 nm $HfO_2$ dielectric, and Pd source/drain contacts. The channel length ($L_{ch}$) is indicated. (b) Top-view SEM image of ~9 nm channel length CNT transistor. This top-view was crucial because the line edge roughness of the contacts was such that the channel length was dependent on where the nanotube actually interfaced with the source and drain. (c) Cross-sectional TEM image showing the profile of the source/drain contacts to ensure accuracy of channel length definition. (d) Cross-sectional TEM image in the Pd contact area showing the metal covering a CNT, which is resting directly on the gate dielectric.

Figure 1a, where the channel length is defined as the distance between source and drain contacts. The corresponding scanning electron microscope (SEM) and transmission electron microscope (TEM) images in Figure 1b–d show how the device structure was characterized after electrical measurements. Especially significant is the cross-sectional TEM image in Figure 1c that provides information on the sidewall shape of the source/drain contacts to ensure that channel length definition is accurate when measured from a top-view SEM image (i.e., TEM image ensured that the metal does not slant inward, exaggerating the smallness of the channel length in top-view). The TEM image of Figure 1d displays how the CNT rests directly on the underlying gate dielectric and is covered in an omega-fashion by the contact metal.

To observe the scaling behavior of nanotube transistors to sub-10 nm, several devices with different channel lengths were fabricated on the same CNT. Using the same nanotube for all channel lengths is critical because the energy band gap ($E_g$) for a CNT is inversely proportional to the diameter ($d_{CNT}$). Changes in band gap will affect performance at small channel lengths by affecting achievable on-current ($I_{on}$) and ambipolar conduction behavior. Subthreshold curves of four transistors on a $d_{CNT} \approx 1.3$ nm nanotube with $L_{ch}$ from 320 nm down to 9 nm are given in Figure 2a. All of the curves are measured at the same drain-source bias ($V_{ds}$) of 0.4 V, yet there is an increase in the minimum current as $L_{ch}$ decreases, primarily a result of the back-injection of carriers into the conduction band from the drain. Importantly, the on-current level for the three devices that have $L_{ch} \leq 41$ nm is consistent (if the curves are shifted on top of each other) and is evidence of reaching ballistic channel transport (negligible channel resistance) as shown in previous work.[7] A final observation from the Figure 2a devices is that while there is some mild shifting between the curves, it is not correlated to $L_{ch}$ scaling and is attributed to the presence of charge traps in the vicinity of the nanotube channel causing hysteresis and threshold voltage variation[13,14] (Figure S3, Supporting Information). These nonideal aspects of the present devices, including hysteresis and trapped charge, must be addressed in future studies to enable a CNT transistor technology.

Characteristics of the 9 nm channel length device reflect superb switching behavior in the off-state (Figure 2b) and clear current saturation at a low drain-source bias of approximately −250 mV in the on-state (Figure 2c). Previous theoretical work suggests that current saturation is not possible in CNT transistors with sub-10 nm channel lengths[11] – the present results defy this projection. Regarding the off-state of the 9 nm device, the SS of 94 mV/decade is nearly half of the SS ≈ 170 mV/decade predicted by previous theory.[11] Importantly, this device is on a relatively large diameter CNT ($d_{CNT} \approx 1.3$ nm ±0.2 nm, $E_g \approx 0.62$ eV ± 0.1 eV); thus, a considerable reduction in *SS* and off-current at minimal cost to $I_{on}$ is attainable by using smaller diameter nanotubes.[7,12] As the diameter reduces, the band gap will increase and create larger barriers to ambipolar transport. One other aspect of the CNT transistors in Figure 2 is regarding the contact resistance. By constructing a plot of the total resistance versus channel length from the four devices, the contact resistance is extracted to be $R_c$ = 6.6 kΩ per contact (Figure S2, Supporting Information), in close agreement with previous reports for similar contacts.[7]

To illustrate the potential advantages of using CNTs to replace Si for sub-10 nm transistor technologies, the scaling behavior is compared to three of the most advanced Si-based

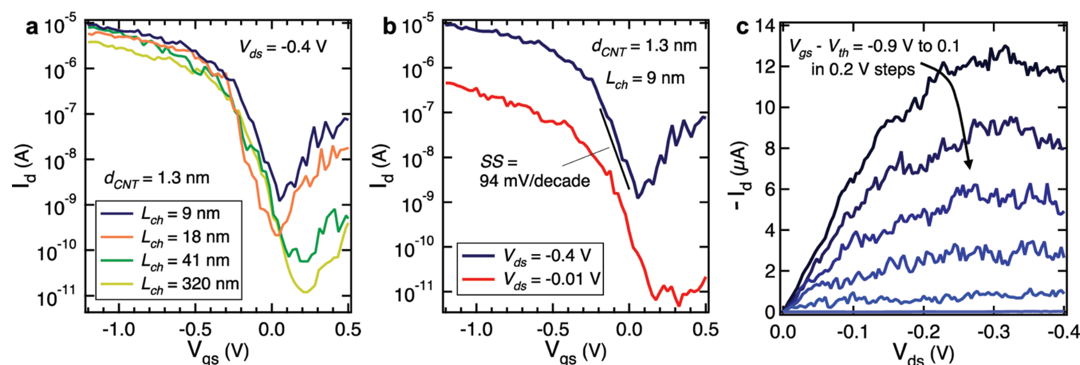


**Figure 2.** Results from scaled CNT transistors on the same nanotube, including electrical characteristics of 9 nm device. (a) Subthreshold curves from four devices assembled on the same CNT, showing increase in minimum current as $L_{ch}$ is reduced and only mild degradation of SS. (b) Subthreshold (off-state) and (c) output (on-state) characteristics of a 9 nm CNTFET.


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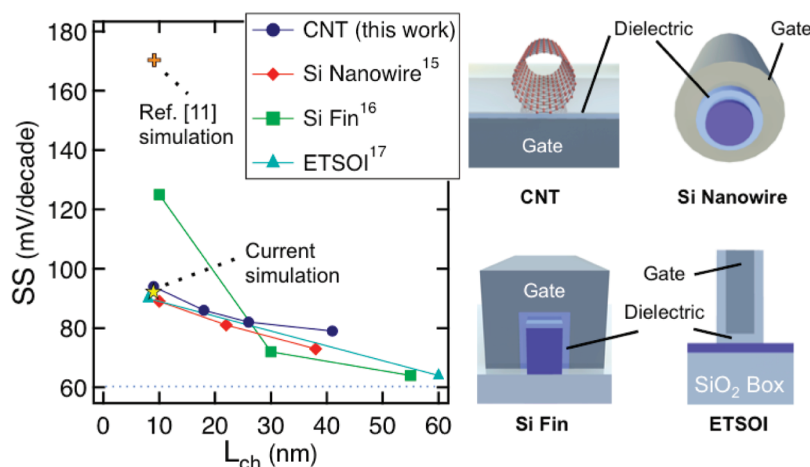


**Figure 3.** Sub-10 nm performance and scaling trend of CNT transistors compared to best reported Si-based devices. Plot of the inverse subthreshold slope versus channel/gate length for CNT transistors compared to competing Si-based, n-type devices. Orange plus sign data point is from theoretical projection in ref 11; yellow star data point is from current numerical simulation; blue dotted line is thermal limit for SS. Cross-sectional schematics show the different gating configurations.

**Table 1. Comparison of Performance Metrics between This Work and the Best-Reported Sub-10 nm Si-Based Transistors**

| ref | channel | $L_{ch}$ (nm) | EOT (Å) | $\|V_{ds}\|$ (V) | $\|V_{gs}\|$ (V) | $I_{on}$ ($\mu$A/$\mu$m)[a] | $I_{on}$ ($\mu$A/$\mu$m) at $V_{dd}$ = 0.5 V[c] diameter[a] | pitch[b] |
|---|---|---|---|---|---|---|---|---|
| this work | CNT | 9 | 6.5 | 0.4 | 0.5 | 1760 | 2410 | 630 |
| 15 | Si nanowire | 10 | 25 | 0.5 | 0.6 | 469 | 469 | 300 |
| 16 | Si Fin | 10 | 17 | 0.5 | | | 28 | 138 |
| 17 | ETSOI | 8 | 15 | 0.5 | 0.6 | 55 | 41 | 41 |

[a] $I_{on}$ is normalized by diameter for CNT and Si nanowires and by two times fin height for Si fin. [b] $I_{on}$ is normalized by physical pitch (spacing from one tube/wire/fin to the next), estimated to be 5 nm for CNTs and 20 nm for nanowires and fins. [c] Performance at $V_{dd}$ technology of 0.5 V, assuming ability to achieve threshold voltage ($V_{th}$) of 0.2 V for all devices with $|V_{gs} - V_{th}|$ = 0.3 V used for $I_{on}$ extraction.

devices: Si nanowires with gate-all-around configuration,[15] Si fins,[16] and extremely thin Si on insulator (ETSOI).[17] Note that the nanowire and fin devices use undoped Si, while the ETSOI incorporates halo doping. Each of the references reports the highest performing sub-10 nm gate length device of its type. For the Si nanowire device the nanowire diameter is 16 nm and in the Si fin device the fin width is approximately 12 nm with a double-gate structure (gated on both vertical sides of the fin, but not on top). The thickness of the Si in the ETSOI device is approximately 8 nm. As seen in Figure 3, the scaling trend of the inverse subthreshold slope for the CNT transistors is similar to those reported for ETSOI and Si nanowires. With the exception of the Si fin, SS for the sub-10 nm devices all fall within a reasonable range of each other.

Other important device metrics from the 9 nm CNT transistor (Figure 2b,c) are compared to the Figure 3 Si-based devices in Table 1. Future transistor technologies will require operation at voltages at or below 0.5 V to limit power consumption. To compare the CNT transistor with the Si-based devices at a supply voltage ($V_{dd} = V_{ds} = V_{gs}$) of 0.5 V, a threshold voltage ($V_{th}$) of 0.2 V was assumed for all devices (also assuming a reasonable SS < 80 mV/dec for the devices) and then the on-current was extracted from the reported data at a gate overdrive $|V_{gs} - V_{th}|$ of 0.3 V. As shown in the rightmost columns of Table 1, the 9 nm nanotube device carries a diameter-normalized 2410 $\mu$A/$\mu$m while the best Si-based device reaches only 469 $\mu$A/$\mu$m (also diameter-normalized). The ETSOI device, while thin at 8 nm, is still difficult to control at sub-10 nm gate lengths, yielding only 41 $\mu$A/$\mu$m.

While normalizing the on-current by diameter is the most common method, it is not a practical projection. To be considered for a technology, CNTs must be densely packed at a certain pitch[18−20] (as will nanowires and fins), so it is more realistic to consider the on-current normalized by a projected tube/wire/fin pitch. For nanowires and fins there must be room for the wire width and gate stack in the pitch, which is aggressively projected to be 20 nm (this would require nanowires and fins smaller than shown in the cited reports), yielding 300 and 138 $\mu$A/$\mu$m for nanowires and fins at $V_{dd}$ = 0.5 V, respectively. With a diameter of ~1 nm and no top gate stack, a pitch of 5 nm is projected for CNTs (200 CNTs/$\mu$m), which yields 630 $\mu$A/$\mu$m at $V_{dd}$ = 0.5 V, still more than double the on-current in the best Si device.

The orange plus sign data point in Figure 3 is the SS for a 9 nm CNT transistor as projected by previous theory.[11] Note the considerably better SS exhibited by the current experimental device. While dissimilar $d_{CNT}$ will affect scaling behavior, the difference would not be so abrupt. The difference in gating geometry will, however, affect the scaling behavior, these experimental devices employ a single bottom gate and the theory uses a gate-all-around structure. Therefore, we performed additional numerical device simulations using a quantum transport model based on the nonequilibrium Green's function formalism similar to previous work but with more consideration for the current device geometry (see the Supporting Information for details of the model). It should be noted that in future work, experimental implementation of a gate-all-around geometry could further improve the scaling behavior.[21]

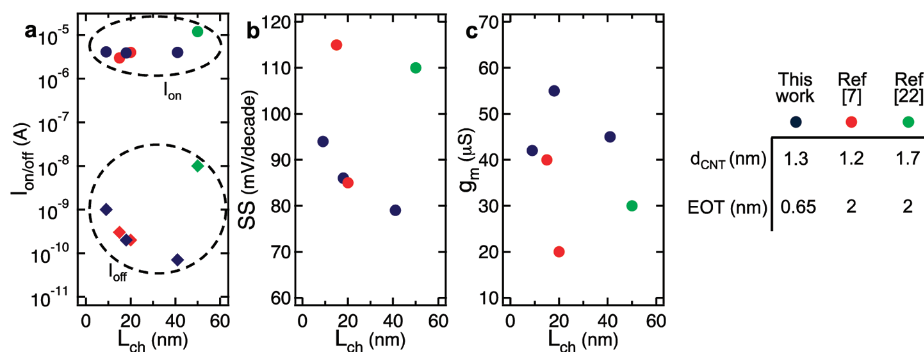


**Figure 4.** Comparison of CNT transistor performance with best-reported nanotube devices from refs 22 and 7. (a) On-current and off-current comparison. $I_{on}$ is extracted from $V_{ds} = V_{gs} - V_{th} = -0.4$ V, while $I_{off}$ is taken as the minimum current at $V_{ds} = -0.4$ V. (b) Subthreshold slope and (c) peak transconductance comparisons. The legend on the right indicates the reported nanotube diameters and equivalent oxide thicknesses.

The primary difficulty in modeling a sub-10 nm CNT device is that at such small $L_{ch}$ the channel becomes less significant than the contacts. In other words, transport in the device is primarily limited by the contacts at these dimensions. Simulation of carrier transport in metal-CNT contacts is far less understood and developed compared to transport in the nanotube channel. A numerical simulation of a 9 nm CNT channel with ideal metallic Schottky contacts yields a subthreshold slope of 270 mV/dec, almost triple the experimentally observed SS. With an experimental channel length accuracy of ±1 nm, it is clear that these ultrashort $L_{ch}$ devices cannot be understood using models that primarily focus on the channel electrostatics.

What is needed is greater understanding of metal-CNT carrier transport to more accurately account for the impact of the contacts on CNT transistor scaling behavior. To demonstrate how significant the contacts are in these devices, we modeled a single, bottom-gate structure and included gate modulation of charge concentration in the source and drain contacts, an effect that occurs in some fashion because the source and drain overlap the gate in these devices. This numerical simulation yielded the yellow star data point SS in Figure 3 and provides a good fit to the 9 nm device subthreshold behavior (Figure S6, Supporting Information). A simple way to understand this improved fit is that the modulation of the source/drain contacts effectively lengthens the channel of the transistor. However, it is critical to note that the numerical simulation herein still lacks an accurate modeling of the physics of the device; rather, this simulation is presented to exemplify the substantial role of transport at the metal-CNT contacts in determining the performance of sub-10 nm CNT transistors. Further work on modeling the transport physics at the contacts must be pursued for a complete understanding of the many aspects that impact performance.

The 9 nm channel length CNT transistor is the smallest reported to date, but there have been previous high-performance nanotube devices with scaled channels.[7,22] In Figure 4, the transistors in this work are compared to the best performing, previously reported devices. Javey et al.[22] used a large diameter nanotube ($d_{CNT}$ = 1.7 nm), yielding a smaller $I_{on}/I_{off}$ ratio with a higher on-current owing to the narrow band gap. However, despite the longer channel length the top-gate structure used by Javey et al. did not provide the type of SS switching performance achieved in the present local bottom gate devices. Peak transconductance ($g_m$) is highest for the present devices, while the previous local bottom gate transistor at $L_{ch}$ = 15 nm is comparable (note that the 20 nm device from ref 7 also has scaled contact lengths causing increased contact resistance).

In conclusion, CNT transistors with channel lengths down to 9 nm show substantially better scaling behavior than theoretically expected. The CNT channel delivers more than double the pitch-normalized on-current at low operating voltage ($V_{dd}$ = 0.5 V) than the best competing Si-based devices produce at similar device dimensions. Numerical simulations highlight the need for more complete theoretical modeling of the transport behavior at metal-CNT contacts in order to accurately project device performance. The CNT transistor's unprecedented performance at sub-10 nm channel lengths should ignite exciting new research into improving the purity and placement of nanotubes, as well as optimizing the transistor structure and integration. Results from aggressively scaling these molecular-channel transistors exhibit their strong suitability for a low-voltage, high-performance logic technology.

## ■ ASSOCIATED CONTENT

### Ⓢ Supporting Information

Detailed information on the transistor fabrication process, extraction of contact resistance, information on gate hysteresis and leakage current, output characteristics for different scaled channel lengths, and details on the numerical simulation with gate modulation of contacts. This material is available free of charge via the Internet at http://pubs.acs.org.

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