Super-junction power device evolution: characteristics analysis and performance comparison between MDmesh M2 and MDmesh M6 technologies

Introduction

The adoption of several optimization starting from the revolutionary principle introduced with super-junction (SJ) devices, has led to different SJ technologies of which the MDmesh M6 is the latest ST's generation. The resulting technology provides high performance both in hard and soft switching topologies (e.g. PFC, LLC) while not sacrificing the ease of use.

The new MDmesh M6 series is a step forward in this direction allowing to achieve extremely low switching losses, especially in light load condition, thus enabling switching applications to reach more easily the target certification level and to be designed more compact and lighter.

In the following are analyzed some aspect of the MDmesh M6 series that make this device suitable for both soft and hard switching applications. This is due not only to very low total gate charge, already an advantage of the previous M2 series, but also due to turn-off switching losses reduction, especially in the low current range, that is of essence to boost the efficiency in light load conditions where certification rules are more and more stringent.

An optimization of both the shape and the absolute value of the output capacitance completes the features that make the MDmesh M6 series well suited to address the target applications.

1 Super-junction (SJ) principle

The basic idea [1] [2] of the almost well-known super-junction principle is quite simple: in the on-state, Figure 1, the electrons flow through a very low resistive n-area while in the blocking state, Figure 2, no electron flow is allowed due to space-charge expansion between the p-doped columns. The practical implementation of this very attractive idea however requires a very sophisticated manufacturing capability due to the mandatory requirement of a perfect compensation of the additional n-charge between adjacent P-columns.

Figure 1. Cross section of a vertical super-junction MOSFET in on-state

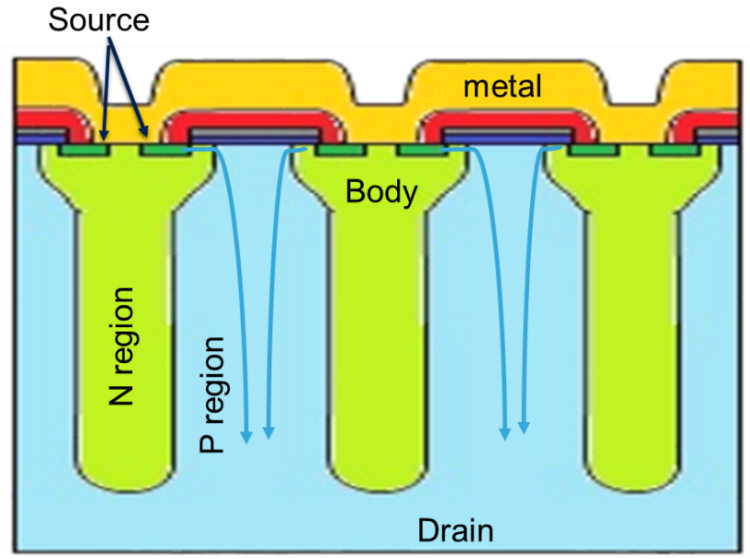
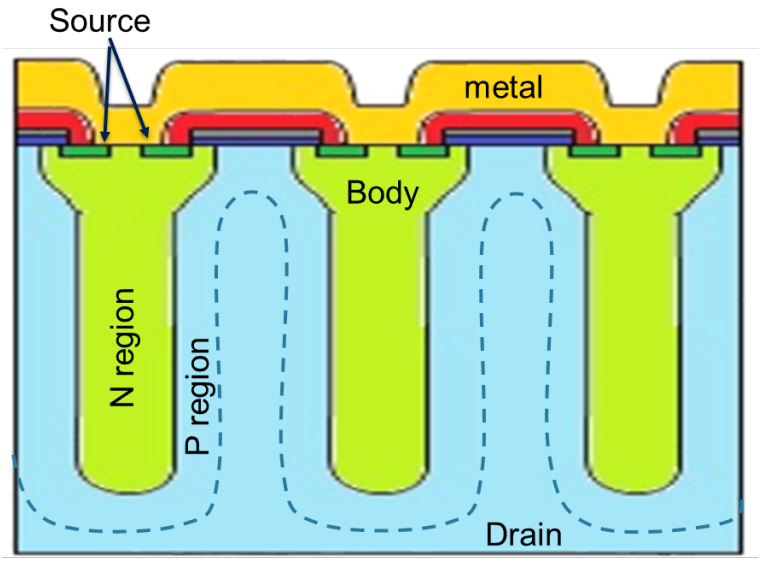


Figure 2. Cross section of a vertical super-junction MOSFET in off-state



The SJ principle overcomes intrinsic silicon limitations to allow smaller chip sizes than conventional Power MOSFETs with the same $R_{DS(on)}$. As a consequence, all the phenomena associated with surface area decrease directly with chip size. Some parameters, however, are also strongly linked to the underlying technology. An example, not present in standard Power MOSFETs, is in the sudden decrease of output capacitance from low to high drain voltage. This is related to the structure of the output capacitance, which changes from a thin very large

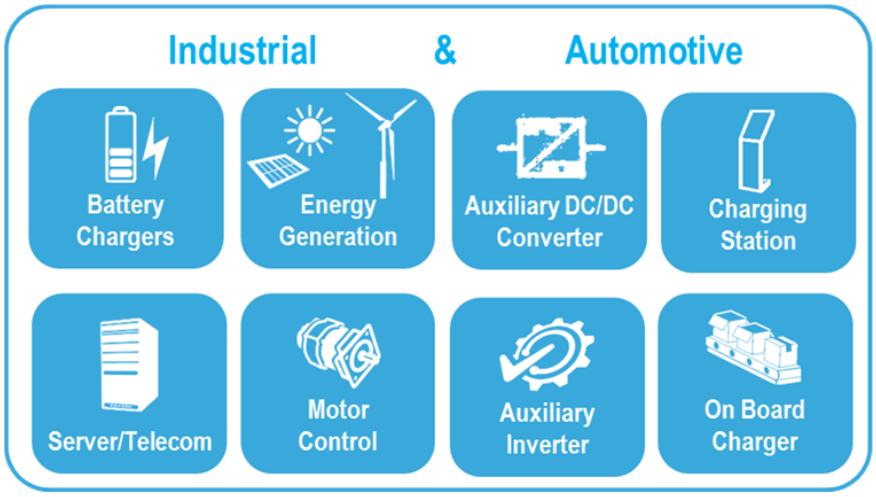
surface capacitor, due to the space surface layer at low voltage drain, to capacitance which is smaller by orders of magnitude due to the full depletion of the space charge layer, leading to surface capacitor decrease and width increase. The lower the voltage under which this transitions occurs, the faster and lower losses the device is subject to. Similar behavior occurs with reverse capacitance, albeit with some differences.

2 Overview and positioning of M6 devices

2.1 Target applications

The MDmesh M6 is the last ST super-junction technology and it has been developed to address mainly the high power SMPS for server and telecom applications and the HEV market including OBC (off-board chargers) and charging stations. The following pictogram, Figure 3, summarize the target applications.

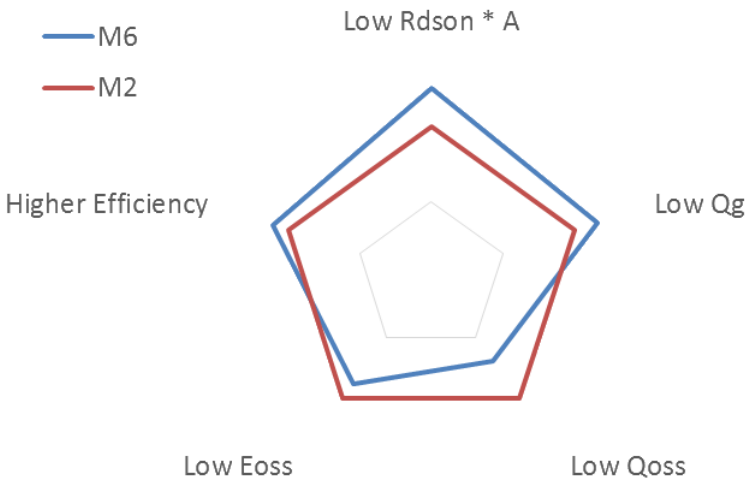
Figure 3. Target applications in industrial and automotive fields



2.2 Predecessors comparison

In the radar chart of the following figure a comparison with the previous super-junction technology is reported. The obtained improvements in both static and dynamic characteristics lead to higher efficiency in target applications. In particular, comparing devices having the same on-resistance, the M6 ones have reduced gate charge and reduced energy losses at turn-off of the MOSFET.

Figure 4. Positioning of the MDmesh M6 against MDmesh M2 predecessor



More detailed results will be reported in the following with focused attention in LLC HB and ZVS PSFB applications.

3 Technology main characteristics

A short recap of the characteristic required to a power switch for working well in power converters is given in the following together with a comparison of the main improvements that the new M6 technology sets out against the M2 one.

3.1 Device electrical characteristic comparison

The following table reports a summary of the typical main static and dynamic electrical characteristics of both a M2 and a M6 device. In the next sections a deeper analysis of some key parameters will show and explain the technological improvement realized by the M6 devices.

Table 1. M6 and M2 device comparison

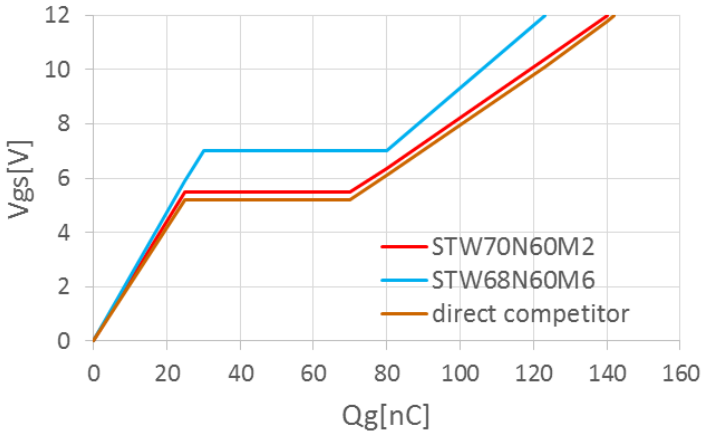
Symbol	Parameter	Test Condition	STW70N60M2	STW68N60M6	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS}= 0V, I_D= 1mA	600	600	V
I_D	Drain current		68	63	A
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS}= 10V, I_D= 20A	40	41	mΩ
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D =250µA	3	4	V
R_G	Intrinsic gate resistance		3.3	1.6	Ω
Q_G	Total gate-charge	V_{DD}= 480V, I_D= 68A, V_{GD}=10V	118	106	nC
Q_{GS}	Gate-source charge		25	35	nC
Q_{GD}	Gate-drain charge		47	45	nC
C_{iss}	Input capacitance	V_{DS}= 100V, V_{GS}= 0V, f= 1MHz	5200	4360	pF
C_{oss}	Output capacitance		250	235	pF
C_{rss}	Reverse capacitance		5	13	pF

3.1.1 Gate charge improvement

The gate charge curve is the main tool for comparing at a glance the on-field behavior that different devices will have in terms of gate driving energy requirements and switching losses. According to Device electrical characteristic comparison and the figure below the difference between the Q_{gs}, Q_{gd} and Q_g values reported in the data sheet are evident, even if, looking only at the numeric values of the different part of the gate charge, give no enough information for understanding the valuable E_{off} reduction in the low current range, that is of essence to boost the efficiency in light load conditions where certification rules are more and more stringent. The driving losses are also reduced leading both to higher switching frequencies.

The improvement of switching losses of the M6 devices respect to the M2 ones as we will see in the next sections, is also related to the different shape of the capacitance profile.

Figure 5. **M6, M2 and direct competitor gate charge comparison**



3.1.2 Output capacitance profile improvement

The SJ principle, overcoming the intrinsic silicon limit, allows a smaller chip size compared to a conventional Power MOSFET having the same $R_{DS(on)}$. As a consequence all the surface area related characteristics decrease directly with the chip size. Some parameters, however, are also strongly linked to technology characteristics. An evidence of this aspect, not present in standard Power MOSFET, is in the sudden decrease of output capacitance from low to high drain voltage. This is related to the structure of the output capacitance which change from a thin very large surface capacitor, due to the space surface layer at low voltage drain, to orders of magnitude smaller capacitance, due to the fully depletion of the space charge layer, leading to surface capacitor decrease and width increase.

The next figure compares the C_{oss} of M6 and M2 series. The obtained results are due to both an optimization of the overall column aspect, even if the ratio height to width has been maintained quite constant, and to the modification of the horizontal structure.

A sharper capacitance transition from low to high V_{DS} voltage has been obtained. The emphasis of non-linearity of the capacitance characteristic, typical of the SJ structure, helps in achieving lower switching losses. The entity of the achieved improvement will be analyzed in the next sections and some real example of obtainable efficiency improvements will be reported.

3.1.3 Charge (Q_{oss}) and energy (E_{oss}) stored in output capacitance

The performance improvements introduced by the charge balancing structures include both $R_{DS(on)}$ and all the junction capacitances valuable reduction even if makes the latter much more nonlinear. The effective stored charge and energy in the super-junction MOSFET are significantly reduced but calculating these parameters for comparing different MOSFETs, to choose the one that best match our application needs, has become not so straightforward. The traditional approach to understanding MOSFET parameters such as C_{oss} and C_{rss} is no longer valid due to the high non linearity they exhibit.

Figure 6. **M6 and M2 C_{oss} comparison**

Until now, super-junction transistors have been used most effectively in hard-switching topologies, where the device is forced to switch even under high current and voltage conditions. The necessity of increasing frequency to achieve higher power density and efficiency has led to resonant converters and to the use of ZVS techniques. The LLC resonant converters, in particular, are widely adopted due to the advantages such as high efficiency, high power density, and low electromagnetic interference in power supply applications among the various power converter designs. In addition to the basic criteria required for power MOSFET selection the keeping of zero voltage switching (ZVS) operation of the power MOSFET is required.

The minimum inductor current required for ZVS, necessary to charge/discharge the effective capacitance appearing in parallel with drain-sources of the power switches in half-bridge LLC, is related to the capacitance itself. The lower the output capacitance value, the lower the charge to be removed the lower the need for magnetizing current and less dead time. For further details, refer to [3] [4] [5].

Figure 7 and Figure 8 show that ZVS operation is easier to be achieved with M2 devices. Nevertheless this drawback of M6 against M2 is not a big issue: the additional losses due to capacitance charge and discharge are generally negligible compared to the overall switching losses, see Section 3.1.4 Switching losses comparison. In addition, designing the application to achieve the device turn-on when V_{DS} is around 20 V results in the reduction the recirculating current needed to discharge the output capacitance and being Eoss losses quite similar it is possible to benefit of the lower E_{off} losses of M6.

Figure 7. Q_{oss}: charge stored in the output capacitance

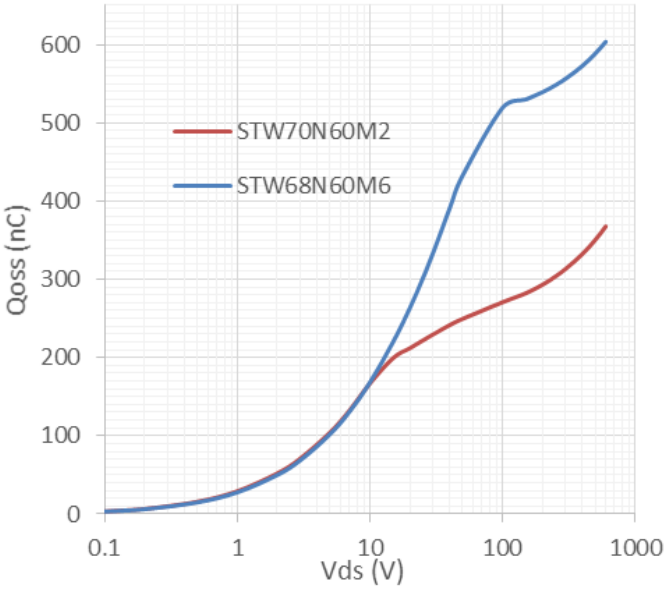
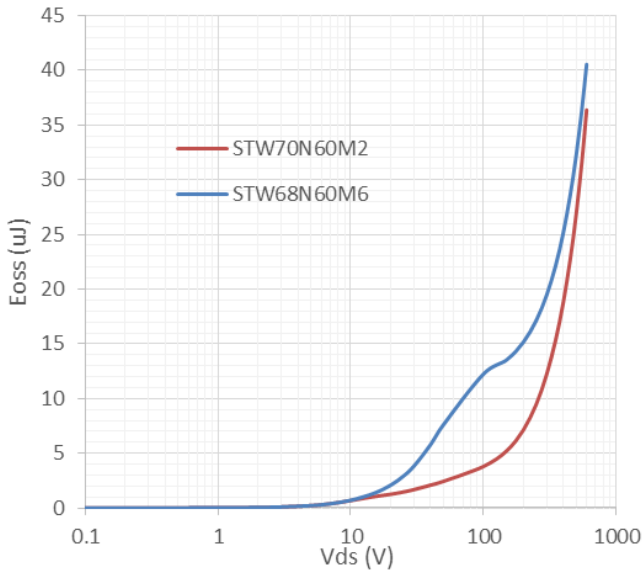


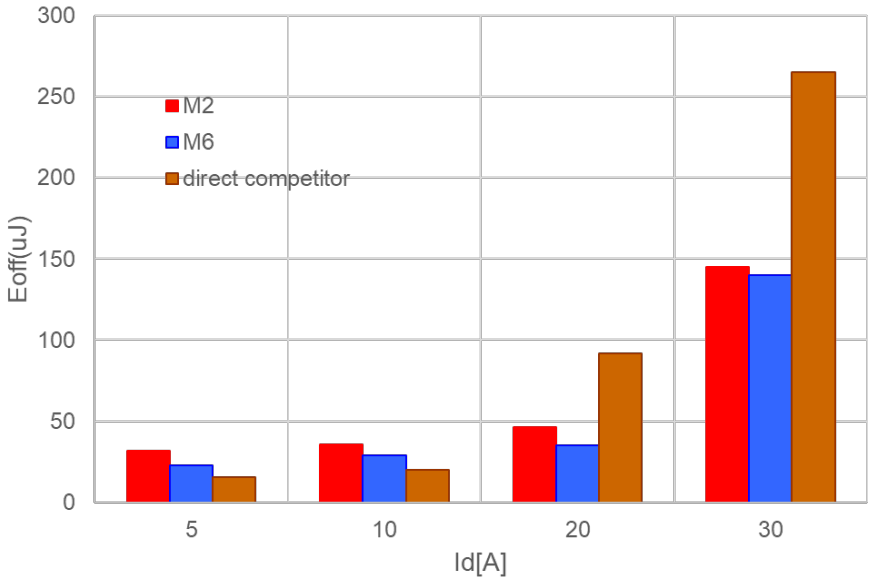
Figure 8. E_{oss}: energy stored in the output capacitance



3.1.4 Switching losses comparison

In the next figure the comparison of switching losses is reported for hard switching at turn off. The M6 technology exhibits lower losses respect to the previous technology due to both the gate charge and output capacitance profile optimization. So, being almost equivalent from both turn-on and on losses the better choice from efficiency point of view are the M6 devices. But, being M6 an even more sophisticated technology respect to the M2 one, cost implication could arise. So the best tradeoff have to be investigated, mainly in terms of efficiency and cost, being the two technologies equivalent from other aspects as ruggedness, reliability and so on. In section 4 some real example of obtainable efficiency improvements will be reported.

Figure 9. Hard switch E_{off} comparison



4 Measurement results

In this section the results of M2 and M6 devices benchmarking is reported. The performances of the two technologies have been compared in state of the art evaluation board, in particular in the LLC section of a 500 W fully digital AC-DC power supply (STEVAL-ISA147V2) and in both the PFC and LLC section of a 150 W high power adapter (STEVAL-ISA170V1).

4.1 STEVAL-ISA147V2 a 500 W fully digital AC-DC power supply

In this section the devices STW40N60M2 [6] and STW36N60M6 [7] are compared. As test vehicle has been used the LLC section of an STEVAL-ISA147V2 a 500 W fully digital AC-DC power supply (D-SMPS) based on STM32F334C8 Microcontroller [8].

The test conditions are:

- V_{mains} = 90 -264 Vac
- V_{OUT} = 12 V
- P_{OUT} = 0W to 500 W
- f_{SW} = 70 kHz up to 130 kHz

The efficiency measurement reported in Figure 10 and Figure 11 shows a higher efficiency of M6 devices on the whole load range in comparison with the M2 ones. The advantage of M6 structure is more evident in light load condition being more evident the influence of the output capacitance which lead to the different shape of the voltage drain, Figure 12, and thus to lower turn-off losses for the M6 devices.

Figure 10. Efficiency comparison between M2 and M6 solution (500 W)

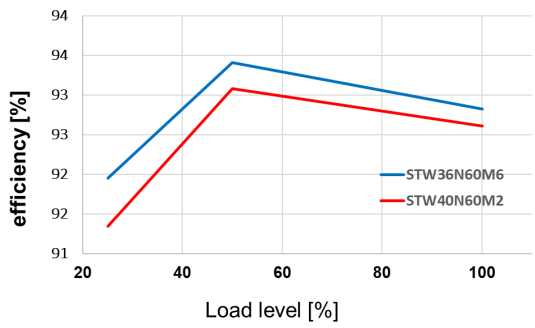


Figure 11. Δefficiency referred to M2 solution (500 W)

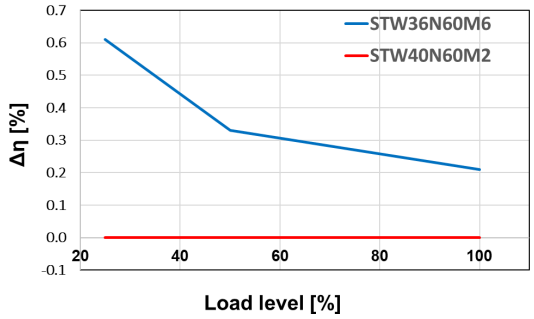
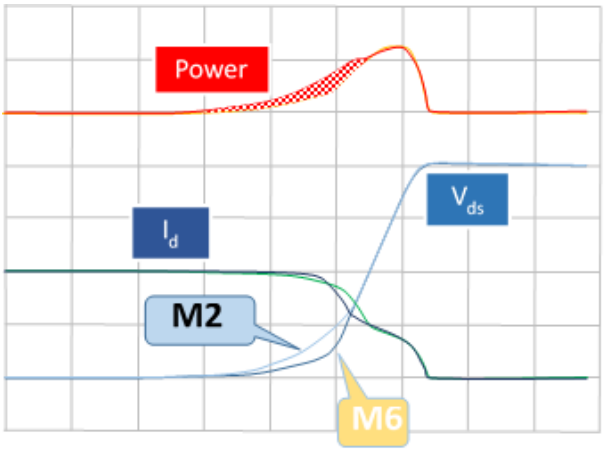


Figure 12. **Influence of output capacitance on turn-off losses**



4.2 STEVAL-ISA170V1 a 150W high power adapter

As test vehicle has been used an STEVAL-ISA170V1 a 150 W high power adapter [9]. The results of efficiency measurement are reported in Figure 13 and Figure 14. They refer to the whole system efficiency, i.e. they comprise the efficiency of both the PFC part and the LLC one. Of course the devices used in the two section are different, in particular it has been compared the [10] and [11] for the PFC section and the [12] and [13] for the LLC one.

The test conditions are:

- V_{mains} = 90 -264 Vac
- V_{OUT} = 12 V
- P_{OUT} = 0 W to 150 W

Figure 13. **Efficiency comparison between M2 and M6 solution (150 W)**

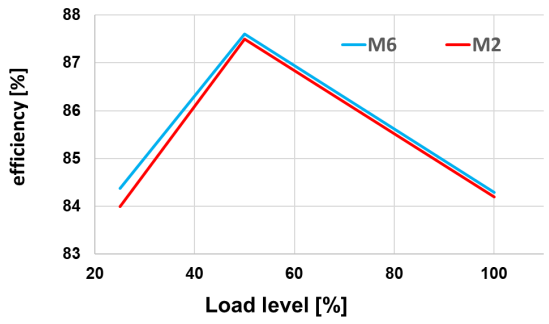
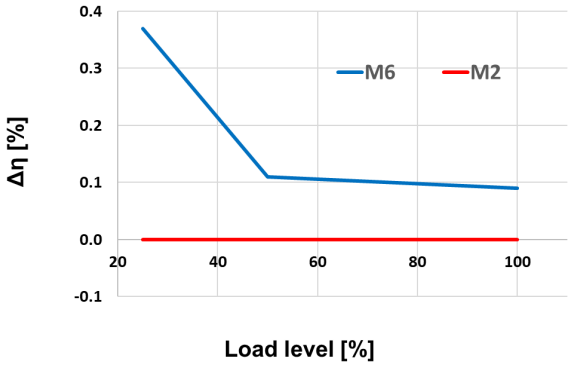


Figure 14. **Δefficiency referred to M2 solution (150 W)**



The same consideration, expressed in the previous section, that giustify the increasing difference in the efficiency curve at light load are valid here too.

5 Conclusion

This application note presents the new STMicroelectronics super-junction technology called M6 compared to both the previous M2 and to competitor ones. This technology is an evolution of the previous M2 one obtained by some optimization regarding the overall column aspect, thus leading to gate charge and output capacitance improvement and leading to efficiency increase both in hard and soft switching applications.

Tests were performed on several application board comparing devices performance. The results have shown that the output capacitance profile influences the switching operation and determines the total efficiency of the system. The optimization of this aspect in MDmesh M6 devices offers higher efficiency, especially when the system operates in light load condition.

6 References

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[6] "STW40N60M2 data sheet," [Online].

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[13] "STF16N60M6 data sheet," [Online].

Revision history

Table 2. **Document revision history**

Date	Version	Changes
03-Apr-2019	1	First release.

List of figures

Contents