Switching Reliability Characterization of Vertical GaN PiN Diodes

O. Slobodyan[1], S. Sandoval[1], J. Flicker[1], R. Kaplar[1], C. Matthews[1], M. van Heukelom[1], and S. Atcitty[1]
[1]*Sandia National Laboratories, Albuquerque, NM, USA*
rjkapla@sandia.gov

Abstract **Vertical GaN (v-GaN) power semiconductor devices offer potential advantages compared to today's state-of-the-art Si, SiC, and lateral GaN power devices, including an enhanced unipolar figure-of-merit, and high-voltage and –current operation have been demonstrated for v-GaN PiN diodes. However, few reliability studies have been performed on such devices, particularly in a realistic switching environment. In this paper, we report on the development of a system for v-GaN power device reliability characterization under switching conditions. The system is based a double-pulse test circuit (DPTC). The paper describes how the DPTC was modified to apply a continuous stream of stress pulses, as opposed to the traditional long-short double-pulse sequence typically used for device characterization. Initial test results on a v-GaN PiN diode show good robustness under switching stress.**

Keywords– **Gallium Nitride, v-GaN, reliability, power switching, wide bandgap, power diode, double-pulse testing**

I. Introduction

Power conversion systems are necessary to process electrical energy (e.g., conversions between AC/DC, frequency, and voltage) in a wide variety of applications. Power semiconductor devices are the heart of the electrical conversion system and tend to be limited by voltage or current ratings. Historically, silicon (Si) has been the main electronic material used to fabricate these devices, and remains so today. However, Si power devices are approaching the limits imposed by the material, and a drive for ever-improving system-level performance has prompted the development of power semiconductor devices based on alternative materials, notably wide-bandgap (WBG) semiconductors. The most mature of these for high-voltage (> 1200 V) applications is silicon carbide (SiC) [1], while power switching devices based on gallium nitride (GaN) have primarily been high electron mobility transistors (HEMTs) targeted at lower voltages (< 600 V) [2]. However, recently vertical GaN (v-GaN) devices have emerged as a possible alternative to SiC for high-voltage power electronics [3], and research into a number of device types is ongoing [4-7].

Interest in v-GaN devices is motivated by the material properties of GaN, which are perhaps most simply (if incompletely) summarized by the unipolar figure of merit (UFOM), shown in Fig. 1. It is seen that for a given breakdown voltage, a GaN drift region has a lower on-resistance than SiC. This is due to the high critical electric field of GaN, which is believed to exceed 4 MV/cm [8]. However, v-GaN power device research has historically been hindered by a lack of high-quality native GaN substrates. Indeed, this lack of native substrates is one factor that has motivated the development of GaN power HEMTs grown on Si substrates. Unfortunately, the high defect densities associated with GaN-on-Si heteroepitaxial growth, as well as non-idealities such as surface breakdown in lateral devices, have limited the achievable voltage rating. While the low-voltage market is quite large and such devices excel in applications requiring very high switching frequencies (> 1 MHz), homoepitaxial vertical drift regions are required if GaN is to realize the potential indicated by the UFOM and compete with SiC in the > 1200 V range. Fortunately, the availability of native GaN substrates has increased substantially in recent years, leading to a large amount of research on v-GaN devices. PiN diodes are perhaps the most mature of these devices, with high breakdown voltages (> 3.7 kV) and high currents (> 400 A) demonstrated [4]. Moreover, the breakdown of such devices is consistent with an avalanche mechanism [4], which is important for avalanche ruggedness. With such performance demonstrated, it is now feasible to consider using v-GaN PiN diodes in high-voltage applications, which may challenge the position of SiC.

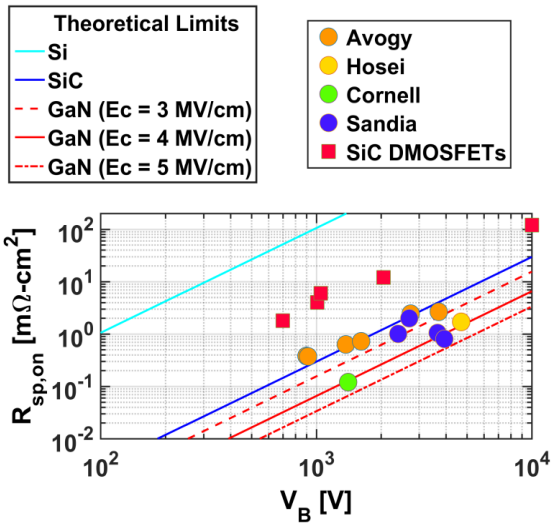

Fig. 1. Theoretical UFOM for Si, SiC, and GaN (lines) as well as reported values for SiC and GaN devices (symbols).

However, there have been few studies on the reliability of v-GaN PiN diodes [9]. Demonstrating high reliability is critical if circuit designers are to adopt such devices. Indeed, the ability to demonstrate high reliability has been one of the major factors that has determined the rate at which WBG power devices of all types have been adopted thus far. As such, this paper reports on reliability studies of v-GaN PiN diodes. Prior to conducting the reliability studies, extensive electrical characterization measurements were performed to verify the diodes' performance, e.g. temperature-dependent current-voltage (I-V) studies of both the forward and reverse bias regimes. Because these diodes are designed to operate in a switching environment in a power conversion circuit, the majority of our reliability characterization has focused on switching stress. For this, we have built on our previous work on characterization of reverse-recovery transients in v-GaN devices [10], and have adapted the double-pulse experimental setup used in that work to apply continuous pulsed stress under inductively-loaded conditions.

The devices investigated in this paper were fabricated by Avogy Inc., and characterization measurements and reliability testing were performed at Sandia National Laboratories.

II. Devices, Experimental Setup, and Results

A. *Vertical GaN Device Characterization*

A schematic of a basic PiN v-GaN diode is drawn in **Error! Reference source not found.**. In addition to the drift region and *p*-type anode, these devices incorporate edge termination structures to control the magnitude of the electric field at the device periphery to prevent early breakdown below that dictated by the intrinsic critical electric field. The diodes used in this study are true vertical structures grown on high-quality GaN substrates. They are rated for 5 A continuous forward current in a 0.72 mm^2 active device area, to yield a conduction current density of nearly 700 A/cm^2. As seen in Fig. 2, the devices consist of an n^+ GaN substrate, with the n^- drift region and p^+ anode homoepitaxially grown on top of it. Varying the thickness and doping of the drift region controls the breakdown voltage of the diode, in conjunction with the design of the edge termination.

Characterization of unpackaged die was done on a manual high-temperature (300°C), high-voltage (10 kV), and high-current (20 A_{DC}) probe station. Humidity was not controlled or monitored during measurement. I-V sweeps were separately performed on the same die in forward and reverse bias, because the high current and voltage capabilities are supported by different instruments and probe setups. Reverse bias measurements were done with the die immersed in Fluorinert FC-70 to prevent arcing.

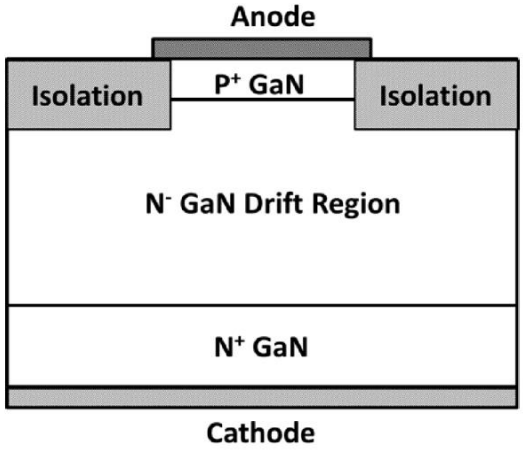

Fig. 2. Schematic drawing of v-GaN PiN diode.

Forward bias sweeps from 25°C to 150°C in 25°C steps are shown in **Error! Reference source not found.**. The turn-on voltage decreases going from 25°C to 150°C, consistent with previous measurements by Avogy [4]. Reverse-bias sweeps taken from 25°C to 125°C in 25°C steps are shown in Fig. 2. The leakage current increases with increasing temperature, consistent with [4]. The breakdown voltage also increases, but not in a linear manner. From 25°C to 125°C, the breakdown voltages are: 1657, 1652, 1675, 1706, and 1711 V.

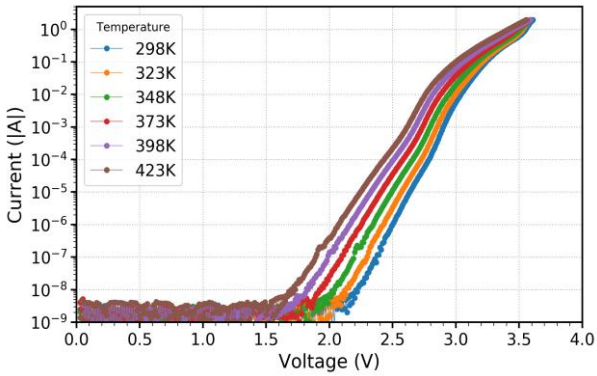

Fig. 3. Forward bias temperature-dependent I-V curves of v-GaN PiN diodes.

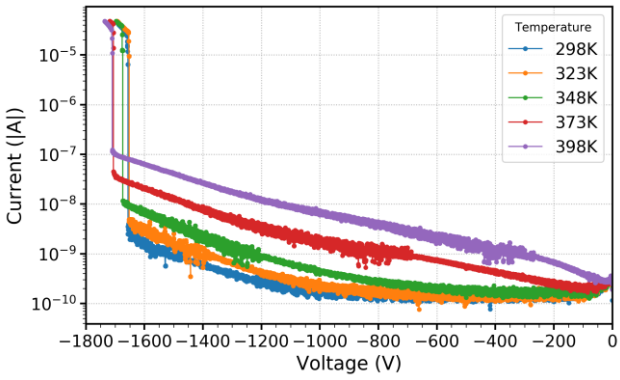

Fig. 2. Reverse bias temperature-dependent I-V curves of v-GaN PiN diodes, demonstrating temperature dependence of breakdown consistent with an avalanche mechanism.

Fig. 3 shows the breakdown voltage plotted as a function of temperature. The breakdown voltage shows a clear positive temperature coefficient of breakdown, which is characteristic of an avalanche process. While the dependence of breakdown voltage on temperature is approximately linear, a hysteresis effect is apparent for the first measurement at room temperature. This may be due to a burn-in effect, e.g., due to changes in the contacts.

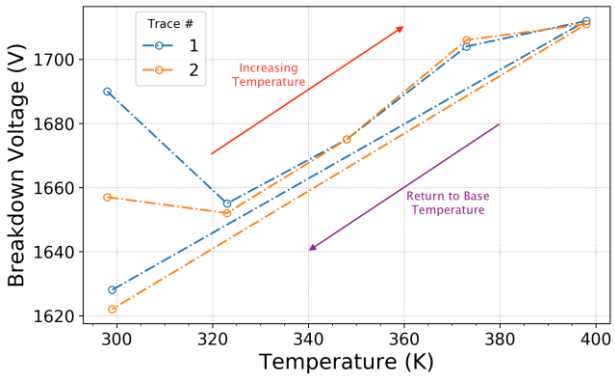

Fig. 3. Measured breakdown voltage as a function of temperature.

B. *Switching Relability Test Set-Up*

DC step-stress experiments are often performed to study degradation and reliability of power devices, and can provide good insight into mechanisms of degradation. However, on their own, and even combined with switching characterization between stressing sequences, these tests are not fully illustrative of typical operating conditions for power devices, where the device is continuously toggling between off- and on-states. Therefore, to better assess realistic degradation of power devices, a different test must be developed, and for this purpose we have focused on the development of pulse stressing using a modified double-pulse test circuit (DPTC).

The circuit diagram of the DPTC is shown in Fig. 4. This circuit is typically used to characterize switching behavior of power transistors under inductively-loaded conditions [11]. However, the DPTC can be adapted to test diodes, and has previously been used by our group to obtain switching characteristics of Avogy v-GaN diodes as well as baseline SiC and Si diodes [10]. The circuit is based on a board available from GeneSiC Semiconductor [12].

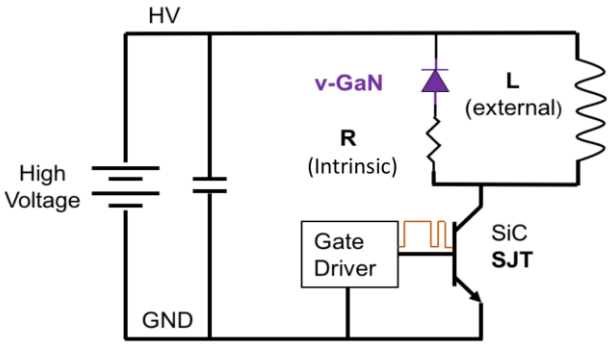

Fig. 4. DPTC used for switching stress of v-GaN diodes.

A photo of the test circuit is shown in Fig. 5. The typical mode of operation for a DPTC is a long-short double-pulse waveform that can be used to determine switching transition speed. However, the DPTC can be thought of as a conventional buck circuit with the output and input tied together [11]. This makes it possible to operate the DPTC in both a steady-state switching mode as well as the traditional double-pulse characterization mode, and the same circuit can be utilized to stress a device via long-term steady-state operation, as well as to periodically characterize the device's switching characteristics via the traditional double-pulse mode.

Fig. 5. Photograph of DPTC used for switching stress of the v-GaN diodes.

For an ideal DPTC operating in continuous operation mode, the current increases without bound because the inductor/diode circulation loop is ideally lossless. However, in a real circuit, the presence of resistance in the circulation loop (Fig. 4) degrades the circulating current while the switch is off. To operate in steady-state mode, the off-time of the switch must be large enough such that the circulating current in the inductor/diode loop decays to its starting value before the previous switching event (i.e., the current increase during the switch-on cycle must equal the current loss during the switch-off cycle). If the circulating current does not decay by a sufficient amount, then the net current flow through the circuit will increase with each switching cycle in a runaway event. Fig. 6 shows such an event. The switch current (pink trace) increases with each switching event, because the off-

time is not long enough for the circulating current to decay to its value at the start of the previous switch-on cycle.

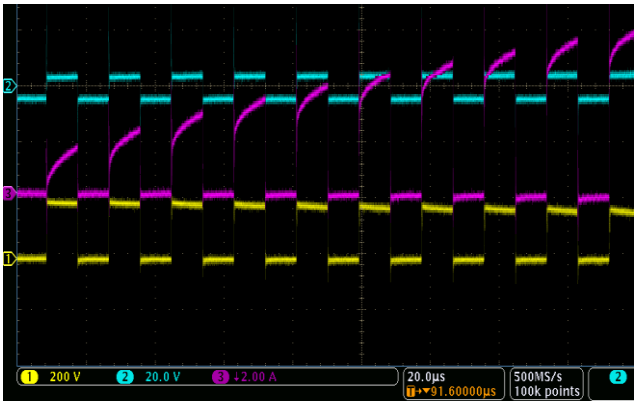

Fig. 6. Waveforms for DPTC in steady-state mode. The switch current (pink trace) shows a net increase with each switching cycle, since the off time is not long enough for the current to decay sufficiently. Yellow trace is diode voltage and blue trace is switch gate voltage.

The value of the inductor and the resistance in the inductor/diode loop therefore determine the switching duty cycle and frequency required to achieve steady-state mode. During the switch on-time, the current flow through the inductor increases linearly. The on-time required to achieve a given change in inductor current (ΔI_L) is determined by the input voltage (V_{in}) and inductance (L) via:

$$t_{on} = \frac{\Delta I_L \cdot L}{V_{in}} \tag{1}$$

When the switch turns off, the current through the diode/inductor pathway decays according to:

$$I_L(t) = I_{Lmax} \cdot e^{-\frac{R}{L}t} \tag{2}$$

Here, I_{Lmax} is the inductor current at the beginning of the switch off-time (this should be no more than the smallest of the current ratings of the inductor, diode, and switch). The off-time required for the current to decay by an amount ΔI_L is therefore equal to:

$$t_{off} = -\frac{L}{R}\ln\left(1 - \frac{\Delta I_L}{I_{Lmax}}\right) \tag{3}$$

Combining Eqs. (1) and (3) yields a relationship between t_{on} and t_{off}, subject to the values of L, R, V_{in}, and I_{Lmax}:

$$t_{off} = -\frac{L}{R}\ln\left(1 - \frac{t_{on} \cdot V_{in}}{L \cdot I_{Lmax}}\right) \tag{4}$$

The DPTC used in this work utilized three 1 mH inductors wired in series. No external resistance was intentionally added to the inductor/diode loop, so the total resistance was the sum of the intrinsic resistances from wiring, traces, and the socket used to mount the diode, as well as the intrinsic diode resistance. To apply rated current to the diode at an input voltage of 1000 V, the value of t_{on} was 2 µs. To prevent a condition of current runaway as dictated by Eq. (4), the switch off-time (978 µs) was kept significantly above the switch on-time (2 µs). Using Eqs. (1)-(4), this implies a parasitic resistance in the system of at least 1 Ω. The long off-time limited the steady-state stress-mode switching frequency to f = 1 kHz.

C. *Switching Reliability Testing Results*

Die situated in a standard TO220 package were tested using the DPTC shown in Fig. 4. A persistent issue during continuous operation of the circuit was overheating. Due to the lack of sufficient heatsinking on the DPTC setup, the device stress was de-rated from 5 A_{pk} to 2.2 A_{pk} to limit packaging-related failure mechanisms that are unrelated to intrinsic device operation (installation of heatsinking sufficient to enable stress/characterization at rated current/voltage is currently being implemented). This de-rating was accomplished by lowering the input voltage in the DPTC circuit. The lower peak current value was achieved using a steady-state operation with V_{in} = 500 V, t_{on} = 3.5 µs, and f = 1 kHz.

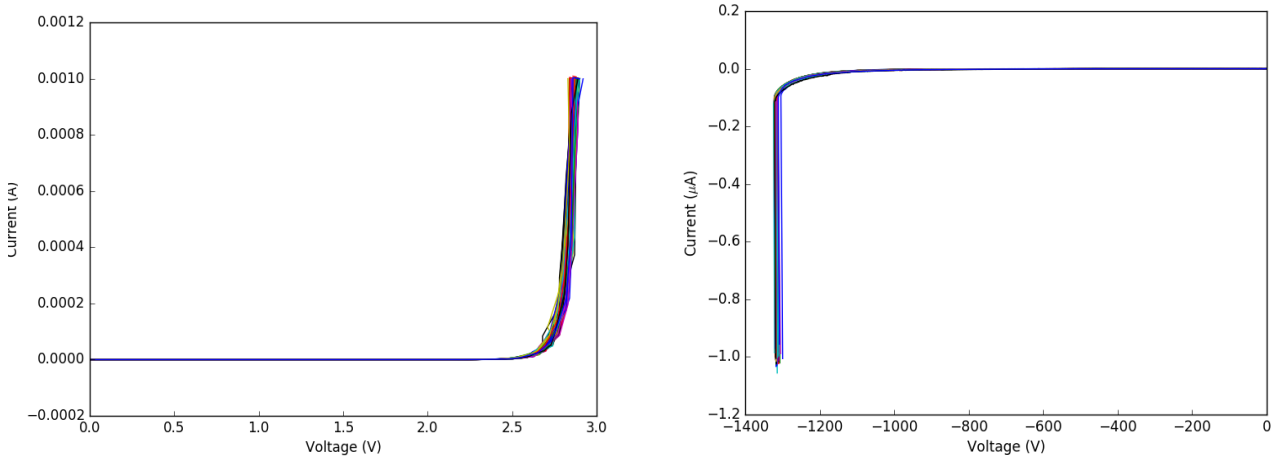

Fig. 7. Forward (left) and reverse (right) I-V curves taken at regular intervals during the first 800 minutes of steady-state switching stress.

To stress and characterize the devices under switching conditions, the DPTC was operated in steady-state mode and the diodes were subsequently characterized *in-situ* via a double-pulse waveform. The double-pulse waveform consisted of two pulses of 15 μs and 4 μs, respectively, separated by a 4 μs off-time. Following the double-pulse characterization, the devices were removed and characterized using forward and reverse I-V curves. The devices were then returned to the DPTC for the next round of steady-state-mode stressing. This process was repeated multiple times. The forward and reverse I-V curves (71 total) for the first 800 minutes of stress on one v-GaN diode are shown in Fig. 9.

These I-V curves show very little variation in the electrical characteristics of the diodes during the extent of the testing. Data analysis was carried out on the I-V curves as a function of total stress time (Fig. 10). In the blocking regime, the breakdown voltage (defined as a current of 1 μA, see Fig. 9) shows little degradation over the stress time measured. After an initial burn-in period where the breakdown voltage increases from an initial value of 1270 V to 1317 V, it stays fairly constant over the remaining duration of the test. There is some increase in the leakage current at a reverse bias of 1,000 V and, although the relative size of the change is significant (~50%), the absolute magnitude of the change in leakage is extremely small (< 3 nA). In the forward direction, the turn-on voltage (defined at a current of 1 mA, again see Fig. 9) shows negligible change as a function of stress time (differences in measured voltage shown in Fig. 10 are due to discretization of the voltage signal). Similarly, the forward current measured at a forward voltage of 2.16 V (picked for convenience due to data sampling) has no dependence on the stress time. Both the initial and final double-pulse characterizations are shown in Fig. 11. The measured switch current is the pink trace, the diode voltage is the yellow trace, and the switch voltage is the blue trace. The double-pulse waveform after 800 minutes of switching stress appears to be indistinguishable from the initial double-pulse waveform, indicating negligible degradation of the v-GaN diode.

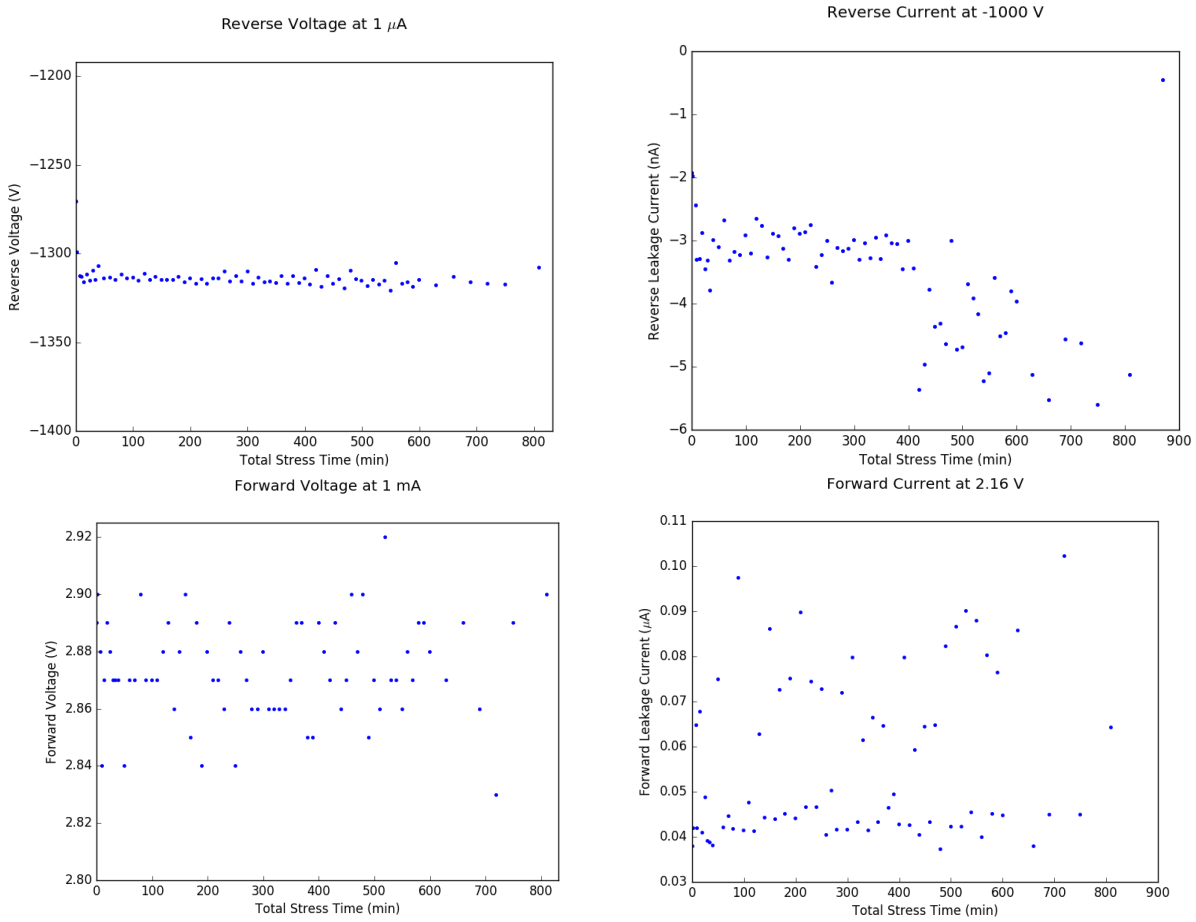

Fig. 10. Extracted data from forward and reverse I-V curves during stress. The reverse breakdown voltage (upper-left) and reverse leakage at 1,000 V (upper-right) throughout the stress time show little deviation from the initial values. The forward voltage (lower-left) at 1 mA and the leakage current at 2.16 V similarly show little signs of degradation.

III. Conclusion

In this work, we verified the electrical performance of v-GaN PiN diodes by characterizing the reverse and forward I-V characteristics of bare die as a function of temperature. The reverse breakdown voltage of the diodes increases as temperature increases, consistent with an avalanche-induced breakdown process.

The primary goal of the work was to demonstrate the utility of a DPTC operating in continuous mode for reliability

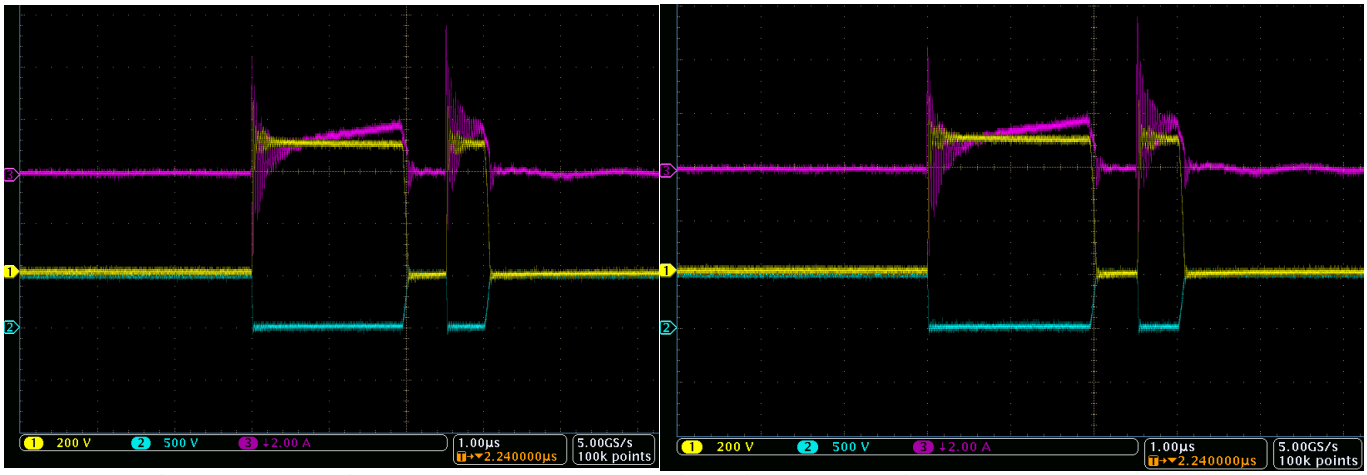

Fig. 11. Initial (left) double-pulse waveforms compared to double-pulse waveforms after 800 minutes of switching stress (right). Pink trace is switch current, yellow trace is diode voltage, and blue trace is switch voltage.

characterization. This allows for *in-situ* stressing and characterization of a packaged device in a realistic loaded switching circuit. A v-GaN die was stressed and repeatedly characterized over the length of the stress time via both DC I-V curves as well as non-continuous, traditional double-pulse characterization. Throughout the extent of the tests, the v-GaN diode showed no significant change in reverse and forward I-V curves, nor in the double-pulse switching characterization waveforms.

ACKNOWLEDGMENTS

The authors thank I. Kizilyalli and O. Aktas, both formerly of Avogy Inc., for providing the diodes studied in this work. The characterization work at Sandia was supported by the Energy Storage Program managed by Dr. Imre Gyuk of the DOE Office of Electricity, and the fabrication work at Avogy was supported by the SWITCHES program managed by Dr. Tim Heidel of ARPA-E. Sandia National Laboratories is a multi-mission laboratory managed and operated by National Technology and Engineering Solutions of Sandia LLC, a wholly owned subsidiary of Honeywell International Inc., for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA0003525.

REFERENCES

[1] D. K. Schroder, "Progress In SiC Materials/Devices and Their Competition," *Int. J. of High Speed Electron. and Syst.*, vol. 21, no. 1, p. 1250009, 2012.

[2] M. J. Scott *et al.*, "Merits of Gallium Nitride Based Power Conversion," *Semiconductor Science and Tech.*, vol. 28, no. 7, p. 074013, 2013.

[3] E. A. Jones, F. F. Wang, and D. Costinett, "Review of Commercial GaN Power Devices and GaN-based Converter Design Challenges," *IEEE J. of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 707-719, 2016.

[4] I. C. Kizilyalli, A. P. Edwards, O. Aktas, T. Prunty, and D. Bour, "Vertical Power p-n Diodes Based on Bulk GaN," *IEEE Trans. on Electron Devices*, vol. 62, no. 2, pp. 414-422, 2015.

[5] A. D. Koehler *et al.*, "Vertical GaN Junction Barrier Schottky Diodes," *ECS J. of Solid State Science and Technol.*, vol. 6, no. 1, pp. Q10-Q12, 2017.

[6] D. Ji *et al.*, "Normally OFF Trench CAVET With Active Mg-Doped GaN as Current Blocking Layer," *IEEE Trans. on Electron Devices*, vol. 64, no. 3, pp. 805-808, 2017.

[7] C. Gupta *et al.*, "In Situ Oxide, GaN Interlayer-Based Vertical Trench MOSFET (OG-FET) on Bulk GaN Substrates," *IEEE Electron. Device Lett.*, vol. 38, no. 3, pp. 353-355, 2017.

[8] A. M. Armstrong *et al.*, "High Voltage and High Current Density Vertical GaN Power Diodes," *Electron. Lett.*, vol. 52, no. 13, pp. 1170-1171, 2016.

[9] I. C. Kizilyalli, P. Bui-Quang, D. Disney, H. Bhatia, and O. Aktas, "Reliability Studies of Vertical GaN Devices Based on Bulk GaN Substrates," *Microelectronics Reliability*, vol. 55, no. 9–10, pp. 1654-1661, 2015.

[10] C. Matthews *et al.*, "Switching Characterization of Vertical GaN PiN Diodes," *IEEE Wide Bandgap Power Device and Appl. (WiPDA)*, pp. 135-138, 2016.

[11] S. R. Bahl, D. Ruiz, and D. S. Lee, "Product-Level Reliability of GaN Devices," *IEEE Int. Reliability Physics Symp. (IRPS)*, p. 4A-3, 2016.

[12] "Double Pulse Switching Board (GA100SBJT12-FR4) Datasheet," GeneSiC Semiconductor, Dulls, VA.