FinFET

EXTENDING MOORE'S LAW

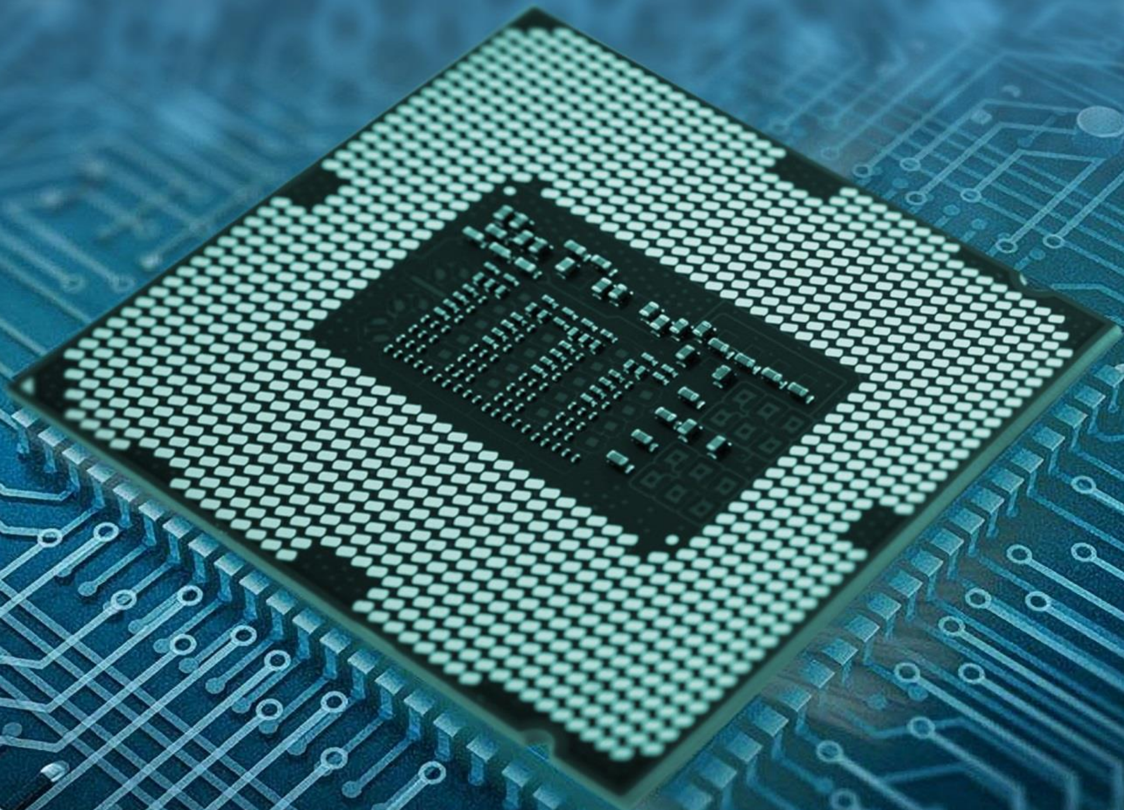

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TABLE OF CONTENTS

EXECUTIVE SUMMARY 2

INTRODUCTION 2

TAXONOMY 2

TOP ASSIGNEES 2

GEOGRAPHICAL COVERAGE 2

LexScore™ 2

LICENSING HEAT MAP 2

APPENDIX 2

EXECUTIVE SUMMARY

Moore's Law started as an observation in 1965 by Dr. Gordon Moore that number of transistors per square inch will double every two years. Over past 50 years this observation has stood the test of time and has been demonstrated as hallmark of human ingenuity and enterprise. To continue the progression of Moore's law the transistor gate geometry (process technology node) needs to shrink every 18-24 months. This requires innovative process technology and massive R&D spending on semiconductor foundries. There have been several speculations in the past for demise of Moore's law due to the limits of physical transistors dimensions and manufacturing complexity. In 2011, at the 22nm process technology node, Intel surprised the semiconductor industry by introducing a three dimensional transistor structure, which Intel calls Tri-Gate, but is more commonly referred to in the industry as FinFETs. FinFET transistor technology is going to extend the Moore's Law beyond sub 28-32nm process technology node. The FinFETs are going to significantly improve the performance of application processors setting off a revolutionary change in the smartphone, tablet or convertible computing market. The strength of FinFET is best demonstrated by use of Samsung Exynos 7 Octa processor (manufactured in 14nm FinFET) in Samsung S6 in advanced markets instead of Qualcomm's Snapdragon 810 (manufactured in 20nm planar). FinFET (14nm) also allowed Intel to ship fanless Broadwell personal computers to consumers.

As the Moore's law extends, the computing products continue to shrink dimensions and improve battery life. The infrastructural cost of developing next-generation products and chip manufacturing processes is increasing with each generation. A study indicated that integrated device manufacturers (IDMs) and foundries are experiencing 35% cost increases from one process technology node to the next while fabless semiconductor companies are seeing even greater cost increases, of roughly 60%, for designs and tapeouts on next generation process technologies. The average cost for setting up a fab has increased from $2b for 90nm node to $10b for 14nm. The huge capital requirement has become the major barrier of entry to this industry. Hence we have very few players who own major fabs in this industry.

In this report, we study the technological landscape of this fast growing technology from the perspective of Intellectual Property (Patents). We find that the majority of patenting activity has occurred in technologies related to semiconductor manufacturing processes such as, 'Etching', 'Device Formation', and 'Lithography' with impact on design parameters such as, 'Structural Features', 'Model Parameters', 'Operating Voltage' and 'Power Consumption'. We also find that majority of the patents/patent applications are distributed among top three companies. IBM is at the top and holds around 15% of the total patents. IBM is followed by TSMC and Intel with a significant number of patents in their portfolio. The share of these top 3 assignees is around 35% of the total patents/patent applications (considered for analysis) in this technology domain. The US geography has seen the maximum patent filings and is followed by the big markets of China, Japan, Korea, and Taiwan.

Using our proprietary patent analytics tool, LexScore™, we identify IBM, TSMC and Intel as the top IP leaders in this technology domain with good patent portfolio quality and high patent filing activity. Since IBM has already moved away from semiconductor fabrication market with its announcement to sell its semiconductor business to GlobalFoundries, TSMC and Intel are now the top leaders in this technology domain. Toshiba also holds a large number of patents in this domain. Given the patent holding pattern and a high patent filing activity, we expect to see significant out-licensing activity in this technology domain. The combination of high start-up cost of setting up FinFET foundries and common manufacturing vendor supply chain will drive high cross-licensing activity to share cost and manufacturing resources. In April 2014 GlobalFoundries announced a strategic partnership with Samsung Electronics to license and manufacture 14nm process technology through a true Fab-Sync methodology. This collaboration allowed GlobalFoundries offer the same lead technology at a faster time to market and leverage the technology maturity, ECO partnerships, IP collaboration, EDA readiness while providing an assurance of supply. Furthermore, using our proprietary Licensing Heat-map framework, we predict significant patent licensing activity in the 'Etching with impact on structural features' technology segment.

Among the top semiconductor foundry companies (Intel, TSMC, GlobalFoundries, Samsung), Samsung has been aggressive in ramping FinFET technology in high volume manufacturing apart from Intel. Samsung has announced that it has begun mass production of Exynos 7 Octa processor using in Samsung S6 built on its 14-nanometer logic manufacturing technology. Despite of promising FinFET production/manufacturing capabilities, Samsung seems to have the least impressive patent portfolio (among the top fabs), so we can expect patent out-licensing activity by other companies with Samsung.

In the following sections, we present our analysis of the Patent Landscape of this technology domain.

INTRODUCTION

Throughout the momentous history of semiconductors, everything from computer hardware to multifunction mobile devices, Moore's law has remained the same: the number of transistors on a given area of silicon doubles every two years. With the foundries developing advanced process nodes and their consumers' unquenchable demand for more functionality, the industry has satisfied Moore's Law. The transistor count on today's advanced multicore processors is reaching the 3 billion range – a long way from the 6800 processor of the mid 1970s that had just 5000 transistors.

Design parameters like performance, power, area, cost and 'time to market' have not changed since the beginning of the integrated-circuit industry. In fact, Moore's law is all about optimizing those parameters by driving to the smallest possible transistor size with each new technology generation. However, as we approached the sub nanometer range with the 90nm node and beyond, static leakage became an important factor such that while every new process generation may have doubled the gate density, it also doubled the amount of leakage current. As process technologies further continued to shrink towards 20nm, it became impossible to achieve a similar scaling of certain device parameters, particularly the power supply voltage, which is the dominant factor in determining dynamic power. Additionally, optimizing for one variable such as performance evidently lead to unwanted compromises in other areas like power.

The issue of leakage current could be mitigated by the use of high voltage threshold dopants at the expense of device performance, or through the use of advanced design techniques, such as power gating or multivoltage islands. Controlling current leakage when the transistors are switched off is important to preserve battery life or minimize power consumption in computer and mobile applications that spend most of their time in an idle state. Economics also plays a vital role in determining whether to move to and when. If chips can take advantage of the increased density to provide more functionality, then it generally made sense to move to the next node, even if mask and process costs were higher. This was the case when designs moved from 65nm to 45/40nm and then again to 28nm. However, as it moved to the 20nm process node, there has been a new set of challenges, including double patterning and very leaky transistors due to short channel effects. Both are nullifying the benefits of transistor scaling if planar transistor technology is used. The move from 28nm to 20nm was unappealing economically to many, since it didn't provide the same level of performance and area gains as observed with previous generations.

FinFET is the culmination of years of research at University of California, Berkeley, in the late 1990s, in response to a call from the United States Defense Advanced Research Projects Agency. The university opted to release the intellectual property into the public domain instead of patenting it; as the Berkeley researchers kept refining the designs, Chenming Hu, one professor involved in the project, presented the work at several companies, including Intel.

Intel didn't invent FinFET design, but the company was the first to get it into production.

Even with the 30 to 50% density improvement enabled by moving from the 28nm to 20nm process technologies, the performance gain is nowhere near what was achieved with the move from the 45/40nm to the 28nm process node.

While the planar FET may have reached the end of its scalable lifespan, the industry has found a fitting alternative in FinFETs for next generation of advanced processes.

FinFET technology had its origins in the 1990s, when DARPA were keen to fund research possibilities of replacements to the planar transistor. A UC Berkeley team led by Dr. Chenming Hu proposed a transistor with a new structure which would reduce leakage current. They suggested that a thin-body MOSFET structure would control short-channel effects and subdue the leakage by keeping the gate capacitance in closer proximity to the whole of the channel.

With advanced geometry planar FET technologies, such as 20nm, the source and the drain intrude into the channel, making it easier for leakage current to flow between them and making it very difficult to turn the transistor off completely. FinFETs are named so because they are 3d structures that projects out of the substrate and resemble a fin. The 'fins' form the source and drain, effectively providing more volume for the same area than a planar transistor (see Figure 1. comparing planar FET and FinFET). The gate wraps around the fin, providing better control of the channel and allowing very little current to leak through the body when the device is in the 'off' state. This, in turn, enables the use of lower threshold voltages and results in better performance and power.

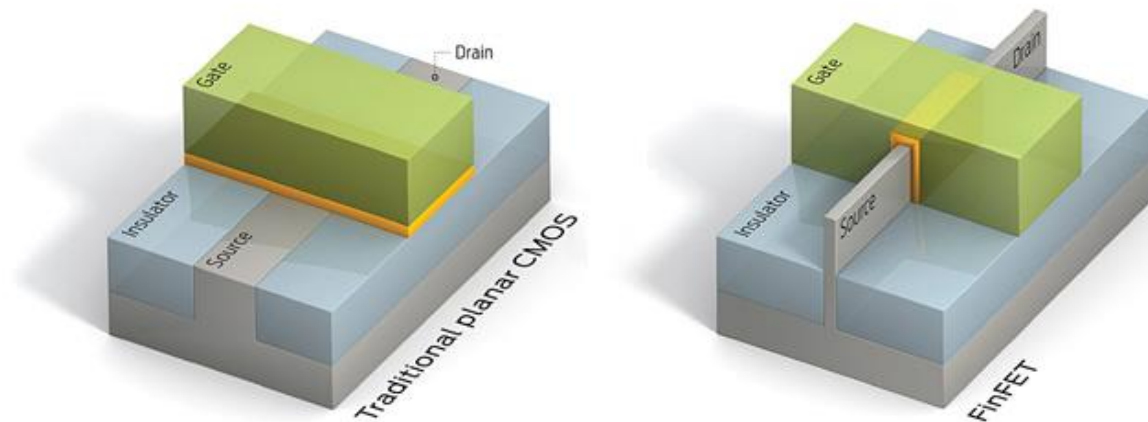

Figure 1: Planar CMOS and FinFET[1]

Many semiconductor design companies are moving quickly to manufacture their devices on the advanced 16nm and 14nm FinFET geometries, just for the

[1] "Transistor Wars" IEEE Spectrum.<http://spectrum.ieee.org/semiconductors/devices/transistor-wars>

better performance and power benefits. Many test chips have tapped out and the results have started to come in now. One of the earliest manufacturers at the 14nm process node, Samsung has been developing FinFET process technology for several years and is now ready for early production. Samsung's 14nm LPE process is providing nearly 150% better performance from a die which is half the size of the previous node. There is also improved power consumption of around 150% as compared to its 28nm process technology.

Samsung stunned the world, showing off the world's first 10nm FinFET DRAM technology in the recently concluded International Solid-State Circuits Conference

Samsung has been developing FinFET process technology for several years and is now ramping production. Samsung's 14nm LPE process is providing almost 150% better performance from a die half the size of the previous node and improving power consumption by around 150% when compared to its 28nm process technology.

From the economic perspective, data from International Business Strategies shows that the move to 20nm and FinFET results in essentially the same cost per die (Q1 2014 estimates), especially as devices increase in size. FinFET devices can operate from a lower supply voltage than planar transistors since they have a lower threshold voltage. This drop in supply voltage can improve dynamic power consumption considerably. Users can atleast expect a 20% improvement from a drop in supply voltage of just 0.1V and this is one of the strong reasons for FinFET adoption. Given that the transistors can operate at a much lower voltage than nominal, additional dynamic power savings on that facet alone would be achievable. In addition, foundation library providers are investigating whether or not it makes sense to introduce smaller height standard cells that could reduce dynamic power consumption further. These providers are likely to release different height libraries, allowing designers to target specific performance or power applications as foundry process design kits are stabilizing for production. This will allow for computing devices like smartphones, laptops and tablets with long battery life.

The 20nm process node was necessary to help build the foundation for the advanced FinFET processes. With the smaller device geometries, traditional lithography/optical manufacturing techniques no longer have the required resolution where double patterning – using litho-etch-litho processing – becomes necessary. The number of manufacturing design rules has increased significantly and these have to be handled by various EDA tools, such as place and route, physical verification, and extraction.

The industry's experience with 20nm has paved the way for an easier transition to FinFET processes. Many of the tool improvements can still be applied, but the handling of FinFETs does require a few more changes; for example, SPICE BSIM-CMG models had to be created to add the 3D effects. It is also true that, with 3D

transistors, capacitance becomes a primary concern. EDA tools must build in high resistance interconnect optimisation in order to mitigate these capacitive effects. Layer awareness is also essential to provide optimal metal layer assignment during routing of the design.

The Exynos 7420 chip inside the Samsung Galaxy S6 is already built on Samsung's 14nm FinFET process

Another interesting trend to note is the cost variation as the size decreases. As the size decrease lower than 28nm, there is a price increase unlike the gradual price decrease with the size reduction upto 28nm.

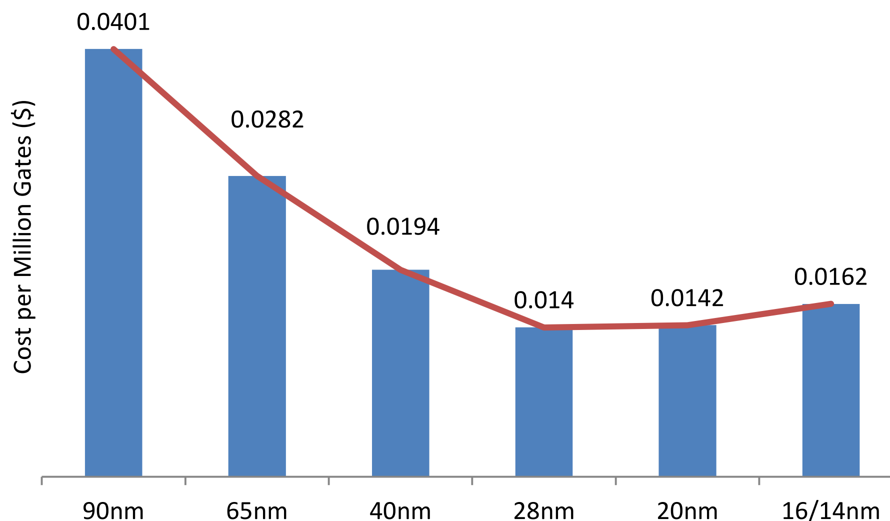

Figure 2: Cost per Million gates v. Feature Size[2]

Although FinFET processes may seem new, development of the technology itself has been in progress for almost a decade. The industry has worked together to make the shift to an advanced new process node as seamless as possible, with minimal impact to current design methodologies. Consumer appetite for new functionality remains high and the move to designing with FinFET process technologies will help fill that need and keep Moore's Law very much alive.

[2] "FinFETs Not the Best Silicon Road" EE Times <http://www.eetimes.com/author.asp?section_id=36&doc_id=1321674>

TAXONOMY

Multi-gate or tri-gate architectures, also known as FinFET technology is a promising technology that lead to creation of even smaller and efficient microprocessors and memory cells. This improves performance and battery life of computing devices. The technology came into existence as a result of relentless increase in the levels of Si process manufacturing and integration. This has resulted in change in many design parameters. Fundamentally the feature sizes have reduced to enable more devices to be fabricated within a given area. However, other figures such as power dissipation and line voltages have also reduced along with increased frequency performance. The taxonomy is presented in the form of a 2D matrix with manufacturing processes on one axis and design parameters on the other axis. The taxonomy focuses on the impact of various manufacturing processes on the design parameters. The categorization of patents/patent applications, related to FinFET technology was done on the basis of manufacturing processes and the affected design parameters. The set considered for the analysis comprised of 12,769 patents/patent applications.

The silicon manufacturing process is divided into FEOL (Front-end-of-line), BEOL (Back-end-of-line), Assembly and Testing. FinFET technology impacts FEOL manufacturing the most as they are created there. Most patents fall in FEOL manufacturing process. Due to this, FEOL is further divided into processes involved in the manufacturing of devices, such as Wafer Development, Oxide Growth, Lithography, Etching, Device Formation and Stacking. The BEOL, assembly and test have comparatively lower impact from planar to FinFET technology, so they have not been sub categorized.

The design parameters are classified as Structural features, Design Flow, Model Parameters, Power Consumption, Feature Size, Operating Voltage, Operating Speed, and Static Leakage Current.

Please refer to Appendix for detailed definitions of the various Level3 categories.

Dr. Chenming Hu, professor at University of California, Berkeley, has been called the Father of 3D Transistor for developing the FinFET in 1999. He is a board director of SanDisk Corp and was the Chief Technology Officer of TSMC from 2001 to 2004

Design Parameters \ Manufacturing Processes	Front-end-of-line (FEOL)						Back-end-of-line (BOEL)	Assembly / Packaging	Testing
	Wafer Development	Oxide Growth	Lithography	Etching	Device Formation	Stacking			
Structural Features	1740	445	1847	2904	2135	1307	1914	243	211
Design Flow	88	23	106	103	99	60	154	38	66
Model Parameters	306	80	248	448	408	258	517	40	99
Power Consumption	156	36	153	222	227	115	474	45	93
Feature Size	156	80	219	291	318	90	204	34	19
Operating Voltage	203	51	189	206	323	183	421	32	103
Operating Speed	214	35	204	255	245	145	279	37	50
Static Leakage Current	63	15	66	79	82	56	83	8	17

Table 1: Taxonomy

In the manufacturing processes category, FEOL and BEOL are of interest. There are 9212 patents/patent applications in FEOL, and 3785 in BEOL. In FEOL category, the following sub-heads are of interest: Etching, Device Formation, and Lithography. There are 4834 patents/patent applications in 'Etching', 3725 in 'Device Formation', and 3267 in 'Lithography'. There are patents/patent applications that cover multiple manufacturing processes and multiple design parameters.

In the design parameters category, the following sub-heads are of interest: Structural Features, Model Parameters, Operating Voltage, and Power Consumption. There are 6650 patents/patent applications in 'Structural features', 1536 in 'Model Parameters', 1272 in 'Operating Voltage, and 1218 in 'Power Consumption'.

Etching is a critically important process in the manufacturing of a FinFET or any other transistor. Every wafer undergoes many etching steps before it is complete. Etching is used to chemically remove layers from the surface of a wafer during fabrication. The part of the wafer is protected from the etchant by a mask which resists etching.

Device Formation refers to the formation of gate, source and drain on the substrate layer. Gate film is formed by oxidation and then, plasma nitridation process is applied to the surface of the gate film. Gate electrode (polysilicon) is formed on it by CVD method. The impurities (specific elements) are diffused into the substrate by ion-implantation to form source and drain. In FinFET technology, the conducting channel is wrapped by a thin silicon "fin", which forms the body of the device. The thickness of the fin (measured in the direction from source to drain) determines the effective channel length of the device. The Wrap-around gate structure provides a better electrical control over the

In the last week of February, Applied Materials, Inc. announced the industry's first in-line 3D CD SEM metrology tool for solving the challenges of measuring the high aspect ratio and complex features of 3D NAND and FinFET devices.

channel, and thus helps in reducing the leakage current and overcoming other short-channel effects.

Structural features refer to the number of gates (double-gate or tri-gate), structure of the fins, and interconnect between the devices. Since FinFET technology has multiple-gate transistors, structural features hold an important position in the analysis.

Model Parameters refer to corner effect, short channel effect, quantum effect, parasitics, etc. These parameters have a great impact on the performance of a transistor and thus, is an important factor in FinFET technology.

Power consumption and operating voltage are closely related. Lesser the operating voltage, lower is the power consumption. FinFET technology has significantly reduced the power consumption by reduction in leakage currents.

TOP ASSIGNEES

Figure below depicts the top assignees having patents/patent applications related to FinFET technology. IBM, Taiwan Semiconductor Manufacturing Company (TSMC) and Intel are the top three assignees with 1885, 1691 and 854 patents/patent applications respectively. The numbers of patents/patent applications owned by top three assignees comprise around 35% of the total patents/patent applications filed in the domain (considered in the analysis). Top 20 assignees in this technology domain hold around 80% of the total patents/patent applications.

Most of the company's filing patents/patent applications are IDMs (integrated devices manufacturers like Intel, IBM, Samsung) and pure-play foundries (like TSMC, GlobalFoundry, UMC), The memory manufacturers (like Micron, Hynix, Samsung) also have significant patents because they are also ramping FinFET technology to produce fast, dense and low power memory used in computing devices. Few semiconductor equipment vendors (Applied Materials/Tokyo Electron, Varian) round up in Top 20.

The top assignee, IBM has already transferred the bulk of their semiconductor business over to GlobalFoundries, which also appears among the top six assignees in this technology. This has resulted in their competitors such as TSMC and Samsung take the lead in rolling out new manufacturing nodes and securing the lucrative contracts that come with being the leader. Samsung is already licensing its 14nm technology to Global Foundry.

IBM had to pay Global Foundries $1.5 Billion to take unprofitable Chip Manufacturing Business off its hands. GlobalFoundries will be IBM's exclusive foundry provider for the next 10 years for the 22nm, 14nm and 10nm process nodes. In exchange, Global Foundries will also get access to IBM patents.

Micron Technologies has shown keen interest in device formation and feature size. A significant portion of their portfolio comprise of patents/patent applications that are filed in etching, device formation, and feature size.

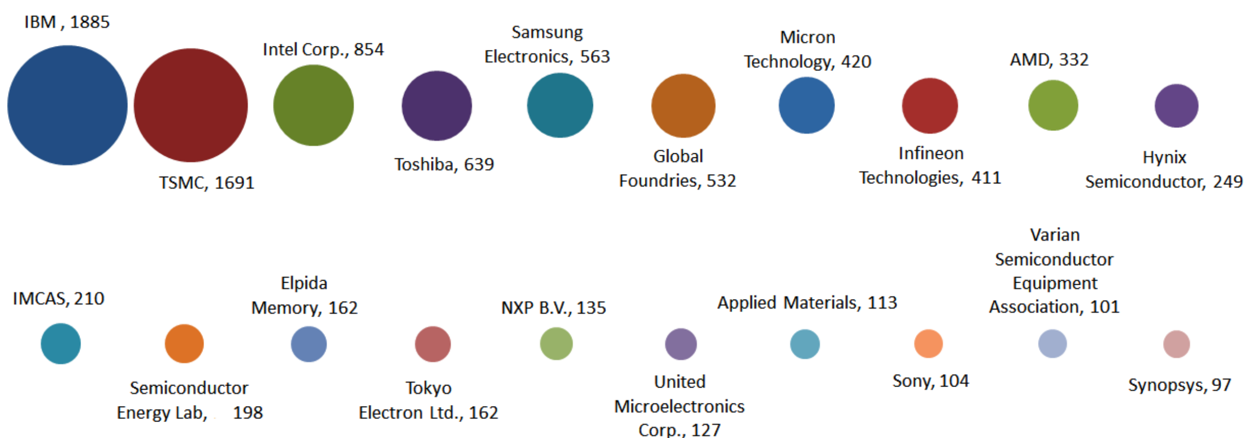

Figure 3: Top Assignees in FinFET technology space

Although IBM and Intel appear at the top, both their approaches are far from similar. While Intel makes it on a standard bulk silicon substrate IBM describe a very different approach to 14nm FinFET transistors. The IBM devices are made not from a standard bulk silicon substrate but from an insulating substrate known as SOI, a more expensive material but one which simplifies manufacturing in terms of device isolation. These devices are over 35% faster than IBM's 22nm planar (i.e. standard, non-FinFET) transistors, with an operating voltage of just 0.8 volts.

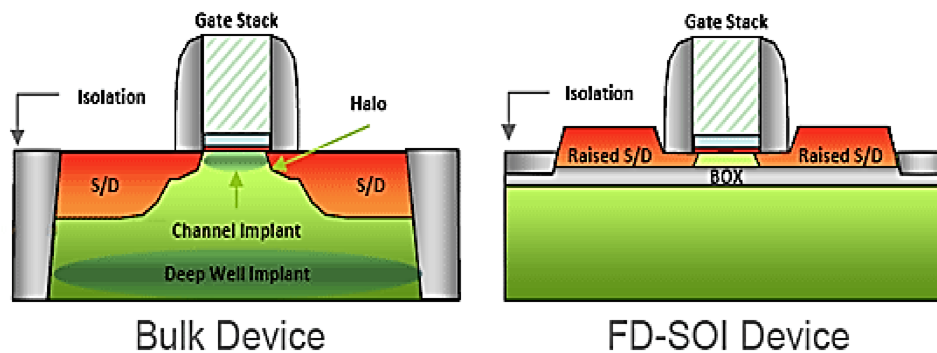

Figure 4: Bulk Device and FD-SOI Device[3]

[3] "Fully depleted SOI shows its stuff in CPU design" EDN Network <http://www.edn.com/electronics-news/4364007/Fully-depleted-SOI-shows-ts-stuff-in-CPU-design>

GEOGRAPHICAL COVERAGE

Figure below represents the geographical filing trend of patents/patent applications related to FinFET technology. The United States has seen maximum number of patent filings in domain of FinFET technology. China, Japan, Korea and Taiwan have also seen good number of patent filings. The patent/patent applications filing trend is fairly distributed and covers most of the developed and developing nations. The targeted customer of companies working in FinFET technology primarily comprise of people using smartphones and other computing devices.

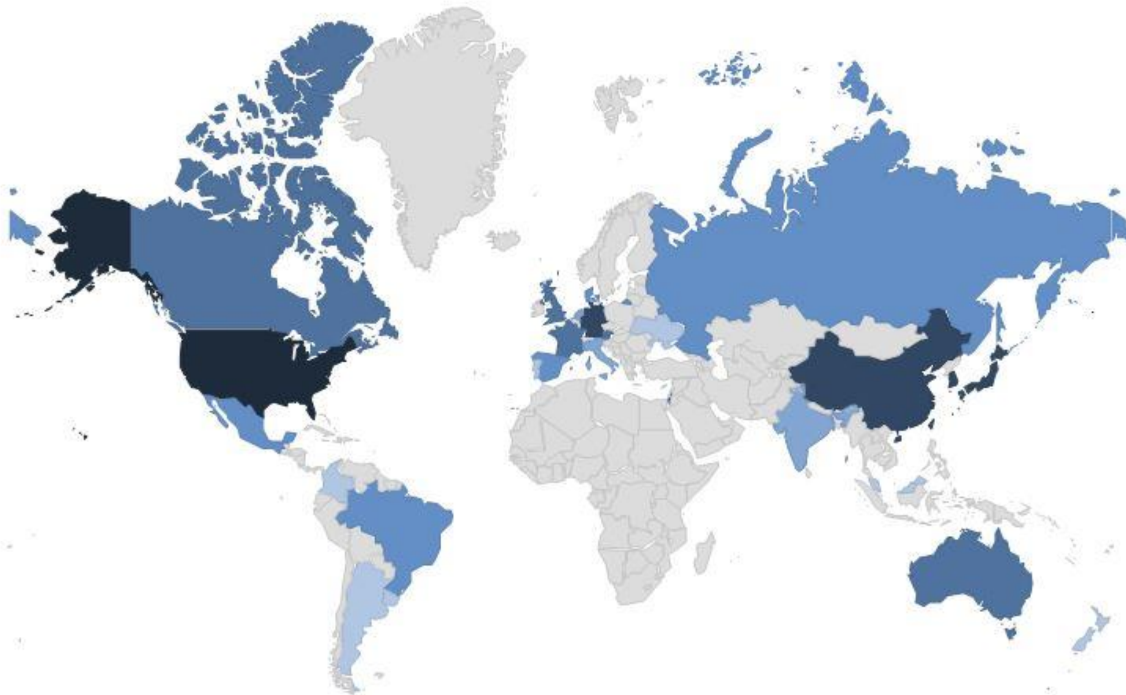

Figure 5: Geographical coverage of the patents/patent applications filed in FinFET technology

Consumers are switching to much smaller devices owing to the ease of handling and portability. With FinFETs in picture, it is possible to create even smaller and power efficient devices. It was almost impossible to create transistors below 28nm, but FinFET has brought a revolution and has further decreased the transistor size down to 14nm. Companies like Intel are already working at 10nm FinFET technology. US and European Union have seen rising trends in this technology.

LexScore™

We use LexInnova's proprietary LexSore^{TM} framework to identify leaders in the FinFET technology domain, from the perspective of intellectual property. Figure 6 depicts the competitive positioning of top 15 assignees, in FinFET technology domain. The assignees are compared on the basis of filing score and quality score. We use our proprietary algorithm (based on bibliographical information and claim characteristics of an invention) to calculate the quality of inventions.

The green region comprises of assignees that have large number of patents in IP portfolio and fairly good patent quality. The top 3 assignees, IBM, TSMC and Intel, appear in this region owing to their huge portfolio of patents/patent applications. TSMC and Intel have high quality score as compared to IBM. IBM has already moved away from semiconductor market with the announcement of transferring majority of its semiconductor business to GlobalFoundries. This announcement leaves TSMC and Intel as the major leaders in this technology domain. TSMC has good claim broadness and GeoScore, while Intel has good claim broadness but average GeoScore. After the acquisition of Tokyo Electron Limited by Applied Materials, their combined patent portfolio has a good quality score as well as filing score. As a result Applied Materials has moved into the green region. This allows them to become a top supplier for FinFET technology manufacturing equipment. Toshiba appears on the green-blue boundary with low claim broadness and average GeoScore. Toshiba has filed most of its patents in US and japan only, hence its quality score will improve as it enhances its geographical distribution.

The blue region contains assignees that possess good quality patents but lack on the patent filing front. Some significant assignees lying in this region are Samsung Electronics, AMD, Micron Technology, Tokyo Electron, Synopsys, etc. Synopsys emerges as the top EDA vendor in FinFET technology outpacing Cadence and Mentor Graphics. Samsung despite being the one of the top FinFET manufactures lacks the patent quality of its competitors like Intel and TSMC.

The red region contains assignees that possess low quality patents and lack on the patent filing front as well. United Microelectronics, Global Foundries, Applied Materials are the significant names appearing in this region. Global Foundries has tried to close the gap through licensing agreement with Samsung and acquiring IBM's semiconductor manufacturing business.

Huawei Unveiled Nova, World's First 16nm FinFET 64-Bit Networking Chip. It supports GSM /UMTS / LTE FDD / LTE TDD on a single chip. This SoC is based on ARM64 architecture, and the 16FinFET process. Huawei claims that this chip is 67% more efficient than regular chips.

The beige region comprises of assignees that have a big patent portfolio in terms of number of patents/patent applications but are lacking in patent quality.

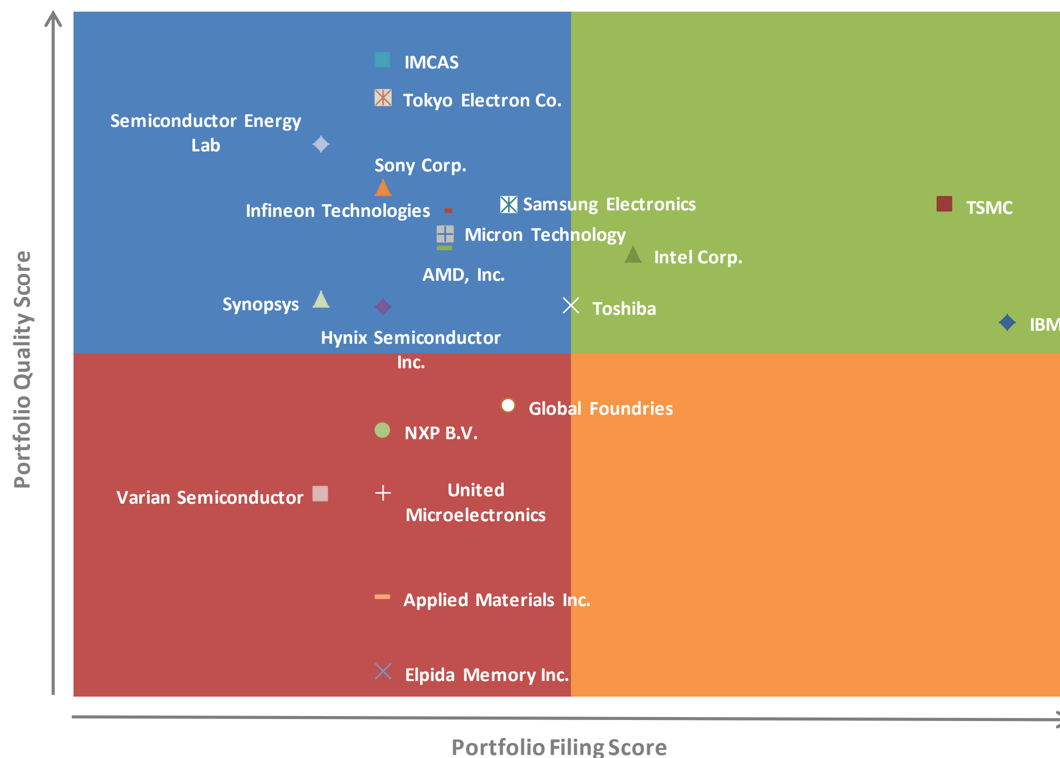

Figure 6: LexScore™

From a bird's eye view, Intel seem to be clear front runner in this industry. Intel's dominancy can be attributed to the fact that they are virtually the only IDM (Integrated Device Manufacturer) left in the semiconductor industry. Although Intel is working to increase its foundry business to maximize revenue of its process lead, foundry's contribution to overall Intel's revenue is still not significant. Though Samsung still handles a major amount of its own product manufacturing, it still has high foundry revenue mainly due to manufacturing of Apple's iPhone and tablet processors.

Node transitions were difficult and occasionally troublesome, but the end results were almost always predictable. Higher short-term costs of new nodes would be more than counterbalanced with improved transistor performance, density and high yields. This degree of predictability is what made the pure-play foundry model work. To counter high start-up cost of new node foundries fabless companies like Nvidia is pushing for new agreements in which custom IP design, R&D costs, and risk production expenses are shared more equitably between foundry and fabless semiconductor company.

Taiwan Semiconductor Manufacturing Co. (TSMC), the world's largest chip foundry, is suing a former R&D employee on the suspicion that he leaked secrets including but not limited to 28 nm process technologies to Samsung.

Copy Exactly!" is Intel's method for replicating successful chip designs across its factories worldwide. The work begins at the company's engineering fabs — **D1C, D1D. Copy Exactly!**, which Intel began following in the late 1980s, is designed to control virtually every manufacturing variable that can be controlled. That starts with ensuring that every production line uses the same machinery, and extends to such seemingly minute details like the ambient humidity, the precise degree of air filtering, the exact color temperature of the room lighting, and the barometric pressure.

The benefit of this method is shown in the following graph. Intel began working on Copy Exactly! after it had trouble at the 500nm node and refined the process through each successive generation. The green line shows the initial product ramp at its first fab — after an early spike, yields cratered and only recovered over a period of months. Once Intel had Fab 1 working well on 0.5um, it started ramping Fab 2 only to run into new problems. As Copy Exactly! was developed and deployed, the company's yields synchronized across the various fabs.

Analysts say that given TSMC's technology leadership, they were surprised when Samsung came abreast of TSMC in FinFET chips, the first of which are expected to be commercially available this year.

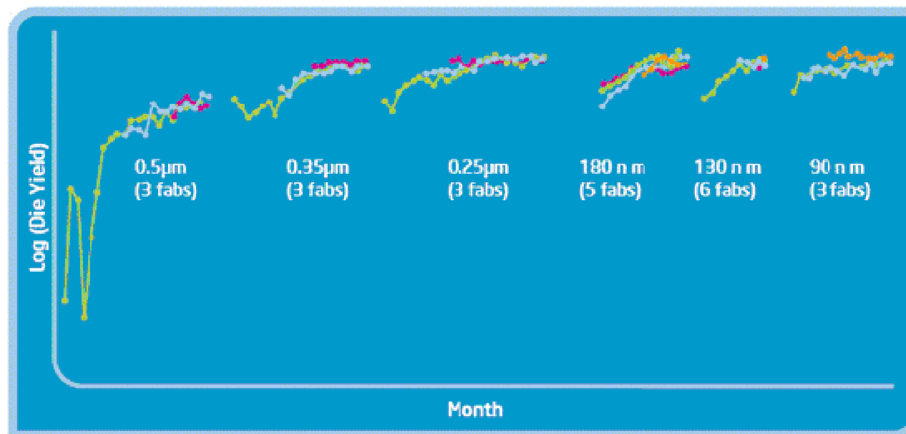

Figure 7: Die Yield v. Month for Intel Corp.[4]

Copy Exactly! Doesn't solve any initial yield or ramp problems, but it helps ensure that such issues don't reoccur at different factories. This, in turn, gives Intel a critical degree of manufacturing flexibility. One of the downsides to a factory with higher yields on Product A than any other facility is that the fab in question is effectively stuck making Product A until the engineering teams can figure out what's causing the discrepancy.

Intel's "tick-tock" model is a way the company manages architectural and process technology node changes. Historically, Intel always tended to follow a tick-tock cadence in which new architectures debuted on established processes followed by die shrinks (process technology node change), but the gap between

[4] "Manufacturing Processes, Copy Exactly!" Intel < http://www.intel.com/content/www/us/en/quality/exact-copy.html>

the two was often uneven and didn't necessarily correspond to product names in a coherent fashion. The first iteration of the Pentium III (Katmai), for example, was basically a Pentium II with SSE support. When Intel moved to 180nm and launched Coppermine, the chip's onboard L2 cache made it significantly faster, clock-for-clock, than its predecessor.

Tick-tock's cadence organizes and deploys new technologies in a consistent fashion. This reduces the chance that a feature added comparatively late in the design cycle will create an unexpected problem in final silicon and streamlines consumer product messaging and gives engineers a solid timetable when it comes to determining which technologies are included in the next revision and which are put back for further development.

Apart from these, certain other obvious factors that contribute to Intel's dominancy in this sector are their superior R&D spending which is generally more than any other semiconductor manufacturer and their talented pool of engineers. Intel's secret is how well engineers in research, development, and manufacturing work together as a team.

If the problems facing future CMOS scaling could be solved by additional funds, AMD and GlobalFoundries wouldn't be at odds with each other. ATIC, the investment company that owns a sizable share of GlobalFoundries, has infused billions into the company since its inception. This infusion of capital was precisely what AMD couldn't afford and it was envisioned to help GlobalFoundries quickly close the process node gap with Intel. Instead, the company ran into serious trouble with its 32nm HKMG technology. Those issues, according to both AMD and GlobalFoundries, are now behind it — but full standardization will be a challenge. GlobalFoundries's acquisition of Chartered Semiconductor in 2010 gave it a good deal of additional fab capacity.

Intel's advantage is the due to the synergy and close collaboration between CPU designers and process engineers, excellent manufacturing controls, and vigorous, continuing investment into R&D. It's by no means certain that these practices will carry the company easily through 14nm, but their success thus far speaks for itself. Whether TSMC or Samsung or GlobalFoundries can achieve similar results within the limitations of this business model is yet to be seen.

TSMC had officially said it will not begin mass production of chips on its 16-nanometer FinFET technology until July 2015; it appears to be about five months behind Samsung on volume production of FinFET chips. This had a negative impact on fabless company Qualcomm which was forced to design Snapdragon on 20nm planar and losing out ~$1b in revenue in 2015 by not being competitive (high power consumption) for Samsung S6 smartphone.

Intel had stated that it would bring 14nm in with substantial scaling in transistor fin pitch, transistor gate pitch, and interconnect pitch, with a further significant reduction in SRAM scaling.

An independent analysis and reverse engineering from Chipworks has confirmed that Intel did indeed deliver on its technological promises. Gate pitch has been measured at ~70nm, fin pitch at ~42nm, and a more complex 13-layer metal design.

TSMC is also missing out on wafer fabrication revenue generated by Snapdragon processor.

It is known that Apple has moved back to Samsung for manufacturing of its next-generation A9 applications processor despite them being direct competitors. Some reports indicate Samsung will handle this job exclusively while others state it will be split between Samsung and Taiwan Semiconductor. In any case, it seems Samsung is ready to go first.

At this point, Samsung production readiness rules out the possibility of the Apple A9 being built on older 20-nanometer manufacturing technology as has been rumored this chip should benefit from all the benefits FinFET manufacturing technology is expected to bring. The recently unveiled Samsung Galaxy S6 features an Exynos 7 Octa built on this new 14-nanometer technology. However, given that the S6 should be a relatively high volume phone, it is not clear if Samsung has enough 14n capacity in place yet to service such a large rollout. But rest assured, Samsung has clearly beaten TSMC to FinFET mass production in the race between foundry giants.

LICENSING HEAT MAP

We use our Proprietary Licensing-Heat Map (Figure below) framework to identify technology sub-domains in the field of FinFET technology where licensing activity is expected to be higher. The size of the sections (representing different technology domains) in the Heat Map indicates the number of patents/patent applications filed in this domain which implies the relative importance of the technology sub-domain whereas the color here represents the chances of future licensing activity in this domain. We study the patent holding pattern to color code the technology sub-domain for future licensing activity.

Red color (and shades thereof) signifies a high chance of licensing activity in a certain technology sub-domain whereas the green color (and shades thereof) represents a low chance of licensing activity in the technology sub-domain. We follow 80-20 rule to decide the colors, yellow is assigned to the domains that lie on the average case (i.e. 20% assignees having 80% of the patents/patent applications). The color drifts towards shades of red if 20% assignees possess less than 80% of the patents/patent applications, while it drifts towards shades of green in the reverse case.

TSMC is planning a $16B mega-fab installation at the Taichung science park in Central Taiwan. The planned investment would be even larger than the expected growth in fab costs through the 10nm node and suggests that TSMC is sending a message to its rivals at Samsung, GlobalFoundries, and to some extent, Intel — the company is willing to spend whatever it takes to regain its lost ground and grow its market share.

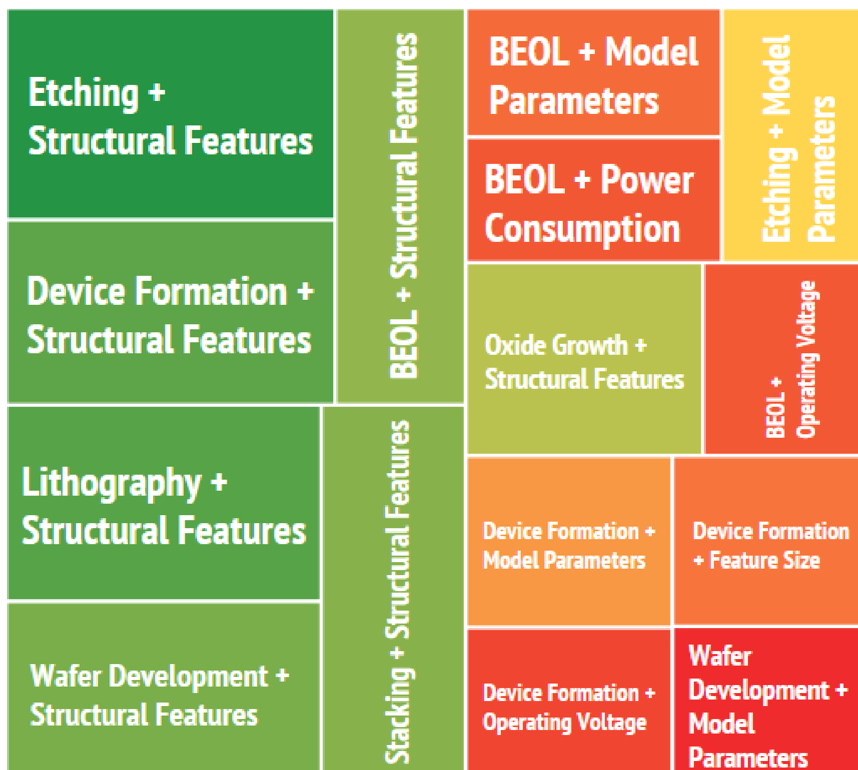

Figure 8: Licensing Heat Map

Sub domains like Etching, Device Formation and Lithography combined with the structural features have the highest number of patent/patent applications in the FinFET technology while domains like Model Parameters and Power Consumption in BEOL which is a second portion of IC fabrication has relatively lesser number of patent/patent applications. As mentioned above sub domains which are dark red in the heat map have higher chances of licensing activity as compared to domains which fall in the lighter shades. Model parameters related to Wafer Fabrication and Operating Voltage in Device Formation and BEOL are red in color which reflects a very distributed portfolio with no monopoly of any assignee in these domains. While domains like Etching, Device Formation and Lithography combined with the structural features fall in the lighter shades reflecting that the patent portfolio in these domains is predominantly held by some top players.

Top 15 tech. sub-domains / Top 10 Companies	IBM	TSMC	Intel	Global Foundries	Micron Tech	AMD	Samsung Electronics	Toshiba	Infineon Tech	Hynix
Etching + Structural Features	616	475	263	224	145	126	91	54	41	27
Device Formation + Structural Features	341	342	258	147	113	122	74	55	51	21
BEOL + Structural Features	318	377	172	63	38	47	45	51	44	13
Lithography + Structural Features	435	262	89	133	106	66	73	43	47	14
Wafer Development + Structural Features	440	234	152	98	57	75	58	28	55	8
Stacking + Structural Features	295	220	137	31	24	14	36	44	19	3
BEOL + Model Parameters	72	42	28	12	11	3	6	27	9	12
BEOL + Power Consumption	23	41	22	7	2	6	11	17	5	3
Etching + Model Parameters	66	33	39	21	3	10	19	23	3	27
Oxide Growth + Structural Features	120	46	50	38	31	17	12	11	10	2
BEOL + Operating Voltage	44	47	20	8	0	6	8	21	5	6
Device Formation + Model Parameters	42	32	75	15	7	10	20	15	7	21
Device Formation + Operating Voltage	44	35	19	12	5	7	13	16	10	14
Device Formation + Feature Size	14	33	26	8	42	14	12	11	8	9
Wafer Development + Model Parameters	67	16	16	10	2	14	4	11	4	7

Table 2: Assignee Focus in respective technologies

Table 2 shows the focus of top 10 assignees in various technology sub-domains. As can be seen from the figure, IBM, TSMC and Intel are leading in most of the technology domains. IBM has shown keen interest in almost every technology domain except 'Device Formation + Feature Size', and 'BEOL and Power Consumption'. While TSMC shows a little interest in wafer development with an impact on Model Parameters. Intel has shown keen interest in device formation with an impact on model parameters. Among the top fab companies (Intel, TSMC, GlobalFoundries, Samsung), Samsung seem to have the least impressive

patent portfolio, so we can expect out-licensing of patents by small companies with Samsung. For example, Micron Technology is leading in 'Device formation with impact on feature size' which is eventually very crucial for manufacturing FinFETs. Therefore, out-licensing opportunities exist between Micron Technology and Samsung. Similar out-licensing opportunities can be predicted from the trends in the table above.

APPENDIX

Taxonomy Heads	Definition
Front-end-of-line (FEOL)	The inventions related to this category cover FEOL processes. FEOL is the first step in the IC fabrication process in which the semiconductor devices are patterned on semiconductor wafer. It covers everything up to the deposition of metal interconnect layers.
Wafer Development	The inventions related to this category cover wafer development techniques. Wafer Development refers to crystal growth, wafer slicing, oxidation, and polishing of the base wafer layer. The wafer is processed before forming individual devices (transistors) on it.
Oxide Growth	The inventions related to this category cover methods for oxide growth on the semiconductor wafer. In this process, wafers are placed in a high-temperature furnace. By exposing wafers to a flow of Oxygen gas, silicon dioxide film is formed on the wafer surfaces.
Lithography	The inventions related to this category cover lithography techniques. It is the first step in pattern formation. In this process, a pattern from a photomask is transferred to the surface of the wafer. For example, the gate area of a MOS transistor is defined by a specific pattern. The pattern information is recorded on a layer of photoresist which is applied on the top of the wafer.
Etching	The inventions related to this category cover etching techniques. Etching is used to remove material selectively in order to create patterns. The pattern is defined by the etching mask, because the parts of the material, which should remain, are protected by the mask.
Device Formation	The inventions related to this category cover device forming techniques. Device formation refers to the formation of gate, source and drain on the wafer layer. Gate electrode is formed by oxidation, and source and drain are formed by doping by ion-implantation method.
Stacking	The inventions related to this category cover stacking techniques. Stacking is an important step in the formation of 3D devices. In this process, the individual devices are stacked on the top of other devices and are interconnected by wire bonds.
Back-end-of-line (BOEL)	The inventions related to this category cover BEOL processes. BEOL comprises of vias and interconnects formation. The holes are developed in the substrate layers and are filled with metal to create interconnects between the different layers of a device and adjacent devices.
Assembly / Packaging	The inventions related to this category cover assembly or packaging techniques. Assembly techniques and packaging involve process of choosing the right type of package for a particular integrated circuit type, and assemble the integrated circuit in the form of die into package that can be used for application.

Testing	The inventions related to this category cover testing techniques. This is the final step in the manufacturing of semiconductor devices. The devices are tested by using a prober or any suitable testing devices, and the devices which fail the test are rejected.
Structural Features	The inventions related to this category cover the structural features of FinFET devices. Structural features include number of gates (double-gate or tri-gate), structure of the fins, and interconnect between the devices.
Design Flow	The inventions related to this category cover the design flow techniques, which include Design Rule Check (DRC), Layout vs. Schematic Check (LVS), parasitic extraction (PEX) which are used to test the efficiency of a device.
Model Parameters	The inventions related to this category cover the modeling parameters. Modeling parameters comprises of corner effect, short channel effect, quantum effect, parasitic, etc. which have a great impact on the performance of a device.
Power Consumption	The inventions related to this category cover the parameters regarding power consumption of a device. It refers to the electrical power consumed by a device during its operation.
Feature Size	The inventions related to this category suggest information related to the feature size of a semiconductor device. Feature size refers to the size specifications of a device, for example, transistor size, transistor width, area, etc.
Operating Voltage	The inventions related to this category suggest information related to operating voltage of a device. Operating voltage is the minimum voltage required for the proper operation of a device.
Operating Speed	The inventions related to this category cover information related to operating speed of a device. Operating speed refers to the time taken by a device to generate the output after an input is applied to it.
Static Leakage Current	The inventions related to this category cover information related to static leakage current in a device. Static Current leakage refers to the current that flows to the ground while the device is in off-state.

Table 3: Definitions of Level 3 Technology Heads in Taxonomy

ABOUT US

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