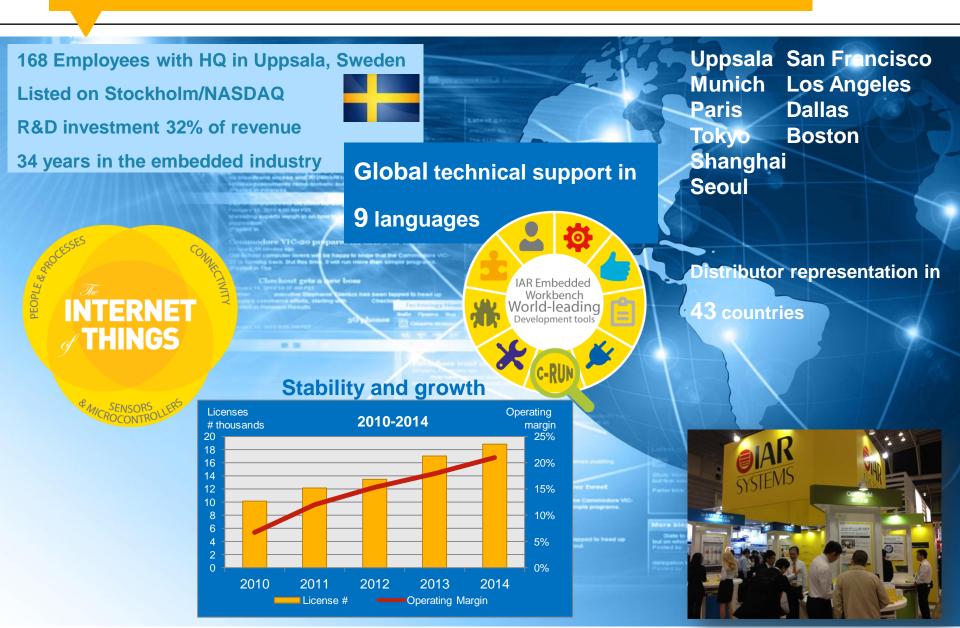
Take full control of your MCU software development

Ryan Sheng ryan.sheng@iar.com



IAR Systems





IAR Embedded Workbench C/C++ compiler and debugger toolchain



Outstanding optimization for both

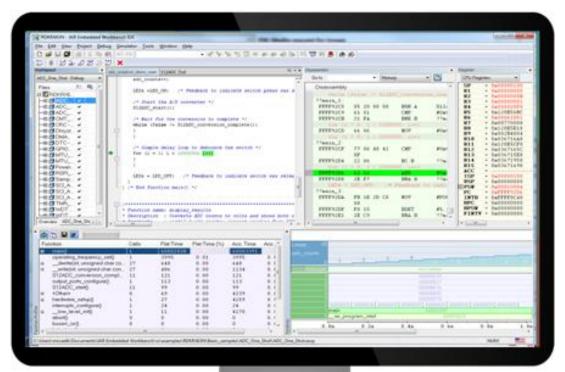
compact code size and high performance

Comprehensive debugger

User-friendly features and broad ecosystem integration

Global technical support





MISRA-C checker ARM ABI compliant



IAR Embedded Workbench Device support for NXP MCU/MPU



IAR Embedded Workbench for ARM

- LPC, Kinetis
- i.MX, Vybrid
- S32K, MAC57D5xx

IAR Embedded Workbench for ColdFire

• V1, V2, V3, ColdFire+

IAR Embedded Workbench for HCS12

• 16-bit HC12, S12 devices

IAR Embedded Workbench for S08

8-bit S08 devices

IAR Embedded Workbench for 8051

• 8-bit LPC7xx, LPC9xx, ...



IAR Embedded Workbench for ARM

- Unique independence with support for all available ARM cores, from all major vendors including NXP, ST, TI, Cypress, Microchip, Renesas, SiLabs, Toshiba, etc.
- 5,000+ supported devices
- Close cooperation with SoC vendors







IAR Embedded Workbench for ARM Recent updates and highlights



- Updated IDE look and feel
- Support C11 (ISO/IEC 9899:2011) standard
- Support C++14 (ISO/IEC 14882:2014) standard
- Enhanced compiler optimizations (for speed)
- Support Cortex-M23 & Cortex-M33 (ARMv8-M)
- CMSIS-Pack
- I-jet Trace for ARM (Cortex-A/R/M)
- Flash breakpoint
- Multi-core debugging
- Stack usage analysis
- Enhanced static and runtime code analysis

IAR Embedded Workbench for ARM Outstanding compiler optimization



•Leading compiler optimizations enable IAR Embedded Workbench to generate the most compact and fast performing code.

- Smaller memory size
- Better real-time reaction
- Lower power consumption

•EEMBC proved code performance: Find the leading CoreMark® scores on the website.

www.eembc.org/ coremark

:	EM	
-	BC	

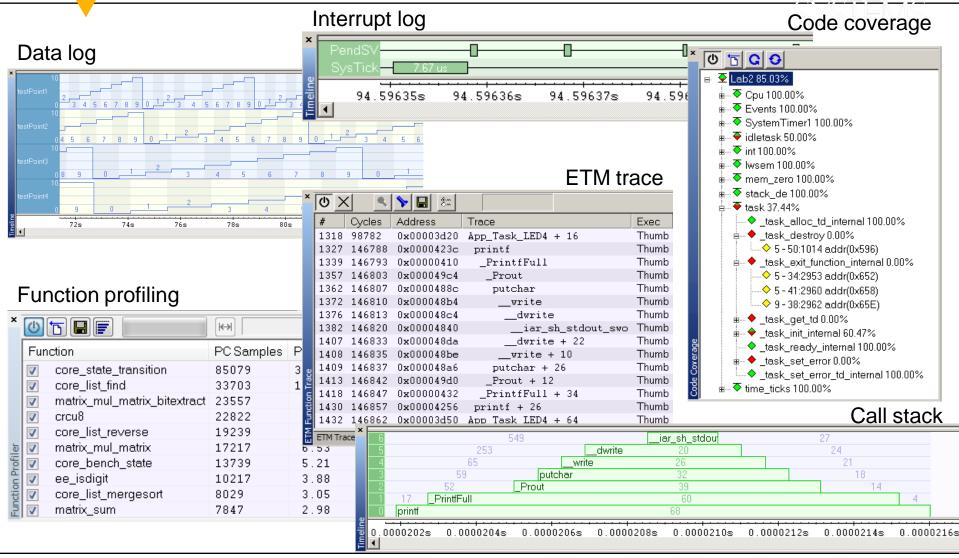


IAR Embedded Workbench generates

	Processor	Compiler	Operating Speed in Mhz	CoreMark /MHz ⁽¹⁾	CoreMark (1)
Cortex-M7	NXP Kinetis KV5x	IAR v7.50.3	240	5.00	1211.00
Cortex-M4	NXP Kinetis K70 90nm	IAR v6.50	150	3.40	510.02
Cortex-M0+	NXP KL25	IAR 6.60	48	2.41	115.46
Cortex-M0+	NXP KL05	IAR 6.60	48	2.42	116.18

IAR Embedded Workbench for ARM Advanced debugging & trace





IAR Embedded Workbench for ARM Functional safety certification



Functional safety certified edition of IAR Embedded Workbench for ARM

- IEC 61508
- ISO 26262
- EN 50128

Simplified validation

- Functional safety certificate
- Report of the certificate
- Safety Guide

Guaranteed support through the product life cycle

- Prioritized technical support
- Validated service packs
- Regular report of known problems



IAR I-jet & I-jet Trace Hardware debuggers for ARM

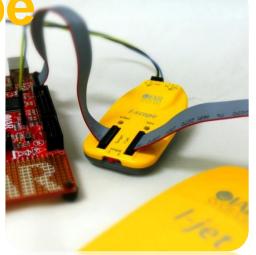


I-jet for ARM

I-jet provides an exceptionally fast debugging platform.

for ARM

I-scope is a small probe that adds current & voltage measurement capabilities to I-jet.



I-jet Trace



3rd-Party Debuggers

CMSIS-DAP Segger J-Link / J-Trace P&E Micro Multilink P&E Micro Cyclone

I-jet Trace delivers large trace memory capacities and high-speed communication via SuperSpeed USB 3.0.

Generate IAR example projects using NXP MCUXpresso Tools



MCUXpresso Software and Tools





for Kinetis and LPC microcontrollers

MCUXpresso IDE

Edit, compile, debug and optimize in an intuitive and powerful IDE



IDE

MCUXpresso SDK

Runtime software including peripheral drivers, middleware, RTOS, demos and more



MCUXpresso Config Tools

Online and desktop tool suite for system configuration and optimization

MCUXpresso Config Tools

<u>mcuxpresso.nxp.com/zh/welcome</u>



MCUXpresso配置工具提供一套系统配置工具,通过基于Kinetis或LPC的MCU解决方案为各级用户提供帮助。它可引导帮助您完成从初次评估到生产开发的整个过程。



IAR

SYSTEMS





Create a new configuration





创建新配置

按器件、电路板和套件名称搜索,并支持按部分字符过滤。

- <u>mcuxpresso.nxp.com/zh/builder</u>
- Select from:
 - Boards
 - Processors
 - •Kits
- Select configuration
- Specify configuration settings
- Jump start you configuration

按名称搜索

搜索...

选择器件、电路板或套件

▼ 电	各板
•	Kinetis
•	LPC
	LPCXpresso54114
	LPCXpresso54608
	LPCXpresso54S618
▶ 处	里器
▶ 套	4

为您的配置命名

LPCXpresso54	LPCXpresso54114				
选择配置	指定其他 配置设置	快速开始您的配置			



Configuration settings





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Download a SDK archive







生成可下载的SDK存档以与桌面MCUXpresso工具搭配使用。

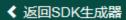
下载SDK 生成存档项

当前配置

如果10秒后未开始下载,请单击以下链接,开始下载软件包:

SDK_2.2_LPCXpresso54114.zip

LPCXpresso54114 💙



查看 SDK 详情

您的 SDK 下载将包含侧边面板列出的项目。 可使用"工具"->"配置设置"页编辑这些选 配置设置 页

此MCUXpresso SDK配置可直接下载



软件包名称

SDK_2.2_LPCXpresso54114



Download an existing example project





示例工程

下载一个现有的独立 SDK示例工程或加载某示例中的引脚和时钟数据到在线配置工具。

下载SDK 生成存档项

如果10秒后未开始下载,请单击以下链接,开始下载软件包:

hello_world_cm4.zip

< 返回示例工程

选择一个示例工程

+	83	=	-	
ſ	÷	矛	έ.	

LPCXpresso54114
cmsis_driver_examples
rtos_examples
driver_examples
multicore_examples
usb_examples
▼ demo_apps
hello_world
utick_wakeup
power_manager_lpc

下载示例 应用工程到配置工具

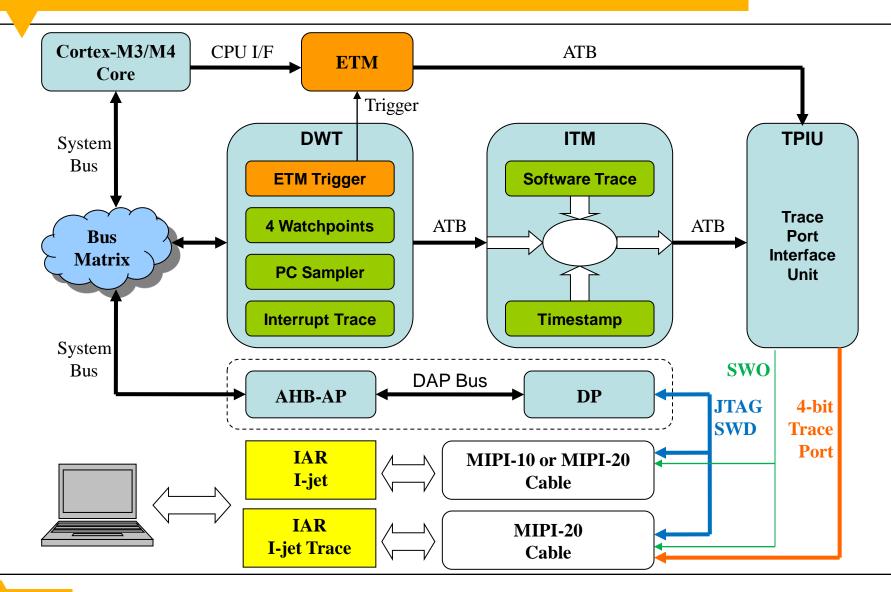


Advanced debugging & trace on LPC & Kinetis Microcontrollers



Cortex-M3/M4 trace system





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Trace pins in different connector



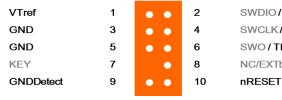
Standard 20-pin \mathbf{O} 2 VTRef Vtarget 1 (nTRST) 3 NC 4 GND NC (TDI) 5 • 6 GND GND SWDIO (TMS) 7 8 SWCLK (TCK) GND

SWCLK	(TCK)	9		10	GND
NC	(RTCK)	11	••	12	GND
SWO	(TDO)	13	• •	14	GND
nSRST		15	• •	16	GND
		17	• •	18	GND
+5V		19	• •	20	GND



JTAG/SWD

MIPI-10 0.05"



JTAG/SWD

SWDIO/TMS SWCLK/TCK SWO/TDO NC/EXTb/TDI

MIPI-20 0.05"

VTref	1	• •	2	SWDIO/TMS
GND	3	• •	4	SWCLK/TCK
GND	5	• •	6	SWO/EXTa/TRACECTL / TDO
KEY	7	•	8	NC/EXTD/TDI
GNDDetect	9	••	10	nRESET
GND/TgtPwr+Cap	11	••	12	TRACECLK
GND/TgtPwr+Cap	13	••	14	TRACEDATA[0]
GND	15	••	16	TRACEDATA[1]
GND	17	• •	18	TRACEDATA[2]
GND	19	••	20	TRACEDATA[3]

JTAG/SWD/ETM

SWO trace



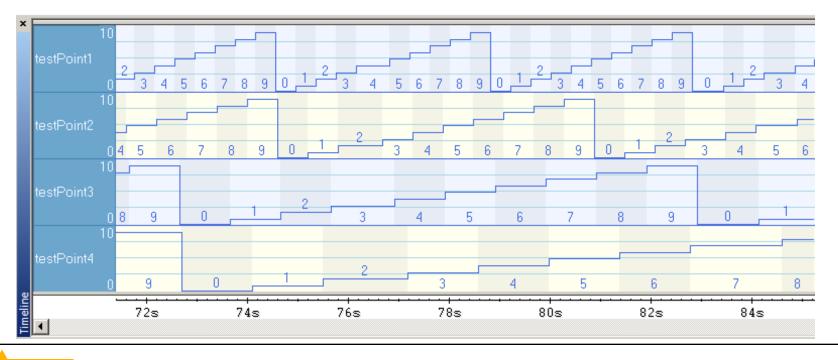
- SWO (Serial Wire Output)
 - •A serial high speed signal that transmits ITM packets
 - Events and sampling based
 - Supported by Cortex-M3/M4 architectures
 - Supported by IAR I-jet and other debuggers
- Trace information going through SWO
 - DWT (Data Watchpoint and Trace)
 - •Watchpoint: 4 independent comparators for address and data
 - •PC sampler: Sampling the PC register at regular intervals
 - Interrupt trace: Logging the enter and exit of each interrupt
 - ITM (Instrumentation Trace Macrocell)
 - •Generate ITM events on 32 independent ports
 - Packetize and timestamp the DWT events



Static variables monitoring



- DWT generates trace events when one of the watchpoint finds a match on specified address/data.
- Up to four different static variables can be monitored together.
- C-SPY displays the collected trace information in the Data Log window and the graphical Timeline window.



Using data log breakpoints

Edit Breakpoint



×

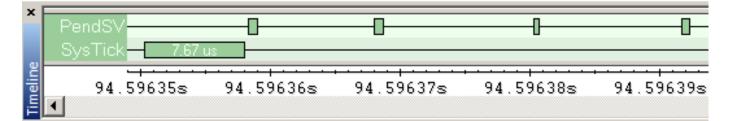
Right-click on the name of a variable to be monitored:

Find in Trace Toggle Breakpoint (Code) Toggle Breakpoint (Log) Toggle Breakpoint (Trace Start) Toggle Breakpoint (Trace Stop) Toggle Breakpoint (Trace Stop) Toggle Breakpoint (Trace Filter) Enable/disable Breakpoint Set Data Breakpoint for 'testPoint1' Set Trace Start Breakpoint for 'testPoint1' Set Trace Stop Breakpoint for 'testPoint1' Set Next Statement Quick Watch: 'testPoint1'	Trigger at: testPoint1 Access type © Read/Write © Read © Write	Edit Size Auto (4) Manual Trigger range Requested: (0x20002DE0 - 0x20002DE3 Effective: (0x20002DE0 - 0x20002DE3 Effective: 0x20002DE0 - 0x20002DE3 Effective:	The breakpoint is triggered when the variable at 0x20002DE0 is read or written as a word (4 bytes). DWT will generate an event but the execution will not be stopped. Go to Source Edit Delete
Check the status and edit the			Disable
properties of the breakpoint in View → Breakpoints:		OK Cancel	Enable All Disable All Delete All
* Breakpoint			
🗳 🔽 🛛 Data Log @ testPoint1 [s	ize 4] [Read/Write]	[0x20002DE0 - 0x20002DE3]	New Breakpoint 🕨
variable name	access type	variable address	

Interrupt logging



- DWT generates trace events when entering or leaving any interrupt.
- C-SPY displays the collected trace information in the Interrupt Log window and the graphical Timeline window.
- Useful to find interrupts which can be fine-tuned to execute faster and analyze problems with nested interrupts.



×	Cycles	Interrupt	Status	Program Counter	Execution Cycles
	164998943	PendSV	Enter		
	164998965	PendSV	Leave		22
	164999263	PendSV	Enter		
	164999285	PendSV	Leave		22
8	165045163	SysTick	Enter		
Interrupt Log	165045469	SysTick	Leave		306
	165093175	SysTick	Enter		
Ĕ	165093480	SysTick	Leave		305

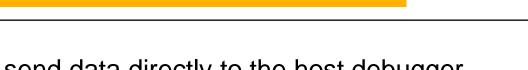
Function profiling



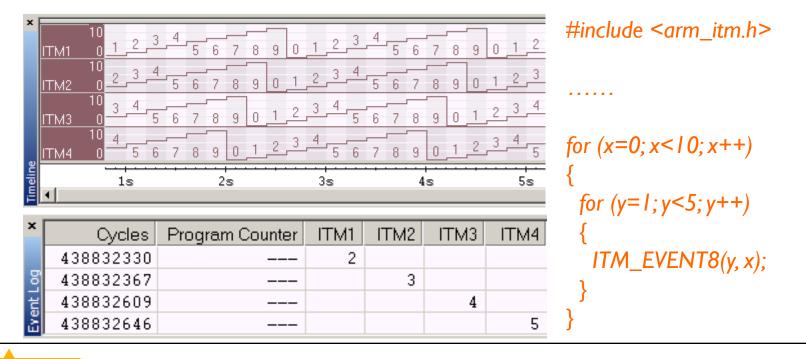
- Code profiling information of each C function is retrieved by counting the number of PC samples generated by the PC sampler of DWT.
- Useful to find where the CPU is spending its time.
- Functions where the most time is spent should be carefully optimized or moved to more efficient memory to increase the performance.

×	ወ 🚡		K⇔I		
	Functio	n	PC Samples	PC Samples (%)	
	1	OS_TaskIdle	1132423	46.58	
	V	OSTaskidleHook	703766	28.95	
	V	OS_CPU_SR_Save	288266	11.86	
<u>b</u>	V	OS_CPU_SR_Restore	196211	8.07	
unction Profiler	1	App_TaskIdleHook	93401	3.84	
ЦЦ	1	OSTimeTick	11188	0.46	
ctio	V	OSTaskStkChk	1987	0.08	
E	V	OS_TaskStatStkChk	931	0.04	

Direct output via ITM stimulus ports



- The target application can send data directly to the host debugger through ITM stimulus ports.
- Each of the 32 ITM ports has its own address (based at 0xE000000).
- C-SPY displays the data sent from ITM port #1~#4 in the Event Log window and the graphical Timeline window.



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Execution time measurement



- Use the functionality of ITM events to measure the time consumption of a piece of code.
- Send two ITM packets before and after the code to be measured and the actual execution time is the interval between them.
- · Easy, accurate and no additional equipments are required!

×	Cycles	Program Counter	ITM1	ITM2	ITM3	ITM4	#include <arm itm.h=""></arm>
	286540110		0x00000055				
	373218529		0x000000AA				
	382817996		0x00000055				ITM_EVENT8(1, 0x55);
	476367457		0x000000AA				CodeToBeMeasured();
8	485966926		0x00000055				
t	580480993		0x000000AA				ITM_EVENT8(1, 0xAA);
a A	590080464		0x00000055				

Time consumption of CodeToBeMeasured() on a 100MHz CPU:
 (476367457 – 382817996) / 10000000 = 0.935 (s)



Instruction trace



- Collect a sequence of every executed instruction continuously for a selected portion of the program.
- Developers can inspect the program flow up to a specific state and locate the origin of the problem.
- Very useful for locating errors that have irregular symptoms and occur sporadically.
 - Illegal instructions and data aborts
 - Runaway programs
 - Interrupt/exception problems
 - Context switch problems

•

- Also helpful for analyzing dynamic system behaviors
 - Code profiling
 - Code coverage



Instruction trace techniques



- ETM (Embedded Trace Macrocell)
 - •Off-chip trace buffer (in the probe, 2~32 MB)
 - •4~16-bit data bus at CPUCLK or CPUCLK/2
 - ·High requirement on the board design, e.g. for acceptable signal quality
 - Expensive trace probes required (e.g. JTAGjet-Trace)
- ETB (Embedded Trace Buffer)
 - On-chip dedicated trace buffer (small a few Kbytes)
 - •No extra pins, no requirement for trace probes
 - ·Cortex-M3, Cortex-M4
- MTB (Micro Trace Buffer)
 - On-chip configurable trace buffer (small a few Kbytes)
 - No extra pins, no requirement for trace probes
 - Cortex-M0+

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Collect executed instructions



• Go to "ETM Trace" window to check the recorded instructions together with mixed C source code.

×	U	XD	N N 🛛 🖄			
	#	Cycles	Address	Trace		Exec
Trace Enable/Disable 🦯 👘	918	48819	0x00002754	MSR	PRIMASK, RO	Thumb
				BX	LR	
Trace Declast Number	919	-	0x00002758	BX	LR	Thumb
Trace Packet Number	920	48822	0x000035d2	} POP	{R0, R4-R7, PC}	Thumb
					if ((test % 7) == 0)	
Cycles Counter		48825		LDR.N	R0, ??DataTable5_2	Thumb
	922		8x00003d4e		R0, [R0]	Thumb
In a firm of the in A deliver a	923		0x00003d50		R1, #7	Thumb
Instruction Address	924			UDIV	R2, R0, R1	Thumb
	925		0x00003d56	MLS	R0, R1, R2, R0	Thumb
Source/Discosombly	926			CMP	RO, #O	Thumb
Source/Disassembly	927	-	0x00003d5c	BNE.N		Thumb
					printf("hello");	
ace	928	48828	0x00003d76	LDR.N	R0, ??DataTable5_10	Thumb
	┛					
	ETM	Trace ETI	M Function Trace			

View the trace data at function-level



- Go to "ETM Function Trace" window to view function-level information.
- Useful to find the internal process of complex functions, or the actual calling sequence of interrupt / task switches.

# Cycles Address Trace Trace Enable/Disable 1318 98782 0x00003d20 App Task LED4 + 16	Exec
1318 98782 0x00003d20 App_Task_LED4 + 16	Thumb
1327 146788 0x0000423c printf	Thumb
Trace Packet Number	Thumb
1357 146803 0x000049c4 _Prout	Thumb
1262 146807 0x0000488c putchar	Thumb
Cycles Counter 1372 146810 0x000048b4write	Thumb
1376 146813 0x000048c4dwrite	Thumb
1362 146820 0x00004840iar_sh_stdo	out_swo Thumb
Function Address 1407 146833 0x000048dadwrite + 22	Thumb
1408 146825 0x000048bewrite + 10	Thumb
$\frac{1409}{146837}$ 0x000048a6 putchar + 26	Thumb
Function Name 1413 146842 0x000049d0 _Prout + 12	Thumb
5 1418 146847 0x00000432 _PrintfFull + 34	Thumb
$\frac{1}{2}$ 1430 146857 0x00004256 printf + 26	Thumb
2 1432 146862 0x00003d50 App_Task_LED4 + 64	Thumb
ETM Trace ETM Function Trace	



Using trace start/stop breakpoints



Right-click in the source or disassembly window:

Move to PC	
Run to Cursor	
Code Coverage	▶
Instruction Profiling	Þ
Toggle Breakpoint (Code)	_
Toggle Breakpoint (Log)	
Toggle Breakpoint (Trace Start)	
Toggle Breakpoint (Trace Stop)	
Toggle Breakpoint (Trace Filter)	
Enable/Disable Breakpoint	
Edit Breakpoint	
	_

Set Next Statement

Check the status and edit the properties of the breakpoint in View → Breakpoints:

Trace Start @ main.c:1

location in

the source

Breakpoint

Breakpoin

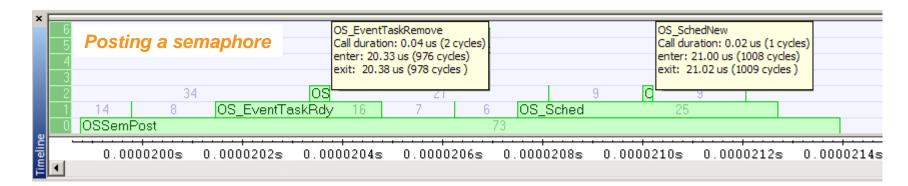
Edit Breakpoint X Trace Start Trigger at: {C:\Test\LCD_Demo\app\main.c}.163.3 Edit	
Access type Size O Read/Write Manual O Read Manual O Write Requested: O Fetch Ox0800BC94 - 0x0800BC94 Match data Effective:	The breakpoint is triggered when the instruction at the specified address is fetched.
Image: Enable 0x0800BC94 - 0x0800BC94 Value: 0x00000000	Go to Source
Mask: OxFFFFFFF	Delete Disable
OK Cancel	Enable All Disable All Delete All
63.3 [Fetch] [0x0800BC94]	New Breakpoint 🕨

address of

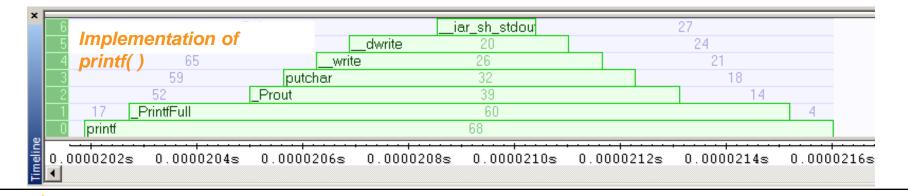
the instruction

Graphical call stack



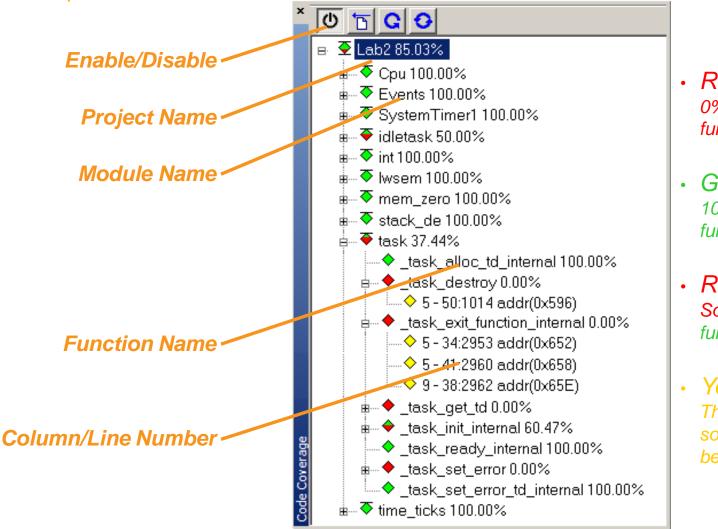


×	6 5 4 3 2		OS_EventTaskV Call duration: 0. enter: 22.04 us exit: 22.15 us (10 us (5 cycles) (1058 cycles)	Pend	ling on a	a semapl	hore	enter: 22.67 exit: 22.81	w : 0. 15 us (7 cycles us (1088 cycles) us (1095 cycles)		Call dur enter: 2	SwHook ation: 0. 13 us (6 cycl 23.29 us (1118 cycles 3.42 us (1124 cycles))
	1	25	12	OS_Eve	7	6 OS	_Sched	1		57			6	12
	0	OSSemPend							117					
Timeline	.000	00216s 0.00	00218s 0.00	00220s 0.	.0000222s	0.0000224	s 0.000022	6s 0.00	00228s 0	.0000230s	0.0000232s	0.0000234s	0.0000236s	0.0000238s



Code coverage





 Red
 0% of the module or function has been executed.

Green 100% of the module or function has been executed.

• Red & Green Some part of the module or function has been executed.

• Yellow The statement in C/C++ source code that has not been executed.

EWARM debugging environment



K60N512 - IAR Embedded Workbench IDE - AF	RM 7.70.2							×
File Edit View Project Debug Disassembl	ly I-jet/JTAGjet μC/OS-II Τοc	ls Window Help						
D 🛩 🖬 🗊 🎒 🐰 🖻 🛍 🗠 🗠	- 4 5	🍾 🛬 🛐 🖻 🧼 d	🐢 👍 💽 🕼 I	× 🕭 🕁 🗠				
5 · I · I · B · B · B · B · B · B · B · B	wo							
Workspace ×		f() 🔫 🗙 Dis	assembly		x	Register		×
Debug	1775 p_arg = p_arg		Go to	✓ Memory	▼ 1	Current CPU Registers	<find register=""></find>	•
Files 8: Bi A	$1776 = for (;;) {$	"	Disassembly		_	$R0 = 0 \times 07070707$	R9 = 0x090	90909
riles ~ 5% 5% 5% 5% 5% 5% 5% 5% 5% 5% 5% 5% 5%		CRITICAL();	-	cpu_sr = Ou;		R1 = 0x20002A48	$\mathbf{R10} = 0\mathbf{x10}$	
	1778 OSIdleCt: 1779 OS EXIT (0x2500	MOVS R5, #0	$R2 = 0 \times 02020202$ $R3 = 0 \times 03030303$	$\frac{R11}{R12} = \frac{0 \times 111}{0 \times 121}$	
		CRITICAL(); leHook();		ER_CRITICAL();	10,0 10, 10	R4 = 0x0000000000000000000000000000000000	$\blacksquare \mathbf{APSR} = \mathbf{0x12}$	
🛛 📙 🔚 app_cfg.h	1781 - }		0x2462:	0xf000 0xf97b	BL OS_CPU_	$R5 = 0 \times 000000000$	$ \pm IPSR = 0x000 $	
→ ⊞ 📴 app_hooks.c	1782 }			0x0005	MOVS R5, R0	R6 = 0x06060606 R7 = 0x07070707	$\begin{array}{rcl} & \\ & \\ \hline \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\$	
Cpu_cfg.h	1783 /*\$PAGE*/ 1784 - /*		OSIdle 0m2460	Ctr++; 0x48a5	LDR.N RO, [PC -	$R8 = 0 \times 08080808$	SP = 0x200	
K60N512	1/64 - /*		UX2468:	UX46a5	LDR.N RU, [PC	4		•
		F X 1						
¹⁰				^^ `	* 🕐 🗖 🖪 🖻 📃	(KN)		
testPoint1	2			2	Function	PCSamples PCSa	amples (%) Address	*
0 7 8 9 0	3 4	testPoint1 @ 0x200	029F4 + ?		🔽 OS_Taskidle	80243 49.7	,	47d 🔲
PendSV III/III/III/III/III/III/III/I III/IIII/III/IIII/IIII/II		SWO capture clock		Ĥ	OSTaskidleHook	38694 23.9	8 0x2852-0x2	859
SysTick				=	OS_CPU_SR_Save	20498 12.7		
INT_UART3_RX_TX		Value is 5 when PC	is 0x00003C8A	F	App_TaskIdleHook	12584 7.8		
Linear 80		Access type: Write			OS_CPU_SR_Resto	re 7651 4.7 493 0.3		
ITrgPwr [mA]		Access time: 95 989	9518.98 us (47949691	L cycles)	✓ OSIntExit	427 0.2		
a second s		Current max: 9 at 3	s 589019.15 us (1722	72919 cycles)	OSTimeTickHook	373 0.2		
10			s 989050.29 us (1914)	74414) cycles)	🛛 🔽 OSTaskStkChk	154 0.1	0 0x32fe-0x3	38f
	6	7 8	a 0	1	OS_TaskStatStkChk Image: State State State Image: State State State Image: State State State Image: State State State Image: State State Image			
	0	7 0	3 0	· · · · · · · · · · · · · · · · · · ·	S SemPend CSSemPend	34 0.0 17 0.0		
7s 8s	9s 10s	11s	12s	13s		17 0.0		
<u>i</u>				•	OS_EventTaskWait OS SchedNew	14 0.0		
×			×	1	×			
Go to 🗸 Memory			Na:		Ref Prio State	🙁 Bunning 🛛	C/OS-II RTOS V292	2 07
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Ready						Ln 1783, Col 10	System	

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Multi-core debugging



Symmetric multicore debugging (SMP)

- Debugging two or more identical cores;
- •One single debug probe;
- •One single instance of IAR EWARM IDE.
- Asymmetric multicore debugging (AMP)
 - Debugging two different cores;
 - •One single debug probe;
 - •Two cooperating instances of IAR EWARM IDE.

😵 dual_core - Master - DR Embedded Workbench IDE
File Edit View Project I-jet/JTAGjet Tools Window Help
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File Edit View Project I-jet/JTAGjet Tools Windo
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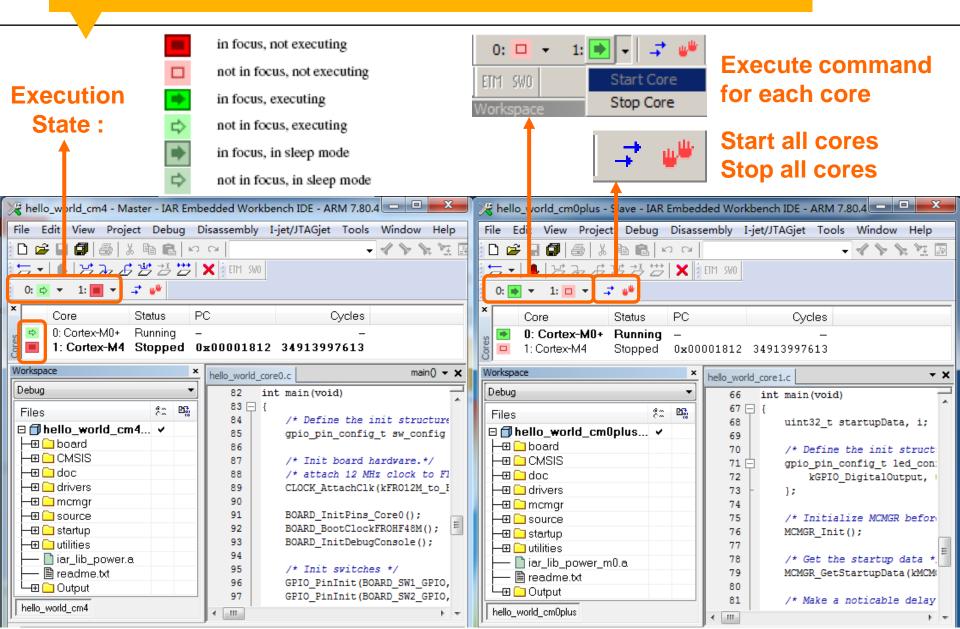
Multi-core debugging: Configuration

Factory Settings Multicore Download Images Extra Options Plugins Setup SMP: Symmetric multicore Number of cores 1 Number of Asymmetric multicore 📝 Enable multicore master mode Port: 53461 AMP: \$PROJ_DIR\$/../hello_world_cmOplus, Set the direction Slave workspace: to the slave hello world cmOplus Slave project: project in the Slave Debug master project. 📝 Attach slave to running target



Multi-core debugging: LPC54114





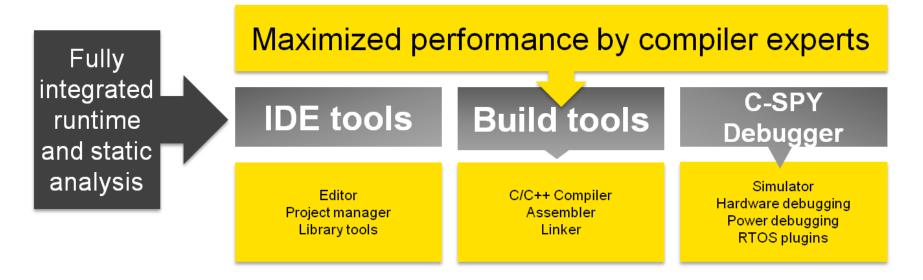
Keeping Safe at C: Static & Runtime Code Analysis



Integrated code analysis add-on tools

EIAR SYSTEMS

- Static code analysis: C-STAT
 - Analyze the C/C++ source code without executing the program.
 - Fully integrated in IAR Embedded Workbench for ARM.
- Runtime code analysis: C-RUN
 - Find C programming errors at runtime.
 - Fully integrated in IAR Embedded Workbench for ARM.



C-STAT and C-RUN





C-STAT Static analysis

C-STAT performs advanced analysis of your C/C++ code and finds potential issues. It helps you improve your code quality as well as prove alignment with standards such as MISRA C:2012.

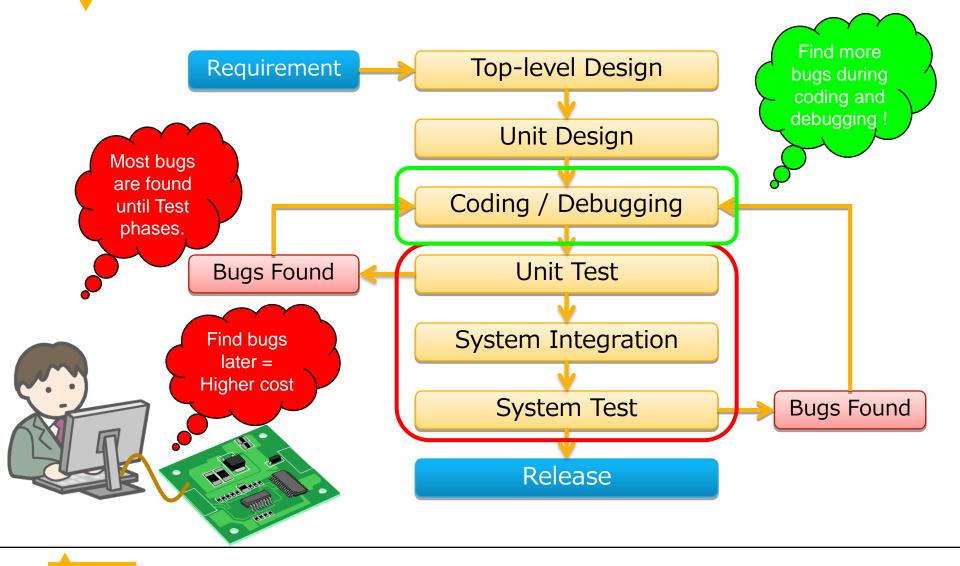
C-RUN Runtime analysis

C-RUN helps you find errors at an early stage. It is completely integrated with IAR Embedded Workbench for ARM, and provides detailed runtime error information.



Code analysis: Find bugs earlier





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C-STAT: What does it check





- Common Weakness Enumeration
- <u>cwe.mitre.org</u>
- An unified and measurable set of software weaknesses.
- Enumerate design and architecture weaknesses, as well as low-level coding errors.



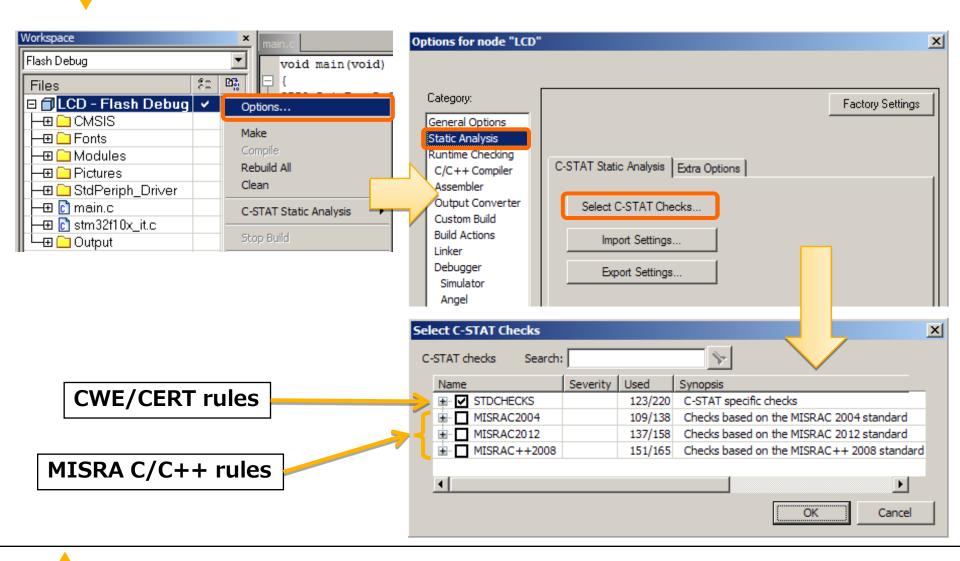
- Computer Emergency Response Team
- <u>www.cert.org</u>
- C/C++ secure coding standards, identifying insecure constructs which could expose a weakness or vulnerability in the software.
- Guidelines to avoid implementation, coding as well as low-level design errors.



- Motor Industry Software Reliability Association
- <u>www.misra.org.uk</u>
- MISRA C:2004 (MISRA C2): Identify unsafe code constructs in the C89 standard.
- MISRA C:2012 (MISRA C3): Extend the support to C99 version of the programming language whilst maintaining the guidelines for C89 standard.
- MISRA C++:2008: Identify unsafe code constructs in the 1998 C++ standard.

C-STAT: Options in IAR EWARM





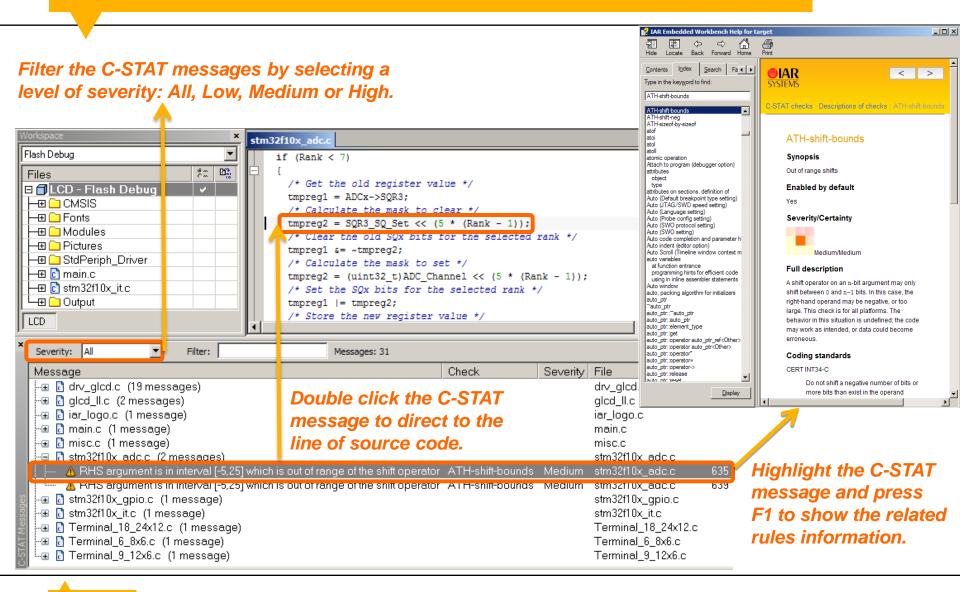
C-STAT: Rules configuration



lect C-STAT Ch -STAT checks	ecks Search:		>			×	Highlight a rule and press F1 to show the	
Name		Severity	Used	Synopsis			detailed description.	
MISRAC	2012		137/158	Checks based on the M	ISRAC 2012 standard			
	RAC2012-Dir-4		2/6	Code design				
	MISRAC2012-Dir-4.3	Low		Inline asm statements t	hat are not encapsulated i	n functions		
	MISRAC2012-Dir-4.4	Low		To allow comments to c	😫 IAR Embedded Workbench H	elp for target		
	MISRAC2012-Dir-4.6_a	Low		Uses of basic types cha				
	ISRAC2012-Dir-4.6_b	Low		Typedefs of basic type	Hide Locate Back Forward	Home Print		
	ISRAC2012-Dir-4.9	Low		Function-like macros	Contents Index Sear ()	⊜IAR	< >	
	MSRAC2012-Dir-4.10	Low		Header files without #i	Type in the keyword to find:	SYSTEMS		
	RAC2012-Rule-1		All	A standard C environm	MISRAC2012-Dir-4.3	STSTEND		
🗄 🗹 Mi Si	RAC2012-Rule-2		4/5	Unused code		C-STAT checks : Description	ons of checks : MISRAC2012-Dir-4.3	
	RAC2012-Rule-3		All	Comments	MISRAC2012-Dir-4.3 MISRAC2012-Dir-4.4			
	AC 2012-Rule-4		None	Character sets and lexi	MISRAC2012-Dir-4.6_a MISRAC2012-Dir-4.6_b	🖖		
😟 🗹 🛝 🗉	RAC2012-Rule-5		All	Identifiers	MISRAC2012-Dir-4.9	MISRAC2012	2-Dir-4.3	
	RAC2 12-Rule-6		All	Types	MISRAC2012-Rule-1.3_a MISRAC2012-Rule-1.3_b			
🖽 🔽 MIS	AC2012-Rule-7		All	Literals and constants	MISRAC2012-Rule-1.3_c MISRAC2012-Rule-1.3_d	Synopsis		
•					MISRAC2012-Rule-1.3_e MISRAC2012-Rule-1.3 f	Inline asm statement	s that are not encapsulated in functions	
					MISRAC2012-Rule-1.3 g MISRAC2012-Rule-1.3 h	Enabled by defau	ult	
					MISRAC2012-Rule-10.1_R2	Yes		
					MISRAC2012-Rule-10.1_R3 MISRAC2012-Rule-10.1_R4			
					MISRAC2012-Rule-10.1_R5 MISRAC2012-Rule-10.1_R6	Severity/Certain	ty	
					MISRAC2012-Rule-10.1_R7 MISRAC2012-Rule-10.1_R8			
					MISRAC2012-Rule-10.2			
					MISRAC2012-Rule-10.3 MISRAC2012-Rule-10.4	Low/Mediur	n	
Enchla ar dischla a sat of					MISRAC2012-Rule-10.6 MISRAC2012-Rule-10.7	Full description		
Enable or disable a set of					MISRAC2012-Rule-10.8 MISRAC2012-Rule-11.1	(Required) Assembly language shall be encapsulated and isolated		
rules or any individual rule.			MISRAC2012-Rule-11.3					
10100 0		uual	เนเธ.		MISRAC2012-Rule-11.4 MISRAC2012-Rule-11.7	Coding standard		
					MISRAC2012-Rule-11.8 MISRAC2012-Rule-11.9	MISRA C:2012 Dir-4.3	3	
					MISRAC2012-Rule-12.1	(Required) Ass	sembly language shall be encapsulated and isolated	
www.iar.co	m				Display	Code examples		
						•	•	

C-STAT: Result of analysis





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C-RUN: What does it check



Heap checking	Category: General Options Runtime Checking C/C++ Compiler Assembler Output Converter	C-RUN Runtime Checking	Arithmetic checking
Bounds checking	Custom Build Build Actions Linker Debugger Simulator Angel CMSIS DAP GDB Server IAR ROM-monitor L-jet/ITAGjet J-Link/J-Trace TI Stellaris Macraigor PE micro RDI ST-LINK	✓ Use checked heap Insert checks for ✓ Enable bounds checking Integer overflow Instrumentation Including unsigned ✓ Track pointer bounds Including explicit casts ✓ Check accesses Including explicit casts Generate functions callable from non-instrumented code Including unsigned shifts ✓ Check pointers from non-instrumented functions Including unsigned shifts ✓ Global bounds table ✓ Division by zero ✓ Unhandled switch case 1000	



C-RUN: How does it work



- Traditional runtime analysis tools:
 - Independent with compiler and debugger;
 - Different applications and license models;
 - Less knowledge about the target and optimization;
 - Insert test code at the source code level;
 - •Large overhead in memory size and execution speed.
- C-RUN:
 - Created by compiler and debugger experts;
 - Fully integrated within IAR Embedded Workbench;
 - Insert target optimized test code directly during compilation;
 - Replace the C/C++ standard library with a dedicated library which contains special functionality for runtime error checking;
 - •Result in minimized ROM/RAM overhead and speed penalty.



Detecting integer overflow



<pre>{ int v1 = 0x7fffffff; unsigned int v2 = 0xfffffff; </pre>	 Insert checks for Integer overflow Including unsigned Integer conversion 		
<pre>v1++; /* signed integer overflow */ v2++; /* unsigned integer overflow */ }</pre>	Including a Integer shift ov Including u Division by zer Unhandled sw	explicit casts rerflow Insigned shifts o	
× Default action: Stop Filter:	Messages: 2		
Messages	Source File	PC	
→ A Signed integer overflow	main.c 6:3-6	0x000000E8	

		A Signed integer overflow	main.cb:3-b	0X00000E8
	┿╤┿	🛆 Unsigned integer overflow	main.c 7:3-6	0x00000114
	2	Result is greater than the largest representable number:		
		4294967295 (0xffffffff) + 1 (0x1).		
		Call Stack		
2	5	· main	main.c 7:3-7	
c c	5	[_call_main + 0x9]		

Detecting heap errors

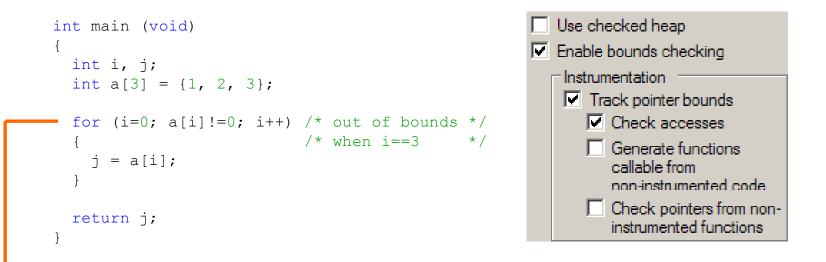




×	Default action: Stop 💌 Filter:	Messages: 1		
	Messages	Source File	PC	
	辛 🔺 Memory leak	main.c 12:3-21	0x00003B16	
	There were a total of 1 heap blocks with no references.			
Se	Heap block 0 at 0x00102450 has no references.			
Message	The block was allocated at line 6 of main.c.	main.c 6:13-22		
	🛄 🖂 Call Stack			
-RUN	main	main.c13:1-1		
풍	ⁱ [_main + 0x4]			

Detecting out-of-bounds





×	Defa	ault action: Stop 💌 Filter:	Messages: 1		
	Mes	sages	Source File	PC	
s B		Access out of bounds	main.c 6:13-16	0×000001E8	
-RUN Messag		Access outside pointer bounds:			
Ξ		Access 0x00101ff0 - 0x00101ff4			
S		Bounds 0x00101fe4 - 0x00101ff0, int a[3];	main.c 4:7-7		
L S	<u></u>	Call Stack			

Take full control of your development



