Technical Program
2019 International Conference on ReConFigurable Computing and FPGAs

	Monday, December 9
08:00 - 17:00	Registration
08:45 - 09:00	**Welcome**
09:00 - 10:10	**Keynote #1 "The future of Reconfigurable Computing: More than Meets the Eye" by Jose Alvarez, Intel** Session Chair: **David Andrews**
10:10 - 10:30	Short break & Group Photo
10:30 - 12:20	**Sesion M1: HPCS** Session Chair: **Ron DeMara**
10:30 - 11:00	Menbere Kina Tekleyohannes, Vladimir Rybalkin, Muhammad Mohsin Ghaffar, Norbert Wehn and Andreas Dengel. *iDocChip - A Configurable Hardware Architecture for Historical Document Image Processing: Text Line Extraction.*
11:00 - 11:30	Shanyuan Gao and Sen Ma. *The Impact of Adopting Computational Storage in Heterogeneous Computing Systems.*
11:30 - 12:00	Andrew Wilson and Michael Wirthlin. *Reconfigurable Real-Time Video Pipelines on SRAM-based FPGAs.*
12:00 - 12:10	Samah Rahamneh and Lina Sawalha. *Efficient OpenCL Accelerators for Canny Edge Detection Algorithm on a CPU-FPGA Platform.*
12:10 - 12:20	Andrei Hagiescu, Martin Langhammer, Bogdan Pasca, Philip Colangelo, Jason Thong and Niayesh Ilkhani. *BFLOAT MLP Training Accelerator for FPGAs.*
12:20 - 13:30	Lunch
13:30 - 15:20	**Session M2: Overlays, CGRAs, HLS** Session Chair: **Shanyuan Gao**
13:30 - 14:00	David Wilson and Greg Stitt. *Seiba: An FPGA Overlay-Based Approach to Rapid Application Development.*

14:00 - 14:30	Caleb Donovick, Makai Mann, Clark Barrett and Pat Hanrahan. *Agile SMT-Based Mapping for CGRAs with Restricted Routing Networks.*
14:30 - 15:00	Guilherme Korol, Michael Jordan, Raul Silveira Silva, Monica Magalhães Pereira, Marcelo Brandalero, Mateus Beck Rutzig and Antonio Carlos Schneider Beck. *A Runtime Power-Aware Phase Predictor for CGRAs.*
15:00 - 15:10	Wesley Stirk and Jeffrey Goeders. *Implementation and Design Space Exploration of a Turbo Decoder in High-Level Synthesis.*
15:10 - 15:20	Kevin Millar, Marcin Łukowiak and Stanislaw Radziszowski. *Design of a Flexible Schonhage-Strassen FFT Polynomial Multiplier with High-Level Synthesis to Accelerate HE in the Cloud.*
15:20 - 16:00	Coffee break
16:00 - 17:20	**Session M3: Systems** Session Chair: **Ali Akoglu**
16:00 - 16:30	Patrick Plagwitz, Franz-Josef Streit, Andreas Becher, Stefan Wildermann and Jürgen Teich. *Compiler-Based High-Level Synthesis of Application-Specific Processors on FPGAs.*
16:30 - 17:00	Carsten Heinz, Yannick Lavan, Jaco Hofmann and Andreas Koch. *A Catalog and In-Hardware Evaluation of Open-Source Drop-In Compatible RISC-V Softcore Processors.*
17:00 - 17:10	Habib Khan, Gökhan Akgün, Ariel Podlubne, Felix Wegener, Amir Moradi and Diana Göhringer. *Cycle-accurate Debugging of Multi-clock Reconfigurable Systems.*
17:10 - 17:20	Ariel Podlubne and Diana Goehringer. *FPGA-ROS: Methodology to Augment the Robot Operating System with FPGA Designs.*
19:00 - 21:00	**Welcome Cocktail & Demo Night**

	Tuesday, December 10
08:00 - 17:00	Registration
09:00 - 10:10	**Keynote #2 "Global-Scale FPGA-Accelerated Deep Learning Inference with Microsoft's Project Brainwave" by Gabriel Weisz, Microsoft** Session Chair: **Rene Cumplido**
10:10 - 10:30	Short break
10:30 - 12:20	**Session T1: AI and Machine Learning** Session Chair: **Ron Sass**
10:30 - 11:00	Ali Mirzaeian, Houman Homayoun and Avesta Sasan. *TCD-NPE: A Re-configurable and Efficient Neural Processing Engine, Powered by Novel Temporal-Carry-deferring MACs.*
11:00 - 11:30	Tatsuya Kaneko, Hiroshi Momose and Tetsuya Asai. *An FPGA Accelerator for Embedded Microcontrollers implementing a Ternarized Backpropagation Algorithm.*
11:30 - 12:00	Sina Boroumand and Philip Brisk. *Approximate Adder Tree Synthesis for FPGAs.*
12:00 - 12:10	Ryosuke Kuramochi, Masayuki Shimoda, Youki Sada, Shimpei Sato and Hiroki Nakahara. *FPGA-based Accurate Pedestrian Detection with Thermal Camera for Surveillance System.*
12:10 - 12:20	Abdelrahman Elkanishy, Derrick Rivera, Paul Furth, Abdel-Hameed A. Badawy, Youssef Aly and Christopher P. Michael. *FPGA-Accelerated Decision Tree Classifier for Real-Time Supervision of Bluetooth SoC.*
12:20 - 13:30	Lunch
13:30 - 15:20	**Session T2: Image and Pixel Processing** Session Chair: **Darshika Perera**
13:30 - 14:00	Ismael Antonio Dávila-Rodríguez, Marco Aurelio Nuño-Maganda, Yahir Hernández-Mier and Said Polanco-Martagón. *Decision-Tree Based Pixel Classification for Real-time Citrus Segmentation on FPGA.*
14:00 - 14:30	Atiyehsadat Panahi, Keaten Stokke and David Andrews. *A Library of FSM-based Floating-Point Arithmetic Functions on FPGAs.*
14:30 - 15:00	Corbin Thurlow, Hayden Rowberry and Mike Wirthlin. *TURTLE: A Low-Cost Fault Injection Platform for SRAM-based FPGAs.*
15:00 - 15:10	Tomáš Beneš, Matěj Bartík and Pavel Kubalík. *High Throughput and Low Latency LZ4 Compressor on FPGA.*

15:10 - 15:20	Siavash Rezaei, Eli Bozorgzadeh and Kanghee Kim. *UltraShare: FPGA-based Dynamic Accelerator Sharing and Allocation.*
15:20 - 16:00	**Coffee Break: Poster session**
16:00 - 17:20	**Session T3: Resource Optimizations** Session Chair: **Eli Bozorgzadeh**
16:00 - 16:30	Patrick Sittel, Nicolai Fiege, Martin Kumm and Peter Zipf. *Isomorphic Subgraph-based Problem Reduction for Resource Minimal Modulo Scheduling.*
16:30 - 17:00	Nils Voss, Stephen Girdlestone, Tobias Becker, Oskar Mencer, Wayne Luk and Georgi Gaydadjiev. *Low Area Overhead Custom Double Buffering for FFT.*
17:00 - 17:10	Ievgen Kabin, Alejandro Sosa, Zoya Dyka, Dan Klann and Peter Langendoerfer. *On the Influence of the FPGA Compiler Optimization Options on the Success of the Horizontal Attack.*
17:10 - 17:20	Regina Marcela Ivo and Daniel M. Muñoz. *RTRLib: A High-Level Modeling Tool for the Implementation of Dynamically Partial Reconfigurable System-on-Chips.*
19:45 - 22:30	**Banquet**

	Wednesday, December 11
08:00 - 12:00	Registration
09:00 - 10:10	**Keynote #3 "Security Challenges with Modern Reconfigurable Devices" by Tim Guneysu, Ruhr-University Bochum, Germany** Session Chair: **Marco Platzner**
10:10 - 10:30	Short break
10:30 - 12:20	**Session W1: Cryprography/Security** Session Chair: **Nele Mentens**
10:30 - 11:10	Sunwoong Kim, Keewoo Lee, Wonhee Cho, Jung Hee Cheon and Rob Rutenbar. *FPGA-based Accelerators of Fully Pipelined Modular Multipliers for Homomorphic Encryption.*
11:00 - 11:30	Joseph Gravellier, Jean-Max Dutertre, Yannick Teglia and Philippe Loubet Moundi. *High-Speed Ring-Oscillator based Sensors for Remote Side-Channel Attacks on FPGAs.*
11:30 - 12:00	Tolga Yalcin and Elif Bilge Kavun. *Almost-Zero Logic Implementation of Troika Hash Function on Reconfigurable Devices.*
12:00 - 12:10	Arkan Alkamil and Darshika G. Perera. *Efficient FPGA-Based Reconfigurable Accelerators for SIMON Cryptographic Algorithm on Embedded Platforms*.
12:10 - 12:20	Abubakr Abdulgadir, William Diehl and Jens-Peter Kaps. *An Open-Source Platform for Evaluation of Hardware Implementations of Lightweight Authenticated Ciphers.*
12:20 - 13:30	Lunch
13:30 - 14:30	**Session W2: Mixed Signal and Fault Injection** Session Chair: **Dirk Stroobandt**
13:30 - 14:00	Adrian Tatulian, Soheil Salehi and Ronald F. DeMara, *Mixed-Signal Spin/Charge Reconfigurable Array for Energy-Aware Compressive Signal Processing.*
14:00 - 14:30	Burak Unal, Md Sahil Hassan, Joshua Mack, Nirmal Kumbhare and Ali Akoglu. *Design of High Throughput FPGA Based Testbed for Accelerating Error Characterization of LDPC Codes.*
14:30 - 15:00	**Closing Remarks**

Poster Session
Abhi D.R., Ron Sass and Andrew Schmidt. *Volcan: System Integration of HLS and HMC on FPGAs.*
Muhamamd Mudussir Ayub, Habibullah Ahmadzay, Josef Eckmueller and Franz Kreupl. *Electronic System-Level Power and Performance Analysis for Multi-Processor-System-on-Chip.*
Tomohiro Kida, Yuichi Kawamata, Yuichiro Shibata and Kentaro Sano. *A High Level Synthesis Approach for Application Specific DMA Controllers.*
Elif Bilge Kavun, Nele Mentens, Jo Vliegen and Tolga Yalcin. *Efficient Utilization of DSPs and BRAMs Revisited: New AES-GCM Recipes on FPGAs.*
Michal Andrzejczak, Farnoud Farahmand and Kris Gaj. *Full-hardware implementation of the Post-Quantum Public Key Cryptography Scheme Round5.*
Cristian Urlea, Wim Vanderbauwhede and Syed Waqar Nabi. *Efficient FPGA Cost-Performance Space Exploration Using Type-driven Program Transformations.*
Beck Strohmer, Anders Bøgild, Anders Stengaard Sørensen and Leon Bonde Larsen. *ROS-Enabled Modular Hardware Framework for Experimental Robotics.*