SMC Standard SMC-S-010
12 April 2013

Supersedes:
SMC-S-010 (2009)

Air Force Space Command

SPACE AND MISSILE SYSTEMS CENTER STANDARD

TECHNICAL REQUIREMENTS FOR ELECTRONIC PARTS, MATERIALS, AND PROCESSES USED IN SPACE VEHICLES

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FOREWORD

1. This standard defines the Government's requirements and expectations for contractor performance in defense system acquisitions and technology developments.

2. This revised SMC standard comprises the text of The Aerospace Corporation report number TOR-2006(8583)-2336 REV B, dated March 6, 2013, entitled *Technical Requirements for Electronic Parts, Materials, and Processes Control Program Used In Space Vehicles.*

3. Beneficial comments (recommendations, changes, additions, deletions, etc.) and any pertinent data that may be of use in improving this standard should be forwarded to the following addressee using the Standardization Document Improvement Proposal appearing at the end of this document or by letter:

Division Chief, SMC/ENE
SPACE AND MISSILE SYSTEMS CENTER
Air Force Space Command
483 N. Aviation Blvd.
El Segundo, CA 90245

4. This standard has been approved for use on all Space and Missile Systems Center/Air Force Program Executive Office - Space development, acquisition, and sustainment contracts.

Mr. David Davis, GG-15, DAF
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Foreword

The requirements of this document were developed for the successful operations of long mission life and/or high reliability space equipment. Attention to every detail is required at every level of assembly throughout development, manufacture, qualification, and testing, starting with the parts, materials, and processes used. Launch vehicle program requirements for PMP are detailed in SMC-S-011 Revision B - Parts, Materials and Processes Control Program for Expendable Launch Vehicles, while experimental/demonstration programs may choose to tailor this document to better align with the programs' objectives and missions.

This document supersedes Aerospace Technical Operating Report TOR-2006(8583)-5236 Revision A, titled Technical Requirements for Electronics Parts, Materials, and Processes Used in Space and Launch Vehicles, and shall be used for all space program PMP procurements.

The objective of this document is to specify the technical baseline in the selection, application, procurement, control and standardization of parts (electrical and mechanical), materials, and processes for space programs. This TOR is intended to be used in conjunction with TOR-2006(8583)-5235 (Parts, Materials, and Processes Control Program for Space) in order to achieve a high reliability space vehicle.

Every effort was made to utilize standard document format, but this document retains the separately called out technical sections (starting with Section 100) to focus the user industry on the unique space quality items that are paramount for mission success in each technical section.

The Referenced Documents Section includes active, inactive, or canceled specifications and standards. When no superseding document is called out, or the superseding document is believed not to include the necessary requirements, then the inactive or canceled specification is listed with the last known revision letter and annotated as either inactive or canceled. When the Acquisition Activity agrees to the use of superseding documents not specifically called out in Section 2, the prime contractor shall be responsible for the continued support to industry organizations responsible for publishing and maintaining the documents, and for active participation in the review and coordination of changes, that occur after contract award, to ensure continued compliance to the original intents of the referenced inactive/canceled documents.

NOTE: Aerospace TOR-2006(8583)-5235 Rev B [PMP Control Plan] is also published as SMC-S-009 (2013).

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1. Scope

1.1 Purpose.

This document establishes the minimum technical requirements for electronic parts, materials, and processes (electronic PMP) used in the design, development, and fabrication of space vehicles. Application information, design and construction information, and quality assurance provisions are provided herein. All electronic PMP selected for use in space vehicles shall meet the requirements specified herein, unless otherwise approved by the program. Either the contractor or its subcontractors may accomplish these requirements. However, the prime contractor has the responsibility for ensuring all requirements are met.

1.2 Baseline Performance.

This document establishes the baseline performance requirements for electronic PMP and the quality and reliability assurance requirements, which shall be met for their acquisition. Detailed requirements, specific characteristics of electronic PMP, and other provisions which are sensitive to the particular intended use shall be specified within the device specification.

1.3 Quality. Quality assurance requirements outlined herein are for all electronic PMP built or performed on a manufacturing line that is controlled through a manufacturer's Quality Management (QM). Several levels of product assurance including Radiation Hardness Assurance (RHA) are provided for in this specification.

1.4 Order of Precedence. In the event of conflict between the text of this document and the references cited herein (except for device specifications), the text of this document shall take precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1.5 Application of the Document. This document is intended for use in acquisition of space vehicles. This document should be cited in the contract statement of work and may be tailored by the acquisition activity for the specific application or program.

1.6 PMP Management. Implementation and changes, or modifications to the requirements of this document shall be accomplished in accordance with TOR-2006(8583)-5235 (Parts, Materials, and Processes Control Program for Space Vehicles), the provisions and authority of the PMP Management, and the requirements of the program.

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2. Reference Documents

2.1 Reference Documents

2.1.1 Government Documents. Unless otherwise specified, the following specifications, standards, and handbooks of the issue listed in the current version of the Department of Defense Index of Specifications and Standards (DoDISS) specified in the solicitation form a part of this document to the extent specified herein.

2.1.1.1 Military Specifications

MIL-W-22759E(2)	Wire, Electric, Fluoropolymer-Insulated, Copper or Copper Alloy (CANCELED)
MIL-DTL-17	Cables, Radio Frequency, Flexible and Semirigid, General Specification for
MIL-PRF-27	Transformers and Inductors (Audio, Power, and High Power Pulse), General Specification for
MIL-C-50D	Copper Alloy Number 260 (Cartridge Brass, 70 Percent); Sheet, Strip, Plate, Bar, and Discs (CANCELED)
MIL-PRF-123	Capacitors, Fixed, Ceramic Dielectric, (Temperature Stable and General Purpose), High Reliability, General Specification for
MIL-PRF-3098	Crystal Units, Quartz, General Specification For
MIL-DTL-5015	Connector, Electrical, Circular Threaded, AN Type, General Specification for
MIL-H-6088G(1)	Heat Treatment of Aluminum Alloys (CANCELED)
MIL-PRF-6106	Relays, Electromagnetic, General Specification for
MIL-H-6875H	Heat Treatment of Steels, Process for (CANCELED)
MIL-C-7438	Core Material, Aluminum, For Sandwich Construction
MIL-S-7742D(1)	Screw Threads, Standard, Optimum Selected Series, General Specification for (INACTIVE)
MIL-B-7883B	Brazing of Steels, Copper, Copper Alloys, Nickel Alloys, Aluminum and Aluminum Alloys (CANCELED)
MIL-PRF-8805	Switches and Switch Assemblies, Sensitive and Push (Snap Action), Basic, Limit, Push Button and Toggle Switches, General Specification for
MIL-W-8939A	Welding, Resistance, Electronic Circuit Modules (CANCELED)
MIL-T-9047G(1)	Titanium and Titanium Alloy Bars (Rolled or Forged) and Reforging, Forging Stock Aircraft Quality (CANCELED)
MIL-DTL-9395	Switches, Pressure, (Absolute, Gage and Differential), General Specification for
MIL-PRF-15305	Coil, Fixed and Variable, Radio Frequency, General Specification for
MIL-PRF-19500	Semiconductor Devices, General Specification for
MIL-PRF-21038	Transformer, Pulse, Low Power, General Specification for
MIL- A-21180D(1)	Aluminum-Alloy Castings, High Strength (CANCELED)
MIL-PRF-23269	Capacitors, Fixed, Glass Dielectric, Established Reliability, General Specification for
MIL-PRF-23419	Fuse Cartridge, Instrument Type, General Specification for
MIL-PRF-23648	Resistors Thermal (Thermistor), Insulated, General Specification for
MIL-PRF-24236	Switches, Thermostatic, (Metallic And Bimetallic), General Specification for
MIL-DTL-24308	Connector, Electrical, Rectangular, Non-environmental Miniature Polarized Shell, Rack and Panel, General Specification for

MIL-DTL-26074F	Coatings, Electroless Nickel Requirements for (CANCELED)
MIL-DTL-26482	Connectors, Electrical, (Circular, Miniature, Quick Disconnect, Environment Resisting, Receptacles and Plugs, General Specification for
MIL-DTL-27500H(1) NOT 1	Cable, Power, Electrical and Cable Special Purpose, Electrical Shielded and Unshielded, General Specification For (CANCELED)
MIL-C-28754	Connectors, Electrical, Modular, and Component Parts General Specification for
MIL-PRF-28861	Filters and Capacitors, Radio Frequency/Electromagnetic Interference Suppression, General Specification for
MIL-PRF-31031	Connectors, Electrical, Plugs and Receptacles, Coaxial, Radio Frequency, High Reliability, for Flexible and Semirigid Cables, General Specification for
MIL-PRF-31032	Printed Circuit Board/ Printed Wiring Board, General Specification for
MIL-DTL-32139	Connectors, Electrical, Rectangular, Nanominiature, Single Row, Plug, Polarized Shell, Pin Contacts, Crimp Type, General Specification for
MIL-PRF-32159	Resistors, Chip, Fixed, Film, Zero Ohm, Industrial, High Reliability, Space Level, General Specification for
MIL-PRF-38534	Hybrid Microcircuits, General Specification for
MIL-PRF-38535	Integrated Circuits (Microcircuits) Manufacturing, General Specification for
MIL-DTL-38999	Connector, Electrical, Circular, Miniature, High Density, Quick Disconnect (Bayonet, Threaded, and Breach Coupling), Environment Resistant, Removable Crimp and Hermetic Solder Contacts, General Specification for
MIL-PRF-39003	Capacitors, Fixed, Electrolytic (Solid Electrolyte), Tantalum, Established Reliability, General Specification for
MIL-PRF-39005	Resistor, Fixed, Wirewound, (Accurate), Non-established and Established Reliability, General Specification for
MIL-PRF-39006	Capacitors, Fixed, Electrolytic (Nonsolid Electrolyte), Tantalum, Established Reliability, General Specification for
MIL-PRF-39007	Resistor, Fixed, Wirewound (Power Type), Non-established Reliability, Established Reliability and Space Level, General Specification for
MIL-R-39008	Resistor, Fixed, Composition (Insulated), Established Reliability, General Specification for
MIL-PRF-39009	Resistor, Fixed, Wirewound (Power Type, Chassis Mounted), Non-established Reliability, Established Reliability, General Specification for
MIL-PRF-39010	Coil, Fixed, Radio Frequency, Molded, Established Reliability and Non-established Reliability, General Specification for
MIL-PRF-39012	Connectors, Coaxial, Radio Frequency, General Specification for
MIL-PRF-39015	Resistors, Variable, Wirewound (Lead Screw Actuated), Non-established Reliability and Established Reliability, General Specification for
MIL-PRF-39016	Relays, Electromagnetic, Established Reliability, General Specification for
MIL-PRF-39017	Resistor, Fixed Film, (Insulated) Non-established Reliability and Established Reliability, General Specification for
MIL-PRF-39035	Resistor, Variable, Non-wirewound (Adjustment Type), Non-established and Established Reliability, General Specification for
MIL-PRF-32192	Resistors, Chip, Thermal (Thermistor), General Specification for
MIL-DTL-45204	Gold Plating, Electrodeposited
MIL-I-46058C(7)	Insulating Compound, Electrical (for Coating Printed Circuit Assemblies) (INACTIVE)
MIL-S-46106	Adhesive-Sealants, Silicone, RTV, One-Component

MIL-A-46146	Adhesive Sealants, Silicone, RTV, Non-corrosive (For Use With Sensitive Metals and Equipment)
MIL-PRF-49142	Connector, Triaxial, Radio Frequency General Specification for
MIL-PRF-49467	Capacitors, Fixed, Ceramic, Multilayer, High Voltage, (General Purpose), Established Reliability, General Specification for
MIL-C-49468(1)	Crystal Units, Quartz, Precision, General Specification for (CANCELED)
MIL-PRF-49470	Capacitor, Fixed, Ceramic Dielectric, Switch Mode Power Supply (General Purpose and Temperature Stable), Standard Reliability and High Reliability, General Specification for
MIL-P-50884D(2)	Printed Wiring, Flexible, or Rigid-Flex, General Specification for (INACTIVE)
MIL-PRF-55110G	Printed Wiring Boards, General Specification for (INACTIVE)
MIL-PRF-55182	Resistors, Fixed, Film, Non-Established Reliability, Established Reliability, and Space Level, General Specification for
MIL-DTL-55302	Connector, Printed Circuit Subassembly and Accessories
MIL-PRF-55310	Oscillator, Crystal Controlled, General Specification For
MIL-PRF-55339	Adapters, Connectors, Coaxial, Radio Frequency, (Between Series and within Series), General Specification for
MIL-PRF-55342	Resistor, Chip, Fixed, Film, Established Reliability, General Specification for
MIL-PRF-55365	Capacitor, Electrolytic Fixed Tantalum, Established Reliability and Non-established Reliability, General Specification for
MIL-T-55631(2)	Transformer, Intermediate Frequency, Radio Frequency, and Discriminator, General specification for (INACTIVE)
MIL-DTL-81381	Wire, Electric, Polyimide-Insulated, Copper or Copper Alloy
MIL-T-81556	Titanium and Titanium Alloys, Extruded Bars, and Shapes Aircraft Quality
MIL-PRF-81705	Barrier Materials, Flexible, Electrostatic Discharge Protective, Heat-Sealable
MIL-P-81728A	Plating, Tin-Lead, Electrodeposited (CANCELED)
MIL-F-83142A(4)	Forging, Titanium Alloys, For Aircraft and Aerospace Applications (INACTIVE)
MIL-PRF-83401	Resistor Networks, Fixed, Film and Capacitor-Resistor Networks, Ceramic Capacitor and Fixed, Film, Resistors, General Specification for
MIL-PRF-83421	Capacitors, Fixed, Metallized, Plastic Film Dielectric, (DC, AC, or DC and AC), Hermetically Sealed in Metal Cases, or Ceramics Cases, Established Reliability, General Specification for
MIL-PRF-83446	Coils, Radio Frequency, Chip, Fixed or Variable, General Specification for
MIL-DTL-83513	Connectors, Electrical, Rectangular, Microminiature, Polarized Shell, General Specification for
MIL-PRF-83536	Relays, Electromagnetic, Established Reliability, 25 Amperes and Below, General Specification for
MIL-A-83577B	Assemblies, Moving Mechanical, for Space and Launch Vehicles, General Specification for (CANCELED)
MIL-DTL-83723	Connector, Electrical, (Circular, Environment Resisting), Receptacle and Plugs, General Specification for
MIL-PRF-83726	Relays, Hybrid and Solid-state, Time Delay, General Specification for

MIL-DTL-83733	Connector, Electrical, Miniature, Rectangular Type, Rack to Panel, Environment Resisting, 200°C Total Continuous Operating Temperature, General Specification for
MIL-PRF-87164A(3)	Capacitors, Fixed, Mica Dielectric, High Reliability, General Specification for (CANCELED)
MIL-PRF-87217A	Capacitors, Fixed, Supermetallized Plastic Film Dielectric, Direct Current for Low Energy, High Impedance Applications, Hermetically Sealed in Metal Cases, High Reliability, General Specification for (CANCELED)

2.1.1.2 Federal Standards

FED-STD-101C	Test Procedures for Packaging Materials (CANCELED)
FED-STD-209E	Airborne Particulate Cleanliness Classes in Clean Rooms and Clean Zones (CANCELED)
A-A-59126	Terminals, Feedthru (Insulated) and Terminals, Stud (insulated and Non-insulated)
QQ-P-35C	Passivation Treatments For Corrosion-Resistant Steel (CANCELED)
QQ-N-290A	Nickel Plating, Electrodeposited (CANCELED)
QQ-B-613D	Brass, Leaded And Nonleaded: Flat Products (Plate, Bar, Sheet, And Strip) (CANCELED)

2.1.1.3 Military Standards

MIL-HDBK-5J	Metallic Materials and Elements for Aerospace Vehicle Structures (CANCELED)
MIL-HDBK-17	Composite Materials Handbook (Volumes 1 through 5)
MIL-HDBK-23A(3)	Structural Sandwich Composites (CANCELED)
MIL-STD-130	Identification Marking of U.S. Military Property
MIL-HDBK-198	Capacitor, Selection and Use of
MIL-STD-199E	Resistors, Selection and Use of (CANCELED)
MIL-STD-202	Test Method Standard, Electronic and Electrical Component Parts
MIL-HDBK-217	Reliability Prediction of Electronic Equipment
MIL-HDBK-263	Electrostatic Discharge Control Handbook for Protection of Electrical and Electronic Parts, Assemblies, and Equipment (Excluding Electrically Initiated Explosive Devices)
MIL-HDBK-339	Custom Large Scale Integrated Circuit Development and Acquisition for Space Vehicles
MIL-STD-403C	Preparation for and Installation of Rivets and Screws, Rocket and Missile Structures (INACTIVE)
MIL-HDBK-454	General Guidelines for Electronic Equipment
MIL-STD-750	Test Method Standard for Semiconductor Devices

MIL-HDBK-814	Ionizing Dose and Neutron Hardness Assurance Guidelines for Microcircuits and Semiconductor Devices
MIL-HDBK-815	Dose Rate Hardness Assurance Guidelines
MIL-STD-866	Grinding of Chrome Plated Steel and Steel Parts Heat Treated to 180,000 psi or Over
MIL-STD-883	Test Methods and Procedures for Microelectronics
MIL-STD-889	Dissimilar Metals
MIL-STD-975M	NASA Standard Electrical, Electronic, and Electromechanical (EEE) Parts List (CANCELED)
MIL-STD-981	Design, Manufacturing, and Quality Standards for Custom Electromagnetic Devices for Space Applications
MIL-STD-1276	Leads for Electronic Component Parts
MIL-HDBK-1331	Parameters To Be Controlled for the Specification of Microcircuits, Handbook for
MIL-STD-1346C	Relays, Selection and Application of (CANCELED)
MIL-STD-1353B(4)	Electrical Connectors Plug-in Sockets and Associated Hardware, Selection and Use of (CANCELED)
MIL-STD-1580	Department of Defense Test Methods Standard, Destructive Physical Analysis for Electrical, Electronic, and Electromagnetic Parts
MIL-STD-1686	Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices)
MIL-STD-1835	Electronic Component Case Outlines
MIL-STD-2154(1)	Inspection, Ultrasonic, Wrought Metals, Process for (CANCELED)
MIL-STD-2175A	Castings, Classification and Inspection of (CANCELED)
MIL-STD-2219	Fusion Welding for Aerospace Applications
MIL-STD-3010	Test Procedures for Packaging Materials
MIL-HDBK-83377	Adhesive Bonding (Structural) for Aerospace and Other Systems, Requirements For
MIL-HDBK-83575	General Handbook for Space Vehicle Wiring Harness Design and Testing

2.1.1.4 Air Force Wright Aeronautical Laboratories (AFWAL)

ADD436124L	DOD/NASA Structural Composites Fabrication Guide Volume I
ADD436125L	DOD/NASA Structural Composites Fabrication Guide Volume II DOD/NASA Advanced Composite Design Guide, Volumes I – IV

2.1.1.5 NASA Publications

GSFC S-311-P-4	Connectors (and Contacts), Electrical, Rectangular, for Space Flight Use, General Specification for
GSFC S-311-P-822	Connectors, PWB, 2 mm cPCI™ Style, High Reliability, General Requirements for
MSFC 40M38277	Marshall Space Flight Connectors
MSFC 40M38298	Marshall Space Flight Connectors
MSFC 40M39569	Marshall Space Flight Connectors and Hardware
JSC-SP-R-0022A	General Specifications, Vacuum Stability Requirements of Polymeric Materials for Spacecraft Applications
MSFC-SPEC-250	Protective Finishes for Space Flight Vehicle Structures and Associate Flight Equipment, General Specification for
MSFC-STD-355	Radiographic Inspection of Electronic Parts
MSFC-SPEC-469	Titanium and Titanium Alloys, Heat Treatment of
MSFC-SPEC-522	Design Criteria for Controlling Stress Corrosion Cracking
MSFC-STD-3029	Guidelines for the Selection of Metallic Materials for Stress Corrosion Cracking Resistance in Sodium Chloride Environments
NASA-SP-8063	Lubrication, Friction, and Wear
NASA-STD-8739.1	Workmanship Standard for Staking and Conformal Coating of Printed Wiring Boards and Electronic Assemblies (CANCELED)
NASA-STD-8739.2	Workmanship Standard for Surface Mount Technology (CANCELED)
NASA-STD-8739.3	Soldered Electrical Connections
NASA-STD-8739.4	Crimping, Interconnecting Cables, Harnesses, and Wiring
NASA TM X-64755	Guidelines for the Selection and Application of Tantalum Electrolytic Capacitors In Highly Reliable Equipment
SSQ-21635	Connectors And Accessories, Electrical, Circular, Miniature, IVA/EVA Compatible, Space Quality, General Specification for

(Application for copies should be addressed to: Marshall Space Flight Center/ Document Repository (AS24D), Huntsville, AL 35812)

NASA Documents can be obtained via www.nepp.nasa.gov

Copies of specifications, standards, handbooks, drawings, and publications required by contractors in connection with specified acquisition functions should be obtained from the contracting activity or as directed by the contracting officer.

2.1.1.6 DLA/Land and Maritime (DSCC)

DSCC 94007	Connector, Electrical, Coaxial, Radio Frequency, Shroud 2 Hole Pin and Adapter, Electrical, Coaxial, RF, Socket Contact, Series SMP to SMP
DSCC 94008	Connector, Electrical, Coaxial, Radio Frequency, Socket Contact Series SMP for .047 and .086 Semirigid Cable

DLA/Land and Maritime (DSCC) documents can be obtained at:

http://www.dscc.dla.mil/programs/MilSpec/ or https://assist.dla.mil/online/start/

2.1.2 Non-Government Documents.

The following documents form a part of this document to the extent specified herein. Unless otherwise indicated, the issue in effect on the date of release of this document shall serve as the applicable revision for all listed non-government specifications/standards.

2.1.2.1 Aerospace TOR

TOR-2006(8583)-5235	Parts, Materials, and Processes Control Program for Space Vehicles

(Application for copies should be addressed to: The Aerospace Corporation, Library, Circulation Desk, P.O. Box 92957, M1-199, Los Angeles, CA 90009-2957)

2.1.2.2 American Society for Testing Material

ASTM-B-211	Aluminum and Aluminum-Alloy Bar, Rod, and Wire
ASTM-B-221	Aluminum And Aluminum-Alloy Extruded Bars, Rods, Wire, Profiles, And Tubes
ASTM-B-322	Metals cleaning, prior to electroplating
ASTM-B-488	Gold for Engineering Uses, Electrodeposited Coatings of
ASTM-B-571	Coating, Metallic, Qualitative Adhesion Testing of
ASTM-B-733	Metal, Autocatalytic Electroless Nickel-Phosphorus Coatings On
ASTM-D-257	Resistance DC or Conductance of Insulating Materials
ASTM-D-903-98	Adhesive Bonds, Peel or Stripping Strength of
ASTM-D-1000	Tapes Pressure-Sensitive Adhesive-Coated Used For Electrical And Electronic Applications
ASTM-E-595	Standard Test Method for Total Mass Loss and Collected Volatile Condensable Material From Outgassing in a Vacuum Environment

(Application for copies should be addressed to: American Society for Testing Materials, 1916 Race Street, Philadelphia, PA 19111, www.astm.org)

2.1.2.3 Electronics Industries Association

EIA-455	Fiber Optic Fibers, Cables, Transducers, Sensors, Connecting and Terminating Devices, and Other Fiber Optic Components
EIA-477	Cultured Quartz
EIA-557	Statistical Process Control Systems

(Application for copies should be addressed to: Electronic Industries Association, 2001 Pennsylvania Ave, N.W., Washington, D.C. 20006 www.eia.org)

2.1.2.4 International Electrotechnical Commission

CEI/IEC 60410	Sampling Plans And Procedures For Inspection By Attributes
CEI/IEC 60758 Ed. 3 Third edition	International Electrotechnical Commission: Synthetic Quartz Crystal – Specification And Guide To The Use

(Application for copies should be addressed to: American National Standards Industries, 1430 Broadway, New York, NY 10018 www.ansi.org)

2.1.2.5 IPC – Association Connecting Electronic Industries

IPC-SM-840	Qualification and Performance of Permanent Polymer Coating (Solder Mask) for Printed Boards
IPC-CC-830	Qualification and Performance of Electrical Insulation Compound for Printed Wiring Assemblies
IPC-TM-650	Test Methods Manual
IPC-CF-152	Composite Metallic Material Specification for Printed Wiring Boards
J-STD-033	Handling, Packaging, Shipping and Use of Moisture/Reflow Sensitive Surface Mounted Devices
J-STD-020	Moisture/Reflow Sensitivity Classification of Plastic Surface Mount Devices
J-STD-006	Requirements for Electronic Grade Solder Alloys and Fluxed and Non-Fluxed Solid Solders for Electronic Soldering Applications
J-STD-002	Solderability Tests for Component Leads, Terminations, Lugs Terminals and Wires
J-STD-001ES	Requirements for Soldered Electrical and Electronic Assemblies
IPC 2221	Generic Standard for Printed Board Design
IPC 2222	Sectional Design Standard for Rigid Organic Printed Boards
IPC 2223	Sectional Design Standard for Flexible Printed Boards
IPC 2252	Design Guide for RF/Microwave Circuit Boards

IPC 4101	Specification for Base Materials for Rigid and Multilayer Printed Boards
IPC 4103	Specification for Base Materials for High Speed/ Frequency Applications
IPC 4202	Flexible Base Dielectric for Use in Flexible Printed Circuitry
IPC 4203	Adhesive Coated Dielectric Films for Use as Cover Sheets for Flexible Printed Circuitry and Flexible Bonding Films
IPC 4204	Flexible Metal Clad Dielectric for Use in Fabrication of Flexible Printed Circuitry
IPC 6012	Qualification and Performance Specification for Rigid Printed Boards
IPC 6013	Qualification and Performance Specification for Flexible Printed Boards
IPC 6018	Microwave End Product Board Inspection and Test

(Application for copies should be addressed to: IPC – 3000 Lakeside Drive, 309 S. Bannockburn, IL 60015) www.ipc.org)

2.1.2.6 National Aerospace Standards

NASM 1312	Fastener, Test Methods
NASM 1515	Fastener Systems for Aerospace Applications

www.nasm.org

2.1.2.7 Society of Automotive Engineers

SAE-AMS-QQ-P-35	Passivation Treatments For Corrosion-Resistant Steel
SAE-AMS-QQ-N-290	Nickel Plating, Electrodeposited
SAE-AMS-QQ-A-367	Aluminum Alloy Forgings
SAE-AMS-STD-1595	Qualification of Aircraft, Missile and Aerospace Fusion Welders
SAE-AS-1933	Hose Containing Age-Sensitive Elastomeric Material, Age Controls for
SAE-AMS-2404	Nickel, Electroless, Plating
SAE-AMS-2418	Copper Plating
SAE-ARP-5316	Seals Assemblies Which Include An Elastomer Element Prior To Hardware Assembly, Storage of Elastomer Seals and
SAE-AMS-F-7190	Forging, Steel, for Aircraft/Aerospace Equipment and Special Ordnance Applications
SAE-AS-8879	Screw Threads, UNJ Profile inch controlled Radius Root With Increased Minor Diameter, General Specification for
SAE-AMS-T-9046	Titanium and Titanium Alloy, Sheet, Strip and Plate

SAE-AMS-S-13165	Shot Peening of Metal Parts
SAE-AMS-A-22771	Aluminum. Alloy Forgings, Heat Treated
SAE-AMS-C-26074	Coatings, Electroless Nickel, Requirements for
SAE-AS-39029	Contacts, Electrical Connector, General Specification For
SAE-AMS-H-81200	Heat Treatment of Titanium and Titanium Alloys
SAE-AS-81703	Connectors, Electric, Circular, Miniature, Rack and Panel or Push-Pull Coupling, Environment Resisting
SAE-AMS-P-81728	Plating, Tin-Lead, Electrodeposited
SAE-AS-85049	Connector Accessories, Electrical, General Specification For

2.1.2.8 ASME/ANSI/IEEE

ANSI/IEEE 176-1987	IEEE Standard on Piezoelectricity
ASME/ANSI B18.18.1M	Inspection and Quality Assurance for General Purpose Fasteners
ANSI/EOS/ESD S11.11-1993	Surface Resistance Measurements of Static Dissipative Planar Materials
AWS-C3.4	Torch Brazing
AWS-C3.5	Induction Brazing
AWS-C3.6	Furnace Brazing
AWS-C3.7	Aluminum Brazing

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3. Definitions

The following definitions describe terms used throughout this document.

Acquisition Activity	The acquisition activity is the Government office or contractor procuring the equipment, system, or subsystem for which this document is being contractually applied.
Case Temperature	The case temperature is the hottest temperature on the external surface of the device's package, and for Surface Mount Devices (SMD), the external surface is the case.
Contracting Officer	A contracting officer is a person with the authority to enter into, administer, or terminate contracts and make related determinations and findings. The term includes authorized representatives of the contracting officer acting within the limits of their authority as delegated by the contracting officer.
COTS Parts and Materials	Commercial-Off-The-Shelf (COTS) parts and materials are those that (a) have been developed and produced to commercial designs and specifications, (b) are readily available from a manufacturer as a catalog item and without additional testing, (c) are typically intended for consumer electronics, and (d) are controlled solely by the supplier of the item.
Derating	Derating of a part is the intentional reduction of its applied stress, with respect to its rated stress, for the purpose of providing a margin between the applied stress and the demonstrated limit of the part's capabilities. Maintaining this derating margin reduces the occurrence of stress-related failures and helps ensure the part's reliability.
Destructive Physical Analysis (DPA)	A Destructive Physical Analysis (DPA) is a systematic, logical, detailed examination of parts during various stages of disassembly, conducted on a sample of completed parts from a given lot, wherein parts are examined for a wide variety of design, workmanship, and processing problems that may not show up during normal screening tests. The purpose of these analyses is to maintain configuration control and determine those lots of parts, delivered by a vendor, which have anomalies or defects such that they could, at some later date, cause degradation or catastrophic failure of a system.
Defect	A defect is any nonconformance from specified requirements which affects form, fit, function, or the long-term life/reliability performance of the part or material.
Electronic Parts	The term "electronic" is used in a broad sense in this document and includes electrical, electromagnetic, electromechanical, and electro-optical (EEEE) devices. Connectors are also classified as electronic parts.
End-of-Life Design Limit	The end-of-life design limits for an item are the expected variations in its electrical parameters over its period of use in its design environment. The parameter variations are expressed as a percentage change beyond the specified minimum and maximum values.
Hot-Welded Can	A Hot-Welded Can is a cap sealed component utilizing thermocompression attachment of the cap to the base of the device. The bond is a brazed attachment of the nickel-plated cap to the nickel-plated base, with nickel acting as a brazing agent.
Inspection Lot	Unless otherwise specified in the applicable detailed military specification, an inspection lot is defined as a group of parts of the same design, the same part number, manufactured on the same product line using the same materials, processes and equipment, of the same date code submitted for inspection at one time.
Kirkendall Voids	Intermetallic growth results from the diffusion of one material into another via crystal vacancies made available by defects, contamination, impurities, grain boundaries and mechanical stress. Diffusion rates vary with different materials. For example, the diffusion rate of Au into Al is different than that for Al into Au. These rates are a function of temperature. If one material overwhelms the other in volume, and diffusion occurs rapidly enough, the minority material can appear to have been completely "consumed" by the majority material. Rapid diffusion of one material into another can cause crystal vacancies to form in the bulk material. These vacancies attract each other which results in the creation of voids. These voids are called Kirkendall voids. Excessive Kirkendall voids can result in out-of-tolerance wire bond resistance and weakened wire bonds.

Lot Date Code	The Lot Date code is defined in the applicable space level Military Specification for the individual commodity or its nearest equivalent. For example, hermetic microcircuit devices are marked with a unique code to identify the period in which devices were sealed. The first two numbers in the code are the last two digits of the current year, while the last two numbers of the code are the calendar week of the year.
Manufacturing Baseline	EEEE part manufacturers establish and maintain a manufacturing baseline. This baseline describes all the manufacturing operations/steps, facilities, equipment and processes necessary to produce the deliverable item. Each step is documented and identified by a title, document number, revision level and date. Any processing, inspections, or tests performed at an outside facility are documented in the manufacturing baseline. All testing, inspections and post assembly processing are also documented on a manufacturer's lot traveler.
Material	Material is a metallic or nonmetallic element, alloy, mixture, or compound used in a manufacturing operation and which becomes either a permanent portion of a manufactured item, or which can leave a remnant, residue, coating, or other material that becomes or affects a permanent portion of a manufactured item. Environmental materials (e.g., moisture or oxygen in the air, etc.) and those used in tooling or equipment not intended to modify or leave residues are not meant to be covered by this definition.
Material Lot	A material lot refers to material produced as a single batch or in a single continuous operation or production cycle, come from the same production lots of raw materials, and offered for acceptance at any one time.
New Technology PMP	New technology PMP is a part, material or process which (a) has never been previously characterized or qualified for the particular space/mission environment, (b) has limited space heritage, (c) is a commercial (COTS) technology, including PEMS, or (d) PMP that has recently undergone major changes in the element selection, process, assembly, manufacturing (including facility change) or testing, and fits the description as written in Appendix D of Aerospace TOR-2006(8583)-5235.
Part	A part is one piece, or two or more pieces joined together, which are not normally subjected to disassembly without destruction or impairment of its designed use.
Parts, Materials and Processes Control Board (PMPCB)	The PMPCB is a formal contractor organization established by contract to manage and control the selection, application, procurement, qualification, and inspection of parts, materials, and processes used in equipment, systems, or subsystems supplied to the Acquisition Activity in accordance with TOR-2006(8583)-5235.
Percent Defective Allowable (PDA)	The percent defective allowable (PDA) of a production lot of parts or materials is the maximum allowable percentage of parts or materials specimens that fail to pass one or more tests before the entire production lot is considered to be unacceptable.
Process	A process is an operation, treatment, or procedure used during fabrication of parts, sub-assemblies and/or assemblies that modifies an existing configuration or creates a new configuration that alters the form/fit/function and/or changes the physical and/or the mechanical properties of the parent material.
Production Lot	Unless otherwise specified in the detail specification, a production lot of parts refers to a group of parts of a single part type; defined by a single design and part number; produced in a single production run by means of the same production processes, the same tools and machinery, same raw material, the same manufacturing and quality controls, and to the same baseline document revisions; and tested within the same period of time. All parts in the same lot have the same lot date code, batch number, or equivalent identification.
Prohibited Parts, Materials and Processes	Prohibited PMP are those items that do not meet PMP technical requirements under any circumstances.

Radiation Hardness Assurance (RHA)	Radiation hardness assurance (RHA) is an integral component of system design to assure the operational/survival capabilities of the system in the specified orbit or radiation environment. Appendix A herein prescribes the preferred methodology for carrying out the specified RHA tasks. Through the process of operability/survivability allocation analysis, it is determined which radiation environments are both operational/survival and which are survival only. This analysis and allocation process results in a flow down of operational/survival requirements down to the box, circuit and piece-part level.
Registered (Reliability Suspect) Parts, Materials and Processes	A registered (reliability suspect) PMP is a part, material, or process, which is registered with the PMPCB to call attention to special reliability, quality, or other concerns, relating to its procurement or application. Registered PMP includes, but is not limited to, reliability suspect PMP, limited application PMP, and PMP involving restricted or special controlled usage, storage, or handling due to safety or environmental concerns.

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4. General Requirements

4.1 Application Requirements

4.1.1 Electrical Derating.

Circuits shall be designed with the parts derated as specified herein, or to an equivalent derating plan which shall be technically justified, as a minimum, with Part Stress Analysis (PSA) and Worst-Case Analysis (WCA) to support the required mission duration and shall be approved by the PMPCB. The extent to which electrical stress (e.g., voltage, current, or power) is derated is dependent upon temperature. The general interrelationship between electrical stress and temperature is shown in Figure 4-1. The approved flight operating conditions lie within the area below the nominal limitation line (ES_{NOM}). The worst-case limits also apply to flight conditions. MIL-STD-975M (CANCELED) derating requirements may be used to justify applications between ES_{NOM} and ES_{WC}.

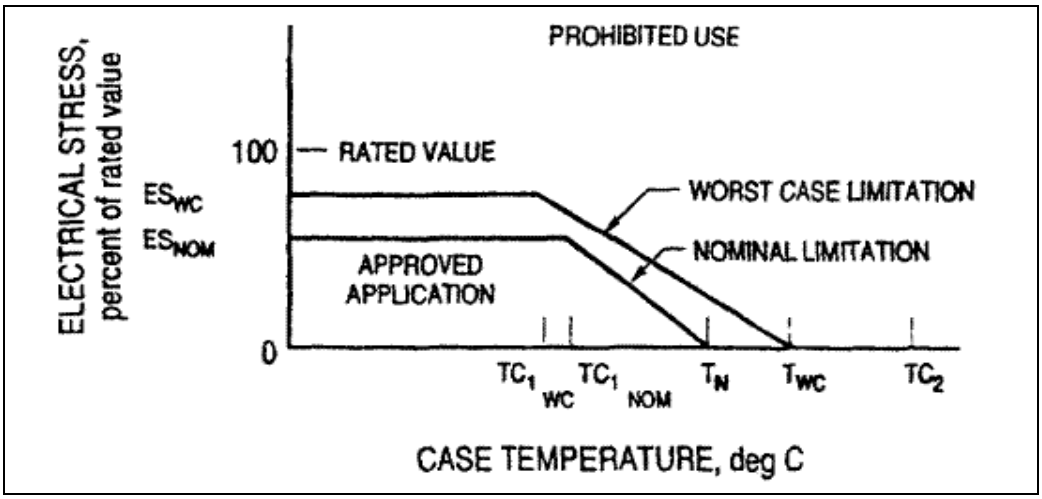

Figure 4-1. Typical electrical stress vs temperature derating scheme.

TC_1	Case temperature above which applied electrical stress should be reduced. Unless otherwise specified, TC_1 for worst case is the same as TC_1 for nominal.
TC_2	Maximum allowable case temperature per detailed specification
T_N	Nominal boundary limitation. Typically: T_N equals (T_{WC} -10ºc). Other temperature deltas may be given in the detailed requirements
T_{WC}	Worst case thermal boundary. Typically: T_{WC} equals (TC_2 - 30ºc)
ES_{NOM}	Nominal flight electrical stress conditions are those experienced during normal, steady-state, mission operations. Included are all maximum steady-state ac and dc components of electrical stresses, all daily temperature variations, and any and all changes in electrical, physical and thermal levels expected during normal operations in the typical mission environment. *Not included* are power-on and power-off events and any associated electrical transients, conditions due to anomalies, radiation-induced effects, electrical, physical and/or temperature excursions outside of the normal mission profile, and end-of-life degradation.
ES_{WC}	Worst-case flight electrical stress conditions (ES_{WC}) are those caused by power-on and power-off events associated with electrical transients not part of the normal, steady-state, mission profile; electrical, physical and/or temperature excursions due to atypical operation, total dose radiation-induced effects, and end-of-life degradation. Not requiring derating from maximum ratings are transients induced by system/sub-system failures (including fuse clearing events), nuclear events [single event (SEE/SEU) radiation-induced effects], and qualification ground test operations. Under no conditions shall maximum ratings be exceeded.
100 percent	Maximum rated value per detailed specification

To obtain the specific curve for each part type, numerical values are applied to the general curve based on the specified maximum rated values being 100 percent. The applicable derating curve or derating factor is given in the detailed section for each part type. The derating factor is to be multiplied times the part rating to obtain the allowed nominal limitation value for specific applications.

4.1.2 Mechanical Derating. Mechanical design properties shall have adequate strength margins for the intended application to sustain long-life performance over the specified design life. This derating shall include design properties associated with environments such as shock, vibration, acceleration, and temperature that produce force-function effects on flight hardware. Strength margins shall be based on mechanical property data from MIL-HDBK-5J where applicable and shall delimit susceptibility to mechanical failure modes such as bending, deformation, fracture, rupture, excessive deflection, and fatigue. Functional margins shall be calculated based on the recommendation of MIL-A83577B wherever possible.

4.1.2 End-of-Life.

Circuits shall be designed such that required functional performance at the component level is maintained even if the performance values of the parts used vary within the program identified end-of-life design limits.

4.1.3 Aging Sensitivity. Electronic, optical, and mechanical parts and materials are aging sensitive when they are subject to gradual shortening of their useful life, or progressive degradation of their performance parameters. Aging mechanisms include the following: Loss of hermeticity

b. Stress relaxation
c. Oxidation and corrosion
d. Outgassing
e. Cold flow and creep
f. Molecular cross-linking
g. Loss of adhesion
h. Embrittlement (including thermal) and hardening
i. Loss of torque
j. Loss of spring tension
k. Moisture absorption
l. Radiation effects

Aging sensitivity shall be considered in the design, selection, and application of parts and materials. In addition, aging sensitivity shall be incorporated into mandatory plans for shelf-life and aging control. These plans shall include requirements for minimum shelf-life assurance when parts and materials are procured, and for required revalidation and/or retesting of parts and materials after the shelf-life is exceeded. All parts and materials shall meet the requirements of TOR 2006(8583)-5235 for shelf-life control.

4.1.4 Sealed Packages.

Hermetically sealed parts are preferred for use in space vehicles. If nonhermetically sealed parts are selected, the in-process assembly and cleaning operations used shall not be detrimental to the parts, and

the subsequent outgassing, sublimation, moisture penetration, or moisture absorption shall not be detrimental to the part and its long-term performance, or to the system.

4.1.5 Registered (Reliability Suspect) PMP and Prohibited PMP.

The detailed sections of this document identify known registered PMP and prohibited PMP including applications and procurement restrictions.

4.1.6 Handling.

Protection against electrostatic damage to electrostatic sensitive devices shall be provided in accordance with paragraph 4.7.

4.1.7 Marking.

Marking shall be in accordance with the applicable military specification.

4.1.8 Outgassing Requirements.

When required by the Contamination Control Plan, all polymeric and organic materials shall be tested for outgassing in accordance with ASTM-E-595, and the results documented on the approved as-designed and as-built materials list. As a guideline, materials should exhibit a total mass loss (TML) of not more than 1.0 percent and a collected volatile condensable material (CVCM) of not more than 0.1 percent. Data listed in the NASA Reference Publication 1124, or on the NASA website for "Outgassing Data for Selecting Spacecraft Materials Online" at http://outgassing.nasa.gov, may be used for applicable materials in lieu of actual testing. The outgassing data should correspond to a condition/cure cycle that will be used.

A program Contamination Control Plan shall be developed, and an outgassing analysis performed, which demonstrates that outgassing from all materials used in the space vehicle, their mass and locations, including water vapor residue (WVR), do not degrade the performance of payload and bus systems, subsystems and units, such that they cannot meet the end-of-life requirements with adequate margin. Outgassing requirements do not apply to the small quantities of marking ink used externally on EEEE parts and printed wiring boards.

4.1.9 Alternate QCI Test/Sampling Plan.

Alternate QCI test/sampling plan for homogeneous lots as defined by the applicable MIL spec for microcircuits, discrete diodes, and transistors shall be in accordance with Appendix C of this document.

4.2 PMP Requirements.

The requirements for specific part types are stated in subsequent detailed requirements sections of this document where the applicable military specification requirements are also identified.

4.2.1 New Technology Insertion Requirements.

New technology PMP is defined as a part, material, or process (PMP) that has never been previously characterized or qualified by the contractor within the space environment intended for the application, or has limited or no space heritage, or commercial technology, and meets Appendix D of TOR-2006(8583)-5235. Class 1 changes (form, fit, function, reliability or radiation) to a previously qualified PMP shall result in the PMP being considered as new technology. A new technology insertion program shall be established for the identification, management, and tracking of new technology. The program shall include a plan that defines the new technology, and the criteria and methodology for characterization and

qualification of new technology. The technical requirements in the individual commodity section of this document may be used as starting boilerplate requirements for the qualification and characterization of new technology.

4.2.1.1 Physics-of-Failure.

Physics of Failure (PoF) is a proactive reliability assessment that is applied early in the product development cycle. PoF considers the mechanical, thermal, electrical, and chemical properties that could contribute to root cause failures through the product life cycle. PoF assessments consider failures that have occurred and their root cause analysis. PoF assessments also include documentation of inherent design attributes that are intended to avoid failures that might be anticipated from a detailed understanding of the product or manufacturing technologies.

As part of the characterization requirements for new technologies, PoF is required both for failures observed and failures avoided. Failures observed during production, manufacturing, test, and field use requires analyses of root cause. These analyses provide an understanding of the physical, chemical, and electrical processes that contributed to the anomaly. It is anticipated that most, hopefully all, vendors have failure analysis processes in place as part of the quality program. These processes, and the understanding of root causes, shall be leveraged for documenting Physics of Failure analyses.

Physics of Failure analysis for failures avoided encompasses failure mechanisms that might result from new or less understood technologies. This requires investigation of product structure, material make-up, and known failure mechanisms. Dominant failure mechanisms and sites shall be analyzed directly to show how failures are mitigated. As applicable, this effort shall be tied to corrective and preventive measures observed during failure investigations.

All accelerating factors and failure mechanisms shall be considered when deciding on the use of various technologies.

4.2.2 Parts and Materials Transfer.

Parts and materials transferred into a Program from other Programs or facilities of a contractor shall be reviewed for compliance to this document and approved by the PMPCB.

4.3 PMP Design, Construction, and Procurement

4.3.1 Design.

Parts shall be designed and constructed to meet the program's technical requirements and the requirements stated herein. Parts shall be designed and constructed of corrosion resistant materials or treated to resist corrosion.

4.3.1.1 Parts Procurement.

All parts shall be procured from the part original equipment manufacturer (OEM) or its franchised/authorized distributor, and shall come with an OEM certificate of compliance.

4.3.1.1.1 Sources of Supply for Procurement of Class S/V/K/JANS/T-Level Equivalent Parts.

[Note: T-level is an acceptable space-level designator for passives only.] When space quality Class S/V/K/JANS/T- level military specification parts cannot be procured because there are no qualified sources of supply, then an SCD (source control drawing) may be used to procure Class S/V/K/JANS/T-level parts provided that the drawings specify full compliance to the technical requirements of this document. These space-level equivalent devices shall be procured from:

1st Order	Certified Class S / V / K / JANS / T-level suppliers with Class S / V / K / JANS / T-level passives or equivalent Space Quality Baseline parts
2nd Order	Certified QML/QPL suppliers for similar product lines if 1st order not available
3rd Order	Suppliers with proven space-level quality infrastructure for similar product lines, which include Contractor approved test labs and third-party manufacturers if 1st and 2nd order not available

4.3.1.2 Materials Procurement.

All materials shall be procured from their original equipment manufacturer (OEM) or its franchised/authorized distributor, and shall come with an OEM certificate of compliance, and/or certification of analysis from the manufacturer.

4.3.2 Material Hazards.

Mechanical and electronic parts shall be constructed of materials that prevent exposure of either personnel or adjacent components to hazardous conditions. Hazardous conditions include, but are not limited to the following: arc generation, flammability, severe outgassing, toxicity, sublimation, and high vapor pressure. Material ratings for these attributes can be found in NASA HBK 8060.1 (superseded by NASA STD 6001) or NASA's MAPTIS database.

4.3.3 Surface Finishes and Solder Attachments

4.3.3.1 Use of Lead-Free Alloys, Pure Tin (plating or coating).

a. No pure tin, or >97 percent tin by weight, shall be used internally or externally, as an under-plating or final finish in the design and manufacture of the space vehicle, including (but is not limited to) EEEE parts and their packages/terminals/leads, mounting hardware, solder lugs, EMI shields, and spacecraft structures. Tin shall be alloyed with a minimum of 3 percent lead (Pb) by weight.

b. Lead-free tin alloy coatings or solders have not been approved for use on space hardware. Lead-free tin alloys may be used only if approved by the program PMPCB with customer concurrence. The contractor shall demonstrate that the lead-free tin alloy soldering process used to manufacture the hardware meets the program's requirements for reliability, mission life, parts compatibility, rework and thermal, vibration and shock environments. The information provided shall include data from design of experiments, life test results, whiskering and/or tin pest susceptibility evaluation results, statistical process control monitor data, temperature / materials compatibility analyses, and mechanical test results. Note that Sn96/Ag4, Au80Sn20, and Sn95/Sb5 are standard solder-attach materials used in high temperature soldering applications and are acceptable for those applications only.

c. Tin plated wire may be used provided that for each lot of wire, all the tin has been converted to copper tin intermetallic as demonstrated by chemical analysis. In addition, the solderability of the wire shall be verified.

4.3.3.2 Other Prohibited Metal Finishes and Alloys.

Materials capable of emitting excessive vacuum condensables, noxious or toxic gases when exposed to low pressure or high temperature shall not be used. Pure zinc, pure cadmium, selenium, or mercury shall not be used. The actual acceptable percentages of zinc and cadmium in alloys or brazes and the extent of over plating, if required, shall be technically substantiated with data for the intended applications and shall require PMPCB approval prior to use. Use of cadmium plating on mechanical fasteners or other parts is not approved on space hardware

4.3.4 Processes and Controls.

The manufacture of parts and materials shall be accomplished in accordance with processes and processing controls that ensure the reliability and quality required. These manufacturing processes and controls shall be accomplished in accordance with fully documented procedures. This documentation shall be in sufficient detail to provide a controlled manufacturing baseline for the manufacturer, which ensures that subsequent production items can be manufactured which are equivalent in performance, quality, dimensions, and reliability to initial production items used for qualification or for flight hardware. This documentation shall include the name of each process, each material required, the point where each material enters the manufacturing flow, and the controlling specification or drawing. The documentation shall indicate required tooling, facilities, and test equipment; the manufacturing checkpoints; the quality assurance verification points; and the verification procedures corresponding to each applicable process or material listed. Processing controls shall have a statistical basis if a sampling plan is used.

4.3.4.1 Solder Dipping, Retinning and Lead Forming.

Any solder dipping, re-tinning, and lead forming processes prior to assembly shall be qualified and monitored to ensure that any electrical, thermal, mechanical property or hermetic seal of the device has not been compromised.

4.3.5 Rework During Manufacture of Electronic Parts.

Rework during manufacturing shall not be allowed except as may be permitted by the applicable military specification of each electronic part.

4.3.6 Bimetallic Bonds.

Bimetallic lead bonds are reliability suspect. They may be used without additional PMPCB approval provided the following process steps are satisfied. Any other use requires specific approval by the PMPCB.

a. In process data for production lot inspection per MIL-STD-883, Method 2011, showing no bond lifts at the bimetallic interface (bond wire to die pad).

b. Machine set-up, bond verification and in process controls shall be performed per the applicable military specification, e.g. MIL-PRF-38535, MIL-PRF-38534, or MIL-PRF-19500.

c. As part of lot acceptance testing, three (3) sample units shall be subjected to a destructive bond pull test per MIL-STD-883, Method 2011 after a 300°C, one hour bake, to verify bond integrity. The Group B devices or PIND failures may be used for this test. Any bond lifts from the die pad shall be considered a failure, regardless of pull strength.

d. All attributes data gathered shall be included in the deliverable data package with each production lot.

4.4 Part Quality Assurance Provisions.

The quality assurance requirements for each part type are specified in the detailed requirements section for that part type. The production lot definition shall be as defined in Section 3 (Definitions), or the individual sections of this document. The quality assurance provisions are classified as:

a. In-process controls

b. Screening (100 percent)

c. Lot conformance tests

d. Qualification tests

e. Other tests (DPA, Hardness Assurance, etc.)

4.4.1 In-Process Controls.

Each production lot shall be subjected to the in-process production controls specified in the detailed requirements section of this document for that part type.

4.4.2 Screening (100 Percent).

Each item in every production lot shall be subjected to the 100 percent screening in the order shown (unless specified otherwise) in the detailed requirements section of this document for that part type.

Note: Many of the screening tables in this document list modifications to the test requirements, methods and criteria of the referenced military specification. When a blank is shown opposite a specific screen or test, it means that there is no change to the test method, criteria, or sample size specified in the referenced military specification. When the screening table is labeled "modifications", it means that the tests include those listed on the table as well as those called out in the referenced specification.

4.4.3 Lot Conformance Tests (or Quality Conformance Inspection).

Lot conformance testing shall be performed as a basis for final lot acceptance on each production lot of parts. After a production lot has passed all in-process controls and 100 percent screening requirements, the lot conformance tests shall be performed in the order shown (unless specified otherwise) on a randomly selected sample taken from the production lot. The detailed requirements for these lot conformance tests for each production lot are specified in the detailed requirements section of this document for each part type. When radiation hardness assurance requirements are specified, wafer lot conformance test shall be conducted per Appendix A of this document. Radiation testing may be conducted anytime following the completion of wafer fabrication and screening. Parts that have undergone destructive tests during lot conformance testing shall not be returned to the production lot for flight use. Samples subjected to the non-destructive test subgroups shall not be used for flight without PMPCB approval.

Note: Many of the lot conformance tables in this document list modifications to the test requirements, methods and criteria of the referenced specification. When a blank is shown opposite a specified test, it means that there is no change to the test method, criteria, or sample size specified in the reference specification and that the test method or criteria are mandatory as referenced. When the lot conformance table is labeled "modifications", it means that the tests include those listed on the table as well as those called out in the referenced specification.

4.4.4 Destructive Physical Analysis (DPA).

Destructive Physical Analysis shall be performed in accordance with MIL-STD-1580 and the detailed sections herein. For FPGAs, ASICs, and Hybrids, the sample size may be reduced to two (2) parts.

4.4.5 Qualification Tests.

All part types shall be qualified in accordance with the requirements stated herein. Parts that have undergone destructive tests during qualification testing shall not be returned to the production lot for flight use.

4.4.5.1 Extension of Qualification

Parts, materials, or processes may be qualified by extension when both of the following criteria are met:

a. The part, material, or process was successfully used in a prior but recent space application in which the application environment conditions of use and test were at least as severe as those required of the candidate PMP for qualification.

b. The part or material is of identical construction or contains constituents identical in composition and near identical in significant properties as the previously qualified part or material. The part or material is manufactured by the same manufacturing facility to the same manufacturing baseline as the previously qualified part or material, and the utilization of the part or material does not result in critical stresses or mechanical strain (such as due to thermal mismatch) greater than the previously qualified part or material. Qualification by extension shall be based on a review of supporting data by the PMPCB. Additionally, the previous qualification test was completed within two years of submittal of the request for qualification extension.

4.5 Material Quality Assurance Provisions.

The quality assurance provisions for specialized materials are specified in the detailed requirements for that material. The production lot definition shall be as defined in Section 3 (Definitions) of this document. The quality assurance provisions are classified as:

a. In-process controls

b. Screening (100 percent)

c. Lot conformance tests (sampling or periodic)

d. Qualification tests

4.5.1 In-Process Controls.

Each production lot or batch or blend of material shall be subjected to the in-process controls specified in the detailed requirements section of this document for that material.

4.5.2 Screening (100 Percent).

Each item, piece, or container of material shall be subjected to the 100 percent screening requirements specified in the detailed requirements section of this document for that material.

Note: Many of the screening tables in this document list, modifications to the test requirements, methods of criteria of the referenced specification. When a blank is shown opposite a screen or test, it means that there is no change to the test method, criteria, or sample size specified in the reference specification. When the screening table is labeled "modifications", it means that the tests include those listed on the table as well as those called out in the referenced specification.

4.5.3 Lot Conformance Tests (or Quality Conformance Inspection): Sampling or Periodic.

Lot conformance testing shall be performed as a basis for final lot acceptance on each production lot or batch or blend of material. After a production lot or batch or blend of material has passed all in-process controls and screening requirements, the lot conformance tests shall be performed on randomly selected samples taken as specified from the production lot or batch or blend. The detailed requirements for these lot conformance tests are specified in the various requirement sections of this document. A physical or chemical analysis shall be performed as a portion of lot conformance testing when specified in the detailed requirements section of this document for that material. Test samples that have undergone destructive tests during lot conformance testing shall not be returned to the production lot or batch or blend.

4.5.4 Qualification Tests.

All materials and blends or composites thereof shall be qualified in accordance with the requirements stated herein. Material samples that have undergone destructive tests during qualification testing shall not be returned to the production lot or batch or blend.

4.6 Packaging.

Packaging of parts and materials during shipment shall be per the requirements imposed by the associated military specification for the particular item. Electrostatic-sensitive items shall be packaged in accordance with paragraph 4.7.

4.7 Electrostatic-Sensitive Items.

Electrostatic discharge (ESD) control for the protection of electrical and electronic parts, components, assemblies, and equipment shall be in accordance with MIL-STD-1686 (MIL-HDBK-263 may be used for guidance in establishing an ESD control plan) or a program approved equivalent.

4.8 Data and Record Retention.

Data files, test samples (e.g., coupons, DPA samples and/or slugs, etc.) and other PMP-related records shall be retained by the supplier or contractor for a period specified by the contract and/or program. The supplier may keep these items in-house or ship them to the purchaser along with the ordered parts or materials. The supplier shall also be required to provide the purchaser at least 30-days notice, or as specified in the contract, prior to any destruction of test samples and records.

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5. Detailed Requirements

The detailed requirements for parts, materials, and processes for use in space vehicles are contained in the following sections of this document. These detailed requirements are in addition to the general requirements contained in Section 4.

Every effort was made to utilize standard document format, but this document retains the separately called out technical sections (starting with Section 100) to focus the user industry on the unique space quality items that are paramount for mission success in each technical section.

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SECTION 100

BOARDS, PRINTED WIRING

1. SCOPE. This section sets forth detailed requirements for rigid printed wiring boards, including:

Type 1 -Single Sided

Type 2 -Double Sided

Type 3 -Multilayer Board without Blind or Buried Vias

Type 4 -Multilayer Board with Blind and/or Buried Vias

Type 5 -Multilayer Metal Core Board without Blind or Buried Vias

Type 6 -Multilayer Metal Core Board with Blind and/or Buried Vias

2. APPLICATION

2.1 General Requirements. Printed wiring boards shall be designed in accordance with IPC 2221 Class 3 and IPC 2222 Class 3, and fabricated in accordance with IPC 6012 Class 3/A, MIL-PRF-31032 /1 or /2 or MIL-PRF-55110G and this document. The contractor shall demonstrate that all the processes used to design, qualify, manufacture and test products are documented and meet all program requirements. In case of conflict, the provisions of this document shall apply.

2.2 Qualifications. The manufacturer shall be qualified/certified to MIL-PRF-31032 /1 or /2, MIL-PRF-55110G, or IPC 6012 Class 3/A. If the supplier is only certified to IPC 6012 Class 3/A, the contractor shall verify by audit that the build documentation, in- process controls, qualification testing and construction review meet the program requirements.

2.3 Materials

a. All materials on the delivered PWBs shall meet the outgassing requirements specified in Section 4, General Requirements, paragraph 4.1.9 of this document.

b. Prepregs and laminates shall comply with the IPC 4101. Minimum Tg shall be 170°C for epoxy materials. In case of conflict, the provisions of this document shall apply.

c. Permanent solder mask shall comply with IPC-SM-840 Class H. In addition, the solder mask shall meet the outgassing requirements specified in Section 4, General Requirements, paragraph 4.1.9 of this document. In case of conflict, the provisions of this document shall apply.

2.4 Raw Materials Storage

a. Laminates shall be stored flat under temperature and humidity conditions specified by their supplier. Laminates shall be supported over their entire surface area to prevent bow and twist. The corners shall be protected to prevent any damage.

b. Prepreg material shall be stored in a protective area, containers, or packaging under temperature and humidity conditions specified by its supplier that minimizes its exposure to temperature, humidity and contamination (dust, hair, etc.). Material that exceeds storage life for the storage conditions shall not be used. During handling and storage, adequate packing support shall be provided for both rolled and sheet material in order to prevent creasing, crazing, or wrinkling. Prepreg shall not be exposed to ultraviolet light during storage. If no shelf life is specified by the supplier, the maximum shelf life shall be 6 months when stored at a maximum temperature of 4.5ºC (40ºF) and 3 months when stored at a relative humidity between 30 and 50 percent and a maximum temperature of 21ºC (70ºF).

The above requirements shall be verified by periodic audit.

3. DESIGN AND CONSTRUCTION

3.1 Rigid Printed Wiring Boards. All rigid printed wiring boards with plated-through holes shall be designed in accordance with IPC 2221 Class 3 and IPC 2222 Class 3 and manufactured in accordance with MIL-PRF-31032 /1 and /2, MIL-PRF-55110G or IPC 6012 Class 3/A and the following:

a. Nonfunctional Lands (Internal Layers)
Nonfunctional lands shall be included on internal layers of multilayer boards whenever clearance requirements permit.

b. Etchback
Etchback shall be used to ensure resin smear is completely removed from the holes of multilayer boards prior to plating. The limits shall be between 0.0001 inch minimum and 0.002 inch maximum.

c. Drill Bit Limit
The board manufacturer shall have a process to define, verify, and maintain a matrix, which identifies the optimum number of drill hits allowed for specific types of materials, number of layers, and hole diameter.

d. Drill Changes
All drill bit changes shall be documented and recorded. The record may be in the form of a drill tape or any digital storage medium.

e. Stacking of Panels When Drilling Plated Through Holes
Stacking of panels when drilling plated-through holes shall not be permitted for multilayered or double sided boards.

f. Tin-lead Plating
Tin-lead plating thickness shall be 0.0003 inch as a minimum before fusing. There shall be no solder plate on any surface that is to be laminated to an insulator, metal frame, heatsink, or stiffener. For final finishes, lead-free tin plating, including immersion tin, shall not be used.

g. Fusing
After solder plating and other processes, unless otherwise specified on the master (source control) drawing, the printed wiring board shall be fused. Only one fusing operation shall be allowed. The fuse time and temperature shall be recorded. After fusing, the solder coating shall be homogeneous and completely cover the conductors with no pitting, no pinholes, or non-wet areas. Sidewalls of conductors need not be solder coated. Touch-up is permitted but shall be limited to no more than 5 percent of lands or pads.

h. Ductility and Tensile Strength
Elongation of as-plated copper shall be 18 percent minimum with a minimum tensile strength of 40 Kpsi. Testing shall be in accordance with IPC 650 Method 2.4.18.1. Samples shall be taken at minimum and maximum current plating densities. Sampling frequency shall be done at a statistically valid frequency to assure that the material properties are under statistical process control. Testing frequency shall not be less than once a month under any circumstance.

i. Process-Control Coupons
Process-control coupons shall be utilized to control the manufacturing processes of each panel. The number of in-process coupons shall be determined by statistical process control sampling requirements. Process-control coupons shall be included in the shipment of the deliverable boards only if requested on the purchase order.

j. Solder Plate Verification
Each board that is to be fused shall have a solder-plate coupon. Solder plate coupons shall be removed from the panel before fusing to verify solder thickness. Solder-plate coupons shall be included in the shipment of the deliverable parent boards. Alternate measuring techniques such as x-ray fluorescence may be used provided the measurements are documented and retrievable within 72 hours of request

k. Deliverable Coupons (Conformance Coupons)
Double-sided and multilayer printed wiring boards shall be produced with two deliverable A or B coupons per board. For small board sizes, two deliverable coupons per 150 square centimeters (24 square inches) of panel area shall be produced. Coupons suitable to monitor the processes involved shall be located on the panel in positions across the diagonal of each board. A single coupon located at the center area common to the inside corners of adjoining boards on a panel may be used as one of the required coupons for each of the adjoining boards. For example, for four large boards on a panel, a coupon at each of the four outside corners and a common coupon at the center, for a total of five coupons, are all that are required (see Figure 100-1 for preferred panel lay-ups). These deliverable coupons shall be in addition to the process-control coupons required for each panel. All coupons shall be completely processed at the same time as the deliverable boards. These coupons may be used for conformance testing.

l. Storage and Retrievability
All deliverable (conformance) coupons shall be stored and shall be retrievable within 72 hours of request for the time period specified by the program or contract.

m. Marking
Each individual board and each set of quality conformance test circuit strips (as opposed to each individual coupon) shall be marked in accordance with the master drawing and MIL-STD-130 with the date code (as specified below), the traceability serial number, the part number, and the manufacturer's CAGE code. Coupon marking shall be the same as board marking and all deliverable coupons shall be individually serialized. The date code shall be formatted as follows:

Year	Day of year (from 1 January)
05	001

This date shall reflect the date of final copper plating.

n. Traceability
The board manufacturer shall establish and maintain forward and backward traceability for all boards. This traceability shall reflect the exact disposition of each board. Boards that are rejected shall also be included in the traceability records and the reason for rejection shall be recorded. Each quality conformance test circuitry shall be traceable to the production boards produced on the same panel. All separated individual coupons shall have their traceability maintained back to the quality conformance test circuitry. Traceability records shall include board and coupon positions on the panel.

o. Copper Plating Thickness
The minimum plating thickness in plated through holes shall be 0.0012 inch. Any copper thickness less than 0.001 inch shall be considered a void. Blind and buried vias connecting across more than three layers shall also comply with this requirement. This requirement does not apply to microvias.

p. Hot Air Leveling
PWBs shall only be hot air leveled once. The solder coating shall be homogeneous and completely cover the conductors with no pitting, no pinholes, or non-wet areas. Sidewalls of conductors need not be solder coated. Touch-up is permitted but is limited to no more than 5 percent of lands or pads. After hot air leveling processing (including cleaning), boards shall undergo ionic verification testing per IPC-TM-650 2.3.25 on a 4.0 sampling basis per IPC 6012 Rev C Table 4-2. The contamination level shall not be greater than an equivalent of 1.56 µg/cm2 of sodium chloride

q. Cracks
No cracks in the copper foil or plating shall be permitted

r. Repair
Repairs shall not be permitted.

3.2 Multilayer Printed Wiring Boards

a. Copper Treatment
The surfaces of the copper on all inner layers of multilayer printed wiring boards to be laminated shall be treated or primed prior to lamination to improve the laminate bonding. A copper oxidation technique is acceptable treatment prior to lamination.

b. Ground plane Distribution
Multilayer printed wiring boards shall be configured so as to equalize the distribution of conductive areas in a layer and the distribution of conductive areas among layers. Ground planes shall be balanced around the midpoint to maintain PWB flatness.

3.3 Metal Core Boards. Metal core boards shall use material in accordance with ANSI/IPC-CF-152 and this document. When metal core boards are used, the lateral dielectric spacing between the metal core and adjacent conducting surfaces shall pass the dielectric withstanding voltage test in accordance with IPC-TM-650, Method 2.5.7 except that the minimum voltage shall be 750 volts D.C. There shall be no flashover, arcing, breakdown, or leakage exceeding one microampere.

4. QUALITY ASSURANCE. Quality assurance provisions shall be in accordance with Section 4, General Requirements, of this document , the requirements of MIL-PRF-31032 /1 or /2, MIL-PRF-55110G, and the following:

4.1 In-process Controls. In-process controls shall be monitored to assure that the manufacturing process is in a state of statistical control for the requirements specified.

a. Elongation And Tensile Strength
Elongation and tensile strength of as-plated copper shall be tested at least once a month.

b. Inner Layer Inspection
Prior to lamination, all inner layers shall be 100 percent inspected for continuity and shorts, correct line width and spacing.

4.2 Lot Conformance Tests. Lot conformance tests shall be in accordance with Section 4, General Requirements, of this document, and the requirements of MIL-PRF-31032 /1 or /2, MIL-PRF-55110G or IPC 6012 Class 3/A and the following:

a. A minimum of one as received and one thermal stress coupon per PWB shall be microsectioned and inspected. Coupons between PWBs may be used to represent contiguous PWBs. These coupons as well as all unsectioned coupons shall be delivered with the PWBs.

b. Electrical continuity and isolation testing on 100 percent of the nets on all PWBS except Type 1 is required and shall be performed in accordance with Section 4, General Requirements, of this document , and the requirements of MIL-PRF-31032 /1 or /2, MIL-PRF-55110G or IPC 6012 Class 3/A.

c. Microsections shall be reviewed for inner layer separation before and after microetching.

4.3 Qualification Tests. The manufacturer shall be certified as a qualified manufacturer in accordance with the requirements of MIL-PRF-31032 /1 or /2, MIL-PRF-55110G, or IPC 6012 Class 3/A. If the supplier is only certified to IPC 6012 Class 3/A, the contractor shall verify by audit that the build documentation, in-process controls, qualification testing and construction review meet the program requirements. If the complexity of the PWB exceeds the standard qualification coupon in the specifications, a flight PWB shall be qualification tested and meet all the Group A and B requirements.

4.4 Lot Verification. For each design type and lot of multilayer PWBs, a flight PWB shall be microsectioned and meet the Plated-Through-Hole (PTH) requirements. The sections shall include all PTH diameters and blind buried vias from various areas of the PWB. The PWB, from the panel whose coupons indicate the thinnest acceptable copper plating thickness, shall be microsectioned, and thermally stressed to demonstrate compliance with PTH requirements. Note that a rejectable PWB from this panel may be used for lot verification provided that the defect is not related to PTH integrity. If any PWB section fails, the lot shall be rejected.

Any alternative lot verification approach shall require approval by the program PMBCB. The alternative approach shall require data that demonstrate, for a particular PWB design and fabrication facility, indisputable correlation between the PTH quality of the flight PWB and the test vehicle of the alternate approach used for lot verification. As a minimum this data shall demonstrate that:

a. The plating uniformity varies less than 10% between plating at the panel center and the coupon locations

b. The supplier process controls show lot-to-lot uniformity over time and process consistency within a lot

c. Any test vehicle used in the alternate approach shall reflect the PWB design including all plated through-hole and via types and PWB processing including all copper plating operations

5. REGISTERED (RELIABILITY SUSPECT) PMP shall include:

a. Microvias

b. Blind vias plated blind (i.e., not made by sequential lamination)

c. ENIG (Electroless Nickel Immersion Gold) requires special controls to reduce risk of black pad.

6. PROHIBITED PMP shall include:

a. Lead-free tin plating/coating in printed wiring boards (see Section 4, General Requirements, paragraph 4.3.3, of this document). Note if tin is used as a metal etch resist it shall be totally removed prior to the final finish application.

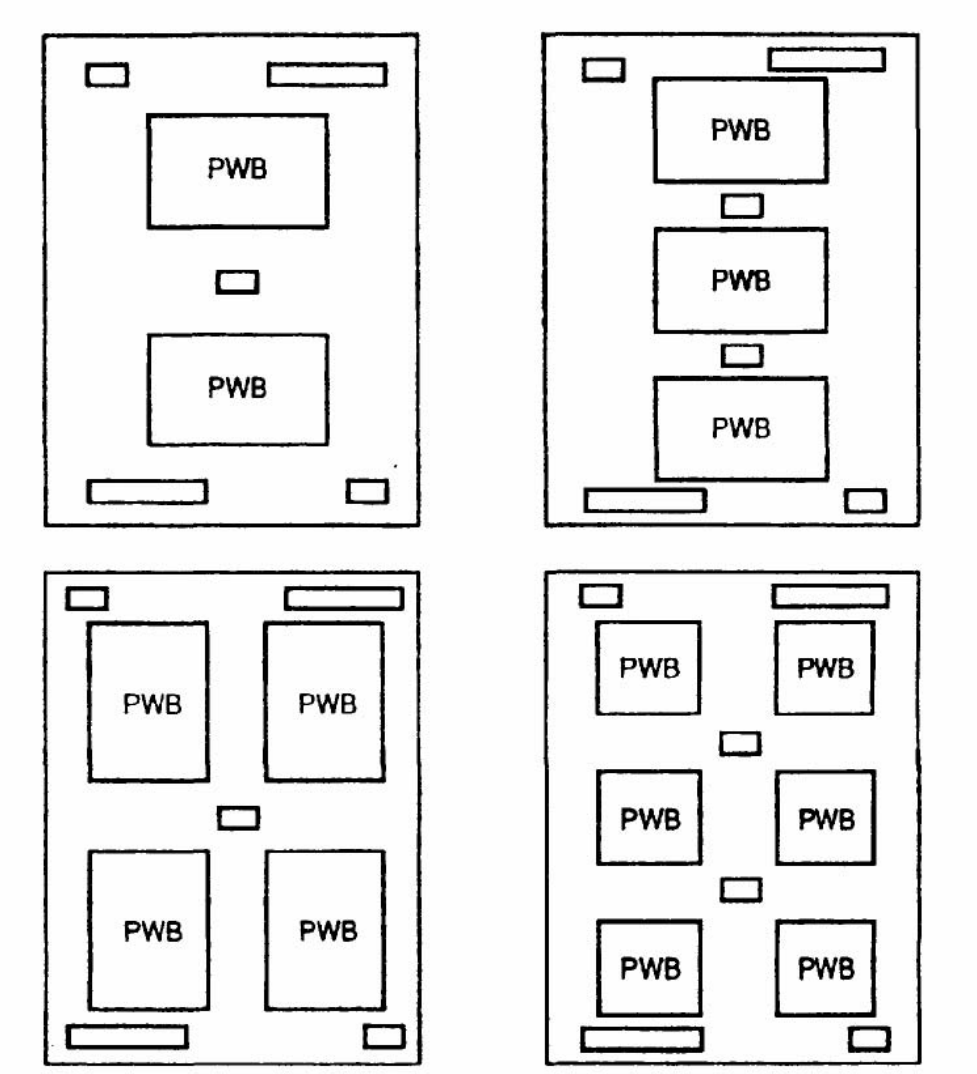

Figure 100-1. Deliverable Coupon Placement.

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SECTION 110
FLEX AND RIGID-FLEX PRINTED WIRING BOARDS

1. SCOPE. This section sets forth detailed requirements for flex printed wiring boards, including:

Type 1 - Single Sided flexible printed wiring containing one conductive layer, with or without stiffeners

Type 2 - Double Sided flexible printed wiring containing two conductive layers, with plated through holes with or without stiffeners

Type 3 - Multilayer flexible printed wiring containing three or more conductive layers, with plated through holes with or without stiffeners

Type 4 - Multilayer rigid and flexible material combinations containing three or more conductive layers with plated through holes

Type 5 - Flexible or rigid–flex printed wiring containing two or more conductive layers, without plated through holes

2. APPLICATION

2.1 General Requirements. Flex and rigid-flex printed wiring boards shall be designed in accordance with IPC 2221 Class 3 and IPC 2223 Class 3 and fabricated in accordance with MIL-P-50884D(2), MIL-PRF-31032 /3 or /4, or IPC 6013 Class 3 and this document. The contractor shall demonstrate that all the processes used to design, qualify, manufacture and test products are documented and meet all program requirements. In case of conflict, the provisions of this document shall apply.

2.1.1 Qualifications. The manufacturer shall be qualified/certified to MIL-P-50884D(2), MIL-PRF-31032/3 or /4, or IPC 6013 Class 3. If the certification to IPC 6013 Class 3 is used, the contractor shall verify by audit that the build documentation, in process controls, qualification testing and construction review will meet the program requirements.

2.1.2 Materials

a. All materials on the delivered PWB shall meet the outgassing requirements specified in Section 4, General Requirements, paragraph. 4.1.9 of this document.

b. Flex materials shall comply with IPC 4202/1, 4203/1 or /18 or 4204/1 or /11 (material shall be restricted to Kapton base materials, adhesiveless or acrylic adhesive systems).

c. Rigid materials shall comply with Section 100.

d. Permanent solder mask shall comply with IPC-SM-840 Class H. In addition, the solder mask shall meet the outgassing requirements specified in Section 4, General Requirements, paragraph 4.1.9 of this document. In case of conflict, the provisions of this document shall apply.

2.1.3 Raw Material Storage

a. Flex materials shall comply with supplier recommended procedures.

b. Laminates shall be stored flat under temperature and humidity conditions specified by their supplier. Laminates shall be supported over their entire surface area to prevent bow and twist. The corners shall be protected to prevent any damage.

c. Prepreg material shall be stored in a protective area, containers, or packaging under temperature and humidity conditions specified by its supplier that minimizes its exposure to temperature, humidity and contamination (dust, hair, etc). Material that exceeds storage life for the storage conditions shall not be used. During handling and storage, adequate packing support shall be provided for both rolled and sheet material in order to prevent creasing, crazing, or wrinkling. Prepreg shall not be exposed to ultraviolet light during storage. If no shelf life is specified by the supplier, the maximum shelf life shall be 6 months when stored at a maximum temperature of 4.5ºC (40ºF) and 3 months when stored at a relative humidity between 30 and 50 percent and a maximum temperature of 21ºC (70ºF).

The above requirements shall be verified by periodic audit.

Section 110 FLEX AND RIGID-FLEX PRINTED WIRING BOARDS

3. DESIGN AND CONSTRUCTION

3.1 Flex Printed Wiring Boards. Flex and rigid-flex printed wiring boards shall be designed in accordance with IPC 2221 Class 3 and IPC 2223 Class 3 and fabricated in accordance with MIL-P-50884D(2), MIL-PRF-31032 /3 and /4, IPC 6013 Class 3 and this document. In case of conflict, the provisions of this document shall apply.

3.2 All flex and rigid–flex PWBs shall meet the following requirements:

a. Ductility and Tensile Strength
Elongation of as-plated copper shall be 18 percent minimum with a minimum tensile strength of 40 Kpsi. Testing shall be in accordance with IPC 650 Method 2.4.18.1. Samples shall be taken at minimum and maximum current plating densities. Sampling frequency shall be done at a statistically valid frequency to assure that the material properties are under statistical process control. Testing frequency shall not be less than once a month under any circumstance.

b. Process-control Coupons
Process-control coupons shall be utilized to control the manufacturing processes of each panel. The number of in-process coupons is at the manufacturer's option. These process-control coupons shall be included in the shipment of the deliverable boards only if requested on the purchase order.

c. Solder Plate Verification
Each board that is to be fused shall have a solder-plate coupon. Solder plate coupons shall be removed from the panel before fusing to verify solder thickness. Solder-plate coupons shall be included in the shipment of the deliverable parent boards. Alternate measuring techniques such as x –ray fluorescence may be used provided the measurements are documented and retrievable within 72 hours of request.

d. Deliverable Coupons (Conformance Coupons)
Double sided flex with plated through holes and multilayer flex and rigid-flex printed wiring boards shall be produced with two deliverable A or B coupons per board. For small board sizes, two deliverable coupons per 150 square centimeters (24 square inches) of panel area shall be produced. Coupons suitable to monitor the processes involved shall be located on the panel in positions across the diagonal of each board. A single coupon located at the center area common to the inside corners of adjoining boards on a panel may be used as one of the required coupons for each of the adjoining boards. For example, for four large boards on a panel, a coupon at each of the four outside corners and a common coupon at the center, for a total of five coupons, are all that are required (see Figure 100-1 for preferred panel lay-ups). These deliverable coupons are in addition to the process-control coupons required for each panel. All coupons shall be completely processed at the same time as the deliverable boards. These coupons may be used for conformance testing.

e. Storage and Retrievability
All deliverable (conformance) coupons shall be stored and shall be retrievable within 72 hours of request for the time period specified by program/contract.

f. Marking
Each individual board and each set of quality conformance test circuit strips (as opposed to each individual coupon) shall be marked in accordance with the master drawing and MIL-STD-130 with the date code (as specified below), the traceability serial number, the part number, and the manufacturers CAGE code. Coupon marking shall be the same as board marking and all deliverable coupons shall be individually serialized. The date code shall be formatted as follows:

Year	Day of year (from 1 January)
05	001

This date shall reflect the date of final copper plating. If no copper plating is done, it shall reflect the lamination date.

g. Traceability
The board manufacturer shall establish and maintain forward and backward traceability for all boards. This traceability shall reflect the exact disposition of each board. Boards, which are rejected, shall also be included in the traceability documentation and the reason for rejection shall be identified. Each quality conformance test circuitry shall be identifiable with those corresponding production boards produced on the same panel. All separated individual coupons shall have their traceability maintained back to the quality conformance test circuitry. Traceability shall include board and coupon positions on the panel.

h. Tin-lead Plating
Tin-lead plating thickness shall be 0.0003 inch as a minimum before fusing. There shall be no solder plate on any surface, which is to be laminated to an insulator, metal frame, heatsink, or stiffener. For final finishes lead-free tin plating, including immersion tin, shall not be used.

i. Fusing
After solder plating and other processes, unless otherwise specified on the master (source control) drawing, the printed wiring board shall be fused. Only one fusing operation is permitted. The fuse time and temperature shall be recorded. After fusing, the solder coating shall be homogeneous and completely cover the conductors with no pitting, no pinholes, or non-wet areas. Sidewalls of conductors need not be solder coated. Touch-up is permitted but is limited to no more than 5 percent of lands or pads.

j. Hot Air Leveling
The PWBs shall only be hot air leveled once. The solder coating shall be homogeneous and completely cover the conductors with no pitting, no pinholes, or non-wet areas. Sidewalls of conductors need not be solder coated. Touch-up is permitted but is limited to no more than 5 percent of lands or pads. After the hot air leveling process (including cleaning), boards shall undergo ionic verification testing per IPC-TM-650 2.3.25 on a 4.0 sampling basis per IPC 6012 Rev C Table 4-2. The contamination level shall not be greater than an equivalent of 1.56 µg/cm2 of sodium chloride

k. Repair
Repairs shall not be permitted

l. Drill Bit Limit
The board manufacturer shall have a process to define, verify, and maintain a matrix, which identifies the optimum number of drill hits allowed for specific types of materials, number of layers, and hole diameter.

m. Drill Changes All drill bit changes shall be documented and recorded. The record may be in the form of a drill tape or any digital storage medium.

n. Stacking of Panels When Drilling Plated Through Holes
Stacking of panels when drilling plated-through holes shall not be permitted for multilayered or double side boards.

3.3 Multiple layer flex and rigid-flex boards with plated-through-holes. In addition to the requirements above, multiple layer boards shall meet the following requirements:

a. Construction
Only adhesiveless construction shall be used on multilayer rigid-flex boards.

b. Nonfunctional Lands (Internal Layers)
Nonfunctional lands shall be included on internal layers of multilayer boards whenever clearance requirements permit.

c. Copper Plating Thickness
The minimum plating thickness in plated through holes shall be 0.0012 inch. Any copper thickness less than 0.001 inch shall be considered a void. Blind and buried vias more than three layers shall also comply with this requirement. This requirement does not apply to microvias.

d. Etchback
Etchback or equivalent processes shall be used to ensure complete resin smear removal from the holes of multilayer boards prior to plating. When etchback is used, the limits shall be between 0.0001 inch minimum and 0.002 inch maximum. This requirement only applies for rigid flex boards.

e. Copper Preparation
The surface of the copper on all rigid (IPC 4101) materials inner layers shall be treated or primed prior to lamination to increase the laminate bonding. A copper oxidation technique is an acceptable treatment prior to lamination.

f. Cracks
No cracks in the copper foil or plate shall be permitted.

g. Power or Ground Plane Distribution
Multilayer printed wiring boards shall be configured so as to equalize the distribution of conductive areas in a layer and the distribution of conductive areas among layers. Ground planes shall be balanced around the mid point to maintain PWB flatness

h. Stacking of Panels When Drilling Plated Through Holes
Stacking of panels when drilling plated-through holes shall not be permitted for multilayered boards.

i. Stress Relief
On rigid-flex boards the egress of the flex from the rigid area shall be stress relieved with an elastomeric materials.

4. QUALITY ASSURANCE. Quality assurance provisions shall be in accordance with Section 4, General Requirements, of this document , the requirements MIL-P-50884D(2), MIL-PRF-31032 /3 and /4, IPC 6013 Class 3, and the following:

If the supplier is only certified to IPC 6013 Class 3, the contractor shall verify that the build documentation, in-process controls, qualification testing and construction review meet the program requirements.

4.1 In-process Controls. In-process controls shall be monitored to assure that the manufacturing process is in a state of statistical control for the requirements specified.

a. Elongation and tensile strength of as-plated copper shall be tested at least once a month.

b. Inner Layer Inspection
Prior to lamination, all inner layers shall be 100 percent inspected for continuity and shorts, and visually inspected for correct line width and spacing.

4.2 Lot Conformance Tests. Lot conformance tests shall be in accordance with Section 4, General Requirements, of this document , and the requirements of MIL-P-50884D(2), MIL-PRF-31032 /3 and /4, IPC 6013 Class 3, and the following:

a. A minimum of one as received and one thermal stress coupon per PWB shall be microsectioned and inspected. Coupons between PWBs may be used to represent contiguous PWBs.

b. Electrical continuity and isolation testing on 100 percent is required on all PWBS except Type 1 and shall be performed in accordance with Section 4, General Requirements, of this document, and the requirements of MIL-P-50884D(2), MIL-PRF-31032 /3 and /4, IPC 2221Class 3 and IPC 2223 Class 3 and IPC 6013 Class 3.

c. Microsections shall be reviewed for inner layer separation before and after microetching.

4.3 Qualification Tests. The manufacturer shall be certified as a qualified manufacturer in accordance with the requirements of MIL-P-50884D(2), MIL-PRF-31032 /3 or /4, or IPC 6013 Class 3. If the supplier is only certified to IPC 6013 Class 3, the contractor shall verify that the build documentation, in-process controls, qualification testing and construction review meet the program requirements. If the complexity of the PWB exceeds the standard qualification coupon in the specifications, a flight PWB shall be qualification tested and meet all the Groups A and B requirements.

4.4 Lot Verification. For each design type and lot of multilayer PWBs, a flight PWB shall be microsectioned and meet the Plated-Through-Hole (PTH) requirements. The sections shall include all PTH diameters and blind buried vias from various areas of the PWB. The PWB, from the panel whose coupons indicate the thinnest acceptable copper plating thickness, shall be microsectioned, and thermally stressed to demonstrate compliance with PTH requirements. Note that a rejectable PWB from this panel may be used for lot verification provided that the defect is not related to PTH integrity. If any PWB section fails, the lot shall be rejected.

Any alternative lot verification approach shall require approval by the program PMBCB. The alternative approach shall require data that demonstrate, for a particular PWB design and fabrication facility, indisputable correlation between the PTH quality of the flight PWB and the test vehicle of the alternate approach used for lot verification. As a minimum this data shall demonstrate that:

a. The plating uniformity varies less than 10% between plating at the panel center and the coupon locations

b. The supplier process controls show lot-to-lot uniformity over time and process consistency within a lot

c. Any test vehicle used in the alternate approach reflects the PWB design including all plated through-hole and via types and PWB processing including all copper plating operations

5. REGISTERED (RELIABILITY SUSPECT) PMP shall include:

a. Rigid-flex wiring board with adhesive construction.

b. Microvias

c. Blind vias plated blind (i.e., not made by sequential lamination)

d. ENIG (Electroless Nickel Immersion Gold) requires special controls to reduce risk of black pad.

6. PROHIBITED PMP shall include:

a. Lead-free tin plating/coating in printed wiring boards (see Section 4, General Requirements, paragraph 4.3.3 of this document). Note that if tin is used as a metal etch resist, it shall be totally removed prior to the final finish application.

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SECTION 120

RF (MICROWAVE) BOARDS, PRINTED WIRING

1. SCOPE. This section sets forth detailed requirements for RF (Microwave) printed wiring boards, including:

Type 1 -Single Sided

Type 2 -Double Sided

Type 3 -Homogenous Multilayer Construction

Type 4 -Mixed Dielectric Materials

Type 5 -Homogenous Multilayer Board with Blind and/or Buried Vias

Type 6 -Mixed Dielectric Multilayer Board with Blind and/or Buried Vias

Type 7 -Metal Core /Backed Boards

2. APPLICATION

2.1 General Requirements. Printed wiring boards shall be designed in accordance with IPC 2221 Class 3 and IPC 2252 Class 3, and fabricated in accordance with IPC 6018 Class 3, MIL-PRF-31032 /5 or /6, or MIL-PRF-55110G (Type 1 and 2) and this document. The contractor shall demonstrate that all the materials and processes used to design, qualify, manufacture and test products are documented and meet all program requirements. In case of conflict, the provisions of this document shall apply.

2.2 Qualifications. The manufacturer shall be qualified/certified to MIL-PRF-31032 /5 or /6, or IPC 6018 Class 3, MIL-PRF-55110G (Type 1and 2). The qualification/certification shall be for the qualified material only. If the supplier is only certified to IPC 6018 Class 3, the contractor shall verify by audit that the build documentation, in process controls, qualification testing and construction review meet the program requirements.

2.3 Materials

a. All materials on the delivered PWBs shall meet the outgassing requirements specified in Section 4, General Requirements, paragraph 4.1.9 of this document.

b. Prepregs, bond films and laminates shall comply with the IPC 4101, IPC 4103, or IPC 4203. In case of conflict, the provisions of this document shall apply.

c. Permanent solder mask shall comply with IPC-SM-840 Class H. In addition, solder mask shall meet the outgassing requirements specified in Section 4, General Requirements, paragraph 4.1.9 of this document. In case of conflict, the provisions of this document shall apply.

2.4 Raw Materials Storage

a. Laminates shall be stored flat under temperature and humidity conditions specified by their supplier. Laminates shall be supported over their entire surface area to prevent bow and twist. The corners shall be protected to prevent any damage.

b. Prepreg material shall be stored in a protective area, containers, or packaging under temperature and humidity conditions specified by its supplier that minimizes its exposure to temperature, humidity and contamination (dust, hair, etc.). Material that exceeds shelf life for the temperature and humidity storage conditions shall not be used. During handling and storage, adequate packing support shall be provided for both rolled and sheet material in order to prevent creasing, crazing, or wrinkling. Prepreg shall not be exposed to ultraviolet light during storage. If no storage life is specified by the supplier, the maximum shelf life shall be 6 months when stored at a maximum temperature of 4.5ºC (40ºF) or 3 months when stored at a relative humidity between 30 and 50 percent and a maximum temperature of 21ºC (70ºF).

c. Bonding Films shall be stored in a protective area, containers, or packaging under temperature and humidity conditions specified by its supplier which minimizes its exposure to temperature, humidity and contamination (dust, hair, etc.). Material that exceeds shelf life for the temperature and humidity storage conditions shall not be used. During handling and storage, adequate packing support shall be provided for both rolled and sheet material in order to prevent creasing, crazing, or wrinkling. Shelf life shall be as specified by the supplier.

The above requirements shall be verified by periodic audit.

3. DESIGN AND CONSTRUCTION

3.1 Printed Wiring Boards. All printed wiring boards shall be designed in accordance with IPC 2221 Class 3 and IPC-2252 Class 3 and fabricated in accordance with MIL-PRF-31032 (/5 or /6), MIL-PRF-55110G (Type 1 and 2) or IPC 6018 Class 3, and the following:

a. Nonfunctional Lands (Internal Layers)
Nonfunctional lands shall be included on internal layers of multilayer boards whenever clearance or performance requirements permit.

b. Etchback
Etchback shall be used to ensure resin smear is completely removed from the holes of multilayer boards prior to plating. When etchback is used, the limits shall be between 0.0001 inch minimum and 0.002 inch maximum for “non-PTFE” type materials. For “PTFE” type materials, there shall be no smear evident or negative etchback.

c. Drill Bit Limit
The board manufacturer shall have a process to define, verify, and maintain a matrix, which identifies the optimum number of drill hits allowed for specific types of materials, number of layers, and hole diameter.

d. Drill Changes
All drill bit changes shall be documented and recorded. The record may be in the form of a drill tape or any digital storage medium.

e. Stacking of Panels When Drilling Plated Through Holes
Stacking of panels when drilling plated-through holes shall not be permitted for multilayered or double sided boards.

f. Tin-lead Plating
Tin-lead plating thickness shall be 0.0003 inch as a minimum before fusing. There shall be no solder plate on any surface that is to be laminated to an insulator, metal frame, heatsink, or stiffener. For final finishes, lead-free tin plating including immersion tin shall not be used.

g. Fusing
After solder plating and other processes unless otherwise specified on the master (source control) drawing the printed wiring board shall be fused. Only one fusing operation is permitted. The fuse time and temperature shall be recorded. After fusing, the solder coating shall be homogeneous and completely cover the conductors with no pitting, no pinholes, or non-wet areas. Sidewalls of conductors need not be solder coated. Touch-up is permitted, but shall be limited to no more than 5 percent of lands or pads.

h. Ductility and Tensile Strength
Elongation of as-plated copper shall be 18 percent minimum with a minimum tensile strength of 40 Kpsi. Testing shall be in accordance with IPC 650 Method 2.4.18.1. Samples shall be taken at minimum and maximum current plating densities. Sampling frequency shall be done at a statistically valid frequency to assure that the material properties are under statistical process control. Testing frequency shall not be less than once a month under any circumstance.

i. Process-Control Coupons
Process-control coupons shall be utilized to control the manufacturing processes of each panel. The number of in-process coupons shall be determined by statistical process control sampling requirements. Process-control coupons shall be included in the shipment of the deliverable boards only if requested on the purchase order.

j. Solder Plate Verification
Each board that is to be fused shall have a solder-plate coupon. Solder plate coupons shall be removed from the panel before fusing to verify solder thickness. Solder-plate coupons shall be included in the shipment of the deliverable parent boards. Alternate measuring techniques such as x–ray fluorescence maybe used provided the measurements are documented and retrievable within 72 hours of request.

k. Deliverable Coupons (Conformance Coupons)
Double-sided and multilayer printed wiring boards shall be produced with two deliverable A or B coupons per board. For small board sizes, two deliverable coupons per 150 square centimeters (24 square inches) of panel area shall be produced. Coupons suitable to monitor the processes involved shall be located on the panel in positions across the diagonal of each board. A single coupon located at the center area common to the inside corners of adjoining boards on a panel may be used as one of the required coupons for each of the adjoining boards. For example, for four large boards on a panel, a coupon at each of the four outside corners and a common coupon at the center, for a total of five coupons, are all that are required (see Figure 100-1 for preferred panel lay-ups). These deliverable coupons are in addition to the process-control coupons required for each panel. All coupons shall be completely processed at the same time as the deliverable boards. These coupons may be used for conformance testing.

l. Storage and Retrievability
All deliverable (conformance) coupons shall be stored and shall be retrievable within 72 hours of request for the time period specified by program/contract.

m. Marking
Each individual board and each set of quality conformance test circuit strips (as opposed to each individual coupon) shall be marked in accordance with the master drawing and MIL-STD-130 with the date code (as specified below), the traceability serial number, the part number, and the manufacturer's CAGE code. Coupon marking shall be the same as board marking and all deliverable coupons shall be individually serialized. The date code shall be formatted as follows:

Year	Day of year (from 1 January)
05	001

This date shall reflect the date of final copper plating.

n. Traceability
The board manufacturer shall establish and maintain forward and backward traceability for all boards. This traceability shall reflect the exact disposition of each board. Boards that are rejected shall also be included in the traceability records and the reason for rejection shall be recorded. Each quality conformance test circuitry shall be traceable to the production boards produced on the same panel. All separated individual coupons shall have their traceability maintained back to the quality conformance test circuitry. Traceability records shall include board and coupon positions on the panel.

o. Copper Plating Thickness
The minimum plating thickness in plated through holes shall be 0.0012 inch. Any copper thickness less than 0.001 inch shall be considered a void. Blind and buried vias connecting across more than three layers shall also comply with this requirement. This requirement does not apply to microvias.

p. Hot Air Leveling
PWBs shall only be hot air leveled once. The solder coating shall be homogeneous and completely cover the conductors with no pitting, no pinholes, or non-wet areas. Sidewalls of conductors need not be solder coated. Touch-up is permitted but is limited to no more than 5 percent of lands or pads. After hot air level processing (including cleaning), boards shall undergo ionic verification testing per IPC TM-650 2.3.25 on a 4.0 sampling basis per IPC 6012 Rev C Table 4-2. The contamination level shall not be greater than an equivalent of 1.56 µg/cm2 of sodium chloride.

q. Repair
Repairs shall not be allowed.

r. Cracks
No cracks in the copper foil or plating shall be permitted.

s. Exposed Fibers
Damage to the PWB surface that exposes fibers shall not be permitted.

3.2 Multilayer Printed Wiring Boards

a. Lamination Preparation
The surfaces of the copper on all inner layers using epoxy or polyimide materials to be laminated shall be treated or primed prior to lamination to improve the laminate bonding.

b. Distribution of Ground or Power Planes
Multilayer printed wiring boards shall be configured so as to equalize the distribution of conductive areas in a layer and the distribution of conductive areas among layers. Ground and power planes shall be balanced around the midpoint to maintain PWB flatness.

c. Inner layer Inspection
Prior to lamination all inner layers shall be 100 percent inspected for continuity and shorts, and visually inspected for correct line width and spacing.

3.3 Metal Core Boards. Metal core boards shall use core material in accordance with ANSI/IPC-CF-152 and this document. When metal core boards are used, the lateral dielectric spacing between the metal core and adjacent conducting surfaces shall pass the dielectric withstanding voltage test in accordance with IPC-TM-650, Method 2.5.7 except that the minimum voltage shall be 750 volts D.C. There shall be no flashover, arcing, breakdown, or leakage exceeding one microampere.

4. QUALITY ASSURANCE. Quality assurance provisions shall be in accordance with Section 4, General Requirements, of this document , the requirements of MIL-PRF-31032 (custom), MIL-PRF-55110G (Type 1 and 2) or IPC 6018 Class 3, and the following:

If the supplier is only certified to IPC 6018 Class 3, the contractor shall verify that the build documentation, in-process controls, qualification testing and construction review meet the program requirements.

4.1 In-process Controls. In-process controls shall be monitored to assure that the manufacturing process is in a state of statistical control for all the requirements specified.

a. Elongation and tensile strength of as-plated copper shall be tested at least once a month.

b. Inner layer Inspection
Prior to lamination, all inner layers shall be 100 percent inspected for continuity and shorts, and visually inspected for correct line width and spacing.

4.2 Lot Conformance Tests. Lot conformance tests shall be in accordance with Section 4, General Requirements, of this document, and the requirements of MIL-PRF-31032 /5 or /6, MIL-PRF-55110G (Type 1 and 2), or IPC 6018 Class 3, and the following:

a. A minimum of one as received and one thermal stress coupon per PWB shall be microsectioned and inspected. Coupons between PWBs may be used to represent contiguous PWBs. These coupons as well as all unsectioned coupons shall be delivered with the PWBs.

b. Electrical continuity and isolation testing is required on all PWBS except Type 1 and shall be performed in accordance with Section 4, General Requirements, of this document, and the requirements of MIL-PRF-31032 (/5 or /6), MIL-PRF55110G (Type 1and 2) or IPC 6018 Class 3.

c. Microsections shall be reviewed for inner layer separation before and after microetching.

4.3 Qualification Tests. The manufacturer shall be certified as a qualified manufacturer in accordance with the requirements of MIL-PRF-31032 (/5 or /6), MIL-PRF-55110G (Type 1and 2) or IPC 6018 Class 3. If the supplier is only certified to IPC 6018 Class 3, the contractor shall verify that the build documentation, in-process controls, qualification testing and construction review meet the program requirements. If the complexity of the PWB exceeds the standard qualification coupon in the specifications, a flight PWB shall be qualification tested and meet all the Group A and B requirements.

4.4 Lot Verification. For each design type and lot of multilayer PWBs, a flight PWB shall be microsectioned and meet the Plated-Through-Hole (PTH) requirements. The sections shall include all PTH diameters and blind buried vias from various areas of the PWB. The PWB, from the panel whose coupons indicate the thinnest acceptable copper plating thickness, shall be microsectioned, and thermally stressed to demonstrate compliance with PTH requirements. Note that a rejectable PWB from this panel may be used for lot verification provided that the defect is not related to PTH integrity. If any PWB section fails, the lot shall be rejected.

Any alternative lot verification approach shall require approval by the program PMBCB. The alternative approach shall require data that demonstrate, for a particular PWB design and fabrication facility, indisputable correlation between the PTH quality of the flight PWB and the test vehicle of the alternate approach used for lot verification. As a minimum this data shall demonstrate that:

a. The plating uniformity varies less than 10% between plating at the panel center and the coupon locations
b. The supplier process controls show lot-to-lot uniformity over time and process consistency within a lot
c. Any test vehicle used in the alternate approach reflects the PWB design including all plated through-hole and via types and PWB processing including all copper plating operations

5. REGISTERED (RELIABILITY SUSPECT) PMP shall include:

a. Microvias
b. Blind vias plated blind (i.e., not made by sequential lamination)
c. ENIG Electroless Nickel Immersion Gold requires special controls to reduce risk of black pad.

6. PROHIBITED PMP shall include:

a. Lead-free tin plating/coating in printed wiring boards (see Section 4, General Requirements, paragraph 4.3.3 of this document). Note: if tin is used as a metal etch resist, it shall be totally removed prior to the final finish application.

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SECTION 200
CAPACITORS, GENERAL

1. SCOPE. This section sets forth the requirements for capacitors used in space applications. Table 200-1 lists, by dielectric type, the capacitor styles and indicates the applicable section in this document where additional detailed requirements are set forth. All capacitors selected for the system application shall meet the requirements specified herein, unless otherwise approved by the program. Alternate approaches to meeting particular requirements shall be proven equivalent or more stringent than specified herein.

Table 200-1. Capacitor Styles Included in Section 200

Section	Dielectric Material	Reference Military Specification	Style
210	Ceramic, Multilayer	MIL-PRF-123 and DSCC Dwgs 06019 and 06022	CKS
211	Ceramic, Single Layer	MIL-PRF-49464	CPCR
215	Ceramic, High Voltage	MIL-PRF-49467	HVR
216	Ceramic, Stacked	MIL-PRF-49470 (T-Level)	SM
217	Ceramic Capacitor Arrays for Filter Connectors	---	---
230	Metallized Film	MIL-PRF-83421	CRH
232	Metallized Film (Low-Energy Applications) 2/	MIL-PRF-87217(A)	CHS
240	Glass 1/	MIL-PRF-23269	CYR
250	Mica 1/	MIL-PRF-87164A(3)	CMS
255	High Voltage Reconstituted Mica	---	---
260	Tantalum Foil 1/	MIL-PRF-39006	CLR
270	Solid Tantalum (Low Impedance Applications)	MIL-PRF-39003/10	CSS
275	Solid Tantalum Chip	MIL-PRF-55365	CWR
280	Wet Tantalum-Tantalum Case	MIL-PRF-39006/22 & /25 and DSCC Dwgs 06013 and 06014	CLR79, CLR81
		MIL-PRF-39006/30 & /31 and DSCC Dwgs 06015 and 06016	CLR90, CLR91

1/ Obsolete for new designs.

2. APPLICATION. Use of capacitors shall be in accordance with the requirements contained in the detailed sections of this document for each capacitor type. For additional capacitor use and information, see MIL-HDBK-198 and NASA TM X-64755.

2.1 Derating. The longevity, and hence the reliability, of a capacitor is improved by operating below its rated temperature limit and below its rated voltage, both AC and DC. Transient and ripple voltage shall be considered to prevent dielectric breakdown and excessive self-heat. Capacitors for AC applications require proper heat sinking to prevent excessive temperature rises, because, in most cases, the capacitor dissipation factor (DF) and leakage

current increase with temperature. The use of derating curves found in each section is described in paragraph 4.1.1 of Section 4, General Requirements, of this document. When capacitors are used in an AC application, the total of the peak AC voltage plus DC bias voltage shall not exceed the derating requirements specified.

2.2 DC Capacitors. Do not subject DC capacitors to AC applications or to high ripple current applications without checking to ensure satisfactory part operation in the particular environment of concern.

3. DESIGN AND CONSTRUCTION. See the detailed requirements section for each capacitor type.

4. QUALITY ASSURANCE. The quality assurance section contains the required verification and validation during the procurement process, screening tests, lot conformance tests, and qualification tests for each capacitor type. Alternate approaches to meeting particular requirements shall be proven equivalent or more stringent than those specified herein.

4.1 Production Lot. Unless otherwise specified, a production lot for capacitors shall consist of all the capacitors of a single capacitance and voltage rating of one design, from the same dielectric material batch with other raw materials coming from one lot number, and processed as a single lot through all manufacturing steps, to the same baseline, and identified with the same date and code designation. The lot may contain all capacitance tolerances for the nominal capacitance value.

4.2 Solder Dip/Retinning. See Section 4, General Requirements, paragraph 4.3.4.1 of this document.

4.3 Incoming Inspection DPA. The DPA shall be performed per MIL-STD-1580 except as modified herein.

4.3.1 External Lead/termination finishes. External lead/termination finishes shall comply with Section 4, General Requirements, paragraph 4.3.3 of this document. Gold plated leads or interconnects shall not be used in solder applications unless the gold is removed by pretinning.

5. REGISTERED (RELIABILITY SUSPECT) PMP shall include the following (see the detailed requirements section for each capacitor type not specified below):

a. Variable capacitors
b. CKR06 capacitors, ceramic dielectric, 1.0 µF/50V (Note: CKS06 1.0 µF/50V capacitors are available and should be used instead.)

6. PROHIBITED PMP. The following parts, part styles, and part types shall not be used.

a. CLR65 (MIL-PRF-39006/9) and CLR69 (MIL-PRF-39006/21) silver-cased wet tantalum slug capacitors
b. Wet tantalum electrolytic capacitors in metal-clad cases
c. All non-metallurgically bonded mica capacitors
d. Glass capacitor styles, CYR 41, 42, 43, 51, 52, 53
e. Aluminum electrolytic capacitors
f. Single-sealed CLR-style (MIL-PRF-39006) capacitors identified by their corresponding compression seal dash numbers
g. Paper
h. Paper/plastic
i. Metallized paper in molded cases
j. Capacitors using prohibited materials in their construction (see Section 4, General Requirements, paragraph 4.3.3 of this document)
k. Ceramic capacitors using base-metal electrodes (BME).

SECTION 210

MULTILAYER CERAMIC CAPACITORS

(MIL-PRF-123)

1. SCOPE. This section sets forth detailed requirements for fixed multilayer ceramic capacitors.

NOTE: Capacitors procured to DSCC Dwgs 06019 and 06022 already meet the design requirements, production lot definition, in-process inspection, Group A, Group B and qualification test requirements of this section and are considered standard. No additional in-process, Group A, Group B and qualification tests are required. However, all the other requirements of this section (e.g., derating, incoming inspection DPA, registered and prohibited PMP, etc.) shall apply.

2. APPLICATION

2.1 Derating. The voltage-derating factor for these capacitors shall be as follows:

ES_{NOM}	0.50 to +85 ºC, decreasing to 0.30 at +125 ºC
ES_{WC}	0.70 to +85 ºC, decreasing to 0.50 at +125 ºC

2.2 End-of-life Design Limits shall be:

	General Purpose BX (X7R)	Temperature Compensated BP (NP0)
Capacitance:	± 20 percent	± 1.25 percent or ± 0.75 pF, whichever is greater, or ± 1.25 percent for ultra low values
Insulation Resistance	50 percent of: initial limit	50 percent of initial limit

2.3 Mounting

2.3.1 Piezoelectric Concerns. Where avoidance of a significant piezoelectric output is critical to circuit performance, BP-type dielectric product shall be used in place of BX-type dielectric product. Piezoelectric output can also be minimized by mounting chips on their side or by using chips with a reduced length to width ratio.

2.3.2 Conductor Contact. In order to minimize part cracking, do not allow the capacitor termination to directly contact or come within 0.001 inch of the conductor pads on the substrate, i.e., solder/conductive adhesive fillet should provide a minimum 0.001 inch distance between capacitor termination and substrate/board metallization.

2.3.3 Capacitor Cracking. Ceramic capacitors are easily cracked when exposed to thermal or mechanical stresses. The assembly, manufacturing and rework processes need to be qualified and shown to produce quality solder joints without resulting in damage to thermal shock sensitive components. The manufacturers' detailed processing and handling recommendations shall be followed, especially those relating to hand and mass reflow soldering operations, including preheat ramp up rates and cool down rates. Hand soldering with soldering irons is strongly discouraged, but if used, under no circumstance shall a soldering iron contact the body or end cap of a ceramic capacitor, and the temperature change rates shall be controlled to prevent thermal shock. In addition, the PWB and the components shall be preheated to further reduce the thermal shock potential when hand soldering. Solder coating (tinning), except by the component manufacturer, shall not be done without PMPCB approval. Also, bare metal tweezers shall not be used to handle/pick-up ceramic chip capacitors which can induce cracks or chip-outs to edges or sides of the capacitor body.

When equipment containing ceramic capacitors is to be subjected to a range of temperature, the stresses resulting from a mismatch of coefficients of thermal expansion of all elements involved shall be accommodated.

3. DESIGN AND CONSTRUCTION. Design and construction shall be in accordance with the requirements of MIL-PRF-123.

4. QUALITY ASSURANCE. Quality assurance provisions shall be in accordance with Section 4, General Requirements, of this document and the following:

Section 210 CERAMIC CAPACITORS (CKS)

4.1 In-process Inspections. In-process inspections shall be in accordance with the requirements of MIL-PRF-123.

4.2 Group A Requirements. Group A requirements shall be in accordance with the requirements of MIL-PRF-123.

4.3 Group B Tests. Group B tests shall be in accordance with the requirements of MIL-PRF-123. All Group B tests shall be done on a production lot by production lot basis. If a chip manufacturing lot is segregated and formed into multiple production lots based on capacitance values (or capacitance tolerances), only one set of Group B samples may be tested. These samples shall be taken from the production lot which represents the highest capacitance value. This consideration only applies to unleaded/unstacked chip capacitors.

4.4 Qualification Tests. Qualification testing shall be in accordance with the requirements of MIL-PRF-123.

4.5 Sample and Data Retention. Sample and data retention for all manufacturing lots shall be in accordance with the requirements of MIL-PRF-123.

4.6 Incoming Inspection DPA. Incoming Inspection DPA shall be in accordance with MIL-STD-1580. All metal surfaces shall be verified for the absence of prohibited materials (e.g., pure tin, zinc, or cadmium).

5. REGISTERED (RELIABILITY SUSPECT) PMP shall include:

a. CKR06, 50 Volt rating, C > 0.47 microfarad (Note: CKS06 style capacitors >0.47 µF are available and acceptable.)

b. Dielectric thicknesses < 0.0008” (20.3 microns)

c. Large aspect (length/width) ratio >2:1

d. Variable devices

6. PROHIBITED PMP shall include:

a. Capacitors using prohibited materials in their construction (see Section 4, General Requirements, paragraph 4.3.3 of this document).

b. Capacitors using base-metal electrodes (BME).

SECTION 211

SINGLE LAYER CERAMIC CAPACITORS

(MIL-PRF-49464)

1. SCOPE. This section sets forth detailed requirements for fixed single layer Class I and Class II ceramic capacitors.

2. APPLICATION

2.1 Derating. The voltage-derating factor for these capacitors shall be as follows:

ES_{NOM}: 0.50 to +85 ºC, decreasing to 0.30 at +125 ºC
ES_{WC}: 0.70 to +85 ºC, decreasing to 0.50 at +125 ºC

2.2 End-of-life Design Limits shall be:

	General Purpose BX (X7R), Class II	Temperature Compensated BP (NP0), Class I
Capacitance:	± 20 percent	± 1.25 percent or ± 0.75 pF, whichever is greater, or ± 1.25 percent for ultra low values
Insulation Resistance	50 percent of initial limit	50 percent of initial limit

2.3 Mounting

2.3.1 Piezoelectric Concerns. Same as paragraph 2.3.1 of Section 210.

2.3.2 Capacitor Cracking. Same as paragraph 2.3.3 of Section 210.

3. DESIGN AND CONSTRUCTION

3.1 Requirements. Design and construction shall be in accordance with the requirements of MIL-PRF-49464 and the requirements of this document. Only Class I and Class II ceramic dielectrics shall be used.

4. QUALITY ASSURANCE. Quality assurance provisions shall be in accordance with the general requirements of Section 4 and the following:

4.1 In-process Controls. In-process controls shall be in accordance with the requirements of MIL-PRF-49464.

4.2 Group A Inspection. Group A Inspection shall be in accordance with the requirements of MIL-PRF-49464 with the following exception:

a. Visual inspection shall be performed on 100% of the lot.

b. Voltage conditioning shall be performed for a minimum of 168 hours, and a maximum of 264 hours, at 125 °C, +4 °C / -0 °C, and twice rated voltage. The voltage conditioning shall be terminated at any time during the 168 to 264-hour time interval in which failures (blown fuses or insulation resistance failures at 125 °C) meet the requirement that a maximum of one failure has occurred in the last 48 hours of testing. After completion of the exposure period, the following electrical tests shall be performed: Capacitance, dissipation factor, dielectric withstanding voltage, and insulation resistance at 25 °C and 125 °C. The manufacturer has the option of performing these electrical tests in any order except both insulation resistance measurements shall always be performed after dielectric withstanding voltage.

4.3 Group B Inspection. Group B Inspection shall be in accordance with the requirements of MIL-PRF-49464 with the following exceptions:

a. Subgroup 3 exceptions:

1. Thermal shock shall be performed on the life test samples prior to life test.

- Test conditions: MIL-STD-202, Test Condition A, except that in step 3, sample units shall be tested at +125 °C

- Number of Cycles: 100

2. The duration of life test shall be 1,000 hours.

b. Group B Inspection shall be performed only on the highest capacitance value within the same case size, voltage rating and using the same raw materials lot/batch, processed at the same time, on the same equipment and at the same facility.

4.4 Qualification Tests. Qualification testing shall be in accordance with the requirements of MIL-PRF-49464.

4.5 Sample and Data Retention. Sample and data retention for all manufacturing lots shall be maintained for a minimum of 10 years, or as specified by the procuring activity.

4.6 Incoming Inspection DPA. Incoming Inspection DPA shall be in accordance with MIL-STD-1580. All metal surfaces shall be verified for the absence of prohibited materials (e.g., pure tin, zinc, or cadmium).

5. REGISTERED (RELIABILITY SUSPECT) PMP

a. Large aspect (length/width) ratio >2:1

6. PROHIBITED PARTS LIST

a. Parts with pure tin, or >97% tin, coated leads/terminations (see Section 4, Paragraph 4.3.3)

b. Base-metal electrode or reduced ceramic oxide technology to manufacture parts.

c. Fully metallized designs (i.e., metallization all the way to the chip edges).

SECTION 215

CERAMIC CAPACITORS, HIGH VOLTAGE (HVR)

(MIL-PRF-49467)

1. SCOPE. This section sets forth the detailed requirements for high voltage encapsulated multilayer ceramic chip capacitors (HVR styles) up to 10,000 volts.

2. APPLICATION

2.1 Derating. Same as paragraph 2.1 of Section 210.

2.2 End-of-life Design Limits shall be:

	General Purpose BR or BZ	Temperature Compensated BP
Capacitance:	±20 percent	± 1.25 percent, or ± 0.75 pF, whichever is greater, or ± 1.25 percent for ultra low values
Insulation Resistance:	50 percent of initial limit	50 percent of initial limit

2.3 Mounting. Additional encapsulation is necessary in applications where the possibility of arcing between the leads of the capacitor, or the capacitor to another potential, could occur. Heat sinks on each lead and adequate preheating are required when these capacitors are installed or removed from circuits by soldering.

2.4 Piezoelectric Concerns. Same as paragraph 2.3.1 of Section 210.

2.5 Capacitor Cracking. Same as paragraph 2.3.3 of Section 210.

3. DESIGN AND CONSTRUCTION

3.1 Requirements. Design and construction shall be in accordance with the requirements of MIL-PRF-49467 and the requirements of this document.

3.2 Production Lot. A production lot shall be as defined in MIL-PRF-123.

3.3 Lead Attachment. Leads shall be attached to the ceramic chip body using high temperature solder with a minimum plastic point of 260ºC.

3.4 Encapsulation. Encapsulation type shall be carefully considered by the user regarding specific environmental requirements and the ceramic chip physical size. Conformally coated parts using the dip or fluidized bed process provide an adhesion to the ceramic body. However, severe thermal shock or temperature cycling may cause cracking due to thermal coefficient difference. True molded cases are prone to voids between the ceramic and the coating because there is no adhesion between the encapsulant and the ceramic. This condition may lead to corona failure on the surface of the ceramic. An epoxy cup with the capacitor back filled with a resilient material may be subject to internal solder joint damage during vibration.

4. QUALITY ASSURANCE. Quality assurance provisions shall be in accordance with Section 4, General Requirements, of this document and the following:

4.1 In-process Inspections. In-process inspections shall be in accordance with the requirements of MIL-PRF-123.

4.2 Group A Requirements. Group A Requirements shall be in accordance with the tests in MIL-PRF-49467 and Table 215-1. The total percent defective allowable for all the electrical tests of Subgroup 1 shall not exceed 5 percent. In addition, the reduced PDA specified in MIL-PRF-123 during the last 50 hours of voltage conditioning shall apply.

4.3 Group B Tests. Group B tests shall be in accordance with the tests in MIL-PRF-49467 and Table 215-2. All Group B tests shall be done on a production lot by production lot basis.

4.4 Qualification Tests. Qualification testing shall be in accordance with MIL-PRF-49467.

4.5 Sample and Data Retention. Sample and data retention for all manufacturing lots shall be in accordance with the requirements of MIL-PRF-123.

4.6 Incoming Inspection DPA. Incoming inspection DPA shall be in accordance with MIL-STD-1580. All metal surfaces shall be verified for the absence of prohibited materials (e.g., pure tin, zinc, or cadmium).

5. REGISTERED (RELIABILITY SUSPECT) PMP shall include:

a. Large Aspect Ratio Product
The length-to-width aspect ratio for these thicker ceramic capacitors shall not exceed 1.8 to 1.

b. Thin Dielectric Product
The maximum stress allowed between plates shall not exceed 120 volts/mil for BX dielectric or 200 volts/mil for BP dielectric.

6. PROHIBITED PMP shall include:

a. Capacitors using prohibited materials in their construction (see Section 4, General Requirements, paragraph 4.3.3 of this document).

b. Capacitors using base-metal electrodes (BME).

Table 215-1. Modifications to Group A of MIL-PRF-49467

MIL-PRF-49467	Modifications to the Methods, Requirements and Criteria of MIL-PRF-49467
Subgroup 1 Thermal Shock Voltage Conditioning 2/	 a. 20 cycles b. 168 hours minimum
Subgroup 4 l/ Solderability	

1/ Sample size shall be in accordance with MIL-PRF-49467.

2/ Reduced PDA during the last 50 hours of testing, as specified in MIL-PRF-123, shall apply. Overall PDA for electrical tests in Subgroup 1 shall not exceed 5 percent.

Table 215-2. Additions and Modifications to Group B OF MIL-PRF-49467

MIL-PRF-49467	Additions and Modifications to the Methods, Requirements and Criteria of MIL-PRF-49467
Subgroup 1 Thermal Shock Life Test	Sample size, test conditions (except voltage), and accept/reject criteria shall be per MIL-PRF-123 100 cycles 1,000 hours
Subgroup 2 1/ Voltage-temperature Limits Resistance to Soldering Heat Moisture Resistance Resistance to Solvents Terminal Strength	10 pieces, use the same samples for all tests, reject on 1

1/ Tests in MIL-PRF-49467 Group B inspection need not be repeated if already done on the lot.

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SECTION 216

STACKED CERAMIC CAPACITORS (SM)

(MIL-PRF-49470, T-LEVEL)

1. SCOPE. This section sets forth detailed requirements for T-level fixed stacked ceramic capacitors (SM styles).

2. APPLICATION

2.1 Derating. The voltage-derating factor for these capacitors shall be as follows:

ES_{NOM} = 0.50 to +85ºC, decreasing to 0.30 at +125ºC

ES_{WC} = 0.70 to +85ºC, decreasing to 0.50 at +125ºC

2.2 End-of-life Design Limits shall be:

	General Purpose BX (X7R)	Temperature Compensated BP (NP0)
Capacitance:	± 20 percent	± 1.25 percent or ± 0.75 pF, whichever is greater
Insulation Resistance:	50 percent of initial limit	50 percent of initial limit

2.3 Mounting. Same as in paragraph 2.3 of Section 210. Furthermore, these capacitors are physically large and heavy, and generally require additional staking during assembly to PWBs so their leads do not break, and the capacitors do not fly off the boards during shock or vibration. Care shall be taken to ensure that the staking compound used (if any) on these capacitors is compatible with the CTE of the ceramic dielectric to prevent cracking of the parts during thermal exposures.

Reflow soldering shall guarantee adequate preheating of a large mass of ceramic and shall adhere to the manufacturer's recommended temperature ramp-up and cool-down rates in order to prevent inducing cracks to the capacitor. Hand-soldering of stacked capacitors is not the preferred method for attaching these parts to boards or substrates. However, if hand soldering cannot be avoided, such as during rework, preheating of the stacks is mandatory prior to any soldering in order to prevent thermally shocking the parts. Temperature rise or temperature drop during preheat or cool down shall not exceed the requirements of the part manufacturer. The preheat temperature shall be within 50ºC of the peak temperature reached by the ceramic bodies (adjacent to the leads) during the soldering process.

2.3.1 High Vibration Environments. Potted assemblies are recommended for high vibration applications, since the parts can be epoxied to the board. Other configurations of encapsulated stacked capacitors have built-in flanges with screw holes to also allow for direct tie-downs to the board. If "strapping" the capacitor to the board is the chosen method of staking unencapsulated stacks, care should be taken not to chip the ceramic or apply undue pressure that can cause the ceramic to crack.

2.4 Handling

a. Leads of stacked capacitors shall not be dipped into a solder pot (to pre-tin, for example) without first properly preheating the stacks.

b. Solder joints shall not be touched with a soldering iron. If touch up is necessary, follow preheating and hand soldering recommendations above.

c. Do not deform leads or use excessive force to install parts. All lead cutting and forming operations shall be qualified.

d. Stacked capacitors shall be protectively packaged to prevent damage and should remain in the same packaging until installation.

Section 216 STACKED CERAMIC CAPACITORS (SM)

3. DESIGN AND CONSTRUCTION

3.1 Requirements. Design and construction shall be in accordance with the T-level requirements of MIL-PRF-49470.

4. QUALITY ASSURANCE. Quality assurance provisions shall be in accordance with Section 4, General Requirements, of this document and the following:

4.1 In-process Inspections. In-process inspections shall be in accordance with the T-level requirements of MIL-PRF-49470.

4.2 Group A Requirements. Group A requirements shall be in accordance with the T-level requirements of MIL-PRF-49470.

4.3 Group B Tests. Group B tests shall be in accordance with the T-level requirements of MIL-PRF-49470. Only subgroups 4 and 5b of Group B shall be done on a production lot by production lot basis for QPL T-level parts. All Group B tests shall be performed on a production lot by production basis for parts not procured to QPL T-level, or from a supplier that is not T-level qualified.

4.4 Qualification Tests. Qualification testing shall be in accordance with the T-level requirements of MIL-PRF-49470.

4.5 Sample and Data Retention. Sample and data retention for all manufacturing lots shall be in accordance with the T-level requirements of MIL-PRF-49470.

4.6 Incoming Inspection DPA. Incoming Inspection DPA shall be in accordance with MIL-STD-1580. All metal surfaces shall be verified for the absence of prohibited materials (e.g., pure tin, zinc, or cadmium).

5. REGISTERED (RELIABILITY SUSPECT) PMP shall include:

a. Dielectric thicknesses < 0.0008” (20.3 Microns)
b. Large aspect ratio (length/width) >2:1
c. Non-leaded stacked capacitors

6. PROHIBITED PMP shall include:

a. Capacitors using prohibited materials in their construction (see Section 4, General Requirements, paragraph 4.3.3 of this document).
b. Capacitors using base-metal electrodes (BME).

SECTION 217

CERAMIC CAPACITOR ARRAYS FOR FILTER CONNECTORS

1. SCOPE. This section sets forth detailed requirements for fixed ceramic capacitor arrays. These parts are fabricated using the same materials and many of the same design rules as multilayer ceramic capacitors. They are generally intended for use in multi-line, EMI filter circuits, and are typically found in filtered connectors. Two basic designs are employed: thick arrays which employ spring clips to maintain electrical connection to the feed thru contacts, and thinner arrays that are soldered to the feed thru contacts.

2. APPLICATION

2.1 Derating. Same as paragraph 2.1 of Section 210.

2.2 End-of-life Design Limits shall be:

	General Purpose BX (X7R)	Temperature Compensating BP (NP0)
Capacitance:	± 20 percent	± 1.25 percent or ± 0.75 pfd, whichever is greater
Insulation Resistance	50 percent of initial limit	50 percent of initial limit

2.3 Mounting. These are large, brittle parts. To prevent cracking, contact to the outside perimeter of the arrays shall not be a soldered interface. Electrical connection to the feed thru holes can be accomplished through soldered or spring contacts. However, spring contacts are not recommended for high vibration environments.

2.4 Piezoelectric Concerns. Where avoidance of a significant piezoelectric output is critical to circuit performance, BP-type dielectric products shall be used in place of BX.

2.5 Capacitor Cracking. Ceramic capacitors easily crack when exposed to thermal or mechanical stresses. Extreme care shall be taken to avoid excessive thermal stresses when tinning or soldering terminations, or when inserting clips into the feed thru holes. When higher assemblies containing ceramic capacitor arrays are to be subjected to a range of temperatures, the stresses resulting from a mismatch of coefficients of thermal expansion (CTE) of all elements involved (which can often cause cracking of the dielectric) shall be carefully considered and accommodated in all aspects of design, manufacturing and testing.

3. DESIGN AND CONSTRUCTION

3.1 Requirements. Design and construction shall be in accordance with the requirements of MIL-PRF-123 and the requirements of this document.

3.2 Design. Fringe capacitor designs meant to achieve low capacitance values using X7R material are prohibited. All designs shall feature internal electrodes.

3.3 Surface Passivation. When used in non-hermetic designs, array faces shall be covered with an insulating polymer coating. Metallic debris in the coating shall not be permitted. Voids in the coating may be permitted as long as the surfaces meet the criteria of 4.2 herein. Surface passivation shall always be employed for arrays rated at 500 volts dc or greater to prevent flashover during high humidity conditions.

4. QUALITY ASSURANCE. Quality assurance provisions shall be in accordance with Section 4, General Requirements, of this document and the following:

4.1 In-process Inspections. In-process inspections shall be in accordance with the requirements of MIL-PRF-123.

4.2 Group A Requirements. Group A requirements shall be in accordance with the requirements of Table 217-1. Group A testing is performed on 100 percent of the lot. (Due to the lack of fixturing for voltage conditioning at most array manufacturers, thermal cycling and voltage conditioning is often accomplished at the next level of assembly.)

4.3 Array Inspection. When arrays are inspected at a minimum of 10X magnification, the following inspection criteria shall be employed:

a. No ceramic cracks shall be permitted.

b. Chipouts on the top and bottom surfaces that expose electrode material or through which electrode material is visible shall be cause for rejection.

c. Crack-free chipouts on the circumference are acceptable if <0.010 inch in their widest dimension, or less than 1/3 any other feature, whichever is less. For example, a crack-free chipout shall not be greater than 1/3 the thickness of the array cover sheet, or 1/3 the distance between any two conductor surfaces, etc., or <0.010 inch, whichever is less. This assumes that the array cover sheet thickness has been predetermined through DPA. No chipout is allowed along the perimeter of the array that represents the active region.

d. Flaking and lifting of metallized surfaces shall not be permitted.

4.4 Supplier DPA. Supplier DPA shall be in accordance with the in-process DPA of MIL-PRF-123.

4.5 Group B Tests. Group B tests shall be in accordance with the requirements of Table 217-2. All Group B tests shall be done on a production lot by production lot basis.

4.6 Qualification Tests. Qualification testing shall be performed in the intended application per the requirements of Section 310.

4.7 Sample and Data Retention. Sample and data retention for all manufacturing lots shall be in accordance with the requirements of MIL-PRF-123.

4.8 Incoming Inspection DPA. Incoming Inspection DPA shall be in accordance with MIL-STD-1580. All metal surfaces shall be verified for the absence of prohibited materials (e.g., pure tin, zinc, or cadmium).

5. REGISTERED (RELIABILITY SUSPECT) PMP shall include:

a. Exposed uncoated silver terminations.

6. PROHIBITED PMP shall include:

a. Fringe capacitor designs to achieve low capacitance values using X7R material.

b. Parts using prohibited materials in their construction (see Section 4, General Requirements, paragraph 4.3.3 of this document).

c. Capacitors using base-metal electrodes (BME).

Section 217 CERAMIC CAPACITOR ARRAYS FOR FILTER CONNECTORS

Table 217-1. Group A Requirements

Inspection	Methods, Requirements and Criteria in accordance with MIL-PRF-123
Visual inspection Capacitance Dielectric withstanding voltage Insulation resistance at +25ºC and +125ºC	Section 4.3 herein

1/ Per the applicable paragraph of MIL-PRF-123.

Table 217-2. Group B Requirements

Test and Sequence	Methods, Requirements (including sample sizes) and Criteria in accordance with the Group B of MIL-PRF-123
Thermal shock Insulation Resistance 1000 hour life test Humidity, steady state, low voltage Voltage-Temperature Limits	

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SECTION 230

METALLIZED FILM CAPACITORS (CRH)

(MIL-PRF-83421)

1. SCOPE. This section sets forth the detailed requirements for fixed, metallized film capacitors (CRH style) for high-energy circuit applications. [Note: Worldwide production of electronics-grade polycarbonate films intended for sale to the open market has ceased since year 2000. Present production of metallized polycarbonate film capacitors is made from existing raw materials inventory. New or modified designs of space electronics hardware should consider eliminating or minimizing the use of polycarbonate capacitors for their inevitable obsolescence, or use alternate capacitor types.]

2. APPLICATION. Metallized polycarbonate capacitors are obsolete for new design.

2.1 Circuit Requirements. Metallized film capacitors meeting the requirements of this section shall not be used in circuits with less than 500 microjoules of energy available for clearing and shall not be used in circuits that would be degraded by voltage transients created by part clearing. For capacitor circuits with less than 500 microjoules of energy, or those sensitive to momentary capacitor breakdown, see Section 232.

2.2 Voltage Derating for Polycarbonate (PC) and Polyphenylene Sulfide (PPS), and Polypropylene (PP) Dielectrics. The voltage-derating factor for these capacitors shall be as follows:

	PC and PPS	PP
ES_{NOM}:	0.50 to +85ºC	0.50 to +70ºC
ES_{WC}:	0.65 to +85ºC	0.65 to +70ºC

2.3 Temperature Derating. Metallized PC or PPS capacitors shall be used to a maximum operating temperature of 85ºC, and PP capacitors shall be used to a maximum operating temperature of 70ºC.

2.4 End-of-life Design Limits shall be:

Capacitance:	± 2 percent of initial tolerance limits
Insulation Resistance:	30 percent degradation from initial minimum limit

2.5 Electrical Recommendations (Self-Healing and Clearing)

2.5.1 Metallized Film. Because the polymeric film used is very thin, pinholes exist. A model of self-healing is when the dielectric strength at a pinhole is not sufficient to withstand the voltage stress, such that a short develops (10-10,000 ohms range). However, high peak currents at the fault site can then cause a clearing action by vaporizing the metallization from around the hole, thereby clearing the short.

Two factors shall be considered relative to a clearing action:

a. The energy necessary to accomplish this clearing
b. Short duration transients (voltage drops) during the clearing

For aluminum electrode materials, the energy required for nominal clearing may range up to 100 microjoules. For application purposes, minimum circuit energy of 500 microjoules (five times the nominal) shall be available before these parts can be used.

2.5.2 Double-Wrap Capacitors. Capacitors made with an extra layer of non-metallized film have a low percentage of parts exhibiting shorting and clearing. Such parts may also have reduced AC current capabilities.

2.5.3 Contamination Shorts. All film-type capacitors (metallized film, single or double-wrap, and extended foil) can behave intermittently when operated under certain conditions. These effects, believed to be caused by ionic conditions or contamination within the capacitor enclosure, can cause spurious, random conduction when the capacitor is operated during temperature changes and where the total circuit energy is less than 500 microjoules. The resistance level for polycarbonate capacitors at +125ºC may vary from 1 to 10,000 megohms for capacitance values below 1.0 microfarad.

2.5.4 AC Applications. Any AC-rated capacitor can be used in an equivalent DC circuit. However, the converse is not true because of:

a. Internal heating due to dielectric and termination losses

b. AC corona inception

For high frequency AC applications (> 400 Hz), the equivalent series resistance (ESR) of each capacitor should be measured per MIL-PRF-83421 at 100 KHz or at a frequency approximately that of its intended use, whichever is higher. Those parts exhibiting increases in ESR greater than 5 percent or 5 milliohms, whichever is larger, shall be removed from the lot.

3. DESIGN AND CONSTRUCTION

3.1 Requirements. Design and construction shall be in accordance with the requirements of MIL-PRF-83421and the requirements of this document.

3.2 Film Cleaning. Film used in all style capacitors shall be room temperature vacuum baked prior to winding for 48 hours minimum to remove all contaminant residues.

3.3 Metallization. Deposited electrode metallization on the plastic film shall be a minimum of 99.9 percent aluminum. Aluminum alloys and other materials either have identified problems or unproven reliability.

3.4 Winding Installation. Windings installed in cases whose diameter is 0.312 inch or larger shall be wrapped or encapsulated prior to installation inside the case in order to prevent radial motion during shock or vibration.

3.5 Insulator Washer. An insulator washer shall be added between the babbit end metallization and glass-to-metal end seal on both ends. The babbit material contains a high percentage of tin, and the process of applying the babbit creates a surface morphology that is susceptible to whisker formation. Tin whiskers can short circuit the end metallization and end seal. Capacitors with case sizes ≤0.235 inch diameter shall use a tape wrap that completely covers the internal babbit end termination and shall use an epoxy potted internal construction identical to those manufactured per MIL-PRF-83421/06. Capacitors with case sizes >0.235 inch diameter shall contain an insulating washer between the babbit end metallization and the glass-to-metal end seal on both ends.

4. QUALITY ASSURANCE. Quality assurance provisions shall be in accordance with Section 4, General Requirements, of this document and the following:

4.1 Failure Level. Only failure rate level “S” parts with “H” designation shall be used.

4.2 In-process Controls. In-process controls shall be in accordance with the requirements of MIL-PRF-83421 and the following:

a. Internal visual examination (5X minimum) of the lead attachment to capacitor babbit (end metallization)
   - End spray coverage that does not provide at least 75 percent area contact to all winding turns.
   - Poor adhesion between end spray and element, or between end spray and external lead connection.

b. Axial push test to verify tight fit between element and case in order to avoid element movement when the capacitor is subjected to random vibration testing (not required for potted parts, or capacitors whose case diameter is <0.312 inch). Axial push test is an in-process test performed on a go-no-go basis by the assembly operator. The operator shall verify prior to sealing that the diameter of the capacitor is big enough to leave no gap between the case wall and the capacitor element. When the element is pushed in, it should not give.

4.3 Group A Requirements. Group A 100% screening (except where noted otherwise) shall be in accordance with the requirements of Table 230-1.

4.4 Group B Tests. Each lot offered for inspection under MIL-PRF-83421 shall be sampled for the Group B inspection of MIL-PRF-83421, which shall include the random vibration test for H-designated units.

4.5 Qualification Tests. Qualification testing shall be in accordance with the requirements of MIL-PRF-83421.

4.6 Incoming Inspection DPA. Incoming Inspection DPA shall be in accordance with MIL-STD-1580. All metal surfaces shall be verified for the absence of prohibited materials (e.g., pure tin, zinc, or cadmium).

5. REGISTERED (RELIABILITY SUSPECT) PMP shall include:

a. Devices manufactured with 2.0 or less microns polycarbonate film or 4.0 or less microns polypropylene film

b. Parts not vacuum baked for 48 hours to remove contaminant residues

c. Capacitor windings installed in 0.312 inch diameter, or larger, cases not wrapped or encapsulated to prevent radial motion during shock or vibration

d. Parts not metallized with 99.9 percent aluminum

6. PROHIBITED PMP shall include:

a. Capacitors using prohibited materials in their construction (see Section 4, General Requirements, paragraph 4.3.3 of this document).

b. Parts with no insulator between babbit terminations and end seals.

Table 230-1. Group A Requirements

MIL-PRF-83421	Modifications to the Methods, Requirements and Criteria of MIL-PRF-83421
Thermal Shock	a. MIL-STD-202, Method 107, condition B, 10 cycles, except: -55ºC to +100ºC for MIL-PRF-83421/1 & /2 -65ºC to +125ºC for MIL-PRF-83421/6
DC Burn-In	168 hours minimum at 1.4 x Vrated, +100ºC. For M83421/6 capacitors, 1.4 x Vrated and +125 ºC. Post-burn-in measurements shall consist of the electrical tests (DWV, IR at 25 ºC, Capacitance, DF and ESR) following seal, and in accordance with MIL-PRF-83421.
AC Burn-In/Conditioning	Additional for AC application only Post-DC burn-in ESR 48 hours minimum at +100ºC Max AC current, 120 percent of IAC rated at 40KHz V_{AC} (rms) shall not exceed 240 Vrms under any conditions Post-AC burn-in measurements shall consist of the electrical tests (DWV, IR at 25 ºC, Capacitance, DF and ESR) following seal, and in accordance with MIL-PRF-83421. ΔESR (post DC Burn-in to post AC Burn-in) shall be no greater than 5 percent or 5 milliohms, whichever is larger
Seal	
Visual and Mechanical Examination (External)	Sample size per MIL-PRF-83421.
X-ray	Per MIL-PRF-87217, or 360-degree view using real-time x-ray with similar resolution and accept/reject criteria as specified in MIL-PRF-87217.
Solderability	Sample size per MIL-PRF-83421.

SECTION 232

METALLIZED FILM CAPACITORS (CHS)

(MIL-PRF-87217A)

(OBSOLETE FOR NEW DESIGNS)

1. SCOPE. This section sets forth detailed requirements for fixed film metallized capacitors for low-energy circuits. [Note: Worldwide production of electronics-grade polycarbonate films intended for sale to the open market has ceased since year 2000. Present production of metallized polycarbonate film capacitors is made from existing raw materials inventory. New or modified designs of space electronics hardware should consider eliminating or minimizing the use of polycarbonate capacitors for their inevitable obsolescence, or use alternate capacitor types. In addition, there is no longer a qualified source for this type of capacitor. This section is being maintained to accommodate existing inventory and heritage hardware/designs.]

2. APPLICATION

2.1 Low-Energy Circuits. These capacitors can exhibit momentary breakdowns in low-energy applications. To ensure clearing of breakdowns, the circuit in which capacitors of 0.1 microfarads and greater capacitance value are intended for use, shall be capable of providing at least 100 microjoules of energy. Applications for these capacitors shall be limited to circuits that can provide the minimum energy and that are insensitive to momentary breakdowns/clearing actions.

2.2 Derating. Same as Paragraph 2.2 and 2.3 of Section 230 except parts shall not be used above +85ºC, or tested above +100ºC.

2.3 End-of-life Design Limits. Same as Paragraph 2.4 of Section 230.

2.4 Electrical Considerations. Same as Paragraph 2.5 of Section 230 except that the minimum clearing energy requirement is 100 microjoules.

3. DESIGN AND CONSTRUCTION

3.1 Requirements. Design and construction shall be in accordance with the requirements of MIL-PRF-87217 and the requirements of this document.

3.2 Insulator Washer. An insulator washer shall be added between the babbit end metallization and glass-to-metal end seal on both ends. The babbit material contains a high percentage of tin, and the process of applying the babbit creates a surface morphology that is susceptible to whisker formation. Tin whiskers can short circuit the end metallization and end seal. Capacitors with case sizes ≤0.235 inch diameter shall use a tape wrap that completely covers the internal babbit end termination and shall use an epoxy potted internal construction identical to those manufactured per MIL-PRF-83421/06. Capacitors with case sizes >0.235 inch diameter shall contain an insulating washer between the babbit end metallization and the glass-to-metal end seals on both ends.

4. QUALITY ASSURANCE. Quality assurance provisions shall be in accordance with Section 4, General Requirements, of this document and the following:

4.1 In-process Controls. In-process controls shall be in accordance with the requirements of MIL-PRF-87217.

4.2 Group A Requirements. Group A screening and testing shall be in accordance with the Group A requirements of MIL-PRF-87217 in the order shown.

4.3 Group B Tests. Each lot offered for inspection under MIL-PRF-87217 shall be sampled for the Group B inspection of MIL-PRF-83421, which shall include the random vibration test for H-designated units.

4.4 Qualification Tests. Qualification testing shall be in accordance with the requirements of MIL-PRF-83421, failure rate level “S” for H-designated parts.

Section 232 METALLIZED FILM CAPACITORS (CHS)

4.5 Incoming Inspection DPA. Incoming Inspection DPA shall be in accordance with MIL-STD-1580. All metal surfaces shall be verified for the absence of prohibited materials (e.g., pure tin, zinc, or cadmium).

5. REGISTERED (RELIABILITY SUSPECT) PMP shall be the same as paragraph 5 of Section 230.

6. PROHIBITED PMP shall include:

a. Capacitors using prohibited materials in their construction (see Section 4, General Requirements, paragraph 4.3.3 of this document).

b. Parts with no insulator between babbit terminations and end seals.

SECTION 240

GLASS DIELECTRIC CAPACITORS (CYR)

(MIL-PRF-23269)

(OBSOLETE FOR NEW DESIGNS)

1. SCOPE. This section sets forth detailed requirements for fixed glass capacitors. [Note: CYR style capacitors will soon be offered only as DLA dwg parts with screening but no qualification, or as commercial catalog items, instead of the fully certified MIL spec established reliability capacitors; hence these are not recommended for new designs. Glass capacitors have long been replaced by temperature-stable ceramic capacitors in most applications..]

2. APPLICATION

2.1 Derating. These glass capacitors shall be derated for voltage versus temperature in accordance with Figure 240-1.

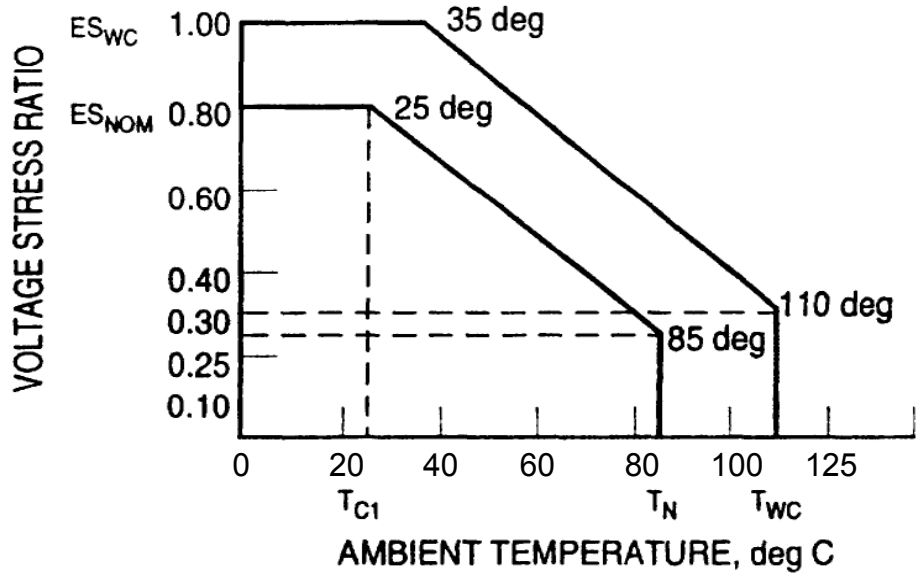

Figure 240-1. Voltage versus Temperature Derating for Glass Capacitors.

2.2 End-of-life Design Limits shall be:

Capacitance:	±0.5 percent of initial limits, or
	±0.5 pF, whichever is greater
Insulation Resistance:	500,000 megohms at +25ºC
	50,000 megohms at +125ºC
Dissipation Factor:	0.2 percent maximum

Section 240 GLASS DIELECTRIC CAPACITORS (CYR)

2.3 Electrical Considerations

2.3.1 General. Glass capacitors are relatively expensive, have poor volumetric efficiency, and have a practical capacitance range limited to 10,000 pF. However, the dielectric has near perfect properties (high IR, high Q, ultrastable capacitance, low dielectric absorption, and fixed TC), and thus these parts are useful in ultrastable and high-frequency circuit applications.

3. DESIGN AND CONSTRUCTION

3.1 Requirements. Design and construction shall be in accordance with the requirements of MIL-PRF-23269 and the requirements of this document.

3.1.1 Acceptable Styles

a. CYR 10
b. CYR 15
c. CYR 20
d. CYR 30

3.1.2 Failure Level. Failure rate level “S” only.

4. QUALITY ASSURANCE. Quality assurance provisions shall be in accordance with Section 4, General Requirements, of this document and the following:

4.1 In-process controls. In-process controls shall be in accordance with the requirements of MIL-PRF-23269.

4.2 Group A Requirements. Group A requirements shall be in accordance with the requirements of MIL-PRF-23269.

4.3 Group C Tests. Group C tests shall be in accordance with the requirements of MIL-PRF-23269. All non-“S” failure rate / non-QPL parts shall be Group C tested on a production lot by production lot basis, including a 1000-hour life test, in accordance with MIL-PRF-23269.

4.4 Qualification Tests. Qualification testing shall be in accordance with the requirements of MIL-PRF-23269.

4.5 Incoming Inspection DPA. Incoming Inspection shall be in accordance with MIL-STD-1580. All metal surfaces shall be verified for the absence of prohibited materials (e.g., pure tin, zinc, or cadmium).

5. REGISTERED (RELIABILITY SUSPECT) PMP. None

6. PROHIBITED PMP shall include:

a. Radial leaded devices: CYR41, CYR42, CYR43, CYR51, CYR52, and CYR53 styles
b. Capacitors using prohibited materials in their construction (see Section 4, General Requirements, paragraph 4.3.3 of this document).

SECTION 250

FIXED MICA CAPACITORS (CMS)

(MIL-PRF-87164A(3))

(OBSOLETE FOR NEW DESIGNS)

1. SCOPE. This section sets forth detailed requirements for fixed mica dielectric capacitors. [Note: There is no longer a qualified source for CMS style mica capacitors. This section is being maintained to cover existing inventory and heritage hardware/design. Since the Established Reliability (ER) version of these parts is prohibited for space application, new or modified designs of space electronics hardware shall use alternate capacitor types.]

2. APPLICATION

2.1 Derating. These capacitors shall be derated for voltage versus temperature in accordance with Figure 250-1.

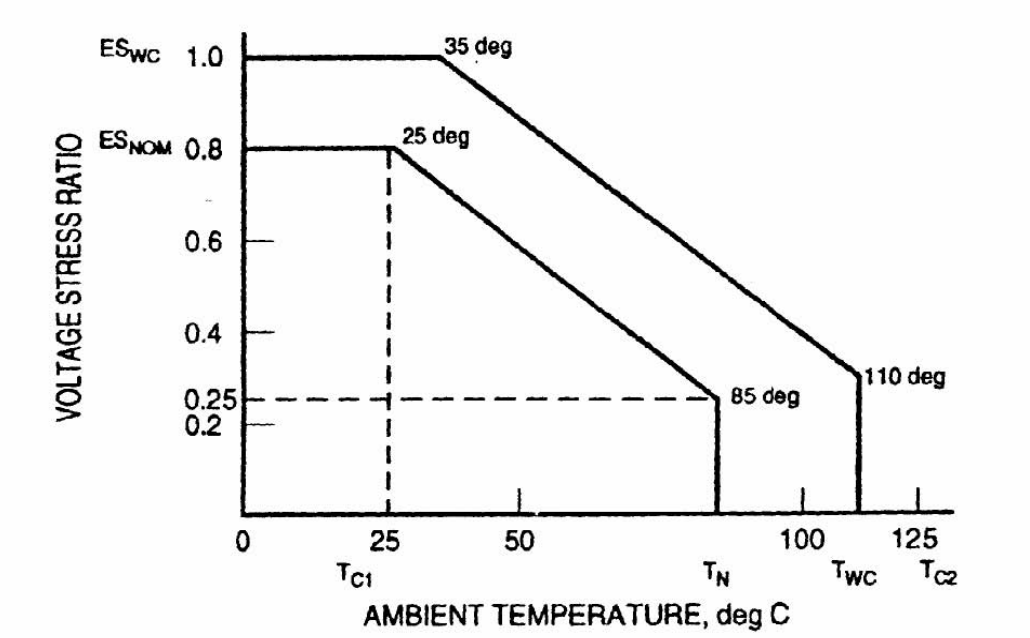

Figure 250-1. Voltage versus temperature derating for mica capacitors.

2.2 End-of-life Design Limits shall be:

Capacitance:	± 0.5 percent of initial limits
Insulation Resistance:	30 percent degradation from initial minimum limit

2.3 Electrical Considerations. This part exhibits electrical characteristics almost identical to those of the CYR style glass capacitors, except that the part is not hermetically sealed.

3. DESIGN AND CONSTRUCTION. Design and construction shall be in accordance with the requirements of MIL-PRF-87164A(3).

4. QUALITY ASSURANCE. Quality assurance provisions shall be in accordance with Section 4, General Requirements, of this document and the following:

Section 250 FIXED MICA CAPACITORS (CMS)

4.1 In-process Controls. In-process controls shall be in accordance with the requirements of MIL-PRF-87164A(3).

4.2 Group A Requirements. Group A requirements shall be in accordance with the requirements of MIL-PRF-87164A(3).

4.3 Group C Tests. Group C tests shall be in accordance with the requirements of MIL-PRF-87164A(3). All Group C tests shall be done on a production lot by production lot basis for non-QPL parts. Group C need not be performed on the same lot that went through qualification.

4.4 Qualification Tests. Qualification testing shall be in accordance with the requirements of MIL-PRF-87164A(3).

4.5 Incoming Inspection DPA. Incoming Inspection DPA shall be in accordance with MIL-STD-1580. All metal surfaces shall be verified for the absence of prohibited materials (e.g., pure tin, zinc, or cadmium).

5. REGISTERED (RELIABILITY SUSPECT) PMP. None

6. PROHIBITED PMP shall include:

a. All non-metallurgically bonded mica capacitors.

b. Capacitors using prohibited materials in their construction (see Section 4, General Requirements, paragraph 4.3.3 of this document).

SECTION 255

FIXED, HIGH-VOLTAGE, RECONSTITUTED MICA CAPACITORS

1. SCOPE. This section sets forth detailed requirements for vacuum encapsulated fixed value, reconstituted mica dielectric capacitors meant for high voltage applications.

2. APPLICATION

2.1 Derating. These capacitors shall be nominally voltage-derated to 50 percent of rated voltage up to a maximum case temperature of 110ºC.

2.2 End-of-life Design Limits shall be:

Capacitance:	± 0.5 percent of initial limits
Insulation Resistance:	30 percent degradation from initial minimum limit

2.3 Electrical Considerations. This part exhibits electrical characteristics almost identical to those of the CYR style glass capacitors.

3. DESIGN AND CONSTRUCTION. Design and construction shall be in accordance with the requirements of MIL-PRF-87164A(3), where applicable, and the requirements of this section. Voltage stress per mil of dielectric should not exceed 1500 V/mil by design. Capacitors shall be fully vacuum impregnated and encapsulated.

4. QUALITY ASSURANCE. Quality assurance provisions shall be in accordance with Section 4, General Requirements, of this document and the following:

4.1 In-process Controls. In-process controls shall be in accordance with the requirements of MIL-PRF-87164A(3).

4.2 Group A Requirements. Group A requirements shall be in accordance with the requirements of Table 255-I.

4.3 Group B Tests. Group B tests shall be in accordance with the requirements of Table 255-II. All Group B tests shall be done on a production lot by production lot basis.

4.4 Qualification Tests. Qualification testing shall be in accordance with the requirements of MIL-PRF-87164A(3).

4.5 Incoming Inspection DPA. Incoming Inspection DPA shall be in accordance with the general requirements of MIL-STD-1580. All metal surfaces shall be verified for the absence of prohibited materials (e.g., pure tin, zinc, or cadmium).

5. REGISTERED (RELIABILITY SUSPECT) PMP. None

6. PROHIBITED PMP shall include:

a. Capacitors using prohibited materials in their construction (see Section 4, General Requirements, paragraph 4.3.3 of this document).

b. Non-metallurgically bonded foil-to-lead terminals.

Section 255 FIXED, HIGH-VOLTAGE, RECONSTITUTED MICA CAPACITORS

Table 255-1. Group A Requirements

Inspection	Methods, Requirements and Criteria in accordance with MIL-PRF-87164A(3) unless otherwise specified	Sample Size
Subgroup 1	All capacitors shall meet the nominal requirements. PDA shall be 5 percent.	100 percent
Thermal Shock and Immersion		
High Voltage Stabilization	1.4X rated voltage	
Dielectric Withstanding Voltage		
Insulation Resistance (at 25ºC)		
Partial Discharge (Corona)	Corona inception voltage shall be measured in accordance with Appendix B of MIL-PRF-49467. Corona inception voltage (CIV) at the 100 picocoulomb (pC) level shall not be less than 0.42 times (dc rated V) rms volts.	
Capacitance	Capacitance values outside the initial limits by 1 percent or 1 pF, whichever is greater, shall be used for PDA lot rejection.	
Dissipation Factor	Dissipation factor greater than 130 percent of the initial limit shall be used for PDA lot rejection.	
Subgroup 2		100 percent
Visual And Mechanical Examination		
Subgroup 3		5 samples, 0 failures
Insulation Resistance at +25ºC and +125ºC		
Moisture Resistance		
Subgroup 4	The same samples can be used for resistance to solvents and solderability.	5 samples, 0 failures
Resistance to Solvents		
Solderability		

Table 255-2. Group B Requirements

Inspection	Methods, Requirements and Criteria in accordance with MIL-PRF-87164A(3) unless otherwise specified	Sample Size
Temperature Coefficient And Capacitance Drift		5 samples, 0 failures
Thermal Shock (25 Cycles) And Immersion		
Life test	2000 hours at 1.4X rated voltage and 125 ºC	
Partial Discharge (Corona)	Corona inception voltage shall be measured in accordance with Appendix B of MIL-PRF-49467. Corona inception voltage (CIV) at the 100 picocoulomb (pC) level shall not be less than 0.42 times (dc rated V) rms volts.	
Terminal Strength		

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SECTION 260

FIXED TANTALUM FOIL CAPACITORS (CLR 25, 27, 35, AND 37)

(MIL-PRF-39006)

(Obsolete For new designs)

1. SCOPE. This section sets forth detailed requirements for fixed tantalum-foil capacitors (CLR 25, 27, 35, and 37). [NOTE: There is no longer a supplier of wet tantalum foil capacitors. This section is maintained only to cover existing or heritage hardware/design.]

2. APPLICATION. MIL-PRF-39006 tantalum foil capacitors are not recommended for incorporation into new designs since there is no longer a manufacturer (domestic or offshore) for these products. There have been a number of failures involving misapplication of tantalum foil capacitors in excessive shock or vibration environments. Only “H” designated units shall be used for these application conditions, and only within the design capability and qualification of the parts.

Additionally, tantalum foil capacitors are not recommended for use at temperatures above 85ºC, due to the lack of evidence that these parts will perform reliably at the higher temperatures even with the voltage derated.

2.1 Derating. These capacitors shall be derated for voltage versus temperature in accordance with Figure 260-1.

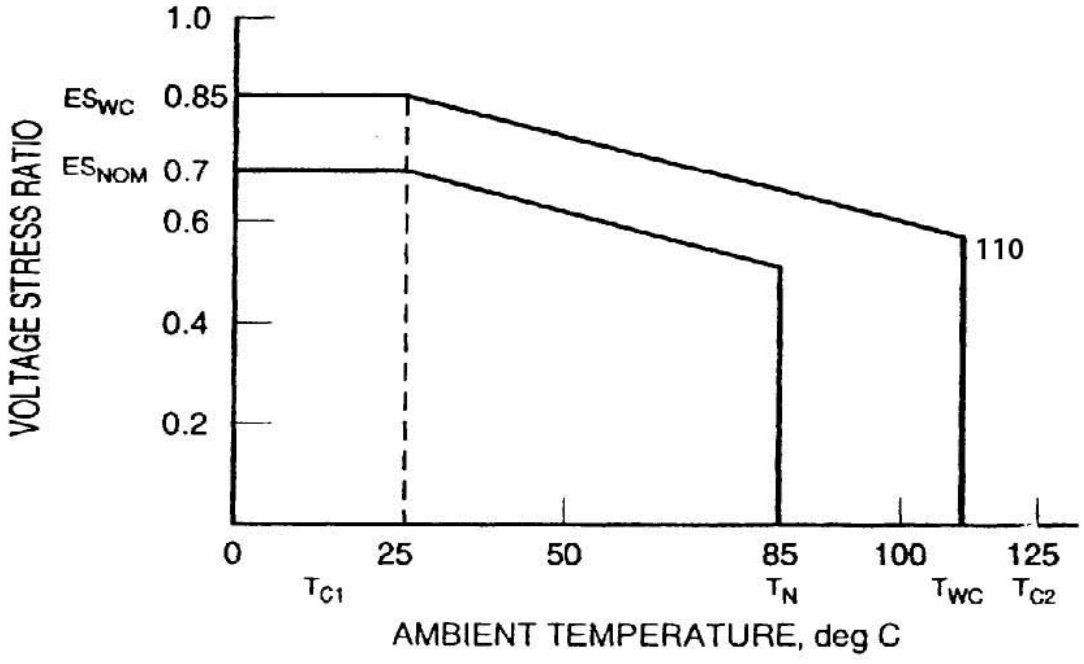

Figure 260-1. Voltage versus temperature derating for tantalum-foil capacitors.

2.2 End-of-life Design Limits shall be:

Capacitance:	± 15 percent of initial limits
Leakage Current:	130 percent of initial maximum limit

Section 260 FIXED TANTALUM FOIL CAPACITORS (CLR 25, 27, 35, and 37)

2.3 Electrical Considerations. The four capacitor styles listed are constructed with either plain (CLR 35 and 37) or etched-foil (CLR 25 and 27) tantalum dielectric, and are either polarized (CLR 25 and 35) or non-polarized (CLR 27 and 37). These capacitors are recommended for either medium or high voltage applications where high capacitance is required. The etched foil provides as much as 10 times the capacitance per unit area as the plain foil for a given size and is the most widely used. The plain foil is just as reliable as the etched foil, and in some cases, it may be more desirable because this style can withstand approximately 30 percent higher ripple currents, has better temperature coefficient characteristics, and has a lower dissipation factor. Parts shall not be used at temperatures above 85ºC.

2.3.1 Reverse Voltage. The polarized capacitor styles can only withstand a maximum of three volts DC reverse voltage at +85ºC. Under these conditions, the following changes in electrical characteristics are possible:

Capacitance:	±10 percent of initial value
Leakage Current:	125 percent of initial maximum limit

2.3.2 AC Ripple Voltage. The peak AC ripple voltage shall not exceed the DC voltage applied. The sum of the peak AC ripple voltage and any applied DC voltage shall not exceed the maximum DC voltage shown in Figure 260-1. Maximum ripple currents are given in literature of the various manufacturers.

2.3.3 Tantalum Capacitor Packs. (See NASA TM X-64755)

2.4 Potted Modules. The glass end seals are designed to withstand high internal pressure. When parts are potted, end seals shall be protected to withstand high external pressures that can result from curing of the encapsulant.

2.5 Vibration Environment. Only “H” designated tantalum foil capacitors shall be used in high shock or vibration environments, and only to within the design capability and qualification of the parts.

3. DESIGN AND CONSTRUCTION

3.1 Requirements. Design and construction shall be in accordance with the requirements of MIL-PRF-39006 and the requirements of this document.

3.2 Failure Level. Failure rate level shall be “R” or better.

4. QUALITY ASSURANCE. Quality assurance provisions shall be in accordance with Section 4, General Requirements, of this document and the following:

4.1 In-process Controls. In-process controls shall be in accordance with the requirements of MIL-PRF-39006.

4.2 Group A Requirements. Group A requirements shall be in accordance with the 100 percent screening requirements of MIL-PRF-39006 and Table 260-1.

4.3 Group B Tests. Group B tests shall be in accordance with the test requirements in MIL-PRF-39006 and Table 260-2. All Group B tests shall be done on a production lot by production lot basis.

4.4 Qualification Tests. Qualification testing shall be in accordance with the requirements of MIL-PRF-39006, Table I.

4.5 Incoming Inspection DPA. Incoming Inspection DPA shall be in accordance with MIL-STD-1580. All metal surfaces shall be verified for the absence of prohibited materials (e.g., pure tin, zinc, or cadmium).

5. REGISTERED (RELIABILITY SUSPECT) PMP shall include all tantalum foil capacitors.

6. PROHIBITED PMP shall include:

a. Capacitors using prohibited materials in their construction (see Section 4, General Requirements, paragraph 4.3.3 of this document).

Section 260 FIXED TANTALUM FOIL CAPACITORS (CLR 25, 27, 35, and 37)

Table 260-1. Modifications to Group A for Tantalum Foil Capacitors

MIL-PRF-39006	Modifications to the Methods, Requirements and Criteria of Group A Inspection in MIL-PRF-39006
Constant Voltage Conditioning	a. Maximum series resistance: 33 ohms b. Burn-in time of 168 hours at +85 ºC
Seal	a. Test conditions A and C
Radiographic Inspection	a. Per MSFC-STD-355; 2 conventional x-ray views 90 degrees apart, or 360-degree view using real-time x-ray (preferred). b. Case Size Max Width Incl. Telescoping Gl 0.3500” G2 0.4375” G3 0.7175” G4 1.4219” G5 2.0000”

Table 260-2. Group B Tests for Tantalum Foil Capacitors

MIL-PRF-39006	Modifications to the Methods, Requirements and Criteria of Group B in MIL-PRF-39006
Subgroup I	
Surge Voltage	
Life	Maximum series impedance: 33 ohms At +85ºC for 1000 hours
DC Leakage	At +25ºC and +85ºC
Subgroup 2	
Vibration (Random)	MIL-STD-202, Method 214, Test Condition II, K for 15 minutes each axis
Seal	Test conditions A and C

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SECTION 270

SOLID TANTALUM CAPACITORS (CSS)

(MIL-PRF-39003/10)

1. SCOPE. This section sets forth detailed requirements for fixed solid tantalum capacitors, styles CSS13 and CSS33. CSR13 and CSR33 are acceptable replacements for M39003/10 capacitors provided that the parts are (a) minimum "C" Weibull-graded, (b) surge current screened to the "C" or "F" option, and (c) conform to the lot definition requirements of M39003/10.

2. APPLICATION. All hermetic style solid tantalum capacitors shall be surge current test screened per M39003/10 prior to Weibull-grading, or per the "C" or "F" surge current option of MIL-PRF-39003.

2.1 Derating. These capacitors shall be derated for voltage versus temperature in accordance with Figure 270-1.

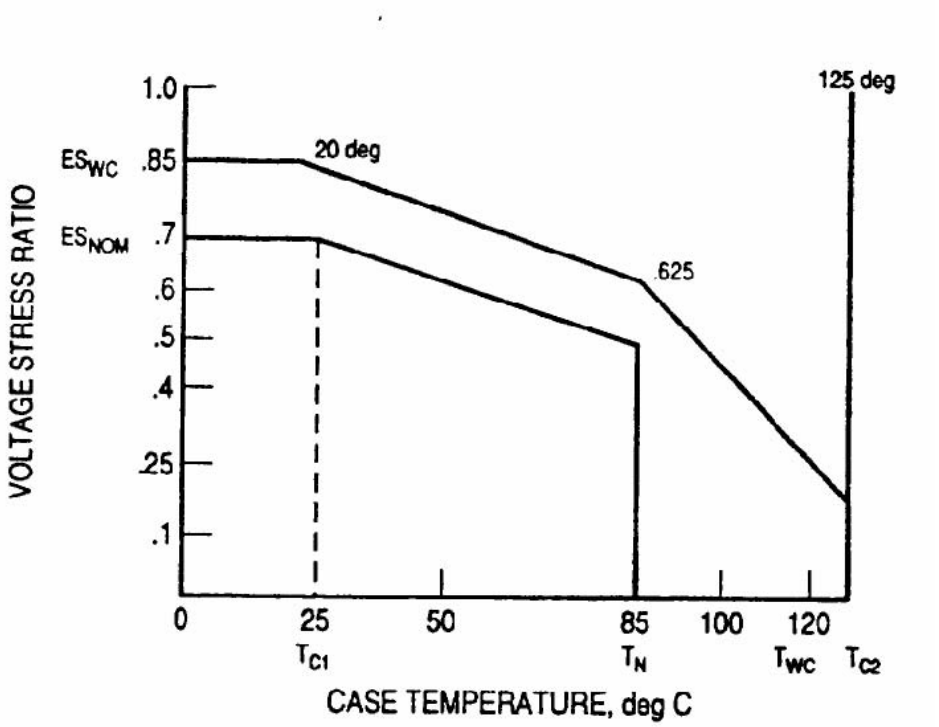

Figure 270-1. Voltage versus temperature derating for solid tantalum capacitors.

2.2 End-of-life Design Limits shall be:

Capacitance:	±10 percent of initial limits
Leakage Current:	200 percent of initial maximum limit

2.3 Allowable In-rush Currents. A circuit impedance of at least 1 ohm per volt, or an equivalent circuit that limits the in-rush current to 1 Amp, shall be used in all circuits containing these parts to control turn-on and peak current surges. Where end-item design goals preclude achieving this, the additional requirements in 2.3.1 and 2.3.2 shall apply:

2.3.1 Circuit impedance less than 1.0 ohm per volt but greater than 0.1 ohm per volt. These capacitors shall be voltage derated to a maximum use voltage of 40 percent V_{rated} from 0ºC - 85ºC. Polarized CSR style capacitors shall be 100 percent surge current screened to the option C requirements of MIL-PRF-39003. [Note: CSS capacitors already come with the equivalent option C surge current test as part of the M39003/10 requirements.]

2.3.2 Circuit impedance less than 0.1 ohm per volt. These capacitors shall be voltage derated to a maximum use voltage of 40 percent V_{rated} from 0ºC - 85ºC, and shall receive additional screening per Table 270-1.

2.4 Mounting. These parts are polarized and care shall be taken to ensure installation with the correct polarity.

3. DESIGN AND CONSTRUCTION

3.1 Requirements. Design and construction shall be in accordance with the requirements of MIL-PRF-39003/10 and the requirements of this document.

3.2 Failure Level. Weibull failure rate level shall be "C" minimum

3.3 Voltage Ratings. These solid tantalum capacitors shall be designed with a DC rated voltage of 75 volts or less, because parts with higher voltage ratings require thicker dielectrics, which contain more impurities, hence, more breakdown sites.

4. QUALITY ASSURANCE. Quality assurance provisions shall be in accordance with Section 4, General Requirements, of this document and the following:

4.1 In-process Controls. In-process controls shall be in accordance with the requirements of MIL-PRF-39003/10.

4.2 Group A Requirements. Group A Requirements shall be in accordance with the requirements of MIL-PRF-39003/10.

4.3 Group B Tests. Group B tests not required.

4.4 Qualification Tests. Qualification testing shall be in accordance with the requirements of MIL-PRF-39003/10.

4.5 Incoming Inspection DPA. Incoming inspection DPA shall be in accordance with MIL-STD-1580 except that tubelet fill shall be per MIL-PRF-39003. All metal surfaces shall be verified for the absence of prohibited materials (e.g., pure tin, zinc, or cadmium).

5. REGISTERED (RELIABILITY SUSPECT) PMP shall include:

a. All solid tantalum capacitors with no surge current screening.
b. Capacitors used in applications with <1 ohm/volt series resistance without meeting the additional requirements of this section.
c. >75V rated capacitors

6. PROHIBITED PMP shall include:

a. Capacitors using prohibited materials in their construction (see Section 4, General Requirements, paragraph 4.3.3 of this document).

Table 270-1. Additional Tests When Source Impedance Is <0.1 Ω/Volt

Tests	Methods, Requirements and Criteria per MIL-PRF-39003
Group A	100 percent
1. Serialization	
2. Electrical measurements	
Capacitance	Read and record
DF	Read and record
DC Leakage	Read and record
ESR	Read and record
3. Surge Current	Option C per MIL-PRF-39003
4. Voltage conditioning	40 hours minimum at 1.1X, or 1.2X, or 1.3X of rated voltage (whichever is higher but still less than the original Weibull test voltage) and 85ºC
5. Electrical measurements	Repeat Step 2.
	Remove parts not meeting requirements of MIL-PRF-39003 and applicable “slash sheet.”
6. 3-Sigma Limit	Remove parts exhibiting DCL and ESR > 3 sigma of lot mean for DCL and ESR.
7. PDA calculation	5 percent total for Steps 3, 4 and 5.
Group B	Sample size of 22 pieces, 0 failure allowed
Surge Voltage	Per MIL-PRF-39003 except:
	10,000 cycles
	Test voltage = 40 percent of rated
	Maximum series resistance = 1 ohm

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SECTION 275
SOLID TANTALUM CHIP CAPACITORS (CWR)
(MIL-PRF-55365)

1. SCOPE. This section sets forth detailed requirements for CWR style fixed solid tantalum chip capacitors. Additional requirements, based on circuit impedance, are also specified. Only T-level 35V and 50V rated MIL-PRF-55365 capacitors shall be used. All non-QPL and non-MIL spec tantalum chip capacitors shall meet all the T-level requirements of MIL-PRF-55365 and the requirements herein.

2. APPLICATION. All chip style solid tantalum capacitors shall be surge current test screened per MIL-PRF-55365 option "C" prior to Weibull-grading.

2.1 Voltage Derating. These capacitors shall be voltage derated in accordance with Figure 270-1.

2.2 Allowable In-rush Currents. A minimum circuit impedance of 1 ohm per volt, or an equivalent circuit that limits the in-rush current to 1 Amp, or more shall be used in circuits containing solid tantalum chip capacitors. Where end-item design goals preclude achieving this, the additional requirements in 2.2.1 and 2.2.2 shall apply:

2.2.1 Circuit impedance less than 1.0 ohm per volt but greater than 0.1 ohm per volt. These capacitors shall be voltage derated to a maximum use voltage of 40 percent V_{rated} from 0ºC - 85ºC, and shall be 100 percent surge current screened to the option C requirements of MIL-PRF-55365.

2.2.2 Circuit impedance less than 0.1 ohm per volt. These capacitors shall be voltage derated to a maximum use voltage of 40 percent V_{rated} from 0ºC - 85ºC, and shall receive additional screening per Table 275-1.

2.3 End-of-life Design Limits shall be:

Capacitance:	±10 percent of initial limits
Leakage Current:	200 percent of initial maximum limit

2.4 Electrical Considerations. This part type is recommended where a high capacitance to volume ratio is required and where relatively high temperature coefficients of capacitance can be tolerated.

2.5 Moisture Sensitivity. Tantalum chip capacitors are either conformally coated or encased in molded epoxy. They are not hermetic, and are subject to moisture ingress if used in humid environments. Such exposure may result in premature catastrophic failures.

2.6 Combustible Environments. Tantalum chip capacitors can ignite during a catastrophic shorting event, and will sustain combustion for as long as oxygen is available in the MnO_2 electrolyte. Such events can cause extensive burn damage to surrounding components or the board the capacitor sits on. For this reason, use of these capacitors in highly combustible environments is not recommended.

3. DESIGN AND CONSTRUCTION

3.1 Requirements. Design and construction shall be in accordance with the requirements of MIL-PRF-55365 and the requirements of this document.

3.2 Failure Rate Level. Weibull failure rate level shall be "C" minimum, with "C" surge current option.

3.3 Production Lot. A production lot for solid tantalum chip capacitors shall consist of all the capacitors of a single nominal capacitance and voltage rating of one design, shall be processed as a single lot through all manufacturing steps on the same equipment and shall be identified with the same date and lot code designation. The lot may contain all available capacitance tolerances for the nominal capacitance value. In addition, the lot shall conform to the following:

a. The tantalum powder shall be traceable to the same lot (or batch) number and be from the same manufacturer

b. Lot numbers shall be assigned at anode formation but should provide for traceability to the anode pressing batch and tantalum powder batch used.

c. The anode shall be pressed in a continuous run on the same pressing machine. Further, it shall be sintered and temperature-processed as a complete batch (batches cannot be split during sintering or subsequent temperature conditioning).

d. The entire production lot shall be voltage-formed (at the same time and in the same tank), impregnated, and otherwise processed through final sealing as a complete production lot with all parts receiving identical processing at the same time.

4. QUALITY ASSURANCE. Quality assurance provisions shall be in accordance with Section 4, General Requirements, of this document and the following:

4.1 In-process Controls. In-process controls shall be in accordance with the requirements of MIL-PRF-55365.

4.2 Group A Requirements. Group A requirements shall be in accordance with the requirements of MIL-PRF-55365.

4.3 Group C Tests. Group C tests shall be in accordance with the requirements of MIL-PRF-55365.

4.4 Qualification Tests. Qualification testing shall be in accordance with the requirements of MIL-PRF-55365.

4.5 Incoming Inspection DPA. Incoming inspection DPA shall be in accordance with MIL-STD-1580, except the T-level criteria for cathode attach as specified in MIL-PRF-55365 shall apply. All metal surfaces shall be verified for the absence of prohibited materials (e.g., pure tin, zinc, or cadmium).

5. REGISTERED (RELIABILITY SUSPECT) PMP shall include:

a. The two highest capacitance values in the 35V and 50V ratings are more difficult to manufacture with the same quality and reliability as the lower capacitance values. Care shall be taken to ensure that the circuit design/functionality cannot be achieved with more reliably designed tantalum chip capacitors before considering the use of the highest capacitance value 35V and 50V parts. In addition, the application, design and quality assurance requirements shall not be tailored when using these capacitors.

b. Use of these capacitors in <1 ohm per volt impedance without surge current screening and the additional requirements of this section.

c. Conformally coated parts (Note: The molded tantalum chips are preferred since they are more robust in a manufacturing environment and are less likely to be damaged during handling and cleaning.)

6. PROHIBITED PMP shall include:

a. Capacitors using prohibited materials in their construction (see Section 4, General Requirements, paragraph 4.3.3 of this document).

Table 275-1. Additional Tests When Source Impedance Is <0.1 Ω/Volt 2/

Tests	Methods, Requirements and Criteria per MIL-PRF-55365
Group A	100 percent
1. Serialization	
2. Electrical measurements	
Capacitance	Read and record
DF	Read and record
DC Leakage	Read and record
ESR	Read and record
3. Surge Current	Option C per MIL-PRF-55365
4. Voltage conditioning	40 hours minimum at 1.1X, or 1.2X, or 1.3X of rated voltage (whichever is higher but still less than the original Weibull test voltage) and 85ºC
5. Electrical measurements	Repeat Step 2.
	Remove parts not meeting requirements of MIL-PRF-55365 and applicable “slash sheet.”
6. 3-Sigma Limit	Remove parts exhibiting DCL and ESR > 3 sigma of lot mean for DCL and ESR.
7. PDA calculation 1/	5 percent total for Steps 3, 4 and 5.
Group B	Sample size of 22 pieces, 0 failure allowed
Surge Current	Per MIL-PRF-55365 except:
	10,000 cycles at +85°C
	Test voltage = 40 percent of rated
	Maximum series resistance = 1 ohm + measured ESR
	Minimum peak current = $\geq$ 0.40 V_{rated} / (1.0Ω + measured ESR)
	Peak current transition ≤100 µS

1/ 20% Maximum PDA is allowed for CWRxx parts in the X case and any non-QPL MIL-PRF-55365 type product.

2/ For CWRxx parts in the X case and any non-QPL MIL-PRF-55365 type product, probability charts, or PMPCB approved alternate, demonstrating the post-Table 275-1, Group A Voltage Conditioning DCL distribution is equal to or better than the original post-Weibull DCL distribution are required as part of the data package.

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SECTION 280

FIXED TANTALUM-TANTALUM CAPACITOR, SINTERED WET SLUG, TANTALUM CASE (CLR79, CLR81, CLR90 & CLR91)

(MIL-PRF-39006/22, /25, /30 & /31)

1. SCOPE. This section sets forth detailed requirements for wet sintered tantalum slug capacitors in tantalum cases. Only “H” vibration qualified designs shall be used.

NOTE: Capacitors procured to DSCC Dwgs 06013, 06014, 06015 and 06016 already meet the production lot definition, in-process inspection, Group A, Group B and qualification test requirements of this section and are considered standard. No additional in-process, Group A, Group B and qualification tests are required. However, all the other requirements of this section (e.g., derating, incoming inspection DPA, registered and prohibited PMP, etc.) shall apply.

2. APPLICATION. These parts are low-impedance, polarized capacitors that are designed for insertion into a circuit with a specific physical orientation. There is some evidence that in circuits active during vibration or shock environments the parts can generate voltage spikes.

2.1 Derating. Parts shall be derated for voltage versus temperature in accordance with Figure 280-1.

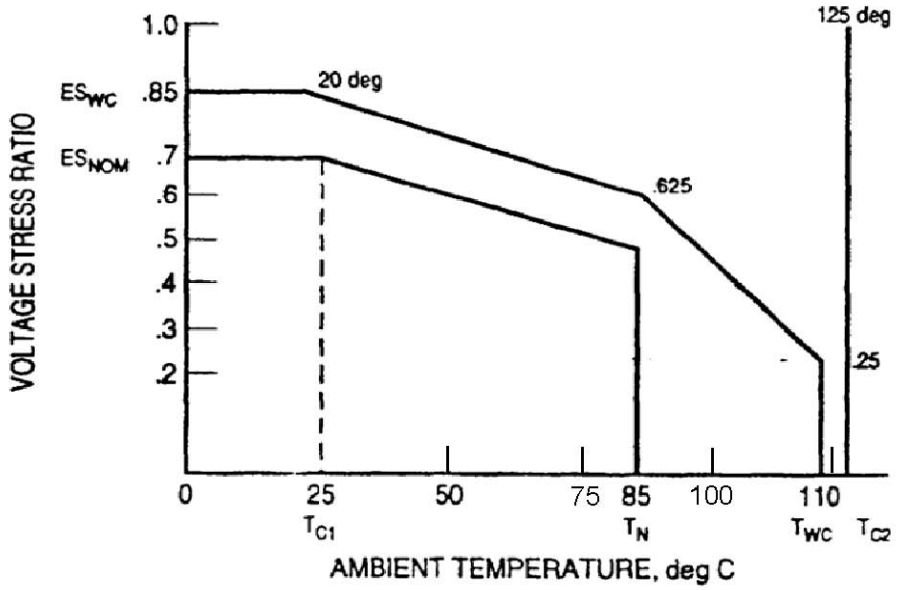

Figure 280-1. Voltage versus temperature derating for tantalum-tantalum (sintered wet slug) capacitor.

2.2 End-of-life Design Limits shall be:

Capacitance:	±10 percent of initial limits
Leakage Current:	130 percent of initial maximum limit

2.3 Electrical Considerations

2.3.1 ESR versus Frequency. Figure 280-2 is a plot of equivalent series resistance (ESR) versus frequency for various case sizes. If ESR vs. frequency is a parameter that is critical to the design application, consideration shall be given to performing read and record measurements of equivalent series resistance measurements during Group A testing. Parts exhibiting ESR characteristics outside those shown in Figure 280-2 shall not be used in flight hardware.

2.3.2 Vibration and Shock. Parts have been tested to 80 g sine vibration (0.06 double amplitude) from 10 to 2000 Hz for 1 1/2 hours in each orthogonal axis. Parts have been shocked to 100 Gs for 6 milliseconds with a saw tooth pulse. The "H" vibration-qualified option shall be used for all CLR79/81 and CLR90/91 capacitors that are used in spacecraft electronics. There are indications, however, that even "H" qualified parts may show intermittent shorting/spikes in these environments.

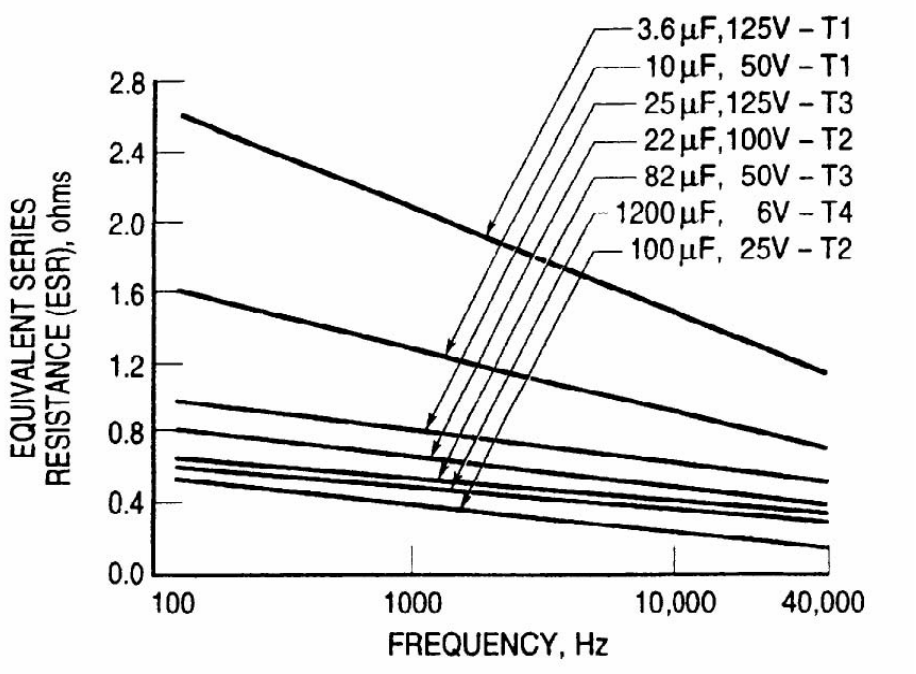

Figure 280-2. ESR versus ac frequency.

2.3.3 Reverse Voltage. Maximum reverse voltage shall be 3.0 VDC at +85ºC or 20 percent of the rated DC voltage, whichever is less.

2.3.4 Other. Detailed mechanical and electrical characteristics shall be as stated in MIL-PRF-39006/22, /25, /30 and /31.

3. DESIGN AND CONSTRUCTION

3.1 Requirements. Design and construction shall be in accordance with MIL-PRF-39006/22, /25, /30 and /31and the requirements of this document.

4. QUALITY ASSURANCE
Quality assurance provisions shall be in accordance with Section 4, General Requirements, of this document and MIL-PRF-39006.

4.1 Production Lot. A production lot shall consist of all the capacitors of a single nominal capacitance/voltage rating on one design. It shall be processed as a single lot through manufacturing steps, including sintering, electrochemical processing and final assembly on the same equipment, to the same revisions of the manufacturer's documentation, and identified with the same date and lot code designation.

4.2 In-process Control. In-process control shall be in accordance with MIL-PRF-39006

4.3 Group A Requirements. Group A requirements shall be in accordance with Table 280-1 and MIL-PRF-39006.

Section 280 FIXED, TANTALUM-TANTALUM CAPACITOR, SINTERED WET SLUG (CLR79/CLR81)

4.4 Group B Tests. Group B tests shall be in accordance with Table 280-2 and MIL-PRF-39006.

4.5 Qualification. Qualification shall be in accordance with MIL-PRF-39006.

4.6 Incoming Inspection DPA. Incoming inspection DPA shall be in accordance with MIL-STD-1580. All metal surfaces shall be verified for the absence of prohibited materials (e.g., pure tin, zinc, or cadmium).

5. REGISTERED (RELIABILITY SUSPECT) PMP. None

6. PROHIBITED PMP shall include:

a. Single-sealed CLR-style capacitors as identified by their compression seal dash numbers
b. Silver-cased, CLR wet slug types
c. Capacitors in metal-clad cases
d. Capacitors using prohibited materials in their construction (see Section 4, General Requirements, paragraph 4.3.3 of this document).

Table 280-1. Group A for Wet Tantalum Slug Capacitors

MIL-PRF-39006	Modifications to the Methods, Requirements and Criteria of Group A Inspection in MIL-PRF-39006
Subgroup 1	
Thermal Shock	10 cycles
Constant Voltage Conditioning	168 hours minimum. Maximum series resistance: 33 ohms
DC Leakage	At 25 ºC and 85 ºC
Capacitance	
DF	
Seal	Test conditions A or D, and C
Subgroup 2	
Mechanical examination (dimensions only)	
Subgroup 3	5 samples, 0 failures allowed
Solderability	Use of electrical failures from subgroup 1 is allowed.
Subgroup 4	13 samples, 0 failures allowed
Visual examination	Material, marking, workmanship

Table 280-2. Group B for Wet Tantalum Slug Capacitors

MIL-PRF-39006	Modifications to the Methods, Requirements and Criteria of Group B in MIL-PRF-39006
Subgroup I Stability at low and high temperatures	13 samples, 0 failures allowed
Subgroup 2 Thermal Shock Life DC Leakage CAP DF	10 samples, 0 failures allowed 30 cycles At +85ºC for 1000 hours At +25ºC and +85ºC
Subgroup 3 /1 Thermal Shock Mechanical Shock Vibration (Random) Moisture Resistance Reverse Voltage DC Leakage CAP DF Seal Visual and Mechanical Inspection	10 samples, 0 failures allowed 100 cycles 500 g, 0.5 sine (1 millisecond duration) MIL-STD-202, Method 214, Test Condition II, K for 15 minutes each axis, or at the maximum random vibration design limit of the part. At +25ºC and +85ºC Test Conditions A or D, and C

1/ Perform Subgroup 3 as part of qualification, or on every lot of non-M39006-QPL part/design.

SECTION 300

CONNECTORS

1. SCOPE. This section sets forth detailed requirements for space-qualified connectors. Additional information and guidance for the general use of connectors can be found in MIL-STD-1353B(4).

2. APPLICATION. The selection and use of connectors shall be in accordance with MIL-STD-1353B(4) and the requirements contained herein. Connector selection shall be based on operational requirements of the equipment and the following considerations:

a. Closed-entry-type socket contacts shall be used whenever available.

b. "Scoop-proof" type (e.g. MIL-DTL-38999 Series I, III, and IV) connectors shall be used whenever possible, especially when installation is difficult to perform or the process is not fully observable.

c. Redundant contacts shall be used in critical signal applications.

d. Guide devices shall be used for proper axial alignment and orientation. These devices shall not be used to carry current.

e. Strain relief for wires, harnesses, and cables shall be provided.

f. Protective covers shall be installed at all times until connectors are mated. If plastic covers are carbon loaded, the process for controlling the particulate slough shall be contained in the Contamination Control plan and approved by PMPCB. Plastic covers shall not contain topical antistats and shall be ESD resistive to the following extent:

(1) Surface Resistivity / Resistance. The surface resistivity shall be greater than 10^5 ohms per "square" and less than 10^{12} ohms per "square" in accordance with ASTM-D-257, MIL-PRF-81705, ANSI/EOS/ESD-S11.11-1993 or equivalent.

(2) Static Decay Time. The static decay rate shall be less than 2 seconds when tested in accordance with MIL-PRF-81705. The material shall retain this decay rate for four years minimum, when stored or used under conditions between 10 percent and 95 percent relative humidity.

(3) Non-corrosivity. The material shall be non-corrosive in accordance with FED-STD-101, Method 3005 or MIL-STD-3010, Method 3005.

g. Rear removable contacts shall be used wherever possible.

h. When connector savers are used on flight equipment, they shall be installed prior to electrical test. If removal is required, each removal/reinstallation shall be recorded in the mate/demate log. Connector savers shall be of equivalent design and construction to the flight connectors and be constructed of flight quality materials and finishes. The connector savers shall be purchased from suppliers qualified per the section herein. Connector savers do not need to meet the additional requirements contained in paragraph 4 herein. Connector savers shall be brightly colored so as to be easily identifiable.

i. Metal flight protective covers on the connectors shall be ESD/EMI/RFI design compatible as required by the spacecraft design.

j. Contact. Insertion/removal tools shall be as specified by the connector manufacturer.

k. 100 percent contact retention testing shall be required in accordance with NASA-STD-8739.4 for all connectors with rear-insertable contacts that are not subsequently potted.

l. All unused contact cavities shall not be filled with unwired contacts.

m. Non-RF connectors (e.g., rectangular or printed circuit board connectors) shall have a secondary method of mounting attachment to hardware and not be held in position by only the contact solder terminations.

n. MIL-DTL-83513 microminiature connectors and MIL-DTL-32139 nanominiature connectors pre-wired with cross-linked ethylene tetrafluoroethylene (XL-ETFE) (e.g. M22759/33) insulated wires shall not be completely sealed in containers/bags. See Section 1500 Wire and Cable, Paragraph 3.2 which addresses use of any XL-ETFE insulated wires/cable. It is recommended that plastic dust caps and/or polyethylene wrap be placed over stored connector shells and that containers/bags have vent holes.

o. Coaxial, Twinaxial, and Triaxial Connector application.

(1) SMP and SMPM intermatability. It is recommended that only the same manufacturer's SMP and SMPM connectors be mated to each other for Flight use to assure optimal connectors performance at high frequencies.

(2) Stress Relief. All attachments to the connector terminations shall provide for six directions of movement (±X, ±Y, ±Z) due to thermal cycling and vibration. The use of ribbons and butterflies to reduce stress is acceptable. On cabled connectors, when semi-rigid cable is used, the cable shall also be designed for six directions of movement. The use of 360-degree loops on semi-rigid cables is acceptable.

(3) Jam Nut Mounting. When jam nuts are used to mount a connector, after torquing the jam nut, both the jam nut and the hex portion of the connector body shall be spot bonded on two flats minimum to the equipment.

(4) Cable Bends. The start of any cable bends shall be a minimum of 0.100 inch from the rear of the connector.

(5) Threaded Connections. All threaded connections shall be fully tightened to the required torque value and then spot bonded to inhibit loosening. In lieu of spot bonding, lock-wire shall also be acceptable.

p. A mate/demate procedure and training are recommended for MIL-DTL-83513 microminiature connectors and MIL-DTL-24308 D-sub miniature connectors. Mating and demating of these connectors should only be performed by trained designated personnel. The use of alignment plugs (plug shells with only plastic inserts bonded in – no pin contacts installed) is encouraged in checking the alignment of exposed socket contact barrels in MIL-DTL-83513 connectors prior to mating. The use of alignment plugs shall not count as a mate/demate cycle to a Flight connector.

q. The contractor shall ensure that its intended torque values and staking practices are compatible with those of its subcontractors. For example, a contractor's coupling nut torque value could be higher than its subcontractor's jamnut torque value, and mating to the subcontractor's connector could result in overhauling (loosening) the jamnut.

2.1 Derating. Connectors shall be derated as follows:

a. The current shall be derated such that the average operating temperature of any connector will be less than the maximum rated temperature minus 25ºC.

b. A contact's worst-case steady state current shall not exceed 50 percent of the contact's current rating.

c. The worst-case steady state hot spot temperature shall not exceed 105°C unless it is shown through analysis and data that the hot spot temperature will not degrade the polymeric materials used in the construction, contact plating and/or the solder joints.

d. Connector worst-case steady state maximum working voltage shall be 25 percent of the connector dielectric withstanding voltage (DWV) rating at sea level.

3. DESIGN AND CONSTRUCTION

3.1 Requirements. Design and construction shall be in accordance with the requirements of the applicable specifications and the requirements of this document.

3.1.1 Vacuum Stability (Outgassing). Outgassing shall be in accordance with Section 4, General Requirements, paragraph 4.1.9 of this document.

3.1.2 Prohibited/Unacceptable Materials. Materials used in the design and construction shall not violate Section 4, General Requirements, paragraph 4.3.3 of this document.

3.1.3 Electrical Connectors. The following criteria shall apply.

a. Electroless nickel plating on aluminum for connector shells per 3.1.3.b (2) is preferred in nonhermetic applications. Passivated stainless steel per 3.1.3.b (3) herein for connector shells is preferred for hermetic applications.

b. Connector and Accessory Plating. Equivalent plating methods may be used with the approval of the Program PMPCB. Connectors and accessory hardware shall be plated and finished as follows:

(1) Brass Shells and Parts – Gold plated, 50 microinches minimum, in accordance with MIL-DTL-45204, Type I or II, Grade C, or ASTM-B-488, Type I or II, Code C, over electrodeposited nickel underplate, 50 microinches minimum, in accordance with QQ-N-290A or SAE-AMS-QQ-N-290. A copper plate or flash under the nickel underplate shall be acceptable. NASA GSFC S-311-P-4 and MIL-DTL-24308, Class M, (D-Subminiature rectangular connectors) shall use copper flash in lieu of nickel underplate to meet low magnetism requirements.

(2) Aluminum Alloy Shells and Parts – As a minimum, all aluminum alloy components shall be plated with at least 500 microinches of electroless nickel, in accordance with ASTM-B-733, Class 1, SAE-AMS-2404, MIL-C-26074, or SAE-AMS-C-26074. A double Zincate coating shall precede the nickel layer. When necessary to achieve low resistance shielding through a mated pair of connector shells (e.g. D-subminiature connectors), a minimum of 50 microinches of gold shall be plated over the nickel layer, in accordance with MIL-DTL-45204, Type I or II, Grade C, or ASTM-B-488, Type I or II, Code C.

(3) Corrosion Resistant Steel Parts – Passivated in accordance with QQ-P-35C, SAE-AMS-QQ-P-35, or an equivalent Specification or Standard document.

c. Contact Plating. Equivalent plating methods may be used with the approval of the Program PMPCB. The plating on non-significant surface (i.e. not in the electrical mating engagement area) in the inner diameter shall be of sufficient thickness to ensure plating continuity and protection. Unless used in applications where ferromagnetic materials should not be used, contact bodies and socket sleeves shall be plated and finished as follows:

(1) Crimp Type, Body – Gold plate, 50 microinches minimum, in accordance with MIL-DTL-45204, Type I or II, Grade C, or ASTM-B-488, Type I or II, Code C, over electrodeposited nickel underplate, 30 to 150 microinches, in accordance with QQ-N-290A or SAE-AMS-QQ-N-290. A copper flash may be put under the nickel underplate to improve plating adhesion.

(2) Solder Type, Body – Gold plate, 50 to 150 microinches, in accordance with MIL-DTL-45204, Type I or II, Grade C, or ASTM-B-488, Type I or II, Code C, over electrodeposited nickel underplate, 30 to 150 microinches, in accordance with QQ-N-290A or SAE-AMS-QQ-N-290. A copper flash may be put under the nickel underplate to improve plating adhesion.

(3) Solder Type, Body Pre-solder Coated - Gold plated contacts for Printed Wiring Board (PWB) terminations shall have solder areas hot solder (Sn50 to Sn95) dipped twice to de-gold areas. Gold plated contacts for PWB terminations may be selectively plated with electrodeposited tin-lead (Sn50 to Sn95), 100 to 300 microinches, in accordance with MIL-P-81728A or SAE-AMS-P-81728 over nickel underplate defined above. When used for de-golding, the solder dipping pot shall be assayed and charted to demonstrate that gold was less than 3 percent by weight during production. Solder in solder pots shall conform to purity requirements of NASA 8739.3 or IPC J-STD-001.

(4) Solder Type, Cups - Gold plated solder cups shall have solder areas de-golded with solder (Sn50 to Sn95) twice prior to a soldering operation. The cups should be filled and then wicked. Only Flux Types ROL0, ROL1, R, and RMA are approved.

(5) Corrosion Resistant Steel Socket Sleeves (Hoods) – Passivated in accordance with QQ-P-35C, SAE-AMS-QQ-P-35, or equivalent Specification or Standard document.

(6) Silver shall not be used as a contact overplate finish, or as an underplate.

d. Crimp Contacts. Crimp rear-release contacts are preferred for all multi-contact nonhermetic connectors. Crimp contacts shall not be used where hermeticity is achieved by encapsulation.

e. Crimp Tools. Crimping tools shall be capable of meeting the tensile strength requirements of NASA-STD-8739.4, Table 12-1.

f. Closed Entry Socket Contacts. Socket contacts shall be of the closed entry type. Exception shall be the protruding socket / recessed pin construction of the MIL-DTL-83513 microminiature and MIL-DTL-32139 nanominiature connectors.

g. Connector and contact manufacturers shall be able to provide forward and backward traceability to plating lots and raw material lots used in the connector construction.

3.1.4 Coaxial, Twinaxial, and Triaxial Connectors. The following criteria shall apply:

a. EMI Tight. EMI (electromagnetic interference) shall be mitigated as follows: All connectors and equipment shall be designed such that there are no exposed holes (openings) extending from the center conductor of the connector through the outside of the outer conductor. This applies after the connectors are mounted and fully mated on the equipment. A mating connector may cover the hole.

b. Contacts. The use of the center conductor of a cable as the mating-interface pin contact (male) for the connector is not acceptable. Only epoxy captivated contacts or interference fit captivated contacts shall be used.

c. Wrench Flats. The connector shall be provided with wrench flats, or equivalent, to prevent rotation during the connector mating/demating process.

d. Solder Cups. It is recommended that solder cups have a cross (bleed/vent) hole at the bottom to facilitate plating process and solderability.

e. Plating. Equivalent plating methods may be used with the approval of the Program PMPCB. The plating on non-significant surface (i.e. not in the electrical mating engagement area) in the inner diameter shall be of sufficient thickness to ensure plating continuity and protection.

(1) Ferrules, contacts, and brass metal parts shall be gold plated, 50 to 150 microinches, in accordance with MIL-DTL-45204, Type I or II, Grade C, or ASTM-B-488, Type I or II, Code C, over electrodeposited nickel underplate, 50 to 150 microinches, in accordance with QQ-N-290A or SAE-AMS-QQ-N-290.

(2) Solderable stainless steel (corrosion resistant steel) metal parts shall be gold plated, 30 to 150 microinches, in accordance with MIL-DTL-45204, Type I or II, Grade C, or ASTM-B-488, Type I or II, Code C, over nickel underplate defined above or copper underplate, 100 microinches minimum, in accordance with MIL-C-14550B or SAE-AMS-2418. A copper plate or flash under the nickel underplate shall be acceptable.

(3) All other stainless steel metal parts shall be passivated in accordance with QQ-P-35C, SAE-AMS-QQ-P-35, or equivalent Specification or Standard document. Coupling nut lockrings shall be unplated beryllium copper or passivated 302, 304, or 316 stainless steel.

3.2 Physical Configurations. Connectors, contacts, and accessories shall have physical configurations compliant with the requirements of this document, in addition to the physical configurations of the following:

a. The use of carbon steels shall be limited to the shells for solder mounting hermetic connectors.

b. MIL-DTL-5015, Series MS345X, Class L (Rear Release Types)

c. MIL-DTL-24308 Class D, K, or M (Rectangular, D-Sub), except that the shells of MIL-DTL-24308 type rectangular connectors shall be brass conforming to QQ-B-613, composition II or MIL-C-50D, or aluminum conforming to alloy UNS A96061, and Temper T6 of either ASTM-B-221 or ASTM-B-211

d. MIL-DTL-26482 Class L, Series 2 (Circular, Miniature, Quick Disconnect, Environment Resisting)

e. MIL-DTL-38999 Class G, H, or F (with processing for outgassing) (Circular, High Density)

f. MIL-PRF-39012 (Coaxial Connectors)

g. MIL-DTL-55302 (Printed Circuit Board Connectors)

h. MIL-DTL-83723, Class R, Series III (Circular, Environment Resisting)

i. MIL-DTL-83733 Class S (Rack and panel, Rectangular)

j. MIL-DTL-83513 Class M, Finish N (Rectangular Microminiature)

k. MIL-C-28754 Types IV and V (Backplane connectors)

l. MIL-PRF-31031 Class B, G, or H (Flexible and semirigid coaxial connectors)

m. MIL-PRF-49142 (Triaxial Connectors)

n. MIL-PRF-55339 (Coaxial Adapters)

o. MSFC-SPEC-40M38277 NASA Marshall Space Flight Center Connectors (NLS Series)

p. MSFC-SPEC-40M38298 NASA Marshall Space Flight Center Connectors (NBS Series)

q. MSFC-SPEC-40M39569 NASA Marshall Space Flight Center Connectors and Hardware (NB Series)

r. DSCC 94007 (SMP to SMP Adapter)

s. DSCC 94008 (0.047 and 0.086 Semirigid cable SMP connectors)

t. SAE-AS-39029 (Contacts)

u. SAE-AS-85049 Finish N (Backshells and Hardware)

v. SAE-AS-81703 Series 3, Class L (Circular, Miniature, Environment Resisting)

w. MIL-DTL-32139 Space Class S (Rectangular Nanominiature)

x. GSFC S-311-P-4 NASA Goddard Space Flight Center (Rectangular, D-Sub)

y. SSQ 21635 Marshall Space Flight Center (MSFC) (NATC Series)

z. GSFC S-311-P-822 (Compact PCI for space)

Note: Only space rated or upgraded to space rated connectors shall be selected. When space rated connectors are not available, upgrading may be performed to meet the requirements herein.

4. QUALITY ASSURANCE. Quality assurance provisions shall be in accordance with Section 4, General Requirements, of this document and the following:

If there is no applicable military slash sheet for the connector interface, such as for the SMP, the connector shall still meet the Group A and B inspection and qualification requirements of MIL-PRF-39012 for coaxial applications and MIL-PRF-49142 for twinaxial and triaxial applications, except the test criteria may be defined by the applicable DSCC drawing.

4.1 In-process Controls. In-process controls shall be in accordance with the requirements of the applicable military specification or aerospace standard. If the connectors are procured unassembled from the supplier, the assembly processes for building the flight connectors shall be verified by building connectors and testing them per the Groups A & B requirements of the applicable military specification. The flight connectors shall be subjected to the requirements of paragraph 4.2 and 4.3 herein.

4.2 Group A Requirements. Group A requirements shall be in accordance with the requirements of the applicable military specification or aerospace standard and the following:

a. 100 percent screening required for separation force of all socket contacts, MIL-DTL-83513 microminiature pin contacts for Class M, Finish N, and MIL-DTL-32139 nanominiature pin contacts for space, Class S.

b. 100 percent testing required for DWV and Insulation Resistance.

4.3 Group B Tests. Group B tests shall be in accordance with the Group B requirements of the applicable military specification or aerospace standard. Group B tests are not required when applicable military specification or aerospace standard does not require Group B as part of standard Quality Conformance Inspection. Example: MIL-DTL-32139 nanominiature connectors only require Group A for standard Quality Conformance Inspection.

4.4 Qualification Tests. Qualification testing shall be in accordance with the requirements of the applicable military specification or aerospace standard. During connector engagement/separation force testing per the applicable military specification, a minimum of ten (10) mate/demate cycles shall be performed on the connectors to condition the spring member. At the tenth cycle, the engagement/separation force shall be measured and shall meet the limits of the applicable military specification or aerospace standard.

4.5 Incoming Inspection DPA. Incoming inspection DPA shall be in accordance with MIL-STD-1580, Requirement 11 with the exception of a sample size of 3 devices per lot for all except micro-miniature connectors (MIL-DTL-83513), nanominature connectors (MIL-DTL-32139) and all non-MIL spec style/design connectors which shall have a minimum DPA sample size of 5 pieces. DPA is not required for connector savers. Plating thickness and adhesion shall be verified. All metal surfaces shall be verified for the absence of prohibited materials (see Section 4, General Requirements, paragraph 4.3.3 of this document).

5. REGISTERED (RELIABILITY SUSPECT) PMP shall include:

a. Ferromagnetic materials (e.g. nickel) used on RF connectors where intermodulation of signals would be a problem

b. Filtered pins

c. Dissimilar metal mates

d. External flat cable connectors

e. Multi-pin connectors without cavity sealing plugs in unused contact cavities of environmental connectors (e.g. those that have silicone or fluorosilicone grommets, reference NASA-STD-8739.4).

f. Soldered terminations of coaxial semi-rigid cables using other than high temperature solder for the internal construction.

g. Compact PCI connector except GSFC S-311-P-822

h. Gold over copper plating schemes operated at temperatures in excess of 150ºC in non-vacuum environments. This will cause the copper to migrate through the gold finish resulting in corrosion.

i. Power connectors that carry both primary and redundant lines within the same connector.

j. Compliant pin (press fit) contacts into printed wiring board (PWB) holes

k. Blind mating (Modules, PWB daughterboards to motherboards, etc.) with standard MIL-DTL-83513 microminiature connectors and standard MIL-DTL-32139 nanominiature connectors which are not scoop-proof design, which can damage the exposed socket contact mating barrels damaging the mating pin contacts. Blind mating connectors shall be accomplished by use of long jackscrews (half turns alternating mate/demate) or by use of long guide pins to bring connector shells together before contacts mate. Blind mating could also be accomplished with modified longer connector shells (e.g. “scoop-proof) allowing the shells to engage/align before the contacts mate.

6. PROHIBITED PMP shall include:

a. Connectors using prohibited materials in their construction and plating (see Section 4, General Requirements, paragraph 4.3.3 of this document)

b. Non-captivated RF connector contacts

c. Silver contact overplate or underplate

d. Wire wrap contacts

e. RF cable assemblies using the cable solid center conductor as the mating-interface pin-contact in the connector

f. Plastic composite connectors exposed to atomic oxygen environment

g. Insulation Displacement Connection (IDC) wire terminations

h. Lockwashers (split, internal tooth, external tooth, etc.). Lockwashers are normally supplied with jackpost hardware kits and should be discarded.

i. Lubricants used on electrical contacts

j. Open barrel crimp-contact terminations except for MIL-DTL-83513 microminiature and MIL-DTL-32139 nanominiature contacts, which are crimped and installed into connectors by QPL manufacturers. [Note: Open barrel contacts which are welded/brazed (closed barrel) are not prohibited.] This does not apply to seamless crimp barrels.

k. Card edge connectors which use PWB pads (lands) as contacts

l. E-clips, C-clips, or snap rings for jackscrew hardware, on space-flight connectors

m. Crimping solder-dipped or tinned stranded or solid conductor wiring

n. RTV (Room Temperature Vulcanizing) silicone compounds which are one part acetic acid cure.

o. Polyvinylchloride (PVC)

p. Polyamide (nylon) connector insert material and cable ties

q. Crimping to solid conductors except for MIL-DTL-83513 microminiature and MIL-DTL-32139 nanominiature contacts, which are crimped and installed into connectors by QPL manufacturers.

r. Fuzz buttons

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SECTION 310

CONNECTORS, FILTERED

1. SCOPE. This section sets forth detailed requirements for space-qualified connectors containing filter elements. Filter elements may include capacitors, inductors, resistors and diodes. Additional information and guidance for the general use of connectors can be found in Section 300 and in MIL-STD-1353B(4) (CANCELED).

2. APPLICATION. The selection and use of connectors shall be in accordance with Section 300 herein.

2.1 Derating. Filtered connectors shall be derated as follows:

a. The current shall be derated such that the temperature of any connector will be less than the maximum rated connector temperature minus 25ºC or the maximum derated temperature of any individual filter element, whichever is lower.

b. In no case shall this current exceed 50 percent of the rated current for the contact.

c. The voltage across ceramic capacitor elements shall be derated according to the requirements of Section 210.

d. Resistors shall be derated according to the provisions of the applicable resistor section in this document.

e. Diodes shall be derated according to the applicable provisions of Section 1400.

2.2 Hot Spot Temperature. The requirements of Section 300 shall apply. In addition, the temperature of individual components installed within the connector shall not exceed their maximum derated temperature for that device.

2.3 End-of-life Design Limits. The end of life design limits shall be according to the requirements of the applicable section herein for the specific filter element.

2.4 Aging Sensitivity. Filtered connectors contain circuit elements (e.g., capacitors) that exhibit aging effects. In the case of certain capacitor dielectric formulations (e.g., BX/X7R ceramic), aging can result in a capacitance decrease over time under bias. Effects specific to each component type are described in the applicable section within this document.

3. DESIGN AND CONSTRUCTION

3.1 Requirements. Design and construction shall be in accordance with the requirements of the applicable filtered connector specification and the requirements of this document.

3.1.1 Electrical Connectors. The following criteria shall apply:

a. Passivated stainless steel per 3.1.1.b (3) in Section 300 herein for connector shells is preferred for hermetic applications. Electroless nickel plated aluminum for connector shells is preferred in non-hermetic applications. Connectors and contacts shall meet the plating requirements of Section 300.

b. Silver shall not be used as a contact overplate finish or as an underplate.

c. All organic materials used in the manufacture of connectors, connector accessories, and flight protective caps shall meet the outgassing requirements specified in Section 4, General Requirements, paragraph 4.1.9, of this document .

d. Solder contacts with potted solder cups or PWB leads are recommended. Connector saver designs which incorporate integral mating contacts on both mating interfaces are also recommended.

e. Nickel or other ferromagnetic materials shall not be used where intermodulation of signals would be a problem.

f. When stainless steel is used, verification testing is required to ensure that any intermodulation of signals is acceptable.

g. Designs containing ferrite beads (e.g., pi filter configuration) that are utilized in high vibration environments shall employ approved RTV or conformally coated ferrites to minimize the dust generated by the motion of the ferrites against other circuit elements.

h. For ceramic arrays utilizing soldered contacts, the connector assembly processes shall allow for thorough cleaning of both faces of the array such that residual flux is not an issue and in order to prevent any surface shorting that may occur as a result.

i. Only high-temperature solder (e.g. Sn96/Ag4) shall be used when attaching de-golded contact leads to non-gold-plated planar array plated thru holes

j. Gold friendly solder (e.g. In50Pb50) shall be used on gold plated areas which cannot be de-golded prior to soldering.

k. Only Flux Types ROL0, ROL1, R, and RMA are approved for use on these connectors.

3.1.2 Physical Configurations. The following connector styles are commonly customizable to include various filter designs:

a. MIL-DTL-24308 (Rectangular, D-Subminiature)

b. MIL-DTL-38999 (Circular, High Density)

c. MIL- PRF-39012 (Coaxial Connectors)

d. MIL-DTL-83513 (Rectangular Microminiature)

3.2 Torquing and Staking. Torquing and staking requirements shall be in accordance with Section 300, paragraph 2.q.

4. QUALITY ASSURANCE. Quality assurance provisions shall be in accordance with Section 4, General Requirements, of this document and the following:

4.1 In-process Controls. In-process controls shall be in accordance with both the Class S (T where available) requirements of the applicable military specifications for both the connector interface and the individual filter elements. Individual elements such as diodes, capacitors, etc. shall be processed as described elsewhere in this document for Class S components prior to being installed into the connector. Ceramic capacitor arrays shall be procured to the requirements specified in Section 217 herein. Pre-encapsulation Source Inspection is recommended on 100 percent of the filter arrays/boards prior to assembly into connector shells, and should include visual inspection of all visible solder joints, cleanliness, dimensions and other workmanship requirements.

4.2 Group A Requirements. Group A testing is 100 percent screening performed at the connector level, which shall include 100 percent testing for separation force of all socket contacts, MIL-DTL-83513 microminiature pin contacts. Group A requirements shall be tailored based on the applicable Class S requirements in this document for the specific connector filter design. For example, connectors using ceramic capacitor elements shall undergo the Group A testing per the Class S requirements of MIL-PRF-28861 (see Table 310-1). Transient suppressor designs containing diodes shall undergo the Group A requirements per Section 1400 for Class S.

4.3 Group B Tests. Group B tests shall be tailored in accordance with the requirements for the specific filter design and the specific connector interface. As a minimum, Group B testing of connectors using ceramic capacitor elements shall include a 100-cycle thermal shock at the rated temperature extremes followed by 1,000-hour life test on the same set of samples, humidity exposure (85 percent relative humidity at 85ºC, and the test voltage shall be either 1.5V maximum when the part is used at <10V, or rated voltage), and random vibration test in accordance with the applicable requirements of MIL-PRF-123 and MIL-PRF-28861. Individual components within the filter shall have independently undergone their specific Class S Group B requirements at the piece-part level.

4.4 Qualification Tests. All piece-parts used in filter construction, as well as the connector interface, require qualification. Qualification testing shall be in accordance with the applicable requirements in the applicable military specification or aerospace standard.

4.5 Incoming Inspection DPA. Piece-parts used in the filter connector assembly shall undergo DPA in accordance with MIL-STD-1580. The requirements for both connectors and the applicable filtering elements shall be used as accept/reject criteria. All metal surfaces shall be verified for the absence of prohibited materials (e.g., pure tin, zinc, unplated brass or cadmium). Completed filter connectors shall undergo DPA to evaluate the workmanship and quality of the assembly, soldered interfaces as well as any forbidden materials.

5. REGISTERED (RELIABILITY SUSPECT) PMP shall include:

a. Inserts made of nonapproved organic materials
b. Nickel or other ferromagnetic materials on RF connectors
c. Dissimilar metal mates
d. External flat cable connectors
e. See additional items in Section 300.

6. PROHIBITED PMP shall include:

a. Silver plate or underplate on contacts
b. Parts with cadmium plating (see Section 4, General Requirements, paragraph 4.3.3 of this document)
c. Parts with zinc plating (see Section 4, General Requirements, paragraph 4.3.3 of this document)
d. Parts with wire wrap contacts
e. Parts with prohibited materials in their construction (see Section 4, General Requirements, paragraph 4.3.3 of this document)
f. EMI or RF filters with tubular ceramic elements
g. Plastic encapsulated diodes
h. Non-passivated, metal film resistors
i. Other prohibitions shall be per the prohibitions listed in the applicable sections for each piece part used in the filter assembly
j. Connectors using ceramic capacitor arrays with base metal electrodes.
k. See additional items in Section 300.

Table 310-1. Group A Requirements for Emi Filter Connectors with Ceramic Arrays

Inspection/Test 1/	Requirement	Method	Sample
Electrical characteristics [C (capacitance), DF (dissipation factor), DWV (dielectric withstanding voltage), and 25ºC & 125ºC IR ([insulation resistance)]	Per detailed Specification	Per detailed Specification	100 percent
Insertion loss at ambient temperature (100 MHz)	Per detailed Specification	Per detailed Specification	5 lines per connector (100 percent)
Thermal shock	Per detailed Specification	20 cycles minimum, MIL-STD-202, Method 107, Condition A, except step 3 shall be at 125ºC.	100 percent
Electrical characteristics (C, DF, DWV, and 25ºC & 125ºC IR)	Per detailed Specification	Per detailed Specification	100 percent
Voltage conditioning	Per detailed Specification	Voltage conditioning shall be performed at twice rated voltage at 125 (+3, -0) ºC for a minimum of 168 hours and a maximum of 240 hours. There shall be no failures in the last 48 hours of burn-in.	100 percent
Electrical characteristics (C, DF, DWV, and 25ºC & 125ºC IR)	Per detailed Specification	Per detailed Specification	100 percent
Insertion loss at ambient temperature (100 MHz)	Per detailed Specification	Per detailed Specification	5 lines per connector (100 percent)
Radiographic Inspection	Per detailed Specification	Per detailed Specification	100 percent
Visual/Mechanical Inspection	Per detailed Specification	3 to 10X magnification	100 percent
Socket Contact Separation Force; Pin Contact (MIL-DTL-83513 Microminiature) Separation Force	Per detailed Specification	Per detailed Specification	100 percent

1/ PDA for all electrical measurements and voltage conditioning is 5 percent or 1 defective unit, whichever is greater.

SECTION 400

QUARTZ CRYSTALS

(MIL-C-49468, CANCELED)

1. SCOPE. This section sets forth detailed requirements for precision quartz crystal units.

2. APPLICATION.

2.1 End-of-life Design Limits. None identified.

2.2 Electrical Considerations. Operation at high drive levels may cause degradation of normal aging characteristics, of spectral purity, and of short-term stability. Low drive levels shall be used where these parameters are critical.

2.3 Installation and Handling. Precautions shall be taken to prevent seal damage and excessive mechanical shock or vibration to the crystal. Precautions shall be taken when trimming wire leads to minimize mechanical shock to the resonator. Plug-in type crystals shall not be used in space flight hardware.

2.4 Aging. Aging is the drift of resonant frequency with time. It may alternatively be specified as drift rate vs time. Aging shall be considered for each application.

3. DESIGN AND CONSTRUCTION.

3.1 Requirements. Design and construction shall be in accordance with the requirements of MIL-C-49468 (CANCELED) and the requirements of this document. The design of the crystal shall be such that the required frequency stability and drift can be maintained at a drive current of 1.0 ± 0.2 mA through the crystal.

3.1.1 Hermetic Sealing. Only hermetically sealed crystals shall be used. If a crystal filter or oscillator manufacturer also manufacturers the quartz crystal units, nonhermetically-sealed crystal units may be used provided the manufacturer arranges for transportation of the crystal to his manufacturing area in a manner that precludes them from being contaminated. Individual crystal units shall be sealed in a package by cold-welding, resistance-welding, or an alternate form of sealing that shall ensure a leak rate of less than 10 atm-cc/sec).

3.1.2 Electrode Metallization. The materials and application techniques for the resonator electrode metallization shall be selected to provide adequate adhesion of the electrode contacts under multiple thermal cycles. If gold electrodes are used, an undercoat, such as chromium or tungsten, shall be used.

3.1.3 Crystal Support. The design and materials employed on the support mechanism for the crystal shall provide adequate reliability under the specified operating and environmental conditions. A minimum 3-point mounting configuration shall be employed.

3.1.4 Quartz Resonator. Quartz resonators shall be cut from a bar of pure Z-growth, cultured quartz in accordance with EIA 477, Grade 2.2 (Q of 2.2×10^6 minimum). The quartz shall be swept (impurities removed by solid-state electro-diffusion process).

3.1.5 Header and Lead Finish. The finish for the package header shall be gold plating in accordance with MIL-DTL-45204, Type II, Grade C, Class 00 except 15 microinches minimum over electroless nickel plating with a thickness of 100 to 200 microinches. Lead finish shall be gold plating in accordance with MIL-DTL-45204, Type II, Grade C, Class 1 over electroless nickel plating with a thickness of 100 to 200 microinches.

4. QUALITY ASSURANCE. Quality assurance provisions shall be in accordance with the requirements of MIL-C-49468 (CANCELED) and the modifications specified in the following subparagraphs:

4.1 In-process Controls. In-process controls shall be in accordance with the Class S requirements of MIL-C-49468 (CANCELED) and the following:

4.1.1 Pre-cap Visual and Mechanical Examination of Installed Crystals. Visual and mechanical examination shall be performed in accordance with MIL-C-49468 (CANCELED), except that the magnification shall be a minimum 10X magnification. Units exhibiting one or more of the following anomalies shall be rejected.

a. Cracks or holes in the weld contact area where crystal support members are welded to the holder base terminal pins

b. Loose or broken terminal pins or crystal mounting supports

c. Cracks or separations in electrically conductive bonding cement between quartz crystal and support member

d. Fractures of any size and any location in the crystal quartz resonator. Cracked/flaked edges, or fractures/cracks/ peeling of the electrodes that are rejectable per paragraph 4.1.1.1.

e. Loose weld spatter, bonding cement, or other particulate matter

f. Less than 0.005-inch clearance between quartz resonator and the package walls.

g. Quartz crystal resonator not parallel, or crystal and package wall not perpendicular to crystal holder base within 10 degrees

h. Joining of packages by interference, friction, crimping or similar methods unreinforced by welding

i. Any surface, including cover, exhibiting contamination, corrosion, adhering particulate, film, flux residue, fingerprint, or other materials not intended by design

j. Adhering weld splatter exceeding 0.03-inch dimension through any plane. Weld splatter shall be considered adherent when it cannot be removed with a 20 psig gas blow of dry, oil-free nitrogen

k. Base terminal and crystal mounting support exhibiting nicks, misalignment, cuts, cracks, or distortion. Scratches in the plating of the package terminals and deformation of the terminals/supports in the weld area shall be acceptable.

l. Quartz crystal not centered within +0.030 inch in its mounting with respect to the quartz crystal holder base

m. Dimensions out-of-tolerance

4.1.1.1 Visual Inspection Criteria of Uninstalled Crystals

1) Crystal Blank Inspection Criteria. No crystal blanks exhibiting the following under 10x magnification are acceptable.

   a. Edge chips/flakes. Any edge chips when examined less than 10 x magnifications that are greater than .005" deep and .010” long. Five (5) chips maximum per resonator.

   b. Flakes / Chip-out. Chip-outs that do not initiate at the edge. Edge chips shall be <.005” in diameter.

   c. Cracks/Fractures. No cracks are acceptable.

   d. Internal crystal defects. Any bubbles or needle inclusions when examined under 10x magnification

   e. Contamination. As evidenced by either significant discolorations or foreign material that cannot be removed by blowing with N_2 at 20 psi.

   f. Extensive Pitting. Polished crystal blanks when examined under 10X shall not show major pitting of the polished surfaces. This is evidenced by cloudiness when examined at 1x magnification. Shallow and uniform etch pits within a well polished surface are acceptable and normal on a polished blanks that has been etched to frequency.

2) Finished Crystals Inspection Criteria. No finished crystal shall be acceptable which exhibits the following when examined at 10x magnification:

   a. Crystal Blank Defects. The crystal blank inspection criteria of paragraph 1 also apply to finished crystals.

   b. Metallization Defects

      1. Blistering, peeling. No finished crystal shall be acceptable that exhibits any blistering or peeling metallization.

2. Scratches/Voids. No finished crystal shall be acceptable that exhibits the following:

Flag portion of the electrode:

a) Any scratch, hole or void that exposes the underlying crystal resonator substrate and reduces the operating flag metallization width greater than 25%.

b) No major scratches >2.5 mm (>0.100") that expose the underlying crystal resonator substrate and travel in a parallel direction with the flag. NOTE: Minor, faint or very shallow surface scratches <2.5mm (<0.100") long in the plating that do not expose the underlying crystal resonator substrate are not grounds for rejection except for loose metallization.

Electrode:

No finished crystal shall be acceptable that exhibits the following:

a) Any scratch, hole or void that exposes the underlying crystal resonator. NOTE: faint surface scratches < 2.5mm (<0.100") long in the plating that do not expose the underlying crystal resonator substrate are not grounds for rejection.

b) Electrode alignment / Concentricity. The spot alignment (top side to bottom side) is off concentricity greater than 10% of the electrode diameter.

Contamination:

No finished crystal when examined at 10X shall be acceptable that exhibits the following:

a) Any particulate foreign matter on the metallization that cannot be removed by blowing with N_2 at 20 psi.

b) Any significant discoloration, staining or pitting effect on the metallization.

Definitions. The following definitions are provided to aid in understanding the visual inspection criteria.

a. Crystal blank. A un-electroded crystal resonator.

b. Crack/Fractures. A crack is a special type of chip with a small fracture line projecting away from the edge of the crystal. It represents a break in the crystal blank without complete separation of parts. This may propagate over time and temperature cycling, stress etc. It is therefore a reliability risk and is always rejected.

c. Edge. The side of the crystal blank that forms the perimeter around the crystal.

d. Edge metallization. The metallization that electrically connects the metallization from the top surface to the opposite side of the crystal blank. It may also be called wraparound metallization.

e. Electrode. The metalized material that is deposited on either side of a crystal blank.

f. Face. The top and bottom surfaces of the crystal blank.

g. Finished Crystal. A crystal resonator made from piezoelectric plate substrate material (quartz) and metallic electrodes.

h. Flag. The portion of the metallic electrode on the crystal that extends out from the center geometric design to the edge of the crystal blank. [NOTE: Flags are, typically, described by using the apparent angle both top and bottom flags produce as they travel from the center of the crystal blank, i.e., 120° or 18.]

i. Flake. A defect representing material from the basic geometry similar to a chip but having a smoother surface at the chip. Flakes also leave a portion of the crystal thickness intact.

j. Flat. The intentional flat segment along the crystal blank's circumference which identifies the X-axis of the blank.

k. Inclusions. Any bulk irregularity not caused by surface mechanical disturbance. Bubbles are spherical defects trapped inside the crystal blank. Needles are small, linear impurities or defects trapped inside the crystal blank.

l. Multilayered metallization. Two or more layers of metal or other material used for interconnections that are not isolated from each other (laminates). The term "underlying metal" shall refer to any layer below the top layer of metal.

m. Original width. The width dimension or distance that is intended by design (i.e., original metal width, original flag width, original spot size, etc.).

n. Overlap Critical Area. The overlap area equal to 1/3 of the total tab / flag overlap closest to the flag intersection.

o. Pits. Multiple small holes in a polished surface which usually appear as spots of light or a general cloudiness. They usually are more visible after metallization.

p. Scratch. Any tearing defects in the surface of the metallization and is represented by a mar or mark, usually thin and shallow and generally not visible without 10x magnification or greater.

q. Spot. The center (geometric design) portion of the metallization on the face of the crystal blank, (usually round) which defines the general area of electric field causing crystal vibration.

4.2 Screening (100 percent). Screening (100 percent) shall be in accordance with the requirements listed in Table 400-1.

4.2.1 Lot Rejection. The PDA for the screening tests (Table I) shall be 5 percent per Class S requirements of MIL-C-49468 (CANCELED).

4.3 Lot Conformance Tests. Lot conformance tests shall be in accordance with the requirements listed in Table 400-2 and the following subparagraphs. Lot conformance testing is not required if the same lot that is being procured is undergoing qualification by test.

4.3.1 Sampling Plans. Eight pieces of each manufacturing lot shall be subjected to lot conformance testing. Sample size for Subgroup 1 shall be four and sample size for Subgroup 2 shall be four.

4.3.1.1 Disposition of sample units. Sample units which have been subjected to lot conformance inspections and tests shall not be delivered on the purchase order, unless otherwise specified. The samples shall be maintained with the associated test data and traceability as specified by the program.

4.3.2 Lot Rejection. The entire manufacturing lot shall be rejected if a failure occurs during lot conformance testing. Further processing of rejected manufacturing lots shall be as specified in MIL-C-49468 (CANCELLED) for Class S devices.

4.3.3 Lot Conformance Subgroup 1 Tests. Subgroup 1 tests shall be in accordance with the requirements of MIL-C-49468 (CANCELED) and the modifications specified in the following subparagraphs:

4.3.3.1 Solderability and Lead Attachments.

a. Wire-lead Terminals: Solderability shall be in accordance with MIL-STD-202, Method 208

b. Ceramic Package: If parallel-gap welding or thermocompression bonding is used, gold wires shall be attached using the specified method. Each wire or ribbon shall be subjected to Test Condition C, Method 2011, of MIL-STD-883. If soldering is specified, 0.25mm diameter (#30 B & S) copper wire shall be soldered to each terminal. Each wire shall be subjected to Test Condition A and Test Condition B of Method 2005 of MIL-STD-883.

4.3.3.2 Terminal Strength. Terminal strength shall be determined in accordance with MIL-C-49468 (CANCELED).

4.4 Qualification Tests. Successful completion of Lot Conformance testing as defined in this section shall form the basis for qualification.

4.5 Incoming Inspection DPA. Incoming inspection DPA shall be in accordance with MIL-STD-1580 and as modified herein. All metal surfaces shall be verified for the absence of prohibited materials (e.g., pure tin, zinc, or cadmium).

4.5.1 Additional Defect Evaluation Criteria. The devices shall also be inspected for loose or loosely attached particles.

5. REGISTERED (RELIABILITY SUSPECT) PMP shall include:

a. Solder sealed packages
b. Gold metallization without barrier metal
c. Two-point mounting internal construction
d. Quartz other than EIA-477 premium Q type
e. Non-swept quartz in radiation environments
f. Plug-in packages

6. PROHIBITED PMP shall include:

a. Devices with prohibited materials in their construction (see Section 4, General Requirements, paragraph 4.3.3 of this document).

Table 400-1. 100 Percent Screening Requirements for Quartz Crystals

MIL-C-49468 (CANCELED)	Modifications to the Methods and Criteria of MIL-C-49468 (CANCELED)
Pre-Seal Visual Examination	Para 4.1.1 of this Section
PIND 1/	MIL STD 883, Method 2020, Condition A unless otherwise specified
Thermal frequency repeatability	Para. 4.9.16.1 of MIL-C-49468, 3 cycles minimum unless otherwise approved by the PMPCB
Frequency	Frequency and equivalent resistance shall be measured at the specified reference temperature
Unwanted Modes	
Capacitance	
Shunt	When specified
Motional	When specified
Quality Factor	When specified
Aging 1/	30 days at 85ºC. $\Delta f/f \leq 2$ ppm
Drive Sensitivity (frequency, resistance)	$\Delta f/f \leq 2$ ppm; R ≤ ±10 percent or ±3 ohms, whichever is greater
Vibration (random)	Random vibration per MIL-STD-202, Method 214, Condition IF, $\Delta f/f \leq 1$ ppm
Thermal shock	MIL STD 202, Method 107, Condition B-1. Delta $f/f \leq 1$ ppm
Insulation Resistance	
Coupled modes (activity dips)	Equivalent resistance shall not exceed the maximum value specified in the detailed specification and the frequency shall not deviate from a sixth order equation curve best fit by more than: a) 1 ppm when accompanied by a reversal of slope, b) 1.5 ppm when not accompanied by a reversal of slope.
Frequency and equivalent resistance at reference temperature	Frequency and equivalent resistance shall be measured at the specified reference temperature.
Frequency and resistance verses temperature (static)	
Seal	MIL-C-49468, except gross leak shall be in accordance with MIL-STD-202, method 112, condition D or E
Radiographic inspection	Per MSFC-STD-355
Visual (External) and Mechanical Examination	

1/ Aging test may be performed anytime after thermal shock and PIND and before final electrical tests. PIND may be performed anytime after thermal shock and before aging.

Table 400-2. Lot Conformance Tests

MIL-C-49468 (CANCELED)	Modifications and Additions to the Methods and Criteria of MIL-C-49468 (CANCELED)
Subgroup 1	
Resistance to Solvents	
Frequency and resistance offset	When specified in the detail drawing
Thermal shock	MIL STD 202, Method 107, Condition B-2.
Thermal time constant	When specified in the detail drawing
Frequency overshoot	When specified in the detail drawing
Thermal frequency repeatability	When specified in the detail drawing
Thermal frequency hysteresis	When specified in the detail drawing
Mechanical shock	MIL STD 202, Method 213, Condition F, 1500g's, 0.5 ms, half sine pulse) for T0-5 style packages, or Condition E (1000 g's, 0.5 ms, half sine pulse) for T0-8 style packages.
Seal	Gross leak test shall be in accordance with MIL STD 202, Method 112, Condition D or E.
Terminal Strength	MIL STD 202, Method 211 and MIL-C-49468 (CANCELED) on two samples
Bond Strength	When specified
Subgroup 2	
Insulation Resistance	
Aging	40 days minimum
	Test temperature shall be the greatest upper turnover temperature measured for the lot.
	$\Delta f/f \leq 2$ ppm. The frequency change after mission life (generally 7 or 10 years, see the operational aging requirement in the detail drawing) shall be calculated using the curve fit specified in MIL-C-49468 and shall not exceed the value specified.
Vibration	Random vibration per MIL STD 202, Method 214, Condition 11K. Delta $f/f \leq 1$ ppm.
Solderability or Lead Attachment	MIL STD 202, Method 208
Resistance to Soldering Heat	Devices shall be cleaned with isopropyl alcohol only.
Radiation Hardness	As specified in the applicable radiation SID

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SECTION 410

CRYSTAL OSCILLATORS & CRYSTAL FILTERS

1. SCOPE. This section sets forth the requirements for crystal oscillators and crystal filters for use in space applications.

2. APPLICATION.

2.1 Derating. Individual elements shall be derated in accordance with the applicable sections of this document.

2.2 End-of-life Design Limits shall be:

a. Crystal Oscillators: Maximum specified parametric limits for high and low temperature operation.

b. Crystal Filters: Maximum specified parametric limits for high and low temperature operation.

3. DESIGN AND CONSTRUCTION. Oscillators and crystal filters that contain quartz bulk acoustical resonators shall meet all the design, construction, workmanship and rework (if any) requirements of MIL-PRF-38534 for Class K and MIL-PRF-55310 for Class S, as applicable, along with all the requirements of Section 960 herein.

4. QUALITY ASSURANCE. The in-process inspection, screening, quality conformance inspection and qualification shall be in accordance with MIL-PRF-38534 Class K with the 30-day Aging for hybridized oscillators, or MIL-PRF-55310 Class S, as applicable, along with all the requirements of Section 960 herein. The elements inside oscillators and crystal filters shall meet all the requirements of the applicable sections in this document. Crystals shall be in accordance with Section 400 herein.

4.1 Incoming Inspection DPA. Incoming inspection DPA shall be in accordance with MIL-STD-1580 and as modified herein. All materials shall be verified for the absence of prohibited materials (e.g., pure tin, zinc, or cadmium).

5. REGISTERED (RELIABILITY SUSPECT) PMP shall include:

a. See applicable sections of elements used within oscillator or filter.

b. Bimetallic bonds. See paragraph 4.3.6 of Section 4 of this document.

6. PROHIBITED PMP shall include:

a. See applicable sections of elements used within oscillator or filter.

b. Devices using prohibited materials in their construction either internally or externally (see Section 4, General Requirements, paragraph 4.3.3 of this document).

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SECTION 500

DIODES

See Section 1400 Semiconductors (Transistors and diodes)

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SECTION 510

RF DIODES

(MIL-PRF-19500)

1. SCOPE. This section sets forth additions and modifications to the requirements in Section 1400. All the requirements of Section 1400 apply unless otherwise modified in this section. This section applies to the following types of diodes: (a) PIN/NIP (b) Step Recovery, (c) Schottky Barrier, and (d) Varactor.

2. APPLICATION.

2.1 Derating. Derating shall be based on the requirements in Section 1400.

2.2 End-of-Life Design Limits shall be in accordance with the requirements of Section 1400.

2.2.1 Leakage Current. End-of-life leakage currents shall not exceed maximum rated limit.

3. DESIGN AND CONSTRUCTION.

3.1 Requirements. Design and construction shall be in accordance with the requirements of Section 1400 and the requirements of this section. Devices shall be metallurgically bonded where practicable. Plastic encapsulation shall not be used without the prior approval of the procuring activity. Monometallic bonding is preferred. Unglassified semiconductors in which leads cross scribe lines with clearance of less than 0.002 inch shall not be used.

4. QUALITY ASSURANCE. Quality assurance provisions shall be in accordance with Section 4, General Requirements, of this document, the requirements of Section 1400, and the following:

4.1 In-process Controls. In-process controls shall be in accordance with the requirements of Section 1400, with the additional in-process tests, or precautions, to be employed when certain materials are used in the construction of the device (like GaAs, which is susceptible to hydrogen poisoning, etc.).

A sample of 3 die per wafer, and a minimum 10 die per wafer lot shall be exposed to a diffusion bake test to determine the quality of the barrier metal. Pre- and post-leakage currents, and/or IV curves, shall be taken. Time and temp duration shall be a minimum of 300ºC for 24 hours. An alternate time/temp relationship may be used, but the minimum temperature shall be 275ºC. Acceptance criteria shall be less than one order of magnitude change from pre-bake electrical measurements.

4.2 Mesa Construction. Verify that there is at least 6000 angstroms of glass or oxide passivation over junctions.

4.3 Screening (100 percent). Screening (100 percent) shall be in accordance with section 1400 for the JAN S requirements of MIL-PRF-19500 and as modified in this section. The electrical tests shall be in accordance with the detailed spec. Unless otherwise specified the reject criteria shall be per the detail specification limit.

Thermal Impedance shall be measured on 100 percent of the diodes.

4.4 Quality Conformance Inspection (QCI). QCI shall be in accordance with section 1400 for the JAN S requirements of MIL-PRF-19500 and as modified in this section. The following tests are optional:

a. Surge current
b. Thermal resistance unless the temperature rise will be more than 5°C.
c. HTRB for Schottky and GaAs diodes
d. Group B, Subgroups 5 and 6
e. Group C, Subgroup 5

Section 510 RF DIODES

4.5 Qualification Tests. Qualification shall be in accordance with section 1400 for the JAN S requirements of MIL-PRF-19500 and as modified in this section:

a. QCI as described in this section.

b. Group E in accordance with MIL-PRF-19500 excluding Subgroups 2, 3, 4, 5, and 8. Subgroup 7 of Group E shall only apply to axial leaded devices and will require at least 3 cycles per lead.

4.6 Incoming Inspection DPA. Incoming inspection DPA shall be in accordance with MIL-STD-1580. All metal surfaces shall be verified for the absence of prohibited materials (e.g., pure tin, zinc, or cadmium).

5. REGISTERED (RELIABILITY SUSPECT) PMP shall include:

a. Hot welded cans

b. Nonpassivated die

c. Bimetallic bonds at die. See paragraph 4.3.6 of Section 4 of this document.

d. Point contact (whisker) devices

e. Silver bump, ramrod construction

f. Non-metallurgically bonded construction (except Schottky devices), unless supported by operational thermal cycle data.

g. Germanium devices

h. Gallium Arsenide devices

i. Flip chip units

j. Glass die attach

k. Parts containing organic materials

6. PROHIBITED PMP shall include:

a. All plastic encapsulated types except quad diode structures used in mixer assemblies.

b. Pure tin coated packages and leads (see Section 4, General Requirements, paragraph 4.3.3 of this document).

SECTION 600

EMI AND RFI FILTERS (FS)

(MIL-PRF-28861, CLASS S)

1. SCOPE. This section sets forth detailed requirement for low-pass RFI and EMI filters. All parts selected for the system application shall meet the requirements specified herein, unless otherwise approved by the program. Alternate approaches to meeting particular requirements shall be proven equivalent or more stringent than specified herein.

2. APPLICATION

2.1 Derating

2.1.1 Voltage Derating. Filters shall not be used at more than 50 percent of their rated voltage at the specified temperature.

2.1.2 Current Derating. The DC current shall be limited to 75 percent of the maximum rated current at the specified temperature.

2.2 End-of Life Design Limits shall be:

Capacitance	±20 percent of specification limits for BX or BR dielectric
Insulation Resistance	50 percent of specification limit

2.3 Electrical Considerations. Under certain conditions, the current parameters of the filter are governed by the transient surge current (I_S). In order to determine whether a filter can withstand a known surge current, the following analysis shall be used. A filter shall not be exposed to a transient current that could damage the device.

a. Transient Current. With no load current flowing:

I_S = Surge current (amperes)

I_R = Rated DC current (amperes)

t_S = Duration of I_S (microseconds)

Then, if t_S multiplied by I_S is less than 1.4 I_R, the filter should not be damaged.

b. Rated Load Current. With rated load current, I, flowing:

Then, if t_S multiplied by I_S is less than 0.4 I_R, the filter should not be damaged.

2.4 Mounting.

2.4.1 Installation and Soldering. Installation and soldering shall be in accordance with Section 3500.

2.4.2 Stud Mounting. Stud mounted devices shall not have the mounting nut torqued more than the specified limit. Never hold the filter body (to keep it from turning when the nut is being tightened or loosened) unless the filter is expressly designed for this purpose. Only internal-style tooth lockwasher shall be used to cut through any mounting surface contamination and the lockwasher shall only be inserted between the filter and mounting surface and not between the nut and mounting surface. Insulation resistance or dielectric with standing voltage should be performed after torquing.

2.4.3 Connecting Wires. When connecting wires to the device, a heat sink shall be used on the filter stud lead. Caution, rework involving solder removal by wicking may damage high temperature solder seals in stud leads.

2.5 Aging Sensitivity. Filters with ceramic discoidal capacitors using BR or BX dielectrics can exhibit capacitance decreases of 2.0 to 4.0 percent per decade hour.

3. DESIGN AND CONSTRUCTION. Filters used for EMI and RFI are usually L, C, Pi, or T sections made up of toroidal wound or ferrite bead inductors and capacitors or of simple feedthrough capacitors. Ceramic capacitors are used in most smaller EMI filters requiring low RF currents.

3.1 Requirements. Design and construction shall be in accordance with the Class S requirements of MIL-PRF-28861.

3.2 Outgassing. All polymeric and organic materials used in the construction of the part shall comply with the outgassing requirements defined in Section 4, General Requirements, paragraph 4.1.9 of this document.

4. QUALITY ASSURANCE. Quality assurance provisions shall be in accordance with Section 4, General Requirements, of this document and the following:

4.1 In-process Inspections. In-process inspections shall be in accordance with the Class S requirements of MIL-PRF-28861.

4.2 Group A Requirements. Group A requirements shall be in accordance with the Group A screening requirements of MIL-PRF-28861, Class S.

4.3 Group B Tests. Group B tests shall be in accordance with the Group B tests of MIL-PRF-28861, Class S requirements.

4.4 Qualification Tests. Qualification testing shall be in accordance with the Class S requirements of MIL-PRF-28861.

4.5 Incoming Inspection DPA. Incoming inspection shall be in accordance with MIL-STD-1580, except for tubelet fill which shall be 50 percent minimum of tubelet diameter, or 0.020 inch of tubelet height, whichever is less. All metal surfaces shall be verified for the absence of prohibited materials (e.g., pure tin, zinc, or cadmium).

4.6 Solder Dip/Retinning. See Section 4, General Requirements, paragraph 4.3.4.1 of this document.

5. REGISTERED (RELIABILITY SUSPECT) PMP shall include:

a. Devices with suspect constituents (see specific capacitor, etc. sections)
b. Nonhermetic devices (polymeric seals)
c. Filters without glass end seals are both subject to corrosion and may outgas significantly. Gold-plated parts with polymeric end seals are especially subject to moisture penetration and outgassing.
d. External tooth locking hardware

6. PROHIBITED PMP shall include:

a. EMI or RFI filters with tubular ceramic elements
b. EMI or RFI filters with prohibited materials in their construction, including the hardware that comes with the parts (see Section 4, General Requirements, paragraph 4.3.3 of this document).
c. Filters using capacitors with base metal electrodes (BME).

SECTION 700

FUSES

1. SCOPE. This section sets forth detailed requirements for fixed, high reliability sealed fuses intended for use in space applications. All parts selected for the system application shall meet the requirements specified herein, unless otherwise approved by the program. Alternate approaches to meeting particular requirements shall be proven equivalent or more stringent than specified herein.

2. APPLICATION. Electrical overload protection, when required, is usually considered part of the electrical power control subsystem. When fuses are required, the current ratings of the fuses shall be determined at specified operating conditions. These conditions typically vary for each application and include:

a. Fuse case temperature

b. Connections/attachment method to the circuit

c. Open Circuit Voltage

d. Maximum current delivered by the power source. The fuse selected shall be matched to the maximum current of the power source, such that the current shall not be so low as to fail to blow the fuse nor so high as to destroy the fuse completely.

e. When heritage, hollow-body, wire element fuses are used, vibration and shock levels (i.e., pyro shock) in the application shall be reviewed. A vibration and shock test shall be performed as part of the lot conformance tests. The vibration and shock test levels shall meet that of the worst case application.

f. For loss of internal pressure, see 2.1.2d.

g. Due to the higher fault clearing currents of solid body fuses (80A/μs), they are not directly interchangeable in application with hollow body fuses.

2.1 Derating. The current ratings of fuses shall be derated depending on the part type and application factors. The following derating criteria shall be used:

2.1.1 Solid, Molded Fuses. For solid, molded fuses with no internal air cavity, including gold element chip fuses:

a. Atmospheric and vacuum. At a fuse case temperature of 25ºC, a derating factor of 0.80 rated current shall be used.

b. Temperature. At fuse case temperatures above 25ºC, additional derating shall be used. The derating factor shall be decreased by either 0.2 percent or the manufacturer's suggested derating factor, whichever is higher, for each degree C above the rated temperature, up to the maximum allowed temperature.

c. Fault clearing current. This fuse clears current at 80A/μs. Consequently, the voltage transients for this fuse are significantly higher than the transients for hollow body constructions. Therefore, the two constructions may not be readily interchangeable.

2.1.2 Hollow body, wire element fuses. For heritage, hollow body, wire element fuses:

a. Atmospheric.
For atmospheric or non-vacuum operating conditions at 25ºC, a derating factor of 0.70 rated current shall be used to compensate for individual tolerances and provide a safety factor.

b. Vacuum.
For use under vacuum conditions at 25ºC, Table 700-1 shall be used. Smaller fuses require greater derating to compensate for loss of cooling due to long-term leakage of air from hermetic devices, which shall be considered in the circuit design and part selection (see Paragraph 3.1 below).

c. Temperature.
Above 25ºC, additional derating is necessary for operation under either atmospheric or vacuum conditions. The derating factor shall be decreased by either 0.2 percent or the manufacturer's suggested derating factor, whichever is higher, for each degree C above the rated temperature, up to the maximum allowed temperature.

d. Voltage.
The interrupt voltage rating shall be derated to 50V, because the fuse will not clear faults above 50V in vacuum.

Table 700-1. Fuse Derating in Vacuum At +25°C

Fuse Rating (Amps)	Derating Factor
2	0.50
1	0.45
1/2	0.40
3/8	0.35
1/4	0.30
1/8	0.25

2.2 Electrical Considerations

2.2.1 Fuse Characteristics. Factors to be considered in the selection of fuses and in their derating shall include the likely variation of fuse element resistance from fuse to fuse, deterioration of fuse rating resulting from repeated turn-on and turn-off of the fuse, other current surge characteristics, and maximum open circuit voltage tolerance.

2.2.2 Voltage. Fuses shall not be used in circuit applications when the open circuit voltage exceeds the maximum specified voltage rating for the fuse.

2.2.3 End of Life. No End of Life requirement applies to fuses.

2.3 Mounting. For hand soldering operations, heat sinking or other controls shall be used to prevent the reflow of internal solder.

3. DESIGN AND CONSTRUCTION

3.1 Requirements. Design and construction shall be in accordance with the requirements of the applicable specifications and the requirements of this document. Solid, molded fuses and chip fuses with glass arc suppressant are the preferred design. Other designs shall be considered for space use only if they can be demonstrated to not alter current ratings more than 10 percent when used under vacuum (i.e., loss of pressure within fuses) or if hermeticity can be demonstrated to provide the above stability over a 10-year period in vacuum. (Extrapolations from leak rate measurements may be used.)

3.2 Outgassing. The organic materials and finishes used in the construction of the part shall meet the outgassing requirements specified in Section 4, General Requirements, paragraph 4.1.9 of this document.

4. QUALITY ASSURANCE. Quality assurance provisions shall be in accordance with Section 4, General Requirements, of this document and the following:

4.1 In-process Controls. In-process controls shall be in accordance with the requirements of MIL-PRF-23419 and MIL-PRF-23419/12.

4.1.1 Solid Body Fuses. Fuse elements shall be visually inspected at 10X minimum magnification prior to encapsulation of all items. Radiographic inspection shall be viewed at 7X minimum at a minimum of 2 orthogonal views or 360° turn and meet the requirements of MIL-PRF-23419/12.

4.1.2 Hollow body, wire element, fuses. Fuse element attachment shall be visually inspected on all items at 10X magnification minimum, except that for fuses with opaque bodies, radiographic inspection viewed at 7X minimum shall be acceptable at a minimum of 2 orthogonal views, or 360° turn using real-time x-ray (preferred)..

4.2 Screening (100 percent). Screening (100 percent) shall be in accordance with the quality conformance requirements listed in MIL-PRF-23419/12, except as modified below.

4.2.1 Chip Fuses. Burn-in and dielectric withstanding voltage are not required as part of quality conformance on chip fuses. For the Overload Current Characterization test, each lot shall be truncated to form an inspection lot based upon the cold resistance instead of voltage drop. The radiographic inspection criteria for chip fuses shall be as stated in 4.2.1.1.

4.2.1.1 Chip Fuse Radiographic inspection. The radiographic examination shall include the following accept and reject criteria:

a. There shall be a minimum of two views.. View 1 shall show the plan view of the part. View 2 shall show a side view of the part on an edge that does not contain terminations.

b. The sensitivity of the radiograph shall be such that a lead particle .004 inch (0.10 mm) in diameter shall be visible. Use of double emulsion film is optional.

c. Contact between internal fuse element and external termination shall be verified (internal film-to-end termination interface).

d. Internal element position shall be verified. Element material shall be completely encapsulated by arc suppressive cover glass. There shall be no exposed element at the sides of the part.

e. There shall be no cracks in the arc suppressive cover glass or in the ceramic base.

f. There shall be no voids in the arc suppressive glass greater than 0.010 inches in diameter.

g. There shall be no voids in the end terminations greater than 0.005 inches in diameter.

h. There shall be no foreign materials in the fuse greater than 0.005 inches in diameter.

4.2.2 Leaded Surface Mount Fuses. Burn-in is not required as part of quality conformance on leaded surface mount fuses. For the Overload Current Characterization test, each lot shall be truncated to form an inspection lot based upon the cold resistance instead of voltage drop.

4.2.3 Hollow body, wire element, fuses. Heritage, hollow body, wire element fuses shall be screened (100 percent) in accordance with the requirements listed in Table 700-2. The requirements of MIL-PRF-23419/12 shall not apply.

4.3 Lot Conformance Tests. Lot conformance tests shall be in accordance with the Group B inspections, of MIL-PRF-23419/12, except as modified below.

4.3.1 Chip Fuses. Lot conformance tests for chip fuses shall be in accordance with Table 700-3.

4.3.2 Leaded Surface Mount Fuses. Lot conformance tests for leaded surface mount fuses shall be in accordance with the Group B inspections, of MIL-PRF-23419/12, except the manufacturer has the option of doing the solderability test before terminal strength. For the terminal strength test, wires may be soldered to the leads prior to test. Subgroup VI in accordance with Table 700-3 shall also be done.

4.3.3 Hollow body, wire element, fuses. Lot conformance tests for heritage, hollow body, wire element fuses shall be in accordance with the quality conformance tests, Subgroups 1, 2, and 5 of Group C inspections, of MIL-PRF-23419. The requirements of MIL-PRF-23419/12 shall not apply.

4.4 Qualification Tests. Qualification testing shall be in accordance with the requirements of MIL-PRF-23419/12, except as modified below.

4.4.1 Chip Fuses. For qualification testing of chip fuses, current-carrying capacity shall not be done as part of Group I. Terminal strength shall not be done as part of Group II and solderability shall be done before overload interrupt. Group VII shall be added for terminal strength. Terminal strength shall be performed on 6 samples in accordance with Table 700-3.

4.4.2 Leaded Surface Mount Fuses. For qualification testing of leaded surface mount fuses, current-carrying capacity shall not be done as part of Group I. For the Group II terminal strength test, wires may be soldered to the leads prior to test.

4.4.3 Hollow body, wire element, fuses. Qualification testing for heritage, hollow body, wire element fuses shall be in accordance with the requirements of MIL-PRF-23419.

4.5 Incoming Inspection DPA. Incoming inspection shall be in accordance with MIL-STD-1580. All metal surfaces shall be verified for the absence of prohibited materials (e.g., pure tin, zinc, or cadmium).

5. REGISTERED (RELIABILITY SUSPECT) PMP shall include:

a. Fuses comprised of low-melting-point alloys
b. Hollow body, wire element fuses
c. Any chip or leaded surface mount fuse with conformal coat coverage instead of a molded body or glass arc suppressant.
d. Wires used as fuses

6. PROHIBITED PMP shall include:

a. All fuses requiring fuse holders
b. Fuses using prohibited materials in their construction (see Section 4, General Requirements, paragraph 4.3.3 of this document).

Table 700-2. 100 Percent Screening Requirements for Hollow Body, Wire Element Fuses

MIL-PRF-23419 Screens	Additions to the Methods and Criteria of MIL-PRF-23419
Thermal Shock	a. MIL-STD-202, Method 107, Condition B; during last cycle, monitor for continuity
Seal, Hermetic	a. MIL-STD-202, Method 112. Gross leak per Test Condition A, or equivalent b. Test may be waived if not applicable
Terminal Strength and DC Resistance	a. Simultaneous DC resistance measurement b. Test current used shall be 10 percent of rated value during strength measurement +25ºC c. Resistance data within spec at all times during strength measurement
Burn-in	a. At +85 +0/-3ºC for 168 hours b. Rated DC voltage c. 50 percent rated DC current d. Test may be waived, except for ceramic and molded-body fuses, if the manufacturer can present written, detailed records to indicate that there have been no anomalies or failures detected in previous tests of similar fuses for the last 3 years (Note: Burn-in not required for pico fuses.)
DC Resistance	a. +25ºC b. Test current used shall be 10 percent of rated value c. Resistance data within spec at all times d. Resistance data within + 8 percent of initial reading at all times
Voltage Drop	a. Measurement taken with 50 percent rated current b. Measurement taken after 5 minutes c. Accept fuses within + 2 standard deviation of lot average
Visual and Mechanical Examination (External)	a. Marking and identification b. Defects and damage; i.e., body finish, lead finish, misalignment, cracks
Radiographic Inspection	a. Per MSFC-STD-355; 2 conventional x-ray views 90 degrees apart, or 360-degree view using “real-time” x-ray (preferred) b. Test may be waived except for ceramic and molded body devices

Table 700-3. Chip Fuse Group B Testing

Examination or Test	Requirement	Method	Number of Samples	Number of Defectives Allowed
Subgroup I				
Overload Current (+25 ºC)	MIL-PRF-23419/12	MIL-PRF-23419/12	20	0
Subgroup II				
Solderability	MIL-PRF-23419/12	MIL-PRF-23419/12	8	0
Subgroup III				
Resistance To Soldering Heat	When fuses are tested, there shall be no mechanical damage and the fuse resistance shall not change by more than 10 percent.	Fuses shall be tested in accordance with Method 210 of MIL-STD-202. The following details and exceptions shall apply: a) Solder temperature: 260ºC ± 5ºC. b) Immersion time: 10 ± 1 seconds. c) DC resistance shall be measured before and after the test in accordance with MIL-PRF-23419	4	0
Subgroup IV				
Termination Strength	When fuses are tested, the end terminations shall not break or loosen. The cold resistance values shall not change by more than 10 percent.	Fuses shall be tested in accordance with Method 211 of MIL-STD-202. The following exceptions shall apply: a) Test Condition - Test Condition A (5-lb pull minimum for fuses rated at 1.0 amp and higher; 4-lb pull for fuses rated at less than 1.0 amp) applying the force axially to each lead wire individually (solder .017 to .020 inch diameter wires to terminations prior to testing). b) Method of Holding - The fuse body shall be held by means other than rigid clamping to prevent stresses from being transferred to the fuse element. c) Measurements - DC resistance measurements shall be taken before and after exposure in accordance with MIL-PRF-23419.	4	0

Table 700-3 (Continued)

<table>
<tr><th>Examination or Test</th><th>Requirement</th><th colspan="2">Method</th><th>Number of Samples</th><th>Number of Defectives Allowed</th></tr>
<tr><td>Subgroup V</td><td></td><td colspan="2"></td><td></td><td></td></tr>
<tr><td>Current-Carrying Capacity (+25 ºC)</td><td rowspan="2">When fuses are tested, they shall show no evidence of mechanical damage and shall carry the current as specified without electrical failure. The temperature rise of the substrate shall at no point rise more than +85ºC above the ambient air temperature.</td><td colspan="2">Fuse samples shall be apportioned and submitted to the following DC test currents at -55ºC to -60ºC, at +20ºC to +35ºC (room ambient temperature), and at +125ºC to +130ºC</td><td rowspan="2">8</td><td rowspan="2">0</td></tr>
<tr><td></td><td>Test Temperature
–55ºC
+25ºC
+125ºC</td><td>DC Test Current
110 percent of Rated
100 percent of Rated
80 percent of Rated</td></tr>
<tr><td>Subgroup VI</td><td></td><td colspan="2"></td><td></td><td></td></tr>
<tr><td>Thermal Shock & 168-Hour Burn-In</td><td>When fuses are tested, the fuse voltage-drop (as measured at 10 percent rated current) shall not have changed by more than +/–10 percent of the pre-thermally shocked value. There shall be no evidence of external mechanical damage.</td><td colspan="2">Fuses shall be solder mounted onto suitable test boards and connected in an electrically series circuit. Prior to testing, the voltage-drop (at 10 percent rated current) of each fuse shall be measured and recorded. Voltage-drop measurements shall be accomplished by probing the fuse leads in the lead egress area. The mounted fuses shall then be subjected to 5 cycles of thermal shock testing in accordance with MIL-PRF-23419/12. Following the thermal shock exposure, the fuses shall be subjected to 168 hours (+4/-0 hours) of rated current testing. During burn-in testing, the ambient room temperature shall be maintained at from +25ºC to +30ºC. Fuse case temperature will not be controlled during the burn-in test. Following the 168-hour burn-in exposure, the fuse voltage-drop at 10 percent rated current shall be measured.</td><td>22</td><td>0</td></tr>
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SECTION 800

MAGNETIC DEVICES

(MIL-STD-981)

1. SCOPE. This section covers the detailed requirements for open and closed construction leaded and surface mount magnetic devices. All parts selected for the system application shall meet the requirements specified herein, unless otherwise approved by the program. Open construction magnetics are generally used for in-circuit tuning, and are unencapsulated and unpotted. These are self-leaded parts consisting of a magnet wire wound around a magnetic or air core, and have no internal connections. Mechanical stability is achieved by staking the magnetic or air wound cores to the board or substrate. These parts are fully visually inspectable; hence, the Group A (except 100 percent visual inspection and 100 percent electrical measurements) and Group B requirements of MIL-STD-981 do not apply. However, all other requirements of Section 800 and MIL-STD-981 for Class S shall apply. All magnetic devices that do not meet the description of an open construction magnetic shall be considered a closed construction device.

2. APPLICATION

2.1 Derating.

2.1.1 Temperature Derating. The maximum operating temperature of the device shall not exceed T_1 -25ºC, where T_1 is the insulation class temperature of the lowest temperature insulation material used in the device. The maximum operating temperature is the same as the allowable hot-spot temperature, which is defined as the sum of the ambient temperature and the device temperature rise.

2.1.2 Voltage Derating. Maximum winding-to-winding and winding-to-case voltages shall be derated to a factor of 0.50 of the minimum rated wire insulation voltage.

2.2 End-of-life Design Limits. The operational life of a magnetic device is limited by the various temperatures, which the insulation may be exposed to. For organic insulating materials, the design service life shall be reduced 50 percent for each 10ºC increase in hot-spot temperature above the derated maximum operating temperature.

3. DESIGN AND CONSTRUCTION

3.1 Requirements. Design and construction shall be in accordance with the requirements of the applicable specifications and the requirements of this document.

3.1.1 Internal Solders. To prevent internal solder reflow, devices shall be designed with higher solder melt temperatures than assembly reflow temperatures.

3.2 Applicable Specifications. The applicable specifications are:

a. MIL-PRF-27 for Audio, Power, Saturable and High-Power Pulse Transformers and Inductors
b. MIL-PRF-21038 for Low-Power Pulse Transformers
c. MIL-PRF-15305 for Fixed and Variable, Radio Frequency Coils
d. MIL-STD-981 for all Custom Magnetic Devices
e. MIL-PRF-39010 for RF Coils, Fixed, Molded
f. MIL-PRF-83446 for Fixed and Variable Chip Radio Frequency Coils
g. MIL-T-55631(2) for Fixed and Variable RF Transformers

3.3 Wire Size. Minimum magnetic wire size shall be as defined for Class S parts in Table I of MIL-STD-981. For devices with smaller diameter gauge than #36 AWG, the wire shall be terminated within the coil housing and a wire larger than #36 AWG shall be used to connect to the terminal. However, twisting smaller gauge wires (such as #36 AWG) and soldering to form a larger lead may fulfill the requirement for terminating with larger wires.

3.4 Organic Materials. Potting, encapsulation and other organic materials shall meet the outgassing requirements specified in Section 4, General Requirements, paragraph 4.1.9 of this document.

4. QUALITY ASSURANCE. Quality assurance provisions shall be in accordance with Section 4, General Requirements, of this document and the following:

4.1 In-process Controls. In-process controls shall be in accordance with the Class S requirements of MIL-STD-981. MIL-STD-981 shall be used in the preparation of contractor specification control drawings.

4.1.1 Pre-cap visual inspection. A pre-cap visual inspection shall be performed on all devices immediately prior to potting or encapsulation. The visual inspection shall be performed to ensure that the devices have been fabricated in accordance with good manufacturing practices and meet the requirements specified in the detail drawing. Devices that fail to meet these requirements shall be removed from the lot and shall not be shipped.

4.1.1.1 Pre-cap Color Images. If DPA is chosen not to be performed, color images shall be taken on a random sample of five parts per lot (or quantity specified on P.O.) during pre-cap inspection when solder joints/splices are still visible. Pre-cap images shall consist of the following:

a. One overall image of the part, using enough magnification so that the part fills the frame.
b. Close-up images of each visible solder joint, using a minimum of 10x magnification. Images may contain more than one solder joint.
c. A minimum of six images per device shall also be taken at 10X minimum magnification, one in each orthographic plane, plus a sufficient number of views to assure that the devices are consistent with high-reliability construction and workmanship.

Images shall be identified with the P.O. number and the marking information specified in the detail drawing.

4.2 Screening (100 percent). Screening (100 percent) shall be in accordance with the Class S requirements of MIL-STD-981 except when temperature rise is 30ºC or less, load burn-in is not required, but no-load burn-in is still required. (See MIL-STD-981 for detailed requirements and test conditions on load or no-load burn-in.) MIL-STD-981 shall be used in the preparation of contractor specification control drawings. Open construction magnetic devices require 100% electrical tests (to include, as a minimum, dielectric withstanding voltage (DWV), insulation resistance (IR), inductance, induced voltage (when applicable), corona test (when required) and all other electrical characteristics required by the applicable MIL spec), and 100% visual and mechanical inspection as a minimum.

4.3 Lot Conformance Tests. Lot conformance tests shall be in accordance with the Class S requirements of MIL-STD-981 for both Group A and Group B and Table 800-1. Lot Conformance stratification may be allowed if multiple dash numbers exist for any one magnetic design configuration. An example where this may apply: inductor designs that use the same core size and material, but varies the electrical properties by varying the wire gauges and/or number of turns. Also, lot conformance tests shall not be required for open construction magnetic devices.

4.4 Qualification Tests. Separate qualification tests are not required. Completion of lot conformance tests as specified in Paragraph 4.3 of this section satisfies the qualification-testing requirement.

4.5 Incoming Inspection DPA. Incoming inspection DPA shall be in accordance with MIL-STD-1580, except DPA is not required for open construction devices. 100 percent pre-cap inspection with color images of representative samples (per 4.1.1.1) in combination with real-time x-ray (per 4.5.1) may be used in lieu of DPA for closed construction magnetics. A minimum of three samples shall be used for DPA. All metal surfaces shall be verified for the absence of prohibited materials (e.g., pure tin, zinc, or cadmium). Though DPA is not required, open construction magnetic devices shall be subjected to 100% electrical tests (see 4.2 for details) and 100% visual and mechanical inspections as a minimum.

4.5.1 Real time x-ray analysis. Real-time x-ray with images (provided as part of the data package) shall be performed with a view of overall construction and two side views. Devices shall be carefully analyzed for winding, core, termination and with close-up views of any anomalous conditions. Devices shall meet the workmanship and x-ray criteria specified in MIL-STD-981 for Class S and in the detail drawing.

5. REGISTERED (RELIABILITY SUSPECT) PMP shall include:

a. Wire sizes not compliant with paragraph 3.3 above

b. Variable devices

6. PROHIBITED PMP shall include:

a. Prohibited materials used in the construction or as surface finish of the device (see Section 4, General Requirements, paragraph 4.3.3 of this document).

Table 800-1. Additions to Group B Lot Conformance

Per Applicable MIL Spec	Additions to MIL-STD-981 Group B
Temperature rise	Performed as part of Subgroup 1 on the same samples
Thermal shock	100 cycles minimum for Group B performed as part of Subgroup 2 just prior to life test For qualification only, perform the required number of cycles to meet the equivalent of 3x mission life minimum

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SECTION 900

MICROCIRCUITS

1. SCOPE. All microcircuits selected for the system application shall meet the requirements specified herein, unless otherwise approved by the program. This section covers the selection of monolithic microcircuits (Integrated Circuits) for space application.

2. APPLICATION. The microcircuits quality and reliability level, critical parameters, and environments for the system application shall be established as defined below. The part application in the system shall form the basis for the technical requirements of each part and critical performance parameters. System application considerations shall include areas such as thermal, mechanical, radiation, derating, End-of-Life limitations, mounting recommendations, and other design considerations necessary to ensure the high reliability of the parts as used in each space application. The design and construction, and the quality assurance requirements shall be established and documented in specifications to ensure their performance and the necessary quality for space applications.

2.1 Microcircuit Selection. The selected devices shall have demonstrated the ability through characterization and test to meet the worst-case requirements (application and acceptance/qualification) with margin to compensate for manufacturing variations and End-of-Life considerations. The contractor shall ensure that the worst-case conditions include recognition of ground tests performed at the subsequent levels of integration and not only those seen during flight. Where assessment data does not exist, the contractor shall define the technical criteria detailing how the capability of each selected device will be verified.

3. MICROCIRCUIT STANDARDIZATION. The number of different part types/part numbers and the use of previously qualified, or approved part types/part numbers for equivalent applications, shall be optimized.

3.1 Design Analysis. Circuit design analysis shall be performed to establish the electrical stresses such as voltage, current, power, etc. for each part under nominal and worst case conditions. The circuit design shall make allowances for worst-case variations, to compensate for manufacturing variations and End-of-Life parameter limits in the following as a minimum, but not limited to: input and output voltages; input and output currents; power dissipation; propagation delays; electromagnetic compatibility (EMC), operating junction temperature, operating frequency. Critical performance parameters shall be identified such that they can be documented in the detailed specifications, including appropriate verification requirements.

3.2 Thermal Analysis. Thermal analysis shall be performed to ensure the selected components are used within the specified derated temperature limits of the part. The derated temperature shall be based on the original die manufacturer/design activity published value.

3.3 Mechanical Analysis. Mechanical stress analysis shall be performed to establish the mechanical stress for each part, including those incurred during manufacturing, handling, and testing. The mechanical design shall make allowances for worst-case variations in mechanical stress due to temperature excursions, mismatches of thermal coefficient of expansion, mechanical shock, mechanical and acoustical vibration.

3.4 Radiation Environment Considerations. The effects of the expected radiation environments on the part performance in the application shall be analyzed and or tested to verify the component will operate successfully. These include Single Event Upset (SEU), Single Event Latch-up (SEL), Single Event Burn-out (SEB), Single Event Transient (SET), Single Event Functional Interrupt (SEFI), Single Event Gate Rupture (SEGR), and Total Dose Radiation both high dose rate, ELDRS conditions, and displacement damage. All mitigation strategies shall be documented. Radiation test sampling shall be relative to lot homogeneity as specified in paragraph 4.1.1. The environments addressed shall include the expected natural space environment calculated over the intended life of the mission and any additional nuclear enhanced environment specified in the system specification.

3.5 Design Margin. A design criterion shall be established, documented, and verified for all selected microcircuit devices to provide adequate performance that meets the application requirements. The design margin shall cover electrical, thermal, mechanical, and radiation performance margin over the worst-case conditions.

3.6 Parameter Derating. The parameters shall be derated according to the defined criteria in TABLES 900-1, 900-2, and 900-3.

Table 900-1. Digital Microcircuits Derating

PARAMETER	FACTOR (Nominal)	FACTOR (Worst Case)	COMMENTS
Total Output Load Current	.80	.90	Not Applicable to single fan-out devices.
Vcc specified	1.1VCC	1.1 VCC	Relative to recommended nominal
Transients	1.2 VCC	1.2 VCC	Transients on supply or I/O relative to nominal Vcc (not to exceed manufacturer specified values).
Propagation Delay	110 percent	110 percent	Design margin beyond worst case expectation
Fan-out	1 load or 80 percent	1 load or 80 percent	One less than, or 80 percent of, rated number of loads, except where fan-out is rated as one
Power Dissipation	.80	.90	
TJ Max.	+80 percent or 105°C whichever is less	+90 percent or 125°C whichever is less	TJ = Not to exceed 90 percent of the rated (in °C) or +125°C, whichever is less
VCC CMOS	.70	.80	Relative to absolute maximum (unless otherwise specified by the manufacturer, and/or still meets max Tj derating).
Maximum Operating Frequency	.80	.80	Unless otherwise specified by the manufacturer, and/or still meets max Tj derating.
Read/Write Cycle for EEPROM & FLASH EEPROM	.50	.50	Of manufacturer’s rated endurance.

Table 900-2. Linear Microcircuits Derating

PARAMETER	FACTOR (Nominal)	FACTOR (Worst Case)	COMMENTS
Input Signal Voltage	.70	.80	
Output Current	.75	.85	DC
Operating Frequency	.75	.85	Not required for devices designed to operate at specific frequencies.
Transients	1.20Vcc	1.4Vcc	Transients on supply and I/O, relative to nominal Vcc.
Gain	.75	.85	
Power Dissipation	.75	.85	
TJ Max.	80 percent or 105°C whichever is less	90 percent or 125°C whichever is less	TJ = Not to exceed 90 percent of the rated (in °C) or +125°C whichever is less

Table 900-3. Linear Voltage Regulator Microcircuit Derating

PARAMETER	FACTOR (Nominal)	FACTOR (Worst Case)	COMMENTS
Input Current	.80	.90	
Input Voltage	.70	.80	
Output Current	.75	.85	DC
Power Dissipation, PD	.75	.85	
TJ Max.	80 percent or 105°C whichever is less	90 percent or 125°C whichever is less	TJ = Not to exceed 90 percent of the rated (in °C) or +125°C whichever is less

3.7 Microcircuit Stress. The microcircuit derating shall be verified by analysis and or test (parts stress analysis) that it meets the established derating criteria. All instances in which the microcircuit is not used within the established derating limits shall be documented, mitigated, and reviewed and approved by the PMPCB.

3.8 Failure Modes and Effect Analysis (FMEA). The microcircuit failure modes and their effects on the system application shall be analyzed. All single point failures and mission critical microcircuits shall be identified and the risk of system failure shall be mitigated.

4. MICROCIRCUIT DESIGN. The microcircuits shall meet the MIL-PRF-38535 requirements for Class V devices. The contractor shall ensure that all microcircuit designs meet these requirements when other than QML V microcircuits are used.

4.1 Microcircuit Performance. The microcircuits electrical, thermal, mechanical, radiation, and reliability performance needed for the application shall be verified over the manufacturer's recommended operating conditions.

4.1.1 Microcircuit Characterization and Qualification. The microcircuits shall be fully characterized and qualified for space application. All failure modes shall be identified and mitigated. Section 5.3 Table 900-4 summarizes the most common and known failure mechanisms and their associated models. In addition, JEDEC Publication 122 provides a good starting point for failure modes identification and reliability. The mitigation shall fully document the tests, pass/fail criteria, and design strategies as appropriate. Where assessment data does not exist, the contractor shall define and describe how the capability of each selected device will be verified. This shall include the configuration controls that ensure the flight devices are form, fit, function, and performance equivalent to the evaluated parts.

When DPA sampling is conducted to verify lot conformance of a homogeneous* production lot of Space Quality microcircuits, the minimum sample size shall be 5 samples or 2 percent of the lot size, whichever is larger, unless otherwise directed by the Program. Also, see additional DPA sampling plan exception in paragraph 4.4.4 of Section 4, General Requirements. Radiation test sample size shall be in accordance with Appendix A requirements. Consideration should be made on a case by case basis of reducing the sample size on all extremely expensive, homogeneous lots where surveillance, close vendor history, and good engineering judgment are appropriate. Further consideration should be made of doubling the sample size for non-homogeneous lots** or lower quality level parts.

* QML Class V, JAN Class S, or other Microcircuits from a single wafer lot diffusion, single die attach machine, single wire bonder, single package lot, single package sealing activity, etc.

** QML Class Q & JAN Class B/883 Microcircuits, etc. with unknown lot diffusion, uncontrolled assembly, uncontrolled number die attach machines, uncontrolled number wire bonding machines, uncontrolled number of package lots, uncontrolled number of package sealing activities, etc.

4.1.2 Electrical Parameters. All critical parameters needed for the application shall be specified and verified (e.g. by analysis, generic characterization, lot characterization, or 100 percent test) over the established minimum and maximum rated operating temperature range. Parametric and test conditions of automatic test equipment programs shall be verified.

4.1.3 Microcircuit End-of-Life. End-of-life design limits shall be the maximum specified parametric limits for high and low temperature performance values unless otherwise established by testing or analysis. For example, the SMDs show pre-aging and pre-radiation limits, so additional factors from actual part/wafer test data due to aging and radiation must be accounted for in the end-use design.

4.1.4 Die Attach and or Substrate Attach. The die attach and or substrate attach design shall provide effective electrical and or thermal-mechanical path. The die attach materials used in the design and construction shall be compatible with the metallization backing of the microcircuit die and shall not harden, soften, blister, flow, crack, peel, flake, break, develop intermetallics or Kirkendall voids, or otherwise lose its properties during and after exposure to all environmental conditioning and qualification, and next assembly environments.

4.1.5 Physics of Failure. Refer to paragraph 4.2.1.1 in Section 4, General Requirements, of this document.

4.2 Mechanical Parameters

4.2.1 Materials Selection. The Microcircuit Design and Construction shall be such that it will not promote the growth of whiskers (e.g., tin, zinc, etc.), dendrites, intermetallic formation, or Kirkendall voids, fungus, or corrosion. Outgassing shall meet the requirements specified in Section 4, General Requirements, paragraph 4.1.9 of this document. Pure tin shall not be allowed (see Section 4, General Requirements, paragraph 4.3.3 of this document).

4.2.1.1 Die Interconnects. The die interconnects materials such as wires, tapes, bumps, columns, etc. shall be compatible with the top metallization of the die. Use of bi-metallic systems, dissimilar metals, or any other systems shall not be allowed unless proven, qualified, and verified not to develop intermetallics or Kirkendall voids, cause corrosion, flow, crack, peel, flake, or break during and after exposure to all environmental conditioning and qualification, and next assembly environments.

4.2.1.2 Metal Finishes. All metals and metal finishes (internal as well as external) shall be such that it will not promote the growth of whiskers (e.g., tin, zinc, etc.), dendrites, “purple plague” or “white plague”, fungus, corrosion, and shall not sublimate in the intended application conditions. Pure tin shall not be allowed (see Section 4, General Requirements, paragraph 4.3.3 of this document).

4.2.1.3 Package. The package design and construction shall not have exposed base material, crack, peel, flake, bend, or break during and after exposure to all environmental conditioning and qualification, and next assembly environments.

Section 900 MICROCIRCUITS

5. MANUFACTURING. The contractor shall ensure that all microcircuits meet the manufacturing criteria below.

5.1 Wafer Fabrication. The Wafer Fabrication shall meet the requirements of MIL-PRF-38535 for Class V, unless otherwise approved by the program.
5.2 Assembly. Microcircuit assembly shall meet the requirements of MIL-PRF-38535 for Class V, and the requirements specified herein unless otherwise approved by the program.

5.2.1 Lot Formation. The microcircuit manufacturer shall define and control the lot formation to ensure lot homogeneity.

5.2.2 Lot Date Code. Devices shall be assigned a lot Date Code with the week number and the year of assembly or device sealing. Devices shall be traceable through the lot date code to the assembly processing and assembly location.

5.2.3 Assembly Documentation. All assembly documentation shall be available for review at the manufacturer.

5.2.4 Facility. Assembly processing shall be in a facility designed and controlled to an appropriate cleanliness level for the technology produced to prevent yield loss and latent defects due to organic and inorganic particle contamination, human handling, and Electro Static Discharge (ESD). The manufacturer shall also define the action limits for the environmental control.

5.2.5 Process Controls. The microcircuit manufacturer shall establish in-process controls for key areas to verify (wafer mounting and wafer saw, wire bonding, die attach, lid seal, particle detection, lead trimming, final lead finish, etc) fabrication steps required to guarantee uniform and homogeneous lot processing. The monitoring process shall document and define: frequency of tests, sample sizes (samples shall be representative of the lot), verification criteria, control and action limits, as well as disposition of the non-conforming devices.

5.2.6 Wire Bonding. The manufacturer shall define, baseline, monitor, and control the wire bond process. As a minimum, the bonding method, wire material, wire size, wire diameter, machine set-up, frequency of set-up verification, the bond strength, bond placement, loop height, bond deformation shall be defined and controlled. All instances of bond lifts, intermetallic and Kirkendall voids formation, shall be rejected and investigated to eliminate the possibility of open bond latent failures. The minimum pull strength documented in the MIL-STD-883 TM 2011 shall be used only as a starting point and shall not be used for process control limits.

5.2.7 Flip Chip. The manufacturer shall define, baseline, monitor, and control the attach process. The process shall define and document as a minimum, the solder ball composition and diameter, attach method, pre-form size, attach materials composition, equipment set-up, temperature profile, and inspection criteria. The Flip Chip Pull-Off test documented in the MIL-STD-883 TM 2031 shall be used only as a starting point and shall not be used for process control limits.

5.2.8 Tape bond. The manufacturer shall define, baseline, monitor, and control the tape bond process. The process shall define and document as a minimum, the attach method, attach materials composition, equipment setup, and inspection criteria. The Tape bond automated bonding inspection documented in the MIL-STD-883 TM 2035 shall be used, or a qualified equivalent.

5.2.9 Die/Substrate Attach. The manufacturer shall define, baseline, monitor, and control the attach process. The process shall define and document as a minimum, the attach method, pre-form size, attach materials composition, equipment set-up, temperature profile, curing time, and inspection criteria. The shear strength documented in the MIL-STD-883 TM 2019 shall be used only as a starting point and shall not be used for process control limits.

5.2.10 Lid Seal. The manufacturer shall define, baseline, monitor, and control the lid seal process. The process shall define and document as a minimum, vacuum bake temperature and time, sealing method, sealing environment (Argon, Helium, etc.) glove box controls (moisture, Oxygen, pressure, air flow), sealing materials composition, equipment set-up, temperature profile, and inspection criteria. The lid seal process shall be controlled such that the sealed components contain less than 5000 ppm of moisture, no corrosive gasses and or compounds, and shall not have any loose particles that could bridge or damage the devices.

5.2.11 Lead Trim. The manufacturer shall define, monitor, and control the lead trim process. As a minimum, the tooling and equipment, equipment set-up, and verification process shall be defined and controlled. The devices shall not have exposed metal, damaged lead seals, damaged leads, or otherwise degrade after lead trim operation.

5.2.12 Final Lead Finish. The manufacturer shall define, monitor, and control the lead finish process. As a minimum, the tooling and equipment set-up, depth of immersion, verification process for the finish composition, and lead finish method, shall be defined and controlled. The devices shall not be stripped and re-plated unless this process has been qualified for the package and technology proposed. Pure tin plating, cadmium or zinc plating shall not be used. Tin shall be alloyed with a minimum of 3 percent lead (Pb) by weight.

5.2.13 Changes. All changes shall be controlled in accordance with MIL-PRF-38535 for Class V.

5.2.14 Verification and Validation. The Contractor shall ensure that all Infant Mortality and Early Life Failures are removed from the flight microcircuit population and all microcircuits perform as specified over the specified operating conditions, temperature environments, radiation environments, and mechanical environments for the required mission life. There are several test methodologies: Stress Tests Driven, Application Specific, and Physics-of-Failure.

5.2.15 Stress Test Driven. This involves subjecting the lot to a predetermined sequence of accelerated tests, covering the worst-case environments and application conditions plus a predetermined margin, to eliminate the infant mortality and early life failures. These tests are classified as screens, parametric, wear-out, package, environmental, and life tests and shall form a part of the security requirements.

5.2.16 Screening. All microcircuits delivered shall be tested to eliminate manufacturing defects causing infant mortality and early life failures. Unless otherwise approved by the program the microcircuits shall meet the requirements of MIL-PRF-38535 Table 1A with the additional requirements of Appendix B for Class V, or MIL-STD-883 TM 5004 for Class S.

5.2.17 Qualification and Quality Conformance Inspection. Qualification and Quality Conformance Inspection shall meet MIL-PRF-38535 for Class V, or MIL-STD-883 TM 5005 for Class S.

5.2.18 Application Specific. A predetermined sequence of tests based on the application conditions designed to validate the microcircuit performance with margin for a specific application. This typically is less robust than the Stress Test Driven methodology in eliminating the infant mortality and early life failures from the population and should only be used on a limited basis driven by program necessity.

5.3 Physics-of-Failure for New Technology. A test or, sequence of tests applied to destruction, which target specific failure mechanisms to model and predict the Time to Failure. This is useful in new technologies characterization and identification of failure mechanisms. The tables below define the major known failure types and failure mechanisms with their most commonly associated failure models. The accelerating factors and failure mechanisms shall be considered when defining the stress test sequence in these situations.

Table 900-4. Electron-Migration Failure Mechanism

Model	Constraint
$T_F = A_0 (J - J_{crit})^{-N} \exp (E_a / kT)$ J will be greater than J_{crit} when failures occur, J_{crit} = critical (threshold) current density J_{crit} is inversely related to the Blech length for the line being evaluated, i.e., $J_{crit} * L_{crit} \cong 6000$ A/cm, typical for aluminum alloys (L_{crit} , JL product is approximately constant) When the test stripe length is ~60 µm, then J_{crit} is comparable to normal EM stressing current densities near 1 MA/cm^2, Layered metal systems exhibit N = 2 for incubation period or N =1 for resistance-rise period E_a = 0.5 – 0.6 eV for Al and Al + small percent Si E_a = 0.7 – 0.9 eV for Al + Al alloys doped with a small percent Cu, or 100 percent Cu For unipolar current waveforms, J is the average current density $< J >$ For bipolar waveforms a “sweep-back’ recovery action takes place and the effective current density J is described by $J = < J_+ > - r < J_- >$, where $< J_+ >$ is the average of the positive polarity pulses and $< J_- >$ is the average of the negative polarity pulses. The recovery factor r has a value of at least 0.7.	For Al-alloy stripes, terminated by bonding pads and having no barrier metallization the total time-to-failure is dominated by nucleation N=2 For Al-alloy stripes on barrier metal and terminated by tungsten plugs the total time-to-failure includes both nucleation (N=2) and resistance rise (drift period) N=1 Under high-current-density test conditions, unaccounted self-heating can produce *apparent* current-density exponents *much* greater than 2 NIST bow-tie type EM test structure with simple bonding pad connections is inadequate for multilevel metal systems and gives optimistic EM results for via-fed test structures

Table 900-5. Corrosion Failure Mechanism

Model	Constraint
Reciprocal Exponential *TF* = *C0* x exp [*b/RH*] x f(*V*) x exp [*Ea /kT*] *C0* = empirical scale factor, *b* = ~300 *a* = 0.3 eV, f(V) = an unknown function of applied voltage	Corrosion failures occur when ULSI devices with pure aluminum or aluminum alloys (small percent Cu and Si) metallization are in the presence of moisture and contaminants. Corrosion failures are either bonding-pad corrosion or internal corrosion. Bond pad corrosion is more common because the die passivation does not cover the metallization in the bond pad locations. Internal corrosion (internal to the chip, away from the bond pads) is attributed to weakness or damage in the die passivation, permitting moisture to reach the metallization. The models assume mathematically separable, independent variables
Power law (Peck) *TF* = *A0* * *RH-N* * f(V) * exp[*Ea /kT*] *A0* = empirical scale factor *N* = ~2.7 *Ea* = 0.7-0.8 eV f(V) = an unknown function of applied voltage	
Exponential *TF* = *B0* * exp [-*a* •*RH*] * f(V) * exp [*Ea /kT*] *B0* = empirical scale factor *a* = (0.10 – 0.15)/RH(%) *Ea* = 0.7- 0.8 eV f(V) = an unknown function of applied voltage	
RH^2 model (Lawson) TF = C0 * RH2 * f(V) * exp [Ea /kT] *C0* = empirical scale factor, (typical value 4.4×10^{-4}) *RH* = Relative Humidity as percent (100% = saturated) *a* = 0.64 eV f(V) = an unknown function of applied voltage	

Table 900-6. Time-Dependent Dielectric Breakdown (TDDB) Failure Mechanism

Model	Constraint
Reciprocal Exponential $T_F = C_0$ x exp [b/RH] x f(V) x exp [E_a /kT] C_0 = empirical scale factor, b = ~300 a = 0.3 eV, f(V) = an unknown function of applied voltage	Corrosion failures occur when ULSI devices with pure aluminum or aluminum alloys (small percent Cu and Si) metallization are in the presence of moisture and contaminants. Corrosion failures are either bonding-pad corrosion or internal corrosion. Bond pad corrosion is more common because the die passivation does not cover the metallization in the bond pad locations. Internal corrosion (internal to the chip, away from the bond pads) is attributed to weakness or damage in the die passivation, permitting moisture to reach the metallization. The models assume mathematically separable, independent variables
Power law (Peck) $T_F = A_0 * RH^{-N} *$ f(V) * exp[E_a /kT] A_0 = empirical scale factor N = ~2.7 E_a = 0.7-0.8 eV f(V) = an unknown function of applied voltage	
Exponential $T_F = B_0$ * exp [$-a \cdot RH$] * f(V) * exp [E_a /kT] B_0 = empirical scale factor a = (0.10 – 0.15)/RH(%) E_a = 0.7- 0.8 eV f(V) = an unknown function of applied voltage	
RH^2 model (Lawson) $T_F = C_0 * RH^2 *$ f(V) * exp [E_a /kT] C_0 = empirical scale factor, (typical value 4.4 x 10^{-4}) RH = Relative Humidity as percent (100% = saturated) a = 0.64 eV f(V) = an unknown function of applied voltage	

Table 900-7. More Physics of Failure

Failure Mechanism	Model	Constraints
Hot Carrier Injection (HCI)	Typically HCI can be described by: $\Delta p = At^n$ p is the parameter of interest (V_t, g_m, I_{dsat}, etc.), t is the time A is a material dependent parameter n is an empirically determined exponent, a function of stressing voltage, temperature, and effective transistor channel length. N-channel model $T_F = B(I_{sub})^{-N} \exp(E_a/kT)$ B = empirical scale factor (strong function of proprietary factors such as doping profiles, sidewall spacing dimensions, etc.) I_{sub} = peak substrate current during stressing *N* = 2 to 4 E_a = -0.1 eV to -0.2 eV (note the apparent activation energy is negative) P-channel model $TF = B(I_{gate})^{-M} \exp(E_a/kT)$ B = empirical scale factor (strong function of proprietary factors such as doping profiles, sidewall spacing dimensions, etc.) I_{gate} = peak gate current during stressing. *M* = 2 to 4 *a* = -0.1 eV to -0.2 eV	Hot carrier injection describes the phenomenon by which carriers gain sufficient energy to be injected into the gate oxide The dominant wearout mode for most processes is “conductive” mode (high V_{gs}, V_{ds}), but degradation in “non-conductive” mode (low V_{gs}, high V_{ds}) should also be considered. For sub-0.25 µm P-channel, the drive current tends to decrease like NMOS after hot carrier stress For sub-0.25 µm P-channel, worst case lifetime occurs at maximum substrate current stress. The T_F model is the same as N-channel The drive-currents for the n-channel transistors tends to decrease after HCI stressing, the p-channel drive current tends to decrease It appears that HCI physics may be starting to change at 0.25 µm and smaller, leading to changing worst-case stress conditions Typically, HCI degradation causes reduced circuit speed rather than catastrophic failure The temperature-dependent model for V_{cc}<2.5V is still under investigation A rough "rule-of-thumb”, for the gate current vs. voltage dependence of P-channel devices is peak gate current doubles for each 0.5V increase in source-drain voltage (V_{ds})

Table 900-7. More Physics of Failure (Continued)

Failure Mechanism	Model	Constraints
Surface Inversion (mobile ions)	Model $T_F = A\ (J_{ion})^{-1} \exp(E_a/kT)$ A = material constant $Ji_{on} = <(eD_0\rho E/kT) - (D_0 \partial \rho(x,t)/\partial x)>$ is the average flow of ions $(eD_0\rho E/kT)$ is the *drift* current $(D_0 \partial \rho(x,t)/\partial x$ is the *back-diffusion* component E = electric field e = charge on the electron D_0 = diffusion coefficient ρ = density of mobile ions E_a = activation energy	Activation energy for mobile-ion diffusion depends on: diffusing species medium through which the mobile ions diffuse The concentration of the contaminant Activation energies have been observed from 0.75 to 1.8 eV for Na+, with eV being typical. For large Na+ concentration & bulk silica (not thin film), activation energy were at the low end, while a larger activation energy was seen in typical semiconductor devices
Stress Migration	Mechanical stress model $T_F = A_o\ (\sigma)^{-n} \exp(E_a/kT)$ A_o is a constant σ = constant stress load n = 2-3 for ductile metal E_a = 0.5 - 0.6 eV for grain boundary diffusion, ~ 1 eV for single grain (bamboo-like) diffusion Thermomechanical stress model $T_F = B_0\ (T_0 - T)^{-n} \exp(E_a/kT)$ B_0 is a constant T_0 = stress free temperature for metal (approximate metal deposition temperature for aluminum) n = 2 – 3 E_a = 0.5 - 0.6 eV for grain-boundary diffusion, ~ 1 eV for intra-grain diffusion	The term stress migration describes the movement of metal atoms under the influence of mechanical-stress gradients Stress gradients can be assumed to be proportional to the applied mechanical stress Model applies to aluminum alloys (doped with Cu and/or Si) Typically, long (> 1000 µm) and narrow (< 2 µm width) stripes are stored (unbiased) at temperatures of 150-250°C for 1-2 kh and then electrically tested for resistance increases or reduction in breakdown currents Maximum in the creep rate (generally 150-250ºC) occurs due to the high stress but low mobility at low temperatures, and low stress but high mobility at high temperatures

Table 900-7. More Physics of Failure (Continued)

Failure Mechanism	Model	Constraints
Dielectric/thin-film cracking Lifted bonds Fractured/broken bond wires Solder fatigue (joint/bump/ball) Cracked die Lifted die	Temperature cycling and thermal shock Coffin-Manson models $Nf = A_0 [1/\Delta\varepsilon p]^B$ N_f = cycles to failure A_0 = a material constant $\Delta\varepsilon P$ = plastic strain range, which is the difference in strain per cycle B = an empirically determined constant Modified Coffin-Manson equation Elastic deformation equation: $\Delta\varepsilon P \propto (\Delta T - \Delta T0)^B$ Plastic deformation equation: $N_f = C0 [\Delta T - \Delta T0]^{-q}$ N_f = Number of cycles to failure, C_0 = a material-dependent constant, ΔT = entire temperature cycle-range for the device, ΔT_0 = the portion of the temperature range in the elastic region, q = the Coffin-Manson exponent, an empirically derived constant, unique to each failure mechanism. For ductile metal, e.g., solder q is between 1-3 hard metal alloys / intermetallics (e.g. Al-Au) q is between 3-5 brittle fracture (e.g. Si and dielectrics : SiO_2, Si_3N_4) q is between 6-9	"Linearity" is assumed, i.e., modeling parameters are constant over the range of interest (stress vs customer application) Alternative methods are needed for reliability estimates (AF or FITs) if the temperature cycle range crosses a critical temperature causing dramatical material property changes over the temperature range of interest such as T_g (glass transition temperature of the polymer) Modified Coffin-Manson model is used when the temperature cycle includes both the elastic and plastic deformations.

5.4 REGISTERED (RELIABILITY SUSPECT) PMP. The following microcircuit types and technologies are considered reliability suspect and shall not be used unless approved by the program (listed in parenthesis are the reasons of concern):

a. Hot welded cans (Uncontrolled Weld Splatter)

b. Plastic encapsulated units (Uncontrolled materials/processes, and variability of performance due to temperature, bimetallic lead bond at die).

c. Packages other than those defined in MIL-STD-1835

d. Programmable units, which do not program with a single pulse (EEPROMs, Fusible link process deficiencies)

e. Internal organic/polymeric materials (lacquers, varnishes, coatings, adhesives, or greases)

f. Flip chip

g. Beam leaded, column grid array, and ball grid array devices Lack of process control leading to intermittency

h. Bimetallic lead bond at die (Intermetallic Formation)

i. Fume etching

j. Laser trimmed elements on the chip (debris, resulting in unglassivated die surfaces)

k. Flash memory devices (considered new technology)

l. Bimetallic bonds at die. See paragraph 4.3.6 of Section 4 of this document.

6. PROHIBITED PMP shall include:

a. Non-passivated devices (No insulation from conductive particles)

b. Internal desiccants (Out-gassing concerns)

c. Ultrasonically cleaned packaged parts (Latent damage)

d. Devices using prohibited materials in their construction (see Section 4, General Requirements, paragraph 4.3.3 of this document)

7. PROCUREMENT. The contractor shall be responsible for implementing and managing a supplier control program to control, manage, and verify the procurement of microcircuit devices from microcircuit Original Equipment Manufacturers (OEM), or their franchised/authorized distributors. As a minimum, the contractor shall address supplier selection, supplier verification, supplier corrective action, supplier rating, frequency of supplier audits, etc. In addition, the contractor shall define the incoming receiving inspection performed on received microcircuits including verification, data review and supplier required data items, shelf life control, microcircuit storage and kitting, ESD handling, etc.

7.1 Incoming Inspection DPA. The procuring activity shall verify the workmanship and the internal Design and Construction through a Destructive Physical Analysis (DPA) performed by the procurement activity or at an independent laboratory. The DPA shall meet MIL-STD-1580 unless otherwise approved by the program. DPA sampling should be relative to lot homogeneity as specified in paragraph 4.1.1. EEEE parts which contain internal cavities, DPA may be performed on parts already subjected to Residual Gas Analysis (RGA) testing. Additionally, one of the DPA samples from each test lot shall be maintained for correlation purposes and future analysis if failures are observed.

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SECTION 910

INTEGRATED CIRCUITS

See Section 900 Microcircuits

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SECTION 960

HYBRIDS

(MIL-PRF-38534, CLASS K)

1. SCOPE. All hybrids selected for the system application shall meet the requirements specified herein, unless otherwise approved by the program. This section covers the selection of hybrid microcircuits, open-chip construction hybrids, chip-on-board and Multi Chip Modules for space application. RF/microwave devices used in hybrids shall be designed and selected in accordance with section 1300.

2. APPLICATION. The hybrid device quality and reliability level, critical parameters, and environments for the system application shall be established as defined below. The hybrid application in the system shall form the basis for the technical requirements of each hybrid and critical performance parameters. System application considerations shall include areas such as hybrid thermal, mechanical, radiation, derating, End-of-Life limitations, mounting recommendations, and other design considerations necessary to ensure the high reliability of the parts as used in each space vehicle application. The design and construction, and the quality assurance requirements shall be established and documented in specifications to ensure their performance and the necessary quality for space applications.

2.1 Hybrid Selection. The selected devices shall have demonstrated the ability through characterization and test to meet the worst-case requirements (application and acceptance/qualification) with margin to compensate for manufacturing variations and End-of-Life considerations. The contractor shall ensure that the worst-case conditions include recognition of ground tests performed at the subsequent levels of integration and not only those seen during flight. Where assessment data does not exist, the contractor shall define the technical criteria detailing how the capability of each selected device will be verified.

2.2 Hybrid Standardization. The number of different hybrid types/part numbers and the use of previously qualified or approved hybrid types/part numbers for equivalent applications shall be optimized.

2.3 Design Analysis. Circuit design analysis shall be performed to establish the electrical stresses such as voltage, current, power, etc for each element under hybrid nominal and maximum rated operating conditions. The circuit design shall make allowances for worst-case variations, to compensate for manufacturing variations and End-Of-Life parameter limits in the following as a minimum, but not limited to: input and output voltages; input and output currents; power dissipation; propagation delays; electromagnetic compatibility (EMC), operating junction temperature, operating frequency. Critical performance parameters shall be identified such that they can be documented in the detailed specifications, including appropriate verification requirements.

2.4 Thermal Analysis. Thermal analysis shall be performed to ensure the selected components/elements are used within the specified derated temperature limits of the part. The derated temperature shall be based on the original die manufacturer/design activity published value. Elements used outside of the published values shall be qualified by a plan approved by the program.

2.5 Mechanical Analysis. Mechanical stress analysis shall be performed to establish the mechanical stress for each component/element inside the hybrid, including those incurred during hybrid and next assembly manufacturing, handling, and testing. The mechanical design shall make allowances for worst-case variations in mechanical stress due to temperature excursions, mismatches of thermal coefficient of expansion, mechanical shock, mechanical and acoustical vibration.

2.6 Radiation Environment Considerations. The effects of the expected radiation environments on the hybrid and internal elements performance in the application shall be analyzed and or tested to verify successful operation. These include Single Event Upset (SEU), Single Event Latch-up (SEL), Single Event Burn-out (SEB), Single Event Transient (SET), Single Event Gate Rupture (SEGR), and Total Dose Radiation (high dose, and ELDRS conditions). All mitigation strategies shall be documented. The environments addressed shall include the expected natural space environment calculated over the intended life of the mission and any additional nuclear enhanced environment specified in the system specification.

2.7 Design Margin. A design criterion shall be established, documented, and verified for all selected microcircuit devices to provide adequate performance that meets the application requirements. The design margin shall cover electrical, thermal, mechanical, and radiation performance margin over the worst-case conditions.

2.8 Derating

2.8.1 Internal Elements Derating

Electrical Stress. Each hybrid element shall be derated for electrical stress (e.g. voltage, current, power) in accordance with the element's technical section of this document (i.e. microcircuits shall be derated per Section 900, semiconductors shall be derated per Section 1400, solid tantalum capacitors shall be derated per Section 270, etc.), except for resistors, where derating to zero power shall occur at the maximum rated temperature of the part as specified in the applicable MIL spec or SCD.

Temperature Stress. Hybrid elements shall be derated for temperature such that when *the hybrid* is operated at its maximum operating temperature during burn-in or life test, the active elements shall not exceed 90% of their manufacturers' maximum temperature ratings and passive elements shall not exceed 3 ^{o}C above their military specification maximum rated operating temperature.

2.8.2 Hybrid Derating

Temperature. Hybrids shall be derated from their maximum rated operating temperature as follows:

Nominal Conditions: Tj Max. = 80% of maximum rated Tj or 105 ^{o}C, whichever is less

Worst-Case Conditions: Tj Max. = 90% of maximum rated Tj or 125 ^{o}C, whichever is less.

At no time during powered testing shall the hybrid be operated above its maximum rated operating temperature or 125 ^{o}C, whichever is less.

2.9 End-of Life-Design. End-of-life design limits shall be the maximum specified parametric limits for high and low temperature performances unless otherwise established by testing or analysis.

3. DESIGN AND CONSTRUCTION

3.1 Requirements. Design and construction shall be in accordance with the requirements of MIL-PRF-38534, Class K, and as specified below.

3.2 Packaging. Packaging shall be in accordance with MIL-PRF-38534, Class K.

3.3 Traceability. Traceability shall be in accordance with MIL-PRF-38534 for Class K. Lot homogeneity shall be demonstrated. Active elements shall be shown to be traceable to the same diffusion run for a single wafer. Passive elements shall be shown to be from one production lot as defined in Table 960-3 or the applicable mil/government specification referenced in Table 960-3.

3.4 Configuration Control. Configuration Control shall be in accordance with MIL- PRF-38534 Class K.

3.5 Serialization. Serialization shall be in accordance with MIL-PRF-38534, Class K.

3.6 Rework. Rework and rework qualification shall be in accordance with MIL-PRF-38534 for Class K. Reworked hybrids with non-homogeneous elements, identified by Serial Number per M38534, shall be represented in the QCI samples during testing of the hybrid lot. All elements used for rework shall satisfy the basic element evaluation tests including radiation testing as required.

3.7 Workmanship. Workmanship shall be in accordance with MIL-PRF-38534 Class K. Particular attention shall be given to wire stress relief, material controls, materials verification of filled epoxies, backside metallization verification, and prevention of gold embrittlement.

4. QUALITY ASSURANCE. Quality assurance shall be in accordance with MIL-PRF-38534, Class K, and as follows:

4.1 Element Evaluation. For dc-dc converter hybrids (Including switching power supply hybrids), element evaluation shall be in accordance with MIL-PRF-38534, Class K, as modified by this section, and Table 960-1, Table 960-2, and Table 960-3. For all other hybrids, element evaluation shall be in accordance with MIL-PRF-38534, Class K.

Any new technology device used within the hybrid shall have a characterization and qualification plan approved by the program, and be fully characterized and qualified prior to use.

Microcircuit and semiconductor die shall meet the traceability requirements of MIL-PRF-38534 for Class K. The sample size for all non-QML/QPL Class V/S die or non-JANKC die that were processed on an approved QML/QPL line shall be per MIL-PRF-38534 for Class K. QML/QPL Class V or S or JANKC certified die from the manufacturer do not require additional element evaluation by the hybrid manufacturer except die visual inspection. Die from QPL/QML wafers not meeting the QPL/QML requirements and downgraded to commercial grade shall not be used.

4.2 Process Control. Process control shall be in accordance MIL-PRF-38534, Class K. Test optimizations are not allowed unless substantial supporting data can demonstrate that the long-term reliability and performance of the part is not affected in any way by the deletion of the test(s).

4.3 Screening (100 percent). Screening (100 percent) shall be in accordance with MIL-PRF-38534, Class K. Test optimizations are not allowed unless substantial supporting data can demonstrate that the long-term reliability and performance of the part is not affected in any way by the deletion of the test(s).

4.4 Quality Conformance Inspection. QCI shall be in accordance with MIL-PRF-38534, Class K. Test optimizations are not allowed unless substantial supporting data can demonstrate that the long-term reliability and performance of the part is not affected in any way by the deletion of the test(s).

4.5 Hybrid Characterization and Qualification. The hybrid shall be fully characterized and qualified for space application in accordance with MIL-PRF-38534 Class K. All failure modes shall be identified and mitigated. JEDEC Publication 122 provides a good starting point for failure modes identification and reliability assessment. The mitigation shall fully document the tests and results, pass/fail criteria, and design strategies applied as appropriate. Where assessment data do not exist, the contractor shall define and describe how the capability of each selected device will be verified. This shall include the configuration controls that ensure the flight devices are form, fit, function, and performance equivalent to the evaluated parts. A worst-case analysis and survivability analysis shall be submitted along with all qualification and characterization data.

4.6 Quality Assurance Plan. A quality assurance plan shall be established in accordance with Appendix A of MIL-PRF-38534, Class K technical requirements.

4.7 Incoming Inspection DPA. The procuring activity shall perform an incoming inspection DPA in accordance with MIL-STD-1580. In addition, elements inside hybrids shall be DPA'd per the applicable requirements section of this document. All metal surfaces shall be verified for the absence of prohibited materials (e.g., pure tin, zinc, or cadmium).

5. REGISTERED (RELIABILITY SUSPECT) PMP shall include:

a. Bonding one resistor chip, or any other element, on top of another to change a design or save on real estate is not allowable without extensive design/process verification, long-term testing, and hybrid requalification.

b. Bimetallic wirebonds at die. See paragraph 4.3.6 of Section 4 of this document.

6. PROHIBITED PMP shall include:

a. Any device with prohibited parts (see individual commodity section for listing) in its construction.

b. Any device with prohibited materials in their construction (see Section 4, General Requirements, paragraph 4.3.3 of this document).

Table 960-1. Microcircuit Die Evaluation Requirements

Class K	Element Quality Level			Test	MIL-STD-883		Quantity (accept number)	Reference Paragraph in MIL-PRF-38534
					Method	Condition		
	QML S/V 8/	QML B/Q 9/	Other					
Sub-group								
1	X	X 1/	X 1/	Element Visual	2010	A	100 percent	C.3.3.2
2		X	X	Element Electrical	2/		100 percent	C.3.3.1
3		X 4/	X	Internal Visual	2010	A	All Packaged Samples	C.3.3.3 C.3.3.4.2
		X 4/	X	Initial Electrical	5/			
4		X 4/	X	Temperature Cycling	1010	C	10(0) for QML B/Q, or 22(0) for "Other" 3/	C.3.3.3
		X 4/	X	Mechanical Shock or Constant Acceleration	2002 2001	B, Y1 orientation or E, Y1 orientation		
		X 4/	X	Interim Electrical	5/			C.3.3.4.3
		X 7/	X 7/	Technology Unique Tests	7/	7/		
		X 4/	X	Burn-in	1015	D		
		X 4/	X	Post Burn-in Electrical	5/			C.3.3.4.3
		X 4/	X	Steady-state Life	1005	D		
		X 4/	X	Final Electrical	5/			C.3.3.4.3
5	X	X 4/	X	Wire Bond Evaluation	2011	Bake for 1 hour @300ºC, for non mono-metallics	22(0) wires or 38 (1) wires 6/	C.3.3.3 C.3.3.5
6		X	X	SEM	2018		See method 2018	C.3.3.6

Notes:

1/ For hybrids utilizing other than QPL S/QML V wafer banked die, and Class H hybrids using other than QPL S/QML V or QPL B/QML Q wafer banked die, an assessment shall be performed and documented as to meeting the requirements of MIL-STD-883, Method 5007 and approval shall be obtained from the acquisition activity.

2/ As a minimum, all practical DC parametrics, and functional testing, per die manufacturer's data sheet, procurement documentation, or DSCC approved military specification, shall be performed at 25°C.

3/ Deleted.

4/ For hybrids utilizing QPL B/QML Q die (with OEM C of C), subgroups 3, 4, and 5 can be omitted if the subject wafer run was subjected to QCI per MIL-STD-883, Method 5005.

5/ Full DC and AC parametrics, per the die manufacturer's data sheet or approved military specification and hybrid worst-case analysis, at minimum operating temperature, +25°C, and maximum operating temperature shall be performed with read and record data. In addition, delta parametrics shall be read and recorded where applicable.

6/ Wires selected for evaluation shall be distributed evenly across all samples, and shall reflect the wire bond system to be used for the flight hybrid.

7/ Appropriate tests (static burn-in, HTRB, etc.) and conditions shall be used as warranted for the applicable technology as documented in the detailed military specification slash sheet or SMD.

8/ Or SCD-procured die to full Class S/V requirements.

9/ Or SCD-procured to full Class B/H requirements.

Table 960-2. Semiconductor Die Evaluation Requirements

Class	Die Quality Level			Test	MIL-STD-750		Quantity (accept number)	Reference Paragraph in MIL-PRF-38534
	KC 8/	HC 9/	Other		Method	Condition		
Sub-group								
1	X	X 1/	X 1/	Element Visual	2069 2070 2072 2073		100 percent	C.3.3.2
2		X	X	Element Electrical	2/		100 percent	C.3.3.1
3		X 4/	X	Internal Visual	2069 2070 2072 2073 2074		All Packaged Samples	C.3.3.3 C.3.3.4.2
		X 4/	X	Stabilization 11/	1032	T_{STG} ≤ maximum rated storage temperature, t = as specified		
		X 4/	X	Initial Electrical	5/			C.3.3.4.3
4		X 4/	X	Temperature Cycling	1051	C	10(0) for QML HC, or 22(0) for "Other" 3/	C.3.3.3
		X 4/	X	Surge (when applicable) 7/	4066	A or B as specified		
		X 4/	X	Constant Acceleration or Mechanical Shock	2006 2016	Y1 orientation 3,000 G's or Y1 orientation 1,500 G's for 0.5 msec		
		X 4/	X	Interim Electrical	5/			C.3.3.4.3
		X 4/	X	High Temperature Reverse Bias (HTRB)	1039 1042 1038	A B A		
		X 4/	X	Interim Electrical Testing and Delta Calculations	5/	Complete within 16hrs of HTRB completion		C.3.3.4.3
		X 6/	X 6/	Technology Unique Tests	6/	6/		

Table 960-2. Semiconductor Die Evaluation Requirements (cont'd)

Class	Die Quality Level			Test	MIL-STD-750		Quantity (accept number)	Reference Paragraph in MIL-PRF-38534
	KC 8/	HC	Other		Method	Condition		
Sub-group								
4		X 4/	X	Burn-in 240 hrs	1039 1042 1038 1040	B A B	10(0) for QML HC, or 22(0) for "Other" 3/	
		X 4/	X	Post Burn-in Electrical	5/			C.3.3.4.3
		X 4/	X	Steady-State Life 1000hrs, or equivalent, per MIL-PRF-19500	1026 1037 1042 1048			
		X 4/	X	Final Electrical	5/			C.3.3.4.3
5		X 4/	X	Wire Bond Evaluation	2037	Bake for 1hr @300ºC for non mono-metallics	10(0) wires or 20(0) wires 10/	C.3.3.3 C.3.3.5
6		X	X	SEM	2018 2077		See method 2018 or 2077	C.3.3.6

Notes:

1/ For hybrids utilizing other than JANKC die, a wafer acceptance assessment shall be performed and documented as to meeting the requirements of MIL-PRF-19500, Appendix E and approval shall be obtained from the acquisition activity.

2/ As a minimum, all practical DC parametrics, and functional testing, per die manufacturer's data sheet, procurement documentation, or DSCC approved military specification, shall be performed at 25°C.

3/ Deleted.

4/ For hybrids utilizing JANHC die (with OEM C of C), the indicated elements of subgroups 3, 4, and 5 can be omitted if the subject wafer run was subjected to QCI per MIL-PRF-19500.

5/ Full DC and AC parametrics at min operating temperature, +25°C, and max operating temperature shall be performed with read and record data. In addition, delta parametrics shall be read and recorded data where applicable.

6/ Appropriate tests (static burn-in, HTRB, etc.) and conditions shall be used as warranted for the applicable technology as documented in the detailed military specification slash sheet or SMD.

7/ As specified in MIL-PRF-19500 slash sheet, or by device type.

8/ Or SCD-procured die to full KC requirements.

9/ Or SCD-procured die to full HC requirements.

10/ Wires selected for evaluation shall be distributed evenly across all samples and shall reflect the wire bond system to be used for the flight hybrid.

11/ As specified in MIL-PRF-19500 slash sheet, or by device type. If required, test duration is 48 hours unless otherwise specified.

Table 960-3. Element Evaluation Requirements for Passive Parts

Part Type	Test	Requirements Paragraph	Sample Size	Allowable Reject(s)
Ceramic capacitors. Production lot definition shall be per M55681 or M123 for chips, or M49470 T-level for stacks.				
M55681 FRL S or M123 (chips)	N/A	N/A	N/A	N/A
DSCC Dwg, COTS (chips)	Ultrasonic scan or CSAM, except single-layer ceramic capacitors (SLCCs)	M123	100 percent	N/A
	Group A	M123	M123	M123
	Group B, Subgroups 1 & 2 if part is used in <10V applications, or Subgroups 1 & 3 if part is used in >10V applications.	M123	M123	M123
T-level M49470 (stacked)	N/A	N/A	N/A	N/A
General-purpose M49470, DSCC dwg, or COTS (stacked)	Ultrasonic scan or CSAM	M49470 for T-level	100 percent	N/A
	Group A	M49470 for T-level	M49470 for T-level	M49470 for T-level
	Group B, Subgroups 2, 4 & 5b	M49470 for T-level	M49470 for T-level	M49470 for T-level
Tantalum Chip Capacitors. Stacking tantalum chips shall require a repeat of the entire Group A in M55365 with minimum Weibull C and surge current option C. Production lot definition shall be per M55365.				
M55365, T-level	N/A	N/A	N/A	N/A
M55365	Group A (Weibull C minimum with surge current option C)	M55365	M55365	M55365
DSCC Dwg, COTS	Group A (Weibull C minimum with surge current option C)	M55365	M55365	M55365
	Group C except Subgroup IV	M55365	M55365	M55365
Crystals. Packaged crystals used in oscillators shall meet all the requirements of Section 400 of this document, while unpackaged (bare) crystals shall meet all the visual inspection requirements specified in para. 4.1.1 of Section 400.				
Resistor Chips. Production lot definition shall be per M55342.				
M55342 FRL R or S, U, V or T-level	N/A	N/A	N/A	N/A
DSCC Dwg (except those listed in the Space Quality Baseline of TOR-2006(8583)-5235), COTS	Group A	M55342 for T-level	M55342 for T-level	M55342 for T-level
	Group B	M55342 for T-level	M55342 for T-level	M55342 for T-level

Table 960-3. Element Evaluation Requirements for Passive Parts (Continued)

Part Type	Test	Requirements Paragraph	Sample Size	Allowable Reject(s)
Wire-bondable COTS Chip Resistors with no end cap terminations	Shall be in accordance with the Inspection of Product for Delivery per MIL-PRF-55342 for ER chips (Group A, Subgroups 1, 2 & 3, and Group B), and the following exceptions: Group A, Subgroup 2, shall be performed on a ten (10) piece sample per resistance value per production lot that will also be used for the Group C, Subgroup 1, life test. Lot Control – Each lot shall be from the same sputtering or evaporation run and shall be photo-etched with the same process within a 48-hour period and using the same mask set. Life Test (Group C, Subgroup 1, for stability verification) shall be in accordance with MIL-PRF-55342 for 1000 ±8 hours, except sampling shall be 10 pieces per resistance value per production lot. Change in resistance shall not exceed ±0.5% after life test. Samples shall have passed Group A, Subgroups 1, 2 and 3, but not subjected to Group B.			
Magnetics (Open Construction 1/, 2/, and Closed Construction) 3/, 4/	Group A	MIL-STD-981	MIL-STD-981	MIL-STD-981
	Group B	MIL-STD-981	MIL-STD-981	MIL-STD-981
1/ Group A is not required for open construction/self-leaded devices, with a minimum wire size of 36 gauge, and are 100% visually inspectable. Also included in this category are magnetic devices using pot cores built by the hybrid manufacturer, where the wound magnetic elements are 100% visually inspected prior to insertion in the pot cores and prior to core lid-attach. For these devices, only 100% visual inspection and electrical tests per MIL-STD-981 for Class S are required. Electrical tests shall include as a minimum: dielectric withstanding voltage (DWV), insulation resistance (IR), induced voltage (when required), inductance, corona test (when required), and all other electrical characteristics required by the applicable MIL spec. 2/ Group B is not required for open construction/self-leaded devices, with a minimum wire size of 36 gauge, including pot core magnetics, that are 100% visually inspected by the hybrid manufacturer prior to insertion into the pot core and before core lid-attach. Visual inspection criteria shall be per the Class S requirements of MIL-STD-981. 3/ All magnetics shall meet the design, construction, workmanship materials/processes requirements of MIL-STD-981, Class S. 4/ Stacking magnetics shall be qualified and the effects to the long-term performance of the hybrids verified. When stacking already fully compliant magnetics, a repeat of the thermal cycling plus all the electrical tests as specified in Group A of MIL-STD-981, Class S, shall be performed. Electrical tests shall include as a minimum: dielectric withstanding voltage (DWV), insulation resistance (IR), induced voltage (when required), inductance, corona test (when required), and all other electrical characteristics required by the applicable MIL spec.			
Thermistors shall be in accordance with Section 1195 of this document.				

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SECTION 1000

RELAYS (CURRENT RATINGS OF 25 AMPERES OR LESS)

1. SCOPE. This section sets forth detailed requirements for electromechanical relays with current rating of 25 amperes or less. All parts selected for the system application shall meet the requirements specified herein. Alternate approaches to meeting particular requirements shall be proven equivalent or more stringent than specified herein.

2. APPLICATION. Selection and application of relays shall be in accordance with MIL-STD-1346 and the requirements contained herein.

2.1 Capacitive Load. Series resistance shall be used with any capacitive load to ensure that currents do not exceed derated levels for resistive loads.

2.2 Suppression Diodes. External diodes are recommended for coil suppression. If coil suppression is used, a double diode configuration is preferred; wherein one diode suppresses reverse transients to two times the nominal coil voltage and the second diode provides reverse polarity protection for the primary diode. Diodes used shall conform to the JANS requirements of MIL-PRF-19500.

2.3 Coil Voltage. The following caution is specified by both MIL-PRF-6106 and MIL-PRF-39016:

Caution: The use of any coil voltage less than the rated voltage compromises the operation of the relay and will decrease the operating life cycles for a given relay. Therefore, the coil operating voltage shall not be subject to a lesser value by derating; that is, shall not be less than the rated coil voltage nor more than the maximum rated coil voltage over the operating temperature range of the relay. For pulsed applications when the duty cycle is 10 percent or less, the coil energizing voltage shall be no greater than 150 percent of the rated coil voltage, and the maximum allowable “on” time shall be 50 milliseconds.

2.4 Loads. If relay usage is at low or intermediate loads relative to the rated load for the relay, the relay shall also be qualified at the reduced (usage) load.

2.5 Derating

2.5.1 Contact Current Derating. Contact current derating shall be based on the contact load type in accordance with Table 1000-1, and the operating life of relay. Inrush currents in excess of the rated resistive load may be permitted with a corresponding reduction in life when the following criteria are met:

a. The relay has been qualified to withstand an inrush of “X” times the rated resistive load for “Y” number of cycles.

b. Lot-by-lot conformance tests are performed to verify continued compliance.

c. The actual application shall not require more than an inrush of “X” times the rated resistive load for 50 percent the specified “Y” number of cycles.

TABLE 1000-1 CONTACT CURRENT DERATING

Contact Load Type	Derating Factor from Rated Resistive Load
Resistive	0.75
Inductive	0.40
Motor	0.20
Filament	0.10
Capacitive	(See 2.1)

2.5.2 Specification Provided Rated Values. When the detail specification provides “rated values” not only for resistive loads, but also for inductive, motor, and lamp loads, the derating factor shall be 0.75. For example, the inductive load shall be derated to 0.75 times the “rated inductive load” provided in the detail specification.

3. DESIGN AND CONSTRUCTION

3.1 Requirements. Design and construction shall be in accordance with the requirements of the applicable specifications, MIL-PRF-6106, MIL-PRF-28776, MIL-PRF-39016, MIL-PRF-83536, and MIL-PRF-83726, and the requirements of this document.

3.1.1 Electronic Parts. Electronic parts that are utilized in manufacturing the relays, such as diodes, transistors, capacitors, and hybrids, shall also meet the applicable requirements stated in their sections of this document.

3.1.2 Critical Processes. The manufacturer shall document the manufacturing flow including the processes and procedures that have critical effect on the fabrication, function, reliability, or service life of the article. As a minimum, these shall include raw material certification and property sample tests, coil assembly, carrier assembly, contact assembly, armature assembly, coil core and pole piece assembly, motor assembly, relay subassembly prior to closure, and final assembly and closure. Inspections and tests associated with each process and assembly operation shall be included in the processes. As a minimum, the following items shall be considered critical materials: coil assembly, carrier assembly, contact assembly (contacts), armature assembly, coil core, pole piece assembly, motor assembly, wires, and header.

3.1.3 Magnet Wire. Coil wire should be 44 AWG or larger and use a polyimide (or equivalent) insulation. Coil wires finer than 44 AWG shall be continuously monitored during thermal shock test for continuity.

3.1.4 Final Assembly. Relays shall be assembled in a clean area. Final cleaning, inspection and storage shall be done in a controlled clean room environment with laminar flow hood, or similar measures to eliminate particulate contamination. After pre-cap visual inspections have been completed, the relay can shall be placed on the relay, and the relay sealed (canned) while in this same controlled clean room environment. If after pre-can visual inspections have been completed, but prior to sealing, the covers are removed for any reason, pre-can visual inspections shall be repeated. If for any reason subassemblies or unsealed relays are removed from the controlled clean room environment, covers or other provisions shall be used to maintain cleanliness. The relays may be remagnetized and stabilized, if applicable.

4. QUALITY ASSURANCE. Quality assurance provisions shall be in accordance with Section 4, General Requirements, of this document and the following:

4.1 In-process Controls. In-process controls shall be in accordance with the requirements of the applicable military specification, and the following:

4.1.1 Vacuum Bake. Relay coil assemblies shall be vacuum baked to ensure no coil outgassing that could cause a film buildup on the contacts that would increase contact resistance.

4.1.2 General Method of Inspection.

4.1.2.1 Visual and Mechanical Examinations. A visual examination shall be performed in a controlled clean room environment with laminar flow hood, or similar measures to eliminate particulate contamination, on 100 percent of the relays prior to final cleaning and assembly in the can.

The examination shall be performed using a 10-power microscope except when an abnormality is observed, then higher magnification (30-50X) shall be used to verify product integrity. All parts not under immediate inspection shall be stored in covered trays and returned to covered trays immediately after inspection.

4.1.2.2 Initial Inspection. Areas to be visually examined shall include:

a. Contact assembly, contact surfaces, stationary and movable contacts, springs
b. Coil, pole piece, armature, header

4.1.2.3 Final Examination for Contamination. Upon completion of final cleaning, the entire relay assembly shall be inspected. Any particulate contamination visible at 20X magnification shall require resubmission of the lot for another cleaning and final inspection for contamination. During this inspection, the relay shall be rotated into various orientations to utilize all available lighting. Also, this step shall be performed in a controlled clean room environment with a laminar flow hood, or similar setup to eliminate any potential re-introduction of particulate contamination.

4.1.3 Inspection Requirements

4.1.3.1 Moving Contact Assembly and Springs. Inspection of the moving contact assembly for proper installation and position shall be done at 20X. The springs shall clear all adjacent parts for both positions of the armature. Support brackets for the moving contact assembly shall be inspected for cracks and loose fractures at 20X, except relays larger than 1 ampere shall be done at 10X.

4.1.3.2 Contact Surfaces (Fixed and Movable). Surfaces shall be inspected and rejected for:

a. Scratches or burrs in contact mating area and cracked or peeling plating (20X)
b. Improper alignment for both positions of the armature (20X)
c. Fibers and other contaminants (20X)
d. Tool marks on the underside of contact supports for (20X). See paragraph 4.1.3.6
e. Weld splatter on contact terminals (20X). See paragraph 4.1.3.6

4.1.3.3 Coil Inspection. Inspect relay coils for the following:

a. Coil lead welds of inadequate quality. Inspect for evidence of weld on each coil lead wire, followed by probing weld area to verify that each coil lead wire is attached to the terminal (20X). The weld area probing procedure shall be defined in a manner to minimize the possibility of mechanical damage.
b. Coil lead wires that have been repaired or spliced shall be rejected.
c. Weld splatter at coil terminals shall be rejected (20X). See paragraph 4.1.3.6
d. Proper lead coil dress; ensure clearance to all moving and conductive surfaces (Coil leads shall not be kinked and shall not be stretched tight from coil to coil lead post (10X)).
e. Nicks in the coil wire shall be rejected (20X)
f. Coil assembly for loose or frayed insulation that may interfere with normal relay operation shall be rejected (10X)

4.1.3.4 Armature and Pole Piece. Inspect armature and pole piece gap for weld splatter and contamination. The presence of either or both shall be rejected (20X).

4.1.3.5 Header. The following conditions shall be rejected during header inspection (20X):

a. Tool marks that affect reliability, See paragraph 4.1.3.6
b. Glass seal defects, See paragraph 4.1.3.6
c. Weld splatter, See paragraph 4.1.3.6
d. Cracked or peeling plating
e. Misalignment of header and frame

4.1.3.6 Inspection Criteria

4.1.3.6.1 Weld Splatter. Weld splatter or weld expulsion balls observed under 20X magnification shall be acceptable if capable of withstanding a probing force of 125 ± 5 grams applied using an approved force gage calibrated for a range of 110 to 135 grams pressure force. User may apply a maximum force of 125 ± 5 grams during pre-cap. Each suspect weld may be probed one time only by the user during pre-cap.

4.1.3.6.2 Scratches and Burrs. Scratches or tool marks wholly below the surface of the metal are acceptable. Burrs protruding above the surface are not acceptable.

4.1.3.6.3 Cracks. Cracks in the header pin glass seals shall not be acceptable, if the crack length from the pin or outer edge is more than one-third the radius of the seal. This criterion is not applicable to glass seals less than 0.10 inch diameter. In case of dispute, all relays shall meet the insulation resistance, dielectric withstanding voltage and seal test requirements.

4.1.3.6.4 Teflon. Teflon strands that are an integral part and extension of the Teflon coil wrap or coil lead insulation are acceptable, but Teflon strands of sufficient length or in a location where they can interfere with the normal actuation and operation of the relay shall be rejected.

4.1.4 Cleaning. Cleaning shall be performed in a controlled clean room environment with laminar flow hood, or similar measures to eliminate particulate contamination. Relays with permanent magnets shall be demagnetized, if they can be remagnetized and stabilized after canning.

4.1.4.1 Ultrasonic Cleaning. Relay trays and covers shall be ultrasonically cleaned. Clean a sufficient quantity of trays and covers for storage and transport of relays, cans, and other parts for the remainder of the required cleaning steps. Store in a controlled clean room environment with laminar flow hood, or similar measures to eliminate particulate contamination. Relays, cans, and any other parts and subassemblies that constitute the final assembly shall be ultrasonically cleaned. Immediately after cleaning, store the parts in covered trays in a controlled clean room environment with laminar flow hood, or similar measures to eliminate particulate contamination. Ultrasonic cleaning shall not be performed on sealed relays.

4.1.4.2 Vacuum Cleaning. Vacuum clean parts in a laminar flow hood, or equivalent, that can preclude particulate contamination. Using a pressure gun and filtered air flowing through a static eliminator, blow filtered air on the parts, holding the parts in front of a vacuum inlet to trap loosened particles. Immediately store cleaned parts in clean covered trays.

4.1.4.3 Cleaning and Small Particle Pre-seal Inspection. Test relays, cans, and any other parts or subassemblies that constitute the final assembly using the following procedure. First obtain reagent grade solvent both compatible with the relay components and meeting other necessary requirements from pre-filtered supply. Assemble pre-cleaned 1000-milliliter flask, vacuum pump, filter holder, pre-cleaned 0.80 micrometer filter, and pre-cleaned funnel. Fill funnel with pre-filtered reagent grade solvent and turn vacuum pump on. Repeat until flask is filled. Fill a pressurized container with cleaned reagent grade solvent. Clean filter by blowing both surfaces with ionized air. Using the pressurized container, wash both sides of the filter with clean filtered reagent grade solvent. Observe filter under 30X magnification; if any particles are observed, repeat the cleaning process until no particles are observed. Place the filter holder and cleaned filter on a clean empty 1000-milliliter flask under funnel. Air blow all parts to be Millipore cleaned using ionized air. Place parts in funnel. Using 1000-milliliter flask of filtered reagent grade solvent, pour the reagent grade solvent into the funnel, covering the parts to be cleaned. Cover funnel. Turn on vacuum pump. When all the reagent grade solvent has passed through the filter, turn off vacuum pumps. Remove filter and examine under 30X magnification. If one or more particles 25.4 microns (0.001 inch) or larger are present, or three or more visible particles under 25.4 microns (0.001 inch) are present on the filter, repeat the process until no additional particles are observed. Place cleaned parts in cleaned covered trays in preparation for canning the relays.

4.2 Screening (100 percent). Screening (100 percent) of MIL-PRF-39016 type relays shall be in accordance with the “M” level of the Group A inspections in MIL-PRF-39016, with the addition and exceptions in Table 1000-2. Screening (100 percent) of MIL-PRF-6106 type relays shall be in accordance with the ER requirements of the Group A inspections in MIL-PRF-6106 with the additions and exceptions in Table 1000-2. Screening (100 percent) of other type relays shall be in accordance with Table 1000-2.

4.2.1 Vibration Miss Test. For those relays in which the noise signature is characterized by mechanical chatter, the Particle Impact Noise Detection (PIND) test may not detect particles. In this case, a Vibration Miss Test shall be used in place of the PIND test. The Vibration Miss Test shall be performed in accordance with the following requirements:

a. Relays shall be vibrated with a 10 g peak sine wave at a fixed frequency of 10 Hz for 3 ± 0.1 minutes.

b. Axis of vibration shall be parallel to contact motion.

c. Relay shall be operated at 9.9 Hz

d. All contacts shall be monitored for any misses.

e. Relays with misses shall be rejected and removed from the production lot

4.2.2 Electrical Characteristics. The following electrical characteristics shall be determined in accordance with the requirements in MIL-PRF-39016, or MIL-PRF-83536, as applicable:

a. Contact Resistance
b. Operate Voltage/Set Voltage
c. Release Voltage, Reset
d. Hold Voltage for non-latching relays only
e. Operate/Set and Release/Reset Times
f. Contact Bounce (MIL-PRF-6106) or contact stabilization time (MIL-PRF-39016 and MIL-PRF-83536)
g. Coil Resistance
h. Transient Suppression
i. Reverse Polarity Protection
j. Latch from neutral for magnetic latching only

4.3 Lot Conformance Tests. Lot conformance tests shall be in accordance with the Group B tests in MIL-PRF39016, or MIL-PRF-83536, as applicable, with the following additions:

a. Random vibration and shock shall conform to the requirements of the specific application.
b. Resistance to solder heat shall be per the applicable specification.
c. Internal moisture shall be determined per the applicable specification.

4.4 Qualification Tests. Qualification tests shall be in accordance with MIL-PRF-39016 and MIL-PRF-83536, as applicable.

4.5 Incoming Inspection DPA. Incoming inspection DPA shall be in accordance with MIL-STD-1580, except paragraph 17.1.1.6f(4) shall be 15 lbs minimum for relays in TO-5 cans. All metal surfaces shall be verified for the absence of prohibited materials (e.g., pure tin, zinc, or cadmium).

5. REGISTERED (RELIABILITY SUSPECT) PMP shall include:

a. Parts with adjunct seals
b. Soldered-sealed cases
c. Units not subjected to PIND or a vibration miss test
d. External dielectric coatings
e. Plug-in devices
f. Internal suppression diode not conforming to the screening requirements of JANS MIL-PRF-19500 and this specification
g. Coil wires finer than #44 AWG not continuously monitored during thermal shock

6. PROHIBITED PMP shall include:

a. Relays with prohibited materials in their construction or finishes (see Section 4, General Requirements, paragraph 4.3.3 of this document).

Table 1000-2. 100 Percent Screening Requirements

MIL-PRF-39016	Modifications to the Requirements, Methods and Criteria of MIL-PRF39016, or MIL-PRF-83536, as applicable
Vibration (Sine)	Relays shall be vibrated in the axis parallel to contact motion
Vibration (Random)	a. MIL-STD-202, Method 214, Test Condition IG (or the requirements of the application) b. 3 orthogonal planes, 3 minutes c. Mounting fixture shall not add or remove energy from relay under test d. Monitored for contact chatter, 10 microseconds maximum (or as specified by the application) per MIL-STD-202, Method 310, Circuit B, or equivalent e. No contact transfer (monitor equipment shall be capable of detecting closures greater than 1 microsecond) f. Energize nonlatch relays during half test time and de-energize during other half g. Latching relays shall be latched in one position for half the test and latched in the other position for the other half (coils de-energized)
Thermal Shock	a. Per MIL-PRF-6106, MIL-PRF39016, or MIL-PRF-83536, operational reliability requirements b. Five thermal shocks c. Record pickup and dropout voltage d. For relays with coil gauge wire of AWG 44 or smaller, continually monitor coil continuity with 350 microamperes (maximum current) during last temperature cycle e. Miss Test during fifth cycle of thermal shock
Intermittency & Particle Impact Noise Detection (PIND)	a. See requirement in paragraph 4.2.1 of this document for the Vibration Miss Test b. MIL-STD-202, Method 217 Detection c. The lot shall be tested a maximum of 5 times. If less than 1 percent of the lot fails during any of the 5 runs, the lot may be accepted. All defective devices shall be removed after each run. Lots that do not meet the 1 percent PDA on the fifth run, or exceed 25 percent defectives cumulative, shall be rejected.
Electrical Characteristics	See requirements in paragraph 4.2.2 of this document
Insulation Resistance	
Dielectric Withstanding Voltage	a. Sea Level Only
Radiographic Inspection	a. Per MSFC-STD-355, 2 conventional x-ray views 90 degrees apart, or 360-degree view with real-time x-ray (preferred).
Seal	a. Per MIL-PRF-6106 or MIL-PRF-39016, or MIL-PRF-83536 (as applicable)
Visual and Mechanical Examination (External)	a. Per MIL-PRF-6106 or MIL-PRF-39016, or MIL-PRF-83536 (as applicable) and this section

SECTION 1100

RESISTORS

1. SCOPE. This section sets forth detailed requirements for resistors and thermistors. Table 1100-1 lists the types covered and indicates the applicable section in this document where detailed requirements are set forth. All resistors selected for the system application shall meet the requirements specified herein, unless otherwise approved by the program. Alternate approaches to meeting particular requirements shall be proven equivalent or more stringent than specified herein.

Table 1100-1. Resistor Types

Section Number	Resistor Type	Specification	Style
1110	Fixed Carbon Composition	MIL-R-39008	RCR
1120	Fixed Film	MIL-PRF-39017	RLR
1125	Fixed Film Resistor Chips	MIL-PRF-55342 or MIL-PRF-32159 [See other T-level DSCC Dwg #s listed in the SQB in TOR-2006(8583)-5235.]	RM or RCZ
1130	Fixed Film	MIL-PRF-55182	RNC/RNR
1140	Variable, Non-wirewound (Adjustment Type)	MIL-PRF-39035	RJR
1150	Variable Wirewound (Lead Screw-actuated)	MIL-PRF-39015	RTR
1160	Fixed, Wirewound (Accurate)	MIL-PRF-39005	RBR
1170	Fixed, Wirewound (Power Type)	MIL-PRF-39007	RWR
1180	Fixed, Wirewound (Power Type, Chassis-mounted)	MIL-PRF-39009	RER
1190	Resistor Network	MIL-PRF-83401	RZ
1195	Thermistor	MIL-PRF-23648	RTH

2. APPLICATION. Use of resistors shall be in accordance with the requirements contained in this document. Further guidance on resistor applications may be found in MIL-HDBK-199.

2.1 Derating. Power derating requirements are based on conditions of temperature and stress that are used for testing to establish failure rate levels. Improved part failure rates result when reduced part stress ratios or reduced temperatures are used. Derating requirements given are based on operation in vacuum. The use of derating curves found in each section is described in paragraph 4.3.1 of Section 4, General Requirements, of this document.

2.2 End-of Life Design Limits. End-of-life design limits do not include item tolerances and shall therefore be additive to values specified in each applicable section.

2.3 Electrical Considerations

2.3.1 Power Ratings. Selection of resistor types and power ratings shall be based on the intended application and allowable failure rate.

2.3.2 Pulse Applications. In applications where pulse voltages are present, the maximum pulse amplitude (including any steady-state voltage) shall not exceed the value established by derating, regardless of resistance value. For repetitive pulses, the average power shall not exceed the established derated value. Average power is defined by

$P (avg) = P (t/T)$

Where:

P = pulse power, calculated from the equation ($P = E^2/R$)

t = pulse width, and

T = cycle width

For nonrepetitive pulses, the thermal time constant of the resistor in the particular application shall be determined and the pulse power limited to a value that does not result in a temperature rise at the resistor surface which is greater than the temperature rise that would result from the applied derated DC power level. When actual test pulse power data exist, the data shall be listed in the appropriate resistor section.

CAUTION: Certain resistor technologies (e.g., metallized thin-film) are not designed or tested for pulsed applications, while others have limited capabilities to withstand pulses. Care shall be taken to ensure that resistors are not used under conditions that will shorten their life spans, or cause them to fail prematurely. As a minimum, resistors shall be characterized and qualified before using in pulsed applications, even inside hybrids.

3. DESIGN AND CONSTRUCTION. See the detailed requirements section for each resistor type.

4. QUALITY ASSURANCE. See the detailed requirements section for each resistor type.

4.1 Production Lot. Per the applicable military specification as referenced in the detailed section of this document, or as specified in Section 4, General Requirements, of this document.

4.2 Solder Dip/Retinning. See Section 4, General Requirements, paragraph 4.3.4.1 of this document.

5. REGISTERED (RELIABILITY SUSPECT) PMP. The following resistor types have failure modes that cannot be completely removed by existing controls and screens. These types are not recommended for mission-significant or critical space applications. Reliability suspect resistors shall include the following (see individual sections for complete list):

a. All variable types
b. Films over solid cores without initial undercoating
c. Chip devices with silver or silver/palladium terminations that have no barrier metallization, and are intended for solder-mounting applications
d. Film chips with films <350 Angstroms thick
e. Non-hermetic film resistors with aluminum terminations without protective undercoating
f. Wirewound resistors with crimped or soldered terminations
g. Wirewound resistors with wire size < 0.001 inch.

h. Resistors using tantalum nitride films < 350 Angstroms thick

i. Non-welded networks

6. PROHIBITED PMP shall include:

a. All carbon film

b. Unpassivated nichrome film

c. Non-hermetic hollow core (ceramic) film types

d. All hermetic hollow ceramic core film resistors with internal metallization

e. Resistors with tin coated leads or terminations (see Section 4, General Requirements, paragraph 4.3.3 of this document).

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SECTION 1110

FIXED COMPOSITION, INSULATED, CARBON COMPOSITION (RCR)

(MIL-R-39008)

1. SCOPE. This section sets forth detailed requirements for RCR style fixed composition resistors (commonly identified as carbon composition resistors). NOTE: There is no longer a qualified supplier of carbon composition resistors. This section is maintained only to cover existing resistor inventory and/or heritage hardware/design.

2. APPLICATION. Carbon composition resistors are obsolete for new designs.

2.1 Derating

2.1.1 Power Derating. Power derating shall be in accordance with Figure 1110-1.

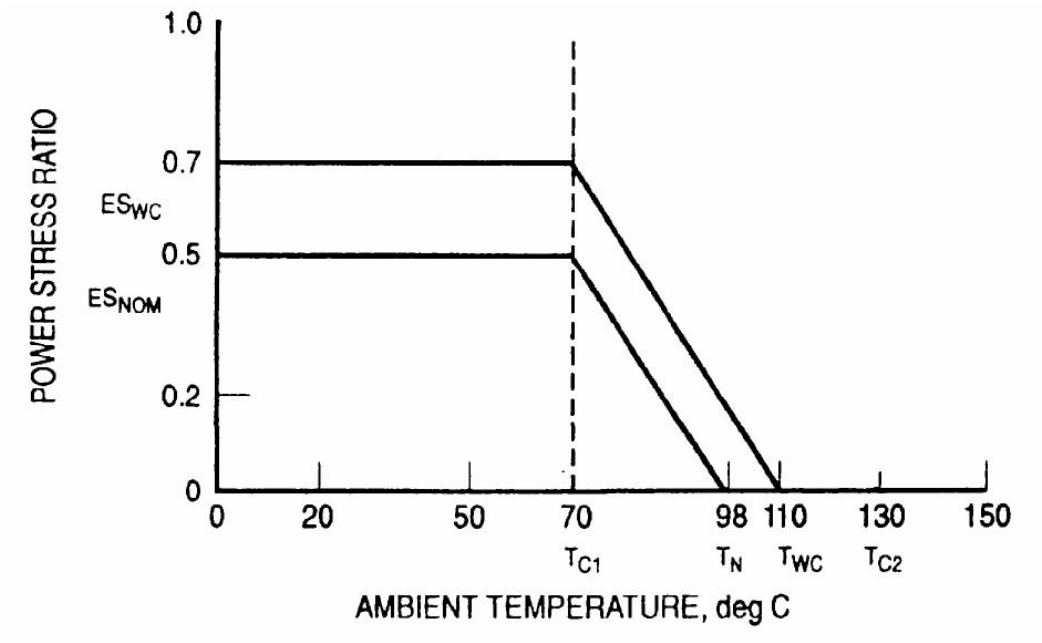

Figure 1110-1. Power derating for carbon composition resistors.

2.1.2 Voltage Derating. Voltage applied to RCR resistors shall be limited to 0.8 times values shown in Figure 301-2 of MIL-STD-199E (CANCELED).

2.2 End-of-Life Design Limits (Resistance) shall be:

a. ±15 percent for approved application

b. ± 20 percent for worst-case application

2.3 Aging Sensitivity. Carbon composition resistors typically exhibit resistance and noise changes of ± 15 percent due to moisture and temperature effects. When a closer tolerance or higher accuracy is needed, metal film or precision wirewound devices shall be used. The increase in resistance due to moisture absorption as well as the corresponding decrease in resistance after space deployment shall be evaluated for their effect on circuit performance.

3. DESIGN AND CONSTRUCTION

3.1 Requirements. Design and construction shall be in accordance with the requirements of MIL-R-39008.

Section 1110 FIXED COMPOSITION, INSULATED, CARBON COMPOSITION (RCR)

4. QUALITY ASSURANCE. Quality Assurance provisions shall be in accordance with the requirements of MIL-R-39008 unless specified otherwise.

4.1 Incoming Inspection. All resistors shall be verified for the absence of prohibited materials (e.g., pure tin, zinc, or cadmium).

5. REGISTERED (RELIABILITY SUSPECT) PMP shall include:

a. Carbon composition (RCR type) resistors shall be limited to applications where resistance accuracies (excluding initial resistor tolerance) in excess of ±20 percent are acceptable.

6. PROHIBITED PMP shall include:

a. Carbon film types (pyrolitic carbon film deposited on glass or ceramic core).

b. Resistors with prohibited materials in their construction or finishes (see Section 4, General Requirements, paragraph 4.3.3 of this document).

SECTION 1120

FIXED FILM RESISTORS (RLR)

(MIL-PRF-39017)

1. SCOPE. This section sets forth detailed requirements for fixed thin/thick film resistors, RLR style. “S” failure rate, and select “R” failure rate, RLR resistors do not have to be subjected to the requirements of paragraphs 4.1, 4.2, 4.3 and 4.4 of this section. The select “R” failure rate RLRs include the following:

a. RLR05 = 302 KΩ to 1.0 MΩ

b. RLR07 = 3.02 MΩ to 10.0 MΩ

c. RLR32

All other resistors of similar style/type shall meet all the requirements of this section.

2. APPLICATION

2.1 Derating

2.1.1 Power Derating. Steady state power shall be derated in accordance with Figure 1120-1.

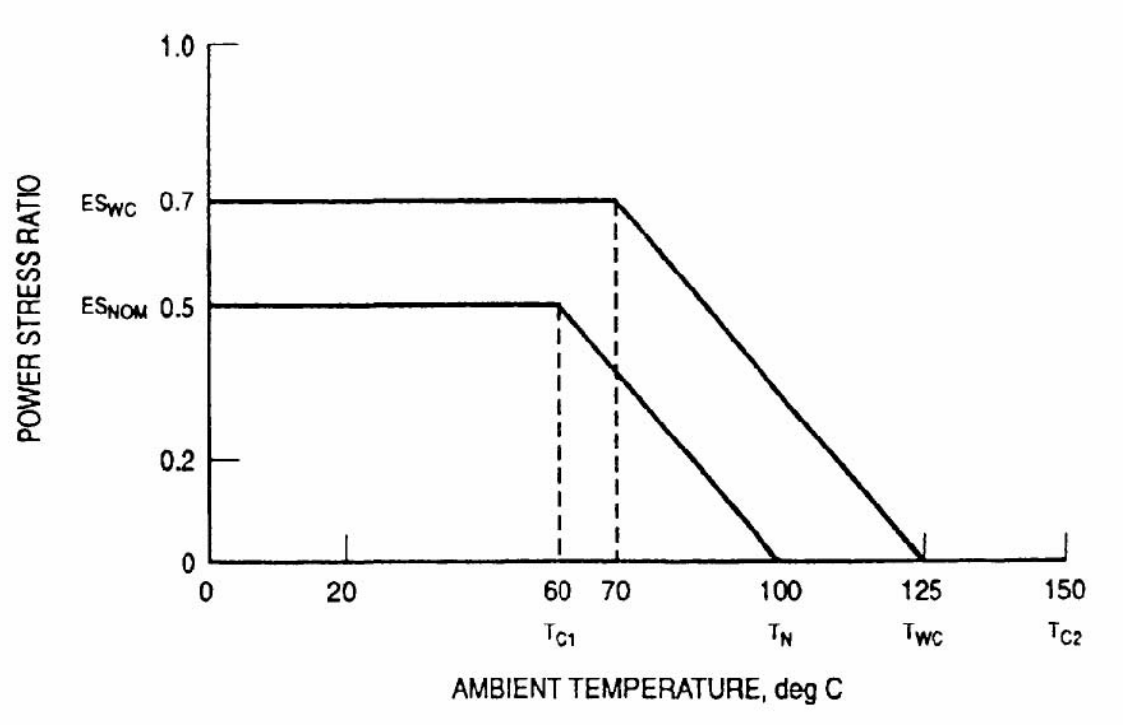

Figure 1120-1. Power derating for film resistors.

2.1.2 Voltage Derating. Voltage applied to these resistors shall be limited to 0.80 of the maximum continuous working voltages as shown in Table 1120-1.

Table 1120-1. Maximum Continuous DC Working Voltages

Part Type	RLR05	RLR07	RLR20	RLR32
Maximum Continuous DC Working Voltage	200V	250V	350V	500V

2.2 End-of-life Design Limits (Resistance) shall be:

a. ±2 percent for approved application

b. ±3 percent for worst-case application

2.3 Electrical considerations

2.3.1 Peak Power. The peak power shall be limited as follows:

Type	Peak Power (Watt-seconds)
RLR 05	1
RLR 07	3
RLR 20	15
RLR 32	40

2.3.2 Electrostatic Discharge Sensitivity. Under low humidity conditions fixed film resistors, particularly those of smaller case sizes manufactured with high sheet resistance films, are subject to electrostatic discharge (ESD) damage and sudden shifts in resistance and the temperature coefficient of resistance. Precautions against ESD shall be used in packaging, handling, storage and kitting.

2.3.3 Humidity/Power Conditions. Most RLR style resistors use nichrome film element, which is susceptible to corrosion/dissolution when operated under humid conditions, causing large increases in resistance values, or open circuit failures. Care shall be taken during handling, storage, board assembly or testing so as not to compromise the integrity of conformal coating, molded or hermetic case.

2.4 Outgassing. The resistor encapsulation shall meet the outgassing requirements specified in Section 4, General Requirements, paragraph 4.1.9 of this document.

3. DESIGN AND CONSTRUCTION. Design and construction shall be in accordance with MIL-PRF-39017, failure rate level “S”.

4. QUALITY ASSURANCE. Quality assurance provisions shall be in accordance with Section 4, General Requirements, of this document and the following:

4.1 In-process Controls. In-process controls shall be in accordance with the requirements of MIL-PRF-39017.

4.2 Group A Requirements. Group A requirements shall be in accordance with the requirements of MIL-PRF39017 and Table 1120-2.

4.3 Group B Tests. Group B tests shall be in accordance with the requirements of MIL-PRF-39017.

4.4 Qualification Tests. Qualification testing shall be in accordance with the requirements of MIL-PRF-39017.

4.5 Incoming Inspection DPA. Incoming inspection DPA shall be in accordance with MIL-STD-1580, and performed on resistors not covered in the "Scope" paragraph of this section, or non-MIL/non-QPL film resistors. However, all film resistors (MIL and non-MIL/ non-QPL) shall be verified for the absence of prohibited materials (e.g., pure tin, zinc, or cadmium).

5. REGISTERED (RELIABILITY SUSPECT) PMP shall include:

a. Resistors not protected from electrostatic discharge during shipping and handling may experience permanent damage.

b. Resistors using aluminum terminations are susceptible to corrosion due to moisture penetration. These parts shall not be used, or procured, unless with protective undercoating.

6. PROHIBITED PMP shall include:

a. Devices constructed with a deposited thin metal film (<350 angstroms) over a solid core that do not have a protective undercoating between the metal film and the outer jacket shall not be used

b. Non-hermetic hollow core (ceramic) film types

c. All hermetic hollow ceramic core film resistors with internal metallization

d. Resistors with pure tin coated leads or terminations (see Section 4, General Requirements, paragraph 4.3.3 of this document).

Table 1120-2. Group A Tests for RLR Style Fixed Film Resistors

MIL-PRF-39017	Modifications to the Methods, Requirements and Criteria for Group A in MIL-PRF-39017
Subgroup 1 (l00 percent)	
DC Resistance	Read and record
Thermal Shock	5 cycles, -55ºC to +125ºC
Overload	24 hours minimum at 25 ± 5ºC with 1.5X rated power
Power Conditioning	96 hours minimum at maximum rated temperature and full rated power; do not exceed maximum voltage specified in the spec
DC Resistance (after Power Conditioning)	Change in DC resistance shall not exceed 0.5 percent +0.05 ohm or ±3 standard deviation, whichever is less, for the combined overload and power conditioning tests DC resistance shall be within initially specified tolerance limits; lots having more than 10 percent out-of-tolerance rejects shall not be used
Subgroup 2 Solderability	
Subgroup 3 Visual and Mechanical Examination	

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SECTION 1125

FIXED FILM RESISTOR CHIPS (RM)

(MIL-PRF-55342, “V” AND “U” FAILURE RATES AND T-LEVEL, AND MIL-PRF-32159, T-LEVEL)

1. SCOPE. This section sets forth detailed requirements for fixed thin/thick film chip resistors, RM style per MIL-PRF-55342, and zero ohm chip resistors, RCZ style per MIL-PRF-32159. T-level RM and RCZ style chip resistors are space quality baseline (SQB) parts. In addition, chip resistors procured as T-level to DSCC drawings 04007B, 04008B, 04009B, 94012F, 94013F, 94015H, 94016G, 94017F, 94018F, 94019F and 94025G are also SQB parts. "V" failure rate, or "U" failure rate if the "V" version of the same part is not listed as a certified QPL part, RM chip resistors are acceptable as-is with no additional requirements per paragraphs 4.1, 4.2, 4.3 and 4.4 of this section except DPA which shall be performed on every lot in accordance with paragraph 4.5. However, for pulsed applications, only T-level MIL-PRF-55342 resistors shall be used (see paragraph 2.1.2 below). All other chip resistors of similar type / style shall meet all the requirements of this section.

Note: "V" = "S" failure rate + lot-specific Group B

"U" = "R" failure rate + lot-specific Group B

2. APPLICATION

2.1 Derating

2.1.1 Power Derating. Power applied to these resistors shall be derated with temperatures in accordance with the following:

	< 70ºC	70ºC to 125ºC
Nominal	50 percent of rated power	linearly derate to zero power
Worst Case	75 percent of rated power	linearly derate to zero power

2.1.2 Pulsed Applications. For pulsed applications (transient events with duty cycles of less than ten (10) percent and maximum duration of < 1 second), T-Level MIL-PRF-55342 resistors may be operated to a maximum of 3.125 times their rated power..

2.1.3 Voltage Derating. Voltage applied to these resistors shall be limited to 0.80 of the maximum voltage values shown in MIL-PRF-55342 and MIL-PRF-32159.

2.2 End-of-life Design Limits (Resistance) shall be:

a. ±2 percent for nominal application

b. ±5 percent for worst-case application

2.3 Electrical Considerations. These resistors are suitable for high frequency operations. Above 200 MHz, however, effective resistance is reduced as a result of shunt capacity between resistance elements and controlling circuits. Manufacturer’s impedance characteristics curves may be used to determine maximum usable frequency for each device style.

2.3.1 Humidity/Power Conditions. Chip resistors using nichrome films are susceptible to large increases in resistance values, or open failures, when operated under humid conditions. For such environments, use tantalum nitride thin films with low ohms/square sheet resistance, or use ruthenium oxide thick films. Additionally, performing the laser trimming prior to passivation minimizes exposure of the metal film to moisture.

2.3.2 Mounting. Certain termination materials for these chips (e.g., palladium or gold) are subject to leaching when exposed to molten solder.

2.3.3 Electrostatic Discharge Sensitivity. Under low humidity conditions fixed film chip resistors, particularly those of smaller case sizes manufactured with high sheet resistance films, are subject to electrostatic discharge (ESD) damage and sudden shifts in resistance and the temperature coefficient of resistance. Precautions against ESD shall be used in packaging, handling, storage and kitting.

Section 1125 RM

3. DESIGN AND CONSTRUCTION

3.1 Requirements. Design and construction shall be in accordance with the T-level requirements of MIL-PRF-55342 and MIL-PRF-32159 and the requirements of this document.

4. QUALITY ASSURANCE. Quality assurance provisions shall be in accordance with Section 4, General Requirements, of this document and the following:

4.1 In-process Controls. In-process controls shall be in accordance with the T-level requirements of MIL-PRF-55342 or MIL-PRF-32159.

4.2 Group A Requirements. Group A requirements shall be in accordance with the T-level requirements of MIL-PRF-55342 or MIL-PRF-32159.

4.3 Group B Tests. Group B tests shall be in accordance with the T-level requirements of MIL-PRF-55342 or MIL-PRF-32159.

4.4 Qualification Tests. Qualification testing shall be in accordance with the T-level requirements of MIL-PRF-55342 or MIL-PRF-32159.

4.5 Incoming Inspection DPA. Incoming inspection DPA shall be in accordance with MIL-STD-1580, and limited to the thin-film construction (typically, the E and H characteristics). Note that certain suppliers manufacture all characteristics using thin metal films, which means that resistor technology will have to be pre-determined in order to know which parts to DPA. However, both thin and thick film chip resistors shall have all metal surfaces verified for the absence of prohibited materials (e.g., pure tin, zinc, or cadmium).

5. REGISTERED (RELIABILITY SUSPECT) PMP shall include:

a. Silver Terminations
   Chip resistors with silver or silver and palladium terminations have, in general, greatly reduced resistance to solder leaching and shall not be utilized unless leach resistant barriers such as nickel or copper are utilized between the termination and the solder.

b. Thin Film Resistors
   Designs requiring film thickness of 350 angstroms or less are reliability suspect due to increased susceptibility of these parts to a) mechanical handling damage b) opens resulting from “hot spots” at surface defects, and c) other anomalies.

c. Large Aspect Ratio
   Aspect ratio (Length-to-Width) for chip resistors shall not be >2:1.

6. PROHIBITED PMP shall include:

a. Fixed film resistor chips with copper or nickel conductor films.

b. Unpassivated nichrome film

c. Resistors with prohibited materials in their construction (see Section 4, General Requirements, paragraph 4.3.3 of this document).

SECTION 1130

FIXED METAL FILM RESISTORS (RNC/RNR)

(MIL-PRF-55182)

1. SCOPE. This section sets forth detailed requirements for fixed metal film resistors (style RNC/RNR). “S” failure rate, and select “R” failure rate, RNC/RNR resistors do not have to be subjected to the requirements of paragraphs 4.1, 4.2, 4.3 and 4.4 of this section. The select “R” failure rate resistors include RNC/RNR 65 and 70, and RNC90s. All other resistors of similar type / style shall meet all the requirements of this section.

2. APPLICATION

2.1 Derating

2.1.1 Power Derating. Power derating shall be in accordance with Figure 1130-1. At temperatures above +70ºC parts shall be linearly derated to zero power at +120ºC in accordance with Figure 1130-1.

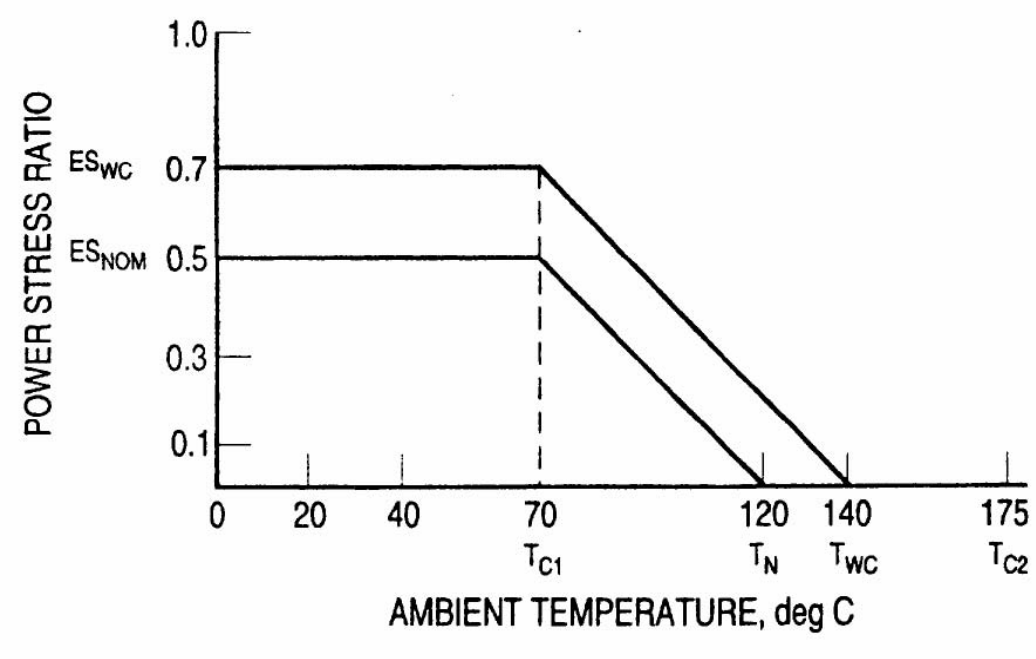

Figure 1130-1. Power derating for metal film resistors.

2.1.2 Voltage Derating. Voltage applied to RNC/RNR resistors shall be limited to 0.80 of the maximum allowable voltage ratings in MIL-PRF-55182.

2.2 End-of-life Design Limits. (Resistance) shall be:

a. ±1.0 percent for approved application

b. ±1.5 percent for worst-case application

2.3 Electrical Considerations

2.3.1 Temperature Coefficient. MIL-PRF-55182 specifies resistance changes of ±5 or ±25 ppm/ºC (relative to 25ºC resistance reading) over the operating temperature range. It should be noted that the TC is established relative to resistor temperature and not the environment.

2.3.2 Electrostatic Discharge. These devices are susceptible to ESD damage; thus precautions for handling of ESD-sensitive parts shall be followed.

2.3.3 Humidity/Power Conditions. Most RNC/RNR style resistors use nichrome film element, which is susceptible to corrosion/dissolution when operated under humid conditions, causing large increases in resistance values, or open circuit failures. Care shall be taken during handling, storage, board assembly or testing so as not to compromise the integrity of conformal coating, molded case or hermetic case.

3. DESIGN AND CONSTRUCTION

3.1 Requirements. Design and construction shall be in accordance with the requirements of MIL-PRF-55182 for T-level and the requirements of this document.

4. QUALITY ASSURANCE. Quality assurance provisions shall be in accordance with Section 4, General Requirements, of this document and the following:

4.1 In-process Controls. In-process controls shall be in accordance with the requirements of MIL-PRF-55182 for T-level.

4.2 Group A Requirements. Group A requirements shall be in accordance with the requirements of MIL-PRF-55182 for T-level, except Resistance Noise is not required.

4.3 Group B Tests. Group B tests shall be in accordance with the requirements of MIL-PRF-55182 for T-level.

4.4 Qualification Tests. Qualification tests shall be in accordance with the requirements of MIL-PRF-55182 for T-level.

4.5 Incoming Inspection DPA. Incoming inspection DPA shall be in accordance with MIL-STD-1580 and performed on parts not covered in the “Scope” paragraph of this section, or non-MIL/non-QPL RNC/RNR-like metal film resistors. All foil resistors, e.g., RNC90 style, require the special DPA processing and evaluation specified in MIL-STD-1580. Regardless of style, all film and foil resistors shall be verified for the absence of prohibited materials (e.g., pure tin, zinc, or cadmium).

5. REGISTERED (RELIABILITY SUSPECT) PMP shall include:

a. Resistors not protected from electrostatic discharge during shipping and handling may experience permanent damage.

b. Resistors using aluminum terminations are susceptible to corrosion due to moisture penetration. These parts shall not be used, or procured, unless with protective undercoating.

c. Non-hermetic resistors using thin film metallization without a corrosion-resistant precoat over the metal film.

6. PROHIBITED PMP shall include:

a. Non-hermetic hollow-core types.

b. Hermetic hollow-core types with internal (inside surface of the core) metallization (susceptible to film corrosion due to contamination from the manufacturing process).

c. Resistors using prohibited materials in their construction (see Section 4, General Requirements, paragraph 4.3.3 of this document).

SECTION 1140

VARIABLE, NON-WIREWOUND RESISTORS (RJR)

(MIL-PRF-39035)

1. SCOPE. This section sets forth detailed requirements for variable, non-wirewound resistors.

2. APPLICATION. Variable resistors shall be avoided whenever possible. They are not recommended for space use. These resistors are not hermetically sealed and are susceptible to degraded performance due to ingress of soldering flux, cleaning solvents, and conformal coatings during equipment fabrication. These parts are also subject to resistance change during shock and vibration.

2.1 Derating

2.1.1 Power Derating. Power shall be derated in accordance with Figure 1140-1

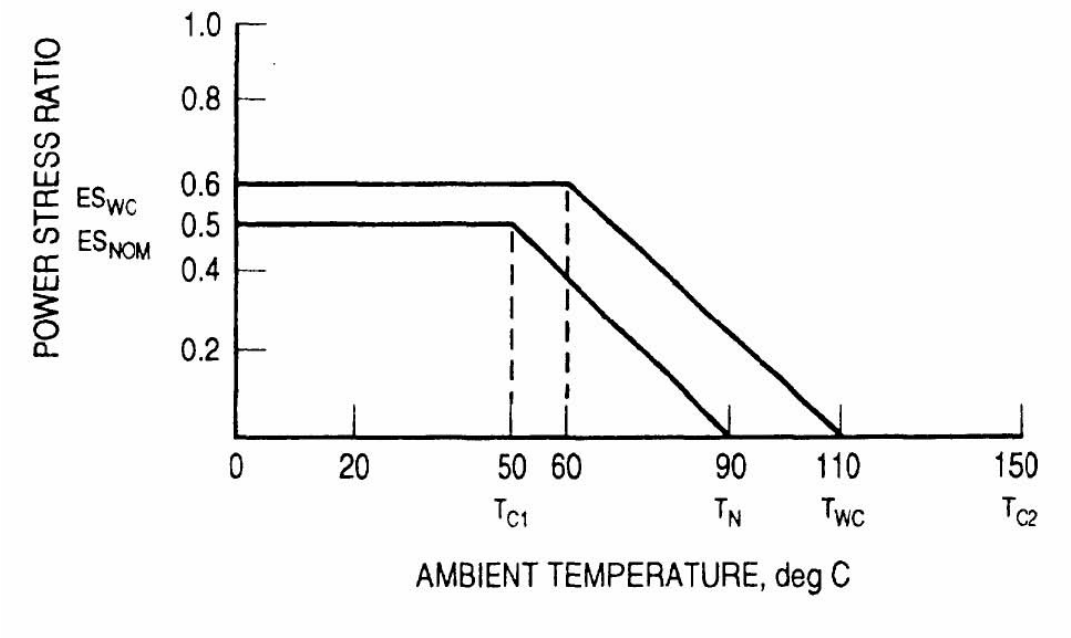

Figure 1140-1. Power derating for variable, non-wirewound resistors.

2.1.2 Voltage Derating. Voltage applied to these resistors shall be limited to 0.80 of the values shown in Paragraph 3.3 of Section 402 of MIL-STD-199E.

2.2 End-of-Life Design Limits (Resistance) shall be:

a. ±22 percent for approved applications

b. ±30 percent for worst-case application

2.3 Mounting. Mounting brackets shall be used.

3. DESIGN AND CONSTRUCTION

3.1 Requirements. Design and construction shall be in accordance with the requirements of MIL-PRF-39035 and the requirements of this document.

3.2 Recommended. None identified.

4. QUALITY ASSURANCE. Quality assurance provisions shall be in accordance with Section 4, General Requirements, of this document and the following:

4.1 In-process Controls. In-process controls shall be in accordance with the requirements of MIL-PRF-39035 and the following: An internal visual inspection is required for all parts. A binocular microscope with minimum 30X magnification and an integral light source or fiber optic light ring shall be used. Any resistor exhibiting one or more of the following defects shall be marked and rejected. The entire lot shall be rejected if the fall-out exceeds 7.0 percent of the lot.

a. Foreign material
b. Chips, spalls, cracks, or scratches in the resistor element
c. Element misalignment or improper seating
d. Incorrect or missing element stops
e. Incorrect seating or damage to wiper arm
f. Faulty termination of element or pins

4.2 Group A Requirements. Group A requirements shall be in accordance with the requirements of MIL-PRF39035 and Table 1140-1.

4.3 Group B Tests. Group B tests shall be in accordance with the requirements of MIL-PRF-39035.

4.4 Qualification Tests. Qualification testing shall be in accordance with the requirements of MIL-PRF-39035.

4.5 Incoming Inspection DPA. Incoming inspection DPA shall be in accordance with MIL-STD-1580. All metal surfaces shall be verified for the absence of prohibited materials (e.g., pure tin, zinc, or cadmium).

5. REGISTERED (RELIABILITY SUSPECT) PMP shall include:

a. All variable resistors are reliability suspect.

6. PROHIBITED PMP shall include:

a. Resistors with prohibited materials in their construction (see Section 4, General Requirements, paragraph 4.3.3 of this document).

Table 1140-1. Modifications to Group A Tests for Variable, Non-Wirewound Resistors

MIL-PRF-39035	Modifications to the Methods, Requirements and Criteria per MIL-PRF-39035
Subgroup 1 (100 percent) 1/ Thermal Shock Conditioning Contact Resistance Variation Immersion	 168 hours minimum at 85 +5ºC
Subgroup 2 Vibration, random	12 samples (6 highest, 6 lowest in resistance value), 0 failure MIL-STD-202, Method 214, Test Condition UK (or to the requirements of the application Two cycles of 10 minutes each in two orthogonal planes Post vibration measurements shall meet specification limits
Subgroup 3 Visual and Mechanical Examination	

1/ PDA is 5 percent

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SECTION 1150

VARIABLE, WIREWOUND RESISTORS (RTR)

(MIL-PRF-39015)

1. SCOPE. This section sets forth detailed requirements for variable, wirewound resistors.

2. APPLICATION. Variable resistors shall be avoided whenever possible. They are not recommended for space use. These resistors are not hermetically sealed and are susceptible to degraded performance due to ingress of soldering flux, cleaning solvents, and conformal coatings during equipment fabrication. These parts are also subject to resistance changes during shock and vibration or aging.

2.1 Derating

2.1.1 Power Derating. These resistors shall be power-derated in accordance with Figure 1150-1.

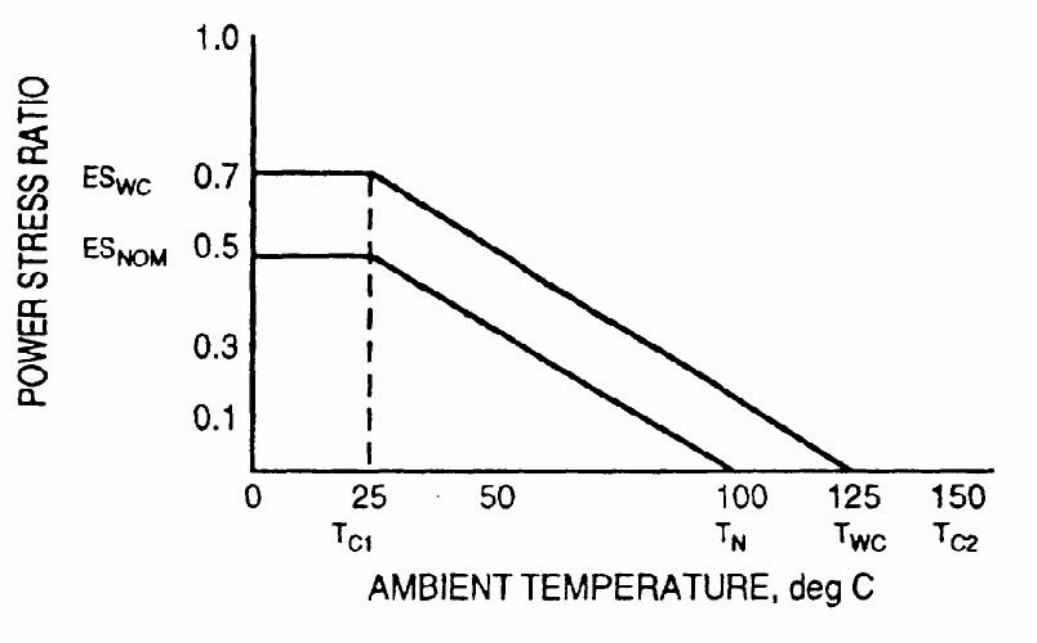

Figure 1150-1. Power derating requirements for variable, wirewound resistors.

2.1.2 Voltage Derating. Voltage applied to these resistors shall be limited to 0.80 of the values shown in Table 1150-1.

Table 1150-1. MIL-STD-199 Rated Voltages

Nominal Resistance Ohms	Maximum Rated Voltage Volts AC (rms) or DC
10	2.7
20	3.8
50	6.1
100	8.7
200	12.3
500	19.4
1000	27.4
2000	38.7
5000	61.3
10000	86.7

2.2 End-of-life Design Limits (Resistance) shall be:

a. ±10 percent for approved applications

b. ± 20 percent for worst-case application

2.2.1 Pulse Power. Same requirements as described in Paragraph 2.3.4 of Section 1170, if the wiper position is not less than 70 percent of the maximum setting.

2.3 Mounting. Mounting shall be in accordance with Section 3500. Mounting brackets may be necessary for part typical shock and vibration environments.

3. DESIGN AND CONSTRUCTION

3.1 Requirements. Design and construction shall be in accordance with the requirements of MIL-PRF-39015 and the requirements of this document.

3.1.1 Wire Diameter. A minimum wire diameter of 25.4 microns (0.001 inch) shall be used.

3.1.2 Internal Connections. All internal connections shall be welded.

4. QUALITY ASSURANCE. Quality assurance provisions shall be in accordance with Section 4, General Requirements, of this document and the following:

4.1 In-process Controls. In-process controls shall be in accordance with the requirements of MIL-PRF-39015 and the following: An internal visual inspection is required for all parts. A binocular microscope with minimum 30X magnification and a coaxial illumination or fiber optic light ring shall be used. Any resistor exhibiting one or more of the following defects shall be marked and rejected. The entire lot shall be rejected if the percentage of its rejected parts exceeds 7.0 percent.

a. Damage to resistance wire reducing its diameter by one-third or more
b. Nonwelded internal connections
c. Loose windings on active portion of resistor
d. Loose wire ends or wraps capable of touching other conductive parts or each other
e. Any lubricant on resistance element
f. Resistance element not secure to resistor body
g. Body and wiper stops cracked, damaged, or distorted
h. Loose welds
i. Burning at weld greater than one-half of tab width
j. Cracks or fractures in welds
k. Loose terminals
l. Foreign material such as weld splatter, fluxes residue, or metallic particles.

4.2 Group A Requirements. Group A requirements shall be in accordance with the requirements in MIL-PRF-39015 and Table 1150-2.

4.3 Group B Tests. Group B tests shall be in accordance with the Group B tests in MIL-PRF-39015.

4.4 Qualification Tests. Qualification testing shall be in accordance with the requirements of MIL-PRF-39015.

4.5 Incoming Inspection DPA. Incoming inspection DPA shall be in accordance with MIL-STD-1580. All metal surfaces shall be verified for the absence of prohibited materials (e.g., pure tin, zinc, or cadmium).

5. REGISTERED (RELIABILITY SUSPECT) PMP shall include:

a. All variable resistors are reliability suspect.
b. Resistors with <0.001 inch wire diameter.

6. PROHIBITED PMP shall include:

a. Resistors with prohibited materials in their construction (see Section 4, General Requirements, paragraph 4.3.3 of this document).

Table 1150-2. Group A Tests for Variable, Wirewound Resistors

MIL-PRF-39015	Modifications to the Methods, Requirements and Criteria of MIL-PRF-39015
Subgroup 1 (100 percent) 1/ Thermal Shock Conditioning Peak Noise Total Resistance Immersion	 168 hours minimum at +85ºC
Subgroup 2 Vibration, random	 12 samples (6 highest, 6 lowest in resistance value), 0 failure MIL-STD-202, Method 214, Test Condition IIK or the vibration level requirements of the application Two cycles of 10 minutes each in two orthogonal planes Measurements before, during and after test shall be in accordance with MIL-PRF-39015 Change in total resistance and setting stability shall meet specification limits
Subgroup 3 Continuity Absolute Minimum Resistance End Resistance Actual Effective Electric Travel DWV IR Torque	
Subgroup 4 Visual and Mechanical Examination Solderability	

1/ PDA is 5 percent.

SECTION 1160

WIREWOUND, ACCURATE, RESISTORS (RBR)

(MIL-PRF-39005)

1. SCOPE. This section sets forth detailed requirements for fixed wirewound (accurate) resistors. “R” failure rate RBR resistors do not have to be subjected to the requirements of paragraphs 4.1, 4.2, 4.3 and 4.4 of this section. All other resistors of similar type / style shall meet all the requirements of this section.

2. APPLICATIONS

2.1 Derating

2.1.1 Power Derating. Power shall be derated with temperature in accordance with Figure 1160-1 based on resistance tolerances as represented by Roman numerals I through IV (see Table 1160-1).

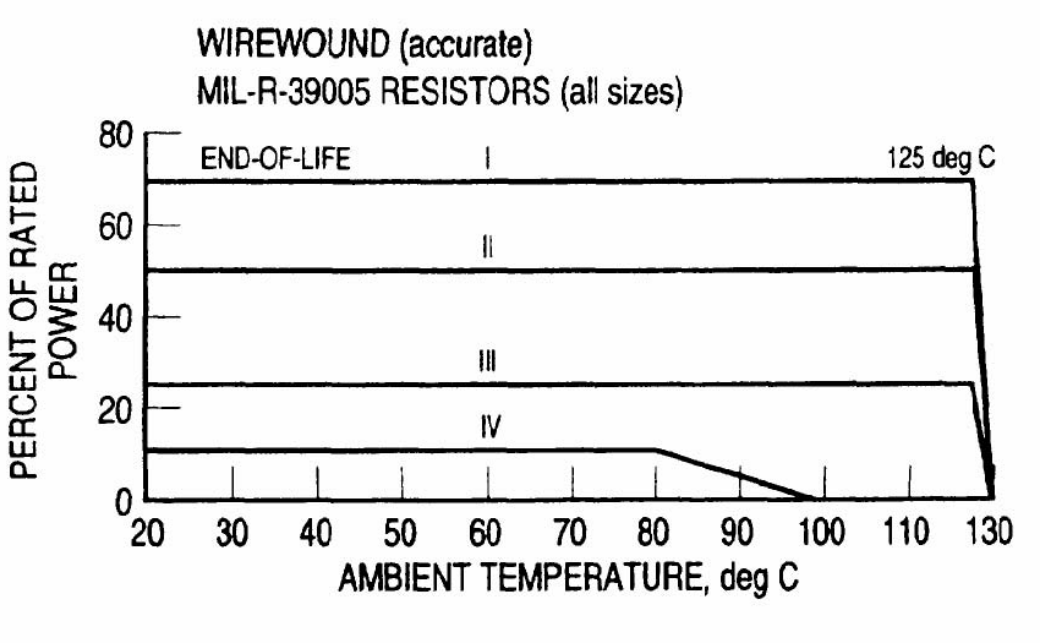

Figure 1160-1. High temperature derating curves for accurate wirewound resistors.

2.1.2 Voltage Derating. Voltages applied to these resistors shall be limited to 0.60 of the values shown as maximum voltages in Table A-II of MIL-STD-199.

2.2 Resistance Tolerances and Power Derating. Maximum steady-state wattages shall be calculated by multiplying the applicable Power Derating factor for the appropriate resistance tolerance (Figure 1160-1 and 2.1.1) by the Additional Derating Factor for Nominal Wattage (Table 1160-1) for the appropriate Tolerance Designator.
.

Table 1160-1. Resistance Tolerance and Required Derating

Tolerance Designator	Resistance Tolerance	Additional Derating Factor for Nominal Wattage
IV	0.01 percent	0.40
III	0.05 percent	0.40
II	0.10 percent	0.40
I	1.00 percent	0.80

2.3 End-of-life Design Limits (Resistance). Power derating is for all sizes in MIL-PRF-39005. The end-of-life (EOL) stabilities are based on power-derating curves of Figure 1160-1.

I. EOL = ±1.00 percent (plus initial tolerance)

II. EOL = ±0.51 percent (plus initial tolerance)

III. EOL = ±0.30 percent (plus initial tolerance)

IV. EOL = ±0.03 percent (plus initial tolerance)

2.4 Electrical Considerations

2.4.1 Moisture. These resistors are susceptible to absorption of water vapor and can exhibit a positive or negative (usually positive) shift of resistance of 30 to 70 parts per million. The shift in resistance is influenced by the relative humidity, temperature, and the time exposed. The process is completely reversible by baking at a moderate temperature. (Consult with manufacturer for temperature and duration.)

3. DESIGN AND CONSTRUCTION

3.1 Requirements. Design and construction shall be in accordance with the requirements of MIL-PRF-39005 and the requirements of this document.

3.1.1 Wire Diameter. A minimum wire diameter of 25.4 microns (0.001 inch) shall be used.

3.1.2 Internal Connections. All internal connections shall be welded.

4. QUALITY ASSURANCE. Quality assurance provisions shall be in accordance with Section 4, General Requirements, of this document and the following:

4.1 In-Process Controls. In-process controls shall be in accordance with the requirements of MIL-PRF-39005 and the following: All exposed inner surfaces of each resistor shall be examined at a minimum of 30X magnification. Any part exhibiting one or more of the following anomalies shall be rejected.

a. Absence of a soft cushion coating over wire winding
b. Burning at weld greater than one-half tab width
c. Lack of indication weld tip indention at welds
d. Cracks, breaks, or partial fracture at welds

4.2 Group A Requirements. Group A requirements shall be in accordance with MIL-PRF-39005 and Table 1160-2.

4.3 Group B Tests. Group B tests shall be in accordance with the requirements of MIL-PRF-39005.

4.4 Qualification Tests Qualification testing shall be in accordance with the requirements of MIL-PRF-39005.

4.5 Incoming Inspection DPA. Incoming inspection DPA shall be in accordance with MIL-STD-1580. All metal surfaces shall be verified for the absence of prohibited materials (e.g., pure tin, zinc, or cadmium).

5. REGISTERED (RELIABILITY SUSPECT) PMP shall include:

a. Designs using soldered or crimped internal connections are reliability suspect.

b. Designs using wire diameters less than 25.4 microns (0.001 inch) are reliability suspect.

6. PROHIBITED PMP shall include:

a. Resistors with prohibited materials in their construction (see Section 4, General Requirements, paragraph 4.3.3 of this document).

Table 1160-2. Group A Tests for Fixed, Wirewound, Accurate Resistors

MIL-PRF-39005	Modifications to the Methods, Requirements and Criteria of MIL-PRF-39005
Thermal Shock	
DC Resistance	
Conditioning	a. 168 hours minimum
Short Time Overload	
Delta DC Resistance	a. ΔR ±(0.01 percent +0.01 ohm)
Radiographic Inspection	a. Per MSFC-STD-355; 2 conventional x-ray views 90 degrees apart, or 360-degree view using real-time x-ray (preferred).
	b. Test may be waived if in-process is performed
Visual and Mechanical	a. Marking and identification
Examination (External)	b. Defects and damage; i.e., body finish, lead finish, misalignment, cracks
Solderability	

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SECTION 1170

WIREWOUND, POWER-TYPE RESISTORS (RWR)

(MIL-PRF-39007)

1. SCOPE. This section sets forth detailed requirements for wirewound (power-type) resistors. “S” failure rate RWR resistors do not have to be subjected to the requirements of paragraphs 4.1, 4.2, 4.3 and 4.4 of this section. All other resistors of similar style / type shall meet all the requirements of this section.

2. APPLICATION

2.1 Derating

2.1.1 Power Derating. Power shall be derated in accordance with Figure 1170-1.

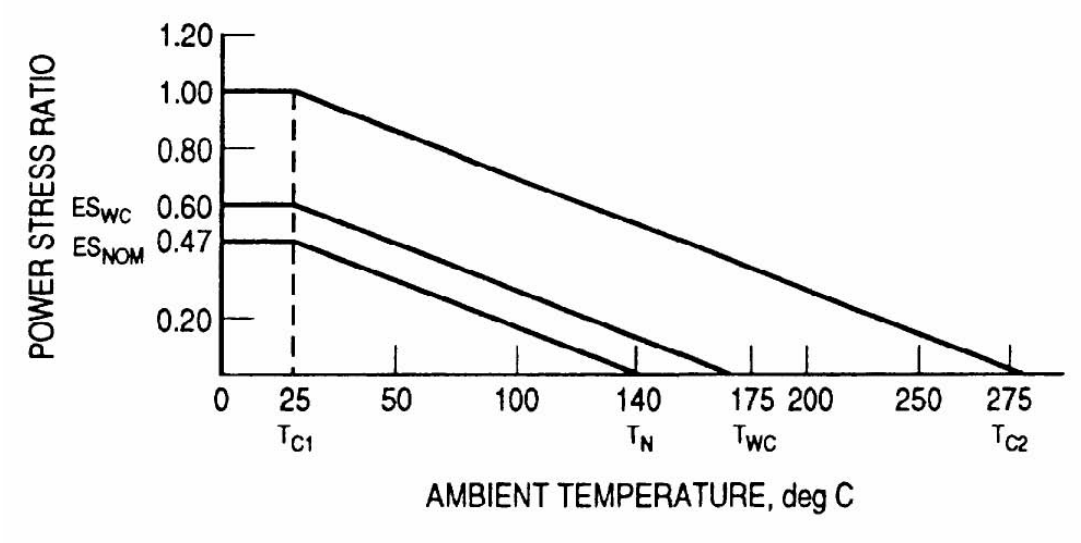

Figure 1170-1. Power derating requirements for wirewound (power-type) resistors.

2.1.2 Voltage Derating. RWR resistors are relatively low ohmic devices, and voltage derating is normally not required.

2.2 End-of-life Design Limits (Resistance) shall be:

a. ±1 percent for approved application

b. ±5 percent for worst-case application

2.3 Electrical Considerations

2.3.1 Temperature Coefficient. The temperature coefficient of resistance (due to wire variations) may be either negative or positive, and the values for each style are listed in the applicable MIL-PRF-39007 slash sheet.

2.3.2 High-Frequency Operation. These resistors are not designed for high-frequency circuits where their AC characteristics are important.

2.3.3 Noise. The only source of noise is thermal agitation, which can be neglected in most circuit applications.

2.3.4 Pulse Power. Steady-state power and voltage ratings for wirewound resistors do not apply to short time constant pulses. Figures 1170-2 through 1170-4 show the maximum power, which the resistors are typically capable of enduring for relatively short periods of time without significant changes in resistance or other parameters. Specific curves should be obtained from the manufacturer for each resistor type. The uses and limitations of these curves are as follows:

2.3.4.1 Maximum Pulse Power. Determine the maximum-pulse power rating for:

a. Non-repetitive Pulses
   - Calculate the pulse power: $P = (E^2/R)$
   - The maximum pulse-power rating is not exceeded if the intersection of the pulse-power line and pulse width line is on or below the pulse-power curve for the appropriate part.

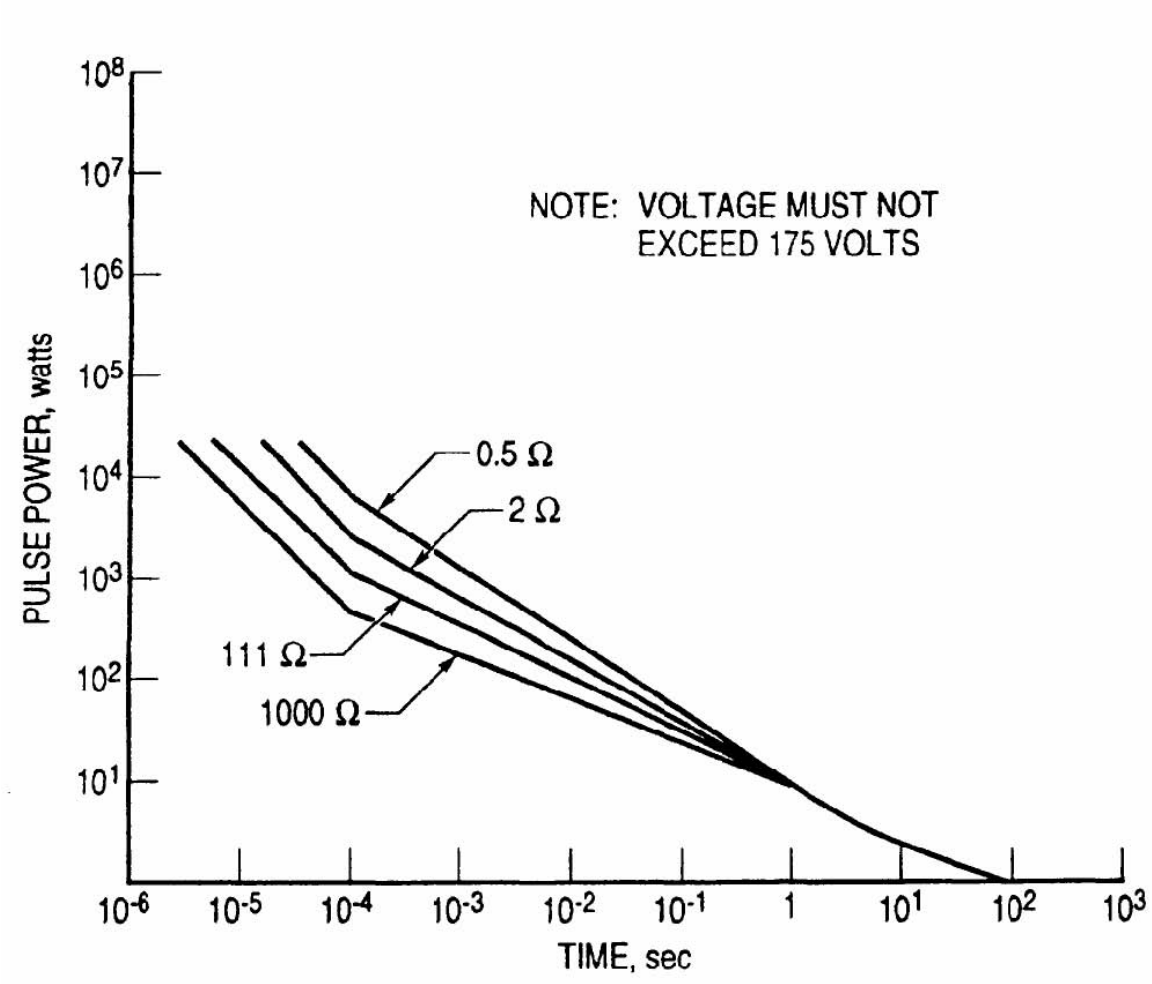

Figure 1170-2. Typical maximum pulse power versus time for RWR 81 (1-watt) resistors.

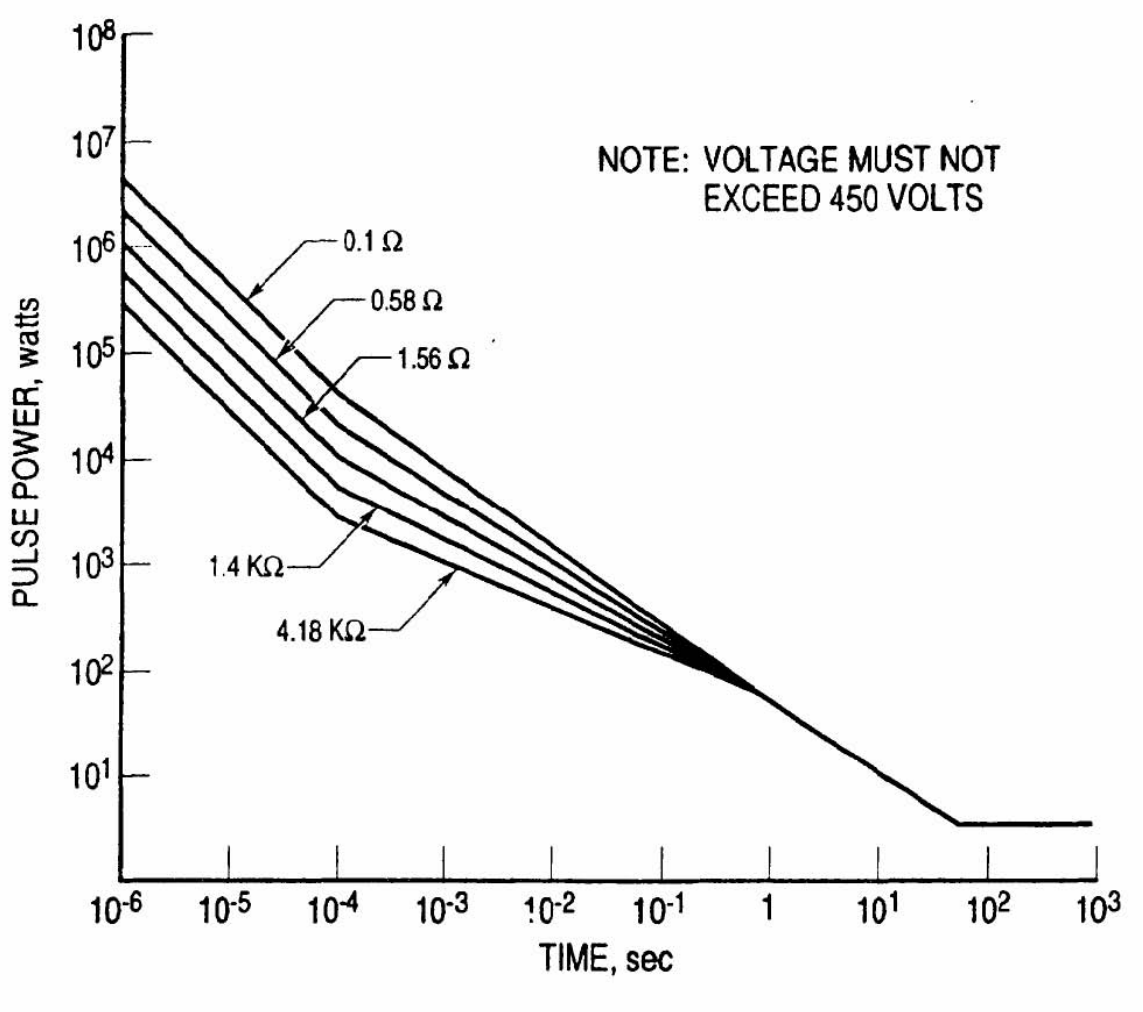

Figure 1170-3. Typical maximum pulse power versus time for RWR 89 (3-watt) resistors.

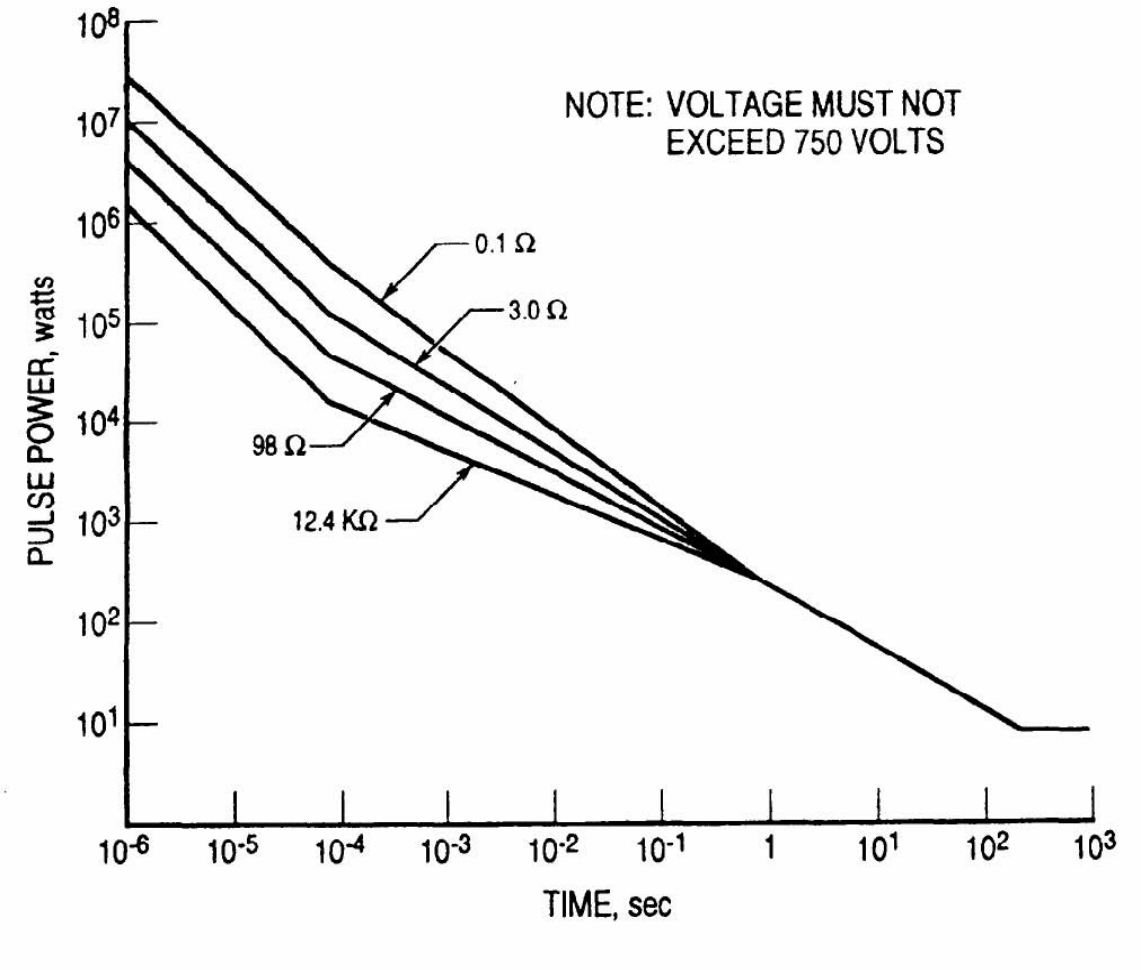

Figure 1170-4. Typical maximum pulse power versus time for RWR 84 (7-watt) resistors.

b. Repetitive Pulses

- Calculate the pulse-power and determine the maximum pulse power rating as in (a) above.
- If the maximum pulse power rating is not exceeded, determine the average pulse power:

P(avg)= P(t/T)

The average pulse power shall not exceed 50 percent of the steady-state power rating.

2.3.4.2 Maximum Pulse Voltage. The maximum pulse voltage shall be:

Style	Voltage
RWR81	175V
RWR89	450V
RWR84	750V

2.3.4.3 Limitations

a. Under reduced pressure conditions, the maximum pulse voltage shall not exceed 50 percent of the reduced dielectric strength of the air under the reduced pressure condition.

b. When the resistors are operated at temperatures above +25ºC, the pulse power rating shall be derated (see Fig. 1170-1).

c. When the resistors are operating under steady-state conditions and a pulse is applied in addition, the pulse power rating shall be derated so that the sum of the steady-state power plus the pulse power does not exceed the derating requirements of Figure 1170-1.

3. DESIGN AND CONSTRUCTION

3.1 Requirements. Design and construction shall be in accordance with the requirements of MIL-PRF-39007 and the requirements of this document. Coating material shall be per MIL-STD-199.

3.1.1 Wire Diameter. A minimum wire diameter of 25.4 microns (0.001 inch) shall be used.

3.1.2 Internal Connections. All internal connections shall be welded.

4. QUALITY ASSURANCE. Quality assurance provisions shall be in accordance with Section 4, General Requirements, of this document and the following:

4.1 In-process Controls. In-process controls shall be in accordance with the requirements of MIL-PRF-39007 and the following: All exposed inner surfaces of each resistor shall be examined at a minimum of 30X magnification. Any part exhibiting one or more of the following anomalies shall be rejected.

a. End cap misalignment greater than 5 degrees

b. Cracks, excessive bends, incomplete wire weld, or loose wire at end cap

c. Split, distorted, or cracked end caps

d. Space between wires turns more than five times the wire diameter, except for values less than 1.0 ohm or for fusible resistors (High resistance values require insulated wire and the wire turns may touch.)

e. Cracks or surface holes in core which exceed 0.025 inch in greatest dimension

4.2 Group A Requirements. Group A requirements shall be in accordance with the requirements in MIL-PRF-39007 and Table 1170-1.

4.3 Supplier DPA. Supplier DPA shall be in accordance with the requirements of MIL-PRF-39007 for T-level.

4.4 Group B Tests. Group B tests shall be in accordance with MIL-PRF-39007. In addition, the resistance temperature characteristics and moisture resistance tests specified in MIL-PRF-39007 shall be performed as part of Group B.

4.5 Qualification Tests. Qualification testing shall be in accordance with the requirements of MIL-PRF-39007.

4.6 Incoming Inspection DPA. Incoming inspection DPA shall be in accordance with MIL-STD-1580. All metal surfaces shall be verified for the absence of prohibited materials (e.g., pure tin, zinc, or cadmium).

5. REGISTERED (RELIABILITY SUSPECT) PMP shall include:

a. Designs using soldered or crimped internal connections are reliability suspect.

b. Designs using wire diameters less than 25.4 microns (0.001 inch) are reliability suspect.

6. PROHIBITED PMP shall include:

a. Resistors using prohibited materials in their construction (see Section 4, General Requirements, paragraph 4.3.3 of this document).

Table 1170-1. Group A Tests for Wirewound (Power Type) Resistors

MIL-PRF-39007	Modifications to the Methods, Requirements and Criteria of MIL-PRF-39007
Subgroup 1 (100 percent) 1/ Thermal Shock Conditioning Short Time Overload Dielectric Withstanding-Voltage DC Resistance	 DC resistance shall be within initially specified tolerance limits; lots having more than 10 percent out-of-tolerance rejects shall not be used
Subgroup 2 (100 percent) Radiographic Inspection	 Per MIL-PRF-39007 for T-level
Subgroup 3 Visual and Mechanical Examination Solderability DPA	 Per MIL-PRF-39007 for T-level Per MIL-PRF-39007 for T-level

1/ PDA for Subgroup 1 tests is 5 percent, or one resistor.

SECTION 1180

WIREWOUND, CHASSIS-MOUNTED RESISTORS (RER)

(MIL-PRF-39009)

1. SCOPE. This section sets forth detailed requirements for fixed, wirewound, power-type, chassis-mounted resistors. “R” failure rate RER resistors do not have to be subjected to the requirements of paragraphs 4.1, 4.2, 4.3 and 4.4 of this section. All other resistors of similar style/ type shall meet all the requirements of this section.

2. APPLICATION

2.1 Derating

2.1.1 Power Derating. Power derating shall be in accordance with Paragraph 2.1.1 of Section 1170.

2.1.2 Voltage Derating. Voltage derating shall be in accordance with Paragraph 2.1.2 of Section 1170.

2.2 End-of-life Design Limits. End-of-life design limits shall be in accordance with Paragraph 2.2 of Section 1170.

2.3 Electrical Considerations. See Paragraph 2.3 of Section 1170.

3. DESIGN AND CONSTRUCTION

3.1 Requirements. Design and construction shall be in accordance with the requirements of MIL-PRF-39009 and the requirements of this document.

3.1.1 Wire Diameter. A minimum wire diameter of 25.4 micrometers (0.001 inch) zero negative tolerance shall be used.

3.1.2 Internal Connections. All internal connections shall be welded.

4. QUALITY ASSURANCE. Quality assurance provisions shall be in accordance with Section 4, General Requirements, of this document and the following:

4.1 In-process Controls. In-process controls shall be in accordance with the requirements of MIL-PRF-39009 and the following: All exposed inner surfaces of each resistor shall be examined at a minimum of 30X magnification. Any part exhibiting one or more of the following anomalies shall be rejected.

a. End cap misalignment greater than 10 degrees
b. Cracks, excessive bends, incomplete wire weld, or loose wire at end cap
c. Split, distorted, or cracked end caps
d. Space between wires turns more than five times the wire diameter, except for values less than 1.0 ohm or for fusible resistors (High resistance values require insulated wire and the wire turns may touch.)
e. Cracks or surface holes in core which exceed 0.025 inch in greatest dimension

4.2 Group A Requirements. Group A requirements shall be in accordance with the requirements in MIL-PRF-39009 and Table 1180-1.

4.2.1 Supplier DPA. Supplier DPA shall be in accordance with the requirements of MIL-PRF-39007 for T-level.

4.3 Group B Tests. Group B tests shall be in accordance with the Group B tests in MIL-PRF-39009.

4.4 Qualification Tests. Qualification testing shall be in accordance with the requirements of MIL-PRF-39009.

4.5 Incoming Inspection DPA. Incoming inspection DPA shall be in accordance with MIL-STD-1580. All metal surfaces shall be verified for the absence of prohibited materials (e.g., pure tin, zinc, or cadmium).

5. REGISTERED (RELIABILITY SUSPECT) PMP shall include:

a. Designs using soldered or crimped internal connections are reliability suspect.

b. Designs using a wire diameter of less than 25.4 micrometers (0.001 inch) zero negative tolerance is reliability suspect.

6. PROHIBITED PMP shall include:

a. Resistors using prohibited materials in their construction (see Section 4, General Requirements, paragraph 4.3.3 of this document).

Table 1180-1. Group A Tests for Wirewound, Power-Type, Chassis-Mounted Resistors

MIL-PRF-39009	Modifications to the Methods, Requirements and Criteria of MIL-PRF-39009
Subgroup 1 (100 percent) 1/	
Thermal Shock	Test conditions and measurements after test shall be per MIL-PRF-39007 for T-level
Conditioning	
Short Time Overload	
Dielectric Withstanding-Voltage	
DC Resistance	DC resistance shall be within initially specified tolerance limits; lots having more than 10 percent out-of-tolerance rejects shall not be used.
Subgroup 2 (100 percent)	
Radiographic Inspection	Per MIL-PRF-39007 for T-level
Subgroup 3	
Visual and Mechanical Examination	
Solderability	
DPA	Per MIL-PRF-39007 for T-level

1/ PDA for Subgroup 1 tests is 5 percent, or one resistor.

SECTION 1190

FIXED FILM RESISTOR NETWORK (RZ)

(MIL-PRF-83401)

1. SCOPE. This section sets forth detailed requirements for a fixed-film resistor network installed in flat pack or dual-in-line packages. All resistor networks shall meet all the requirements of this section.

2. APPLICATION

2.1 Derating

2.1.1 Power Derating. Steady-state power applied to these resistors shall be limited to temperatures below +70ºC to 0.50 of the power rating values shown in Table 1190-1 for approved applications. Power applied to these resistors shall be limited to temperatures below +70ºC to 0.75 of the power rating values given in Table 1190-1 for worst-case applications. Both the steady-state and the worst-case power applied to these resistors shall be linearly reduced to zero power from +70ºC to +125ºC.

2.1.2 Voltage Derating. Voltage applied to these resistors shall be limited to 0.80 of the maximum voltage values shown in Table 1190-1.

Table 1190-1. Manufacturer's Element Power, Network Power, and Voltage Ratings

Resistor Style	Schematic Type	Element Power Rating at +70°C in watts	Network Power Rating at +70°C in watts	Maximum Voltage DC or AC (rms)
RZ010	A	0.2	1.4	100
RZ010	B	0.1	1.3	100
RZ020	A	0.2	1.6	100
RZ020	B	0.1	1.5	100
RZ030	A	0.05	0.35	50
RZ030**	B	0.025	0.325	50
RZ030**	A	0.2	1.0	50
RZ030	B	0.1	1.0	50
RZ040	C	0.2	1.8	50
RZ040	G	0.2	1.0	50
RZ050	C	0.2	1.8	50
RZ050	G	0.2	1.0	50
RZ060	C	0.2	1.8	50
RZ060	G	0.2	1.0	50
RZ070	C	0.12	0.6	50
RZ070	G	0.12	0.36	50
RZ080	C	0.12	0.84	50
RZ080	G	0.12	0.48	50
RZ090	C	0.12	1.08	50
RZ090	G	0.12	0.6	50

** Schematics are shown in detail specification of MIL-PRF-83401. RZ030 ratings are based on case temperature (heat sinking applied) up to +50°C for the total network and up to +90°C per element. Rating shown here is for thick film.

2.2 End-of-life Design Limits (Resistance) shall be:

a. ±1 percent for approved application

b. ±2 percent for worst-case application

2.3 Electrical Considerations. The resistance temperature coefficient (TC) can be either characteristic H (± 50 parts per million per ºC) or characteristic K (± 100 parts per million per ºC). Since all resistors in a network are manufactured from the same batch at the same time, the TCs should be matched within ±5 parts per million.

2.3.1 Humidity/Power Conditions. Nichrome film element used in a lot of resistor networks is susceptible to corrosion/dissolution when the part is operated under humid conditions, causing large increases in resistance values, or open circuit failures. Care shall be taken during handling, storage, board assembly or testing so as not to compromise the integrity of conformal coating, molded or hermetic case.

3. DESIGN AND CONSTRUCTION

3.1 Requirements. Design and construction shall be in accordance with the requirements of MIL-PRF-83401 and the requirements of this document. The resistance temperature coefficient (TC) shall be either characteristic H (± 50 parts per million per °C) or characteristic K (± 100 parts per million per °C). All resistors in a network shall be manufactured from the same batch at the same time.

3.2 Recommended

a. Tantalum nitride, deposited onto substrate, and protected by tantalum pentoxide passivation.

b. The surface should be anodized for moisture protection or laser-trimmed and subsequently glassivated.

c. Welded internal connections

d. Hermetically sealed units

4. QUALITY ASSURANCE. Quality assurance provisions shall be in accordance with Section 4, General Requirements, of this document and the following:

4.1 In-process Controls. In-process controls shall be in accordance with the requirements of MIL-PRF-83401 and the following:

4.1.1 Precap Visual Inspection. Precap visual inspection is required for all parts. A binocular microscope with at least 100X magnification and a coaxial illuminated or fiber optic light ring shall be used. The resistor side visual inspection shall be performed at 100X minimum magnification, perpendicular to the die surface, with illumination normal to the die surface. Any die exhibiting one or more of the following defects shall be marked and rejected.

4.1.1.1 Metallic Particles

a. Attached. Attached metallic particles shall not exceed 0.005 inch in the major dimension. Particles shall not touch nor extend over the metal film. Particles shall be considered attached when they cannot be removed with a 20 psig gas blow of dry nitrogen or dry, oil-free, air.

b. Residue. There shall be no residue from the spiral cutting operation at 100X magnification within the enclosure.

4.1.1.2 Nonmetallic Particles. Glass, fibers, and other nonmetallic materials within the enclosure shall not exceed 0.005 inch in their major dimension.

4.1.1.3 Metallization Defects. Any of the following anomalies in the active circuit metallization shall be cause for rejection.

a. Metallization Scratches. Any scratch in metallization through which the underlying resistor material also appears to be scratched. Any scratch in the interconnecting metallization which exposes resistive material or oxide anywhere along its length and reduces the width of the scratch-free metallization strip to less than 50 percent of its original width. A scratch is defined as any tearing defect that disturbs the original surface of the metallization.

b. Metallization Voids. Any void in the interconnecting metallization which leaves less than 50 percent of the original width undisturbed. A void is defined as any region in the interconnecting metallization where the underlying resistive material or oxide is visible which is not caused by a scratch.

c. Metallization Adherence. Any evidence of metallization lifting, peeling or blistering.

d. Metallization Probing. Probe marks on the interconnecting metallization other than the bonding pads that violate the scratch or void criteria.

e. Metallization Bridging. Bridged metallization defect that reduces the distance between any two metallization areas to less than 0.0003 inch. Bridging between metallization and resistor pattern not intended by design that reduces the distance between the two to less than 0.0001 inch.

f. Metallization Alignment. Any misalignment between the resistor pattern and the metallization such that more than 0.0005 inch of resistor on a side is exposed.

g. Metallization Corrosion. Any evidence of localized heavy stains, metallization corrosion, discoloration or mottled metallization.

4.1.1.4 Resistor Defects. Any of the following anomalies within the active resistor area shall be cause for rejection. The active area of resistor is that part of the resistance pattern which remains in series connection between resistor terminals and is not shorted by metallization.

a. Resistor Scratches. Any scratch within the active resistor area.

b. Resistor Voids. Any void or neckdown in the active resistor path, which reduces the width of the stripe by more than 50 percent of the original width. Any void or necking down in the active resistor path for a line width design of less than 0.0002 inch which reduces its original width by 25 percent or more. Any void or chain of voids in the resistor element at the gold termination.

c. Resistor Adherence. Any evidence of resistor film lifting, peeling or blistering.

d. Probe Marks. Any probe mark on the resistor material.

e. Resistor Material Corrosion. Any evidence of localized heavy stains or corrosion of resistor material in the active resistor path; however, discoloration of tantalum-based resistors due to thermal stabilization is not a cause for rejection.

f. Resistor Bridging Defects. Any conductive continuous bridging between active resistance stripes. A partial bridging defect is that which reduces the distance between adjacent active resistance stripes to less than 0.1 mil or 50 percent of the design separation, whichever is less, when caused by smears, photolithographic defects or other causes. For a partial bridge within lines and spacing of 0.0001 inch design width, visual separation (evident at 400X) is sufficient for acceptance.

4.1.1.5 Laser Trim Faults. Resistors that show any of the following shall be rejected:

a. A partially cut, or bridged, coarse or mid-range trim link.

b. The remaining width in fine-trim top hat area after laser cut is less than the width of the narrowest line within the same resistor pattern. Uncut material remains after a laser scribe due to “skipping” of the laser beam. If laser cut is not straight lines, the narrowest remaining width shall be equal to or greater than the width of the narrowest lines within the same resistor pattern.

c. Laser cut scribed to indicate a reject chip when the scribe does not meet the requirements of the individual mask model lists.

d. Oxide voids, cracking or similar damage caused to the SiO_2 underlayer by laser beam where such damage touches active interconnects or resistor path.

e. Laser trim cut where edge of cut touches the active resistor path.

f. Any discoloration or change in surface finish of a resistor stripe by the direct laser beam or by spurious reflections caused by optics of the system. Discoloration of tantalum-based resistors in and around laser kerf is not a cause for rejection.

g. Any chip intended to be laser-trimmed that is not laser-trimmed.

4.1.1.6 Resistor Bonding Pad Defects. Any resistor containing one or more bonding pads with one or more of the following anomalies shall be rejected.

a. Globules. A globule is defined as any material with a smooth perimeter extending out from the bonding pad onto the resistor or substrate material. Such globules are usually featureless and of low reflectivity and therefore difficult to focus upon.

b. Missing Metallization. Any indications of missing metallization whether at the perimeter or totally within the bonding pad. Resistor material may be visible in the areas of missing metallization.

c. Metallization Corrosion. Any evidence of localized heavy, diffuse stains, discolored material, or low-density material either on the pad's perimeter or totally within the bonding pad. Any evidence of stains or discoloration extending out onto the resistor or substrate material.

4.1.1.7 Oxide Defects. Any resistor having excessive oxide defects or voids shall be rejected. An oxide void is a fault in the oxide evidenced by localized double or triple colored fringes at the edges of the defect visible at 100X. The following shall be cause for rejection:

a. Any oxide void that bridges any two resistor or metal areas not intended by design.

b. Any oxide void under metallization or resistor geometry.

c. Less than 0.0005 inch oxide visible between active metallization and edge of a die. Excluded from this are any inactive metallization lines.

4.1.1.8 Scribing and Die Defects. Any resistor having the following scribing or die anomalies shall be rejected:

a. Any chipout or crack in the active resistor or metal area.

b. Any crack that exceeds 0.005 inch in length or comes closer than 0.001 inch to an active area on the die.

c. Any crack in a die that exceeds 0.001 inch in length and points towards the active circuit area.

d. A die having an attached portion of an adjacent die which contains metallization or resistor material.

e. A crack or chip in the backside of a die that leaves less than 75 percent of area intact or a crack or chip under a bonding pad.

4.2 Group A Requirements. Group A requirements shall be performed on a 100 percent basis in accordance with the requirements in MIL-PRF-83401 and Table 1190-2 and the following:

4.2.1 Fail Criteria. Resistor networks that are out of resistance tolerance, or which exhibit a change in resistance greater than that permitted, shall be removed from the lot. Lots having more than 5 percent total rejects due to resistance tolerance or resistance change shall be rejected.

4.2.2 Power Conditioning

a. The network shall be mounted to attain the test temperature condition noted below. Leads shall be mounted by means other than soldering or welding to avoid stress or damage to the leads. Networks shall be so arranged that the temperature of one network cannot appreciably affect the temperature of any other network.

b. Operating conditions shall be in accordance with MIL-PRF-83401. The supply voltage shall be regulated and controlled to maintain a tolerance ± 5 percent of the maximum voltage specified.

c. With the dc voltage applied, the ambient temperature shall be adjusted to obtain a case temperature of +70ºC, with a tolerance of +5ºC, -0ºC.

d. Initial and final resistance shall be at room ambient temperature

e. Test duration shall be 168 hours minimum

4.3 Group B Tests. Group B tests shall be performed on every lot in accordance with the Group B tests in MIL-PRF-83401.

4.4 Group C Tests. Group C tests shall be in accordance with MIL-PRF-83401, and performed on every lot.

4.5 Qualification Tests. Qualification testing shall be in accordance with the requirements of MTL-R-83401.

4.6 Incoming Inspection DPA. Incoming inspection DPA shall be in accordance with MIL-STD-1580. All metal surfaces shall be verified for the absence of prohibited materials (e.g., pure tin, zinc, or cadmium).

5. REGISTERED (RELIABILITY SUSPECT) PMP shall include:

a. Thick Film Designs. Resistor networks manufactured by thick film technology are reliability suspect due to the internal solder connections required.

b. Excessively Thin Tantalum Nitride. Designs requiring tantalum nitride thicknesses below 35 nanometers are reliability suspect due to the increased susceptibility of these parts to (a) mechanical handling damage, (b) opens resulting from “hot spots” at surface defects and (c) non-ohmic behavior at low voltages.

6. PROHIBITED PMP shall include:

a. Unpassivated Nichrome. Unpassivated nichrome resistors, either planar or discrete, shall not be used in networks due to the potential opening of nichrome traces in the presence of moisture and bias, even in hermetically sealed packages.

b. Resistors with prohibited materials in their construction (see Section 4, General Requirements, paragraph 4.3.3 of this document).

Table 1190-2. 100 Percent Group A Tests for Fixed-Film Resistor Networks

MIL-PRF-83401	Modifications to the Methods, Requirements and Criteria of MIL-PRF-83401
Precap Visual Inspection	Paragraph 4.1 of this section
Thermal Shock	
Power Conditioning	Paragraph 4.2.2 of this section
Short Time Overload	
Dielectric Withstanding Voltage	
Insulation Resistance	
DC Resistance	
Particle Impact Noise Detection (PIND)	For cavity devices only. MIL-STD-202, Method 217 Detection The lot shall be tested a maximum of 5 times. If less than 1 percent of the lot fails during any of the 5 runs, the lot may be accepted. All defective devices shall be removed after each run. Lots which do not meet the 1 percent PDA on the fifth run, or cumulatively exceed 25 percent defectives, shall be rejected.
Radiographic Inspection	
Seal	For hermetic devices only.
Visual and Mechanical Examination (External)	Marking and identification Defects and damage, i.e., body finish, lead finish, misalignment, cracks
Solderability	

SECTION 1195

THERMISTORS (RTH)

(MIL-PRF-23648 AND MIL-PRF-32192)

1. SCOPE. This section sets forth detailed requirements for thermistors, i.e., temperature-sensitive resistors. There are two classes of thermistors, one with positive temperature coefficients of resistance (PTC) and one with negative coefficients (NTC).

2. APPLICATION

2.1 Derating

2.1.1 Positive Temperature Coefficient (PTC). Positive temperature coefficient thermistors are generally operated in the self-heat mode (heated as a result of current passing through). Such parts should be derated to 50 percent of their rated power at any given temperature as provided in the thermal derating curve of a given slash sheet.

2.1.2 Negative Temperature Coefficient (NTC). Negative coefficient types operated in the self-heat mode shall be derated in accordance with Figure 1195-1 to prevent thermal runaway. Such parts should be derated to a power level causing a maximum increase of 50 times the dissipation constant or a maximum part temperature of 100ºC, whichever is less. Operation in a heat-sunk mode allows greater power levels.

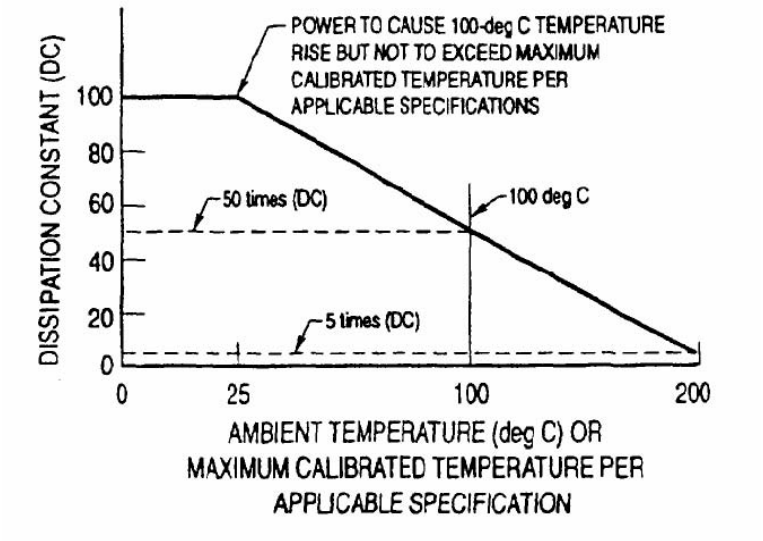

Figure 1195-1. Derating curve for negative coefficient thermistors.

2.2 End-of-life Design Limits Resistance (for Five Years) shall be:

a. Glass Bead (Negative TC) ± 1.3 percent + initial tolerance *
b. Bead Encapsulated (Positive TC) ± 1.8 percent + initial tolerance *
c. Disc (Positive or Negative TC) ± 5 percent + initial tolerance *

*EOL resistance factor is the total RSS (root sum square) design tolerance:

Total design tolerance = $[(\text{Aging} + \text{initial tolerance})^2 + (\text{environments})^2]^{1/2}$

2.3 Electrical Considerations. The following circuit design cautions shall be observed:

a. Use a current limiting resistor or a series circuit design when using a fixed voltage source to prevent the negative coefficient type thermistor from going into thermal runaway.

b. Never exceed the maximum current or power rating, even for short time periods.

c. Never move a thermistor (used in the self-heat mode) into a medium of lower thermal conductivity without careful analysis in order to prevent thermal runaway conditions.

d. Accurate thermistors (± 1 percent) are calibrated for specific temperature test points; operation beyond the test points could result in permanent tolerance changes greater than those allowed for in the calibration.

2.3.1 Mounting. The following shall be considered when mounting thermistors:

a. The dissipation constant is specified in still air with the thermistor suspended by its leads. Any thermal or mechanical contact with an item acting as a heat sink, or change in surrounding media, changes the resistance of the thermistor.

b. Heat sinks should be used when soldering to thermistor leads.

2.4 Radiation Environment Considerations. PTC thermistors with silicon elements can be sensitive to radiation. As a minimum, the effects of the expected radiation environments on the part performance in the application shall be analyzed to verify the component will operate successfully. All mitigation strategies shall be documented. The environments addressed shall include the expected natural space environment calculated over the intended life of the mission and any additional nuclear enhanced environment specified in the system specification.

3. DESIGN AND CONSTRUCTION

3.1 Requirements. Design and construction shall be in accordance with the requirements of MIL-PRF-23648 or MIL-PRF-32192 and the requirements of this document.

3.2 Recommended

a. Glass bead style.

b. Hermetically sealed thermistor where appropriate. (The only hermetically sealed thermistor available in MIL-PRF-23648 is the /19, a PTC device type.)

4. QUALITY ASSURANCE. Quality assurance provisions shall be in accordance with Section 4, General Requirements, of this document and the following:

4.1 In-process Controls. In-process controls shall be in accordance with the requirements of MIL-PRF-23648 or MIL-PRF-32192.

4.2 Group A Requirements. Group A requirements shall be in accordance with the requirements in MIL-PRF-23648 and Table 1195-1. Chip thermistors shall be Group A tested in accordance with the requirements of MIL-PRF-32192 and Table 1195-1.

4.3 Group B Tests. Group B tests shall be in accordance with the requirement in MIL-PRF-23648 and Table 1195-2. Chip thermistors shall be Group B tested in accordance with the requirements of MIL-PRF-32192 and Table 1195-2.

4.4 Qualification Tests. Qualification testing shall be in accordance with the requirements of MIL-PRF-23648. Qualification testing of chip thermistors shall be in accordance with the requirements of MIL-PRF-32192.

4.5 Incoming Inspection DPA. Incoming inspection DPA shall be in accordance with MIL-STD-1580. All metal surfaces shall be verified for the absence of prohibited materials (e.g., pure tin, zinc, or cadmium).

5. REGISTERED (RELIABILITY SUSPECT) PMP shall include:

a. Disc-type thermistors that absorb water
b. Thermistors that are mechanically fragile and easily break
c. Nonpassivated devices
d. Plastic encapsulated units
e. Internal organic/polymeric materials (lacquers, varnishes, coatings, adhesives, or greases)
f. Bimetallic lead bond at die
g. Ultrasonically cleaned parts

6. PROHIBITED PMP shall include:

a. Thermistors using prohibited materials in their construction (see Section 4, General Requirements, paragraph 4.3.3 of this document).

Table 1195-1. Group A Tests for Thermistors

MIL-PRF-23648 and MIL-PRF-32192	Modifications to the Methods, Requirements and Criteria of MILPRF-23648 and MIL-PRF-32192
Zero Power Resistance (Initial)	a. At +25ºC
Thermal Shock	a. Maximum of 1.0 percent change
Bake (High temperature storage)	a. 100 hours at maximum specified operating temperature
Burn-in	a. For positive TC devices only
	b. 168 hours at +25ºC and rated power
Zero Power Resistance	
Resistance Ratio Characteristic	
Insulation Resistance (Not applicable to chip thermistors)	a. Minimum of 500 megohms
Visual and Mechanical Examination (External)	a. Marking and identification
	b. Defects and damage; i.e., body finish/ lead finish, misalignment, cracks
Solderability (Not applicable to gold terminations)	

Table 1195-2. Modifications to Group B Tests for Thermistors

MIL-PRF-23648 and MIL-PRF-32192Tests	Modifications to the Methods, Requirements and Criteria of MIL-PRF23648 and MIL-PRF-32192
Subgroup 1	
Short Time Overload	a. Maximum delta Zero Power Resistance: 1 percent
Dielectric Withstanding Voltage (Not applicable to chip thermistors)	
Insulation resistance (Not applicable to chip thermistors)	
Low Temperature Storage	
High Temperature Exposure	
Dissipation Constant	a. Maximum delta Zero Power Resistance: 1 percent
Terminal Strength (Not applicable to chip thermistors)	Minimum 1.0 pound strength Maximum delta Zero Power Resistance: 0.5 percent
Subgroup 2	
Resistance to Solvents	
Subgroup 3 (Chip thermistors only.)	In accordance with MIL-PRF-32192
Solder mounting integrity	
Bondable mounting integrity	
Wire bonding integrity	

SECTION 1200

SWITCHES

1. SCOPE. This section sets forth common requirements for switches. Table 1200-1 lists the military specifications for the general switch types and indicates the applicable section in this standard where detailed requirements are set forth.

Table 1200-1. Switch Types

Section Number	Switch Type	Specification Number
1210	Sensitive and push (snap action)	MIL-S-8805
1220	Thermostatic (Thermal)	MIL-PRF-24236
1230	Pressure	MIL-S-9395

2. APPLICATION. The selection and use of switches and associated hardware shall be in accordance with the requirements contained herein. Contact data such as loads, protection, arc suppression, and noise -suppression are similar to those for relay contacts of the equivalent type. See Section 1000 of this standard for applicable information.

2.1 Derating. Derating of switch contacts for operation at ambient temperature shall be in accordance with the derating requirements for relay contacts in Section 1000.

2.2 Electrical Considerations. Each switch is rated for a specified number of operations at rated current and voltage parameters over a specific temperature range.

2.2.1 Contact Current. For Sensitive, Push and Pressure only: Current during make, break and continuous duty shall be carefully considered. Ratings of contacts are usually given for room temperature. As the ambient temperature increases, switching current ratings are reduced. Typical switch currents versus temperatures are shown in Figure 1200-1 for a typical switch.

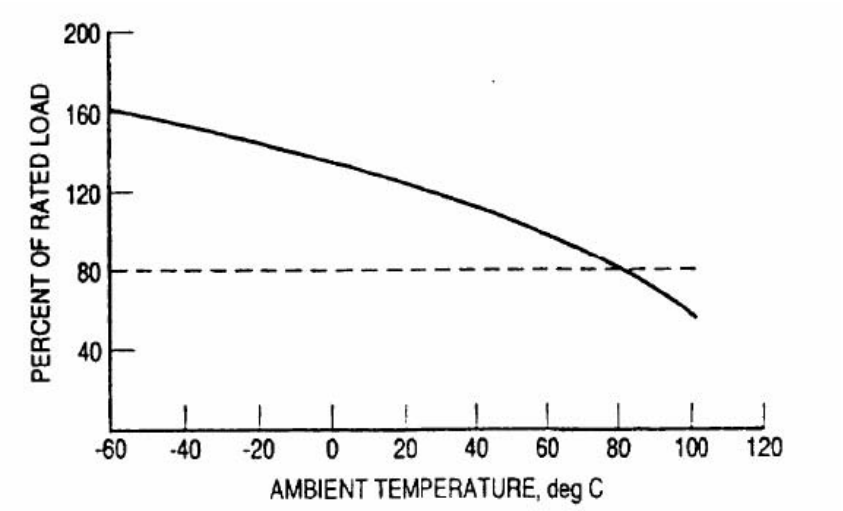

Figure 1200-1. Switch current rating versus temperature for a typical switch (not applicable for thermostatic type).

2.2.2 Cautions

2.2.2.1 Manually Operated Switch. Manually operated switches that are not toggle or snap action can have the contacts damaged or seriously reduce their load handling capabilities when the switch is deliberately operated in slow motion.

2.2.2.2 Load Considerations. For inductive loads, low level loads, intermediate range loads, parallel contacts, series contacts, dry circuit switching, transformer switching, transient suppression, and dynamic contact resistance, the requirements of MIL-STD-1346 (as applicable) shall apply.

2.2.2.3 Environmental Conditions. The environmental conditions shall be considered when using the leaf type actuator. Uncontrolled forces due to shock, vibration, and acceleration can result in inadvertent plunger actuation.

3. DESIGN AND CONSTRUCTION

3.1 Requirements. Design and construction shall be in accordance with the requirements of the applicable specifications and the requirements of this standard.

3.2 Construction Controls. The following controls shall apply:

a. Each switch not being assembled or inspected shall be kept in a clean dust-free enclosure.

b. Subsequent to final cleaning and assembly, all open switches shall be worked on under a controlled clean room environment with laminar flow hood, or similar measures to eliminate particulate contamination.

c. Pre-closure wash (Millipore) and cleanliness verification (micro-particle analysis) shall be accomplished per Section 1000, or in accordance with a PMPCB approved equivalent procedure.

3.3 Recommended. Recommended designs and constructions are:

a. Switch shaft and housing of corrosion-resistant material
b. High contact pressures in cold environments
c. Hermetically sealed
d. Snap-action style contacts
e. Positive break
f. Panel seal

4. QUALITY ASSURANCE. The quality assurance requirements for snap action switches, thermal switches, and pressure switches are stated in subsequent sections of the standard. Quality assurance provisions for other switches shall be in accordance with Section 4, General Requirements, of this document and the following:

4.1 In-process Controls. In-process controls shall be in accordance with the requirements of the applicable specifications, and the following:

4.1.1 Internal Visual Inspection Inspect 100 percent at 10X minimum for:

a. Particles greater than 25.4 micrometers (0.001 inch) in maximum dimension shall be rejected.
b. Solder and weld joints
c. Proper alignment
d. Feedthroughs with contamination, debris, damage or misalignment shall be rejected.
e. Normal contacts

4.1.3 Additional Requirements. The following requirements shall apply:

a. Inspect seals and encapsulation 100 percent at 10X minimum for cracks

b. Leads and terminals are clean, straight, and free of prohibited materials

c. Each switch shall have its contact closure force setting checked by the manufacturer to comply with requirements of detailed specifications with full documentation provided.

d. Each switch shall have its critical internal dimensions checked for correctness and detail.

4.2 Screening (100 percent). Screening shall be in accordance with the requirements in the applicable specifications. Unless otherwise specified, the screening shall include 500 cycles minimum of run-in testing with contacts monitored for misses at 6 Volts dc, 100 milliamperes maximum.

4.3 Lot Conformance Tests. Lot conformance tests shall be in accordance with the Group B, or equivalent, tests in the applicable specifications.

4.4 Qualification Tests. Qualification testing shall be in accordance with the requirements of the applicable specifications.

4.5 Incoming Inspection DPA. Incoming inspection DPA shall be in accordance with MIL-STD-1580.

5. REGISTERED (RELIABILITY SUSPECT) PMP shall include:

a. Nonhermetic units

b. Noncorrosion resistant materials

c. Slide devices

6. PROHIBITED PMP shall include:

a. Switches using prohibited materials in their construction (see Section 4, General Requirements, paragraph 4.3.3 of this document).

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SECTION 1210

SENSITIVE AND PUSH (SNAP ACTION) SWITCHES

(MIL-PRF-8805)

1. SCOPE. This section sets forth detailed requirements for hermetically sealed snap-action switches.

2. APPLICATION. See Section 1200.

3. DESIGN AND CONSTRUCTION

3.1 Requirements. Design and construction shall be in accordance with the requirements of MIL-PRF-8805 and the requirements of this document.

3.2 Recommended. See Section 1200.

4. QUALITY ASSURANCE. Quality assurance provisions shall be in accordance with Section 4, General Requirements, of this document and the following:

4.1 In-process Controls. In-process controls shall be in accordance with the requirements of MIL-PRF-8805. Internal visual inspection shall also be in accordance with the requirements of Paragraph 4.1 in Section 1200. In addition, devices shall be inspected at 10X minimum for the following defects. Devices exhibiting any of the following defects shall be rejected:

a. Adhering conductive or nonconductive particles (metal burrs or case flashing)

b. Incomplete (less than 360 degrees) swaging, or staking of assembly components

c. Scratches or nicks in contact surface areas

4.2 Screening (100 percent). Screening (100 percent) shall be in accordance with the requirements listed in Table 1210-1.

4.3 Lot Conformance Tests. Lot conformance tests shall be in accordance with the Group B tests in MIL-PRF-8805.

4.4 Qualification Tests. Qualification testing shall be in accordance with the requirements of MIL-PRF-8805.

4.5 Incoming Inspection DPA. Incoming inspection DPA shall be in accordance with MIL-STD-1580. All metal surfaces shall be verified for the absence of prohibited materials (e.g., pure tin, zinc, or cadmium).

5. REGISTERED (RELIABILITY SUSPECT) PMP shall include:

a. Switches using thermoplastic dielectric or packaging.

6. PROHIBITED PMP shall include:

a. Switches using prohibited materials in their construction (see Section 4, General Requirements, paragraph 4.3.3 of this document).

Table 1210-1. 100 Percent Screening Requirements

MIL-PRF-8805 Screens	Modifications to the Methods, Requirements and Criteria of MIL-PRF8805
Operating Characteristics	
Dielectric Withstanding-Voltage	
Contact Resistance	
Vibration (Random)	MIL-STD-202, Method 214, Test Condition II, K (switch in critical system position and test to the requirements of the application) 3 orthogonal planes, 1 minute each Mounting fixture shall not add or remove energy from switch under test Monitored for contact chatter, 10 microseconds maximum per MIL-STD-202, Method 310, Circuit B No contact transfer (monitor equipment be capable of detecting closures greater than 1 microsecond) If more than one critical system position exists, repeat steps a, b, c, d, and e, with the switch in each critical position.
Thermal Shock	During last cycle (5th), measure contact resistance at temperature extremes
Particle Impact Noise Detection (PIND)	MIL-STD-202, Method 217 Detection The lot shall be tested a maximum of 5 times. If less than 1 percent of the lot fails during any of the 5 runs, the lot may be accepted. All defective devices shall be removed after each run. Lots which do not meet the 1 percent PDA on the fifth run, or exceed 25 percent defectives cumulative, shall be rejected.
Insulation Resistance	
Mechanical Run-in	500 cycles at 10 cycles per minute at +25ºC Monitor all make and break contacts at 6 VDC, 100 mA max
Seal	
Dielectric Withstanding-Voltage	
Insulation Resistance	
Operating Characteristics	
Radiographic Inspection	Per MSFC-STD-355; 2 conventional x-ray views 90 degrees apart, or 360-degree view using "real-time" x-ray (preferred).
Visual and Mechanical Examination (External)	Marking and identification Defects and damage; i.e., body finish, lead finish, misalignment, cracks
Solderability	

SECTION 1220

THERMAL SWITCHES

(MIL-PRF-24236)

1. SCOPE. This section sets forth detailed requirements for thermal switches.

2. APPLICATION

2.1 Derating. The derating requirements given in Section 1000 for relay contacts shall be used to derate switch contacts.

2.2 Electrical Considerations. Bimetallic disc thermal switches are used for thermal control and thermal protection. They have the advantage of being lightweight, sturdy (withstand high shocks of 750 g and vibration of 60 g rms random), and require no external power.

2.2.1 Anomalous Switch Behaviors. Some of the anomalous switch behaviors involved fast cycling in both upper and lower set point. These anomalies are known as “creepage” or “dithering”.

2.2.1.1 Creepage. Creepage is defined as an opening or closing of the switch contacts not concurrent with the disc snap. This condition can lead to increased contact wear and shortened switch life as well as increased potential for welded contacts on higher load applications.

2.2.1.2 Dither. Dither is defined as the opening or closing of the switch contacts caused by internal I^2R self heating. This condition exhibits itself in a series of openings and closings with some loss in thermal accuracy.

These failure anomalies usually are exhibited and screened out during acceptance testing and are therefore rarely seen in the field.

2.2.1.2.1 Creepage mitigation. Creepage can be mitigated by performing controlled temperature rate of change creepage test performed at 500 Vdc minimum, 5 ms maximum allowable arc duration, 1ºC/minute rate of change is a good screen.

2.2.1.2.2 Dither mitigation. Dither can be mitigated by minimizing internal switch resistance through design and material choice and observing established derating criteria.

2.3 Electrical Requirements. To alleviate the possibility of dither, a 2.2ºC minimum thermal deadband shall be required (temperature separation between the thermal switch “on” position and the switch “off” position).

3. DESIGN AND CONSTRUCTION

3.1 Requirements. Design and construction shall be in accordance with the requirements of MIL-PRF-24236 and the requirements of this standard.

3.2 Recommended designs include:

a. Snap-action.

b. Contact current rating, 5 amperes maximum

4. QUALITY ASSURANCE. Quality assurance provisions shall be in accordance with Section 4, General Requirements, of this document and the following:

4.1 In-process Controls. In-process controls shall be in accordance with the requirements of MIL-PRF-24236 and the following:

Section 1220 THERMAL SWITCHES

4.1.1 Switch Assembly

a. Each switch shall have its contact closure and opening force setting checked and documented.

b. Each switch shall have its critical internal dimensions checked for correctness.

c. Each switch not being assembled or inspected shall be kept in a clean dust-free enclosure.

d. Subsequent to final cleaning and assembly, all open switches shall be maintained in a controlled clean room environment with laminar flow hood, or similar measures, to eliminate particulate contamination.

e. All switches that utilize different materials for movable and stationary contacts shall have the terminal polarity identified as + or – and the life verified by tests with voltage applied in the polarity specified.

4.1.2 Precap Visual Inspection (100 percent). Precap visual inspection shall be performed at 30X minimum magnification under laminar flow hood, or equivalent, that can preclude particulate contamination. The following conditions shall be rejectable:

a. Particle contamination greater than 25.4 micrometers (0.001 inch) in maximum dimension.

b. Plating defects such as flaking or blistering.

c. Loose oxide film on surface of bimetallic disc.

d. Organic compounds or films on contacts or header base.

e. Sharp peaks, cracks, chips, and flakes on actuator chips.

f. Radial cracks on the glass seal extending greater than one-half the distance from the center post to the outside edge.

4.1.3 Cleaning (Pre-Seal) and Small Particle Inspection (100 percent). Thermostatic switches, cans, and any other parts or subassemblies that constitute the final assembly shall be subjected to micro-particle cleaning and inspection prior to insertion into their enclosures. Devices containing particles greater then 25.4 micrometers (0.001 inch) in maximum dimension shall be rejected. Micro-particle cleaning and inspection shall be in accordance with the manufacturer’s standard procedures. A copy of the manufacturer’s documented micro-particle cleaning and inspection procedures shall be available for review by the procuring activity upon request.

4.1.4 Screening (100 percent). Screening shall be in accordance with the requirements listed in Table 1220-1.

Table 1220-1. 100 Percent Screening Requirements for Thermal Switches

Test No. 1/	Test Description	Reference Paragraph
1	Post screen Internal Visual (Pre-seal) Inspection	4.1.5
2	Micro-particle Cleaning and Inspection	4.1.6
3	Run-in 2/	4.1.7
4	Vibration	4.1.8
5	Particle Impact Noise Detection (PIND)	4.1.9
6	Calibration	4.1.10
7	Creepage	4.1.11
8	Seal	4.1.12
9	Dielectric Withstanding Voltage (DWV)	4.1.13
10	Insulation Resistance	4.1.14
11	Contact Resistance	4.1.15
12	External Visual and Mechanical Examination	4.1.16

1/ Tests shall be performed in the order listed.

2/ As an option, run-in may be performed after PIND.

4.1.5 Post Screen Visual Inspection. A 100 percent pre-seal visual inspection shall be performed. The internal visual inspection shall be performed using appropriate magnification (10X minimum). The purpose of this examination is to detect faulty workmanship and extraneous particles or materials that are not a required functional part of the mechanism. This examination shall be made on the header assembly, disc, and case, and shall be made from all views necessary to ensure the absence of contamination from contacts and crevices. In addition, the following is required:

a. There shall be no evidence of case distortion, which could impair operation of the switch. Any damage or indentation of the weld rim or disc seating surfaces shall be a cause for rejection. There shall be no evidence of blistering, or flaking of the plating from either the base or terminal posts.

b. Transfer pins (striker pins) or insulators that have sharp peaks, cracks, or loose flaking shall be rejected.

c. There shall be adequate clearance around moving parts, and adequate spacing or proper insulation of isolated electrical parts.

4.1.6 Micro-particle Cleaning and Inspection. Switches, thermostatic, shall be subjected to micro-particle cleaning and inspection prior to insertion into their enclosures. Micro-particle cleaning and inspection shall be in accordance with Section 1000, or a PMPCB approved equivalent procedure.

4.1.7 Run-in (pre-Acceptance conditioning). Switches shall be operated for a minimum of 500 consecutive total cycles (one cycle constitutes one closure and one opening of the switch contacts). The switch shall be alternately heated and cooled to switch at the maximum actuating temperature and the minimum actuating temperature. The switch cycling rate shall not exceed three cycles per minute. The contacts shall switch a load of 6 ± 1 VDC @ 100 ± 25mA. This test shall be monitored to verify the proper switch function and contact resistance. There shall be no evidence of intermittent contact operation. The monitored contact resistance during each cycle shall not exceed 100 milliohms.

4.1.8 Vibration (Random). Testing shall be performed per Method 214, MIL-STD-202 with the following details and exceptions:

Frequency	Spectrum
20 Hz	0.01 g2/Hz
20 – 90 Hz	Increase, 9 dB/octave
90 – 350Hz	0.9 g2/Hz
350 – 2000Hz	Decrease, -6 dB/octave
Overall Grms	22.7

a. Switches are to be functioning during testing: contacts shall be connected to a power supply at the manufacturer's specified voltage and load current to monitor switching and contact chatter. There shall be no opening of closed contacts or closing of open contacts in excess of 10 microseconds. Afterwards, there shall be no evidence of mechanical damage.

b. Perform for 1 minute per axis per contact position in each of 3 mutually perpendicular axes, 6 minutes total per device.

4.1.9 Particle Impact Noise Detection (PIND) Switches, thermostatic shall be PIND tested in accordance with the manufacturer's standard PIND test procedure. A copy of the manufacturer's documented PIND test procedure shall be available for review by the procuring activity upon request. There shall be no evidence of particulate contamination. The following conditions apply:

a. The switch has to be in a thermal state that applies force to the loose member.

b. The switch's thermal rating can't exceed the ambient environmental rating of the PIND equipment. (If the switch's rating does exceed the thermal capability of the PIND equipment, it will have to rely on particle analysis of 4.1.6.)

4.1.10 Calibration. When switches are tested as specified in MIL-PRF-24236, quality conformance inspection calibration method for switches, the operating points for the opening and closing temperatures shall be within the tolerance specified.

4.1.11 Creepage. Switches shall be heated or cooled as specified with a temperature rate of change of less than 1ºC per minute for three complete cycles. Voltage to be switched shall be 500 VDC minimum with sufficient load to limit the current to 1 milliampere maximum. The switch shall respond to specified temperature changes with immediate positive snap action. The arc duration shall not exceed 5 milliseconds.

4.1.12 Seal. The test method and requirements shall be in accordance with MIL-PRF-24236.

4.1.13 Dielectric Withstanding Voltage (DWV). The test method and requirements shall be in accordance with MIL-PRF-24236.

4.1.14 Insulation Resistance. The test methods and requirements shall be in accordance with MIL-PRF-24236.

4.1.15 Contact Resistance. The test methods and requirements shall be in accordance with MIL-PRF-24236. Unless otherwise specified in the detail specification, the contact resistance shall not exceed 25 milliohms.

4.1.16 External Visual and Mechanical Examination. The switches shall be examined to verify that the workmanship, configuration and dimensions are in accordance with paragraph 3.1.

4.2 Lot Conformance Tests. Lot conformance tests shall be in accordance with the Group B tests in MIL-PRF-24236 with the following exceptions:

a. Solderability per MIL-PRF-24236

b. MIL-PRF-24236, Group B tests not required on each lot are as follows:

Subgroup 1 – Moisture Resistance
Flame Response
Short Circuit
Overload Cycling

Subgroup 3 – No tests of this subgroup required
Subgroup 4 – Sensitivity Response
Temperature Anticipation

(All tests of Subgroup 2 shall be performed)

c. Endurance test per MIL-PRF-24236 shall be performed at 28 VDC, 5 amperes for 100,000 cycles using a resistive load.

4.2.1 Residual Gas Analysis (RGA) RGA per MIL-STD-883 Test Method 1018 shall be performed on 2 pcs per sealing lot (i.e., material vacuum-baked and final-sealed as a batch) to verify moisture content of 5,000 ppm (maximum).

4.3 Qualification Tests. Qualification testing shall be in accordance with the requirements of MIL-PRF-24236 with the addition of a test for resistance to soldering heat per Condition B of Method 210 of MIL-STD-202.

4.4 Incoming Inspection DPA. Incoming inspection DPA shall be in accordance with MIL-STD-1580. All metal surfaces shall be verified for the absence of prohibited materials (e.g., pure tin, zinc, or cadmium).

5. REGISTERED (RELIABILITY SUSPECT) PMP shall be the same as paragraph 5 of Section 1200.

6. PROHIBITED PMP shall include:

a. Switches using prohibited materials in their construction (see Section 4, General Requirements, paragraph 4.3.3 of this document).

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SECTION 1230

PRESSURE SWITCHES

(MIL-DTL-9395)

1. SCOPE. This section sets forth detailed requirements for hermetically sealed pressure switches.

2. APPLICATION. See Section 1200.

3. DESIGN AND CONSTRUCTION

3.1 Requirements. Design and construction shall be in accordance with the requirements of MIL-DTL-9395 and the requirements of this document. (See the requirements of Section 1200 and Section 300, as applicable.)

4. QUALITY ASSURANCE. Quality assurance provisions shall be in accordance with Section 4, General Requirements, of this document and the following:

4.1 In-process Controls. In-process controls shall be in accordance with the requirements of MIL-DTL-9395 and Paragraph 4.1 in Section 1200.

4.2 Screening (100 percent). Screening (100 percent) shall be in accordance with the requirements listed in Table 1230-1.

4.2.1 Lot Conformance Tests. Lot conformance tests shall be in accordance with the requirements in Table 1230-2.

4.2.2 Qualification Tests. Qualification testing shall be in accordance with the requirements of MIL-DTL-9395.

4.2.3 Incoming Inspection DPA. Incoming inspection DPA shall be in accordance with MIL-STD-1580. All metal surfaces shall be verified for the absence of prohibited materials (e.g., pure tin, zinc, or cadmium).

5. REGISTERED (RELIABILITY SUSPECT) PMP shall include:

a. Nonhermetic units
b. Noncorrosion resistant materials or tin in units
c. Slide devices

6. PROHIBITED PMP shall include:

Switches using prohibited materials in their construction (see Section 4, General Requirements, paragraph 4.3.3 of this document).

Table 1230-1. 100 Percent Screening Requirements for Pressure Switches

MIL-DTL-9395 Screens	Modifications to the Methods and Criteria of MIL-DTL-9395
Vibration (Random)	MIL-STD-202, Method 214, Test Condition II, K (switch in critical system position and test to the requirements of the application) 3 orthogonal planes, 1 minute each Mounting fixture shall not add or remove energy from switch under test Monitored for contact chatter, 10 microseconds maximum per MIL-STD202, Method 310, Circuit B No contact transfer (monitor equipment shall be capable of detecting closures greater than 1 microsecond) If more than one critical system position exists, repeat steps a, b, c, d, and e, with the switch in each critical position.
Vibration (Sine)	MIL-STD-202, Method 204
High Temperature	
Low Temperature	
Particle Impact Noise Detection (PIND)	MIL-STD-202, Method 217 Detection The lot shall be tested a maximum of 5 times. If less than 1 percent of the lot fails during any of the 5 runs, the lot may be accepted. All defective devices shall be removed after each run. Lots which do not meet the 1 percent PDA on the fifth run, or exceed 25 percent defectives cumulative, shall be rejected.
Mechanical Run-in	500 cycles at 10 cycles per minute at +25ºC Monitor all make and break contacts at 6 VDC 100 mA max. c. Miss test monitoring equipment to measure contact resistance required.
Proof Pressure	
Calibration	
Coincidence of Operation	Multi-pole only
Contact Resistance	
Dielectric Withstanding-Voltage	
Seal	
Radiographic Inspection	Per MSFC-STD-355; 2 conventional x-ray views 90 degrees apart, or 360-degree view using "real-time" x-ray (preferred).
Visual and Mechanical Examination (External)	Marking and identification b. Defects and damage; i.e., body finish, lead finish, misalignment, cracks

Table 1230-2. Lot Conformance Tests for Pressure Switches

MIL-DTL-9395 Screens	Modifications to the Methods and Criteria of MIL-DTL-9395
Group I	Samples. NOTE: Because this sampling plan is different than MIL-DTL-9395, the group samples shall be unique and cannot be used in more than 1 group test.
Solderability	If applicable
Shock	
Moisture Resistance	
Overload Cycling	
Seal	
Group II	3 Samples
Mechanical Endurance	
Electrical Endurance	
Contact Resistance	
Seal	
Dielectric Withstanding Voltage	
Group III	2 Samples
Burst Pressure	
Explosion	If applicable

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SECTION 1300

ACTIVE RF AND MICROWAVE DEVICES

1. SCOPE

This section sets forth detailed requirements for Active RF and Microwave Devices. All of the applicable requirements of Section 1400 apply to diodes and transistors and Section 900 apply for MMIC devices as modified by this section. The Device types covered in this section are:

a. Microwave and RF Field Effect Transistors (FETs) manufactured in technologies including GaAs and related compound semiconductor materials – InP, GaN, SiC, InGaP, AlGaAs, InGaAs, etc.

b. Microwave and RF Bipolar and Heterojunction Bipolar Transistors manufactured in silicon, germanium and SiGe.

c. Microwave and RF Heterojunction Bipolar Transistors (HBTs) manufactured in technologies including GaAs and related compound semiconductor materials – InP, GaN, SiC, InGaP, AlGaAs, InGaAs, etc.

d. Microwave and Millimeter-Wave Monolithic Integrated Circuits (MMICs) manufactured in technologies including GaAs and related compound semiconductor materials – InP, GaN, SiC, InGaP, AlGaAs, InGaAs, etc.

e. Microwave Diodes

   (1) Impact Transit-Time (IMPATT) devices manufactured in silicon and gallium arsenide

   (2) Gunn devices manufactured in gallium arsenide or indium phosphide.

NOTE: Many signal processing devices operate at RF and microwave frequencies within computers and digital and analog control systems. However, the devices considered in this section include those active devices that relate specifically to the use, processing, and control of RF and microwave energy intended for RF radiation.

2. APPLICATION. See Section 1400 for diodes and transistors and Section 900 for MMIC devices.

2.1 Derating. The derating factors shall be as described below.

2.1.1 Derating Factors for Transistors

a. For bipolar silicon transistors, all breakdown voltages shall be derated to 0.75 of the rated value, see Table 1300-1 for other derating factors.

b. Bipolar transistors derating factors shall provide adequate current and voltage derating to preclude secondary breakdowns.

c. Heterojunction Bipolar Transistors, HBTs, shall be derated as shown in Table 1300-1.

d. For field effect transistors, all breakdown voltages shall be derated to a percentage of the rated value. See Table 1300-1 for values and other derating factors.

e. For all transistors, the derating factors shall be as shown in Table 1300-1 depending on the technology used.

Table 1300-1. Derating Factors for Transistors

		JUNCTION TEMPERATURE, (°C) 4/		POWER DISSIPATION, (percent of rated value)		BREAKDOWN VOLTAGE(V)		HIGH POWER (SAFE) OPERATING AREA [1/ (percent of rated value)]	
DEVICE	TECH NOLOGY	NOMINAL	WORST CASE	NOMINAL	WORST CASE	NOMINAL	WORST CASE 5/	NOMINAL	WORST CASE
Bipolar Transistor	Silicon	105	125	60	70	75	75	VCE = 75 IC = 75	VCE = 75 IC = 75
Hetero-junction Bipolar Transistor	Gallium Arsenide 3/	105	125	N/A	N/A	75	75	Current Density = 50 percent	Current Density = 75 percent
Field Effect Transistor	Gallium Arsenide MESFET 2/	105	125	50	60	75	75	N/A	N/A
Field Effect Transistor	Gallium Arsenide HEMT 2/	105	125	50	60	75	75	N/A	N/A
Field Effect Transistor	Gallium Arsenide MHEMT 2/	105	125	50	60	75	75	N/A	N/A
Field Effect Transistor	Gallium Arsenide PHEMT 2/	105	125	50	60	75	75	N/A	N/A
Field Effect Transistor	Silicon Carbide 2/	150	200	60	75	75	80	N/A	N/A
Field Effect Transistor	Gallium Nitride 2/	150	200	60	75	75	80	N/A	N/A
Field Effect Transistor	Indium Phosphide HEMT 2/	105	125	50	60	75	75	N/A	N/A

1/ The safe operating area is a curve or vendor-prepared specification at the stated percent set of rated value curves defining the maximum Energy (Power and time) allowed through a device. For any condition other than DC it assumes a single pulse.

2/ To measure the breakdown voltage set Vgs at a voltage that will result in Ids approximately Imax/2. Increase Vds while monitoring Igs. The on-state breakdown is defined as the Vds that results in a gate current of 1mA per mm of gate periphery

3/ For HBTs, the current collapse contour (specific to device layout and ballasting) is important in determining the safe operating area. Data from Life Tests that are sensitive to current accelerated failure mechanisms with low activation energy can be used to justify higher current density operation.

4/ Thermal impedance shall be determined as described in JEDEC Publication 110, published July 1988. Maximum channel or junction temperature shall be limited to 125°C or to 40°C below the manufacturer's maximum rating, whichever is lower.

5/ Voltage derating factor applies to worst-case combination of DC, AC and transient voltages.

2.1.2 Derating for MMICs.

MMIC derating shall be based on the individual active devices, thermally stressed passive components, capacitors and diodes per Table 1300-2.

Table 1300-2. Derating Factors for MMICS

		TEMPERATURE 1/, °C		POWER DISSIPATION, (percent of worst case)		BREAKDOWN VOLTAGE, V		MULTIPACTION	
ELEMENT	TECHNOLOGY	NOMINAL	WORST CASE	NOMINAL	WORST CASE	NOMINAL	WORST CASE	NOMINAL	WORST CASE
Active Device	See Table 1300-1	See Table 1300-1	See Table 1300-1	See Table 1300-1	See Table 1300-1	See Table 1300-1	See Table 1300-1		
Capacitor	See Section 200	See Section 200	See Section 200	See Section 200	See Section 200	See Section 200	See Section 200		
Resistor	See Section 1100	See Section 1100	See Section 1100	See Section 1100	See Section 1100	See Section 1100	See Section 1100		
Diode	See Section 500 and 510	See Section 500 and 510	See Section 500 and 510	See Section 500 and 510	See Section 500 and 510	See Section 500 and 510	See Section 500 and 510		

1/ Junction temperature for active devices; hottest temperature for other devices.

2.1.3 Microwave Diodes.

(1) Derating for IMPATT diodes shall be as shown in Table 1300-3.

Table 1300-3. Derating Factors for IMPATTS

		JUNCTION TEMPERATURE, °C		OUTPUT POWER (percent of rated value)	
DEVICE	TECHNOLOGY	NOMINAL	WORST CASE	NOMINAL	WORST CASE
IMPATT	Gallium Arsenide	105	140	30	N/A
IMPATT	Silicon	105	140	30	N/A

(2) Derating for Gunn diodes.

Because space usage of these devices has declined and manufacturer interest in this technology is not great, the section on GUNN devices has been tabled. This action does not preclude their use in the future. It is intended to prevent the application of old Gunn technology rules to emergent technology. If new interest in the use of Gunn technology emerges in the future, this area can be revisited.

2.2 Failure Modes and Effect Analysis (FMEA).

The device failure modes and their effects on the system application shall be analyzed and identified to the customer. Table 1300-8 provides a partial list of failure mechanisms and shall be mitigated as a minimum.

3. DESIGN AND CONSTRUCTION

3.1 Requirements. Design and construction shall be in accordance with the requirements of MIL-PRF-19500 JANS for transistors and diodes, MIL-PRF-38535 Class V for MMICs, and the requirements of this section.

a. Interconnects. Monometallic bonding shall be used unless adequate reliability can be demonstrated for other configurations.

b. Hydrogen Poisoning. Manufacturers using hermetically sealed packages containing gallium arsenide and related devices shall demonstrate that the effects of hydrogen poisoning are adequately controlled or non-existent for the duration of the mission (See lessons learned, section 5).

c. Die Passivation. Passivated semiconductors shall be used when available. For applications where unpassivated die must be used, the manufacturer shall demonstrate that the end of life goals can be met with adequate assurance per the specific program requirements.

d. Packaging. Plastic encapsulation shall not be used unless otherwise approved by the PMPCB based on data demonstrating they meet the program end-of-life goals, and the new technology insertion criteria are met with adequate assurance using their plastic packaging (See for example, NASA/TP—2003–212244, PEM-INST-001: Instructions for Plastic Encapsulated Microcircuit (PEM) Selection, Screening, and Qualification.

4. QUALITY ASSURANCE Quality assurance provisions shall be in accordance with the JANS requirements of MIL-PRF-19500 for transistors and diodes, MIL-PRF-38535 Class V for MMICs, Table 1300-4, and the following:

4.1 In-process Controls. In-process controls shall be in accordance with the requirements of MIL-PRF-19500 JAN S for transistors and diodes, and MIL-PRF-38535 Class V for MMICs. As a minimum, areas of concern identified in Tables 1300-5 and 1300-6 shall be addressed.

4.2 Epoxy Materials. Epoxy materials shall meet the requirements of MIL-PRF-19500 JANS for transistors and diodes, and MIL-PRF-38535 Class V for MMICs.

4.3 Screening (100 percent). Screening (100 percent) shall be in accordance with the JAN S Screening requirements of MIL-PRF-19500 for transistors and diodes, MIL-PRF-38535 and paragraph 4.7 for MMICs, as shown in Table 1300-7. The electrical tests shall include the parameters listed in Table 1300-9, the tests listed in Table 1300-11, and all other Group A electrical parameters specified in the detail drawing. Unless otherwise specified, the reject criteria shall be per the detailed specification limit.

4.3.1 IMPATT Diodes. The HTRB for IMPATT devices shall be accomplished by applying a reverse voltage until a 1mA of reverse current is reached instead of the conventional 80 percent of the rated voltage, see Table 1300-7. The Power Burn-in shall be accomplished by applying a reverse voltage to generate a reverse current to reach the maximum specified operating junction temperature.

4.4 Quality Conformance Inspection (OCI). QCI shall be in accordance with the quality conformance tests of MIL-PRF-19500 JAN S for transistors and diodes, and MIL-PRF-38535 and paragraph 4.7 for MMICs. When radiation hardness is specified, wafer lot testing shall be accomplished in accordance with the Group D tests for JAN S per MIL-PRF-19500 and Group E tests of MIL-PRF-38535 for MMICs. For power RF devices, an RF Life test at maximum RF rated Power shall be performed in addition to the Life Test prescribed in MIL-PRF-19500 for JANS and MIL-PRF-38535 for Class V. Table 1300-11 provides a list of recommended tests for RF and Microwave transistors.

4.5 Qualification Tests. Qualification testing shall be in accordance with the requirements of MIL-PRF-19500 for transistors and diodes, and MIL-PRF-38535 for MMICs. All devices used shall have demonstrated MTTF, FIT data and Activation energies derived from accelerated life tests (min 50 percent failure). Table 1300-11 provides a list of recommended tests for RF and Microwave transistors.

4.6 Incoming Inspection DPA. Incoming inspection DPA shall be in accordance with MIL-STD-1580. All metal surfaces shall be verified for the absence of prohibited materials (e.g., pure tin, zinc, or cadmium).

Table 1300-4. Quality Assurance

Wafer Fabrication	Table 1300-5
In-Process Controls: Shall be in accordance with Section 900 for monolithic and Section 1400 for diodes and transistors.	Lot Homogeneity Production Lot Formation Device Serialization Traceability Control Rework Provisions IAW approved procedures Process Controls and their verification and validation elements Screening Tests (100 percent) Lot conformance tests (Destructive and non-destructive tests) Qualification conformance tests (Destructive and non-destructive tests)
Screening (100 percent): Shall be in accordance with Section 900 for monolithic and Section 1400 for diodes and transistors.	Review screening data (attributes and variables). Verify test equipment correlation, repeatability, test windows were met, test conditions, and PDA compliance.
Lot Conformance: Shall be in accordance with Section 900 for monolithic and Section 1400 for diodes and transistors.	Review lot conformance data (attributes and variables)
Supplier DPA: Shall be in accordance with Section 900 for monolithic and Section 1400 for diodes and transistors.	Review supplier DPA and compare to incoming DPA.
Qualification Testing: Shall be in accordance with Section 900 for monolithic and Section 1400 for diodes and transistors. However, FET life testing shall be in accordance with JEDEC JEP118, published January, 1993.	Review qualification data (attributes and variables)
Incoming Inspection DPA: Shall be in accordance with MIL-STD-1580.	Review incoming DPA and compare to supplier DPA.
Sample and Data Retention: Data retention information shall be in accordance with Section 4, General Requirements, of this document.	Maintain samples and data for future use.

4.7 Radiation Hardness. The contractor shall demonstrate that, for the device proposed, the end of life goals will be met with adequate margin per the specific program.

5. LESSONS LEARNED The contractor shall be responsible for ensuring that the problem areas and failure mechanisms described herein are sufficiently addressed in the design, construction, manufacturing and testing of all types of RF devices.

5.1. Design and Application. These areas can determine whether devices can provide reliable performance to end-of-life. Examples of lessons learned in these two areas are the following.

a. Hydrogen Poisoning. Hermetic packages containing materials which involve hydrogen in their manufacture or processing, such as Kovar and electrochemically plated layers, have been found to develop partial pressures of up to 4 percent hydrogen over time due to outgassing from package constituents. This can result in sudden and dramatic changes in the characteristics of GaAs and InP field effect transistors, including PHEMTs and HEMTs, which employ Ti, Pt, or Pd in the gate electrode. Users of III-V device technologies are cautioned to require manufacturers to determine if devices are susceptible to hydrogen poisoning and to take appropriate remedial actions as discussed in references [1-3] below. The use of SiN passivation does not necessarily provide protection.

1) Practical Approaches to Remediation of Hydrogen Poisoning in GaAs Devices, Anthony A. Immorlica Jr., Stephen B. Adams, and Axel R. Reisinger, 1999 GaAs ManTech Conference, Digest of Papers, pp223-226, 1999.

2) http://nppp.jpl.nasa.gov/Mmic/9-VII.pdf A. Immorlica et. al., “Hydrogen Poisoning of GaAs MMICs in Hermetic Packages” a JPL publication

3) http://www.cooksonsemi.com/tech_art/pdfs/Article_Final%20Report.pdf “Sections I - III Hydrogen Effects on GaAs Microwave Semiconductors”, Report sponsored by JEDEC Committee on GaAs, Oct 1997, 41 pages.

4) JPL Publication 96-25 - GaAs MMIC Reliability Assurance Guideline for Space Applications - Chapter 9-VII for a discussion of the issues.

b. IMPATT Circuits. IMPATTs depend on tuned circuits for their attractive qualities for amplifiers and oscillators. However, though their properties are attractive in the appropriate circuit, they can be exposed to electrical overstress if used in an inappropriately tuned circuit. In those circumstances, their reliability is degraded. These devices also present a negative resistance to their power supplies, which can result in bias circuit oscillations if the supply is not properly designed. Such oscillations can affect device operation and life. Parametric oscillations are often present when unwanted device operation occurs. Consequently, the use of appropriate equipment, such as a spectrum analyzer, is recommended to confirm the absence of such oscillations.

c. Wafer Fabrication. This is probably the most critical area that determines the device reliability and performance. Traditionally this area has been downplayed in its importance to the reliability of the end product and consequently controlled by OEMs through a flow chart at best. With the change from “screening of devices to meet quality requirements” to “building of quality into devices” this area becomes the only area that builds quality into the die. Table 1300-5 outlines some of the areas that need specific attention.

NOTE: For most of the older semiconductor device technologies the wafer fabrication process is designed to a nominal level that would produce a range of device types and device families on the same line. It may not be cost effective to target qualification of these processes for only one device type.

d. Assembly. This is an area where the die or chips, processed through wafer fabrication, are put in packages or assembled so that they can be used in systems. These packages and assembly materials used determine in most cases, where the die ratings outperform the package ratings, the final device ratings such as Power Dissipation, Operating and Storage Temperature Ranges, Output Steady State Current, and Thermal Resistance. It is very important that the assembly processes are closely monitored and controlled so that defects are not introduced. MIL-PRF-19500 Appendix D has traditionally provided the guidelines for process controls for semiconductor devices. Table 1300-6 outlines some of the areas that need specific attention.

e. Failure Mechanisms. Table 1300-8 lists failure mechanisms pertinent to solid-state active RF devices. These are mechanisms that have been life limiting in space, as well as other, applications.

Table 1300-5. Wafer Fabrication

Area of Concern	Effect on Performance	Potential Remedy
Wafer Lot formation	Determines die lot performance homogeneity	Use wafers from single batches/ manufacturers.
Wide resistivity and thickness, epi and epi thickness specifications	Allows wide range of electrical characteristics which lead to new device types and or product downgrading.	Use only the devices for which the target specifications of the raw wafers were designed and not the downgraded by products.
High defect count per cm2.	Increase of device to device variation, risk of premature device failure, lower yields.	Lower the acceptable number of defects per cm on the incoming wafers.
High Substrate resistivity	Increased Ohmic contact resistance, resulting in contact failures	Lower the resistivity of starting substrate material
Wafer Fab. Processing	Determines the device performance	
Particle sizes and counts allowable in the clean room.	Depending on the device type, geometry, and technology may impact device reliability and electrical performance. Ionic contamination.	Use positive airflow interlocks and entries, air filters, process only devices for which clean room characteristics were proven to be acceptable.
Water purity and Diffusion cleanness	Potential for ionic contamination. Increases defects in junction formation	Use water filters; test for bacteria, C-V plots.
Rework	Increase of device to device variation, risk of premature device failure, lower yields.	If allowed, verify that the rework did not have adverse effects on device performance in the intended application.
Wafer Fab Location	Use of foundries and other manufacturer's die leads to loss of visibility into wafer fab processing and controls may impact device performance.	Verify the supplier of devices has visibility and control over the wafer fabrication processes, changes, and implementation.
Metallization	Pinholes in top contact metallization and lack of appropriate barrier metal and thickness result in premature device failures	SEM inspection of finished die
Wafer Lot Acceptance	Data provided does not correlate or tie into the wafer fab process controls for dielectric, die, metallization, and passivation layer thickness. Sampling may not be valid.	Ensure wafer lot acceptance provides meaningful data to ascertain the wafer fabrication process and controls.
Radiation Tolerance	Process, design & layout can impact radiation performance.	Use design techniques & process methods that are minimally impacted (affected) by radiation influences.

Table 1300-6. Assembly

Area of Concern	Effect on Performance	Potential Remedy
Die attach is not consistent	Devices fail prematurely due to voids which cause over heating/ or current crowding effects	Implement die-attach monitors such as Transient Thermal Response, DVBE, SOA, and die shear.
Attach materials are not optimized for the package and design application.	Devices fail prematurely due to die-attach degradation when operated under simulated and accelerated application conditions.	Qualify and validate the die-attach process and materials for the intended design application.
Use of Organic material coatings and desiccants.	Devices may intermittently open during temperature transitions while under operation.	Validate and monitor the process through Monitored Temp Cycle and extended life tests.
Multiple Lots formation and loss of Lot Traceability	Increase potential for lot failure due to loss of traceability to individual lots.	Maintain traceability to individual lots.
Rework Provisions	Allowing rework on the production line may not enforce corrective action implementation and promote loose process controls.	If rework was allowed maintain traceability to the reworked portion of the lot for future valuation of adverse rework effects.
Purple Plague (Au wire on Al metallization)	Open circuit.	Validate process through extensive High temperature storage; subject lot to 300°C.
Purple Plague (Al wire on Au metallization	No impact if Gold is thin and the bonding is to the Ni under plate. Otherwise will lead to open circuit.	Validate process through Temperature and Operating Cycles; peel wire to verify bond.
Al wire bonds on Ag metallization.	Open circuit due to operating/ Thermal cycles.	Validate process through Temperature and Operating Cycles;
Improper metallization design	Conductive channels leading to failure by shorts have been observed in IMPATTs	Validate metallization design through adequate time and temperature testing
Particles inside cavity	Potential short due to conductive particles such as die-attach slag, weld splash, etc.	Validate the processes to ensure loose particles are not introduced. Institute PIND. If package too small for PIND to be effective, X-ray the package
Device Irradiation	Targets hFE and V(sat) selection; Devices may return to original values if not annealed properly.	Validate the annealing process and monitor the hFE and V(sat) drift over HTRB, Power Burn-In, and Life tests. For IMPATTs, monitor the reverse breakdown voltage and leakage current.
Gold or gold plated termination embrittlement	Package failures and loss of hermeticity	Have terminations solder dipped before assembly

Table 1300-7. Screening

Screening Test (MIL-PRF-19500 Table IV)	Effect on Performance	Rationale for Test Conditions
Pre-Cap Visual Inspection	Ensures the devices are free of defects prior to encapsulation	Depending on the manufacturer's process controls this may be done on a sample basis.
High Temperature Storage	Some device technologies require this to stabilize the junction characteristics without degradation in reliability	Select the max. device rated temperature storage.
Temperature Cycling	Intended to screen out infant mortality defects due to die attach and other package mismatch defects.	20 cycles were initially established as sufficient to pass the infant mortality stage. Tests should represent application's operating conditions. Devices should reach temperature extremes.
Constant Acceleration	Test designed to stress the wire bonds and die-attach areas.	The G-force level is determined by the package capability and should be above the application requirements.
Transient Thermal Response	Non-destructive die-attach screen for voids outside the process capabilities.	Applicable only to devices with negative voltage temperature coefficient. Limits should track back to maximum RqJC, PD, and or Surge characteristics.
SOA1 (Low Voltage High Current)	Developed to screen out devices with die attach, junction, and or bulk silicon defects.	SOA should not exceed the max. design capability of the die under DC conditions.
SOA2 (High Voltage - Low current)	Developed to screen out devices with junction, and or bulk silicon defects	SOA should not exceed the max. designed capability of the die under DC conditions.
Forward Bias Resistance	Developed to screen out devices with die attach, junction, and or bulk silicon defects.	Forward bias current should not exceed the max. designed capability of the die under DC conditions.
PIND	Developed to screen out devices with loose particles inside the cavity.	Set-up sensitivity, location and tester mounting, shock/ co-shock and vibration levels, and transducer couple medium are important to effective PIND screening.
Pre-Electrical Tests	Electrical parameters (at TA=25°C) established for each technology and device type to be indicative of a good device.	Parameters important to device application operating conditions are tested to validate device reliability over mission duration. These include RF/microwave characteristics as well as DC.
HTRB	Stress test designed to screen out ionic contaminated devices using DC Bias Voltage and Temperature to accelerate the effects. Ions are made mobile through Temperature exposure while the DC Bias Voltage acts as dipole magnet attracting the ions on each positive and negative side of the power supply.	The applied Temperature should be that of the Max. Operating Ambient without heat sink, and the applied voltage should be 80 percent of the rated breakdown voltage of the stressed junction. The magnitude of the exposing temperature and applied bias directly affect the result. Applying AC Voltage or removal of the bias before devices reached approx. 35°C will negate the test.

Table 1300-7 (Continued)

HTRB IMPATT	Stress test designed to screen out ionic contaminated devices using DC Bias Voltage and Temperature to accelerate the effects. Ions are made mobile through Temperature exposure while the DC Bias Voltage acts as dipole magnet attracting the ions on each positive and negative side of the power supply.	The applied Temperature should be that of the Max. Operating Ambient without heat sink, and the applied reverse voltage should correspond to a low level of current, typically 1 mA. The magnitude of the exposing temperature and applied bias directly affect the result.
Post-HTRB electrical tests	Repeat of Pre-HTRB electrical tests to validate that devices did not drift outside the established limits. Test should be performed within 16 hrs of bias removal.	Ionic contamination, if free to move around, will cause a change in the device electrical characteristic. Depending on the contaminant type and level the ions will eventually return to original state.
Percent Defective Allowable (PDA)	Establishes the random failure rate expected during the useful life of the devices.	Typical PDA is 5 percent max. with a one time resubmission if Percent Defective (PD) < 20 percent. Lots failing these criteria should be considered reliability suspect.
Power Burn-In	Test designed to screen out assembly defects.	Test conditions should be established such that device junction temperature is that of the maximum Operating Junction Temperature Ratings. The goal is for the temperature to be high enough to eliminate as many infantile failures as possible without substantially lowering the useful life of the device.
Post Power Burn-In electrical tests	Verify that devices still meet the established electrical characteristics, both DC and RF	Repeat the Post HTRB (Pre Burn-In) electrical tests plus the rest of the DC/RF characteristics including those at high and low temperatures.
Percent Defective Allowable (PDA)	Establishes the random failure rate expected during the useful life of the devices.	Typical PDA is 5 percent max. with a one time resubmission if Percent Defective (PD) < 20 percent. Lots failing these criteria should be considered reliability suspect.
X-Ray	Test was developed for workmanship verification (it does not replace Pre-Cap Visual Inspection). Can identify poor die attach	Criteria and level of inspection is based on the package and defect type. Reduces the occurrence of over-temperature failure mechanisms

Table 1300-8. Failure Mechanisms for Active RF Devices

Failure Mode/ Mechanism	Technology	Ea (eV)	Primary Acceleration factor	Secondary Acceleration Factor	Effect	Acceleration model
Gate sinking	FET	≅1.6	Temperature		Positive shift in VP, reduction in drain current	Arrhenius; Ea~1.6Ev
Ohmic contact degradation.	FET	≅1.4 to 1.8	Temperature	Current Density	Increased on-resistance, decreased drain current	Arrhenius; Ea~1.4-1.8
Ohmic contact degradation	IMPATT	≅1.2 to 1.8	Temperature	Current Density	Increased forward voltage; Increased thermal resistance	Arrhenius; Ea~1.2-1.8
Hot carrier degradation (Power slump)	FET	Negative	Peak channel field (voltage, RF drive)		Reduction in saturated output power	
Hydrogen poisoning	FET		Hydrogen Concentration	Temperature	Reduction in drain current, gain	Inversely proportional to H2 partial pressure; temperature dependence follows Arrhenius model with Ea~0.4 eV
Hydrogen poisoning	IMPATT	~0.4	Hydrogen Concentration	Temperature	Increased reversed leakage	Inversely proportional to H2 partial pressure; temperature dependence follows Arrhenius model with Ea~0.4 eV
Passivation degradation (surface)	FET		Temperature		Increased gate leakage current	
Passivation degradation (surface)	IMPATT		Temperature		Increased reverse leakage current	
Humidity degradation (corrosion)	FET, HBT		High Relative humidity	Temperature, field	Electrical shorts	Peck
Humidity degradation (corrosion)	IMPATT		High Relative humidity	Temperature, field	Reverse leakage current, possibly electrical shorts	
Vbe Shift	HBT		Current density	Temperature		Eyring

TABLE 1300-8 (Continued)

Gradual beta degradation	HBT		Current density	Temperature	Gradual, moderate loss of current gain	Eyring
Sudden beta degradation (REDR)	HBT		Current density	Temperature	Rapid, significant loss of current gain	Eyring
Time dependent dielectric breakdown	MIM cap.		Field	Temperature	Capacitor shorts	
Electrostatic Discharge	FET, HBT, MIM cap		Field	Low humidity	Can cause catastrophic failure or latent damage with subsequent failure	Highly dependent on critical dimensions [e.g., gate length in FETs]
Electromigration	FET, HBT, IMPATT	≅0.5	Current density	Temperature	Opens and/or shorts	Proportional to square of current density; Ea ~.5 eV
Conductive Channel	IMPATT			Temperature	Shorts	

Arrhenius A*exp[Ea/kT]

References

a. Failure Mechanisms on GaAs Integrated Circuits: Electromigration on GaAs, RADC-TR, Contract No. F30602-88-C-0052, July 1990

b. GaAs MMIC Reliability Assurance Guideline for Space Applications, Kayali et al., editors, JPL Publication 96-25, December 1996

c. D. S. Peck, comprehensive Model for Humidity Testing Correlation International Reliability Physics Symposium, 1986, pp. 44 ñ 50

d. O. Hallberg and D. S. Peck, Recent Humidity Accelerations, a Base for Testing Standards Quality and Reliability Engineering International, Vol. 7, pp. 169 ñ 180 (1991)

5.2 Parameters. Some of the parameters that should be measured include those in Table 1300-9.

Table 1300-9. Required Electrical Parameters

Device Type	Parameter	Measurement Point	Measurement Temperature (1)
Small Signal, Switching and General Purpose Transistors, Power Transistors	ICBO	At 80 percent of rated BVCBO	At room, hot, and cold.
	hFE	At specified DC conditions	At room, hot, and cold.
	VBE(sat)	At specified DC conditions	At room, hot, and cold.
	VCE(sat)	At specified DC conditions	At room, hot, and cold.
	IEBO	At 80 percent of rated BVCBO	At room, hot, and cold.
	ICES	At 80 percent of rated BVCEO	At room, hot, and cold.
	BVCBO	At 10x ICBO	At room and cold
	BVCEO	At 10x ICEO	At room and cold
	BVEBO	At 10x IEBO	At room and cold
	ΔICBO, ΔICES, ΔhFE, ΔVBE(sat), ΔVCE(sat)	Post HTRB, Burn-In, Life Tests, Temperature Cycling, Operating Cycling.	Room Temperature
	SOA1 and SOA2	Peak Rated Current At rated DC SOA curve points	Room Temperature

TABLE 1300-9 (Continued)

Device Type	Parameter	Measurement Point	Measurement Temperature (1)
FETS	IGSS	At ±80 percent of rated BVGSS	At room, hot, and cold.
	YFS	At specified DC conditions	At room, hot, and cold.
	IDSS	At 80 percent of rated BVCBO	At room, hot, and cold.
	VGS(off)	At specified current	At room, hot, and cold
	BVDSS	At 10x ICBO	At room and cold
	BVGSS	At 10x IGSS	At room and cold
	ΔIGSS, ΔIDSS, ΔYFS,	Post HTRB, Burn-In, Life Tests, Temperature Cycling, Operating Cycling.	Room Temperature
	SOA1 and SOA2	At rated DC SOA curve points	Room Temperature
	CISS, and COSS,	At specified Voltage and frequency	Room Temperature
	Switching Times	At specified VGS, ID, load resistance, and load capacitance.	Room Temperature

TABLE 1300-9 (Continued)

Device Type	Parameter	Measurement Point	Measurement Temperature (1)
MOSFETS and IGBTS	IGSS	At ±80 percent of rated BVGSS	At room, hot, and cold.
	gFS	At specified DC conditions	At room, hot, and cold.
	VSD	At specified DC conditions	At room, hot, and cold.
	rDS(on)	At specified DC conditions	At room, hot, and cold.
	IDSS	At 80 percent of rated BVCBO	At room, hot, and cold.
	BVDSS	At 10x ICBO	At room and cold
	BVGSS	At 10x IGSS	At room and cold
	ΔIGSS, ΔIDSS, ΔgFS, ΔVSD, ΔrDS(on)	Post HTGB, HTRB, Burn-In, Life Tests, Temperature Cycling, Operating Cycling.	Room Temperature
	SOA1 and SOA2	At rated DC SOA curve points	Room Temperature
	CISS, COSS, CRSS and or	At specified Voltage and frequency	
	Gate Charges and Switching Times	At specified VGS, ID, VDS, load resistance, and load.	Room Temperature

TABLE 1300-9 (Continued)

Device Type	Parameter	Measurement Point	Measurement Temperature (1)
Optically Coupled Isolators	Forward Voltage (Vf)	At rated IF	At room, hot, and cold.
	Leakage Current (IR)	At 80 percent of rated BVR	At room and hot temp.
	Power Output (PO)	At specified DC conditions	Room Temperature
	ΔVF, ΔIR , and ΔPO, ΔICBO, ΔICES, ΔhFE, ΔVBE(sat), ΔVCE(sat)	Post HTRB, Burn-In, Life Tests, Temperature and Operating Cycling	Room Temperature
	ICBO	At 80 percent of rated BVCBO	At room, hot, and cold.
	hFE	At specified DC conditions	At room, hot, and cold.
	VBE(sat)	At specified DC conditions	At room, hot, and cold.
	VCE(sat)	At specified DC conditions	At room, hot, and cold.
	IEBO	At 80 percent of rated BVCBO	At room, hot, and cold.
	ICES	At 80 percent of rated BVCEO	At room, hot, and cold.
	BVCBO	At 10x ICBO	At room and cold
	BVCEO	At 10x ICEO	At room and cold
	BVEBO	At 10x IEBO	At room and cold
	Junction Capacitance CJ	At specified Voltage and frequency	Room Temperature
	Switching Times	At specified VCB, Vf, If, IB, IC, load resistance, and load	Room Temperature
RF Transistors (Bipolar &FET)	Apply all parameters for the Bipolar or FET as applicable and the following:	Same as for Bipolar and FET as applicable. Post HTRB, Burn-In, Life Tests, Temperature and Operating Cycling	Same as for Bipolar and FET as applicable Room temperature.
	IDS', Gm, Pout, NF, Cobo		

6 REGISTERED (RELIABILITY SUSPECT) PMP. Experience has shown the parts or designs listed in Table 1300-10 to have problems meeting mission goals.

Table 1300-10. Registered (Reliability Suspect) PMP

Part Type	Potential Problem	Remedy
Hot welded cans	Short due to conductive particles	100 percent PIND and Weld monitors
Non-glassivated Die	Short due to particles, moisture and contamination	Extended vacuum bake prior to seal, 100 percent PIND, RGA < 5000ppm moisture, 1000 hrs. Life test.
Bimetallic bonds at die	Open due to bond lift.	300C bake, bond pull post IOL and Life Test on samples.
Internal Organic materials	Open due to lifted bonds; Short due to moisture and contamination.	Extended vacuum bake prior to seal, monitored Temp. Cycling, 1000 hrs. Life test with wire pull.
Silver glass/ epoxy die-attach.	Open and or short due to lack of die attach	Mechanical shock, transient thermal response post extended Temperature cycles, IOL, 1000 hrs. Life test.
Mesa Design	Old technology	Use in non-critical applications only.
Alloy junction	Old technology	Use in non-critical applications only.
Plastic encapsulated	Not proven reliable for applications outside commercial and industrial environments.	Conduct extensive qualification for the application prior to use.
Flip chips	Not recommended for high vibration/shock and power management applications.	Provide system level design solutions.
Beam leaded	Not recommended for high vibration/shock applications	Provide system level design solutions.
Third party assembled	Lower reliability	Qualify and validate all processing as necessary to ensure device reliability for the applications.
Chip on board	Not proven reliable for applications outside commercial and industrial environments.	Provide system level design solutions
GaAs MESFETs, HEMTs and PHEMTs in hermetic packages	Parts can be subject to "hydrogen poisoning" causing loss of gain, especially with Platinum or Palladium in the gate electrodes.	Non-hermetic packages or hydrogen getters
GaAs FETs (MESFETs, HEMTs, and PHEMTs)	Parts can be subject to subsurface burnout due to singe event radiation.	Proper shielding
Power GaAs FETs, etc.	Electromigration in gate metal of power FETs is a wearout mechanism.	Proper design

TABLE 1300-10 (Continued)

Part Type	Potential Problem	Remedy
Ceramic substrates used for impedance matching	Can crack and lift due to thermal cycling and mechanical fatigue, especially in multi-watt power devices.	Proper design of ceramics and packaging materials
Nichrome resistors used in MMICs	Can become oxidized and increase in resistance causing circuit failure.	Proper package environmental control or surface stabilization techniques
GaAs transistors	Surface gold metal migration on GaAs can lead to increased leakage currents in GaAs transistors for both FETs and bipolars. This phenomenon is very sensitive to surface cleaning methods and is lot related.	Proper cleaning and passivation
Multiple finger GaAs HBTs	Second breakdown resulting from negative current gain Vs temperature characteristic when used with a high impedance collector supply.	A low impedance (voltage source rather than current source) should be used to avoid this problem.
Metal insulator metal (MIM) capacitors	Susceptible to destructive breakdown, very sensitive to voltage but relatively insensitive to temperature.	Applications shall be properly voltage derated.
GaAs/AlGaAs heterojunction bipolar transistors (HBTs)	Current gain degradation and 1/f noise increase that is strongly accelerated by emitter current density (life ~ J-n, with n=1.5 to 2), but weakly affected by temperature (EA =0.15 to 0.5 eV). Degradation rate is greatly affected by processing	Accelerated life test results at high current from specific wafer lots, including multiple wafer locations, is recommended. InP-based or GaInP/GaAs or SiGe/Si HBT technologies may provide lower risk if they meet performance requirements and are qualified.
MESFET and HEMTs	Susceptible to electrostatic discharge, which has on occasion damaged but not completely destroyed the gate metallization, resulting in a latent failure that is a reliability concern.	ESD precautions shall be followed in handling microwave transistors, especially GaAs parts.
Alloyed Ohmic contacts in GaAs and other III-V devices (MESFETs, HEMTs, HBTs)	Can degrade with a resulting increase in resistance as a result of aging at high temperature. Non-alloyed contacts (refractory metal on heavily doped narrow bandgap material) are less sensitive to this aging phenomenon.	Proper accelerated life testing and screening is needed to avoid this problem.

TABLE 1300-10 (Continued)

Part Type	Potential Problem	Remedy
Power MESFETs and HEMTs	Subject to power slump and "gate lag," a phenomenon that is strongly affected by the surface passivation of the FET.	Proper design of transistor and passivation
GaAs Bipolar Devices	See Note 1/	See Note 1/

1/ AlGaAs/GaAs HBTs are subject to degradation in current gain (Beta) and sometimes increases in turn-on voltage VBE operated in forward active bias. There are several mechanisms that cause degradation, and a number of material growth and wafer processing methods that have been used to control it. An important class of failure mechanisms is enhanced by electron hole recombination that increases the defect density in the base and emitter transition region, especially at the surface of the GaAs (GaAs has a relatively high surface recombination velocity). Defects cause excessive base current which in turn leads to an increase in the defect density causing more base current and increasing degradation of current gain. Since the energy for defect formation comes from electron-hole recombination, this class of failure mechanisms is strongly accelerated by emitter current density (degradation rate is reportedly proportional to J^{a} with α from 1.4 to 2) but may not be greatly accelerated by temperature (Arrhenius activation energy E_A reported from 0.15 eV to 0.45 eV). If the temperature of an accelerated life test is too high and the emitter current density is too low, a temperature-accelerated failure mechanism with a high activation energy is likely to be observed instead of the actual life limiting failure mechanism, and an inaccurate overly optimistic prediction of median time to fail will result.

Other GaAs bipolar devices (tunnel diodes, laser diodes, light emitting diodes, etc.) are also susceptible to degradation (increase in non-ideal forward current) that is accelerated to current density but has a low activation energy.

Operation of an HBT in saturated bias (base-collector junction forward biased) can result in more recombination current than operation with forward active bias.

Qualification of an HBT MMIC should follow Jedec JEP118 concerning accelerated life test conditions, and MIL-PRF-38535 concerning technology characterization vehicle (TCV) and standard evaluation circuit (SEC) design. Emitter current density as well as temperature shall be used to accelerate life in accelerated life tests of the TCV, and the relationship between current density and lifetime limited by Beta degradation or VBE shift shall be determined. The SEC design should include HBTs that operate at the highest emitter current density permitted by the design rules and the SEC should be sensitive to Beta degradation in these high-current HBTs. Since collector current is approximately equal to emitter current in forward active operation, collector current density can be substituted for emitter current density if collector current density is the specified design parameter. As described in JEP118, at least one life test in any three temperature life test used to determine temperature acceleration shall be at an ambient temperature at 200°C or at 50°C above the operating ambient temperature, which ever is lower, and such life test should continue for a minimum of 2000 hours. If a history of reliable operation has not been established through field usage, then a life test duration of greater than 5,000 hours is recommended.

Specifically, programs that identify usage of GaAs HBT devices should review life test data at the piece part level as well as higher levels of assembly for any indications of degradation in current gain. Further, the programs should ensure that the device will meet the operating performance specification in the various circuit applications where HBTs of this type are used. Specifically, it is necessary to ensure that the allowable gain degradation over the design life has adequate end of life margin. For additional information, refer to references (a-e) below.

a. T. Henderson, D. Hill, W. Liu, D. Costa, H.-F Chau, T. S. Kim, A. Kharibzadeh, Characterization of Bias-Stressed Carbon-Doped GaAs/AlGaAs Power Heterojunction Bipolar Transistors, Digest IEEE IEDM (1994).

b. J. J. Liou, Long-Term Base Current Instability: A Major Concer for AlGaAs/GaAs HBT Reliability, Semiconductor Conference, 1998 CAS '98 Proceedings International, Volume: 1 (1998).

c. P. Ma, J. Chen, M. F. Chang, InGaP/GaAs HBT Failure Mechanism Investigation and Reliability Enhancement, Second Report for 19999-2000 for MICRO Project 99-015 (2000).

d. M. Wetzel, M. C. Ho, P. Asbeck, P. Zampardi, C. Chang, C. Farley, M. F. Chang, Modeling Emitter Ledge Behavior in AlGaAs/GaAs HBTs, 1997 GaAs Manufacturing Technology Conference (1997).

e. N. Pan, R. E. Welser, C. R. Lutz, J. Elliot, J. P. Rodrigues, Reliability of AlGaAs and InGaP Heterojunction Bipolar Transistors, IEICE Trans. Electron., Vol. E82-C, No. 11, November 1999.

6.1 Relevant Tests. The following tests have proven to be relevant to RF/Microwave devices.

Table 1300-11. Electrical Test Criteria for Radio Frequency and Microwave Transistors

Bipolar	FET	Tests and Criteria [NOTE: Unless otherwise specified, reject criteria shall be per detail spec limit.]
	X	IGSS, Delta IGSS greater than ± 100 percent of initial value or greater than ± 10 percent of specification limit, whichever is greater
	X	VGS (th), VDS (on), Delta VGS (th), or Delta VDS (on) greater than ± 15 percent of initial value
	X	IDSS, Delta IDSS greater than ± 100 percent of initial value or greater than ± 10 percent of specification limit, whichever is greater
	X	Gm Transductance ± 10 percent
X	X	Pout ± 0.5 dB output power
	X	VP pinch-off voltage ± 15 percent of initial value or 0.1V, whichever is greater, (see Note 1 below)
	X	IDS, specific drain current ± 15 percent
X	X	NF ± 10 percent where appropriate
X		I ebo
X		ICES
X		VCE (sat), VCE (sat) greater than ±50 mVDC
X		hFE, hFF greater than ±15 percent of initial value
X		V(BR) CBO, V(BR) EBO
X		VBF (sat)
X		ICBO, ICBO greater than ± 100 percent of initial value or greater than ± 10 percent of specification limit, whichever is greater
X		Cobo, and Cobo greater than ± 25 percent
X		Each application shall be tested for 100,000 turn-on and turn-off cycles at a rate not to exceed 1000 cycles per second with no power degradation in output

NOTE: This parameter is sensitive to changes in the barrier height of the Schottky barrier formed by the gate and the channel, also to gate sinking and any other phenomenon that is associated with an unstable metal semiconductor junction. So if the pinch off voltage is small because the doping of the channel or the barrier layer thickness or some combination of effects results in a pinch off voltage that is near VGS = 0 V, then using a delta pinch-off voltage criterion that is some fraction of a typical barrier height might be a way around that problem

Modern Devices. The state of the art is continuing to advance in active RF device technology, and understanding of device reliability physics is improving. New devices are, and will be designed. Also, some components do not yet have the level of technological maturity and the extensive experience that is desired for high-reliability applications. For these reasons, potential users of these components should become familiar with the current engineering literature that covers the reliability, failure and degradation mechanisms, life testing, screening and application conditions appropriate for long life of the component technology of interest. This handbook cannot by itself provide adequate information to assure the user of the suitability of a particular technology. There are many resources available to help the user identify all the known risks associated with a candidate device. Regular conferences such as the annual Reliability of Compound Semiconductors (ROCS) Workshop (formerly the GaAs Reliability Workshop), which is sponsored by JEDEC and IEEE and the International Reliability Physics Symposium and the Integrated Reliability Workshop, both sponsored by IEEE address this topic. Journals such as Microelectronics Reliability, published by Elsevier, are helpful. Many journals published by IEE and IEEE, and by the American Institute of Physics and other publishers, cover electron device physics and technology in general but also include important papers devoted to reliability topics. A very important resource is the device manufacturer. Users with high reliability needs are strongly encouraged to contact the manufacturer of the device that they propose to use, and learn what life testing has been done and what the manufacturer recommends concerning high reliability applications.

7. RELIABILITY DETERMINATION/VERIFICATION Parts delivered for this application shall have been determined to have significant assurance of reliability given the following requirements are satisfied:

a. Demonstration of satisfactory lifetime through appropriate testing. This requirement may be reduced by appropriate successful field history.

b. Demonstration of adequate process stability and control.

c. Demonstration of adequate understanding of life-limiting failure mechanisms

d. Demonstration of adequate precautions against low activation energy mechanisms

e. Demonstration of adequate process control.

If these conditions are not met, then the following requirements shall apply.

a. Documented demonstration of satisfactory field performance over a time equal to the mission.

b. Certification that no processes or procedures have changed from those used to produce the devices satisfying the conditions.

8. PROHIBITED PMP shall include:

a. Components using prohibited materials in their construction or finishes. See Section 4, General Requirements, paragraph 4.3.3 of this document.

SECTION 1350

SURFACE ACOUSTICAL WAVE DEVICES

1. SCOPE. All surface acoustical wave devices selected for the system application shall meet the requirements specified herein unless otherwise approved by the program. This section covers the selection of surface acoustical wave devices for space application.

2. REFERENCES.

ANSI/IEEE Std. 176-1987	Institute of Electrical and Electronic Engineers Standard on Piezoelectricity
MIL-STD-1835	Department Of Defense Interface Standard: Electronic Component Case Outlines
MIL-STD-202	Test Methods Standards For Electronics and Electrical Component Parts
MIL-STD-883	Department Of Defense: Test Method Standard; Microcircuits

3. TERMS AND DEFINITIONS.

Quartz — Single crystals approximately described by chemical formula SiO_2, grown by the hydrothermal crystal growth method. The commonly utilized quartz crystal “cut’ for surface acoustical devices is the ST-cut.

4. APPLICATION. The surface acoustical wave device quality and reliability level, critical parameters, and environments for the system application shall be established as defined below. The part application in the system shall form the basis for the technical requirements of each part and critical performance parameters. System application considerations shall include areas such as thermal, mechanical, radiation, derating, End-of-Life limitations, mounting recommendations, and other design considerations necessary to ensure the high reliability of the parts as used in each space vehicle application. The design and construction, and the quality assurance requirements shall be established and documented in specifications to ensure their performance and the necessary quality for space applications.

4.1 Surface Acoustical Wave Device Selection. The selected devices shall have demonstrated the ability through characterization and test to meet the worst-case requirements with adequate margin to compensate for manufacturing variations and End-of-Life considerations. Where adequate assessment data do not exist, the contractor shall define a set of technical requirements detailing how the capability of each selected device will be verified, including the procurement of the devices from qualified sources of supply as determined by the system manufacturer (prime, sub, etc). This shall include the configuration controls that ensure the flight devices are form, fit, function, and performance equivalent to the evaluated parts. The contractor shall ensure that the worst-case conditions include recognition of ground tests performed at the subsequent levels of integration and not only those seen during flight.

4.2 Design Analysis. The surface acoustical wave device design shall make allowances for worst-case variations to compensate for manufacturing variations and End-of-Life parameter limits in the following:

a. Lapping/Polishing surface finish
b. Piezoid Material Thickness
c. Crystal Angle
d. Metallization Thickness
e. Electrical Contact Adhesion
f. Aging Mechanisms

Critical performance parameters shall be identified such that they can be documented in the detailed specifications, including appropriate verification requirements.

4.3 Thermal Analysis. Thermal analysis shall be performed to ensure the selected components are used within the specified temperature limits of the part. If the components are used outside the temperature ranges specified by the component manufacturer, a complete characterization and qualification is required to be performed to ensure the component will meet the mission/application and reliability requirements.

4.4 Mechanical Analysis. Mechanical stress analysis shall be performed to establish the mechanical stress for each part, including those incurred during manufacturing and handling. The mechanical design shall make allowances for worst-case variations in mechanical stress due to temperature excursions, mismatches of thermal coefficient of expansion, mechanical shock, mechanical and acoustical vibration. All surface acoustical wave device mechanical parameters needed in the application shall be verified over the Worst Case Application Conditions plus any additional margin required to compensate for variations in manufacturing and measurement systems.

4.5 Radiation Environment Considerations. The effects of the expected radiation environments on the part performance in the application shall be analyzed to verify the component will operate successfully (See Appendix A). All mitigation strategies shall be documented. The environments addressed shall include the expected natural space environment calculated over the intended life of the mission and any additional nuclear enhanced environment specified in the system specification.

4.6 Design Margin. A design criterion shall be established, documented, and verified for all surface acoustical wave devices to provide adequate performance that meets the application requirements. The design margin shall cover electrical, thermal, mechanical, and radiation performance margin over the worst-case conditions and shall be considered when the surface acoustical wave device absolute maximum ratings and tests are established.

4.7 Parameter Derating. All surface acoustical wave device electrical parameters needed in the design application that could degrade performance shall be identified, rated, and verified over the Rated Device Temperature range. These parameters shall be derated according to the defined criteria for mission life requirements. The contractor shall apply derating criteria based on the system application and specific performance parameters/characteristics of each device.

4.8 Surface Acoustical Wave Device Stress. The surface acoustical wave device derating shall be verified by analysis and/or test (parts stress analysis) in order to show that it meets the established derating criteria. All instances in which the surface acoustical wave device is not used within the established derating limits shall be documented and mitigated. The surface acoustical wave device shall not be stressed beyond the device manufacturer recommended operating limits without a full characterization and qualification.

5. SURFACE ACOUSTICAL WAVE DEVICE DESIGN. The contractor shall ensure that all surface acoustical wave device designs meet the requirements outlined herein.

5.1 Surface Acoustical Wave Device Performance. The electrical, thermal, mechanical, radiation, and reliability performance of the surface acoustical wave device needed for the application shall be verified over the worst-case application environments plus the established design margin.

5.1.1 Surface Acoustical Wave Device Characterization And Qualification. The surface acoustical wave devices shall be fully characterized and qualified for the intended application. All failure modes shall be identified and mitigated. The mitigation shall fully document the tests and results, pass/fail criteria, and design strategies applied as appropriate. Where adequate assessment data do not exist, the contractor shall define and describe how the capability of each selected device will be verified. This shall include the configuration controls that ensure the flight devices are form, fit, function, and performance equivalent to the evaluated parts.

5.1.2 Electrical Parameters. All parameters needed for the application shall be specified and verified over the established rated operating temperature.

5.1.3 Surface Acoustical Wave Device Expected Life. The expected useful life shall be defined and verified for thermal, mechanical, radiation, and operating stress conditions.

6. MANUFACTURING. The contractor shall ensure that all surface acoustical wave devices meet the manufacturing criteria below.

Section 1350 SAW DEVICES

6.1 Wafer Requirements

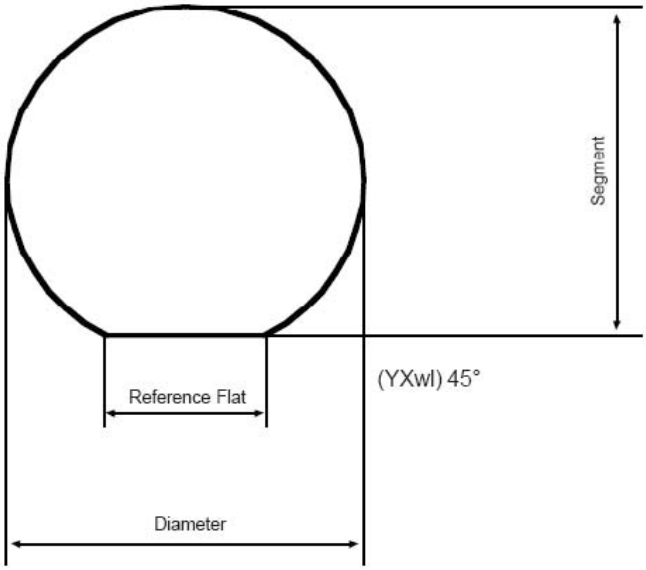

Figure 1350-1. Wafer requirements.

6.1.1 Orientation. Nominal wafer orientation shall be described as per ANSI/IEEE 176-1987 and Figure 1350-1.

6.2 Packaged Surface Acoustical Wave Device Requirements. The following screens shall be required unless alternate practices are specified. If alternate practices are applied, the contactor shall be responsible for ensuring that they are equal to or better than the requirements specified herein and that all the provisions of the practice are met. Alternate requirements shall be approved by PMPCB for the program.

6.2.1 Handling Precautions. ESD handling precautions of surface acoustical wave devices shall be required after the fine pitch geometry metal patterns are applied for all surface acoustical wave devices. $LiNbO_3$ devices, in particular, have a potential structural defect and a metal oxide formation defect which are caused by the application of high voltage at elevated temperature; thus requiring additional handling precautions.

6.2.2 Visual And Mechanical Inspection. 100 percent of the inspection lot shall be screened per MIL-STD-883 Method 2009.

6.2.3 Backfill. Packaged surface acoustical wave devices shall be hermetically sealed in vacuum or backfilled with dry gas. Type of gas, purity, moisture, temperature, and pressure at sealing shall be traceable to the production lot(s).

6.2.4 Solder Seal. Solder sealing shall not be used.

6.2.5 Group 1 Thermal shock. 100 percent of the inspection lot shall be screened per MIL-STD-883 Method 1011, Test Condition A (15 cycles minimum) for space application.

6.2.6 Group 1 Temperature Cycling. 100 percent of the inspection lot shall be screened per MIL-STD-883 Method 1010, 10 cycles minimum, test condition B for space application. This test shall be followed by an external visual and mechanical inspection for any device damage that may have been caused by the Temperature Cycling.

6.2.7 Group 1 Hermetic Seal. 100 percent of the inspection lot shall be screened per MIL-STD-883 Method 1014 Condition A.

6.2.8 Group 1 Visual And Mechanical Inspection. 100 percent of the inspection lot shall be screened per MIL-STD-883 Method 2009.

6.2.9 Group 1 Electrical Inspection. All parameters needed for the application shall be specified and verified over the established rated operating temperature.

6.2.10 Group 1 Internal Visual Inspection. 100 percent of the inspection lot shall be screened per MIL-STD-883 Method 2017, test condition H and MIL-STD-883 Method 2032 Condition M for space application.

6.2.11 Group 1 Nondestructive Bond Pull. 100 percent of the inspection lot shall be screened per MIL-STD-883 Method 2023.

6.2.12 Group 1 Stabilization Bake (prior to sealing). 100 percent of the inspection lot shall be screened per MIL-STD-883 Method 1008, test condition C (150°C, 48 hours minimum) for space application.

6.2.13 Group 2 Mechanical Shock. 100 percent of the inspection lot shall be screened per MIL-STD-883 Method 2002, Condition B.

6.2.14 Group 2 Vibration. 100 percent of the inspection lot shall be screened per MIL-STD-883 Method 2007 Condition A.

6.2.15 Group 2 Constant Acceleration. 100 percent of the inspection lot shall be screened per MIL-STD-883 Method 2001, test condition A, Y_1 plane only, accelerated to 5000g minimum for space application. This test shall be followed by an external visual and mechanical inspection for any device damage that may have been caused by the Constant Acceleration.

6.2.16 Group 2 Hermeticity. Hermetic seal shall be verified in accordance with the requirements of paragraph 6.2.7.

6.2.17 Group 2 External Visual. External visual inspection shall be in accordance with the requirements of paragraph 6.2.2.

6.2.18 Group 2 Electrical Inspection. Electrical performance shall be verified in accordance with the requirements of paragraph 6.2.9.

6.2.19 Group 2 Enclosed Particles (Particle Impact Noise Test, PIND). 100 percent of the inspection lot shall be screened per MIL-STD-883 Method 2020, test condition A. The Failure criteria and screening lot acceptance of the test method shall apply.

6.2.20 Group 2 Serialization. Device serialization is used for tracking and correlating each device with 1) individual Read and Record data values, 2) assembly lots by the device manufacturer and to track where is used in the next higher assembly by the contractor. Each device shall be readily identified by a serial number in accordance with device requirement.

7. REGISTERED (RELIABILITY SUSPECT) PMP. The following surface acoustical wave device types and technologies shall not be used unless approved by the program:

a. Hot welded cans
b. Plastic encapsulated units
c. Packages other than those defined in MIL-STD-1835
d. Programmable units, which do not program with a single pulse
e. Internal organic/polymeric materials (lacquers, varnishes, coatings, adhesives, or greases)
f. Flip chips
g. Beam leaded devices
h. Bimetallic lead bond at die

7.1 PROHIBITED PMP shall include:

a. Nonpassivated devices

b. Internal desiccants

c. Ultrasonically cleaned packaged parts (Latent damage)

d. Devices using prohibited materials in their construction (see Section 4, General Requirements, paragraph 4.3.3 of this document).

8. PROCUREMENT. The contractor shall be responsible for implementing and managing a supplier control program to control, manage, and verify the procurement of surface acoustical wave devices (devices). As a minimum, the contractor shall address supplier selection, supplier verification, supplier corrective action, supplier rating, frequency of supplier audits, etc. In addition, the contractor shall define the incoming receiving inspection performed on received devices including verification, data review and supplier required data items, shelf life control, device storage and kitting, ESD handling, etc.

8.1 Documentation. The surface acoustical wave device design, processing, and testing shall be documented and controlled by the device manufacturer and verified by the procuring/qualifying organization. The manufacturer shall verify device performance, quality, and reliability was not degraded as a result of any subsequent changes from the original qualification.

9. INCOMING INSPECTION DPA. The procuring activity shall verify the workmanship and the internal Design and Construction through a Destructive Physical Analysis (DPA) performed by the procurement activity or at an independent laboratory. All metal surfaces shall be verified for the absence of prohibited materials (e.g., pure tin, zinc, or cadmium).

9.1 Method

9.1.1 External Visual. Visual inspection at 30X minimum magnification shall be conducted with the surface acoustical device being illuminated with a light source of at least 300 foot-candle intensity and a grazing angle of about 20 degrees. Units exhibiting one or more of the following anomalies shall be rejected.

a. Adherent weld splatter exceeding 0.80 millimeters (.031 inches) dimension in any plane.

b. Crack or holes in any welded joint.

c. Indications of corrosion or discoloration on any metal surface.

d. Any dents or protrusions into the case.

e. Cracks, fractures, misalignments, or bends in case-to-lead or case-to-stud joints.

9.1.2 Hermeticity. Hermetic seal shall be verified in accordance with the requirements of paragraph 6.2.7.

9.1.3 Radiographic examination. Radiographic examination shall be performed on all samples in accordance with method 209 of MIL-STD-202.

9.1.4 Particle Impact Noise Detection (PIND). PIND testing shall be performed on all samples in accordance with method 2020 of MIL-STD-883, condition A.

9.1.5 Internal water vapor testing/Residual Gas Analysis (RGA). Internal water vapor /IGA testing shall be performed in accordance with method 1018 of MIL-STD-883. The sample size for this testing shall be one for QPL/QML devices and three for non-QPL devices with zero failures or five devices with a maximum of one failure (3/0, 5/1).

9.1.6 Sample preparation. During the process of opening the surface acoustical device enclosure, care shall be exercised to assure that external liquid, gaseous, particulate, or other types of contamination do not enter the interior areas.

9.1.7 Internal visual. All exposed inner surfaces of the device shall be examined at a minimum magnification of 30X and in accordance with the procedure in paragraph 6.2.2 for configuration compliance and existence of anomalies.

9.2 Data records. DPA findings that deviate from the required configuration or other requirements or exhibit anomalies shall be documented as defects.

9.3 Evaluation criteria. When the DPA is being conducted as a lot conformance test, the associated production lot shall be rejected if the DPA sample parts exhibit any of the following defects:

a. Cracks or holes in the weld contact area where surface acoustical device support members are welded to the holder base terminal pins.

b. Loose, distorted, or broken terminal pins or surface acoustical device mounting supports.

c. Cracks or separation in silver-epoxy electrically conductive bonding cement between the surface acoustical device and support member.

d. Fractures of any size in any location in the surface acoustical device, cracked or flaked edges, and fractures, cracks, peeling, or voids in electrodes.

e. Loose weld spatter, bonding cement, extraneous epoxy, or other foreign matter found on the header, the surface acoustical device and support structure, or inside the cover.

f. Less than 0.125 millimeters (.005 inches) clearance between the surface acoustical device holder cover and the surface acoustical device with its mounting support.

g. Cracks or visible bubbles in glass headers.

h. Chemical corrosion of any metallic surfaces in surface acoustical device can or associated support structure.

i. Surface acoustical device not perpendicular or parallel to the base within the requirements of the procurement requirement.

j. Seal leakage in excess of requirements.

k. Joining of packages by interface that reduces part reliability.

l. Any surface, including cover, exhibiting contamination (adhering particulate, film, flux residue, or other type).

m. Non-uniform quantities of bonding cement at mounting points or bonding cement in areas other than mounting points.

n. Adherent weld splatter with a dimension exceeding 0.80 millimeters (.031 inches) through any plane. Weld splatter shall be considered adherent when it cannot be removed with a gas blow of dry oil-free nitrogen from a 150 kilopascal (22 psi) gauge pressure source.

o. Base terminal and surface acoustical device mounting support exhibiting nicks, misalignment, cuts, cracks, or distortion.

p. Surface acoustical device not centered within ±0.80 millimeters (±.031 inches) in its mounting with respect to the surface acoustical device holder base.

q. Any other defect that reduces part reliability, such as evidence of peeling plateback metallization, voids, or missing metallization on either side of the surface acoustical device.

SECTION 1360

COAXIAL CERAMIC RESONATORS

1. SCOPE. All coaxial ceramic resonators selected for the system application shall meet the requirements specified herein unless otherwise approved by the program. This section covers the selection of coaxial ceramic resonators for space application.

2. REFERENCES

ASTM-B-322	Standard Practice for Cleaning Metals Prior to Electroplating.
ASTM-B-571	Standard Practice for Adhesion of Metallic Coating
IPC/EIA J-STD-002	Solderability Tests For Component Leads, Terminations, Lugs Terminals, and Wires
MIL-STD-1835	Department Of Defense Interface Standard: Electronic Component Case Outlines
MIL-STD-202	Test Methods Standards For Electronics and Electrical Component Parts
MIL-STD-883	Department Of Defense: Test Method Standard; Microcircuits

3. TERMS AND DEFINITIONS

Ceramic Resonator	There are several types of passive resonators commonly referred to as “Ceramic Resonators” that are either piezoid or non-piezoid. Within this document, “Ceramic Resonators” refers to non-piezoelectric short-circuited coaxial ceramic structures that are ¼ or ½ wavelength at some desired resonate frequency of Transverse Electric-Magnetic wave.
Characteristic Impedance	The coaxial resonator impedance is a direct function of its dimensions and of the dielectric material permittivity.
Coupling	The method by which a dielectric resonator is electromagnetically connected to the external environment
Firing	The curing of the ceramic material at elevated temperatures.
Frequency Adjustment	The resonate frequency of ceramic resonators is adjusted by mechanical lapping of the ceramic, or mechanical grinding of metallization.
Green Resonators	The state of coaxial ceramic resonators just prior to the “Firing” manufacturing processing step.
Spurious mode	Output from a dielectric resonator caused by a signal or signals having frequencies other than the resonant frequency desired. The presence of higher resonant modes close to the resonant frequency of the principal mode will interfere with filter or oscillator performance
SRF	Series resonate frequency

4. APPLICATION. The coaxial ceramic resonator quality and reliability level, critical parameters, and environments for the system application shall be established as defined below. The part application in the system shall form the basis for the technical requirements of each part and critical performance parameters. System application considerations shall include areas such as thermal, mechanical, radiation, derating, End-of-Life limitations, mounting recommendations, and other design considerations necessary to ensure the high reliability of the parts as used in each space vehicle application. The design and construction, and the quality assurance requirements shall be established and documented in specifications to ensure their performance and the necessary quality for space applications.

4.1 Coaxial Ceramic Resonator Selection. The selected devices shall have demonstrated the ability through characterization and test to meet the worst-case requirements with adequate margin to compensate for manufacturing variations and End-of-Life considerations. Where adequate assessment data does not exist the contractor shall define a technical set of requirements detailing how the capability of each selected device will be verified, including the procurement of the devices from qualified sources of supply as determined by the system manufacturer (prime, sub, etc.). This shall include the configuration controls that ensure the flight devices are form, fit, function, and performance equivalent to the evaluated parts. The contractor shall ensure that the worst-case conditions include recognition of ground tests performed at the subsequent levels of integration and not only those seen during flight.

4.2 Design Analysis. Circuit design analysis shall be performed to establish the electrical stresses such as voltage, current, power, etc for each part under nominal and worst case conditions. The circuit design shall make allowances for worst-case variations, to compensate for manufacturing variations and End-Of-Life parameter limits in the following: input and output voltages; input and output currents; power dissipation; transient delays; electromagnetic compatibility (EMC). Critical performance parameters shall be identified such that they can be documented in the detailed specifications, including appropriate verification requirements.

4.3 Thermal Analysis. Thermal analysis shall be performed to ensure the selected components are used within the specified temperature limits of the part.

4.4 Mechanical Analysis. Mechanical stress analysis shall be performed to establish the mechanical stress for each part, including those incurred during manufacturing and handling. The mechanical design shall make allowances for worst-case variations in mechanical stress due to temperature excursions, mismatches of thermal coefficient of expansion, mechanical shock, mechanical and acoustical vibration. All coaxial ceramic resonator mechanical parameters needed in the application shall be verified over the Worst Case Application Conditions plus an adequate margin to compensate for variations in manufacturing and measurement systems.

4.5 Radiation Environment Considerations. The effects of the expected radiation environments on the part performance in the application shall be analyzed to verify the component will operate successfully. All mitigation strategies shall be documented. The environments addressed shall include the expected natural space environment calculated over the intended life of the mission and any additional nuclear enhanced environment specified in the system specification.

4.6 Design Margin. A design criterion shall be established, documented, and verified for all coaxial ceramic resonators to provide adequate performance that meets the application requirements. The design margin shall cover electrical, thermal, mechanical, and radiation performance margin over the worst-case conditions and shall be considered when the coaxial ceramic resonator absolute maximum ratings and tests are established.

4.7 Parameter Derating. All coaxial ceramic resonator electrical parameters needed in the design application that could degrade performance shall be identified, rated, and verified over the Rated Device Temperature range. These parameters shall be derated according to the defined criteria for mission life requirements. The contractor shall apply derating criteria based on the system application and specific performance parameters/characteristics of each device.

4.8 Coaxial Ceramic Resonator Stress. The coaxial ceramic resonator derating shall be verified by analysis and or test (parts stress analysis) that it meets the established derating criteria. All instances in which the coaxial ceramic resonator is not used within the established derating limits shall be documented and mitigated. The coaxial ceramic resonator shall not be stressed beyond the device manufacturer recommended operating limits without a full characterization and qualification.

5. COAXIAL CERAMIC RESONATOR DESIGN. The contractor shall ensure that all coaxial ceramic resonator designs meet the requirements outlined herein.

Section 1360 COAXIAL CERMAIC RESONATORS

5.1 Coaxial Ceramic Resonator Performance. The electrical, thermal, mechanical, radiation, and reliability performance of the coaxial ceramic resonator needed for the application shall be verified over the worst-case application environments plus the established design margin.

5.1.1 Coaxial Ceramic Resonator Characterization And Qualification. The coaxial ceramic resonators shall be fully characterized and qualified for the intended application. All failure modes shall be identified and mitigated. The mitigation shall fully document the tests, pass/fail criteria, and design strategies as appropriate. Where adequate assessment data does not exist the contractor shall define and describe how the capability of each selected device will be verified. This shall include the configuration controls that ensure the flight devices are form, fit, function, and performance equivalent to the evaluated parts.

5.1.2 Electrical Parameters. All parameters needed for the application shall be specified and verified over the established rated operating temperature.

5.1.3 Coaxial Ceramic Resonator Expected Life. The coaxial ceramic resonator expected useful life shall be defined and verified for thermal, mechanical, radiation, and operating stress conditions.

6. MANUFACTURING. The contractor shall ensure that all coaxial ceramic resonators meet the manufacturing criteria below.

6.1 Packaged and/or Unpackaged Coaxial ceramic resonator Screening. The following screens shall be required unless alternate practices are specified. If alternate practices are applied, the contactor shall be responsible for ensuring that they are equal to or better than the requirements specified herein and that all the provisions of the practice are met. Alternate requirements shall be approved by PMPCB for the program.

6.1.1 Visual And Mechanical Inspection. The purpose of this screen is to verify that the materials, design, construction, physical dimensions, marking, and workmanship are in accordance with the application requirements.

6.1.1.1 Required Baseline Screening

6.1.1.1.1 Body Dimensions. The contractor shall determine that the physical dimensions are in accordance with the application requirements.

6.1.1.1.2 Diameter and Length of Leads. The diameter and length of leads of leaded coaxial ceramic resonators shall be as per MIL-STD-1276.

6.1.1.1.3 Marking. Coaxial ceramic resonators shall be marked with the PIN and the manufacturer's name, trademark, or code symbol, and lot date code in accordance with MIL-STD-1285. When there is insufficient space on the device package for complete marking, all the required information shall be included on the labels of the container packages.

6.1.1.1.4 Workmanship. Coaxial ceramic resonators shall be processed in a manner as to be uniform in quality and shall be free from holes, fissures, chip, and malformation. The leads shall be unbroken and not crushed or nicked, and the coaxial ceramic resonators shall be free from other defects that will affect life, serviceability, or appearance.

6.1.2 Backfill. Packaged coaxial ceramic resonators shall be hermetically sealed in vacuum or dry backfill gas. Type of gas, purity, moisture, temperature, and pressure at sealing shall be traceable to the production lot(s).

6.1.3 Solder Seal. Solder sealing shall not be used.

6.1.4 Group 1 Thermal Shock.

6.1.4.1 Required Baseline Screening. As a baseline, each sampled coaxial ceramic resonator shall be inspected in accordance with method 107 of MIL-STD-202, Test condition A, upper temperature 125°C.

6.1.4.2 Alternate Screening. As the alternative to paragraph 6.1.4.1, the contractor may verify that the resistance of a coaxial ceramic resonator to exposures at extremes of high and low temperatures, and to the shock of alternate exposures to these extremes meets application requirements.

6.1.5 Group 1 Temperature Cycling.

6.1.5.1 Required Baseline Screening. As a baseline, 100 percent of the inspection lot shall be screened per MIL-STD-883 Method 1010, 10 cycles minimum, test condition B for space application. This test shall be followed by an external visual and mechanical inspection for any device damage that may have been caused by the Temperature Cycling.

6.1.5.2 Alternative Screening. Alternate test methodologies may be used provided test data exist and have been verified to meet or exceed the criteria of paragraph 6.1.5.1.

6.1.6 Group 1 Hermetic Seal.

6.1.6.1 Required Baseline Screening. As a baseline, 100 percent of the inspection lot shall be screened per MIL-STD-883 Method 1014 Condition A.

6.1.6.2 Alternate Screening. Alternate test methodologies may be used provided test data exist and have been verified to meet or exceed the criteria of paragraph 6.1.6.1.

6.1.7 Group 1 Visual And Mechanical Inspection.

6.1.7.1 Baseline. As a baseline , 100 percent of the inspection lot shall be screened per MIL-STD-883 Method 2009.

6.1.7.2 Alternate Screening. As an alternate to paragraph 6.1.7.1, sampled quantities are to be screened as to verify that the materials, design, construction, physical dimensions, marking, and workmanship are in accordance with the application requirements.

6.1.8 Group 1 Electrical Inspection. All parameters needed for the application shall be specified and verified over the established rated operating temperature.

6.1.9 Group 1 Internal Visual Inspection.

6.1.9.1 Required Baseline Screening. As a baseline and unless otherwise required, 100 percent of the inspection lot shall be screened per MIL-STD-883 Method 2013 and MIL-STD-883 Method 2014.

6.1.9.2 Alternative Screening. Alternate test methodologies may be used provided objective evidence exists and is verified to meet or exceed the 6.1.9.1 criteria.

6.1.10 Group 1 Stabilization Bake (prior to sealing).. This method may also be used in a screening sequence or as a preconditioning treatment prior to the conduct of other tests. This test shall not be used to determine device failure rates for other than storage conditions. It may be desirable to make end point and, where applicable, intermediate measurements on a serialized device basis or on the basis of a histogram distribution by total sample in order to increase the sensitivity of the test to parameter degradation or the progression of specific failure mechanisms with time and temperature.

6.1.10.1 Required Baseline Screening. As a baseline and unless otherwise required, 100 percent of the inspection lot shall be screened per MIL-STD-883 Method 1008, test condition C (150°C, 48 hours minimum) for space application.

6.1.10.2 Alternate Screening. As an alternate to 6.1.10.1 this stabilization bake may be preformed in a vacuum chamber at such temperature to allow for a preconditioning treatment prior to the conduct of other tests.

6.1.11 Group 2 Mechanical Shock.

6.1.11.1 Baseline Screening. As a baseline, 100 percent of the inspection lot shall be screened per MIL-STD-883 Method 2002 Test Conditions B.

6.1.11.2 Alternate Screening. Alternate test methodologies may be used provided test data exist and have been verified to meet or exceed the criteria of paragraph 6.1.11.1

6.1.12 Group 2 Vibration.

6.1.12.1 Baseline Screening. As a baseline , 100 percent of the inspection lot shall be screened per MIL-STD-883 Method 2007 Condition A.

6.1.12.2 Alternate Screening. Alternate test methodologies may be used provided test data exist and have been verified to meet or exceed the criteria of paragraph 6.1.12.1

6.1.13 Group 2 Constant Acceleration.

6.1.13.1 Required Baseline Screening. As a baseline 100 percent of the inspection lot shall be screened per MIL-STD-883 Method 2001, Test Condition A, Y_1 plane only, accelerated to 5000g minimum

This test shall be followed by an external visual and mechanical inspection for any device damage that may have been caused by the Constant Acceleration.

6.1.13.2 Alternative Screening. As the alternative to paragraph 6.1.13.1, the contractor shall perform adequate nondestructive screening tests to assure that the device structural and mechanical weaknesses not necessarily detected in shock and vibration tests meet acceptable requirements for space application.

6.1.14 Group 2 Hermeticity. Hermetic seal shall be verfied in accordance with the requirements of paragraph 6.1.6

6.1.15 Group 2 External Visual. External visual shall be performed in accordance with the requirements of paragraph 6.1.7

6.1.16 Electrical Inspection. Electrical performance shall be verified in accordance with the requirements of paragraph 6.1.8

6.1.17 Solderability.

6.1.17.1 Required Baseline Screening. As a baseline and unless otherwise required, 100 percent of the inspection lot shall be screened per MIL-STD-883 Method 2003 for space application.

6.1.17.2 Alternate Screening. As an alternate to paragraph 6.1.17.1 a screening may be offered that is appropriate to inspection of both standard and non-standard parts similar to MIL-STD-883 Method 2003.

6.1.18 Enclosed Particles (Particle Impact Noise Test, PIND).

6.1.18.1 Required Baseline Screening. As a baseline, 100 percent of the inspection lot shall be screened per MIL-STD-883 Method 2020, test condition A. The Failure criteria and screening lot acceptance of the test method shall apply.

6.1.18.2 Alternative Screening. As the alternative to paragraph 6.1.18.1, the contractor may perform adequate nondestructive screening tests to assure that the device unfilled cavity is devoid of loose particles of sufficient mass, size, or material properties as to cause a device failure.

6.1.19 Serialization.

6.1.19.1 Required Baseline Screening. Each device shall be readily identified by a serial number in accordance with device requirement.

6.1.19.2 Alternative Screening. Alternate device tracking may be used provided the same traceability is achieved.

7. PROHIBITED PMP shall include:

a. Ultrasonically cleaned packaged parts

b. Use of prohibited materials in the device construction (see Section 4, General Requirements, paragraph 4.3.3 of this document)

8. PROCUREMENT. The contractor shall be responsible for implementing and managing a supplier control program to control, manage, and verify the procurement of coaxial ceramic resonators (devices). As a minimum, the contractor shall address supplier selection, supplier verification, supplier corrective action, supplier rating, frequency of supplier audits, etc. In addition, the contractor shall define the incoming receiving inspection performed on received devices including verification, data review and supplier required data items, shelf life control, device storage and kitting, ESD handling, etc.

8.1 Documentation. The coaxial ceramic resonator design, processing, and testing shall be documented and controlled by the device manufacturer and verified by the procuring/qualifying organization. The manufacturer shall verify device performance, quality, and reliability are not degraded as a result of any subsequent changes from the original qualification.

9. INCOMING INSPECTION DPA. The procuring activity shall verify the workmanship and the internal Design and Construction through a Destructive Physical Analysis (DPA) performed at an independent laboratory from the device manufacturer. The DPA shall meet MIL-STD-1580 unless otherwise approved by the program.

SECTION 1400

SEMICONDUCTORS

1. SCOPE. All packaged semiconductors selected for the system application shall meet the requirements specified herein, unless otherwise approved by the program. This section covers the selection of semiconductors (diode and transistors) for space application. See section 1300 for RF microwave semiconductors.

2. APPLICATION. The semiconductor diodes specified in this section include rectifiers, zeners, general purpose, PIN diodes, varactors, SCRs, thyristors, schottky, schottky barrier, transient supressors, switching, photo, and other diode types. The semiconductor transistors specified in this section include silicon bipolar, MOSFET, power, JFET, switching, and small signal, and other transistors.

The semiconductors quality and reliability level, critical parameters, and environments for the system application shall be established as defined below. The part application in the system shall form the basis for the technical requirements of each part and critical performance parameters. System application considerations shall include areas such as thermal, mechanical, radiation, derating, End-of-Life limitations, mounting recommendations, and other design considerations necessary to ensure the high reliability of the parts as used in each space vehicle application. The design and construction, and the quality assurance requirements shall be established and documented in specifications to ensure their performance and the necessary quality for space applications.

2.1 Semiconductor Selection. The selected devices shall have demonstrated the ability through characterization and test to meet the worst-case requirements (application and acceptance/qualification) with margin to compensate for manufacturing variations and End-of-Life considerations. The contractor shall ensure that the worst-case conditions include recognition of ground tests performed at the subsequent levels of integration and not only those seen during flight. Where assessment data does not exist the contractor shall define the technical criteria detailing how the capability of each selected device will be verified.

2.2 Semiconductor Standardization. The number of different part types/part numbers and the use of previously qualified or approved part types/part numbers for equivalent applications, shall be optimized.

2.8 Parameter Derating. The parameters shall be derated according to the defined criteria in TABLES 1400-1 and 1400-2 as appropriate.

Table 1400-1. Derating Factors for Transistors

Factor	Bipolar Silicon Transistors		Field-Effect Transistors	
	Nominal	Worst Case	Nominal	Worst Case
Maximum Junction Temperature (ºC)	105	125	105	125
Power Dissipation (percent of Rated Value)	60	70	60	70
Breakdown Voltage (percent of Rated Value)	Low-Power Device	Low-Power Device	75	75
High-Power Device Safe Operating Area 1/ (percent of Rated Value) 1/ (parts shall be used below secondary breakdown)	75 percent Vce 75 percent Ic	75 percent Vce 75 percent Ic	BVDSS BVGSS 75 percent	BVDSS BVGSS 75 percent
Current (percent of rated value)	75 percent	75percent	75 percent	75 percent

Table 1400-2. Derating Factors for Diodes

DIODE TYPE	PARAMETERS DERATED 1/	DERATING FACTOR
Axial Lead (general purpose, switching, small signal)	Reverse Voltage (factor times rated value)	0.75
Rectifiers	Reverse Voltage (factor times rated value)	0.75
	Average Forward Current (factor times rated value)	0.75
	Surge Current (factor times rated value)	0.75
	Power (factor times rated value)	0.65
Transient Suppressor	Transient Current (factor times rated value)	0.75
	Power Dissipation (factor times rated value)	0.75
Varactor	Power (factor times rated value)	0.50
	PIV (factor times rated value)	0.75
	Forward Current (factor times rated value)	0.75
Photo	Current (factor times rated value)	0.50
Current Regulator	Current (factor times rated value)	0.75
	Power (factor times rated value)	0.65
Zener	Current (factor times rated value)	0.75
	Power (factor times rated value)	0.65

1/ The maximum junction temperature shall be +105ºC worst case, for all diodes.

3. SEMICONDUCTOR DESIGN. The semiconductors shall meet the MIL-PRF-19500 requirements for JANS devices. The contractor shall ensure that all semiconductor designs meet these requirements when other than JANS semiconductors are used.

3.1 Semiconductor Performance. The semiconductors electrical, thermal, mechanical, radiation, and reliability performance needed for the application shall be verified over the manufacturer's recommended operating conditions.

3.1.1 Semiconductor Characterization and Qualification. The semiconductors shall be fully characterized and qualified for space application. All failure modes shall be identified and mitigated. The mitigation shall fully document the tests, pass/fail criteria, and design strategies as appropriate. Where assessment data does not exist the contractor shall define and describe how the capability of each selected device will be verified. This shall include the configuration controls that ensure the flight devices are form, fit, function, and performance equivalent to the evaluated parts.

When sampling is conducted to verify lot conformance of a homogeneous* production lot of Space Quality semiconductors, the minimum sample size shall be 5 samples or 2 percent of the lot size, whichever is larger, (unless otherwise directed by the Program). Radiation test sample size shall be in accordance with Appendix A requirements..

Consideration should be made on a case by case basis of reducing the sample size on all extremely expensive, homogeneous lots where surveillance, close vendor history, and good engineering judgment is appropriate. Further consideration should be made of increasing the sample size to random representative sampling with a minimum of 90 percent confidence level for non-homogeneous lots** or lower quality level parts.

* JANS semiconductors from a single JANS inspection lot in compliance with MIL-PRF-19500, controls of bonding, die attach, packaging, etc.

** JANTXV, JANTX and non-homogeneous lots, as well any lot not fully conforming to MIL-PRF-19500 JANS requirements and controls.

3.1.2 Electrical Parameters. All critical parameters needed for the application shall be specified and verified over the established minimum and maximum rated operating temperature range. Parametric and test conditions of automatic test equipment programs shall be verified.

3.1.3 Semiconductor End-of-Life. The End-of-Life values as defined in the General section of this specification shall be defined for all critical parameters.

3.1.4 Die Attach and/or Substrate Attach. The die attach and or substrate attach design shall provide effective electrical and or thermal-mechanical path. The die attach materials used in the design and construction shall be compatible with the metallization backing of the semiconductor die and shall not harden, soften, blister, flow, crack, peel, flake, break, or otherwise lose its electrical or properties during and after exposure to all environmental conditioning and qualification, and next assembly environments.

3.2 Mechanical Parameters

3.2.1 Materials Selection. The Semiconductors Design and Construction shall be such that it will not promote the growth of whiskers (e.g., tin, zinc, etc.), dendrites, “purple plague” or “white plague”, fungus, corrosion, or outgassing.

3.2.1.1 Die Interconnects. The die interconnects materials such as wires, tapes, bumps, columns, etc. shall be compatible with the top metallization of the die. Use of bi-metallic systems, dissimilar metals, or any other systems shall not be allowed unless proven, qualified, and verified not to develop intermetallics or “purple plague” or “white plague”, cause corrosion, flow, crack, peel, lift, flake, or break during and after exposure to all environmental conditioning and qualification, and next assembly environments.

3.2.1.2 Metal Finishes. All metals and metal finishes (internal as well as external) shall be such that it will not promote the growth of whiskers (e.g., tin, zinc, etc.), dendrites, intermetallic formation or fungus, corrosion, . Metal finishes shall not peel or detach during required environmental exposure in test or usage.

3.2.1.3 Package. The package design and construction shall prevent corona discharge and or arcing up to 100000ft altitude, shall not have exposed base material, crack, peel, flake, bend, or break during and after exposure to all environmental conditioning and qualification, and next assembly environments.

4. MANUFACTURING. The contractor shall ensure that all semiconductors meet the manufacturing criteria below. There are two major areas to be covered under the Manufacturing provisions. These are the Wafer Fabrication and Assembly. MIL-PRF-19500 has provided the basis for compliance requirements for the Qualified Military Line (QML) semiconductor device manufacturers and for the Space QML/QPL devices.

4.1 Wafer Fabrication. The Wafer Fabrication shall meet the requirements of MIL-PRF-19500 for JANS, unless otherwise approved by the program.

4.2 Assembly. Semiconductor assembly shall meet the requirements of MIL-PRF-19500 for JANS, specified herein unless otherwise approved by the program.

4.2.1 Lot Formation. The semiconductor manufacturer shall define and control the lot formation to ensure lot homogeneity.

4.2.2 Lot Date Code. Devices shall be assigned a lot Date Code with the week number and the year of device sealing. Devices shall be traceable through the lot date code to the assembly processing and assembly location.

4.2.3 Assembly Documentation. All assembly documentation shall be available for review at the manufacturer.

4.2.4 Facility. Assembly processing shall be in a facility designed and controlled to an appropriate cleanliness level for the technology produced to prevent yield loss and latent defects due to organic and inorganic particle contamination, human handling and Electro Static Discharge (ESD). The manufacturer shall also define the action limits for the environmental control.

4.2.5 Process Controls. The semiconductor manufacturer shall establish in-process controls to verify key areas (wafer mounting and wafer saw, wire bonding, die attach, lid seal, particle detection, lead trimming, final lead finish, etc.) of fabrication steps required to guarantee uniform and homogeneous lot processing. The monitoring process shall document and define: frequency of tests, sample sizes, verification criteria, control and action limits, as well as disposition of the non-conforming devices.

4.2.6 Wire Bonding. SPC shall be established for the wire bonding process. The manufacturer shall define, baseline, monitor, and control the wire bond process. As a minimum, the bonding method, wire size, wire diameter, machine set-up, frequency of set-up verification, the bond strength, bond placement, loop height, bond deformation shall be defined and controlled. All instances of bond lifts, intermetallic and Kirkendall void formation, shall be rejected and investigated to eliminate the possibility of open bond latent failures. The minimum pull strength documented in the MIL-STD-750 TM 2037 shall be used only as a starting point and shall not be used for process control limits.

4.2.7 Die/Substrate Attach. The manufacturer shall baseline, monitor, and control the attach process. The process shall define and document, as a minimum, the attach method, preform size, attach materials composition, equipment set-up, temperature profile, curing time, and inspection criteria. The shear strength documented in the MIL-STD-750 TM 2017 shall be used only as a starting point and shall not be used for process control limits.

4.2.7.1 Lid Seal. The manufacturer shall define, baseline, monitor, and control the lid seal process. The process shall define and document as a minimum, vacuum bake temperature and time, sealing method, sealing environment (Argon, He, etc.) glove box controls (moisture, Oxygen, pressure, air flow), sealing materials composition, equipment set-up, temperature profile, and inspection criteria. The lid seal process shall be controlled such that the sealed components contain less than 5000ppm of moisture, no corrosive gasses and or compounds, and shall not have any loose particles that could bridge or damage the devices.

4.2.7.2 Lead Trim. The manufacturer and/or user shall define, monitor, and control the lead trim process. As a minimum, the tooling and equipment, equipment set-up, and verification process shall be defined and controlled. The devices shall not have exposed metal, damaged lead seals, damaged leads, or otherwise degrade after lead trim operation.

4.2.7.3 Final Lead Finish. The manufacturer shall define, monitor, and control the lead finish process. As a minimum, the tooling and equipment set-up, depth of immersion, verification process for the finish composition, and lead finish method, shall be defined and controlled. The devices shall not be stripped and re-plated unless this process has been qualified for the package and technology proposed.

4.2.7.4 Changes. All changes shall be controlled in accordance with MIL-PRF-19500 for JANS.

5. VERIFICATION AND VALIDATION. The Contractor shall be responsible for ensuring that all Infant Mortality and Early Life Failures are removed from the flight semiconductor population and that all semiconductors perform as specified over the specified operating conditions, temperature environments, radiation environments, and mechanical environments for the required mission life. There are several test methodologies: Stress Tests Driven, Application Specific, and Physics-of-Failure.

5.1 Stress Test Driven. This involves subjecting the lot to a predetermined sequence of accelerated tests, covering the worst-case environments and application conditions plus a predetermined margin, to eliminate the infant mortality and early life failures. These tests are classified as screens, parametric, wear-out, package, environmental, and life tests.

5.1.1 Screening. All semiconductors delivered shall be tested to eliminate manufacturing defects causing infant mortality and early life failures. Unless otherwise approved by the program the semiconductors shall meet the requirements of MIL-PRF-19500. The screening of Schottky barrier power rectifier diodes shall include peak inverse energy test as a lot screening tool for packaged devices.

5.1.2 Qualification and Quality Conformance Inspection. Qualification and Quality Conformance Inspection shall meet MIL-PRF-19500 for JANS.

5.2 Physics-of-Failure. A test or, sequence of tests applied to destruction, which target specific failure mechanisms to model and predict the Time to Failure. In new technologies characterization shall be required to identify failure mechanisms.

5.3 REGISTERED (RELIABILITY SUSPECT) PMP. The following semiconductor types and technologies shall not be used unless approved by the program:

a. Point contact (whisker) devices
b. Internal organic/polymeric materials (lacquers, varnishes, coatings, adhesives, or greases)
c. Flip chips
d. Hot welded cans (Uncontrolled Weld Splatter)
e. Plastic encapsulated units (Uncontrolled materials/processes, and variability of performance due to temperature, bimetallic lead bond at die.)
f. Packages other than those defined in MIL-STD-1835
g. Beam leaded devices (Lack of process control leading to intermittency)
h. Bimetallic lead bond at die (Intermetallic Formation)
i. Silver bump, ramrod construction
j. Programmable units, which do not program with a single pulse (Fusible link process deficiencies)
k. Laser trimmed elements on the chip (debris, resulting in unglassivated die surfaces)

5.4 PROHIBITED PMP shall include:

a. Nonpassivated devices
b. Internal desiccants
c. Ultrasonically cleaned packaged parts (Latent damage)
d. All tin coated or undercoated packages or leads (see section 4, General Requirements, paragraph 4.3.3 of this document)

6. PROCUREMENT. The contractor shall be responsible for implementing and managing a supplier control program to control, manage, and verify the procurement of semiconductor devices from semiconductor Original Equipment Manufacturers (OEM) or their franchised/authorized distributors. As a minimum, the contractor shall address supplier selection, supplier verification, supplier corrective action, supplier rating, frequency of supplier audits, etc. In addition, the contractor shall define the incoming receiving inspection performed on received microcircuits including verification, data review and supplier required data items, shelf life control, microcircuit storage and kitting, ESD handling, etc.

6.1 Incoming Inspection DPA. The procuring activity shall verify the workmanship and the internal design and construction through a destructive physical analysis (DPA) performed by the procurement activity or at an independent laboratory. The DPA shall meet MIL-STD-1580 unless otherwise approved by the program. All metal surfaces shall be verified for the absence of prohibited materials (e.g., pure tin, zinc, or cadmium). DPA sampling should be relative to lot homogeneity as specified in paragraph 3.1.1.

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SECTION 1500

WIRE AND CABLE

1 SCOPE. This section sets forth requirements for wire and cable for use in space vehicles.

2. APPLICATION

2.1 External. Wiring external to electronic enclosures shall be in accordance with the requirements below. Additional guidance may be found in MIL-HDBK-83575.

2.2 Internal. Wiring internal to electronic enclosures should conform to the guidelines provided in MIL-HDBK-454, Guidelines 20 and 69.

2.3 Coaxial Cable. Coaxial cable, both flexible and semi-rigid, shall be in accordance with MIL-DTL-17.

2.4. Derating. Derating factors and wire current shall be based on wire size, on the wire insulation, and the number of wires used in a cable or harness. For harnesses composed of round single conductors in helically wound bundles that operate in an ambient temperature that is less than or equal to 70 C, the current ratings and deratings derived in accordance with MIL-STD-975M shall be used. For harnesses composed of round single conductors in helically wound bundles that operate in an ambient temperature greater than 70C or for harnesses composed of flat conductors and/or ribbon cable, an application specific Thermal Math Model (TMM) approach shall be used to predict the worst-case-wire operating temperature.

3. ELECTRICAL AND HANDLING CONSIDERATIONS – INSULATIONS. The characteristics of the insulation used on wire shall be used in the selection of the proper wire type for each application.

3.1 Ethylene Tetrafluoroethylene (ETFE, Tefzel). Tefzel, a DuPont trade name, is a high temperature resin consisting of 75 percent TFE by weight and its balance of properties is well suited for space vehicle applications. It can withstand an unusual amount of physical abuse during and after installation, and has good electrical characteristics, good thermal and low temperature properties, and chemical inertness. Its high flex life, exceptional impact strength, and service temperature of 150ºC are all superior to Kynar. Its embrittlement temperature is below -100ºC. This insulation meets the outgassing requirements of NASA SP-R-0022. When used in external areas of the spacecraft, this material shall be evaluated for tolerance of the radiation environments.. This wire insulation material is in SAE-AS22759/16, /17, /18, and/19. The equivalent cable specifications are NEMA-WC27500 types TE, TF, TG, and TH.

3.2 Crosslinked ETFE (XL-ETFE). This material is a modified version of ETFE. The improved properties are a higher service temperature of 200ºC and much better resistance to radiation effects. The flexibility, tensile strength, and chemical inertness remain unchanged. This insulation meets the outgassing requirements of NASA SP-R-0022. This material shall be evaluated against radiation environments for use in external areas. This wire insulation material is in SAE-AS22759/32, /33, /34, /35, /41, /42, /43, /44, /45, and /46. The equivalent cable specifications are NEMA-WC27500 types SB, SC, SD, SE, SM, SN, SP, SR, SS, and ST. **Caution**: XLETFE insulated wires and harnesses shall not be stored in sealed containers/bags. The residual carbonyl fluoride in the insulation shall be allowed to outgas freely to prevent its reaction with potentially entrapped moisture in the containers resulting in acidic by-products that can corrode the wires, contacts, connectors, and other conductors.

3.3 Polyvinylidenefluoride (PVF2)(Kynar). Polyvinylidenefluoride, Kynar (a Pennwalt Corporation trade name), is a crystalline, high molecular weight polymer of vinylidenefluoride with excellent abrasion and cut through resistance. Its electrical, thermal, chemical and radiation resistance properties are inferior to Tefzel. Its nominal service temperature is -65ºC to +135ºC. Kynar is typically used as a jacket material over a soft insulation material such as polyalkene, rather than as a primary insulation. The high dielectric constant makes it undesirable as a primary insulation. This insulation material is specified in NEMA-WC27500 jacket symbol 08, 10, 58, and 60. Caution: This material is a reliability suspect PMP item. This material is considered unacceptable for new design and shall only be considered for use on Heritage Programs.

3.4 Polyalkene. This is a dual extrusion of polyolefin and polyvinylidenefluoride (Kynar), with those materials crosslinked for increased heat resistance and greater mechanical strength. Combining these two insulating materials mutually offsets their individual disadvantages. This insulation material exhibits good properties for thinner-walled, lighter weight wire constructions. This insulation meets the outgassing requirements of NASA SP-R-0022. This wire insulation material is in SAE-AS81044/6, /7, /9, /10, /12, and /13. The equivalent cable specifications are NEMA-WC27500 types ME, M, MH, MJ, ML, and MM. However, this material is a reliability suspect PMP item. Caution: This material is considered unacceptable for new design and shall only be considered for use on Heritage Programs.

3.5 FN or HN Grade polyimide (Kapton). Polyimide, Kapton (a DuPont trade name), has excellent thermal and electric properties, and solvent resistance except when exposed to concentrated acids and alkalies. Its nominal service temperature is 200ºC with occasional extended operation to 250ºC. Kapton's main benefit is that it is the lightest weight wire insulation material. This insulation meets the outgassing requirements of NASA SP-R-0022 and the flammability and toxicity requirements of MSFC-HDBK-527. Some of its drawbacks are its inflexibility (stiffness), water absorption, and lack of abrasion and cut through resistance. Under certain specific conditions, this insulation material is more prone than other insulation materials to exhibiting both wet-arc and dry-arc tracking, especially from abrasions and cuts in the insulation material exposing the conductors. An insulation failure that results in a hard short to ground can result in an explosive (rapid) carbonization of the insulation materials. Tests conducted under the auspices of Naval Air Development Center have shown this insulation material to have the potential for causing fires, explosions, and other damage to the host vehicle when an insulation failure results in a hard short to ground. This wire insulation material is in MIL-DTL-81381, all slash sheets. However, the Teflon Kapton Teflon variant is not susceptible to arcing. The equivalent cable specifications are NEMA-WC27500 types MR, MS, MT, MV, MW, MY, NA, NB, NE, NF, NG, NH, MK, and NL. This material is a reliability suspect PMP item.

3.6 T Grade Polyimide (Oasis). Oasis, a DuPont trade name, has improved hydrolytic stability, higher dielectric strength, and somewhat higher density than traditional Kapton. Traditional FEP binders yield a 200ºC thermal limit but new fluoropolymer blends have extended the usable service temperature to 260ºC. There are no existing wire specifications dedicated to utilizing this material exclusively, though it could be substituted for traditional FN Grade Polyimide in a Mil-DTL-81381 type construction, and is often used in conjunction with fluoropolymer tapes in so-called composite insulation designs, such as those in SAE-AS22759/80 thru /92.

3.7 Composite Insulation Constructions (also known as TK or TKT). In response to the perceived dangers of arc-tracking in various types of insulation systems, particularly traditional Kapton insulation, wire insulation designs have been developed that combine discreet fluoropolymer layers with Kapton to produce an insulation construction that is very resistant to arc-tracking initiation and is self-extinguishing should an arc-tracking event be initiated. Other advantages of composite constructions include; very high dielectric strength, greater mechanical toughness at temperature, and high service temperatures of between 200ºC and 260ºC, depending on the construction specifics. The primary disadvantage is higher cost and slightly higher weight due to higher insulation densities and insulation thicknesses typical of these designs. This wire insulation construction is used in SAE-AS22759/80 thru /92.

4. ELECTRICAL AND HANDLING CONSIDERATIONS – CONDUCTORS. The characteristics of the conductors used in the wire or cable shall be considered when selecting the proper wire type for each application. Conductor strands shall be made of soft annealed copper (22 AWG or larger), high strength copper alloy (24 AWG to 28 AWG), or beryllium-copper alloy (30 AWG or smaller). The conductor strands shall be coated with silver or nickel.

4.1 Silver Coated Wire. The upper temperature bounds for this wire are above 150ºC to about 200ºC, which is good for high frequency applications in addition to its higher conductivity. A silver coating shall be used on beryllium copper alloy wire. However, silver-coated copper wire is susceptible to "red plague", a corrosion of the copper conductor when the silver coating thickness is insufficient or porous and the wire is exposed to high humidity. For this reason, a minimum of 40 microinches of silver coating is required.

4.2 Nickel Coated Wire. Solder does not wick under the insulation beyond the joint, leaving a good flexible area. Also, the finish is good for temperatures up to 260ºC. It is acceptable for crimp applications, provided the crimp values in SAE-AS39029 are used.

4.3 Wire and Cable Stripping. The characteristics of the particular wire or cable type as well as the manufacturing through-put requirements shall be considered when determining the optimal wire stripping method and associated tooling.

4.3.1 Laser Stripping. Laser stripping is the preferred method of stripping, particularly for very large (>8AWG wire) or very small (<30AWG wire) wire. Laser stripping has the advantages of being both non-contact, which precludes the possibility of mechanical damage, as well as having higher through-put efficiency. The primary disadvantage of laser stripping is the cost and size of the stripping unit.

4.3.2 Thermal Stripping Thermal stripping of wire insulation is considered an acceptable method and, for some applications, may be the preferred method for certain wire insulation materials, particularly when cost is considered. CAUTION: Thermal stripping of PTFE and possibly other fluoropolymer insulations can produce extremely toxic gases that, if inhaled in sufficient concentrations for long enough, can produce an allergic type sensitization to these materials, thus making future exposure to these materials potentially life-threatening. Ample ventilation shall be provided if thermal stripping of PTFE or other fluoropolymer insulations is performed.

4.3.3 Mechanical Stripping. Mechanical stripping of wire insulation is an acceptable method and, for some applications, may be the preferred method, particularly when cost is considered. Mechanical stripping is most effective, particularly for small gauge wires (28 and 30AWG), if so-called precision mechanical strippers are used. These stripping devices are designed as dedicated tools to be used on a single wire gauge only. Traditional (squeeze handle) mechanical stripping devices may also be used, provided adequate process controls and workmanship precautions are taken to avoid quality problems such as nicks or gouges due to the use of a tool with the incorrect die size.

5. DESIGN AND CONSTRUCTION

5.1 General Purpose Wire. If non-military specification wire is used (wire procured to a contractor prepared specification) the Quality Conformance Inspection tests in accordance with SAE-AS22759 Table VI shall be required.

5.2 General Purpose Cable. If non-military specification cable is used (cable procured to a contractor prepared specification) the Quality Conformance Inspection tests in accordance with NEMA-WC27500 Table VII shall be required.

5.3 Radiation Hardness Assurance. If the wire or cable shall be used in an application where exposure to a total ionizing irradiation of greater than 10^5 rads (Si), the contractor shall develop a test method to ensure that the selected insulation material shall withstand the radiation environment.

6. QUALITY ASSURANCE. Quality assurance requirements shall be in accordance with Section 4, General Requirements, of this document and the requirements of the applicable military specification.

7. REGISTERED (RELIABILITY SUSPECT) PMP shall include:

a. Teflon (PTFE) insulated wire in general, though there are specific configurations and applications where PTFE insulated wires are prohibited (see below).

b. FN or HN Grade polyimide (Kapton) insulated wire

c. Polyalkene insulated wire

d. Polyvinylidenefluoride (PVF2)(Kynar) insulated wire

8. PROHIBITED PMP shall include:

a. MIL-DTL-16878 wire types

b. All Polyvinyl chloride (PVC) insulated wire and cable.

c. SAE-AS22759 wire with only one PTFE layer

d. MIL-W-76 wire

e. Aluminum wire or cable

f. Pure tin plated wire and braid except as allowed by Section 4, General Requirements, paragraph 4.3.3.1 of this document

g. Teflon (PTFE) insulated wires in application which have a high probability of producing cold flow of the insulation.

h. MIL-DTL-81381 wire

i. MIL-W-81044 or SAE-AS81044 wire

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SECTION 1600

PHOTONICS

1. SCOPE. This section sets forth detailed requirements for Electro-Optical devices, modules, and/or submounts intended for use in hi-reliability applications. The requirements set forth here-in are general guidelines to be used in the development of hi-reliability space components. Specific electrical and environmental conditions should be specified in the detailed component specification.

1.1 Applicable documents

MIL-STD-38534	HYBRID MICROCIRCUITS, GENERAL SPECIFICATION FOR
MIL-PRF-85045F	PERFORMANCE SPECIFICATION CABLES, FIBER OPTICS, (METRIC), GENERAL SPECIFICATION FOR
MIL-STD-883	TEST METHOD STANDARD MICROCIRCUITS
MIL-STD-790	STANDARD PRACTICE FOR ESTABLISHED RELIABILITY AND HIGH RELIABILITY QUALIFIED PRODUCTS LIST (QPL) SYSTEMS FOR ELECTRICAL, ELECTRONIC, AND FIBER OPTIC PART SPECIFICATIONS.
MIL-PRF-49291C	FIBER, OPTICAL, (METRIC) GENERAL SPECIFICATION FOR
MIL-M-24791	MODULE, FIBER OPTIC, TRANSMITTER OR RECEIVER,
MIL-HDBK-217	RELIABILITY PREDICTION OF ELECTRONIC EQUIPMENT
MIL-HDBK-340	TEST REQUIREMENTS FOR LAUNCH, UPPER-STAGE, AND SPACE VEHICLES Vol II: Applications Guidelines
Telcordia GR-468	Generic Reliability Assurance Requirements for Optoelectronic Devices Used In Telecommunications Equipment
JPL-D-8545, Rev D	JPL DERATING GUIDELINES

1.2 References

a. Chuck Chalfant, Fred Orlando, Pat Parkerson, “Photonic Packaging for Space Applications”, IMAPS OE Workshop, Oct. 12, 2001. http://www.spacephotonics.com/Resources/Papers/PhotonicsforSpace.pdf

b. Allan Johnston,” Space Radiation Effects in Optoelectronics”, http://www.aero.org/conferences/mrqw/2004papers/Johnston.pdf

2. APPLICATION

2.1 Derating. The instructions for its use are given in Section 4, General Requirements, of this document. General derating criteria is given in the table below. If further derating criteria is required, then the device, module, or submount shall be evaluated on a case-by-case basis based on the application and shall be specified in the detailed specification.

Verification of junction-case thermal resistance by testing and thermal mapping shall be required for new designs, and especially for new technologies.

Table 1600-1. General Derating Criteria

Device Type	Critical Stress Parameter	Derating Factor	Maximum Junction Temperature
Light Emitting Diodes (Tx) & Photo Diodes (Rx)	Power Current	0.50 0.75	1/
Laser Diodes (Tx)	Power	2/	1/

NOTES:

1/ Maximum junction temperatures for optical devices, modules, and/or submounts shall be limited to 95˚C or to 30˚C below the manufacturer's maximum rating, whichever is lower.

2/ Consult the specific program or parts and radiation specialists for derating due to aging and radiation. The specific details should be specified in the associated detail specification.

2.2 End-of-Life Design Limits. The end-of-life design limits shall be evaluated on a program-by-program basis and shall be specified in the detailed device, module, and/or submount specification.

2.3 Reliability. The reliability of electro-optical devices, modules, and/or submounts is continuously improving and evolving. Aside from the requirements outlined in Section 4, General Requirements, of this document and the guidelines and reliability predictions given in MIL-HDBK-217, Telcordia GR-468, and MIL-STD-38534, it is up to the manufacturer to incorporate and set-up a comprehensive component level reliability program to assure the devices, modules, and/or submounts meet mission requirements. The critical nature of many optoelectronic devices, plus the rapid evolution of designs and manufacturing practices, make such a program particularly important. The major elements of a comprehensive reliability program are as follows:

a. Vendor and Device Qualification Programs
b. Lot-to-Lot Quality and Reliability Controls
c. Feedback and Corrective Action Programs
d. Storage and Handling
e. Documentation

The devices used in high reliability systems shall be qualified and purchased only from approved vendors. The reliability and quality of each lot shall be tested and analyzed. Any problem detected in the manufacturing processes or reported from field applications shall be examined and corrected. This information shall be fed back as the input for vendor and device qualification. Devices shall also be stored properly, avoiding excessive heat and humidity. Manufacturers and suppliers shall carefully adhere to Electrostatic Discharge (ESD) precautions which they have tailored for their particular situations. Finally, the reliability assurance program shall be fully documented to ensure consistency and continuity. The elements of a complete reliability assurance program are shown pictorially below.

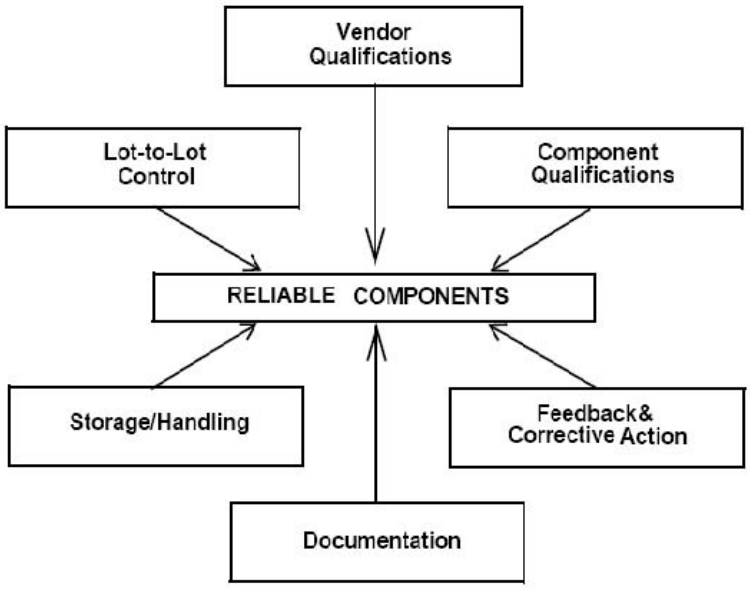

Figure 1600-1. Reliability assurance program elements.

2.3.1 Reliability Analysis and Data. Optoelectronic reliability is a continuously evolving field. For the various component types published industry standards for failure rates, FIT, activation energies and MTBF/MTTF is typically not available. As a general guideline MIL-HDBK-217 can be used. In-depth reliability analysis for the specific device types shall be imposed on the manufacturer. Because of differences in designs and assembly practices reliability shall be specified in the detailed specification. Typically accelerated aging tests are used to gather long-term life test data. Determining a representative failure for devices or demonstrating reliability of devices is subject to the specific conditions. Wear-out failures are activated by temperature and current. Step-stress life testing is typically done at three (3) temperatures specifically chosen to accelerate specific failure mechanisms. The procuring activity shall work closely with the manufacturer to choose the specific test temperatures and operating conditions for the various device types. See Section 6 for additional information on calculating MTBF.

2.3.2 Electrical/Optical Considerations. Unless otherwise indicated in the detailed specification or in the derating sections, the manufacturers recommended operating electrical/optical conditions shall be used. See Table 1600-1 and 1600-4 for specific electrical/optical parameters and de-rating criteria for the specified device types. For additional detailed procedures and test methods for the specific device types see Telcordia GR-468.

2.4 Mounting. General mounting practices shall be in accordance with Appendix A. If further mounting requirements are needed than they shall be addressed in the detailed device, module, and/or submount specification. Unless otherwise specified in the associated detail specification, the fiber pigtail cable shall be perpendicular to the side of the case it exits. The pigtail cable shall be securely affixed to the package and the cavity sealed as required to provide the mechanical strength, hermeticity, and functional performance as specified in the detailed specification.

Note: When soldering GaAs and InP based die temperature shall not exceed 300˚C and 5 minutes.

2.5 Handling. To prevent electrostatic damage to devices, modules, and/or submounts the following shall be required.

2.5.1 Grounding

a. Bonders, pellet pickup tools, table tops, trim and form tools, sealing equipment used in chip or device handling shall be properly grounded.

b. Operator(s) shall be properly grounded.

2.5.2 In-Process Handling.

a. Assemblies or subassemblies of chips and/or devices shall be transported and stored in conductive carriers or containers.

b. All external leads of the assemblies or subassemblies and devices shall be shorted together.

2.5.3 External Bonding Sequences

a. Connect Vcc and Vee shall be connected to the external connections first.

b. Remaining functions may be connected to their external connections in any sequence.

2.5.4 Static Sensitive Devices. . For applications where transients are a potential hazard, a “zap” test wherein a capacitor (100 pf) is charged to at least 400V then discharged through a 1000Ω resistor into the device inputs shall be required on a sample basis. Subsequent to the “zap” test, the devices shall be subjected to the Group A tests. The Sample size shall be two devices per lot. Any failure shall be cause for lot rejection. This test is considered destructive. Caution: This test shall be verified with the manufacturer prior to implementation. NOTE: Semiconductor LED’s/Lasers are based on III-V materials and are ESD rated Class 0. Human Body Model (HBM) ≤250V.

3. DESIGN AND CONSTRUCTION. The design and construction of devices, modules, and/or submounts shall be in accordance with the requirements of MIL-PRF-38534, Class K devices unless otherwise specified in the associated detail specification. For pigtailed devices, the fiber cable shall be in accordance with the requirements of MILPRF-85045F for space applications.

3.1 Hot Welded Cases. Header design shall include an effective weld-splash barrier ring.

3.2 Protective Coating A protective coating of internal elements shall be used, provided adequate thermomechanical evaluation and qualification testing at the part level is performed to assure that no potential failure mechanisms of a more undesirable type have been introduced into the component/module for that application.

4. QUALITY ASSURANCE REQUIREMENTS. Quality assurance provisions shall be in accordance with Section 4, General Requirements, of this document and the requirements outlined in the following paragraphs. Test and inspection methods and criteria shall be in accordance with MIL-PRF-38534, Class K devices unless otherwise specified. Electrical/Optical characteristics for the specific device types shall be in accordance with Telcordia GR-468, unless otherwise specified in the detailed specification. Additional detailed procedures and test methods for the specific device types are also available in Telcordia GR-468.

4.1 Element Evaluation. Element evaluation shall be in accordance with MIL-PRF-38534, Class K devices.

4.2 In-Process Controls. Controls shall be in accordance with the requirements of MIL-PRF-38534, Class K devices as outlined in appendix A.

4.3 Lot-to-Lot Controls. Lot-to-lot controls shall include 100 percent screening in accordance with Table 1600-2. A percent defective allowed (PDA) during screening shall also be specified (to be agreed upon by the manufacturer and its customers but shall not exceed 10 percent). In addition, an ongoing, continuous reliability improvement program shall be implemented by both the equipment supplier and the device manufacturer. See Sections 2.3 herein and Telcordia GR-468 for specific details..

4.4 Screening. Screening requirements shall be in accordance with the 100 percent screening requirements of MIL-PRF-38534, Class K devices and as outlined in Table 1600-2. Electrical/Optical characteristics shall be in accordance with Telcordia GR-468. See Table 1600-4 for specific electrical/optical tests for the specified device types.

4.5 Burn-In. The screening of laser diodes shall include burn-in for all devices. The burn-in shall be chosen to: {a} stabilize the device with respect to its performance and degradation rate and {b} assure that only “good,” stable devices that meet the reliability and quality requirements can successfully pass the burn-in. Specific burn-in conditions should be specified in the associated detail specification.

4.6 Conformance and periodic inspections. Conformance inspection (CI) and periodic inspection (PI) shall be in accordance with MIL-PRF-38534, Class K devices for Group A, Group B, Group C, and Group D tests and as modified herein in Table 1600-3A unless otherwise specified in the associated detail specification. Electrical/Optical characteristics shall be in accordance with Telcordia GR-468. See Table 1600-3 for specific electrical/optical tests for the specified device types.

4.6.1 Qualification Testing Concerns. Qualification testing concerns for specific tests.

4.6.1.1 PIND testing. PIND testing of fiber coupled devices, modules, and/or submounts can sometimes give false negative results. If devices, modules, and/or submounts fail to pass PIND testing then the test set-up may need to be modified. Typically loose or un-secured fiber gives false negative results. The specific conditions and set-up should be specified in the associated detail specification.

4.6.1.2 Steady-State Life Test/HTOL and Burn-in. It should be noted that at this time there are no optoelectronic devices that can meet the +125˚C operational requirement for Hi-Rel applications. The effectiveness of life testing/HTOL and burn-in depends on the operational conditions during HTOL/burn-in, the HTOL/burn-in time, and the acceptable changes in device performance during and after HTOL/burn-in. It is crucial that the operational conditions do no cause early failures or "infant mortality” and are representative of the environmental conditions and application the devices will be subjected to. For devices with internal thermal shutdown, extended exposure at a temperature in excess of the shutdown temperature will not provide a realistic indicator of long-term operating reliability. If internal power dissipation activates a thermal shutdown circuit then the test temperature may be reduced and the test time extended. The operating life test shall be performed at that ambient temperature which will result in a worst case junction temperature at least 5ºC but no more than 10ºC below the minimum junction temperature at which the device would go into thermal shutdown. The procuring activity should work closely with the manufacturer to devise a test plan that will yield useful results. The specific life-test/HTOL and burn-in conditions should be specified in the associated detail specification.

4.6.1.3 Hermeticity. Testing hermeticity is not trivial for these components. The traditional hermeticity definition used for integrated circuits (ICs) as passing the fine leak test may not be applicable, because the fiber coating of the pigtails can absorb and release helium which result in a faulty leakage indication. The moisture content measurement after the damp/heat stress test is a practical and useful test. Special test conditions and/or special testing conditions shall be invoked subject to procuring activity approval.

5. REGISTERED (RELIABILITY SUSPECT) PMP shall include:

a. Hot-welded cases
b. Nonglassivated devices
c. Laser scribed devices
d. Gold-Aluminum bonds

6. PROHIBITED PMP. The following parts, part styles, and part types shall not be used in space hardware.

a. All plastic encapsulated part types
b. Components using prohibited materials in their construction or surface finishes (see Section 4, General Requirements, paragraph 4.3.3 of this document).

7. NOTES

7.1 MTBF Calculation. MTBF requirements for electronic components vary depending on the level of criticality of their application. From a system designer's perspective it is important to have reliable MTBF/FIT data for a component/device to calculate reliability figures for complete systems and assess the requirements for redundancy. Active devices shall undergo accelerated life testing to determine their high temperature operating life, preferably at Tamb (max), with a sufficient sample size to obtain useful MTBF data. Operation at high temperature significantly decreases the expected lifetime of optoelectronic active devices. When testing devices for reliability a suitable test duration and sample size should be determined between the device supplier, equipment manufacturer, and/or the procuring activity. The example in Table 1600-5 shows some MTBF values at a confidence limit of 90 percent for a transceiver with a junction temperature 20°C above ambient and an activation energy of 1.0.

Table 1600-2. Screening Plan for Packaged Devices

Test	Standard	Conditions	Sampling
Preseal bake out (Review needed) 1/	5/	5/	100 percent
Nondestructive bond pull	MIL-STD-883, Method 2023		100 percent
Internal Visual (prior to seal)	MIL-STD-883, Method 2017	3/ 5/	100 percent
Thermal cycling or Thermal shock 2/	MIL-STD-883, Method 1010 or 1011	5/	100 percent
Thermal Vacuum	MIL-HDBK-340	5/	100 percent
Mechanical Shock or Constant Acceleration	MIL-STD-883, Method 2002 or 2001	B, (Y1 direction only) 3000g's, Y1 direction 5/	100 percent
PIND	MIL-STD-883, Method 2020	Condition B 5/	100 percent
Pre-burn-in electrical/optical characteristics	Table 1600 for specific device type	5/	100 percent
Burn-in 4/	MIL-STD-883, Method 1015 and Telcordia GR-468, 4.2.3	5/	100 percent
Post-burn-in electrical/optical characteristics	Table 1600 for specific device type	5/	100 percent
Electrical(High temp/Low Temp) PDA	5/	5/	100 percent
Seal (fine/gross)	MIL-STD-883, Method 1014		100 percent
Radiographic	MIL-STD-883, Method 2012		100 percent
External Visual	MIL-STD-883, Method 2009		100 percent

1/ Potential metallization concerns utilizing Ti/Pt/Au and Ti/Pd/Au contacts. Bake out might be needed before encapsulation.

2/ Thermal Cycling can be performed under vacuum to meet the thermal vacuum requirements.

3/ Confirmation of a "clean" facet (i.e., no metal overhang, chip-outs, debris nearby, solder run-up)

a. Good attachment to the heat sink (and mount)

b. Good wire bonding

c. No evidence of damage from any rework

d. Acceptable shipping or packing materials.

4/ The burn-in shall be chosen to: {a} stabilize the device with respect to its performance and degradation rate and {b} assure that only "good," stable devices that meet the reliability and quality requirements can successfully pass the burn-in.

5/ In accordance with the applicable device specification

Table 1600-3A. Conformance Inspection (CI) and Periodic Inspection (PI) for Packaged Laser Devices

Subgroup	Test	Standard	Conditions	Sampling		
				LTPD	SS	C
1	External Visual	MIL-STD-883, Method 2009		20	11	0
	Electrical at 25˚C	1/		20	11	0
	Mechanical Shock and/or Acceleration	MIL-STD-883, Method 1002 and/or 2001	B, (Y1 direction only) or 3000g's, Y1 direction 5/	20	11	0
	Vibration	MIL-STD-883, Method 2007	20 Hz - 0.125 G2/Hz 50 Hz - 800 Hz - 0.8 G2/Hz 2000 Hz - 0.125 G2/Hz 3 min in each axis. Attenuation rate shall not increase by more than 0.5 dB/km at 1300 nm. Peak acceleration shall be at least 20 g.	20	11	0
	Thermal Vacuum	MIL-HDBK-340	1/	20	11	0
	Thermal Cycling or Thermal Shock	MIL-STD-883, Method 1010 or 1011	1/ 10 cycles 15 cycles	20	11	0
	Seal (fine and gross)	MIL-STD-883, Method 1014		20	11	0
	PIND	MIL-STD-883, Method 2020	A or B 1/	20	11	0
	End-point electrical		1/	20	11	0
	Solderability	MIL-STD-883, Method 2003	Steam aging not required	20	11	0
	Fiber Pull	1/	1 kg; 3 times; 5 sec 2 kg; 3 times; 5 sec	20	11	0
	Visual examination	MIL-STD-883, Method 2009		20	11	0
2	Steady-state life test	MIL-STD-883, Method 1005	1/	20	11	0
	End-point electrical	1/	1/	20	11	0
	High temp storage	1/	1/	20	11	0
	Low temp storage	1/	1/	20	11	0

1/ In accordance with the applicable device specification

Table 1600-3B. Conformance Inspection (CI) and Periodic Inspection (PI) FOR Packaged Laser Devices

Radiation	Type	Standard	Test Levels and Description	LTPD	SS	C
		IEEE-1393 EIA RS455-49	After a total ionizing radiation dose of 10kRad(Si) (dose rate of 1300 Rads/min), the fiber attenuation rate shall not increase by more than 20 dB/km at 1300 nm over the attenuation rate due to other effects. The system shall operate when exposed to a proton flux of 105 protons/sq. cm. 1/	20	11	0
Total Radiation Dose per year	Trapped e- and p+, heavy ion	IEEE-1156.4 IEEE-1393	30 to 200 krad(Si) per year *Special testing required for Military 1/	20	11	0
SEE Rate	Non-Destructive	IEEE-1156.4	<3x10-3 events per day 1/	20	11	0
SEE Rate	Destructive	IEEE-1156.4	<3x10-5 events per day 1/	20	11	0
		IEEE-1156.4 IEEE-1393	30 to 200 krad(Si) per year *Special testing required for Military 1/	20	11	0

1/ In accordance with the applicable device specification.

Table 1600-3C. Special Requirements for Fiber Pigtailed and Connectorized Packaged Devices

Optical Fiber	Description	Standard	Conditions and Requirements	LTPD	SS	C
Type	1300 nm Graded Index Multimode	IEEE-1393 EIA RS-455-58. EIA RS-455-45. EIA RS-455-55.	100 ± 3 microns Core 140 ± 2 microns Cladding 170 ± 2 microns Protective Hermetic Coating when required 1/	20	11	0
Performance		IEEE-1393 EIA RS-455-46 EIA RS-455-50,Pr.A	Cable lengths up to 200 m Attenuation < 5.0 dB/km at 1300 nm Numerical aperture shall be 0.29 ± 0.01 1/	20	11	0
Dispersion limited bandwidth		IEEE-1393 EIA RS-45530,54	400 MHz-Km at 1300 nm 1/	20	11	0
Outgassing		IEEE-1393 ASTM-E-595 SP-R-0022	Maximum volatile condensable material content of 0.10 percent maximum total mass loss of 1.0 percent 1/	20	11	0
Hermeticity		IEEE-1393	Fiber hermetically sealed when required. Hermetic coatings shall be 20 ± 5 nm 1/	20	11	0
Tensile Strength		IEEE-1393 EIA RS-455-31	Proof-tested tensile strength shall be at least 100,000 psi. 1/	20	11	0
Life Requirements	Attenuation Aging Test 0° C to 110ºC, 240 hours	IEEE-1393 MIL-STD-202, method 8 EIA RS-455-31	Shall not increase by more than 0.5 dB at 1300 nm When returned to ambient temperature, the fiber coatings shall not be cracked or melted. No scratches, nicks, or inclusions in the stripped fibers or residual coating material on the stripped fiber which cannot be easily removed. 1/	20	11	0
Attenuation		IEEE-1393	Maximum of 0.75 dB at 1300 nm 1/	20	11	0
Reflection		IEEE-1393	Less than -40 dB 1/	20	11	0
Connector Life	Attenuation & Aging Test 0° C to 110ºC, 240 hours	IEEE-1393 MIL-STD-202, method 8 EIA RS-455-31	Shall not increase by more than 0.25 dB at 1300 nm over losses attributed to the optical fiber or original connection 1/	20	11	0

1/ In accordance with the applicable device specification

Table 1600-4A. Typical Electro/Optical Characterization Tests for Laser Diodes. **

TEST or MEAS.	PARAMETER	SYMBOL	TEST TEMP.
Optical Spectrum	Central or Peak Wavelength	λ_c *or* λ_p	room, min., max.
	Spectral Width	$\Delta\lambda$	room, min., max.
	Secondary Peaks/ Modes	$\lambda_{\pm1}, \lambda_{\pm2}, \ldots$	room, min., max.
Light-Current Curve	Threshold Current or Characteristic Temp.	I_{TH}	room, min., max.
		T_o	room, min., max.
	Optical Power @ I_{TH} or Modulation Depth	P_{TH}	
		ΔP_{mod}	
	L-I Linearity/Kinks	—	room, min. max.
	L-I Satur./Slope Eff.	η	room, min., max.
	F/R Tracking Ratio	$r_{f/r}$	room, min., max.
Voltage-Current Curve	Forward Voltage	V_F	room, min., max.
Modulated Output*	Self-Pulsation	—	room
	Rise & Fall Times	t_r, t_f	room
	Turn-on Delay	t_{on}	room
Far-Field Pattern	FWHM Angles	$\theta_{\|\|}, \theta_{\perp}$	room

* Measured at the maximum modulation rate.

** Refer to Telcordia GR-468 for test specifics.

Table 1600-4B. Typical Electro/Optical Characterization Tests for Laser Modules. *

TEST or MEAS.	PARAMETER	SYMBOL	TEST TEMP.
Optical Spectrum	Central or Peak Wavelength	λ_c orλ_p	room, min., max.
	Spectral Width	$\Delta\lambda$	room, min., max.
	Secondary Peaks/ Modes	$\lambda_{\pm1}$,$\lambda_{\pm2}$, ...	room, min., max.
Light-Current Curve	Threshold Current	I_{TH}	room, min., max.
	Optical Power @ I_{TH}	P_{TH}	room, min., max.
	L-I Linearity/Kinks	—	room, min., max.
	L-I Saturation	—	room, min., max.
	Slope Efficiency	η	room, min., max.
Voltage-Current Curve	Forward Voltage	V_F	room, min., max.
Modulated Output	Self-Pulsations	f_{sp}	room, min., max.
	Modulation Depth	ΔP_{mod}	room, min., max.
	Rise & Fall Times	t_r,t_f	room
	Turn-on Delay	t_{on}	room
	Cutoff Frequency	f_c	room
Monitor Operation	Dark Current	I_d	room, min., max.
	Photocurrent @ $P_{o(max)}$	I_{ph}	room, min., max.
TEC and Temp.Sensor†	TEC Current	I_{TEC}	min., max.
	TEC Voltage	V_{TEC}	min., max.
	Sensor Resistance/	V_{TS}	min., max.
	Sensor Voltage		
Component Alignment	Coupling Efficiency	η_c	room
	F/R Tracking Ratio	$r_{f/r}$	oper. temp. range
	F/R Tracking Error	T_e	oper. temp. range
Thermal Characteristics	Thermal Impedance	θ_{JS}	room

* Refer to Telcordia GR-468 for test specifics.

Table 1600-4VC. Typical Electro/Optical Characterization Tests for Leds. **

TEST or MEAS.	PARAMETER	SYMBOL	TEST TEMP.
Optical Spectrum	Central or Peak Wavelength	λ_c *or* λ_p	room, min., max.
	Spectral Width	$\Delta\lambda$	room, min., max.
Light-Current Curve	Optical Power @ I_{op} *	P_{op}	room, min., max.
Modulated Output	Rise & Fall Times	t_r, t_f	room
	Turn-on Delay	t_{on}	room

* The L-I curve of Edge-Emitting LEDs (ELEDs) should be checked for two additional concerns. They are: [a] lasing threshold, which might occur at low temperatures, and [b] super luminescence.

** Refer to Telcordia GR-468 for test specifics.

Table 1600-4D. Typical Electro/Optical Characterization Tests for Photodiodes. **

TEST or MEASUREMENT	PARAMETER	SYMBOL	TEST TEMP.
Optical Response	Responsivity	*R*	room temp.
	Quantum Effic.	ηQ	room
	Linearity	-	room
	Gain*	*G*	room, min., max.
Electrical Performance	Dark Current	I_d	entire operating range
	Capacitance	C	room
	Cutoff Frequency	f_c	room
	Breakdown Voltage	V_{br}	room, min., max.
	Excess Noise Factor*	F	room

* Only for an avalanche photodiode (APD).

** Refer to Telcordia GR-468 for test specifics.

Table 1600-5. MTBF Calculation Example

Sample Size	Test Duration (hours)	Test T_{amb} (°C)	No of observed failures	MTBF @ 85°C (years)	MTBF @ 55°C (years)	MTBF@ 25°C (years)
10	2000	85	0	1.0	13.9	321.8
20	2000	85	0	2.0	27.9	643.6
20	2000	85	1	1.2	16.4	379.6
20	5000	85	0	5.0	69.7	1609.0
50	2000	85	0	5.0	69.7	1609.0

Using:

$$MTBF = \frac{1}{FR} = \frac{2 \times N \times t \times A_T}{Chi^2(B, c)}$$

Where:

MTBF = Mean Time Before Failure

FR = Failure Rate

N = Sample Size

t = Test Duration (Hours)

A_T = Temperature Acceleration Factor

B = Upper Confidence Limit

c = Number of Observed Failures

Where A- is calculated using:

$$A_T = \exp\left[\frac{Ea}{K} \cdot \left(\frac{1}{T} - \frac{1}{T_{test}}\right)\right]$$

Where:

Ea = Activation Energy

K = Boltzmann's Constant

T = Temperature at which MTBF is calculated

T_{test} = Temperature at which high temperature operating lifetime test is performed

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SECTION 1700

MECHANICAL PIECE PARTS

1. SCOPE. This section sets forth the procurement and testing requirements for mechanical piece parts, such as screws, bolts, washers, nuts, terminals, lugs etc.

2. APPLICATION. Mechanical piece parts shall be procured in accordance with the requirements contained within this section, the part specification and additional requirements contained in applicable sections of this specification. In the event of conflict between requirements, this specification section shall take precedence.

a. For fasteners, ASME ANSI B18.18.1M shall be used. For terminals A-A-59126 shall be used.

b. Class 3 screw threaded products shall be procured and tested to the requirements of NASM1515 and NASM1312

3. SPECIAL CONSIDERATIONS.

3.1 Application Classification. All applications of mechanical piece parts shall be classified according to the potential impact of a part failure on the system. Classification shall result from the application of Failure Modes, Effects, and Criticality Analysis (FMECA). Two application categories shall be identified and are defined as follows:

3.1.1 Mission or Safety Critical. A mechanical piece part failure that can cause severe injury, death, mission degradation, or system loss.

3.1.2 Other. All other failure consequences.

3.2 Mission and Safety Critical Applications.

a. For these applications, the Original Equipment Manufacturer (OEM) or its authorized franchised distributor of the mechanical piece part shall be required to conduct 100 percent screening of all nondestructive quality conformance inspection (QCI) requirements specified. All destructive QCI tests and screens shall be performed on a manufacturing lot sampling basis as specified. The contractor is responsible for ensuring that the seller has performed all required testing required and that the product meets these requirements.

b. Copies of certifications, chemical analyses, and test data shall be provided with the mechanical piece parts.

c. Fasteners shall be from the same manufacturing lot and traceability shall be maintained to that lot.

d. All mechanical piece parts used in Mission or Safety Critical Applications shall be included on the critical items list.

e. Engineering drawings shall identify all “Mission or Safety Critical” mechanical piece part applications.. Physical Configuration Audit (PCA) procedures or other government reviews of engineering drawings shall include verification of this requirement.

3.3 Certifications and Test Data. Procurement specifications shall require that copies of all certifications be provided with the mechanical piece parts.

3.4 Manufacturing Lot Procurement. Mechanical piece parts shall be procured from the original manufacturer or its authorized distributor. Combining of more than one manufacturing lot shall not be allowed on the purchase order. .

3.5 Outgassing. Materials used for self-locking features of fasteners or lubrication shall meet the outgassing requirements specified in Section 4, General Requirements, paragraph 4.1.9 of this document.

4. QUALITY ASSURANCE. Quality assurance requirements shall be in accordance with Section 4, General Requirements, of this document and the requirements of the applicable specifications. In addition, all metal surfaces shall be analytically verified for the absence of prohibited materials (e.g., pure tin, zinc, or cadmium) for each lot of mechanical piece parts.

5. REGISTERED (RELIABILITY SUSPECT) PMP shall include:

a. Lubricants and other materials on fasteners is a concern on systems with critical cleaning requirements. In such instances, fasteners shall be pre-cleaned prior to usage.

b. Cold Flow Susceptibility. Materials that have a potential to cold flow, such as Teflon used to insulate terminals and lugs, shall be evaluated prior to use for cold flow potential in the selected application.

c. Formate Lock washers. Lock washers (either split type or star type) shall not be used as locking devices for space mechanisms. By “biting” into the surface they often damage it and create debris. In addition, their overall effectiveness is poor.

d. For solder-coated/plated washers, solder may creep under a torque load.

6. PROHIBITED PMP shall include:

a. Parts with prohibited materials in their construction or finishes (See Section 4, General Requirements, paragraph 4.3.3 of this document).

SECTION 2000

MATERIALS REQUIREMENTS

1. SCOPE. This section sets forth the common requirements for materials used in mechanical applications. Materials fall into three categories: Metals, Polymerics and Ceramics

2. APPLICATION. The selection of all materials for space applications shall be made such that the system will operate in the specified environments without maintenance over a specified mission lifetime. Therefore, the selection of suitable materials and appropriate processing methods and protective treatments shall be made such that design allowables are adequate for the system's anticipated worst-case environment.

3. SPECIAL CONSIDERATIONS. All materials used shall meet the outgassing and hazardous property requirements specified in Section 4, General Requirements, paragraphs 4.1.9 and 4.3.2 of this document, respectively.

4. PROHIBITED PMP shall include:

a. Items plated with cadmium and zinc shall not be used on space flight items. Alloys and brazing materials containing these metals shall not be used without overplating unless analysis demonstrates that in the application sublimation will not occur. These materials shall not be used in test and ground support equipment within the thermal vacuum chambers used for testing flight hardware: (See Section 4, General Requirements, paragraph 4.3.3 of this document)

b. Lead-free (less than 3 percent lead) tin coated items whether on external or internal surfaces shall not be used. (See Section 4, General Requirements, paragraph 4.3.3 of this document) . Exceptions are gold-tin, tin-silver (Sn96), or tin-antimony (Sn95Sb5) bulk solders.

c. Lead free solders (See Section 4, General Requirements, paragraph 4.3.3 of this document)

d. Alloys or compounds containing mercury

e. Corrosive (acetic acid evolving) silicone sealants, adhesives, or coatings

f. Chlorinated Fluorocarbons (CFCs) or other Ozone Depleting Compounds (ODCs) as mandated by federal or state regulations.

g. Aluminum alloys with a stress corrosion threshold in any grain direction less than 25 ksi.

h. Asbestos-containing materials

i. Silicone grease used as a thermal couplant

j. PTFE and PFE (Telfon) in applications under pressure, torque or compression, in which creep or cold flow will occur.

k. Unplated brass

SECTION 2100

METALS

1. SCOPE. This section sets forth the common requirements for the use of metals.

2. APPLICATION. MIL-HDBK-5J should be used as the basic document for defining strength allowables and other mechanical and physical properties for metallic materials. When data is not contained in MIL-HDBK-5J, contractor allowables developed in accordance with MIL-HDBK-5J may be used.

3. SPECIAL CONSIDERATIONS.

3.1 Forgings.

3.1.1 Forging Design. Forgings shall be produced in accordance with SAE-AMS-F-7190 for steel, SAE-AMS-A-22771 or SAE-AMS-QQ-A-367 for aluminum alloys and MIL-T-9047(1) (CANCELED) for titanium alloys. Recognized industrial association or contractor specifications shall be used for alloys not covered by the above specifications. . Because mechanical properties are maximized in the direction of material flow during forging, forging techniques shall be used that produce an internal grain flow pattern such that the direction of flow in all stressed areas is essentially parallel to the principal tensile stresses. The grain flow pattern shall be free from reentrant and sharply folded flow lines. After the forging parameters, including degree of working, are established, the first production forging shall be sectioned to show the grain flow patterns and to determine mechanical properties and fracture toughness values at control areas. The procedure shall be repeated after any significant change in the forging parameters. The information gained from this effort shall be utilized to redesign the forging as necessary. Test data, material samples, and results of the tests on redesign, shall be retained by the contractor for the life of the program.

3.1.2 Forging Surfaces. Surfaces of structural forgings in regions identified by analyses as fatigue critical or in regions of major attachment shall be shot peened or placed in compression by other means demonstrated to be equivalent. Those areas of forgings requiring lapped, honed, or polished surface finishes for functional purposes shall be shot peened prior to surface finishing operations.

3.1.3 Residual Stresses. Residual stresses are normally induced into manufactured parts as a result of forging, machining, heat-treating, welding, special metal removal processes, and assembly. Even with in-process controls to minimize the potential buildup of residual stresses, the final production parts will usually contain some residual stresses. These stresses may be harmful in structural applications when the part is subjected to fatigue and loading, additive operation stresses, or corrosive environments. Therefore, residual stresses in finished structural parts shall be eliminated or minimized by appropriate heat treatments, such as annealing and stress relieving, and process optimization.

3.2 Stress Corrosion Considerations. Alloys and heat treatments, which result in a high resistance to stress corrosion cracking as defined in MSFC-STD-3029 Table 1, shall be utilized in all structural, load- carrying applications. Materials that are subject to stress corrosion cracking conditions and do not have a high resistance to stress corrosion cracking as defined in MSFC-STD-3029 Table 1. shall be considered a non-standard material and shall require program PMPCB approval..

3.3 Castings. Castings shall be classified and inspected in accordance with MIL-STD-2175A. Structural castings shall be procured to guaranteed properties, premium quality specifications including MIL-A-21180(D), SAE-AMS-5343, or other document in accordance with the contractor's approved PMP control plan.

3.4 Protective Finishes. The requirements for and application of protective finishes, including cleaning prior to application, shall be in accordance with MSFC-SPEC-250, with the exception of zinc, cadmium, and pure tin finishes which are prohibited. (See Section 4, General Requirements, paragraph 4.3.3 of this document).

3.5 Dissimilar Metals. Use of dissimilar metals in contact, as defined by MIL-STD-889, shall be limited to applications where similar metals cannot be used due to design requirements. When use is unavoidable, metals shall be protected against galvanic corrosion by a method listed in MIL-STD-889. Composite materials containing graphite fibers shall be treated as graphite in MIL-STD-889.

SECTION 2110

ALUMINUM AND ALUMINUM ALLOYS

1. SCOPE. This section sets forth the common requirements for the use of aluminum and its alloys.

2. APPLICATION. In structural applications requiring the selection of aluminum alloys, maximum use shall be made of those alloys, heat treatments and coatings which minimize susceptibility to general corrosion, pitting, intergranular and stress corrosion and maximize fracture toughness.

3. SPECIAL CONSIDERATIONS

3.1 Aluminum Heat Treatment. Heat treatment of wrought aluminum alloys shall meet the requirements of MIL-H-6088G (S/S by SAE-AMS-H-6088, 9/26/97), and the heat treatment of wrought aluminum alloy parts shall meet the requirements of SAE-AMS-2770. Heat treatments not included in above specifications may be used if sufficient test data is available to prove that the specific heat treatment improves the mechanical and/or physical properties of the specific aluminum alloys without altering susceptibility to degradation. This data shall be retained by the contractor and is subject to review.

3.2 Aluminum Forming and Straightening. Forming and straightening operations shall be limited to processes that do not result in stress corrosion sensitivity of the part, or to detrimental residual stresses, or losses in mechanical properties, or fracture toughness on structurally critical parts. The contractor shall maintain controls and data to support the use of the forming and straightening processes. These controls and data are subject to review.

3.3 Stress Corrosion Cracking. Alloys and heat treatments, which result in a high resistance to stress corrosion cracking as defined in MSFC-STD-3029 Table 1, shall be utilized in all structural, load- carrying applications. Materials that are subject to stress corrosion cracking conditions and do not have a high resistance to stress corrosion cracking as defined in MSFC-STD-3029 Table 1. shall be considered a non-standard material and shall require program PMPCB approval

4. PROHIBITED PMP shall include:

a. Alloys with a stress corrosion threshold in any grain direction less than 25 ksi
b. Aluminum alloy 5083-H32, where temperature > 150° F
c. Aluminum alloy 5083-H38, where temperature > 150° F
d. Aluminum alloy 5086-H34, where temperature > 150° F
e. Aluminum alloy 5086-H38, where temperature > 150° F
f. Aluminum alloy 5456-H32, where temperature > 150° F
g. Aluminum alloy 5456-H38, where temperature > 150° F
h. Since mercury and mercuric compounds can cause accelerated stress cracking of aluminum alloys, their use is prohibited in conjunction with the manufacturing, storage, or use of aluminum alloys.

SECTION 2120

BERYLLIUM

1. SCOPE. This section sets forth the common requirements for the use of beryllium and its alloys.

2. APPLICATION. Beryllium and beryllium alloys, such as AlBeMet, shall be restricted to applications in which their properties offer definite performance and cost advantages over other materials. Additionally, beryllium parts shall be tested under simulated service conditions and exhibit mission life, including any expected corrosive environments, prior to Critical Design Review. This restriction applies to alloys with greater than 5 percent beryllium.

3. SPECIAL CONSIDERATIONS

3.1 Toxicity. The toxicity of beryllium dust and fumes is a critical problem and minimization of exposure shall be a goal during fabrication, assembly, installation, and usage of beryllium parts.

3.2 Storage. Beryllium products that may generate dust or particles shall be stored in closed containers, which shall only be opened in a controlled environment.

3.3 Design. Design of beryllium parts shall include consideration of its low impact resistance, and notch sensitivity, particularly at low temperatures, and its directional material properties and sensitivity to surface finish requirements.

SECTION 2130

MAGNESIUM

1. SCOPE. This section sets forth the requirements for the use of magnesium and its alloys.

2. APPLICATION. Magnesium alloys shall not be used for structural applications, in any area subject to wear, abrasion, erosion or where fluid entrapment is possible. Magnesium alloys shall not be used except in areas where exposure to corrosive environments is prevented and protection systems are maintained.

3. SPECIAL CONSIDERATIONS

3.1 Stress Corrosion Cracking. Magnesium and magnesium alloy products shall be treated after forming to avoid stress corrosion cracking.

3.2 Corrosion. Magnesium and magnesium alloy products shall not be used without a corrosion protection system designed for its mission, manufacturing and storage environment.

3.3 Dissimilar Metals. Dissimilar metal protection shall be used regardless of the environmental controls.

SECTION 2140

STEELS

1. SCOPE. This section sets forth the requirements for the use of steels.

2. APPLICATION. High strength steels heat-treated at or above 200 ksi Ultimate Tensile Strength (UTS) shall not be used unless approved by the PMPCB. These steels are subject to delayed failure mechanisms, such as those caused by contamination elements introduced during fabrication processing. Also, the effect of low temperature on reducing high strength steel toughness and ductility shall be considered in the design and application of these steels.

3. SPECIAL CONSIDERATIONS

3.1 Heat Treatment of Steels. Steel parts shall be heat-treated as specified to meet the requirements of MIL-H-6875H. All high strength steel parts heat-treated at or above 180 ksi UTS shall include appropriate test coupons or specimens, which shall accompany the part through the entire fabrication cycle to assure that desired properties are obtained. Heat treatments not included in MIL-H-6875H may be used if test data demonstrates that the heat treatment improves the mechanical and/or physical properties of the specific steel without altering susceptibility to degradation. This data shall be retained by the contractor and made available upon request.

3.2 Drilling and Machining of High Strength Steels. The drilling of holes, including beveling and spot facing, in martensitic steel hardened to 180 ksi UTS or above shall be avoided. When such drilling or machining is unavoidable, carbide tipped tooling and other techniques necessary to avoid formation of untempered martensite shall be used. Microhardness and metallurgical examination of test specimens typical of the part shall be used to determine if martensite areas are formed as a result of drilling or machining operations. The surface roughness of finished holes shall not be greater than 63 RHR, and the ends of the holes shall be deburred by a method which has been demonstrated not to cause untempered martensite. (An etching procedure may be used as an alternate to metallurgical testing to determine the presence of untempered martensite.)

3.3 Grinding of High Strength Steels. Grinding of martensitic steels hardened to 180 ksi UTS and above shall be performed in accordance with MIL-STD-866. Grinding of chromium plated martensitic steels hardened to 180 ksi UTS and above shall also be performed in accordance with MIL-STD-866.

3.4 Corrosion Resistant steels

3.4.1 Austenitic Stainless Steels. Free machining stainless steels intended for fatigue critical applications shall not be performed. Sulfur or selenium additions improve machinability but lower fatigue life.

3.4.2 Precipitation Hardened Stainless Steels. These steels shall be aged at temperatures not less that 1000ºF. Exception is made for castings which may be aged at 935ºF ±15ºF, fasteners which may be used in the H950 condition and springs which have optimum properties at the CH 900 condition.

3.5 Forming or Straightening of Steel Parts. Procedures and tooling shall be used to minimize warping during heat treatment of steel parts. Steel parts shall be formed or straightened as follows:

a. Parts hardened up to 165 ksi UTS may be straightened at room temperature.

b. Parts hardened from 165 to 200 ksi UTS may be straightened at room temperature provided they are given a stress relieving heat treatment subsequent to straightening.

c. Parts hardened over 200 ksi UTS shall be hot formed or straightened within a temperature range from the tempering temperature to 50ºF below the tempering temperature.

3.6 Shot Peening. After final machining, all surfaces of critical or highly stressed parts which have been heat treated to or above 200 ksi UTS except for rolled threads, inaccessible areas of holes, pneumatic or hydraulic seat contact areas, and thin sections or parts which if shot peened could violate engineering and functional configuration, shall be shot peened in accordance with SAE-AMS-S-13165. Areas requiring lapped, honed, or polished surfaces shall be shot peened prior to finishing.

3.7 Stress Corrosion Cracking. The assembly stresses of low alloy steel heat treated above 200 ksi UTS shall not exceed the stress corrosion threshold limitation for the particular material and grain-flow orientation.

3.8 Low Alloy High Strength Steel Corrosion Prevention. All low alloy, high strength steel parts heat treated at 180 ksi UTS and above, including fasteners, shall require corrosion preventative metallic coatings by a process that is nonembrittling to the alloy/heat treatment combination.

SECTION 2150

TITANIUM

1. SCOPE. This section sets forth the requirements for the use of titanium and its alloys.

2. APPLICATION. Titanium sheet and plate stock shall be procured to meet the requirements of SAE-AMS-T-9046, as supplemented by contractor specifications, drawing notes or other approved documents which reflect the quality properties and processing to provide material suitable for its intended use. All titanium extruded bars, rods or special shaped sections shall be procured from the titanium Original Equipment Manufacturer (OEM), or its franchised distributor to meet the requirements of MIL-T-81556. The procurement may be supplemented by such contractor documents as necessary to assure that the metallurgical and structural properties required to meet the reliability and durability requirements of the system are met. Heat treatment of titanium and titanium alloy products shall be in accordance with MSFC-SPEC-469. For titanium alloy products not covered in MSFC-SPEC-469, heat treatment shall be in accordance with SAE-AMS-H-81200, as specified by contractor specifications.

3. SPECIAL CONSIDERATIONS

3.1 Hardenability. Titanium alloys have limited hardenability with section size and shall not be used in sections which exceed their specified limits. The surfaces of titanium parts shall be machined or chemically milled to eliminate all contaminated zones formed during processing.

3.2 Titanium Forgings. All titanium bar and forging stock shall be procured in accordance with the requirements of MIL-T-9047, supplemented by contractor documents as necessary to assure the metallurgical and structural properties required to meet the reliability and durability requirements of the system.

3.3 Titanium Contamination. Care shall be exercised to ensure that cleaning fluids and other chemicals used on titanium are not detrimental to performance. The following materials can induce stress corrosion, hydrogen embrittlement, or reduce fracture toughness and shall be prohibited from the manufacturing, assembly or contact with titanium or its alloys.

a. Hydrochloric Acid
b. Silver
c. Halogenated solvents
d. Methyl Alcohol
e. Mercury and Mercuric Compounds
f. Trichloroethylene/Trichloroethane
g. Carbon Tetrachloride
h. Halogenated Cutting Oils
i. Halogenated Hydrocarbons
j. Cadmium or silver plated clamps, tools, fixtures or jigs

3.4 Fretting of Titanium Components manufactured with titanium and titanium alloys shall be designed to prevent fretting.

3.5 Titanium Corrosion Considerations.

3.5.1 Surface Considerations. The surfaces of titanium and titanium alloy mill products shall be 100 percent machined, chemically milled or pickled to a sufficient depth to remove all contaminated zones and layers formed while the material was at elevated temperature. This includes contamination as a result of mill processing, heat-treating and elevated temperature forming operations.

SECTION 2160

OTHER METALS

1. SCOPE. This section sets forth the requirements for the use of metals not otherwise specified in this document.

2. APPLICATION. Other metals, such as nickel and copper and their alloys, which have common heritage in aerospace applications, may be used. Other metals and alloys without this heritage shall not be used unless the contractor performs and maintains a design trade study/testing that (1) demonstrates the desirability over commonly used materials, and (2) clearly demonstrates that no additional reliability risks or hazards, such as specified in paragraph 4.3, will be incurred by using these uncommon materials.

3. SPECIAL CONSIDERATIONS

3.1 Stress Corrosion Cracking. For those metals and alloys which are not covered in Mil-HDBK-5(J) or MSFC-STD-3029, or which have no available stress corrosion data or documented use history, the contractor shall demonstrate through testing in accordance with MSFC-STD-3029 that the metal or alloy is free from stress corrosion cracking from the environment and stress level in its application.

SECTION 2200

Polymeric Materials

1. SCOPE. This section sets forth the common requirements for the use of polymeric materials.

2. APPLICATION. Polymeric materials shall be selected and qualified for each application. The rationale and qualification data shall be maintained and available for review. The consideration of the following, as a minimum shall be evaluated:

a. Design engineering properties

b. Application operational requirements

c. Compatibility with other materials used

d. Material hazards and restrictions as specified in Section 4, General Requirements, paragraph 4.3.2 of this document.

e. Environmental and health restrictions mandated by applicable federal, state and local regulations

2.1 Composition and Processing. Specifications for composition and processing shall be used to ensure a product that is reproducible and meets all physical, chemical, and mechanical requirements of the intended application.

2.2 Compatibility. Polymeric materials shall be evaluated and tested or documented on the basis of detailed history for compatibility with temperature, pressure, radiation and fluid or gas environments. Tests for compatibility with hazardous fluids and gases such as oxygen or hydrogen shall consider energy sources available in the proposed application that could initiate adverse reactions.

2.3 Outgassing. All materials shall meet the outgassing requirements specified in Section 4, General Requirements, paragraph 4.1.9 of this document.

2.4 Stability. The materials shall be hydrolytically stable and not subject to reversion for their intended environments including manufacturing, testing, transportation and storage.

2.5 Storage. Polymers that are procured in non-cured or partial cured states, i.e., prepregs, frozen premixes, etc. shall be held in controlled temperature storage. Some specific materials require storage at reduced temperatures or at specific humidity conditions and shall be stored as recommended by the manufacturer. A first in, first out policy shall also be maintained.

3. SPECIAL CONSIDERATIONS

3.1 Chlorinated Fluorocarbons (CFCs). All PMP shall be free of CFCs as mandated by federal or state regulations.

3.2 Shelf-Life Limitations. Many polymeric flight materials have a shelf life specified by the manufacturer. The PMPCB shall define the shelf life control program which controls all flight materials as specified. This program shall specify what materials may have the shelf life extended and the justification and testing necessary to extend the shelf life.

3.3 Hygroscopic Materials. The hygroscopic nature of materials shall be factored in the contamination analysis. For example, nylon may pass the outgassing test but absorb water quickly from the air. (See Section 4, General Requirements, paragraph 4.1.9 of this document)

3.4 Fluoropolymers. Fluoropolymers such as PTFE, Teflon(R), FEP and TFE may creep or cold flow under pressure, or degrade when exposed to radiation environments. These materials shall not be used in these applications.

SECTION 2210

ELASTOMERS

1. SCOPE. This section sets forth the general and specific requirements for the use of Cured Elastomers, Non-cured Elastomers, and Silicone Elastomers.

2. APPLICATION. Elastomeric components shall be hydrolytically stable, not subject to reversion, and possess resistance to aging, low temperature, ozone, heat aging, working fluids, lubricants and propellants for the system for the mission life, manufacturing and storage life for which they are designed. Elastomeric materials in contact with hydrazine shall be prohibited.

3. SPECIAL CONSIDERATIONS

3.1 Cured Elastomers. Cured elastomers that are age sensitive, such as o-rings or hoses, shall be controlled by AS1933 and SAE-ARP5316. All cured elastomeric materials shall be cure dated either on the item itself or on the packaging. A policy of first in, first out shall be maintained. Cured elastomeric materials shall be protected from sunlight, fuel, oil, water, dust, and ozone. A maximum storage temperature 37.8ºC (100ºF) is recommended; the maximum storage temperature shall not exceed 51.7ºC (125ºF).

3.2 Non-cured Elastomers. Materials that are procured in non-cured state such as sealants and potting compounds shall be held in controlled temperature storage not to exceed 26.7ºC (80ºF). Some specific materials require storage at reduced temperatures and shall be stored as recommended by the manufacturer. The PMPCB shall define the shelf life control program which controls all flight materials as specified. This program shall specify what materials may have the shelf life extended and the justification and testing necessary to extend the shelf life. A first in, first out policy shall also be maintained.

4. PROHIBITED PMP shall include:

a. Some one-part silicone products including commercial adhesives/sealants, as well as those meeting the requirements of MIL-S-46106, give off acetic acid during cure and shall not be used.

SECTION 2220

FOAMED PLASTICS

1. SCOPE. This section sets forth the requirements for the use of foamed plastics.

2. APPLICATION

2.1 Hydrolytic Stability. Foamed plastics used shall be hydrolytically stable and shall not be subject to reversion.

2.2 Application. Foamed plastics shall be applied in a manner, which prevents damage to fragile components or exerts damage to adjacent surfaces. Testing or analysis shall be done and be available for review which demonstrates that the foamed plastics meet these requirements in their intended application.

2.3 Outgassing and Flammability. Only a few foamed plastics meet outgassing and flammability requirements. Often such materials require baking at elevated temperatures to reduce outgassing to acceptable levels. Nevertheless, all foamed plastics shall comply with the outgassing requirements specified in Section 4, General Requirements, paragraph 4.1.9 of this document.

3. SPECIAL CONSIDERATIONS. Foam plastics shall not be used for metal skin reinforcement, or as a core material in sandwich structural components. Foam plastics may be used in plastic sandwich parts, or as low density filler putties or syntactic foam.

SECTION 2230

LUBRICANTS

1. SCOPE. This section sets forth the general requirements for the use of lubricants.

2. APPLICATION. NASA SP-8063 shall be used as a guide in the design and application of lubricants for space flight systems and components.

3. SPECIAL CONSIDERATIONS

3.1 Application Documents. Application documents for dry film lubricants shall define surface finish requirements for surfaces to be coated. The use of film lubricants is recommended for applications requiring minimum levels of friction, maximum life, and maximum load-bearing capability.

3.2 Lubricant. Selection of a lubricant requires evaluation of life cycles, including installation, test, and utilization, as well as design margin. This rationale shall be documented and available for review.

3.3 Lubricants shall comply with the outgassing requirements specified in Section 4, General Requirements, paragraph 4.1.9 of this document.

SECTION 2240

ADHESIVES, SEALANTS, COATINGS, & ENCAPSULANTS

1. SCOPE. This section sets forth the requirements for the use of adhesives, sealants, coatings and encapsulants.

2. APPLICATION

2.1 Adhesives. Silicone adhesives for general use shall be qualified to MIL-A-46146. Adhesives for structural applications should be qualified using MIL-HDBK-83377 as a guideline, for the specific materials to be bonded.

2.3 Coatings. Conformal coatings shall be qualified to IPC-CC-830, or MIL-I-46058C(7).

2.4 Encapsulants. Materials and processes used to encase components and assemblies in plastic or elastomeric resins for electrical insulation, protection from environmental conditions, and protection from mechanical damage shall be qualified by component or assembly-level testing or past space experience under equivalent or more severe thermomechanical and radiation stresses.

All materials shall meet the outgassing requirements specified in Section 4, General Requirements, paragraph 4.1.9 of this document.

3. SPECIAL CONSIDERATIONS

3.1 Glass Transition Temperature. The secondary or glass transition temperature of silicone-based adhesives or sealants subjected to application to cryogenic temperatures during test or usage shall be a minimum of 30ºF lower than the usage qualification temperature.

3.2 Processing Requirements. Processing requirements for encapsulation shall include as a minimum the following: surface preparation or cleaning, resin or elastomer preparation, processing temperatures (including exothermic heat of reaction), shrinkage during cure, and rework.

4. PROHIBITED PMP shall include:

a. Asbestos-containing materials
b. Silicone grease as a thermal couplant
c. Corrosive (acetic acid evolving) silicone sealants, adhesives, or coatings
d. Materials which can undergo reversion in their intended application including manufacturing, testing, storage and transportation.

SECTION 2250

COMPOSITES

1. SCOPE. This section sets forth the general requirements for the use of composites and the specific requirements for the use of advanced composites, metal matrix composites, and conventional composites.

2. APPLICATION. Composite materials are material systems made up of more than one constituent, usually a strong stiff fiber and a relatively weak soft binder. For the purposes of this document, composite materials are divided into three broad categories, these being conventional composites, advanced composites and metal matrix composites. Conventional composites are fiberglass reinforced organic resins. Advanced composites are organic resins reinforced with high strength, high stiffness fibers such as aramid boron or carbon. Metal matrix composites are fiber, whisker or particulate reinforced metals. Selection of materials and processes for composites shall consider all aspects of the intended application. These aspects include: service environment, system requirements, structural and functional requirements, electrical or dielectric requirements, serviceability, manufacturability and repairability.

3. SPECIAL CONSIDERATIONS

3.1 Advanced Composites. Advanced composites consist of an organic matrix reinforced by high modulus and/or high strength fibers. The fiber reinforcement takes the form of continual unidirectional filaments (tape), woven fabric (cloth), chopped fibers etc. The fiber materials are boron, carbon, aromatic polyamide etc. Guidance in the processing and production of advanced composite materials can be found in the 436124L DOD/NASA Structural Composites Fabrication Guide. Guidance in the effective utilization of advanced composite materials and design concepts in aerospace structures can be found in the 436125L DOD/NASA Advanced Composites Design Guide, Vol I - Vol IV.

3.2 Metal Matrix Composites. In a metal matrix composite, the metal serves the same purpose as the organic binder of an organic matrix composite. Aluminum, magnesium and titanium alloys are common metal matrices.

3.3 Conventional Composites. Glass fiber reinforced plastic parts should be designed using the guidelines of MIL-HDBK-17.

SECTION 2260

CERAMICS

1. SCOPE. This section sets forth the general requirements for the uses of glasses and ceramics as structural elements.

2. APPLICATION

2.1 Limitations on Material Use. Glasses and ceramics are limited in their use as structural elements due to their brittleness at ambient temperatures and lack of suitable nondestructive inspection techniques to ensure adequate strength and fracture resistance for specific stress and environmental conditions. Mechanical properties and fracture toughness information, as well as a plan to ensure adequate quality, shall be required to demonstrate ability to use these materials in their intended application including manufacturing, testing, storage and transportation.

3. SPECIAL CONSIDERATIONS

3.1 Materials Design Information. There is no central source of materials design on glasses and ceramics similar to MIL-HDBK-5 for metals. The following sources of information are useful:

a. Larsen, D. C., Adams, J. W., and S. A. Bortz, “Survey of Potential Data for Design Allowable MIL-Handbook Utilization for Structural Silicon-Based Ceramics,” prepared by IIT Research Institute, Materials and Manufacturing Technology Division, Chicago, IL 60616, December 1981, Final Report in Contract No. DAAG 46-79-C-0078.

b. Touloukian, Y. S., Powell, R. W., Ho, C. Y., and P. G. Klemens, “Thermophysical Properties of Matter - the TPRC Data Series,” Volumes 2,5,8,9,11, and 13, IFI/Plenum, New York-Washington 1970.

c. Lynch, J. F., Ruderer, C. G., and W. H. Duckworth, “Engineering Properties of Selected Ceramic Materials,” published and distributed by the American Ceramic Society, Inc., 4055 N. High Street, Columbus, Ohio 43214, 1966.

d. Bradt, R. C., D. Hasselman, P. H., and F. F. Lange, “Fracture Mechanics of Ceramics,” Volumes 1-6, Plenum Press, New York-London 1974 (Volumes 1 and 2), 1978 (Volumes 3 and 4), 1983 (Volumes 5 and 6).

SECTION 2270

SANDWICH ASSEMBLIES

1. SCOPE. This section sets forth the requirements for the use of Sandwich Assemblies.

2. APPLICATION. All sandwich assemblies shall be vented and designed to prevent entrance and entrapment of water or other contaminants in the core structure. Sandwich assemblies should conform to the guidelines in MIL-HDBK23 and shall be tested in accordance with SAE-AMS-STD-401. Aluminum honeycomb core sandwich assemblies shall use MIL-C-7438 perforated core. Non-metallic cores may be used in structural applications where technically advantageous, but shall meet the requirement of 3.1.

3. SPECIAL CONSIDERATIONS

3.1 Nonmetallic Sandwich Assemblies. Nonmetallic structural sandwich assemblies shall be qualified for specific applications by passing a test program subjecting them to anticipated worst-case environments including mission, and ground testing.

SECTION 3000

PROCESSES

1. SCOPE. This section sets forth the common requirements for use of processes.

2. APPLICATION. Processing specifications herein represent minimum standards of quality required for space and associated hardware. In most instances, manufacturing, installation, and inspection processes are controlled by contractor specifications. The use of these specifications is encouraged provided that the minimum standards of quality and quality assurance required by the appropriate contractual specifications is achieved.

3. SPECIAL CONSIDERATIONS

3.1 Corrosion Considerations. Precautions shall be taken during manufacturing, testing, and installation operations to maintain corrosion prevention requirements and environment control to prevent the introduction of contamination, corrosion, or corrosive elements.

3.2 Statistical Process Control. Process quality controls shall be maintained through a formal, documented, statistical process control program meeting the requirements of EIA-557.

3.3 Process Records. Written or computerized process records that demonstrate successful application and completion of all required processes and related quality assurance requirements shall be maintained for the life of the program. Certifications of compliance shall not be considered acceptable proofs without associated results of analyses or documentation showing successful processing or testing.

3.4 Cleaning Prior to Application. All processes involving adhesives, prepregs, sealants, coatings and encapsulants shall require careful surface preparation to ensure adequate adhesion. Each qualified material shall be associated with one or more documents describing its application and usage. Each application document shall detail the specific cleaning procedure for all surfaces to be coated or bonded and a maximum time period between surface preparation and bonding or coating, after which surfaces shall be reprocessed. Materials covered by this section shall be qualified with the specific surface preparation procedure described.

3.5 Cleaning and Storage. All materials, parts, and assemblies that have been subjected to processing shall be appropriately cleaned and maintained in a cleaned state prior to the next process, test, use, or installation. Where appropriate, verification of appropriate levels of cleanliness and freedom from contamination shall be required.

SECTION 3100

ADHESIVE BONDING

1. SCOPE. This section sets forth the requirements for the use of adhesive bonding.

2. APPLICATION. Structural bonding shall conform to the guidelines of MIL-HDBK-83377.

3. SPECIAL CONSIDERATIONS.

Bonding of structural components, except for high temperature nozzle bonds, shall be tested under simulated service conditions using tag-end test specimens whenever possible to demonstrate that the materials and processes selected will provide the desired properties for the entire life of the component. When thermal cycle testing is required, the rate of temperature change shall not exceed the expected rate of temperature change in service. Hardware qualifications and acceptance tests plus lap shear witness coupons processed concurrently using the same material cleaning method and cure cycles can be used in lieu of tag-end test specimens. As a minimum, structural bonds shall require lap shear witness coupons processed concurrently using the same material cleaning method and cure cycles.

SECTION 3200

WELDING

1. SCOPE. This section details the general requirements for the use of welding operations and the specific requirements for weld rework and weld filler material.

2. APPLICATION. Resistance welding of electronic circuit modules shall meet the requirements of MIL-W-8939A. Training and certification of personnel and machine qualification shall be required. The design and selection of parent materials and weld methods shall be based on consideration of the weldments, including adjacent heat affected zones, as they affect operational capability of the parts concerned. Welding procedures and supplies shall be selected to provide the required weld quality, minimum weld energy input, and protection of heated metal from contaminants. The suitability of the equipment processes, welding supplies and supplementary treatments selected shall be demonstrated through qualification testing of welded specimens representing the materials and joint configuration of production parts. As a minimum requirement, welding operators shall be qualified in accordance with SAE-AMS-STD-1595. In addition, the contractor shall provide the necessary training and qualification requirements to certify each operator and the applicable welding equipment for specific welding tasks required of critical spaceflight hardware such as pressure vessel weldments, tubing weldments, and other primary structural components.

3. SPECIAL CONSIDERATIONS

3.1 Weld Filler Material. Weld rod or wire used as filler metal on structural parts shall be fully certified and documented for composition, type, heat number, manufacturer, supplier etc., as required to provide positive traceability to the end use item. In addition, qualitative analysis and nondestructive testing shall be conducted on segments of each filler rod or wire as necessary to assure that the correct filler metal is used on each critical welding task. Quantitative analyses of weld filler metal on a lot-by-lot basis will be considered acceptable, provided that each structural weldment is subjected to simulated service testing or proof loading prior to acceptance.

3.2 Weld Rework. Weld rework shall be minimized by discriminating selection of acceptable methods, procedures and specifications developed by the contractor. Weld rework is limited to the rework of welding defects in a production weld as revealed by inspection. Weld rework does not include the correction of dimensional deficiencies by weld buildup or “buttering” of parts in areas where the design did not provide for a welded joint. All weld rework shall be fully documented. Documentation as a minimum shall include weld procedures and schedules, location of the rework, nature of the problem and appropriate inspection and qualification requirements for acceptance. The quality of reworked welds shall be confirmed by 100 percent inspection of both surface and subsurface, using visual, dimensional and nondestructive techniques. Rework of welds in high performance or critical parts shall not be permitted.

SECTION 3300

BRAZING

1. SCOPE. This section sets forth the requirements for brazing operations.

2. APPLICATION

2.1 General brazing shall meet the following requirements

2.2 AWS-C3.4, AWS-C3.5, AWS-C3.6 and AWS-C3.7. Metals not covered by AWS-C3.4, AWS-C3.5, AWSC3.6 and AWS-C3.7 shall not be brazed. Resistance and dip brazing shall meet the requirements of Mil-B-7883(B). Fusion welding, or other operations involving high temperatures that may affect the brazed joint, shall be prohibited in the vicinity of brazed joints. Brazed joints shall be designed for shear loading and shall not be used to provide strength in tension for structural parts. Allowable shear strength and design limitations shall conform to those recommended in MIL-HDBK-5(J).

3. SPECIAL CONSIDERATIONS. None

4. PROHIBITED PMP shall include:

a. All metals not listed in AWS-C3.4, AWS-C3.5, AWS-C3.6 and AWS-C3.7 or MIL-B-7883(B) for resistance and dip brazing.

b. Cadmium and zinc braze fillers, if used, shall be handled to preclude the material hazards described in Section 4, General Requirements, paragraph 4.3.2 of this document.

c. Cadmium and zinc braze fillers and alloys not be used unless they comply with Section 4, General Requirements, paragraph 4.3.3 of this document.

SECTION 3400

FASTENER INSTALLATION

1. SCOPE. This section sets forth the requirements for the use and installation of fasteners.

2. APPLICATION. The installation of mechanical fasteners and associated parts, including cleaning prior to installation and application of protective finishes, shall meet the requirements of MSFC-SPEC-250 or MIL-STD-403(C) as appropriate.

3. SPECIAL CONSIDERATIONS.

3.1 Lubrication on fasteners, corrosion inhibiting materials or locking materials shall meet the outgassing requirements specified in Section 4, General Requirements, paragraph 4.1.9 of this document. Non-compliant materials shall be removed prior to installation.

3.2 Torque values and staking requirements shall be defined in the engineering drawings for all fasteners.

3.3. Fasteners installed in dissimilar metals shall meet the requirements of MIL-STD-889.

3.4 Anaerobic curing agents (i.e., loctite) typically do not pass outgassing. The outgassing requirements specified in Section 4 General Requirements, paragraph 4.1.9 of this document shall be met.

4. PROHIBITED PMP shall include:

a. Zinc and/or Cadmium platings/coatings are prohibited materials and shall not be used on space flight hardware or in thermal vacuum chambers. (See Section 4, General Requirements, paragraph 4.3.3 of this document).

b. Pure tin plating/coating on space flight hardware or in thermal vacuum chambers is prohibited (see Section 4, General Requirements, paragraph 4.3.3 of this document). Tin shall be alloyed with a minimum of 3 percent lead (Pb) by weight.

SECTION 3500

PRINTED CIRCUIT ASSEMBLY

1. SCOPE. This section sets forth the requirements for printed circuit assemblies.

2. APPLICATION

2.1 Rigid Printed Circuit Assemblies. Rigid printed circuit assemblies shall be designed in accordance with IPC-2221 Class 3 and IPC 2222 Class 3 and Section 100 of this document.

2.2 Flexible Printed Circuit Assemblies. Flexible printed circuit assemblies shall be designed in accordance with IPC-2221 Class 3 and IPC-2223 Class 3 and Section 110 of this document.

2.3 RF (microwave) Printed Circuit Assemblies. RF printed circuit assemblies shall be designed in accordance with IPC-2221 Class 3 and IPC-2252 Class 3 and Section 120 of this document.

2.4 Installation, mounting and component filleting/bonding. Installation, mounting and component filleting/bonding shall be as approved by the PMPCB, and in accordance with NASA STD-8739.3(CANCELED) for general soldering, NASA STD-8739.2 (CANCELED) for surface mounting, and NASA STD-8739.1 for bonding and filleting or J-STD-001ES. Materials shall meet the requirements of Section 2240.

2.5 Sleeving. Fragile (i.e., glass) parts shall be fitted with sleeving or buffer coat to prevent damage when coated with epoxy or other rigid conformal coatings or encapsulates. Each material shall be evaluated for the particular application and operational environment.

2.6 Hermetic Seals. Hermetically sealed devices susceptible to damage during lead formation (i.e., device leads sealed with glass or ceramic) shall be identified. Any solder dipping, re-tinning, and lead forming processes prior to assembly shall be qualified and monitored to ensure that any electrical, thermal, mechanical property or hermetic seal of the device has not been compromised.

2.7 Soldering. Soldering shall be per NASA STD-8739.3 (CANCELED) for general soldering, and NASA STD-8739.2 (CANCELED) for surface mounting or J-STD-001ES. When using the J-STD -001ES for surface mounted chip components, the “minimum end overlap” shall be 50% of the end cap. Mounting and soldering configurations not addressed in these standards shall be qualified for the life and environments of the mission by testing, with the end product requirements documented. Use of these configurations shall require customer approval. Heat sensitive components, such as fuses, shall be protected by heat sinks or other means. Solders shall meet the requirements of paragraph 4.3.3 of Section 4, General Requirements, of this document, and paragraph 3.2.g of this section.

2.8 Terminal Soldering. Step-soldering with a high temperature solder conforming to J-STD-006 shall be used when it is necessary to solder terminals to the printed circuit board. Composition of solders shall be in accordance with paragraph 3.2g of this section.

2.9 Solder in the Bend Radius. For through-hole mounted components, the solder in the bend radius shall only be acceptable for axial leaded components with a body diameter of 0.125 inch or less, and with leads formed to a 90° bend.

2.10 Cleanliness Testing. All uncoated printed wiring assemblies (circuit card assemblies) shall be meet the minimum ionic and other contaminants requirements as inspected and tested in accordance with NASA STD-8739.3 (CANCELED) or NASA STD-8739.2 (CANCELED) or J-STD-001ES.

2.11 Packaging After Test. To ensure that cleanliness levels are maintained after cleanliness testing, all Printed Wiring Board Assemblies (PWBAs) shall be protected from the environment by packaging or some other comparable means.

2.12 Conformal Coatings. All printed wiring board assemblies, except RF applications in which performance is degraded by coating, shall be conformally coated with materials specified in Section 2240 per NASA STD-8739.1 (CANCELED) or J-STD-001ES. The coated assemblies shall exhibit no blisters, cracking, crazing, peeling, wrinkles, measling, evidence of reversion or corrosion at 3-5X magnification. A pinhole, bubble, or combination thereof, shall not bridge more than 50 percent of the distance between non-common conductors.

To prevent stressing solder joints, a technique of applying conformal coating shall be used to ensure that the coating does not bridge between the printed wiring board surface and the parts or part leads. If this condition occurs, documented analysis or testing shall demonstrate that bridging by the coating does not reduce the reliability of the hardware over its mission life.

3. SPECIAL CONSIDERATIONS

3.1 Survival over a mission life. Survival of PWBAs over a mission life depends on the number of thermal cycles, the temperature range of these thermal cycles, and the levels of vibration and pyroshock. The end product requirements and mounting configurations listed in the reference specifications may not be adequate for every environment. Solder joints typically fail from thermal cycling. Vibration and pyroshock typically affect leads, ribbons and components. Analysis and/or life testing shall be performed to demonstrate survival for the intended mission and application.

3.2 REGISTERED (RELIABILITY SUSPECT) PMP

a. Large surface mounted components like chip resistors, capacitors and diodes when used in applications that require a large number of thermal cycles or large delta temperature cycles. Reliability of installation and rework procedures shall be demonstrated to meet the mission life requirements.

b. The use of all LCC (leadless chip carrier) components shall be demonstrated by qualification of assembly and cleaning procedures, and testing of flight like hardware to the mission life environments, using flight like production processes. Reliability of rework procedures shall also be demonstrated to meet the mission requirements.

c. Land grid array components, such as BGAs (Ball Grid Arrays), CCGAs (Ceramic Column Grid Arrays), are considered reliability suspect. Their use shall be demonstrated by qualification of assembly and cleaning procedures, and testing of flight like hardware to the mission environments, using flight like production processes. Reliability of rework procedures shall also be demonstrated to meet the mission requirements.

d. Barium titanate-based ceramic chip capacitors, including stacked capacitors, are subject to failure due to cracks if thermally shocked during a soldering operation. Documented assembly and rework procedures for both mass reflow and hand soldering shall be developed and qualified in accordance with the manufacturer's recommendations to prevent inducing thermal shock damage to these parts. Solder coating (tinning), except by the capacitor manufacturer, shall not be done without PMPCB approval. See Section 216 paragraph 2.3 and 2.4 for precautions with stacked capacitors.

e. Large leaded devices, such as quad packs, MCM and hybrids, that are not bonded or are improperly bonded may fail in vibration. The typical failure mode is fracturing of leads. Use of improperly chosen bonding and applied staking materials can lead to solder joint fatigue and failure. Analysis or life testing shall be performed to demonstrate survival with margin for the intended mission and application.

f. Plastic encapsulated microcircuits (PEMs) shall be baked out prior to soldering or rework in accordance with J-STD-020, Revision C, and J-STD-033, Revision E. Encapsulation material and processing may vary from component lot to lot. Glass transition temperature, Environmental resistance of the potting material, and adhesion to the lead frames may vary from component lot to component lot. Glass transition temperature shall be verified for each component lot. Verification of adhesion to the lead material that it is still intact after the soldering and rework process, and that the die is still environmental sealed shall be verified on each lot (date code) of PEMs. In addition, these parts shall require program approval prior to use.

g. Lead-free solders and finishes: Space systems are particularly vulnerable because of the severe environment and the impossibility of repairing fielded equipment. Lead-free tin platings and solders represent a significant reliability risk in space applications and shall not be used unless there is no other option. In the event that lead-free material is the only option, the contractor shall submit to the acquisition authority (the government procuring agency and the prime PMPCB) their lead-free soldering process description, lead-free tin plating description, and qualification data in the use environments for all lead-free solders and/or lead-free platings for review and approval. Note: For particular applications, the following lead-free solders have been used in space applications and are considered acceptable for the specific applications for which they were qualified: low temperature soldering In52Sn48A (In52A), high temperature soldering Sn96.3Ag3.7 (Sn96A) and Sn95Sb5 (Sb5).

APPENDIX A

RADIATION HARDNESS ASSURANCE REQUIREMENTS

THIS APPENDIX IS A MANDATORY PART OF THE DOCUMENT

A.1. SCOPE. This Appendix establishes radiation hardness assurance (RHA) requirements for monolithic microcircuit, semiconductor, and hybrid/multipchip module (MCM) parts. The RHA measures prescribed in this appendix are intended to assure operational/survival capabilities of the system in the specified radiation environment. This Appendix also prescribes preferred methodology for carrying out the specified RHA tasks.

These RHA requirements are derived from the system/equipment specification. This specification may require operational and/or survival capabilities, while the system is deployed in a prescribed orbit or radiation environment. Thus, through the process of operability/survivability allocation analysis, it is determined which radiation environments are both operational/survival and which are survival only. This analysis and allocation process results in flow down of operational/survival requirements down to the box, circuit and piece-part level.

This appendix deals with the subset of requirements that apply to piece-parts in a radiation environment, as well as the norms and disciplines that apply to incorporation of these requirements into the hardware design/manufacturing processes.

A.2. REFERENCED DOCUMENTS

MIL-HDBK-814	Ionizing Dose and Neutron Hardness Assurance Guidelines for Microcircuit and Semiconductor Devices
MIL-HDBK-815	Dose Rate Hardness Assurance Guidelines
ASTM F 1892	Standard Guide for Ionizing Radiation (Total Dose) Effects Testing of Semiconductor Devices
ASTM F 1192	Standard Guide for the Measurement of SEP Induced by Heavy Ion Irradiation of Semiconductor
ASTM F 1032	Measuring Time-Dependent Total-Dose Effects in Semiconductor Devices Exposed to Pulsed Ionizing Radiation
JESD 57	Test Procedures for the Measurement of Single –Event Effects in Semiconductor Devices from Heavy Ion Irradiation
JEP 133	Guide for the Production and Acquisition of Radiation-Hardness- Assured Multichip Modules and Hybrid Microcircuits
MIL-STD-883	Test Method Standard, Microcircuits
MIL-STD-750	Test Method Standard, Test Methods for Semiconductor Devices

A.3. ENVIRONMENTS

A.3.1 Radiation Environments. Generally, the system specification defines the orbit where the equipment will be deployed and the models that describe the trapped particle environment, the Galactic Cosmic Ray (GCR) environment and the Solar Flare environment. When man-made (nuclear weapons) radiation environments apply, the system specification would include the models that best describe the threat, as well as the operate/survive/recovery requirements. Using the particular description of these environments (in terms of ionizing dose and/or particle energy-fluences spectra), dose transport codes may be utilized to construct dose-depth curves. These could be used as first cut estimate of the dose and fluence levels that apply inside the spacecraft. As the design evolves, a more accurate mechanical model of the spacecraft can be made and dose at each location can be estimated with greater accuracy. The types of radiation environments include:

a. Trapped electrons and protons capable of inducing ionization type damage in electronic components. This damage is cumulative and is measured in terms of total ionizing dose (TID) damage. To mitigate its effect in electronic circuits, design margins shall be incorporated that will allow circuit nodes to remain functional at end-of-life.

b. Neutrons (weapons emitted), as well as trapped, solar and GCR protons capable of inducing bulk damage in monolithic microcircuits and semiconductor parts. This damage is of cumulative nature, and it is measured in terms of total non-ionizing energy loss (NIEL), or in terms of equivalent 1MeV neutron fluence. To mitigate

   its effect in electronic circuits, design margins shall be incorporated that will allow circuits to remain functional at end-of-life.

c. Protons and heavy ions of GCR and solar origin capable of inducing transient upset and/or permanent damage in electronic components. This environment is known as Single Event Phenomena (SEP) or Single Event Effects (SEE) and is characterized in terms of LET versus fluence spectra (heavy ions), or in terms of energy versus flux spectra for protons. SEE induced upsets may result in disruption of services (outages). The frequency, duration and method of recovery from outages are generally specified in the dependability and availability requirements for the system. These outage constraints are normally flowed down to the box level and to the part level. SEE induced permanent damage may cause box/system failures and thus erode the reliability of the system. Mitigation measures include judicious part selection and "in circuit" measures (EDAC, TMR, Refresh, etc.)

d. X-Rays and Gamma-rays capable of inducing prompt dose effects such as upset, latchup and burnout. These effects will cause disruption in functionality. The system requirements document generally specifies minimum upsettability thresholds below which no disruption of functionality is allowed, as well as survival and recovery requirements following an allowable outage. Mitigation measures include judicious part selection, prompt dose shielding as well as in-circuit measures (current limiting).

A.3.2 Radiation Design Margin (R_{DM}). Circuit nodes that are critical to "within specification" performance of the system shall incorporate margins intended to accommodate radiation degradation (as sustained by its monolithic microcircuit and semiconductor parts). These design margins shall be derived from, or shall be consistent with degradation limits established for monolithic microcircuit and semiconductor parts at a minimum of 2X the in-situ total ionizing dose (TID) level and displacement damage fluence (if displacement damage is applicable). R_{DM} is defined as follows:

$R_{DM} = F_{spec} / F_{in\text{-}situ}$

where

F_{spec} = Specification dose/fluence. This is the fluence and/or dose at which RWLAT is performed. It is also the dose/fluence at which parameter deratings are generated

$F_{in\text{-}situ}$ = In-situ dose and/or fluence

A.4. DESIGN REQUIREMENTS AND CHARACTERIZATION

A.4.1 Neutron/Proton Induced Displacement Damage (DD) and Total Ionizing Dose (TID) Damage. Displacement and TID induced damage cause permanent degradation in performance. For this reason, it is necessary to quantify the magnitude of this degradation as well as to incorporate sufficient design margins in circuits so that they continue to operate during/after receiving full exposure to specified dose. Accordingly, the objective of characterization testing is to measure the radiation induced parameter shift (deltas). The resulting sampling data are then used to generate degradation limits. Degradation limits are used by designers to incorporate circuit margins and to assure circuit nodes will remain operational at end-of-life (EOL)

A.4.2 Part Selection Criteria. To the maximum extent possible, QML/RHA parts that satisfy program radiation requirements shall be selected for use. Use of RHA devices lacking QML hardness validation is permitted so long as procuring activity assumes responsibility for validation of vendor's RHA process. If no suitable RHA part can be found, use of non-RHA devices is permitted if buyer assumes responsibility for radiation verification of flight lots. In all of the above cases, the device specification drawing (SMD, SCD, AID, etc.) shall state radiation performance and survival rating of the part and requirements for validation and verification of same. Also, the part nomenclature shall bear distinctive characters that are indicative of the device's radiation rating.

A.4.2.1 Characterization Test. The capability of each candidate part to operate/survive in each applicable radiation environment, and while satisfying design margin and statistical derating constraints shall be assessed by performing radiation characterization test. Use of recent (generated within last 5 years) data to assess part capability is acceptable so long as these data represents the current design (and manufacturing process at the same foundry). Assessment of successful post radiation performance shall include: functional verification of DUT's operational capability at, above and below the anticipated neutron and/or TID rating of the part.

When neutron and TID environments apply, the above functional verification of operational capability shall be done on samples that have been exposed to the cumulative effect of both neutron and TID. If using the same samples, neutron exposure shall precede TID. Functional verification using the same samples for TID and neutrons shall not apply to parameters that exhibit synergistic effects (see below).

Caution: Existing literature [1] indicates that some linear devices exhibit synergistic effects with respect to neutron and subsequent TID exposure. Synergistic effects are present when the neutron exposure that precedes total dose exposure softens (reduces) the effects of total dose. In this case, the cumulative damage caused by the combined effect of neutron plus total dose may be of lesser magnitude than the damage induced solely by either of the two and may lead to overly optimistic assessment of parameter degradation. Whereas there is no explicit requirement (insufficient data exists at this time) to test solely for the purpose of investigating this effect, Original Equipment Manufacturers (OEMs) are asked to check existing data and verify that synergistic effects are not present. If it is found that synergistic effects exist, separate samples shall be used for hardness assurance testing with respect to neutron and total ionizing dose in accordance with Paragraph 4.2.2.3.

A.4.2.2 Derivation of Radiation Degradation Limits for TID and/or Neutron. Radiation induced degradation limits shall be derived from sampling data at minimum RDM of 2X. This requirement applies to critical parameters. These are parameters that are entered in circuit node equations that demonstrate satisfactory end-of-life (EOL) performance. Once derived, these radiation degradation limits shall be disseminated to all equipment designers for incorporation in parameter's EOL values and their subsequent use in worst-case analysis.

ELDRS Mitigation Schemes. All linear bipolar and BiCMOS devices shall be tested for ELDRS susceptibility in accordance with MIL-STD-883, Method 1019. If a part is determined to be susceptible to ELDRS, the corresponding degradation limits (used for RLAT acceptance) shall be established via test data obtained at exposure rate no higher than 10 millirad per second. Radiation Wafer Lot Acceptance test of ELDRS integrated circuit devices shall be in accordance with Condition D of MIL-STD-883, Method 1019. Generally, additional mitigation measures are incorporated to compensate for the fact that the dose rate in the application is much lower that the dose rate at which radiation acceptance is performed, These ELDRS mitigation measures may consist of application of an enhancement factor to the delta limit used in worst case design and/or additional shielding beyond that required to satisfy the RDM requirement of 2X. The following constraints apply to the ELDRS enhancement factor:

a. The ELDRS enhancement factor shall be determined in accordance with MIL-STD-883, test Method 1019.
b. Alternate methodology for calculation of the ELDRS enhancement factor may be approved by the PMPCB
c. If the observed enhancement factor is greater than 1, the degradation limit used in worst case analysis (as derived from characterization test data at10 millirad/sec) shall be adjusted by this factor. Alternately, the shielding may be increased to reduce the "in-situ" dose by the appropriate adjustment factor.

A.4.2.2.1 Standard Normal Distribution. Standard normal distribution, or log normal distribution (as appropriate) of parameter values may be used for estimates of parameter limits not to be exceeded by a particular fraction of the population. MIL-HDBK-814 provides ample definitions of the variables involved for either process. Radiation degradation limits shall be set at a minimum 99 percentile cut off line as drawn on the corresponding 90 percent confidence probability density curve. In the case of standard normal distribution (refer to MIL-HDBK-814 for log-normal distribution), this is represented by the formula:

$X_R = X_{mean} \pm K_{TL}(C, N).\ S_x$ (Equation 1a)

Where

X_R = Radiation degradation limit

X_{mean} = Sample mean over all values of X, where X is the radiation-induced shift in the subject parameter

K_{TL} = Multiplying factor denoting the offset from the mean in units of sample sigma. This factor is a function of P, C and N. Tables of K_{TL} values are found in MIL-HDBK-814

P = Percentage of total population exhibiting radiation degradation not exceeding limit of X_R (99 percent)

C = Confidence level with which population inference is made (90 percent)

N = Sample size

S = Sample sigma

A.4.2.2.2 Log Normal Distribution. For the case where log-normal distribution of parameter values among the population is assumed, the above expression is modified:

$X_R = X_G \,.\, \exp\left(\pm K_{TL}(P, C, N).S_{\ln(X)}\right)$ (Equation 1b)

Where

X_R = Radiation degradation limit

X_G = Geometric mean of all X values in the sampling data = $(\Pi Xi)^{1/N}$

$S_{\ln(X)}$ = sample sigma over all values of ln(X)

A.4.2.2.3 Combining Neutron and TID Damage. Hardness assurance testing for each environment, DD and TID could be performed using a different set of radiation samples. When this approach is utilized, the combined neutron and TID degradation factor used in EOL shall be no less than:

$X_R = X_{mTID} + X_{mDD} + K_{TL}[(S_{xTID})^2 + (S_{xDD})^2]^{1/2}$

for the case of standard normal distribution. The first and second terms on the right represent the mean degradation due to TID and DD respectively. The terms in the root sum squares (RSS) represent the standard deviation due to TID and DD respectively. It is assumed that the same number of samples, as well as the same P and C are used for either neutron or TID tests.

The above expression shall be modified for the case of log normal distribution:

$X_R = (X_{GTID}).\,(X_{GDD})\exp\left(\pm K_{TL}[(S_{\ln(XTID)})^2 + (S_{\ln(XDD)})^2]^{1/2}\right)$, where X represents the normalized radiation-induced shift in the subject parameter.

The X_{GTID} and X_{GDD} terms are the geometric means from the TID and DD sampling data. The RSS terms inside the bracket represent the standard deviations.

A.4.2.2.4 Applicability and Exceptions. QML/RHA parts need not have their post radiation limits, as stated in applicable SMD, readjusted to satisfy the above 99/90 constraints. However, the basis of the post radiation limits need to be reviewed to determine if additional RDM needs to be employed to compensate for those cases where the manufacturer does not meet the 99/90 criteria. The post radiation limits in the SMD may be used in EOL calculations so long as an explicit delta term representing temperature-induced degradation is included in the calculation of EOL values.

RHA devices lacking QML validation may be derated in similar fashion as QML/RHA devices so long as the procuring activity assumes responsibility for third party validation of the part's RHA process. In this case, validation of the supplier's RHA process shall include verification that the procedures for generation of post radiation limits and for radiation acceptance of wafer lots is equivalent to and as effective as those of QML/RHA pedigree

Methodology for generation of degradation limits of non-RHA parts is subject to the above 99/90 derating constraints.

A.4.3 Single Event Effects (SEE) and Prompt Dose. SEE and prompt dose environments are capable of inducing transient (recoverable) upset, and in some cases, catastrophic damage to monolithic microcircuits, semiconductor and hybrid/MCM parts. For these motives, the prescribed hardness measures deal with operational, recovery and survival capabilities of circuits and their monolithic microcircuit and semiconductor parts. The objective of characterization testing is to measure survivability thresholds as well as susceptibility thresholds to transient upsets, and to determine recovery characteristics. This information is then used by designers to validate system level upsettability, throughout the mission, including survivability and recovery requirements

A.4.3.1 SEE Characterization Test. Part upset rates and part upset/survival threshold data are needed by equipment designers to demonstrate (via SEE Analysis) that system satisfies reliability/availability/dependability requirements. Generally, a system requirements analysis and allocation process translates system-level outage constraints into specific upset rates that apply (flow down) to subsystem, box, circuit and part level. When data indicates that the upset rate of a particular part exceeds allocated constraints, “in-circuit” mitigation measures such as EDAC, TMR, watchdog timer, etc. shall be incorporated in the design in order to achieve allocated upset rate. Survival requirements apply to all monolithic microcircuit and semiconductor parts that are deemed susceptible to SEE induced catastrophic damage. Upset/recovery constraints may not apply globally, but only to the extent necessary to satisfy system level reliability/ dependability/ availability requirement as determined via systems requirements analysis and allocation process. To the maximum extent possible, existing SEE upset and survival data may be used. SEE characterization testing in accordance with ASTM F-1192 shall be performed when suitable data are not available.

A.4.3.2 Prompt Dose Upset and Survival Characterization Test. Prompt dose upset threshold data, as well as prompt dose survival/recovery data are needed by equipment designers in order to demonstrate (via analysis and box level flash X-ray test) that subsystem, box, circuit, etc., meet operate-~~-~~through, survival, circumvention and recovery constraints. Whereas survival requirements apply globally to all parts in the equipment, operate through, circumvention and recovery constraints shall be allocated via systems requirements analysis and allocation process. To the extent necessary to satisfy, demonstrate and validate system level operate through~~,~~ survival, circumvention and recovery requirements, prompt dose upset and survival testing of piece parts shall be performed when suitable data are not otherwise available. Generally (unless otherwise specified) all prompt dose testing, except for latchup, are considered as engineering level testing. The following details apply:

Upset testing may be done using MIL-STD-883, Methods 1021 (digital parts) and 1023 (linear devices) as a guide.

Survival characterization tests shall consider photocurrent burnout threat and cable induced SGEMP currents at interfaces.

A.5. PRODUCTION ACCEPTANCE TEST

A.5.1 Radiation Wafer Lot Acceptance Testing (RWLAT). RWLAT requirements apply to wafer lots of monolithic microcircuit and semiconductor parts intended for flight use. For QML/RHA devices, the RWLAT performed in accordance with manufacturer’s QML protocol needs to be validated against the flight design to verify that the manufacturer’s irradiation bias circuit bounds the flight application. For RHA devices lacking QML/RHA validation, supplier’s lot-to-lot testing is sufficient so long as the buyer has provided third party validation of the supplier’s hardness protocol. For all other cases, including non-RHA devices, RWLAT shall be performed in accordance with Table A-I

When wafer lot traceability is not available, or when radiation samples represent 2 or more wafer lots, it is permissible to perform RWLAT so long as the prescribed sample size for a single lot is doubled (2X) while the K_{TL} multiplier remains the same as for a single lot. The K_{TL} multiplier shall be based on 99/90 statistics.

TABLE A-1. RWLAT METHODS

TEST SEQUENCE NO.	TEST	METHOD	SAMPLE SIZE
1	Neutron induced displacement damage (DD)	MIL-STD-883/750, Method 1017	Recommended sample size is a minimum of 5/wafer lot, plus 1 control sample
2	Total Ionizing Dose (TID)	MIL-STD-883/750, Method 1019. For ELDRS parts (ICs), use Condition D only.	Recommended sample size is 5/wafer lot, plus 1 control sample. For ICs that exhibit ELDRS, use Condition D only.
3	Prompt Dose Induced Latchup Test (if applicable)	MIL-STD-883, Method 1020	100 percent Screening requirements apply.

For test sequences 1 and 2, acceptance of each wafer lot shall be predicated on the program-required sampling statistics (sample mean, sample sigma, geometric mean, etc.) for the particular lot under consideration satisfying the constraints of Equations 1a or 1b above. For sequence 3, acceptance of the lot shall be based on all samples passing the acceptance criteria in the detailed test specification, or adequate mitigation in the circuit design approved by PMPCB.

A.5.2 Conditions for exemption from RWLAT. In general, devices that have an R_{DM} of 10X or greater are also exempted from RWLAT, Sequences 1 and/or 2. CMOS devices are exempted from neutron induced displacement damage test (Sequence 1).

ICs that are built using a Dielectric Isolation (DI) technology that has demonstrated radiation hardness are exempted from Sequence 3, latchup test. Also, QML/RHA devices that incorporate design features to prevent prompt dose induced latchup are exempted from latchup testing so long as the latchup hardness capability and method for verification of same are stated in applicable SMD.

A.5.3 Deleted.

A.5.4 PMP Hardness Assurance Program Plan. The contractor shall institute and incorporate into the design and manufacturing of the system a Hardness Assurance Program applicable to monolithic microcircuit and semiconductor parts in accordance with the requirements of this Appendix, as modified/tailored by SOW and system/subsystem level specification. The contractor shall prepare a Monolithic Microcircuit and Semiconductor Parts Hardness Assurance Program Plan specifying methodology for implementation of the requirements of the monolithic microcircuits and semiconductor parts Hardness Assurance Program. The plan shall include a task matrix identifying all survivability and hardness assurance tasks/subtasks, the organizational structure of the parties responsible for carrying out specific tasks, and where they fit with respect to program organizational structure. The matrix shall also identify (as applicable) intended product output of each task, receiver of this output, criteria for closure and method of reporting.

The program plan shall also discuss level of participation of parts hardness assurance responsible parties in Survivability Working Group and PMPCB functions. The plan shall address subcontractor flow down of parts hardness assurance requirements and methodology for validation of radiation hardness processes for non-QML suppliers

The program plan shall also address methodology for ELDRS testing of bipolar linear and BiCMOS microcircuits. The program plan shall define methodology for verification/validation of all piece part hardness and survivability requirements.

The plan shall address methodology for hardness assurance of hybrids and MCMs.

A.5.5 Test Documentation. Documented test plans/procedures shall be used for all piece part radiation testing for which buyer assumes responsibility. The results of this testing shall be documented in a test report, that, as a minimum, documents the test bias circuit, radiation levels, parametrics to be measured pre/post radiation exposure, statistical analysis, and a summary of the test results. Unless otherwise specified, these test reports shall be made available to the procuring activity upon request.

A.6. MATERIALS SELECTION. Materials shall be selected based on radiation design margin equal to or greater than 2X. When no supporting data are available, radiation testing shall be performed to characterize the material. Unacceptable degradation may include outgassing, elongation, embrittlement, and darkening of optical materials. The evaluation should include materials such as elastomers, adhesives, lubricants, coatings and films, propellants, optical materials and dielectrics.

1/ Jerry L. Gorelick, Ray Ladbury and Lina Kanchawa, "The Effects of Neutron Irradiation on Gamma Sensitivity of Linear Integrated Circuits," IEEE Trans. Nucl. Sci., vol. 5 , pp3679-3691, Dec. 2004.

A.7 RADIATION HARDNESS ASSURANCE REQUIREMENTS FOR HYBRID MICR0CIRCUITS AND MULTICHIP MODULES

A.7.1 Scope. This section establishes the performance requirements for hybrid microcircuits and multichip modules (MCM's) that have a radiation hardening requirement. This section is intended for devices that are offered as radiation hardened devices and are in compliance with section 960 of this document. These requirements are in addition to those previously specified in this Appendix for RHA.

A.7.2 Essential Characteristics. RHA Hybrids and MCMs are distinguished from their non-RHA counterparts by the following characteristic attributes:

a) Circuit nodes within the hybrid incorporate specific margins (headroom) intended to accommodate radiation induced degradation. This added radiation margin enables the circuit to perform its intended function after accumulation of the specified radiation dose.

b) Parent wafers and wafer lots (of component elements used for device build) shall demonstrate acceptable radiation degradation when subjected to Radiation Wafer Lot Acceptance Test (RWLAT). "Acceptable" means that the radiation samples should not degrade in excess of the allocated radiation circuit design margin budget allocated from the WCCA.

c) For those devices specifying SEP requirements, component elements shall demonstrate that they are capable of surviving a specified SEP environment (background as well as solar heavy ions and protons, and trapped protons). RHA devices should also undergo assessment of susceptibility to disruptions in functionality and propensity for upset (SEP test).

A.7.3 DESIGN REQUIREMENTS

A.7.3.1 Circuit Design Margin. The design of circuit nodes within the hybrid shall incorporate margin to assure that the hybrid will meet its specified performance requirements during the mission, at end-of-life (EOL), after accumulation of specified dose/fluence and under all rated conditions of temperature, supply voltages, input/output levels, etc. The total design margin of critical nodes shall be sufficient to accommodate worst case values of each of the above factors occurring simultaneously. Critical nodes are defined as those nodes that are essential for the hybrid device to meet its specified performance requirements. This EOL margin shall be demonstrated by performance of worst case circuit analysis (WCCA) whereby it is verified that critical nodes perform their intended function at end of life. When performing this analysis, worst case, end-of-life (EOL) values of relevant parameters shall be plugged into relevant node equations. As a minimum, the worst case, EOL values of component element parameters shall include the margins called out in Paragraph A.7.3.6.

A.7.3.2 Definition of Radiation Design Margin (RDM). RDM is defined (section A.3.2) as the ratio of test dose (or fluence) divided by "in-situ" dose (or fluence).

A.7.3.3 Radiation Design Margin Requirements. The value of RDM is intended to accommodate Displacement Damage (DD) if applicable, and Total Ionizing Dose (TID) damage caused by specified radiation dose/fluence, as stated in the applicable hardness rating of the hybrid. The following details apply:

a) If applicable, the hybrid rating shall call for both TID and DD hardness as specified in Table A.7-2. The radiation margin shall account for the combined effect of TID and DD induced degradation.

b) If the hybrid rating only specifies TID hardness, it is not necessary to incorporate damage due to DD.

c) Required margin shall be established from actual test data of component elements (TID or/and DD as applicable) in accordance with Sections A.7.4 and A.7.5

A.7.3.4 Temperature and Voltage Margin. Parameter EOL values shall incorporate the necessary margin to assure performance within specification at all temperatures and bias voltages within the specified operating temperature and bias voltage range (as specified in the hybrid's rating).

A.7.3.5 Aging Margin. Parameter EOL values shall incorporate the necessary margin to assure performance within specification during and after the end of an aging period of continuous mission operation at rated conditions. The aging factors (deltas) that are incorporated in parameter end-of-life values shall be consistent with the aging factors called out in each element's corresponding section.

A.7.3.6 Parameter's EOL Value. The hybrid's circuit design margin afforded by component element parameters is embedded into their End-of-Life (EOL) parameter values. These represent worst-case values of those parameters that appear in circuit node equations. Therefore, the formulation of parameter EOL values shall be:

$P_{EOL} = P_{SPEC} + X_T + X_R + X_{AGE} + X_V$ (Formula A.7-1), where

P_{EOL} = Parameter's EOL value

P_{SPEC} = Group A test acceptance limit at room temperature

X_T = Parameter's shift (delta) due to temperature. See Paragraph A.7.3.4

X_R = Radiation (TID + DD as applicable) induced degradation delta. See Paragraph A.7.3.3

X_{AGE} = Aging degradation delta. See Paragraph A.7.3.5

X_V = Parameter shift (delta) due to bias voltage variation. See Paragraph A.7.3.4

The above formulation of P_{EOL} applies only to a subset of component element parameters: i.e., those parameters that appear in equations of critical nodes only. Please note that in the mathematical expression for P_{EOL} (Formula A.7-1), the first 2 terms to the right of the equal sign ($P_{SPEC} + X_T$) may be replaced by the Group A test limit over the specified temperature range.

In those cases where the calculation of P_{EOL} using Formula A.7-1 results in an unacceptable result, alternate worst-case methodologies, such as RSS or Monte Carlo techniques, may be employed with the approval of the PMPCB.

A.7.3.7 Selection of Monolithic Microcircuit and/or Semiconductor Component Elements. The first order of precedence is to satisfy the radiation hardness constraints listed below. Next order of precedence is given to the manufacturing source. Preference shall be given to wafer foundries that are sources of QML certified devices or monolithic microcircuit and semiconductor devices meeting the requirements of MIL-PRF-38535 or MIL-PRF-19500. Wafer lot and/or wafer traceability requirements apply (see Section A.7.8). As part of the radiation hardness baseline, the hybrid manufacturer shall track the revision status of all monolithic microcircuit and semiconductor elements. Change notification clauses shall also be called out and exercised when procuring active devices. The radiation hardness constraints for die selection are delineated in paragraphs A.7.3.7.1 through A.7.3.7.4:

A.7.3.7.1 Selection constraints for TID and/or DD. Only devices that can survive and operate within the allocated degradation margin (X_R) may be selected for use.

A.7.3.7.2 Selection Constraints for Single Event Phenomena (SEP). The following requirements apply:

a) With respect to SEP-induced catastrophic events such as Single Event Burnout (SEB), Single Event Latchup (SEL), Single Event Gate Rupture (SEGR), etc., devices having LET threshold higher than 75 MeV-cm^2/mg are acceptable. Devices having LET threshold lower than 37 MeV-cm^2/mg are not acceptable. PMPCB shall determine the necessary requirements for devices having LET thresholds between 37 and 75 MeV-cm2/mg.

b) With respect to disruptive events that cause single-event functional interrupt (SEFI) of the hybrid and require removal of power to recover or an externally commanded reset, the same acceptability rules called out above for catastrophic damage apply.

c) With respect to single event induced upsets, preference for selection of component elements shall be given to devices that exhibit the lowest upset rate.

A.7.3.7.3 Dose Rate Effects. When dose-rate effects are specified in the acquisition documentation, the following requirements apply:

a. With respect to dose-rate-induced catastrophic events such as burnout, and latchup, susceptible active elements shall be identified and the respective dose rate limits determined, so that necessary system level mitigation can be planned, and/or alternate element selection (including the use of a 4-pi, high-Z shielded package) can be employed. Alternatively, more robust active elements with higher threshold levels to burnout and/or latchup should be considered.

b. With respect to disruptive events that cause dose-rate functional interrupt (DRFI) of the device and assembly and require removal of power to recover, the same methodology called out in (a) above for catastrophic damage shall apply.

c. With respect to dose-rate-induced upsets, preference for active element selection shall be given to devices that exhibit the highest upset threshold. Circuit redesign and/or additional 4-pi, high-Z package shielding should be considered to optimize upset performance, if still required.

d. MIL-HDBK-815 shall be used as a guideline for Hardness Assurance design considerations.

A.7.3.7.4 Stress Derating. The component elements shall satisfy the temperature and electrical stress derating limitations specified in element sections of this document. Additionally, Power MOSFETs shall be derated sufficiently with respect to V_{DS} and V_{GS} to satisfy the SEGR survival requirements specified in this appendix.

A.7.4 Radiation Characterization. The objectives of radiation characterization tests are to demonstrate/validate acceptable survival and operational performance boundaries of hybrid elements as a function of their application in the hybrid circuit. The capability of each element to operate/survive in each applicable radiation environment shall be assessed with respect to degradation in performance and respective upset/survival rates by performing radiation characterization tests. Use of recent data (no older than 60 months) to assess component element capability is acceptable so long as these data represent the current design and manufacturing process at the same foundry. Assessment of successful post radiation performance shall include verification of functional capability at intermediate dose levels below rated dose and beyond (minimum of 50% above rated TID and/or Displacement Damage (DD) of the device or failure, whichever is lower). When DD and TID environments apply, the above stated verification of functional capability shall be performed on separate samples and their effects combined as explained in Paragraph A.7.5.3.

A.7.4.1 Displacement Damage (DD) and TID. When DD and TID testing is required, the above functional verification of operational capability shall be done on samples that have been exposed to the cumulative effect of both DD and TID. Combined DD and TID testing shall be performed on separate samples and statistically analyzed in accordance with Section A.7.5. As an option, the use of the same samples for these tests shall be contingent on compliance to the requirements in paragraph A.4.1 concerning synergistic effects and shall require PMPCB approval.

A.7.4.2 SEP Characterization Test. Characterization tests of SEP-susceptible component elements shall be carried out as follows:

a) Perform SEP testing to verify compliance with the requirements of component element selection with respect to SEP as specified in Paragraph A.7.3.7.2

b) Perform SEP testing to characterize the types of upset, their LET threshold, cross section, duration and any other relevant (relevancy to hybrid's performance) attributes. The data obtained in this fashion may be used to assess (via analysis and/or simulation) the effect of upset of component elements on hybrid performance. Again, this test shall be performed to the extent necessary to support the SEP analysis in accordance with Paragraph A.7.7.3.

c) Elements shall be tested for proton SEP susceptibility unless the device is known to be immune to proton-induced SEP.

d) SEP test methodology shall be in accordance with ASTM F-1192, TM 1080 of MIL-STD-750, and JESD 57, as applicable.

Hybrid level SEP characterization tests can be substituted for the element SEP testing or used to supplement the element SEP testing when appropriate and with the approval of the PMPCB. The appropriateness of performing hybrid level SEP testing in lieu of, or in addition to, element SEP testing shall be demonstrated to the PMPCB.

A.7.5 Degradation limits. Radiation-induced degradation limits for component elements shall be derived from sampling data at minimum of 2X the rated DD fluence and/or TID dose for critical parameters. These are parameters that are entered in circuit node equations that demonstrate satisfactory end-of-life (EOL) performance of the hybrid. Once derived, these radiation degradation limits shall be incorporated in parameter's EOL values. Additionally, during radiation wafer lot acceptance, these same degradation limits shall be used as pass/fail criteria of component elements (wafer lots or individual wafers) used in hybrid build.

A.7.5.1 Sampling Statistics - Normal Distribution. The standard normal curve, or a log normal curve (as appropriate) may be used to represent the distribution of parameter values (deltas) about the mean value. MIL-HDBK-814 provides definitions of the variables involved for either process. Using the radiation characterization sampling data, radiation degradation limits shall be established at P = 99% fractional cut-off value representing acceptable degradation and C = 90% confidence. In the case of standard normal distribution, this is represented by Equation 1a (section A.4.2.2.1).

A.7.5.2 Sampling Statistics - Log Normal Distribution. For the case where log-normal distribution is used, the logarithms of parameter values are normally distributed about the log of the mean value as in Equation 1b (section 4.2.2.2).

A.7.5.3 Combining DD and TID Degradation. Hardness assurance testing for each environment, DD and TID shall be performed using separate sets of radiation samples if antagonistic effects are present (see A.4.2.1) or TID testing is for ELDRS. The combined DD and TID degradation factor used in parameter's EOL value shall be as calculated in section A.4.2.2.3.

A.7.6. RHA Baseline. The RHA baseline consists of all elements such as parts, materials, manufacturing processes, acceptance inspections, tasks, etc, that are critical to the end item satisfying its survival and operational requirements during exposure to the specified radiation environment and at end-of-life (EOL). The RHA baseline shall include engineering documents that specify items in the RHA baseline. As a minimum, the RHA baseline shall include the following items:

a) A flow chart showing how all elements in the RHA baseline come into play and are incorporated into the manufacturing and test processes. The flow chart shall also denote the timeline for execution of all hardness assurance and verification tasks

b) An RHA Baseline Matrix listing all engineering documents and revision status of elements in the radiation hardness assured (RHA) baseline for each hybrid type that undergoes successful RHA qualification.

c) A listing of all monolithic microcircuit and semiconductor elements and their approved sources of supply

d) A listing of all applicable procurement specifications for each monolithic microcircuit and semiconductor element.

e) A listing of all radiation test documents that are applicable to each monolithic microcircuit and semiconductor element. These radiation test specifications shall include the rated radiation capability and the pass/fail criteria for each parameter that is designated as critical for the hybrid to satisfy its end-of-life performance requirement.

f) A general radiation plan that covers applicable test methodology and verification processes that pertain to radiation hardness

g) Identification of any process and/or material that is deemed critical to the end item (the hybrid) satisfying its end-of-life performance requirements

The RHA baseline (and associated documentation) shall be maintained current during active procurement and shall be the subject of periodic audits and verification by the qualifying activity.

A.7.6.1 Change control procedures. Changes to the RHA baseline are not permitted unless they are accompanied by analyses and tests to evaluate the impact to RHA. In some instances such as those involving change of a monolithic microcircuit, or semiconductor element, or change of a procurement source, requalification is required. Other changes shall be evaluated jointly by the supplier and by the qualifying activity. Prior to implementation, the manufacturer and the customer community, as represented by the qualifying activity, must concur as to what additional verification shall be performed to ensure that the proposed change will not degrade the radiation hardness of the device. Accordingly, in addition to the change control procedures specified for non-RHA devices, manufacturers of RHA devices shall have in place a procedure to notify their customers (and the qualifying activity) of any proposed changes to the items under RHA baseline control (e.g., all class I and applicable class II changes).

A.7.7. Verification methods. Verification methods consist of a combination of testing at the element level and analyses at the hybrid level using the test data (statistical sampling as in the case of TID and DD) obtained at the element level as shown in Table A.7-1. Successful RHA verification to the requirements of this appendix and to the requirements of the applicable device specification drawing (SCD, SMD, etc) consist of

a. Demonstration that parent wafer lots (with respect to the component elements used inside the hybrid) satisfy the Radiation Wafer Lot Acceptance Test (RWLAT) requirements specified in A.7.8.

b. Demonstration by analysis (worst case EOL analysis) as supported by the above component element RWLAT data that the hybrid satisfies the EOL limits specified in the device specification drawing. It is surmised that this demonstration can be used to assert that the hybrid is capable of satisfying its performance requirements at end of the contractually specified mission.

c. If element level SEP characterization test data is available then a SEP analysis can be used to verify that the hybrid satisfies the element selection criteria of A.7.3.7.2 and that the hybrid operates reliably and uninterruptedly when exposed to the SEP hazards encountered in a reference geosynchronous, unless otherwise specified, environment. Otherwise, SEP testing at the hybrid level, with the approval of the PMPCB, shall be performed. Uninterrupted operation means that the rate of occurrence of disruptive events (those that need an external reset to restore functionality) shall be specified by the PMPCB.

Table A.7-1. Verification Method

Radiation	Analysis (hybrid level)	Test (element level)	Remarks
Neutron Induced Displacement Damage (DD)	Worst Case End-of-Life Analysis	Radiation Lot Acceptance Test (lot-to-lot)	Sampling statistics (0.99/0.90) apply
Total Ionizing Dose (TID)			
SEP	Hybrid's SEP Analysis	SEP Characterization Test	

A.7.7.1 Worst Case Circuit Analysis (WCCA). WCCA shall be performed to the extent necessary to demonstrate that the hybrid device will satisfy its specified performance requirements at End-of-Life. Worst case supply values, as well as worst case input signal levels and EOL parameter values shall be used in the circuit node equations (critical nodes). The analysis shall demonstrate that under worst case radiation tolerance accumulation, the circuit nodes perform their intended functions and that hybrid's functionality as well as hybrid's output parameters remain within the specified limits at end-of-life. The following requirements also apply:

a. It is not necessary for the applicable device specification drawing to list post radiation acceptance limits since no radiation test requirements are specified at the hybrid level. However, the device specification drawing shall specify EOL limits for a subset of hybrid parameters.

b. The applicable device specification drawing shall specify “beginning-of-life” (BOL) limits as well as EOL limits. The BOL limits apply to “fresh-out-the-factory” product and consist merely of the Group A limits. These are verified by performance of Group A test. The EOL limits on the other hand apply at end of mission and are verifiable via worst case analysis

c. Parameters that represent important (to the user) attributes of the hybrid shall be included in the subset of electrical parameters that have EOL limits specified.

d. The details and results of the WCCA shall be published in a supplier’s technical report. This report shall be part of the hybrid’s RHA baseline. The WCA report shall be made available to users upon request.

e. The WCCA shall include a compliance matrix denoting how each component element used in the hybrid complies with the applicable stress derating limitations specified in A.7.3.7.4.

f. The WCA shall include an EOL Parameter value matrix listing all critical parameters (to RHA) of each component element. The matrix shall also list

   1) Beginning of life limit (Group A limit)

   2) Neutron (if applicable) and TID degradation limit

   3) Temperature delta if explicitly accounted for in the EOL calculation

   4) Method for arriving at EOL value (direct sum, RSS, Monte Carlo Analysis, etc)

A.7.7.2 SEP Analysis. Analysis/simulation at the hybrid level shall be conducted using the SEP data of component elements. The objective is to assess the impact of the types of upsets that occur on component elements. The results of this analysis shall address behavior/performance of the hybrid in the standard Geosynchronous environment. Consideration shall be given to upset rates, transient loss or disturbance of an output, recovery characteristics etc. Conversely, the hybrid may be subjected to SEP testing in lieu of performing this analysis. SEP rates shall be calculated in the reference geosynchronous orbit. The following requirements also apply for calculation of SEP rates:

a. The background GCR environment shall be represented by that of CREME96, or PMPCB approved equivalent.

b. Assume occurrence of 1 solar flare event per solar cycle (every 11 years) over the mission lifetime.. SEP rates shall be calculated using CREME96 worst week environment, or PMPCB approved equivalent.

c. For devices that are susceptible to SEP events at 10 MeV-cm^2/mg or lower, proton SEP testing shall be performed and representative plots of cross section versus proton energy shall be provided so that users may calculate SEE rates that apply at their orbit of interest.

A.7.7.3 Performance requirements for RHA devices. RHA device elements shall come from wafer lots that satisfy the specified RLAT requirements. In addition, RHA devices shall meet the performance requirements of this document for the applicable device class (D, E, G, H, or K) and shall be capable of passing the tests, analyses, and inspections applicable for the environments specified in the device specification and the manufacturers approved QML RHA program plan. For further guidance on specific methods related to radiation hardness assurance see MIL-HDBK-814, MIL-HDBK-815; methods 1017, 1019, 1020, 1021, 1022, 1023 and 1032 of MIL-STD-883; methods 1017, 1019, and 1080 of MIL-STD-750; JESD 57, JEP 133, ASTM F 1892, ASTM F 1032, and ASTM F 1192.

A.7.7.4 Radiation hardness assurance (RHA) levels. The RHA designators defined in table A.7-2 shall be used in the PIN of the compliant devices which meet the requirements of the manufacturer’s approved QML RHA program. Other parameters may be specified in the device specification.

Table A.7-2. RHA Levels

RHA level and corresponding designator	Radiation total ionizing dose ((krad (Si))	Neutron Induced Displacement Damage
- (dash)	No RHA	No RHA
M	3	As specified in the acquisition documentation.
D	10	
P	30	
L	50	
R	100	
F	300	
G	500	
H	1000	

A.7.7.5 Implementation of this appendix. Manufacturers wishing to offer compliant RHA devices in accordance with this appendix may request certification by the qualifying activity (DLA Land and Maritime). In addition to the standard certification requirements, the qualifying activity shall examine all aspects of the RHA program. This includes determining that the manufacturer's conversion of customer requirements procedure includes the RHA requirements of this appendix and that the manufacturer's change control procedure includes the requirements of A.7.6. Furthermore, all RHA tests, process flows, and configuration control documentation shall be available for review to determine if they meet the requirements of this appendix. To apply for RHA certification, manufacturers shall satisfy the following

a. Successful build of initial lot of hybrids that satisfy requirements of Sections A.7.3 – A.7.5 of this appendix
b. Construction and documentation of the RHA baseline in accordance with Section A.7.6 of this appendix
c. Successful RHA verification of product in accordance with Section A.7.7 of this appendix

A.7.8 Production acceptance. Product Acceptance test applies only to the monolithic microcircuit and semiconductor elements used in the hybrid build, and it consists of Radiation Wafer Lot Acceptance Test (RWLAT). The objective of RWLAT is to conduct statistical inference based on sampling data from representative devices of such wafer lot. The lot is acceptable if it can be inferred with 90% confidence that at most, only 1% of the lot will exceed the radiation degradation limits allocated to the circuit node (per applicable WCCA) where the device under test is used.

A.7.8.1 Radiation Wafer Lot Acceptance Testing (RWLAT). RWLAT may be performed on a wafer lot basis or on a wafer-by-wafer basis. When testing on a wafer lot basis, the test samples shall be drawn from a minimum of 2 wafers. RWLAT shall be performed in accordance with Table A.7-3.

A.7.8.2 Traceability. The RWLAT scheme requires wafer lot traceability. If the wafer-by-wafer RWLAT methodology is chosen, traceability shall be carried out to the individual wafers. When wafer lot traceability is not available, or when radiation samples represent 2 or more wafer lots, it is permissible to perform RWLAT so long as the prescribed sample size for a single lot is doubled (2X) while the K_{TL} multiplier remains the same as for a single lot.

A.7.8.3 Acceptance Criteria. Sampling statistics shall be calculated in accordance with Section A.7.5 of this appendix. The lot is acceptable if the sampling data satisfy the post radiation limits specified in the device specification drawing.

Table A.7-3. RWLAT Methods

TEST SEQUENCE NO.	TEST	METHOD	SAMPLE SIZE
1	Displacement Damage (DD)	MIL-STD-883 or -750, Method 1017	Minimum sample size is 5/wafer lot (or individual wafer), plus 1 control sample
2	Total Ionizing Dose (TID)	MIL-STD-883 or -750, Method 1019. For ELDRS parts, use Condition D only	Minimum sample size is 5/wafer lot, plus 1 control sample

A.7.8.4 ELDRS Acceptance Criteria. To insure that ELDRS response is not affected by the hybrid package, radiation samples of component monolithic microcircuit and semiconductor elements that are known to manifest ELDRS shall be radiation tested in packages with similar internal gas composition (hydrogen content) and internal materials compared to the hybrid package.

A.7.8.5 Acceptance Test Precedence. If using the same samples for sequences 1 and 2 in Table A.7-3, Displacement Damage Test precedes TID. If synergistic effects are manifest, separate samples shall be used. Acceptability of the lot shall be determined on the basis of X_R of the particular lot under test not exceeding the allocated design margin of the circuit application. It is not necessary for the hybrid specification to call out radiation acceptance limits of component elements so long as these limits are captured in the suppliers RHA Plan and this plan is part of the hybrid's design/build baseline.

A.7.8.6 Radiation test reports. A test report shall be generated and available to the qualifying and procuring activities.

A.7.8.6.1 Test report. The test report shall include as a minimum; summary test plan, package type, completed radiation travel card, radiation source C of C, radiation dosimetry measurements, dose rate, temperature, pre-radiation, post radiation and control electrical measurements, as well as extended room temperature anneal conditions and electrical measurements (if required).

APPENDIX B

RESCREENING/QUALITY CONFORMANCE INSPECTION REQUIREMENTS

B.1. SCOPE. This appendix specifies rescreening requirements for Class B/QML Q microcircuits, JANTXV transistors and diodes, and Class H hybrids.

B.2. APPLICATION. When allowed per contract, the following rescreening and quality conformance inspection requirements shall be applied. These requirements are applicable only to QPL product and only to the product assurance levels specified. All other product assurance levels are unacceptable unless otherwise specified in the contract.

B.3. CLASS B/QML Q MICROCIRUIT UPSCREENING/LOT ACCEPTANCE TESTING. MIL-PRF-38535 microcircuits, Class B/QML Q shall be rescreened and lot acceptance (1/) tested in accordance with Tables B-lA, B-1B and B-1C.

B.4. CLASS H HYBRID UPSCREENING/LOT ACCEPTANCE TESTING. MIL-PRF-38534 hybrids, Class H shall be rescreened and lot acceptance (1/) tested in accordance with Tables B-2A, B-2B and B-2C.

B.5. JANTXV TRANSISTOR AND DIODE UPSCREENING/LOT ACCEPTANCE TESTING. MIL-PRF-19500 transistors and diodes, JANTXV, shall be rescreened and lot acceptance tested (1/) in accordance with Tables B-3A, B-3B and B-3C.

1/ Manufacturer lot acceptance test data in accordance with Tables B-lb, B-2b, and B-3b may be used in lieu of testing if conducted on the flight lot.

Table B-1A. MIL-PRF-38535 Class B/QML Q Microcircuit Upscreening (Test 100 percent), Test Methods of MIL-STD-883

	SCREEN	METHOD	REQUIREMENTS 1/
1.	Prescreen electricals 3/ & 7/	5005	YLN of 2 percent 9/ Optional but encouraged.
2.	Particle Impact Noise Detection (PIND)	2020	2/
3.	Serialization		100 percent
4.	Radiographic	2012	
5.	Pre-HTRB electrical parameters 3/ & 7/	-	Read and record at 25ºC
6.	High Temperature Reverse Bias (HTRB) burn-in 6/ & 8/	1015	Test condition A or C, 48 hours minimum at +150ºC or the device maximum operating limit, whichever is lower
7.	Post HTRB electricals and deltas 3/ & 7/		Read and record at 25ºC within 48 hours of removal from bias. Percent Defective Allowable: - First Pass: 5 percent or 1, whichever is greater 5/ - Second Pass: 3 percent or 1, whichever is greater 6/

TABLE B-1A. (Continued)

	SCREEN	METHOD	REQUIREMENTS 1/
8.	Dynamic Burn-in test 8/	1015 4/	240 hours minimum at +125ºC
9.	Post burn-in electrical parameters and deltas 3/ & 7/		Read and record at 25ºC within 96 hours of removal from bias. Percent Defective Allowable: First Pass: 5 percent or 1, whichever is greater 5/
10.	Final Electricals 3/ & 7/ Static Tests Subgroups 1, 2, and 3 of Table I, Method 5005 Dynamic Tests Subgroups 4, 5, and 6, or Subgroups 7 and 8 of Table B-I, Method 5005 Switching Tests Subgroup 9 of Table B-I, Method 5005	 5005 5005 5005	All failures shall be data logged Electrical testing performed at step 9 does not need to be repeated
11.	Seal test (a) Fine (b) Gross	1014	Reject criteria per test method
12.	External Visual	2009	100 percent

NOTES:

1/ Except as stated below, the requirements shall be per Class S of applicable MIL-PRF-38535 detail specifications

2/ Test condition A, multiple pass criteria of MIL-STD-883, Method 2020

3/ Parameters as called out in MIL-STD-883, Method 5004 for Class S and:

a. The Class S slash sheet, SMD if released.

b. The Class B slash sheet, SMD if released.

c. The most similar Class S family device slash sheet/SMD if there is no detail Class S slash sheet.

d. The most similar Class B family device slash sheet/SMD if there is no detail Class B slash sheet

4/ Test condition as specified in the applicable detailed slash sheet as determined in note 3/ above. Test Conditions A, B, C, and F of Method 1015 shall not apply.

5/ The lot may be automatically resubmitted to a second Dynamic Burn-in or HTRB one-time only without the necessity for MRB approval if the PDA does not exceed 20 percent . A PDA of greater than 20 percent shall require lot rejection.

6/ HTRB shall be performed when specified in the applicable MIL-PRF-38535 detail slash sheet/SMD, as determined in note 3/ above, and for certain MOS, linear, and other Microcircuits where surface sensitivity is of concern.

7/ Two correlation samples shall be used to verify functionality of all Automatic Test Equipment (ATE) and bench testing equipment. Correlation units shall be tested prior to any electrical testing. All parameters specified in the applicable detail slash sheet/SMD, as determined in note 3/ above, shall be read and recorded. If correlation units are not available, they may be removed from the lot being processed. Correlation units shall be controlled by the contractor for future upgrade screening.

8/ The order in which Dynamic Burn- in and HTRB are performed may be switched at the contractor's option.

9/ Perform Group A, subgroups 1 and 7. This test is designed to evaluate lots for continued upscreening or return to the vendor. A yield loss notification (YLN) of 2 percent should be imposed as a flag for review and disposition.

Table B-1B. MIL-PRF-38535 Class B/QML Q Microcircuit Lot Acceptance Testing, (Sample as Specified), Test Methods of MIL-STD-883

SUBGROUP	METHOD	REQUIREMENTS 11/
Subgroup 1 (a) Internal water-vapor content 5/	1018	3 devices sampled with 0 failures or 5 devices sampled with 1 failure 5,000 ppm max water content at 100ºC
Subgroup 5 (a) Electrical measurements 1/ & 2/ a. Subgroups 1,2, and 3 of Table I, Method 5005 (b) Steady state life 4/ & 10/ (c) Electrical measurements and deltas 1/ & 2/ a. Subgroups 1,2, and 3 of Table I, Method 5005	 5005 1005 5005	LTPD = 10 over subgroup 5 9/ Read and record 1000 hours minimum at +125ºC Read and record 8/
Subgroup 6 (a) Temp cycling 3/ (b) Constant acceleration 6/ (c) Seal - fine and gross 7/ (d) Electrical measurements 1/, 2/ & 7/ a. Subgroup 1 of Table I, Method 5005	 1010 2001 1014 5005	LTPD - 15 over subgroup 6 9/ Condition C, 100 cycles minimum Test condition E, Y1 orientation only Reject criteria per test method Read and record 9/

Notes:

1/ Parameters as called out in MIL-STD-88, Method 5005 and:

a. The Class S slash sheet/SMD if released
b. The Class B slash sheet/SMD if released
c. The most similar Class S family dev sheet/SMD if there is no detail Class S slash sheet.
d. The most similar Class B family dev sheet/SMD if there is no detail Class B slash sheet.

2/ Two correlation samples shall be used to verify functionality of all Automatic Test Equipment (ATE) and bench testing equipment. Correlation units shall be tested prior to any electrical testing. All parameters specified in the applicable detail slash sheet/SMD, as determined in note 1/ above, shall be read and recorded. Correlation units shall be controlled by the contractor for future upgrade screening.

3/ Temperature cycling may be performed as a part of 100 percent testing with 10 thermal cycles performed to Test Condition C of MIL-STD-883, Method 1010.

4/ A 340-hour intermittent operating life test per MIL-STD-883, Method 1006, and the applicable slash sheet may be performed in lieu of steady state life.

5/ Internal water-vapor testing may be performed as part of the DPA.

6/ Constant acceleration may be performed as part of 100 percent testing. If performed as part of 100 percent testing, constant acceleration shall be performed prior to seal leak testing.

7/ Seal leak and electrical testing need not be performed if thermal cycling and constant acceleration are performed as part of 100 percent screening.

8/ Life test samples tested at temperatures below the maximum specified junction temperature, meeting all specified acceptance criteria, and not subjected to the destructive testing of Subgroup 1, test (b), Internal Water Vapor and/or Subgroup 6, test (a), Temp cycling may be used in flight hardware with contractor's approved PMP Control Plan.

9/ Reference MIL-PRF-38535, Table B-I for the number of samples required for each specified LTPD. Resubmission of a failed lot shall be permitted one time only. The resubmission sample size shall be the sample size called out in the next lower LTPD for the number of failures experienced during the first submission with zero additional failures or larger sample sizes at the same lower LTPD with total failures between the first and second submission as specified. Parts passing the first test shall not be included in the resubmission sample without contractor's approved PMP Control Plan.

10/ Test condition as specified in the applicable detailed slash sheet as determined in note 1/ above. Test conditions A, B, C, and F of Method 1005 shall not apply.

11/ Post burn-in electrical rejects from the same inspection lot may be used for all subgroups when end-point measurements are not required.

Table B-1C. MIL-PRF-38535 Class B/QML Q Microcircuit Destructive Physical Analysis (DPA)

DPA per MIL-STD-1580 Or approved procedure	Double the sample size All anomalies shall be dispositional as acceptable or rejectable
Internal water-vapor content	Per MIL-STD-883, Method 1018. 3 devices sampled with 0 failures or 5 devices sampled with 1 failure. 5,000 ppm max water content at 100ºC 1/

NOTES:

1/ Internal water-vapor may be performed as part of Lot Acceptance Testing.

Table B-2A. MIL-PRF-38534 Class H Hybrid Upscreening (Test 100 percent), Test Methods of MIL-STD-883

	SCREEN	METHOD	REQUIREMENTS 1/
1.	Prescreen electricals 3/ & 6/	5005	YLN of 2 percent 7/ Optional but encouraged.
2.	Particle Impact Noise Detection (PIND)	2020	2/
3.	Serialization	--	100 percent
4.	Radiographic	2012	2 views
5.	Pre burn-in electrical parameters 37 & 6/	--	Read and record at 25ºC
6.	Burn-in test	1015	320 hours at +125ºC
7.	Post burn-in electricals and deltas 3/ & 6/		Read and record at 25ºC within 96 hours of removal from bias. Percent Defective Allowable: First Pass: 2 percent or 1, whichever is greater 5/
8.	Final Electricals 3/ & 6/ Static Tests Subgroups 1, 2, and 3 of Table X, Method 5008 Dynamic Tests Subgroups 4, 5, and 6 of Table X - or -Functional Tests Subgroups 7 and 8 of Table X Switching Tests Subgroups 9, 10, and 11 of Table X, Method 5008	 5008 5008 5008	All failures shall be data logged Electrical testing performed at step 7 does not need to be repeated
9.	Seal test (a) Fine (b) Gross	1014	Reject criteria per test method
10.	External Visual	2009	100 percent

NOTES:

1/ Except as stated below, the requirements shall be per Class K of applicable MIL-PRF-38534 detail specifications.

2/ Test condition A, multiple pass criteria of MIL-STD-883, Method 2020.

3/ Parameters as called out in MIL-STD-883, Method 5008 for Class K and: a. The Class K slash sheet/SMD if released, b. The Class H slash sheet/SMD if released, c. The most similar Class K family device slash sheet/SMD if there is no detail Class K slash sheet. d. The most similar Class H family device slash sheet/SMD if there is no detail Class H slash sheet.

4/ Test condition as specified in the applicable detailed slash sheet as determined in note 3/ above. Test conditions A, B, C, and F of Method 1015 shall not apply.

5/ The lot may be automatically resubmitted to a second Burn-in onetime only without the necessity, for MRB approval if the PDA does not exceed 10 percent. A PDA of greater than 10 percent shall require lot rejection.

6/ Two correlation samples shall be used to verify functionality of all Automatic Test Equipment (ATE) and bench testing equipment. Correlation units shall be tested prior to any electrical testing. All parameters specified in the applicable detail slash sheet/SMD, as determined in note 3/ above, shall be read and recorded. If correlation units are not available, they may be removed from the lot being processed. Correlation units shall be controlled by the contractor for future upgrade screening.

7/ Perform Group A, subgroups 1 and 4. This test is designed to evaluate lots for continued upscreening or return to the vendor. A yield loss notification (YLN) of 2 percent should be imposed as a flag for review and disposition.

Table B-2B. MIL-PRF-38534 Class H Hybrid Lot Acceptance Testing, (Sample as Specified), Test Methods of MIL-STD-883

SUBGROUP	METHOD	REQUIREMENTS ll/
Subgroup 1	1018	3 devices sampled with 0 failures or
		5 devices sampled with 1 failure
(a) Internal water-vapor content 4/		Max water content per MIL-PRF-38534
Subgroup 2		15 devices sampled with zero failures 5/ & 6/
(a) Electrical measurements 1/, 2/	5008	Read and record
a. Subgroups 1, 2, and 3 of Table X, Method 5008		
(b) Steady state life 3/ & 10/	1005	1000 hours minimum at +125ºC
(c) Electrical measurements and deltas 1/ & 2/	5008	Read and record 5/
a. Subgroups 1, 2, and 3 of Table X, Method 5008		
Subgroup 3		15 devices sampled with zero failures 6/
(a) Temp cycling 7/	1010	Condition C, 20 cycles minimum
(b) Constant acceleration 8/	2001	Y, orientation only 12/
(c) Seal - fine and gross 9/	1014	Reject criteria per test method
(d) Electrical measurements 1/ and 2/	5008	Read and record
a. Subgroups 1, 2, and 3 of Table X, Method 5008		

Notes:

1/ Parameters as called out in MIL-STD-883, Method 5008 for Class K and:

   a. The Class K slash sheet/SMD if released.
   b. The Class H slash sheet/SMD if released.
   c. The most similar Class K family device slash sheet/SMD if there is no detail Class K slash sheet.
   d. The most similar Class H family device slash sheet/SMD if there is no detail Class H slash sheet.

2/ Two correlation samples shall be used to verify functionality of all Automatic Test Equipment (ATE) and bench testing equipment. Correlation units shall be tested prior to any electrical testing. All parameters specified in the applicable detail slash sheet, as determined in note 1/ above, shall be read and recorded. If correlation units are not available, they may be removed from the lot being processed. Correlation units shall be controlled by the contractor for future upgrade screening.

3/ A 340-hour intermittent operating life test per MIL-STD-883, Method 1006 and the applicable

4/ Life test samples tested at temperatures below the maximum specified junction temperature, meeting all acceptance criteria, and not subjected to the destructive testing of Subgroup 1, test (b), Internal Water Vapor, and/or Subgroup 3, test (b), Temperature Cycling may be used in flight hardware with contractor's approved PMP Control Plan.

5/ Resubmission of a failed lot shall be permitted one time only using double the sample size with zero failures allowed. Parts passing the first test shall not be included in the resubmission sample without contractor's approved PMP Control Plan.

6/ Temperature cycling may be performed as part of 100 percent testing with 10 thermal cycles performed to test Condition C of MIL-STD-883, Method 1010.

7/ Constant acceleration may be performed as part of 100 percent testing with 10 thermal cycles performed to test Condition C of MIL-STD-883, Method 1010.

8/ Seal leak and electrical testing need not be performed if thermal cycling and constant acceleration are performed as part of 100 percent screening.

9/ Test Condition as specified in the applicable detailed slash sheet as determined in note 1/ above. Test conditions A, B, C, and F of Method 1005 shall not apply.

10/ Post burn-in electrical rejects from the same inspection lot may be used for all subgroups when end-point measurements are not required.

11/ Test condition A of MIL-STD-883, Method 2001

Table B-2C. MIL-PRF-38534 Class H Hybrid Destructive Physical Analysis (DPA)

DPA per MIL-STD-1580 Or approved procedure	Double the sample size or approved procedure All anomalies shall be dispositioned as acceptable or rejectable.
Internal water-vapor content 1/	Per MIL-STD-883, Method 1018. 3 devices sampled with 0 failures or 5 devices sampled with 1 failure. 5,000 ppm max water content at 100ºC. 1/

NOTES:

1/ Internal water-vapor may be performed as part of Lot Acceptance Testing.

Table B-3A. MIL-PRF-19500 JANTXV Transistor and Diode Upscreening (Test 100 Percent), Test Methods of MIL-STD-750

SCREEN	METHOD	REQUIREMENTS 1/
1. Prescreen electricals 3/ & 9/	-	YLN of 2 percent 11/ Optional but encouraged.
2. Particle Impact Noise Detection (PIND) 6/	2020	Per MIL-STD-883 2/
3. Serialization		100 percent
4. Pre HTRB electrical parameters 3/ & 9/	-	Read and record at 25ºC
5. High temperature reverse bias burn –in (HTRB) 10/ &12/ Reverse bias burn-in (for transistors) Reverse bias burn-in (for diodes and rectifiers)	 1039 1038	48 hours minimum at +150ºC or the device maximum operating temperature, whichever is lower and at minimum applied voltage a follows Transistor - 80 percent of rated VCB (bipolar) or VGS (FET and MFET) Diodes (except zeners of 10 volts or less) and rectifiers - rated < 10 amps at tc > 100ºC - 80 percent at rated vb
6. Interim electricals and deltas 3/ & 9/		Read and record at 25ºC within 16 hours of removal of bias. Percent Defective Allowable: First Pass: 5 percent or 1, whichever is greater 4/ Second Pass: 3 percent or 1, whichever is greater 5/
7. Power burn-in l0/& 13/ Burn-in (for transistors) Burn-in (for diodes and rectifiers)	 1039 1038	240 hours minimum per the applicable slash sheet
8. Post burn-in electrical parameters and deltas 3/ & 9/	-	Read and record at 25ºC within 96 hours of removal of bias. Percent Defective Allowable: First Pass: 5 percent or 1, whichever is greater 4/
9. Final electricals 3/ & 9/ a. Static Tests Subgroups 2 and 3 of Table III, MIL-PRF-19500 b. Dynamic Tests Subgroups 4 and 7 Table III of MIL-PRF-19500	-	All failures shall be data logged Electrical testing performed at step 8 does not need to be repeated.

TABLE B-3A. (Continued)

SCREEN	METHOD	REQUIREMENTS 1/
10. Radiography	2076	Optional
11. Seal test (a) Fine 7/ & 8/ (b) Gross		 (a) Test conditions 6 G or H, max leak rate = 5 X 10-6 atm cc/s except 5 X 10^-7 atm cc/s for devices with internal cavity > 0.3 cc (b) Test conditions A, C, D, E, or F
12. External Visual	2071	100 percent

NOTES:

1/ Except as stated below, the requirements shall be per JANS requirements of the applicable MIL-PRF-19500 detail
specifications.

2/ Test condition A, multiple pass criteria of MIL-PRF-19500.

3/ Parameters as called out in MIL-PRF-19500, Table II, JANS Requirements and:

a. The JANS slash sheet if released.
b. The JANTXV slash sheet if released.
c. The most similar JANS family device slash sheet if there is no detail JANS slash sheet.
d. The most similar JANTXV family device slash sheet if there is no detail JANTXV slash sheet.

4/ The lot may be automatically resubmitted to a second Power Burn-in or HTRB one-time only without the necessity for MRB approval if the PDA does not exceed 20 percent. A PDA of greater than 20 percent shall require lot rejection.

5/ A PDA of greater than 3 percent on the Power Burn-in or HTRB resubmittal shall require lot rejection.

6/ For all devices with an internal cavity.

7/ Omit this test for painted glass diodes.

8/ Omit this test for metallurgically bonded, double plug diodes.

9/ Two correlation samples shall be used to verify functionality of all Automatic Test Equipment (ATE) and bench testing equipment. Correlation units shall be tested prior to any electrical testing. All parameters specified in the applicable detail slash sheet, as determined in note 1/ above, shall be read and recorded. If correlation units are not available, they may be removed from the lot being processed. Correlation units shall be controlled by the contractor for future upgrade screening.

10/ The order in which Power Burn-in and HTRB are performed may be switched at the contractor's option.

11/ Perform group A, subgroups 2 and 4. This test is designed to evaluate lots for continued upscreening or return to the vendor. A yield loss notification (YLN) of 2 percent should be imposed as a flag for review and disposition.

12/ Test Condition A of the appropriate test method shall apply.

13/ Test Condition B of the appropriate test method shall apply.

Table B-3B MIL-PRF-19500 JANTXV Transistor and Diode Lot Acceptance Testing, (Sample As Specified), Test Methods of MIL-STD-750

SUBGROUP	METHOD	REQUIREMENTS
Subgroup 1		3 dev ices sampled with 0 failures or
		5 devices sampled with 1 failure
(a) MIL-PRF-38535, Method 5005 Internal water-vapor content 4/	1018 of MIL-STD-883	On cavity devices only. 5000 ppm max water content at 100ºC
Subgroup 4		LTPD - 5 over subgroup 4 8/
(a) Electrical measurements 1/ & 2/	--	Read and record
a. Subgroups 2 and 3 of Table III of MIL-PRF-19500		
(b) Intermittent Operating Life	1037	340 hours per the applicable slash sheet
(c) Electrical measurements and Deltas 1/ & 2/	---	Read and record
a. Subgroups 2 and 3 Table III of MIL-PRF-19500		
Subgroup 3		LTPD = 15 over subgroup 3 8/
(a) Temp cycling 3/	1051	Condition C3, 100 cycles minimum
(b) Constant acceleration 5/ & 9/	2006	Y1 orientation only
(c) Seal - fine and gross 6/	1014	Reject criteria per test method
(d) Electrical measurements 1/, 2/ & 6/	---	Read and record
a. Subgroup 2 of Table III of MIL-PRF-19500		

NOTES:

1/ Parameters as called out in MIL-PRF-19500, Table IVa and:

   a. The JANS slash sheet if released.
   b. The JANTXV slash sheet if release.
   c. The most similar JANS family dev sheet, if there is no detail JANS slash sheet.
   d. The most similar JANTXV family dev slash sheet, if there is no detail JANTXV slash sheet.

2/ Two correlation samples shall be used to verify functionality of all Automatic Test Equipment (ATE) and bench testing equipment. Correlation units shall be tested prior to any electrical testing. All parameters specified in the applicable detail slash sheet, as determined in note 1/ above, shall be read and recorded. If correlation units are not available, they may be removed from the lot being processed. Correlation units shall be controlled by contractor for future upscreening.

3/ Temperature cycling may be performed as part of 100 percent testing with 20 thermal cycles performed to test Condition C of MIL-STD-750, Method 1051.

4/ Internal water-vapor may be performed as part of the DPA.

5/ Constant acceleration may be performed as part of 100 percent screening. If constant acceleration is performed as part of 100 percent screening, It shall be performed prior to seal leak testing.

6/ Seal leak and electrical testing need not be performed if temperature cycling and constant acceleration are performed as part of 100 percent screening.

7/ Life test samples tested at temperatures below the maximum specified junction temperature, meeting all acceptance criteria, and not submitted to destructive testing of Subgroup 1, test (a), Internal Water Vapor, of Subgroup 3, test (a), Temperature Cycling may be used in flight hardware with contractor's approved PMP Control Plan.

8/ Reference MIL-PRF-19500, Table IX for the number of samples required for each specified LTPD.

9/ Resubmission of a failed lot shall be permitted one time only. The resubmission sample size shall be the sample size called out in the next lower LTPD for the number of failures experienced during the first submission with zero additional failures or larger sample sizes at the same lower LTPD with total failures between the first and second submission as specified. Parts passing the first test shall not be included in the resubmission sample without contractor's approved PMP Control Plan. Omit this test for non-cavity devices.

Table B-3C. MIL-PRF-19500 JANTXV Transistor and Diode
Destructive Physical Analysis (DPA)

DPA per MIL-STD-1580	- Double the sample size or approved procedure - All anomalies shall be dispositioned as acceptable or rejectable.
Internal water-vapor content 1/	- Per MIL-STD-883, Method 1018. - 3 devices sampled with 0 failures or 5 devices sampled with 1 failure. - 5,000 ppm max water content at 100ºC

NOTES:

1/ Internal water-vapor may be performed as part of Lot Acceptance Testing.

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APPENDIX C

ALTERNATE QCI TEST/SAMPLING PLAN

C.1. SCOPE. This appendix sets forth the requirements for implementing an alternate Quality Conformance Inspection (QCI) test plan and reduced sample size plan, which may be applied in lieu of the QCI requirements in the detailed device specification.

C.2. APPLICATION. This section may be applied to part acquisitions, which satisfy the criteria defined below. These requirements supersede the detailed requirements specified in the individual part sections.

C.2.1 Supplier. Use of the alternate QCI test/sampling plans specified in paragraph C.2.3.1 of this section may be used under the following conditions:

The product being purchased is manufactured at a supplier with a current QML/QPL certification for similar product and product technology.

The product being purchased is similar in design, materials, and processes to the product listed in the QPL (e.g., die size, die attach, bonding interconnects, etc.).

C.2.2 Product. Use of the alternate QCI test/sampling plans specified in paragraph C.2.3.1 of this section may be used under the following conditions:

a. The manufacturer has qualified the product in accordance with the qualification requirements of the part general specification. The specimen lot is homogeneous, from a single wafer lot, a single die attach machine, a single wire bonder, and a single package lot.

b. The contractor has a demonstrated manufacturing history of space quality product of this type.

c. The contractor has qualification and/or lot acceptance data, which demonstrates the reliability of this technology from this manufacturer.

d. No test and other QCI optimization have been done by the manufacturer.

e. All product alerts (GIDEP, etc.) applicable to the product in question have been reviewed and dispositioned.

C.2.3 Microcircuits per MIL-PRF-38535.

C.2.3.1 Reduced Group B Sample Size. For space quality microcircuits the requirements of MIL-STD-883, Method 5005 apply. For reduced sample size Group B testing, Table C-I may be used as an alternate to Table IIA of Method 5005 when the conditions of paragraph C.2.2 above are followed.

C.2.3.2 Reduced Group D Sample Size. For space quality microcircuits, the requirements of MIL-STD-883, Method 5005 apply. For reduced sample size Group D testing, Table C-2 may be used as an alternate to Table IV of Method 5005 when a single package lot is used.

If valid Group D data per MIL-PRF-38535 for similar devices fabricated within 6 months to this lot date code were available, the data may be used as evidence of conformance; otherwise use Table C-2.

C.2.4 Diodes and Transistors per MIL-PRF-19500.

C.2.4.1 Reduced Group B Sample Size. For diodes and transistors, the requirements of MIL-PRF-19500 apply. For reduced sample size Group B testing, use Table E-VIa of MIL-PRF-19500.

APPENDIX C ALTERNATE QCI TEST/SAMPLING PLAN

If valid Group B data per MIL-PRF-19500 is available for similar devices fabricated within 6 months to this lot date code, only Group C Subgroup 6 per Table E-VII of MIL-PRF-19500 need be performed.

C.2.4.2 Reduced Group C Sample Size. For diodes and transistors, the requirements of MIL-PRF-19500, Table V apply for reduced Group C sample size, (see paragraph C.2.2).

If valid Group C data per MIL-PRF-19500 for QPL devices fabricated within 6 month to this lot date code were available, the data may be used as evidence of conformance. The life test per 30.2.1.1 shall still be performed.

Table C-1. Reduced Group B Sample Size

SUBGROUP AND TEST 1/	MIL-STD-883 METHOD	QUANTITY 3/			
		USE PARTS FROM PREVIOUS TESTS	UNTESTED NO. OF PARTS		REJECTS ALLOWED
			ELEC REJ1/	ELEC GOOD	
Subgroup 1					
a) Physical Dimensions	2016	--	3		0
b) Internal Water-Vapor Content 12/	1018	3			0
Subgroup 2		--			
a) Resistance to Solvents	2015	2	3		0
b) Internal Visual	2013 & 2014	2			0
c) Bond Strength 4/	2011 Cond D	3			0
d) Die Shear	2019	3			0
Subgroup 3 2/					
Solderability	2003	3			0
Subgroup 4					
a) Lead Integrity	2004 Cond B2	--	2		0
b) Seal 6/	1014				
1) Fine	Cond A or B	2			0
2) Gross	Cond C				
c) Lid Torque 5/	2024	2			0

APPENDIX C ALTERNATE QCI TEST/SAMPLING PLAN

TABLE C-1 REDUCED GROUP B SAMPLE SIZE (Continued)

SUBGROUP AND TEST 1/	MIL-STD-883 METHOD	QUANTITY 3/			
		USE PARTS FROM PREVIOUS TESTS	UNTESTED NO. OF PARTS		REJECTS ALLOWED
			ELEC REJ1/	ELEC GOOD	
Subgroup 5 7/ 8/ 13/					
a) Electrical Parameters	per detail spec	5		5	0
b) Steady State Life (1000 hrs. min) ll/	1005 Cond D	5			0
c) Electrical Parameters	per detail spec				0
Subgroup 6 8/ 9/					
a) Electrical Parameters	per detail spec	--		4	0
b) Temperature Cycling	1010-C, 100 cycles	4			0
c) Constant Acceleration	2001 Cond E	4			0
d) Seal 6/	1014	4			0
1) Fine	Cond A or B				
2) Gross	Cond C				
e) Electrical Parameters	per detail spec	4			0
TOTAL - 17 10 /			8	9	

NOTES:

1/ At vendor's risk, electrical rejects or delta failures may be used for Subgroups 1,2,3, & 4 but shall have been processed through all the S-level screening requirements of MIL-STD-883, Method 5004. Sequence of tests may be altered at vendor's option. To minimize the total sample size requirements, the suggested sequence of subgroup testing is 1a), 4a), 4b), 3, 2a), 1b), 4c), 2b), 2c), 2d). The same four samples may then be used throughout Subgroups 1-4 (saving five samples from the total required). Care should be taken in samples selected for tests following test 1b) (internal water-vapor content) in this sequence since the lid puncture may affect the integrity of the seal or the internal cavity. Additional samples may be required to substitute damaged parts.

2/ Subgroup 3 (solderability) shall be performed prior to Subgroup 2 (Resistance to Solvents, etc.) when the same samples are used for both subgroups. LTPD and footnote for Subgroup 3 of Method 5005 Table IIa shall apply,

3/ Quantities stated represent minimum quantities. If larger sample sizes are used, the reject criteria shall not change.

4/ Number of bonds to be pulled shall be equally distributed among the test parts using the quantity/accept number (based on the number of bonds to be pulled) of MIL-STD-883, Method 5005, Table IIa.

5/ Lid Torque test shall apply only to glass-frit-sealed packages.

6/ Test Conditions D and E prohibited.

7/ Unless otherwise specified, all test conditions and end points shall be per the Table 1, Group B requirements of the detail specification.

8/ A minimum of 5 samples shall be randomly selected from each wafer lot after successful completion of Group A.

9/ At the vendor's option, with written approval from the Procuring Activity, Subgroup 5 samples may be used for Subgroup 6.

10/ If the sample options of notes 1/ and 9/ are used the total sample size requirement is nine (9) parts.

11/ The time/temperature regression table (for Class S) of Method 1005 may be utilized;, however, the life test temperature shall be the same as the burn-in screen temperature.

12/ Internal water-vapor content test is required only on glass-frit-sealed packages. On other package types, the periodic Group D test is therefore required, using the same quantity/accept number samples as identified for this Group B test. The internal water-vapor content quantity/accept number footnote of Method 5005 Table IIa shall apply here.

13/ Read and record.

Table C-2. Reduced Group D Sample Size 1/

SUBGROUP AND TEST 2/	MIL-STD-883 METHOD - CONDITION	QUANTITY 3/			
		USE PARTS FROM PREVIOUS TESTS	UNTESTED NO. OF PARTS		REJECTS ALLOWED
			ELEC REJ1/	ELEC GOOD	
Subgroup 1 4/ 6/		---			
a) Physical Dimensions	2016		3		0
Subgroup 2 4/ 6/					
Lead Integrity	2004-B2	3 and	2		0
Seal 5/	1014	5			0
a) Fine	Con A or B				
b) Gross	Cond C				
Subgroup 3					
Thermal Shock	1011-B, 15 cycles	---			0
Temperature Cycling	1010-C, 100 cycles	5		5	0
Moisture Resistance	1004	5			0
Seal 5/	1014	5			0
a) Fine	Cond A or B				
b) Gross	Cond C				
Visual Examination	1004/1010	5			0
End-Point Elect. Parameters	per detail spec	5			0

Table C-2. Reduced Group D Sample Size (Continued)

SUBGROUP AND TEST 2/	MIL-STD-883 METHOD – CONDITION	QUANTITY 3/			
		USE PARTS FROM PREVIOUS TESTS	UNTESTED NO. OF PARTS		REJECTS ALLOWED
			ELEC REJ1/	ELEC GOOD	
Subgroup 4					
Mechanical Shock	2002 -B	5			0
Vibration, Var. Freq.	2007-A	5			0
Constant Acceleration	2001-E	5			0
Seal 5/	1014	5			0
a) Fine	Cond A or B				
b) Gross	Cond C				
Visual Examination	1010/1011	5			0
End-Point Elect. Parameters	per detail spec	5			0
Subgroup 6 4/ 6/ Internal Water-Vapor Content	1018	– –	N/A 10/		
Subgroup 7 6/ Adhesion of Lead Finish	2025	– –	5 8/		0
Subgroup 8 4/ 6/ Lid Torque 7/	2024	5			0
TOTAL - 15 9/			10	5	

NOTES:

1/ Footnotes to MIL-STD-883, Method 5005 apply.

2/ Unless otherwise specified, all test conditions and end-points shall be per the Table I, Group D requirement of the detail specification.

3/ Quantities stated represent minimum quantities. If larger sample sizes are used, the reject criteria shall not change.

4/ Data results from Group B samples may be used in lieu of performing Group D, Subgroups 1, 2, 6, and 8 where Group B inspection is being performed on samples from the same inspection lot.

5/ Test Conditions D and E prohibited.

6/ Electrical rejects or delta failures from the same inspection lot may be used provided they have been processed through all the S level screening requirements of MIL-STD-883, method 5004.

7/ To be performed only on packages which used glass-frit seal to leadframe.

8/ At the vendor's option Subgroup 2 samples may be used for Subgroups 7 & 8.

9/ If the sample option of note 8/ is used the total sample size requirement is ten (10) parts.

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APPENDIX D
NOTES

The contents of this Appendix are intended for guidance and information only.

D.1. INTENDED USE. This document should be cited in the program-specific contract requirements for PMP. This document is intended for use in all USAF Space and Missile Systems Center and DDSE acquisitions for space vehicles, payloads, and for their subtier equipments.

The requirements in the text of this document state the application requirements for all electronic parts used in a space program. These application requirements include derating requirements, end-of-life limitations, mounting requirements, and other requirements intended to ensure the high reliability of the parts when used in space equipment.

The requirements in the text of this document are also intended to be the basis for preparing detailed part, material, and process specifications for the purchase of parts and materials for use in space. These requirements include the design, construction, and quality assurance requirements that are necessary for space-level PMP. The requirements included supersede or supplement requirements in existing general military specifications to ensure the necessary performance in the space environment and the necessary quality and reliability for space use.

For the convenience of everyone using this document, and also using TOR-2006(8583)-5235 (Parts, Materials, and Processes Control Program for Space Vehicles), the definitions of common key terms are the same for both.

Contracts for ground equipment (e.g., control segments and user segments of space systems) usually apply other part specifications for equipment in those segments unless it is determined that a tailored application of this document would be more appropriate for the reliability or standardization objectives of the program. Note that many space acquisition contracts include both space and ground equipment, so care should be taken to ensure that the applicability of this document is clearly stated in the program specifications.

There may be acquisition contracts for other types of equipment requiring high reliability where the special requirements stated in this document should be applied. For those acquisition contracts, this document may be cited to specify the applicable requirements. However, a statement should be included in the contract or the program specifications indicating that the words "space" in this document are to be interpreted as the applicable equipment. The requirements in this document would then be interpreted as applying to the PMP requirements for the acquisition of the applicable equipment. The use of such wording could avoid any possible misinterpretation or misapplication.

D.2. TAILORING

D.2.1 Tailored Application. The PMP requirements in each acquisition should be tailored to the needs of that particular program. Military specifications and standards need not be applied in their entirety. Only the minimum requirements needed to provide the basis for achieving the required performance should be imposed. The cost of imposing each requirement of this document should be evaluated by the program office and by the contractors against the benefits that should be realized. Provisions not required for the specific application should be excluded. The surviving provisions should be tailored to impose only the minimum requirements necessary to support the system.

D.2.2 Tailoring To Contract Phase. This document contains comprehensive requirements for electronic PMP that primarily apply during the design and production phases of a program. When this document is made compliant in a contract for a concept development phase or for a validation and demonstration phases, it does not imply that space quality PMP requirements apply to anything other than qualification and flight hardware (e.g., they do not apply to ground demonstration models). Contracts for the demonstration and validation phase usually require the development of a Parts, Materials, and Processes Control Program plan and at least a first draft of a parts selection list. The contractor should, therefore, have a complete understanding of the parts requirements to successfully transition into subsequent phases of the contract. This document is intended to be "self tailoring" in this respect so that specific tailoring to each phase of the contract should not be required.

APPENDIX D NOTES

D.2.3 Tailoring Part Specifications. The intent of the design and construction requirements, and quality assurance requirements, specified in this document is to assure that acceptable space quality parts are acquired. The part qualification is intended to verify the design. The in-process production controls specified in the detailed requirements section of this document for each part type are intended to assist in maintaining the quality of each production lot. Additional in-process controls should be imposed as required to achieve the high quality and reliability goals of space parts. The imposition of appropriate in-process controls is a more cost-effective way of screening out defects than the imposition of tests and inspections on completed units. In fact, the high reliability goals for space quality parts can only be achieved by the imposition of all of the appropriate in-process controls. Nonconforming material or items that do not meet the established tolerance limits set for the in-process production screens should be removed from the production lot.

The 100 percent screening requirements specified in the detailed requirements section of this document for each part type are intended to be the last step in assuring the quality of each part in a production lot. Nonconforming units that do not meet the established limits set for the 100 percent screens are removed from the production lot. When it has been thoroughly demonstrated that the purpose of a 100 percent screening requirement specified for a particular part type has been met by the in-process controls imposed by the manufacturer, consideration should be given to deleting that screening requirement. For most contracts, this tailoring of the requirements would require approval by the contracting officer.

The lot conformance testing requirements specified in the detailed requirements section of this document for each part type are intended to be a sample check of the achieved quality of each production lot. If no failures occur during lot conformance tests, the remaining portion of the production lot is certified as acceptable. If any of the sample units subjected to the lot conformance tests fail during the testing, a detailed failure analysis should be conducted to establish the cause of failure and the corrective actions that would eliminate subsequent failures of a similar type. Failures not affecting the part reliability or performance, such as due to test equipment or procedural errors, should not be counted as a part failure, and another randomly selected sample taken from the production lot may be substituted. However, any part failure during lot conformance testing must be taken as a very serious matter. Each part failure should be identified as either screenable from the completed production items, screenable from new production items by implementing corrective actions that would eliminate subsequent failures of a similar type, or not screenable. Appropriate corrective actions may require approval by the contracting officer.

When it has been thoroughly demonstrated that the purpose of a lot conformance test requirement specified for a particular part type has been met by the in-process controls and the 100 percent screening requirements imposed by the manufacturer, consideration should be given to deleting that lot conformance test requirement. For most contracts, this tailoring of the requirements would require approval by the contracting officer.

D.3. DATA ITEMS. This document does not require the delivery of any data. Data requirements are not to be considered deliverable unless specifically identified as deliverable data in the contract or purchase order, with the appropriate Data Item Description (DID) referenced.

SMC Standard Improvement Proposal

INSTRUCTIONS

1. Complete blocks 1 through 7. All blocks must be completed.
2. Send to the Preparing Activity specified in block 8.

NOTE: Do not use this form to request copies of documents, or to request waivers, or clarification of requirements on current contracts. Comments submitted on this form do not constitute or imply authorization to waive any portion of the referenced document(s) or to amend contractual requirements. Comments submitted on this form do not constitute a commitment by the Preparing Activity to implement the suggestion; the Preparing Authority will coordinate a review of the comment and provide disposition to the comment submitter specified in Block 6.

SMC STANDARD CHANGE RECOMMENDATION:	**1. Document Number**	**2. Document Date**
3. Document Title		

4. Nature of Change
(Identify paragraph number; include proposed revision language and supporting data. Attach extra sheets as needed.)

5. Reason for Recommendation

6. Submitter Information

a. Name	**b. Organization**
c. Address	**d. Telephone**
e. E-mail address	**7. Date Submitted**

8. Preparing Activity

Space and Missile Systems Center
AIR FORCE SPACE COMMAND
483 N. Aviation Blvd.
El Segundo, CA 91245
Attention: SMC/EN