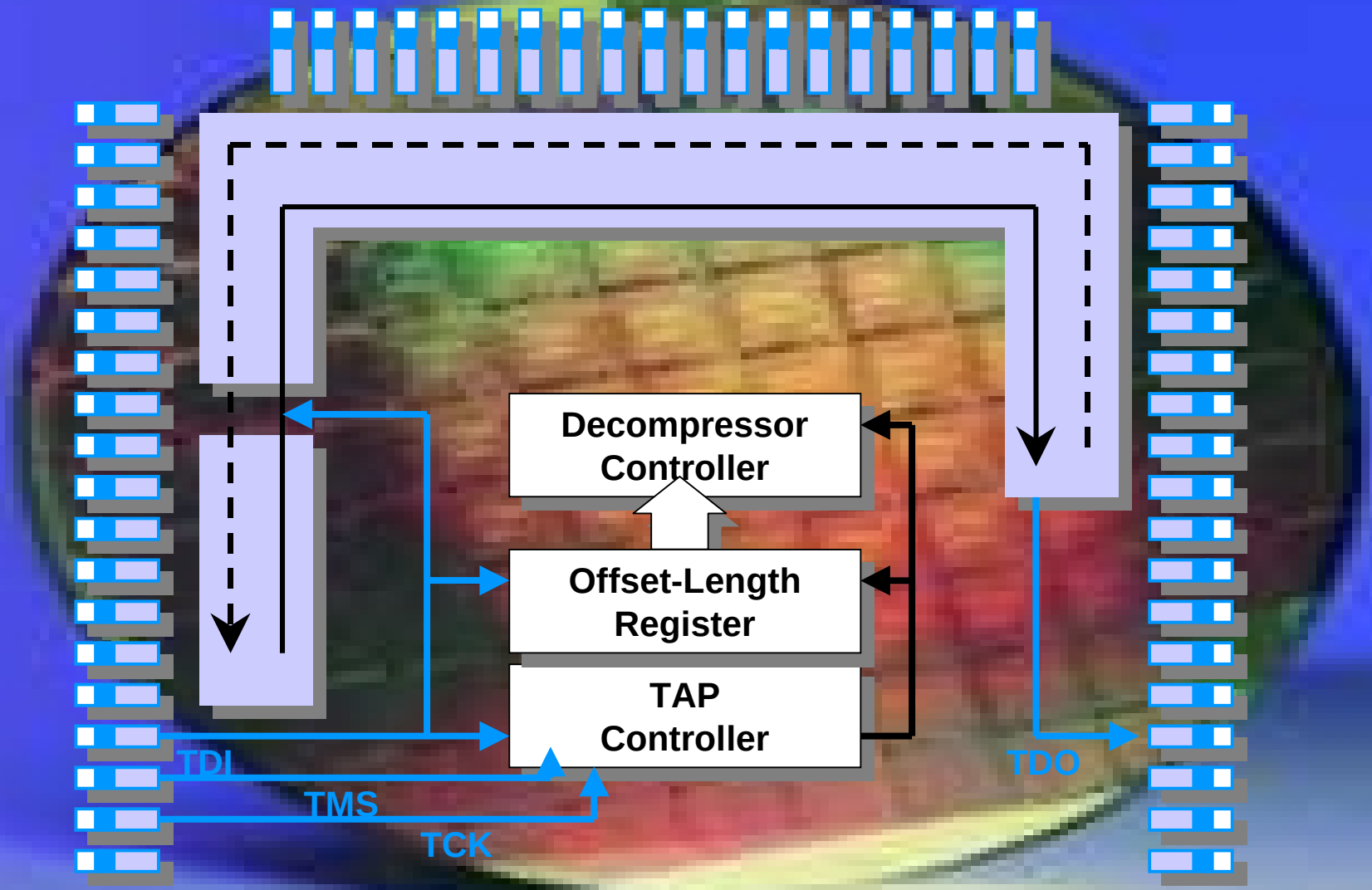
Test Data Compression and Hardware Decompression for Systems on a Chip



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Outline

- Motivation
- System-on-a-Chip testing
- Lempel-Ziv compression
- Test data compression
- Hardware decompression
- Conclusion & future works

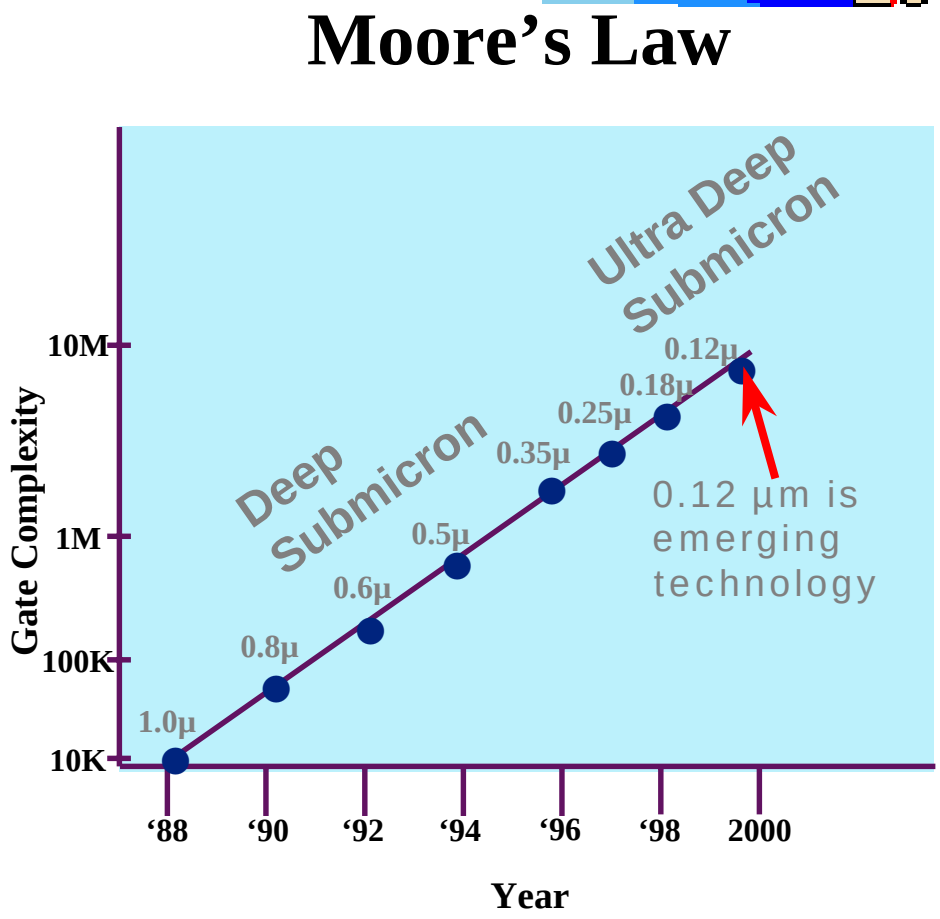
Motivation: Moore's Law

Every 18 months:

- **Gate count doubles**
- **Vector set grows 10x**
- **Frequency increases 50%**

Benchmark Design

- **0.18µ**
- **>600 MHz**
- **10 million gates**

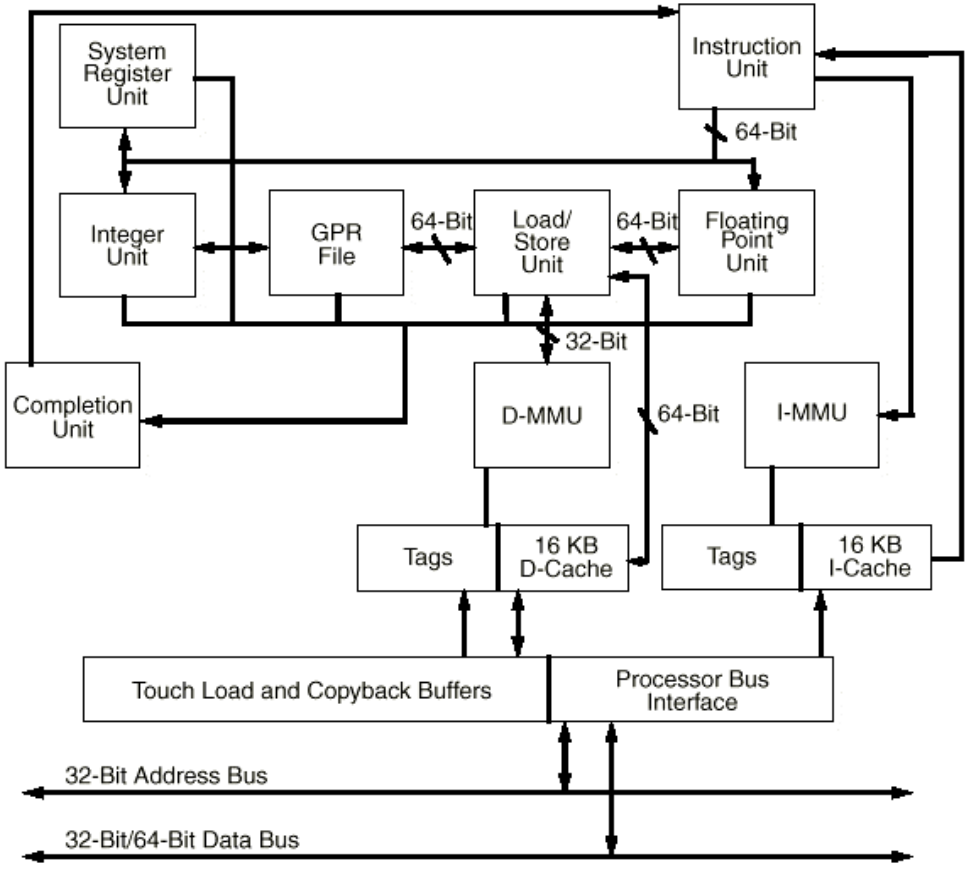


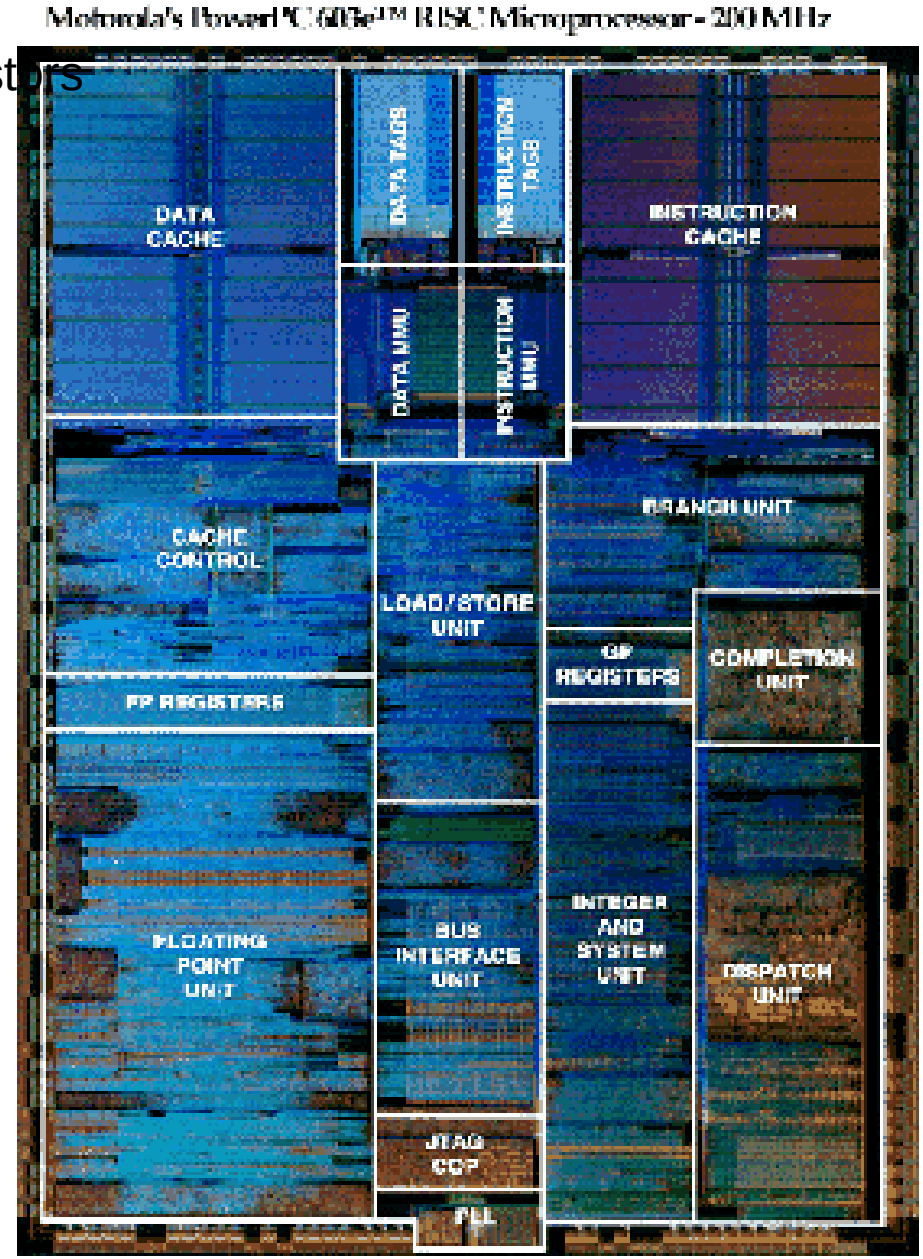
- SoCs by the year 2005, predicts that the state of the art ICs will exceed 100 million gates.
- SoC chip testing technology based on ATE (automatic test equipment) taking longer.

Processor-on-a-Chip: PowerPc 603

Year: 1994 / 66 to 80 MHz
Process: 0.5-micron CMOS / 1.6 million transistors
Cache: 8Kb Inst. / 8 kb Data

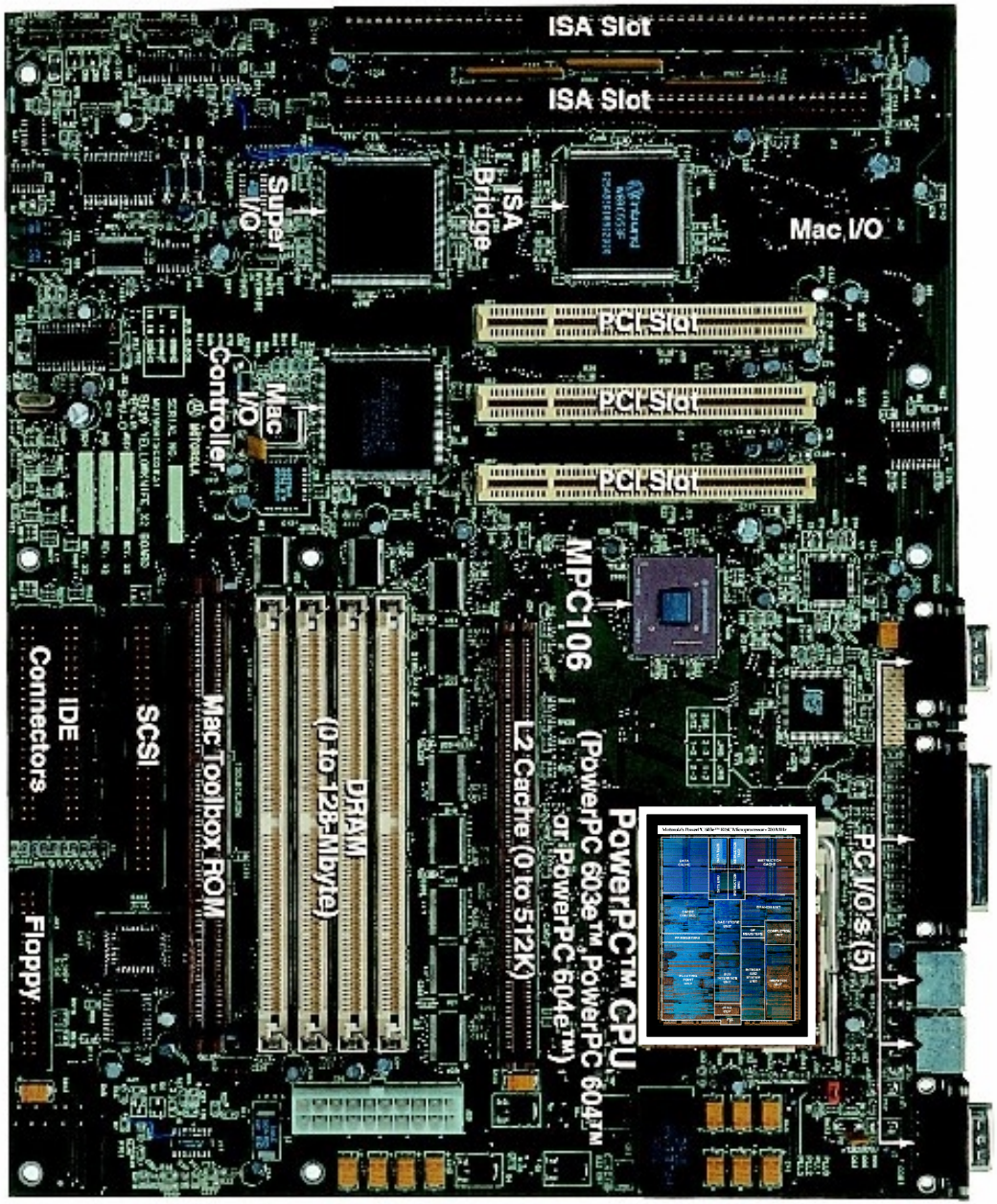
Year: 1997 / 225 Mhz to 300 Mhz
Process: 0.5 to 0.35-micron CMOS
Cache: 16 Kb Inst / 16 Kb Data





System-on-a-Chip: SoC

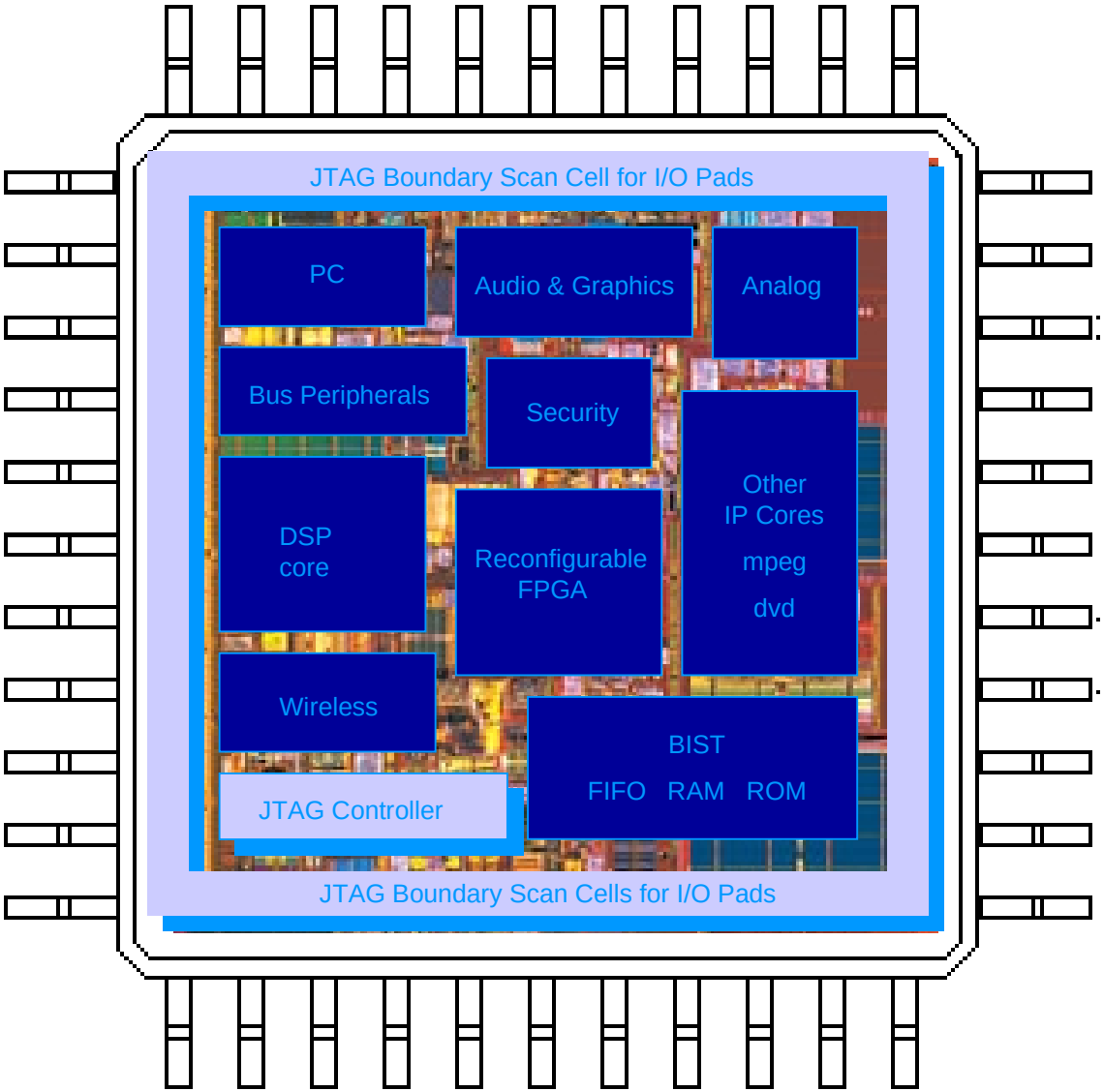
- *Systems* are traditionally composed of many separate chips: microprocessor, RAM, audio chips, …
- SoCs goal is to integrate all these components on a single chip: Better, Faster and Cheaper.



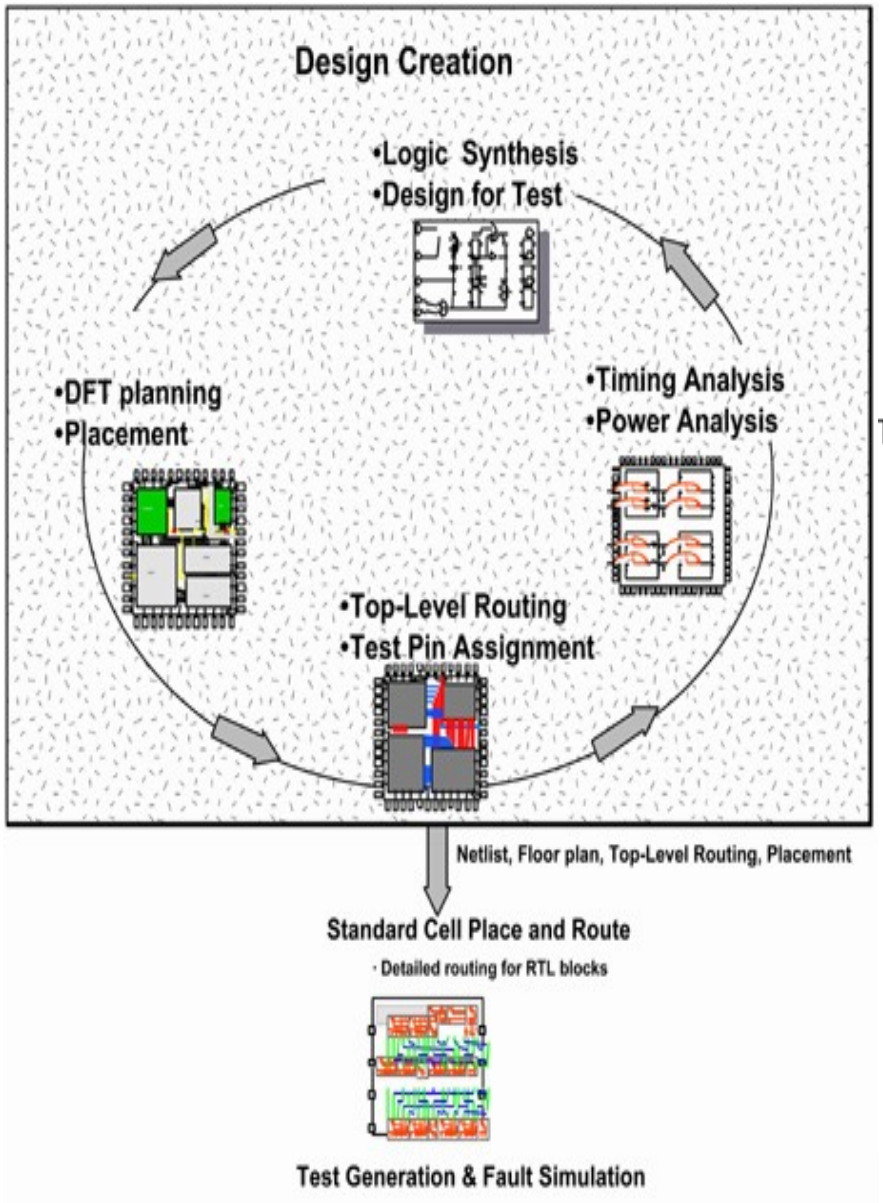
- Alternative Note: NASA says it's Faster, Better and Cheaper.

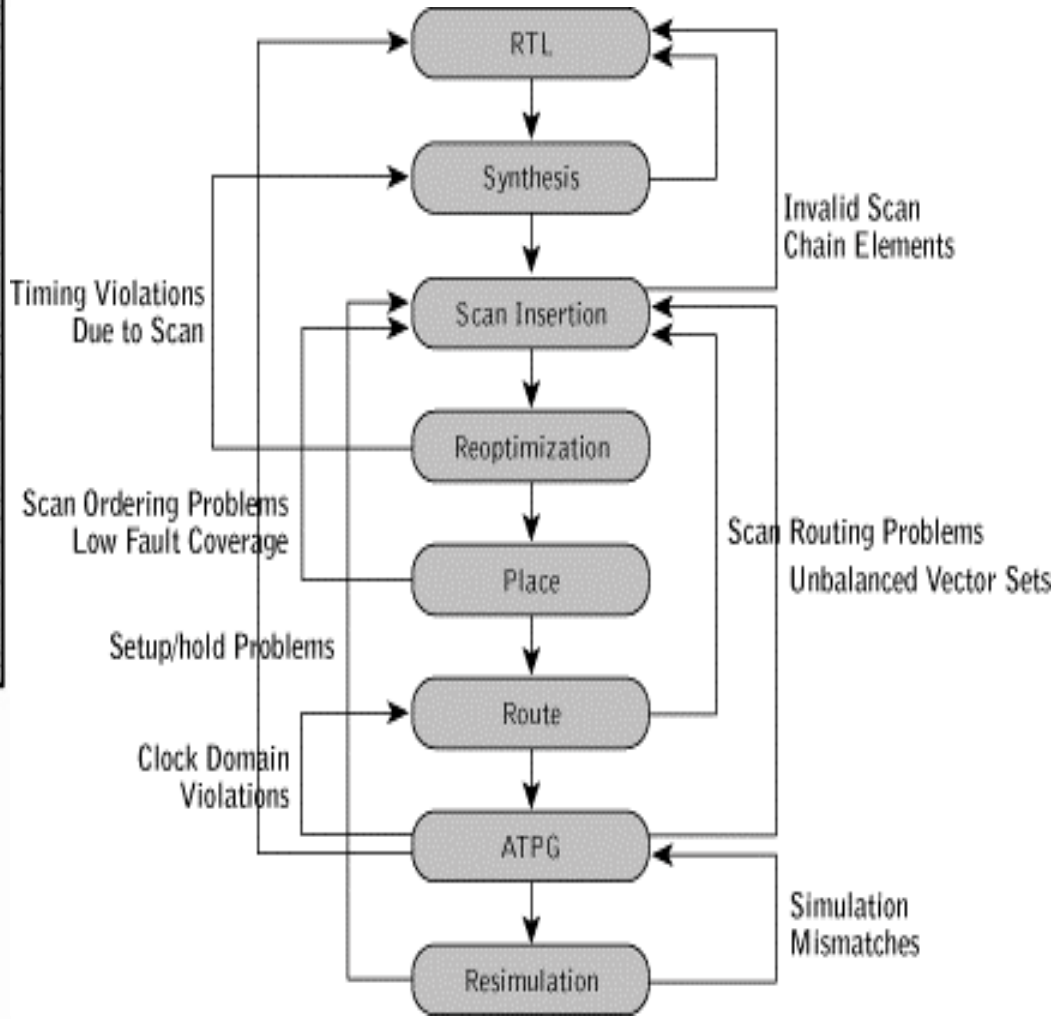
SoC: System on a Chip

- SoC is an enabling technology for embedded systems.
- Embedded systems handle and manipulate large volumes of data in real-time.
- Some Examples: Internet Appliances, PDAs, cell phones, MP3 players, ...



SoC: Design Methodology

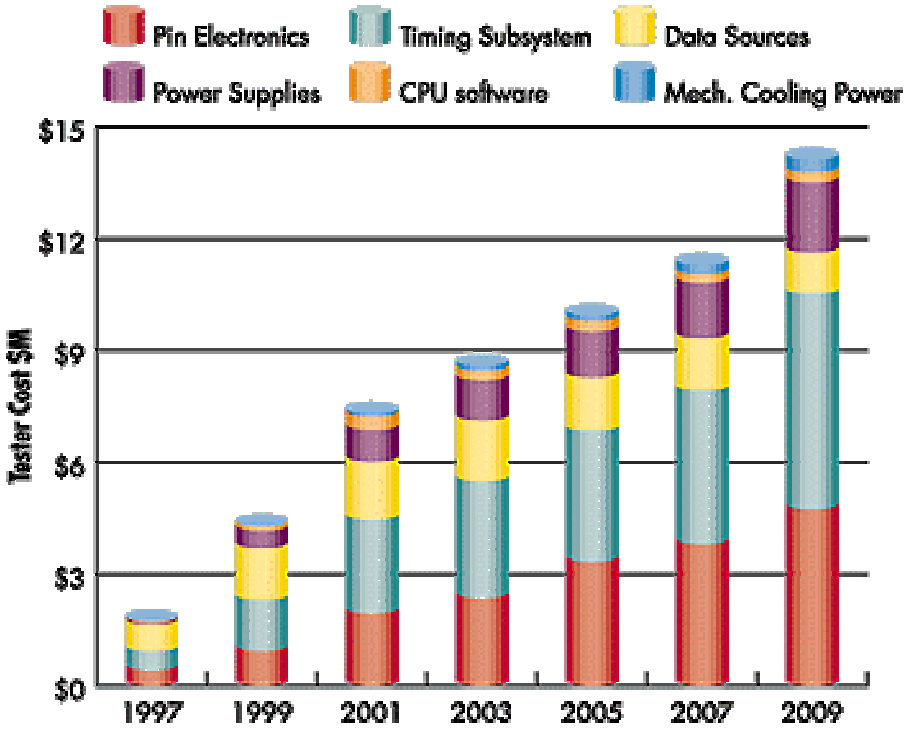




Ref: **www.eedesign.com and www.synopsys.com**

ATE: Automatic Test Equipment

- Several major difficulties arise with SoC chip testing technology based on ATE (automatic test equipment).
- One is the ATE cost that keeps on growing and growing.
- Another serious problem is that ATE speed is behind the chip native speed, and this speed gap keeps increasing.
- A third related problem is that the volume of test data is now very large, especially for large SoCs with many embedded cores.



ATE: Agilent 93000 SoC series

At $1.5k/pin the Agilent 93000 SoC Series Model C200e is the first tester to break the $2k/pin price barrier for SoC test.

ATE Type	C200e	C400	P600	P1000
Max Digital Channel Count	512 - 1024	512 - 1024	512 - 1024	512 - 1024
Max Vector Memory	28M	28M	112M	112M
Maximum Scan Memory/pin	336M	336M	336M	326M
Maximum I/O Data Rate (Mbits/Sec)	200	400	660	1Gb/s
Target Applications	Wafer sort, low end DSPs, baseband wireless devices, ASICs, etc.	PC-Graphics, PC-Chipset, PC133/PC166 & DDR266/ DDR333 memory interfaces, high end DSPs,	Characterization of high-speed ASICs and high-speed communication devices.	Headroom for "at speed" test applications

http://www.ate.agilent.com/ste/products/intelligent_test/SOC_test/descriptions/93000_features.shtml http://www.teradyne.com/prods/icd/products/a5.html

Test Data: Vectors

- Boundary scan (JTAG) test vectors are used to test the wires on circuit board between the chip pins.
- Scan chain test vectors are used to test the internal logic of each embedded system with the chip itself for manufacturing defects.
- Not every bit is required when a test vector is applied to the chip. These bits are labeled as don't cares (X).

Test#	Input/Scan-In Values	Output/Scan-Out Values
1	1 0 X 1 X X X X X X	X X X X 1 X X X X 0 X
2	X 0 1 1 0 1 X X X X	X X X 1 X X X X X X X
...	...	...

Test Data: Don’t Cares

- It is not intuitively obvious how many of these Don’t Cares actually exist.
- *Well, it turns out lots, if you know how to get them!*

ISCAS 89 Benchmark	s420.1	s838.1	s9234.1	s35932
Pseudo Primary Inputs (PPI)	34	66	247	1763
Total number of test vectors	71	154	171	22
Total test set size in bits	2414	10164	42237	38786
Total Don’t Cares in percent	60%	68%	78%	71%
Average Length of DC string	200	400	660	1Gb/s
Maximum Length of DC string	200	200	200	200

Test Data: Compression

- One approach to alleviate these problems is to reduce the volume of test data by using data compression techniques.
- Lempel-Ziv compression (LZ77, LZ78, LZW) schemes are well known in the software world.
- Belong to a family of dictionary-based compression techniques using a sliding text window.
- Software tools that use these techniques successfully are PKZip, GNU gzip, and GIF & PNG image formats.
- Lossless by nature as opposed to other lossy compression techniques used in image compression such as JPEG or MPEG formats.

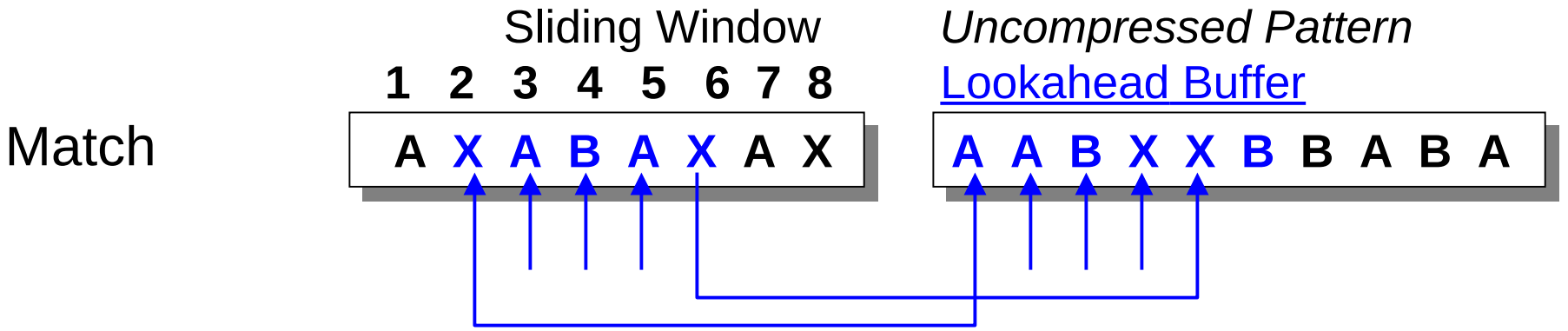
Test Data: Lempel-Ziv Compression

- Not only reduces the size of the data but also reduces the communication time to transfer this reduced data.
- Are finding their way into hardware, specifically embedded systems
- A novel adaptation of the much utilized Lempel-Ziv compression in software as it applies directly to hardware.
- The large presence of don't cares is exploited in uncompressed test sets that we generated using commercial ATPG tools.

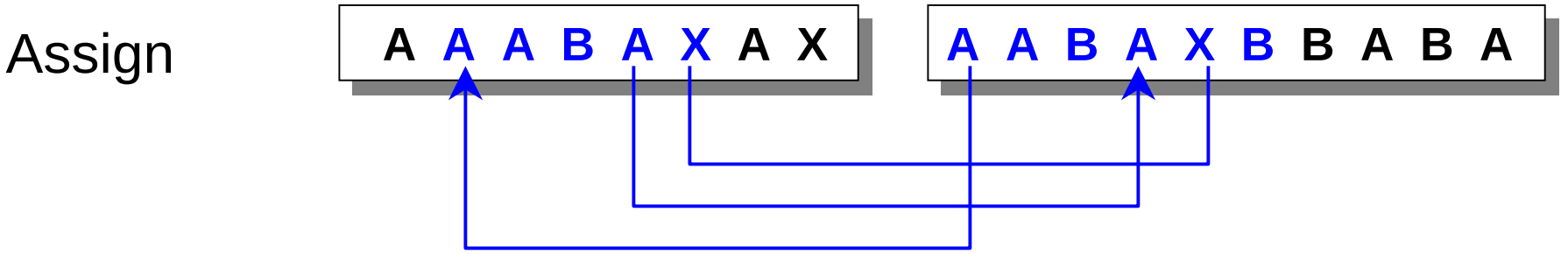
Lempel-Ziv Compression: Example

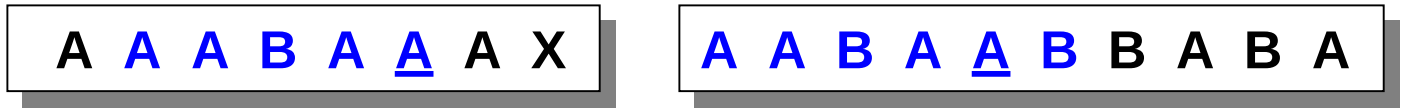
Compressed Pattern	Sliding Window (1 2 3 4 5 6)	*Uncompressed Pattern* Lookahead Buffer
A		A B A B A B A B B A
A B	A	B A B A B A B B A B
A B (5,2)	5 A B	A B A B A B B A B A
A B (5,2) (3,4)	3 A B A B	A B A B B A B A
A B (5,2) (3,4) (2,4)	2 A B A B A B	B A B A
A B (5,2) (3,4) (2,4)	A B B A B A	

Compression: Don’t Care Pattern Matching



- There are several possible matches: AA (1,2,5,6,7), AAB (2), …
- The longest string match is always used





Compression: Size Results

	ISCAS 89 Benchmark			
Window Size	s420.1	s838.1	s9234.1	s35932
16 bits	15%	26%	27%	24%
32	26%	45%	44%	36%
64	28%	52%	52%	42%
128	29%	57%	54%	42%
256	31%	59%	55%	53%
Don’t Cares	60%	68%	78%	71%
Avg. DC	6.8	13.4	9.6	4.3
Test set size	2414	10164	42237	38786

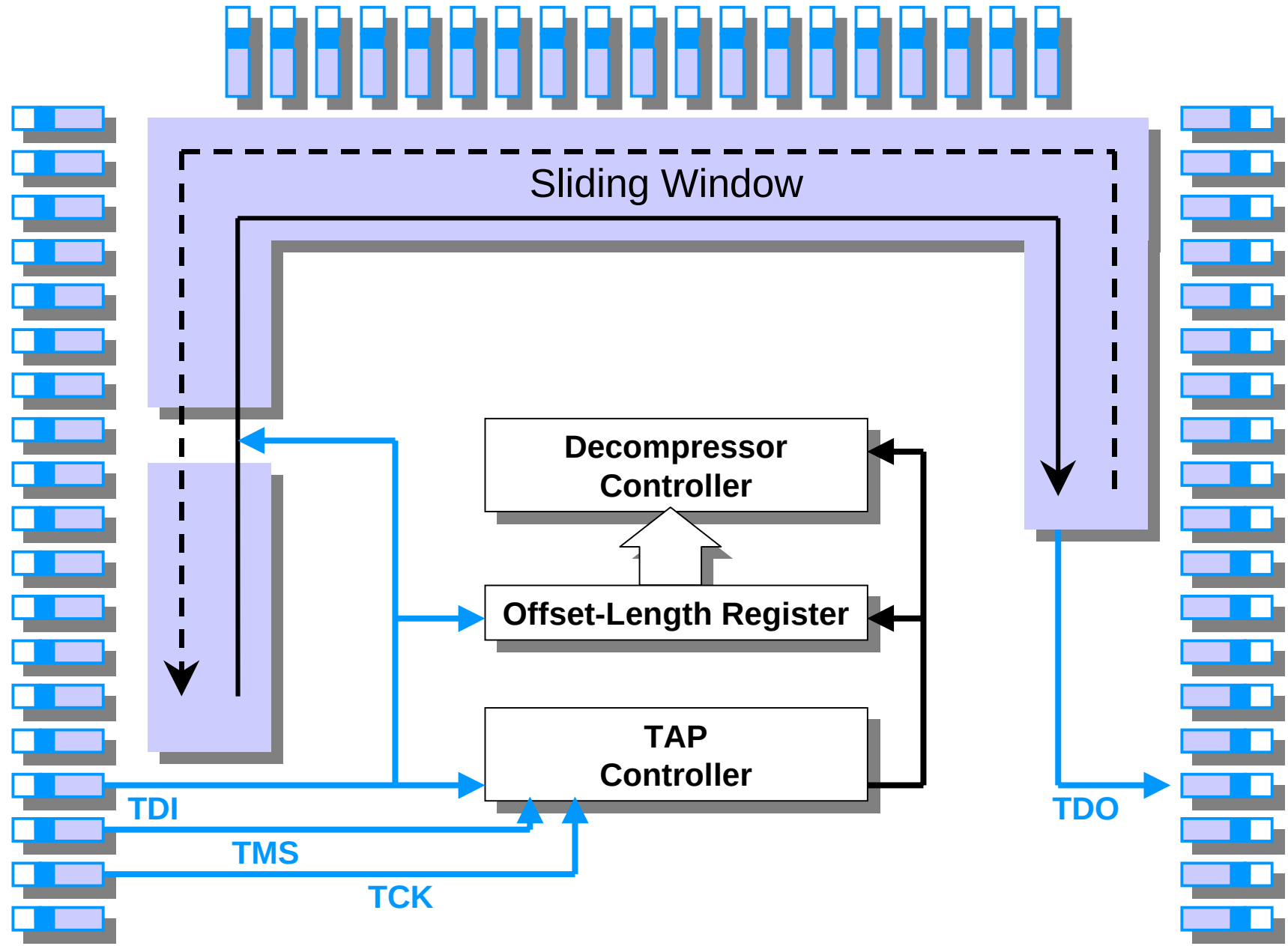
Hardware Test Data Compression: related work

- Run Length Encoding (RLE) schemes have been developed using Golomb codes. (see: Chanda, Date 2001 conference). RLE encoding requires a simple state machine to implement and does give good to fair results.

- Microprocessor implementations of Lempel-Ziv are well know but have poor hardware performance and hence impractical for real time manufacturing testing.

- Other exotic schemes have be proposed (i.e. cycle scan chains) but this methods place a constraint on place & route tools. This constraint hinders the original design performance.

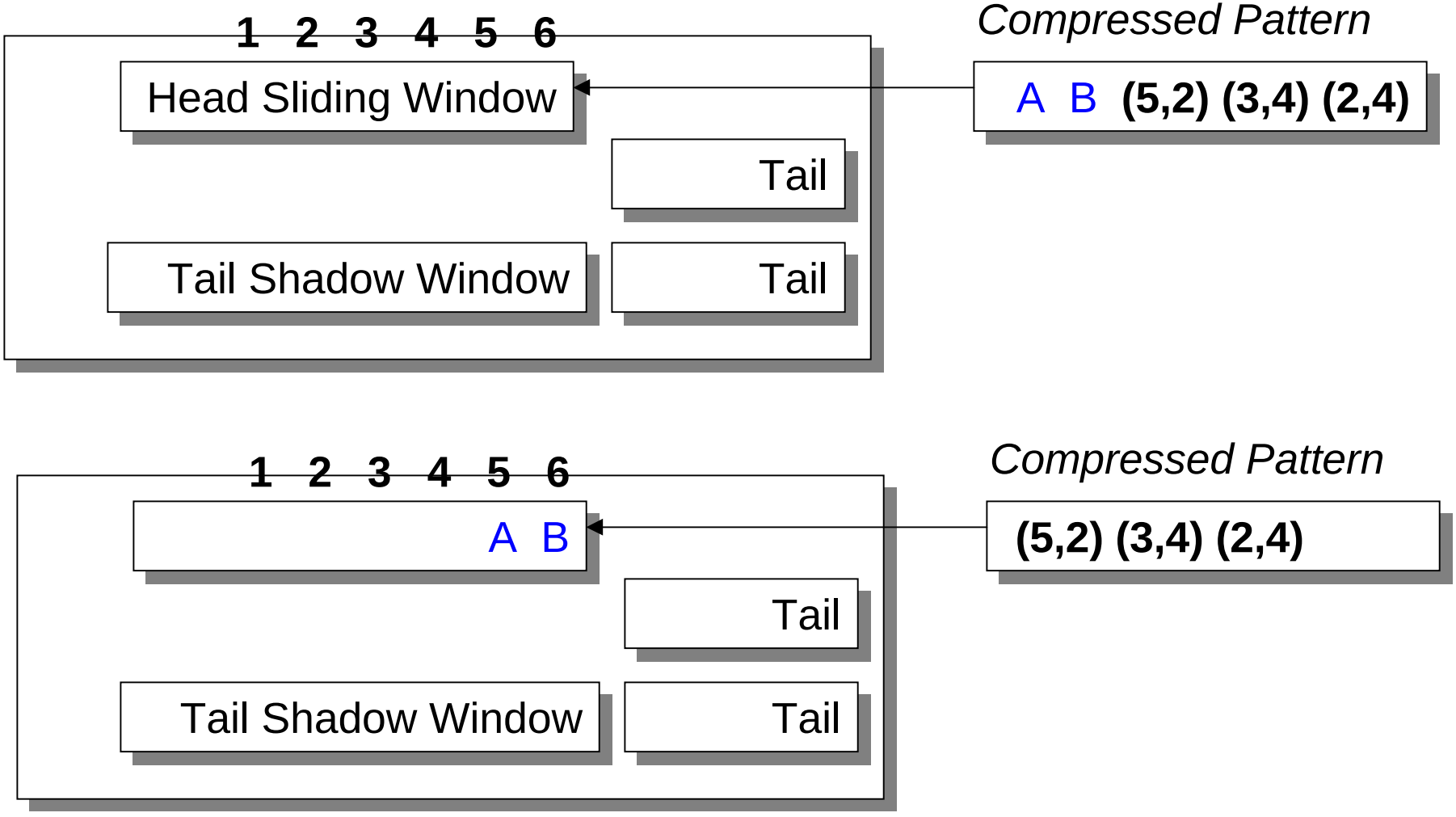
Hardware Decompression: Decompressor



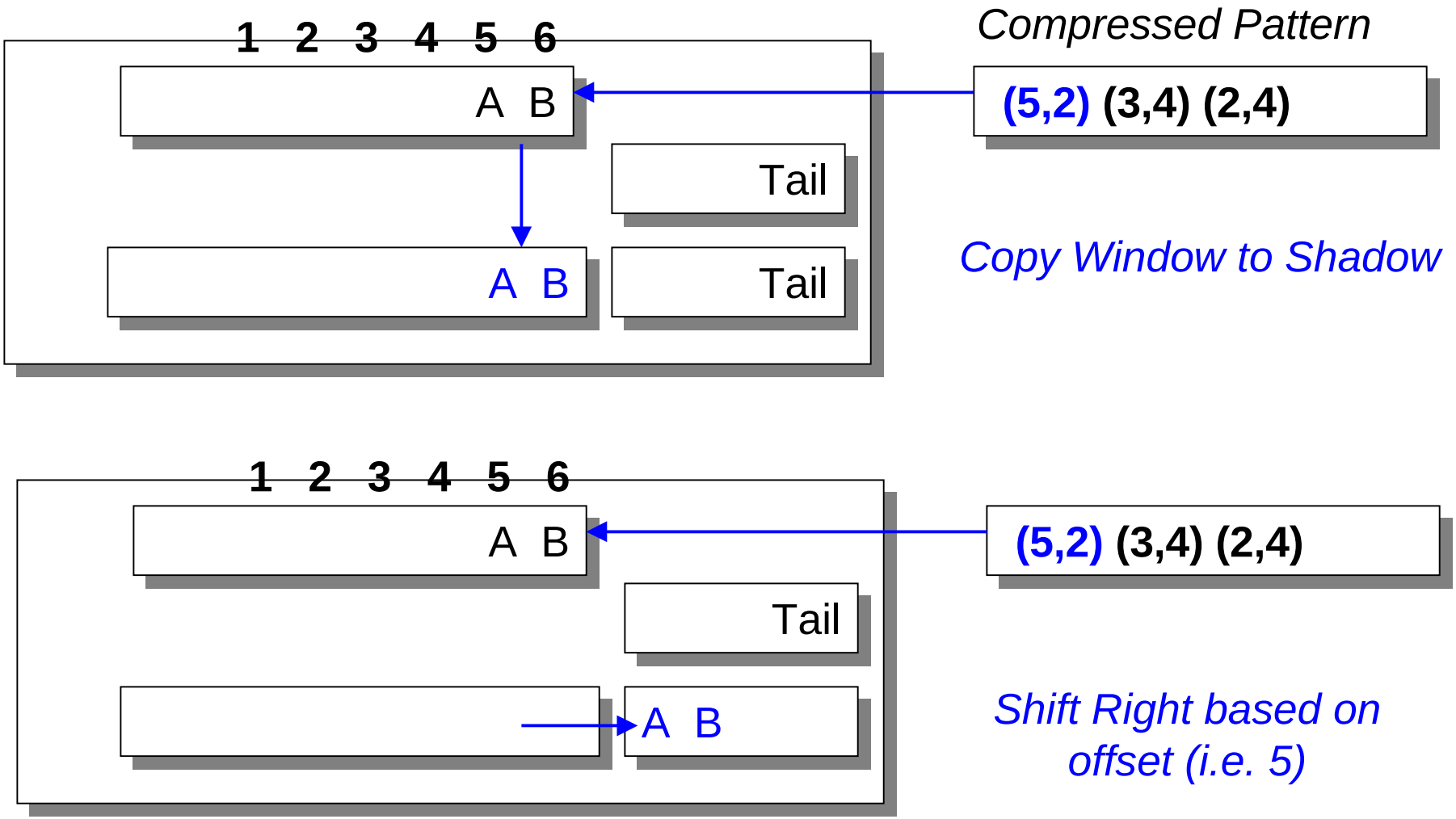
Hardware Decompression: Example a.

Test Data Packets

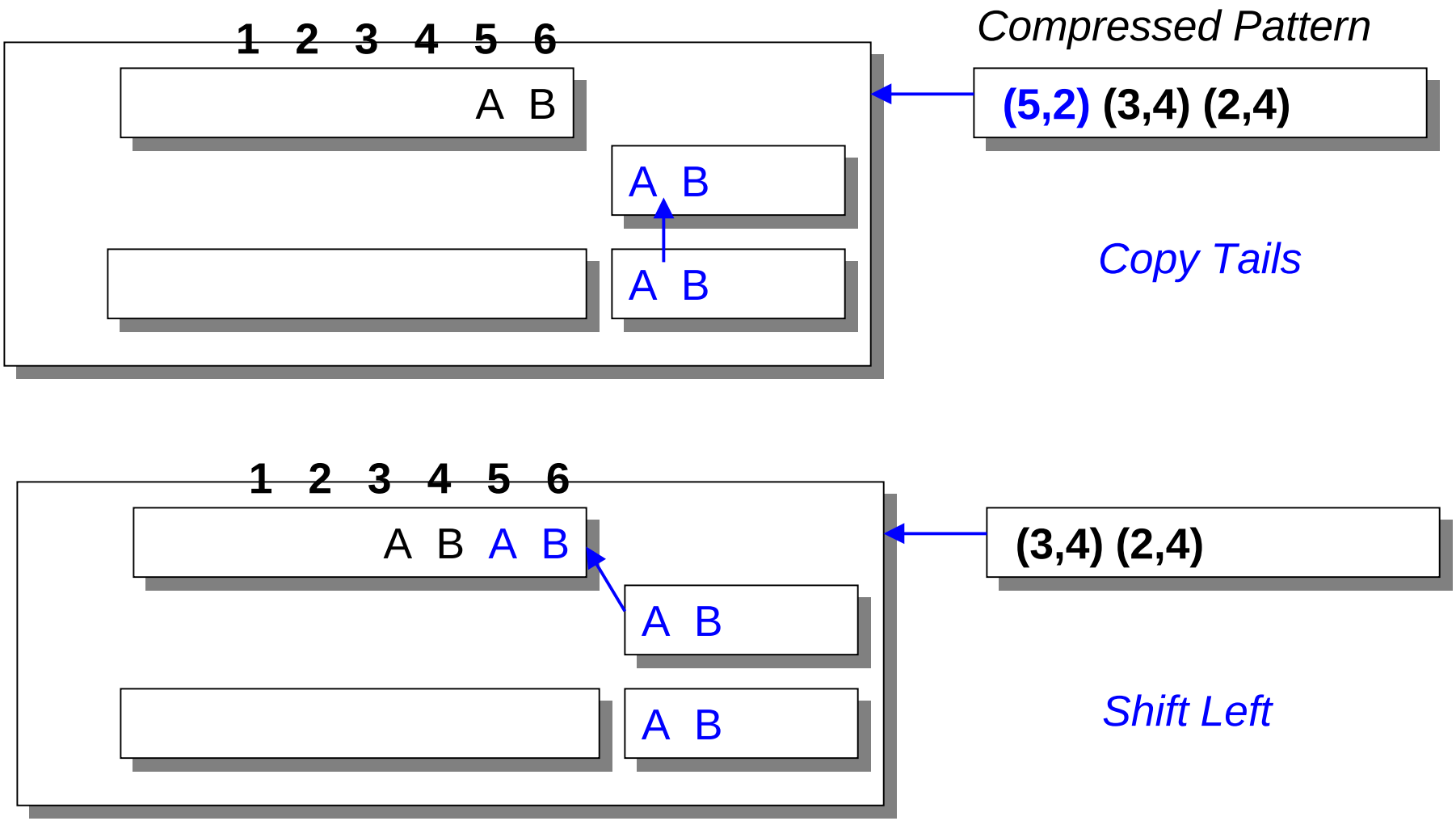
0	Length	Bit string...
1	Offset	Length



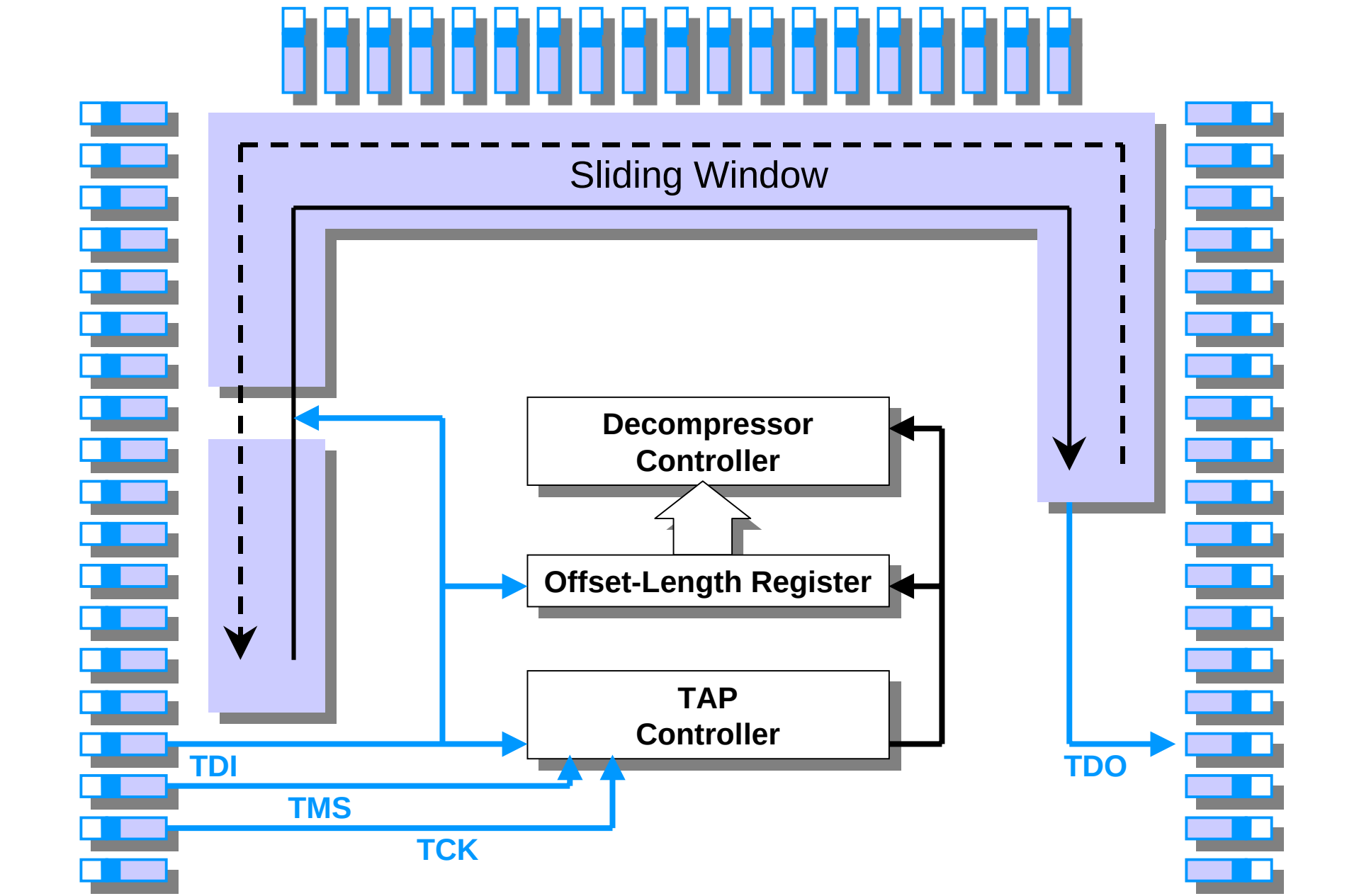
Hardware Decompression: Example b.



Hardware Decompression: Example c.



Hardware Decompression: Review Decompressor

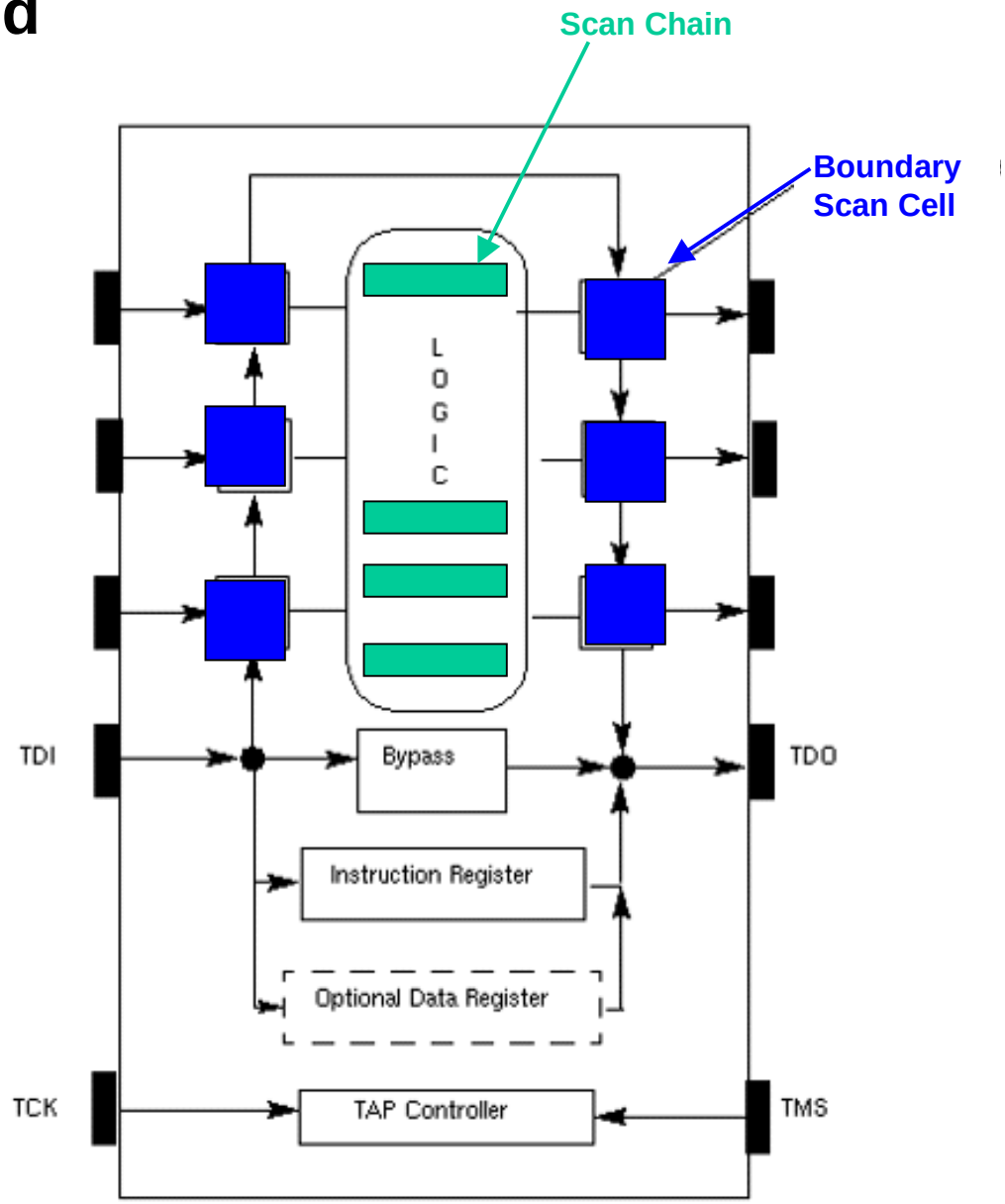


Hardware Decompression: JTAG

Boundary scan **(JTAG) is used to test the wires on circuit board between the chip pins.**

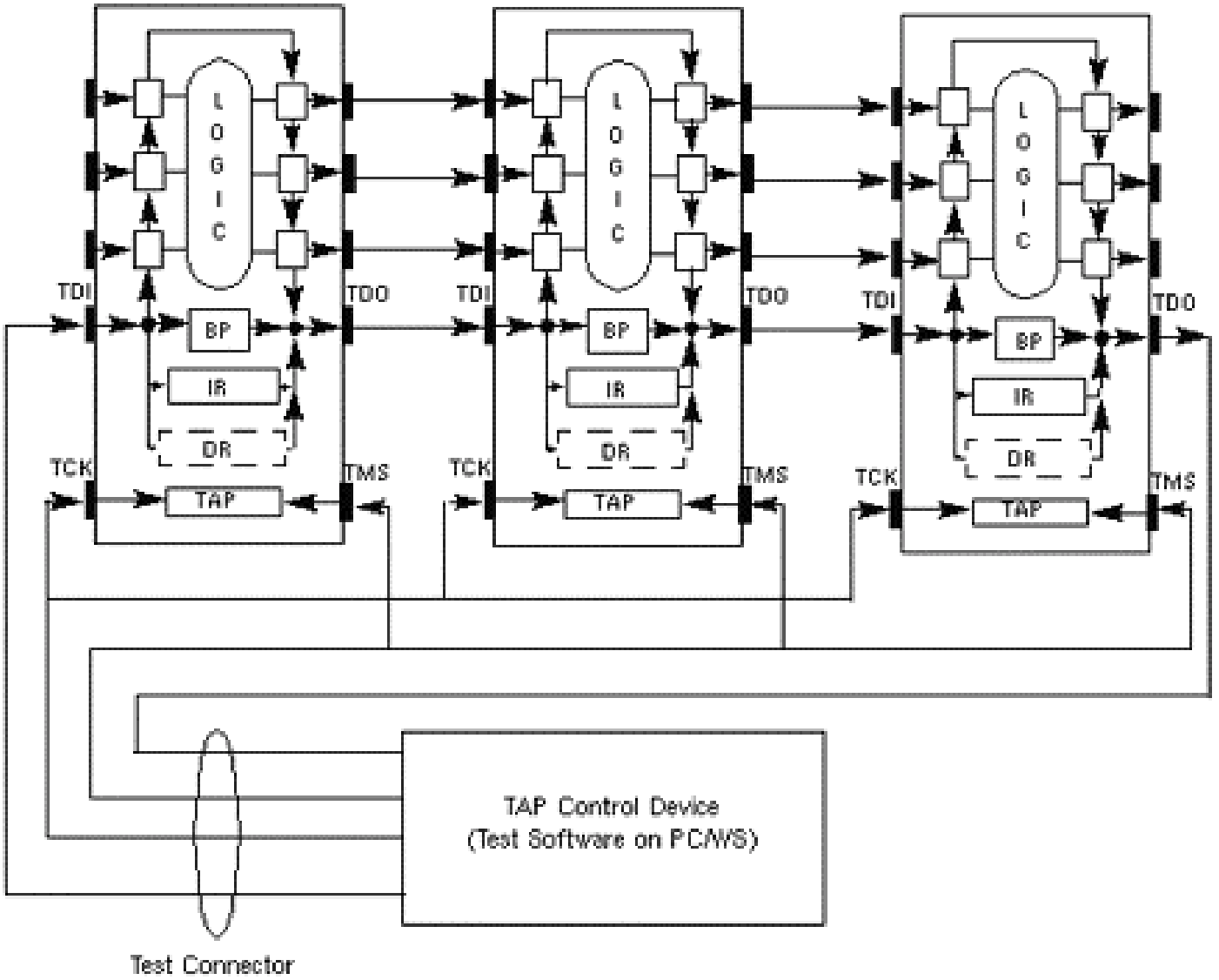
Scan Chains **are used to test the internal logic of each embedded system with the chip itself.**

In order to further reduce the hardware decompressor chip area overhead, we enhance the existing JTAG boundary scan cell already connected to SoC pins feeding the internal test scan chain.

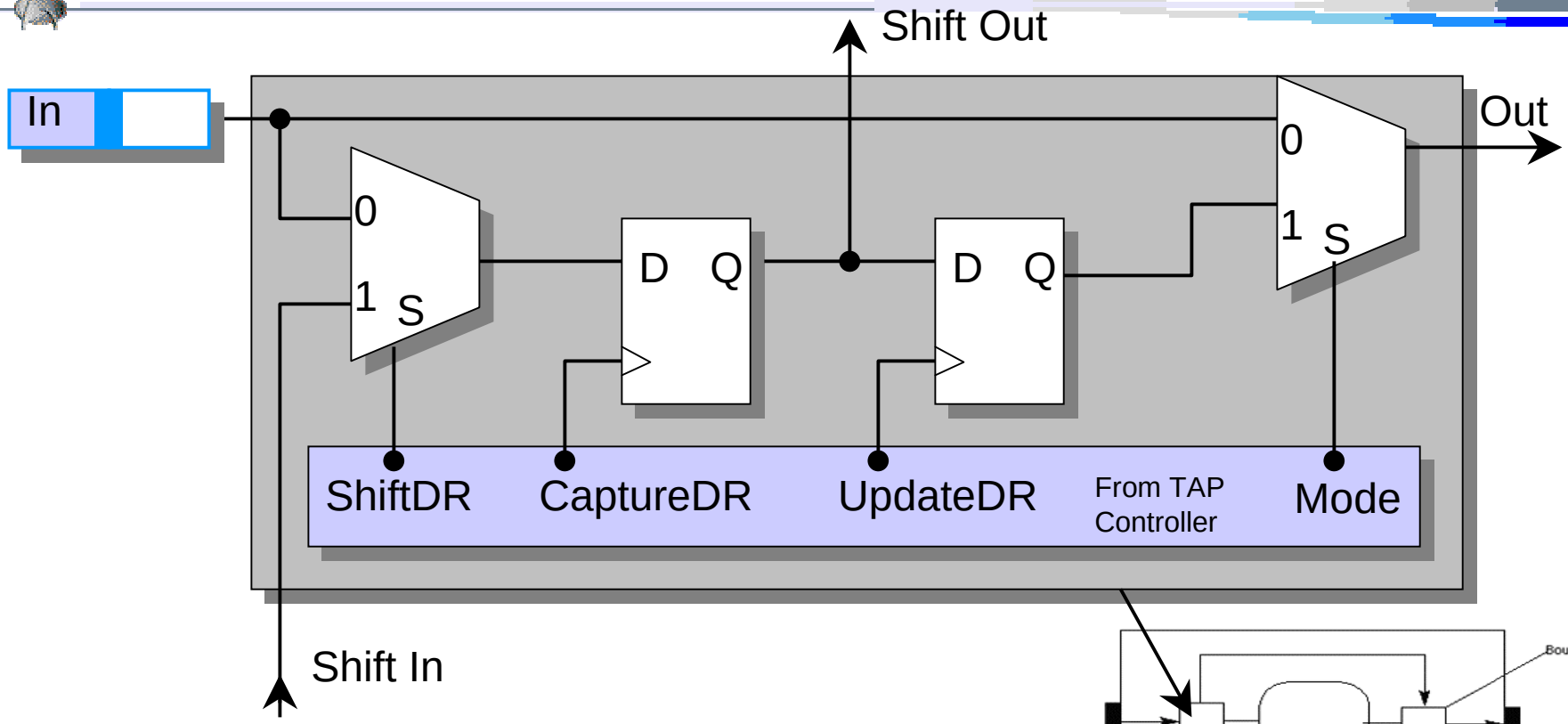


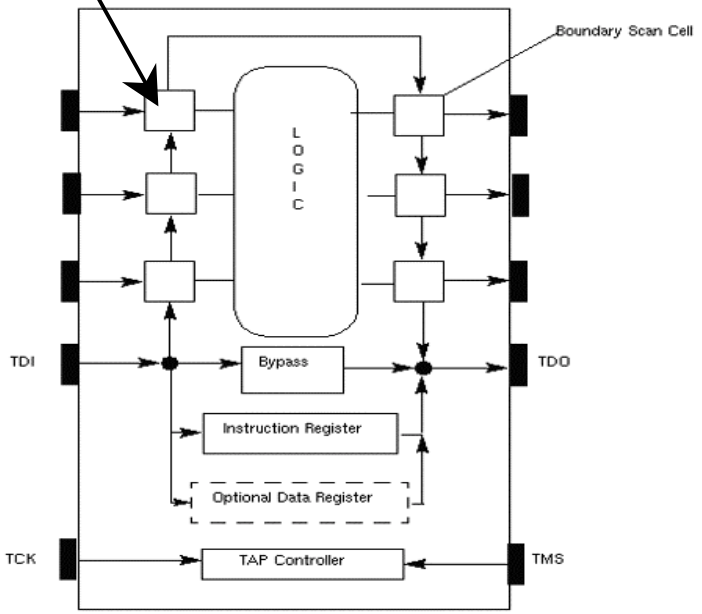
http://www.sun.com/microelectronics/whitepapers/wpr-0018-01/

Hardware Decompression: JTAG

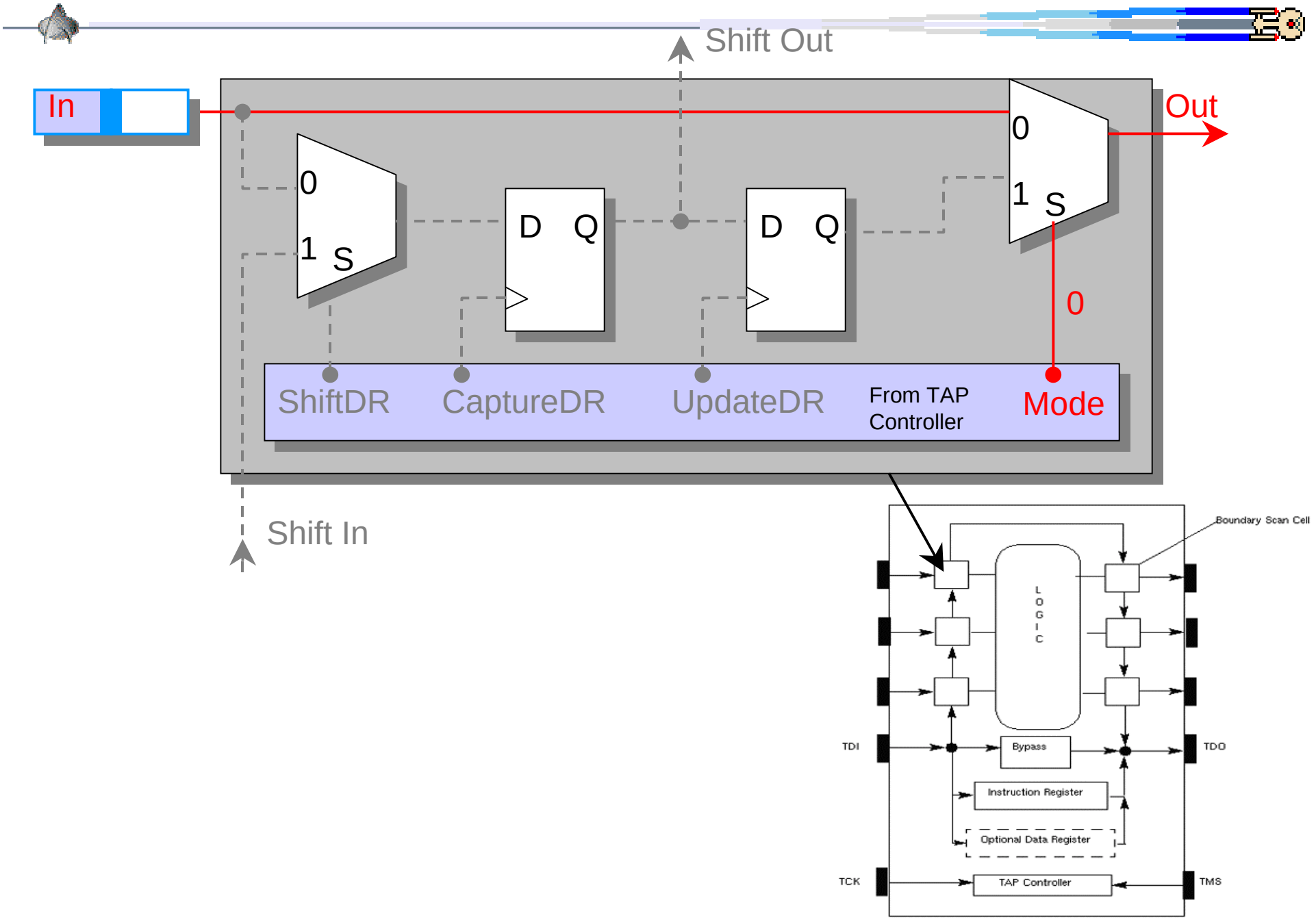


JTAG cell: input

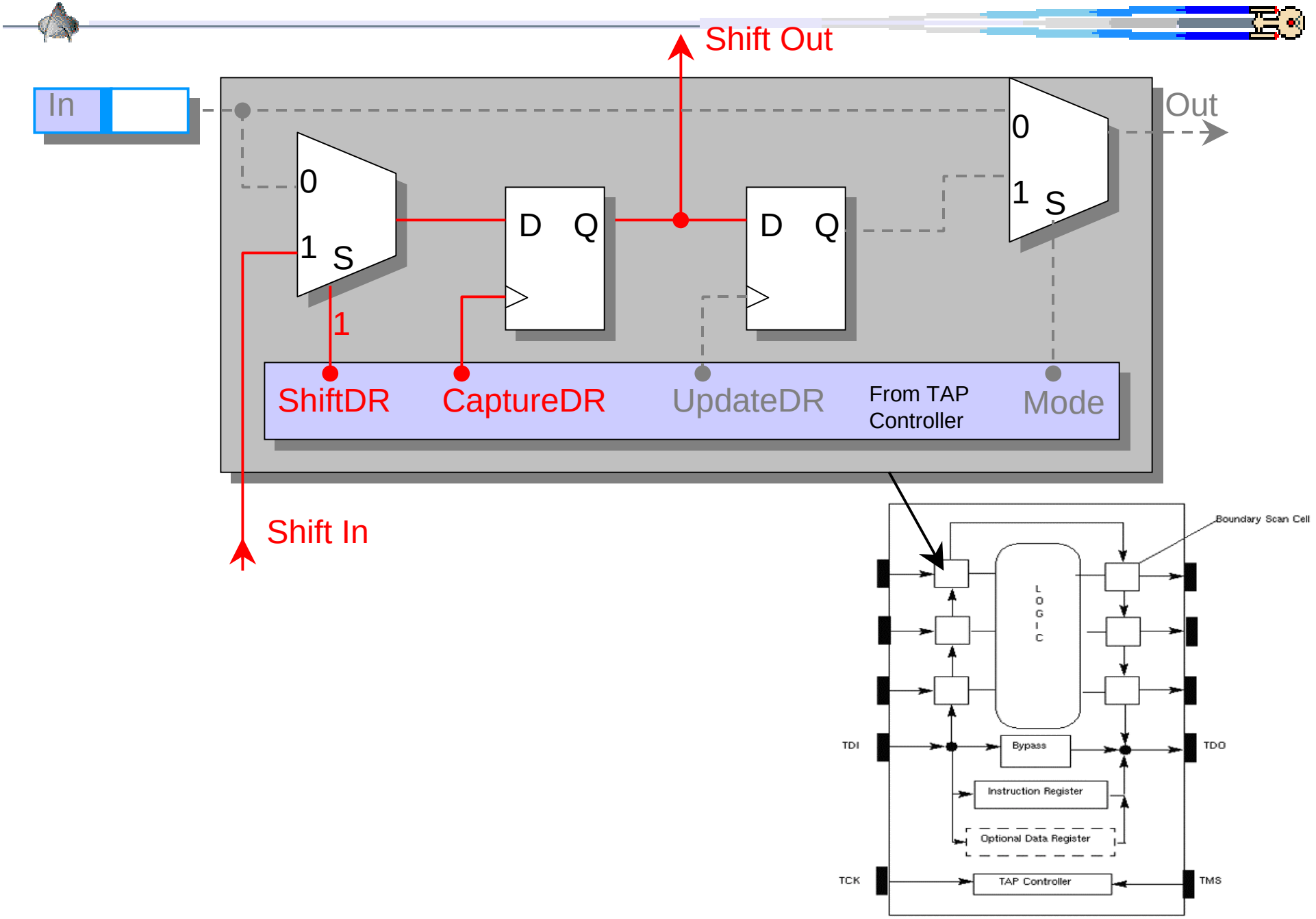




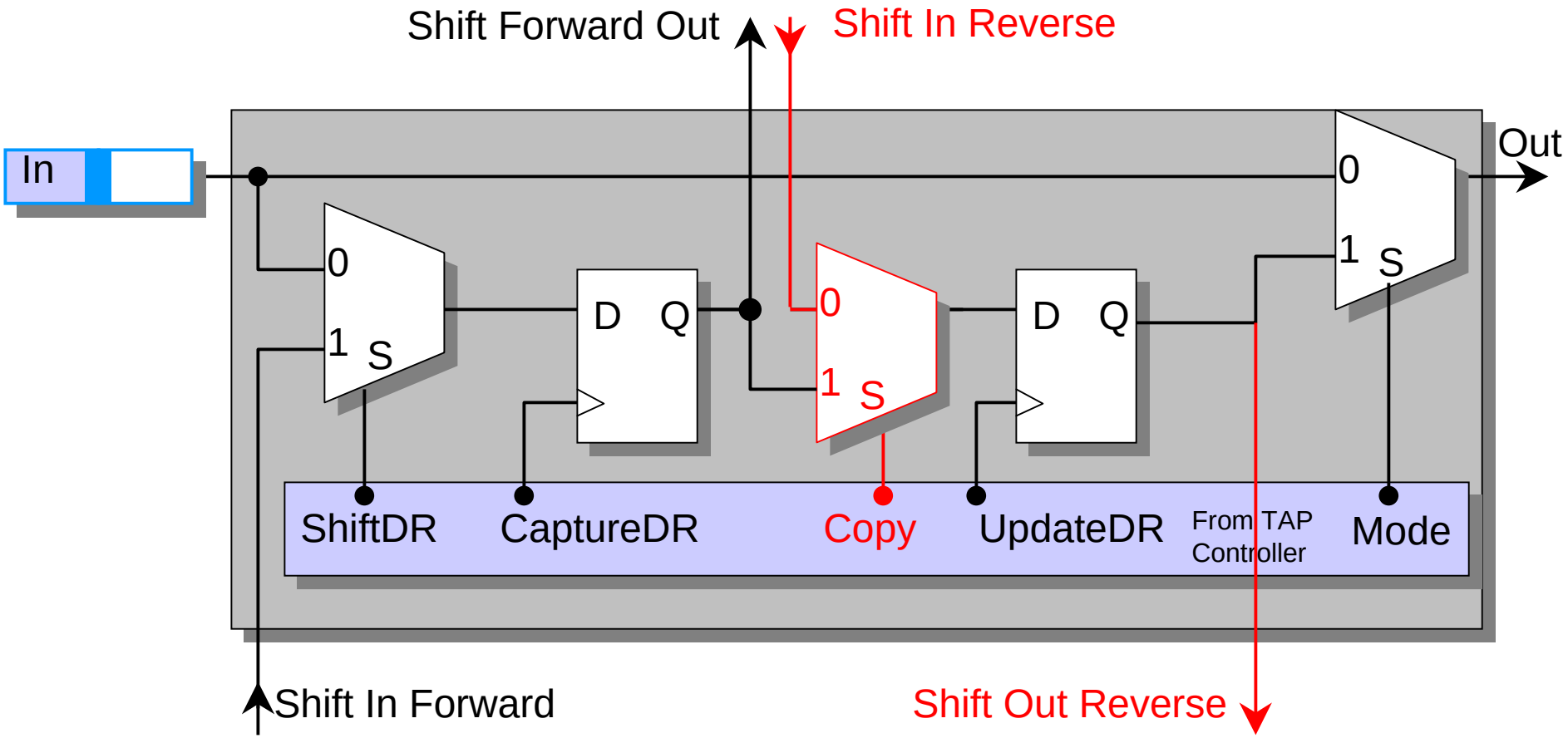
JTAG cell: normal input mode



JTAG cell: Shift mode



JTAG cell: modified



Compression: Timing Results

Tradeoff between decompress time and compression ratio.

	ISCAS 89 Benchmark			
Window Size	s420.1	s838.1	s9234.1	s35932
Minimum time — 16 bits	*2984*	*11764*	*49132*	46107
32	3412	12415	51771	49896
64	4540	14663	60738	*41793*
128	6517	19494	83222	55386
Best Size Compression — **256**	**10517**	**28533**	**118634**	**81772**
Don't Cares	**60%**	**68%**	**78%**	**71%**
Avg. DC	**6.8**	**13.4**	**9.6**	**4.3**
Test set size	**2414**	**10164**	**42237**	**38786**

Conclusions & future work.

- A new test data compression method was presented based on Lempel-Ziv compression for bit strings rather than character sets.
- High compression ratio are due to the heavy exploitation of Don’t Cares in the test data sets.
- An efficient hardware decompressor with minimal area overhead was presented using a modified boundary scan cell.
- Future work will extend this scheme to multi--scan chains.