The Art of ANALOG LAYOUT
Second Edition

Alan Hastings

PEARSON
Prentice
Hall

Pearson Education International

Contents

Preface to the Second Edition xvii
Preface to the First Edition xix
Acknowledgments xxi

1 *Device Physics 1*
- 1.1 Semiconductors 1
  - 1.1.1. Generation and Recombination 4
  - 1.1.2. Extrinsic Semiconductors 6
  - 1.1.3. Diffusion and Drift 9
- 1.2 PN Junctions 11
  - 1.2.1. Depletion Regions 11
  - 1.2.2. PN Diodes 13
  - 1.2.3. Schottky Diodes 16
  - 1.2.4. Zener Diodes 18
  - 1.2.5. Ohmic Contacts 19
- 1.3 Bipolar Junction Transistors 21
  - 1.3.1. Beta 23
  - 1.3.2. I-V Characteristics 24
- 1.4 MOS Transistors 25
  - 1.4.1. Threshold Voltage 27
  - 1.4.2. I-V Characteristics 29
- 1.5 JFET Transistors 32
- 1.6 Summary 34
- 1.7 Exercises 35

2 *Semiconductor Fabrication 37*
- 2.1 Silicon Manufacture 37
  - 2.1.1. Crystal Growth 38
  - 2.1.2. Wafer Manufacturing 39
  - 2.1.3. The Crystal Structure of Silicon 39
- 2.2 Photolithography 41
  - 2.2.1. Photoresists 41
  - 2.2.2. Photomasks and Reticles 42
  - 2.2.3. Patterning 43
- 2.3 Oxide Growth and Removal 43
  - 2.3.1. Oxide Growth and Deposition 44
  - 2.3.2. Oxide Removal 45
  - 2.3.3. Other Effects of Oxide Growth and Removal 47
  - 2.3.4. Local Oxidation of Silicon (LOCOS) 49
- 2.4 Diffusion and Ion Implantation 50
  - 2.4.1. Diffusion 51
  - 2.4.2. Other Effects of Diffusion 53
  - 2.4.3. Ion Implantation 55

2.5 Silicon Deposition and Etching 57
  2.5.1. Epitaxy 57
  2.5.2. Polysilicon Deposition 59
  2.5.3. Dielectric Isolation 60
2.6 Metallization 62
  2.6.1. Deposition and Removal of Aluminum 63
  2.6.2. Refractory Barrier Metal 65
  2.6.3. Silicidation 67
  2.6.4. Interlevel Oxide, Interlevel Nitride, and Protective Overcoat 69
  2.6.5. Copper Metallization 71
2.7 Assembly 73
  2.7.1. Mount and Bond 74
  2.7.2. Packaging 77
2.8 Summary 78
2.9 Exercises 78

3 *Representative Processes 80*
3.1 Standard Bipolar 81
  3.1.1. Essential Features 81
  3.1.2. Fabrication Sequence 82
    Starting Material 82
    N-Buried Layer 82
    Epitaxial Growth 83
    Isolation Diffusion 83
    Deep-N+ 83
    Base Implant 84
    Emitter Diffusion 84
    Contact 85
    Metallization 85
    Protective Overcoat 86
  3.1.3. Available Devices 86
    NPN Transistors 86
    PNP Transistors 88
    Resistors 90
    Capacitors 92
  3.1.4. Process Extensions 93
    Up-Down Isolation 93
    Double-Level Metal 94
    Schottky Diodes 94
    High-Sheet Resistors 94
    Super-Beta Transistors 96
3.2 Polysilicon-Gate CMOS 96
  3.2.1. Essential Features 97
  3.2.2. Fabrication Sequence 98
    Starting Material 98
    Epitaxial Growth 98
    N-Well Diffusion 98
    Inverse Moat 99
    Channel Stop Implants 100
    LOCOS Processing and Dummy Gate Oxidation 100
    Threshold Adjust 101

Polysilicon Deposition and Patterning 102
Source/Drain Implants 102
Contacts 103
Metallization 103
Protective Overcoat 103
3.2.3. Available Devices 104
NMOS Transistors 104
PMOS Transistors 106
Substrate PNP Transistors 107
Resistors 107
Capacitors 109
3.2.4. Process Extensions 109
Double-Level Metal 110
Shallow Trench Isolation 110
Silicidation 111
Lightly Doped Drain (LDD) Transistors 112
Extended-Drain, High-Voltage Transistors 113
3.3 Analog BiCMOS 114
3.3.1. Essential Features 115
3.3.2. Fabrication Sequence 116
Starting Material 116
N-Buried Layer 116
Epitaxial Growth 117
N-Well Diffusion and Deep-N+ 117
Base Implant 118
Inverse Moat 118
Channel Stop Implants 119
LOCOS Processing and Dummy Gate Oxidation 119
Threshold Adjust 119
Polysilicon Deposition and Pattern 120
Source/Drain Implants 120
Metallization and Protective Overcoat 120
Process Comparison 121
3.3.3. Available Devices 121
NPN Transistors 121
PNP Transistors 123
Resistors 125
3.3.4. Process Extensions 125
Advanced Metal Systems 126
Dielectric Isolation 126
3.4 Summary 130
3.5 Exercises 131

4 *Failure Mechanisms 133*
4.1 Electrical Overstress 133
4.1.1. Electrostatic Discharge (ESD) 134
Effects 135
Preventative Measures 135
4.1.2. Electromigration 136
Effects 136
Preventative Measures 137

- 4.1.3. Dielectric Breakdown 138
  - *Effects 138*
  - *Preventative Measures 139*
- 4.1.4. The Antenna Effect 141
  - *Effects 141*
  - *Preventative Measures 142*
- 4.2 Contamination 143
  - 4.2.1. Dry Corrosion 144
    - *Effects 144*
    - *Preventative Measures 145*
  - 4.2.2. Mobile Ion Contamination 145
    - *Effects 145*
    - *Preventative Measures 146*
- 4.3 Surface Effects 148
  - 4.3.1. Hot Carrier Injection 148
    - *Effects 148*
    - *Preventative Measures 150*
  - 4.3.2. Zener Walkout 151
    - *Effects 151*
    - *Preventative Measures 152*
  - 4.3.3. Avalanche-Induced Beta Degradation 153
    - *Effects 153*
    - *Preventative Measures 154*
  - 4.3.4. Negative Bias Temperature Instability 154
    - *Effects 155*
    - *Preventative Measures 155*
  - 4.3.5. Parasitic Channels and Charge Spreading 156
    - *Effects 156*
    - *Preventative Measures (Standard Bipolar) 159*
    - *Preventative Measures (CMOS and BiCMOS) 162*
- 4.4 Parasitics 164
  - 4.4.1. Substrate Debiasing 165
    - *Effects 166*
    - *Preventative Measures 167*
  - 4.4.2. Minority-Carrier Injection 169
    - *Effects 169*
    - *Preventative Measures (Substrate Injection) 172*
    - *Preventative Measures (Cross-Injection) 178*
  - 4.4.3. Substrate Influence 180
    - *Effects 180*
    - *Preventative Measures 180*
- 4.5 Summary 183
- 4.6 Exercises 183

5 *Resistors 185*

- 5.1 Resistivity and Sheet Resistance 185
- 5.2 Resistor Layout 187
- 5.3 Resistor Variability 191
  - 5.3.1. Process Variation 191
  - 5.3.2. Temperature Variation 192

        5.3.3. Nonlinearity 193
        5.3.4. Contact Resistance 196
    5.4 Resistor Parasitics 197
    5.5 Comparison of Available Resistors 200
        5.5.1. Base Resistors 200
        5.5.2. Emitter Resistors 201
        5.5.3. Base Pinch Resistors 202
        5.5.4. High-Sheet Resistors 202
        5.5.5. Epi Pinch Resistors 205
        5.5.6. Metal Resistors 206
        5.5.7. Poly Resistors 208
        5.5.8. NSD and PSD Resistors 211
        5.5.9. N-Well Resistors 211
        5.5.10. Thin-Film Resistors 212
    5.6 Adjusting Resistor Values 213
        5.6.1. Tweaking Resistors 213
            Sliding Contacts 214
            Sliding Heads 215
            Trombone Slides 215
            Metal Options 215
        5.6.2. Trimming Resistors 216
            Fuses 216
            Zener Zaps 219
            EPROM Trims 221
            Laser Trims 222
    5.7 Summary 223
    5.8 Exercises 224

6 *Capacitors and Inductors 226*

    6.1 Capacitance 226
        6.1.1. Capacitor Variability 232
            Process Variation 232
            Voltage Modulation and Temperature Variation 233
        6.1.2. Capacitor Parasitics 235
        6.1.3. Comparison of Available Capacitors 237
            Base-Emitter Junction Capacitors 237
            MOS Capacitors 239
            Poly-Poly Capacitors 241
            Stack Capacitors 243
            Lateral Flux Capacitors 245
            High-Permittivity Capacitors 246
    6.2 Inductance 246
        6.2.1. Inductor Parasitics 248
        6.2.2. Inductor Construction 250
            Guidelines for Integrating Inductors 251
    6.3 Summary 252
    6.4 Exercises 253

7 *Matching of Resistors and Capacitors 254*

    7.1 Measuring Mismatch 254

7.2 Causes of Mismatch 257
    7.2.1. Random *Variation* 257
        Capacitors 258
        Resistors 258
    7.2.2. Process Biases 260
    7.2.3. Interconnection Parasitics 261
    7.2.4. Pattern Shift 263
    7.2.5. Etch Rate Variations 265
    7.2.6. Photolithographic Effects 267
    7.2.7. Diffusion Interactions 268
    7.2.8. Hydrogenation 270
    7.2.9. Mechanical Stress and Package Shift 271
    7.2.10. Stress Gradients 274
        Piezoresistivity 274
        Gradients and Centroids 275
        Common-Centroid Layout 277
        Location and Orientation 281
    7.2.11. Temperature Gradients and Thermoelectrics 283
        Thermal Gradients 285
        Thermoelectric Effects 287
    7.2.12. Electrostatic Interactions 288
        Voltage Modulation 288
        Charge Spreading 292
        Dielectric Polarization 293
        Dielectric Relaxation 294
7.3 Rules for Device Matching 295
    7.3.1. Rules for Resistor Matching 296
    7.3.2. Rules for Capacitor Matching 300
7.4 Summary 303
7.5 Exercises 304

8 *Bipolar Transistors 306*
8.1 Topics in Bipolar Transistor Operation 306
    8.1.1. Beta Rolloff 308
    8.1.2. Avalanche Breakdown 308
    8.1.3. Thermal Runaway and Secondary Breakdown 310
    8.1.4. Saturation in NPN Transistors 312
    8.1.5. Saturation in Lateral PNP Transistors 315
    8.1.6. Parasitics of Bipolar Transistors 318
8.2 Standard Bipolar Small-Signal Transistors 320
    8.2.1. The Standard Bipolar NPN Transistor 320
        Construction of Small-Signal NPN Transistors 322
    8.2.2. The Standard Bipolar Substrate PNP Transistor 326
        Construction of Small-Signal Substrate PNP Transistors 328
    8.2.3. The Standard Bipolar Lateral PNP Transistor 330
        Construction of Small-Signal Lateral PNP Transistors 332
    8.2.4. High-Voltage Bipolar Transistors 337
    8.2.5. Super-Beta NPN Transistors 340
8.3 CMOS and BiCMOS Small-Signal Bipolar Transistors 341
    8.3.1. CMOS PNP Transistors 341
    8.3.2. Shallow-Well Transistors 345

- 8.3.3. Analog BiCMOS Bipolar Transistors 347
- 8.3.4. Fast Bipolar Transistors 349
- 8.3.5. Polysilicon-Emitter Transistors 351
- 8.3.6. Oxide-Isolated Transistors 354
- 8.3.7. Silicon-Germanium Transistors 356

8.4 Summary 358
8.5 Exercises 358

9 *Applications of Bipolar Transistors 360*

9.1 Power Bipolar Transistors 361
- 9.1.1. Failure Mechanisms of NPN Power Transistors 362
  - *Emitter Debiasing 362*
  - *Thermal Runaway and Secondary Breakdown 364*
  - *Kirk Effect 366*
- 9.1.2. Layout of Power NPN Transistors 368
  - *The Interdigitated-Emitter Transistor 369*
  - *The Wide-Emitter Narrow-Contact Transistor 371*
  - *The Christmas-Tree Device 372*
  - *The Cruciform-Emitter Transistor 373*
  - *Power Transistor Layout in Analog BiCMOS 374*
  - *Selecting a Power Transistor Layout 376*
- 9.1.3. Power PNP Transistors 376
- 9.1.4. Saturation Detection and Limiting 378

9.2 Matching Bipolar Transistors 381
- 9.2.1. Random Variations 382
- 9.2.2. Emitter Degeneration 384
- 9.2.3. NBL Shadow 386
- 9.2.4. Thermal Gradients 387
- 9.2.5. Stress Gradients 391
- 9.2.6. Filler-Induced Stress 393
- 9.2.7. Other Causes of Systomatic Mismatch 395

9.3 Rules for Bipolar Transistor Matching 396
- 9.3.1. Rules for Matching Vertical Transistors 397
- 9.3.2. Rules for Matching Lateral Transistors 402

9.4 Summary 402
9.5 Exercises 403

10 *Diodes 406*

10.1 Diodes in Standard Bipolar 406
- 10.1.1. Diode-Connected Transistors 406
- 10.1.2. Zener Diodes 409
  - *Surface Zener Diodes 410*
  - *Buried Zeners 412*
- 10.1.3. Schottky Diodes 415
- 10.1.4. Power Diodes 420

10.2 Diodes in CMOS and BiCMOS Processes 422
- 10.2.1. CMOS Junction Diodes 422
- 10.2.2. CMOS and BiCMOS Schottky Diodes 423

10.3 Matching Diodes 425
- 10.3.1. Matching PN Junction Diodes 425

        10.3.2. Matching Zener Diodes 426
        10.3.3. Matching Schottky Diodes 428
    10.4 Summary 428
    10.5 Exercises 429

11 *Field-Effect Transistors 430*

- 11.1 Topics in MOS Transistor Operation 431
  - 11.1.1. Modeling the MOS Transistor 431
    - *Device Transconductance 432*
    - *Threshold Voltage 434*
  - 11.1.2. Parasitics of MOS Transistors 438
    - *Breakdown Mechanisms 440*
    - *CMOS Latchup 442*
    - *Leakage Mechanisms 443*
- 11.2 Constructing CMOS Transistors 446
  - 11.2.1. Coding the MOS Transistor 447
    - *Width and Length 448*
  - 11.2.2. N-Well and P-Well Processes 449
  - 11.2.3. Channel Stop Implants 452
  - 11.2.4. Threshold Adjust Implants 453
  - 11.2.5. Scaling the Transistor 456
  - 11.2.6. Variant Structures 459
    - *Serpentine Transistors 461*
    - *Annular Transistors 462*
  - 11.2.7. Backgate Contacts 464
- 11.3 Floating-Gate Transistors 467
  - 11.3.1. Principles of Floating-Gate Transistor Operation 469
  - 11.3.2. Single-Poly EEPROM Memory 472
- 11.4 The JFET Transistor 474
  - 11.4.1. Modeling the JFET 474
  - 11.4.2. JFET Layout 476
- 11.5 Summary 479
- 11.6 Exercises 479

12 *Applications of MOS Transistors 482*

- 12.1 Extended-Voltage Transistors 482
  - 12.1.1. LDD and DDD Transistors 483
  - 12.1.2. Extended-Drain Transistors 486
    - *Extended-Drain NMOS Transistors 487*
    - *Extended-Drain PMOS Transistors 488*
  - 12.1.3. Multiple Gate Oxides 489
- 12.2 Power MOS Transistors 491
  - 12.2.1. MOS Safe Operating Area 492
    - *Electrical SOA 493*
    - *Electrothermal SOA 496*
    - *Rapid Transient Overload 497*
  - 12.2.2. Conventional MOS Power Transistors 498
    - *The Rectangular Device 499*
    - *The Diagonal Device 500*
    - *Computation of* R_M *501*

        Other Considerations 502
        Nonconventional Structures 503
    12.2.3. DMOS Transistors 505
        The Lateral DMOS Transistor 506
        RESURF Transistors 508
        The DMOS NPN 510
12.3 MOS Transistor Matching 511
    12.3.1. Geometric Effects 513
        Gate Area 513
        Gate Oxide Thickness 514
        Channel Length Modulation 515
        Orientation 515
    12.3.2. Diffusion and Etch Effects 516
        Polysilicon Etch Rate Variations 516
        Diffusion Penetration of Polysilicon 517
        Contacts Over Active Gate 518
        Diffusions Near the Channel 518
        PMOS versus NMOS Transistors 519
    12.3.3. Hydrogenation 520
        Fill Metal and MOS Matching 521
    12.3.4. Thermal and Stress Effects 521
        Oxide Thickness Gradients 522
        Stress Gradients 522
        Thermal Gradients 522
    12.3.5. Common-Centroid Layout of MOS Transistors 523
12.4 Rules for MOS Transistor Matching 528
12.5 Summary 531
12.6 Exercises 531

13 *Special Topics 534*
13.1 Merged Devices 534
    13.1.1. Flawed Device Mergers 535
    13.1.2. Successful Device Mergers 539
    13.1.3. Low-Risk Merged Devices 541
    13.1.4. Medium-Risk Merged Devices 542
    13.1.5. Devising New Merged Devices 544
    13.1.6. The Role of Merged Devices in Analog BiCMOS 544
13.2 Guard Rings 545
    13.2.1. Standard Bipolar Electron Guard Rings 546
    13.2.2. Standard Bipolar Hole Guard Rings 547
    13.2.3. Guard Rings in CMOS and BiCMOS Designs 548
13.3 Single-level Interconnection 551
    13.3.1. Mock Layouts and Stick Diagrams 551
    13.3.2. Techniques for Crossing Leads 553
    13.3.3. Types of Tunnels 555
13.4 Constructing the Padring 557
    13.4.1. Scribe Streets and Alignment Markers 557
    13.4.2. Bondpads, Trimpads, and Testpads 558
13.5 ESD Structures 562
    13.5.1. Zener Clamp 563
    13.5.2. Two-Stage Zener Clamps 565

- 13.5.3. Buffered Zener Clamp 566
- 13.5.4. V_{CES} Clamp 568
- 13.5.5. V_{ECS} Clamp 569
- 13.5.6. Antiparallel Diode Clamps 570
- 13.5.7. Grounded-Gate NMOS Clamps 570
- 13.5.8. CDM Clamps 572
- 13.5.9. Lateral SCR Clamps 573
- 13.5.10. Selecting ESD Structures 575

13.6 Exercises 578

14 *Assembling the Die 581*

14.1 Die Planning 581
- 14.1.1. Cell Area Estimation 582
  - *Resistors 582*
  - *Capacitors 582*
  - *Vertical Bipolar Transistors 583*
  - *Lateral PNP Transistors 583*
  - *MOS Transistors 583*
  - *MOS Power Transistors 584*
  - *Computing Cell Area 584*
- 14.1.2. Die Area Estimation 584
- 14.1.3. Gross Profit Margin 587

14.2 Floorplanning 588

14.3 Top-Level Interconnection 594
- 14.3.1. Principles of Channel Routing 594
- 14.3.2. Special Routing Techniques 596
  - *Kelvin Connections 597*
  - *Noisy Signals and Sensitive Signals 598*
- 14.3.3. Electromigration 600
- 14.3.4. Minimizing Stress Effects 603

14.4 Conclusion 604

14.5 Exercises 605

Appendices

- A. Table of Acronyms Used in the Text 607
- B. The Miller Indices of a Cubic Crystal 611
- C. Sample Layout Rules 614
- D. Mathematical Derivations 622
- E. Sources for Layout Editor Software 627

Index 628