The back to back converter

control and design

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Preface

This thesis covers work I have carried out at the department of Industrial Electrical engineering and Automation in a project on power-grid friendly power converters. The main subject is the DC-link capacitor in back-to-back converters, but the main part of the work is the design of a control computer for power conversion.

My interest for power converter control started in late 1992 while I was completing my masters thesis. I was looking for an application for the real-time kernel I had designed, and controlling a power converter was suggested by Dr Mats Alaküla. The experience from this work inspired thoughts on the ideal controller hardware for electrical drive research. However, at that time there was no financial support for the development of such hardware. In 1994 an opportunity arose to design this computer when a project on power-grid friendly converters was initiated by Dr Alaküla.

It is a great pleasure to complete this thesis. If, at some point in the future, back-to-back power converters become economically feasible I hope the analysis and the design ideas presented in this thesis will be of good use.

Acknowledgements

First of all, I would like to thank my supervisor, Prof. Mats Alaküla. Without his work on financial support, this project would never have started. He has also raised prudent questions regarding reliability and safety issues.

For discussions and comments I am grateful to Åke Christensson at ADTranz, Västerås, Sweden (previously at ABB Corporate Research, Västerås, Sweden), Prof. Lars Norum at the Norwegian Institute of Technology, Trondheim, Norway, Ole Morten Stangvik at the Norwegian Institute of Technology, Trondheim, Norway, Bengt Bengtsson at the department of Applied Electronics, Lund Institute of Tecnology, Lund, Sweden and Tore Svensson at Högskolan i Skövde, Skövde, Sweden.

I would also like to thank Jonas Forsberg at the Department of LTH-Malmö. His input on programmable logic was invaluable. Bertil Lindvall at the Department of Information Technology has given me access to their circuit programmer, many thanks.

For building and partly designing the wire-wrapped control computer prototype I am indebted to Svante Andersson and Peter Franz. The prototype had over 400 connections and thanks to their expertise, the prototype worked almost immediately. Thanks also to Johan Bengtsson and Anders Stenudd, who designed and built the back-to-back AC/AC converter which I have used for experiments and demonstrations.

The personnel at IEA has been very supportive. In particular Getachew Darge and Mansour Mojtahedi (now at Högskolan i Karlskrona-Ronneby) who assembled the electronics and maintained the workshop. Their demand for perfect drawings improved the quality of my designs. Bengt Simonsson is an outstanding purchaser and always helpful with anything practical.

Finally I would like to thank my fellow graduate students. They

are an important part of the creative research environment at IEA that makes it fun to go to work. Dr Gunnar Lindstedt got me started with the electronics CAD system. Morten Hemmingson maintains the LaTeXinstallation and Dr Ulf Jeppsson carefully maintains the UNIX system. Sven-Göran Bergh (now at Industrial Communication) is always ready for a big laugh, or a good hack, or both.

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Chapter 1

Introduction

More than half of the electric energy production in Sweden is consumed in electrical drives. An increasing number of them are power electronically controlled variable speed drives. Using variable speed drives is advantageous. In many applications, such as pump drives, a variable speed drive can pay back the purchase in a single year, just from energy savings.

One drawback of conventional variable speed drives, however, is the large content of low frequent line-current harmonics due to the diode rectifier on the line side. For a wide use of variable speed drives, care must be taken to limit these low order harmonics in the utility grid. Passive filters, or other rectifier solutions are available to solve these problems.

One possible solution, studied in this thesis, is the back-to-back converter which has a second transistor bridge on the line side instead of the diode rectifier. This approach eliminates the main drawback of diode rectifiers and introduces a number of advantages like increased dc link voltage and minimized energy storage as well as active filtering and reactive power compensation capabilities.

1.1 History

Around the year 1960, static (electronic) power converters were scarce, though not entirely new. Six years earlier, the first commercial HVDC[1]

[1]HVDC = High Voltage, Direct Current.

power line in the world, between the Swedish mainland and the island of Gotland, had been completed. The mercury arc valve had for several years been used for high power applications (such as HVDC) but the silicon thyristor was invented and already usable for megawatt power levels. Several companies were working on static power converters for different applications. For instance, ASEA was working on the Rc series engines for the Swedish state railways, which employs thyristor-based power converters and DC machines with separate excitation to improve traction performance.

In the following years, static power converters spread through the industry. Not rapidly though, since the cost of the converter was too high to motivate its use in all but the most demanding applications. Furthermore, most power system engineers questioned the reliability of variable speed drives, a situation that remained unaltered as late as the 1980s.

Line-commutated converters

In the 1960s power converters connected to a AC power grid were line commutated; the individual valves in the converter bridge are switched on when the voltage across is positive and a gate pulse is applied, thereafter switched off when the current [flowing through them] changes direction and the voltage across becomes negative.

A drawback with line commutated converters, apart from cycloconverters, is that they cannot be used to feed an induction machine. Furthermore, a synchronous machine must be rotating before the converter can operate. Another problem is the high levels of low-order harmonics in the line current.

Force-commutated PWM converters

By the end of the 1960s, it was possible to build power converters in the kilowatt range with bipolar transistors, instead of thyristors. The transistor can be switched on and off regardless of the current flowing through it, so the converter can be made force-commutated, instead of line commutated. A force commutated converter can have much faster control over its input current and output voltage, which gives it better performance. This property is useful in servo applications with high performance requirements.

The availability of force commutated converters opened up new possibilities. For instance, it became possible to build variable speed drives

with induction machines and mastering the control of induction machines has been a major research topic since that time. Other application areas for force commutated power converters are synchronous machine drives, brushless DC drives and uninterruptible power supplies.

Since the early 1970s, solid state switching components suitable for force commutated power converters has developed quite far. Today, bipolar transistors have been replaced by IGBTs and MOSFETs, which simplifies the converter design and enables considerably higher switching frequencies. Transistorized power converters can be readily built for power levels up to a tens of megawatts.

1.2 Converter harmonics

The deficiencies of the line commutated power converters are well known; Rather high low-order harmonics in the line current (depending on the existence of a DC-choke) and high demand for reactive power when the output voltage is low. These deficiencies are taken care of with filters and reactive power compensation. For small converters, though, the problem is mostly ignored. Filtering is applied only to minimize radio-frequency interference (RFI).

The three-phase diode bridge rectifier is only slightly better. Since the output voltage is uncontrolled, the current has the same shape as the line current of a fully saturated thyristor bridge. The fundamental power factor is thus unity, but the harmonics are still there.

Worst of all, single-phase rectifiers without a DC-choke have a line current shape which resembles a pulse-train. When connected between line and neutral, the combined effect of single-phase rectifiers connected to all three phases is large third-harmonic and ninth harmonic currents in the neutral line. The third harmonic in the neutral line can be four times as large as the fundamental line current, causing unwanted losses in the power lines.

1.2.1 Harmonics in the power grid

For small to medium sized power converters, the cost of harmonics-elimination is often considered too high compared to the limited influence the single power converter has on the power grid. This was a reasonable assumption fifteen years ago, since linear loads like incandescent lamps, induction machines, electric stoves, electric heaters and so forth dominated the load on the power grid.

	Percent of fundamental			
k	IEC 1000-2-2	IEC 1000-2-4		
		Class 1	Class 2	Class 3
5	6	3	6	8
7	5	3	5	7
11	3.5	3	3.5	5
13	3	3	3	4.5
17	2	2	2	4
19	1.5	1.5	1.5	4
23	1.5	1.5	1.5	3.5
25	1.5	1.5	1.5	3.5
> 25	$0.2 + 12.5/k$	$0.2 + 12.5/k$	$0.2 + 12.5/k$	$5\sqrt{11/k}$
THD	8	5	8	10

Table 1.1: Allowed harmonic voltage distortion in general (IEC 1000-2-2) and industrial (IEC 1000-2-4) distribution networks

	IEC 1000-3-2	IEC 1000-3-4
	$I_1 < 16$A	$I_1 > 16$A
k	I_k (A)	I_k/I_1 (%)
3	2.3	21.6
5	1.14	10.7
7	0.77	7.2
9	0.40	.
11	0.33	.
13	0.21	.
$15 - 39$	$0.15 \cdot 15/k$	.
31	–	0.7
> 33	–	≤ 0.6

Table 1.2: Allowed current harmonic emissions for equipment connected to common distribution networks

Recent years, however, have seen an increased proliferation of relatively small electronic loads. Fixed speed drives for fans and pumps are replaced with variable speed drives. Heavy and repetitive tasks are now performed by industrial robots with servo drives. Pneumatic power tools are replaced by electric power tools with better performance. Rotary converters are replaced with solid-state converters. Inductive ballasts for fluorescent lamps are replaced by electronic ballasts.

Most of these relatively small loads has a diode rectifier connected to the power grid. In many cases the rectifier does not even have a DC-choke to smooth the line current. Each one of these loads is small compared to the total load. Despite this, they dominate the total load because of the large number of them. Further, since diode rectifiers operate synchronously, a large number of small rectifier loads will behave like a single large rectifier load.

The fact that electronic loads will eventually dominate the power consumption has led the EU[2] to implement restrictions on harmonic levels, see table 1.1 and 1.2. These restrictions prohibit the use of simple diode rectifiers, at least in principle. In practice, the rules do not impose any restrictions on normal household appliances, TV-sets, personal computers, power tools, industrial equipment etc.

1.2.2 Elimination of harmonics

The high level of the low-order harmonics generated by line commutated rectifiers has made engineers and scientists develop methods to reduce the influence on the power grid or to eliminate the problem entirely. Some of these methods are:

- Filters, both LCL, and multiple series resonant links
- Third harmonic injection
- Twelve-pulse operation
- Multi-level rectifiers
- Force commutated rectifiers (e.g PWM-rectifiers)

All of these methods imply higher cost for the power converter. Some of the methods also result in a heavier and more voluminous converter.

[2]The European Union

For certain applications (e.g. HVDC transmission), elimination of low-order harmonics is required by the utility. Because of the high power levels, these applications are implemented with line commutated rectifiers. Consequently, these plants have large filter yards. The filters increase the cost for the plant, but not so much that the plant cannot be profitable.

In most cases though, elimination of the line current harmonics is not considered economical, or even necessary. In the future, LVDC and MVDC distribution might supersede the three-phase system for feeding individual drives in industrial plants. It is probably cheaper to eliminate line current harmonics from a single large rectifier feeding an entire plant or factory, than having filters and force commutated rectifiers on every single drive throughout the plant.

1.3 The back-to-back converter

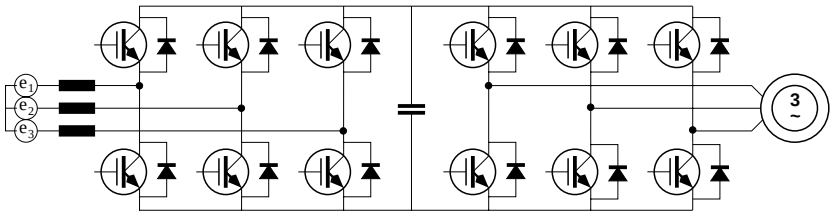

Figure 1.1: Back-to-back converter

The back-to-back converter is hinted at in the above discussion on line current harmonics. It consists simply of a force-commutated rectifier and a force-commutated inverter connected with a common DC-link, see figure 1.1. The properties of this combination are well known; the line-side converter may be operated to give sinusoidal line currents, for sinusoidal currents, the DC-link voltage must be higher than the peak main voltage, the DC-link voltage is regulated by controlling the power flow to the AC grid and, finally, the inverter operates on the boosted DC-link, making it possible to increase the output power of a connected machine over its rated power. Another advantage in certain applications is that braking energy can be fed back to the power grid instead of just wasting it in a braking resistor.

An important property of the back-to-back converter is the possibility of fast control of the power flow. By controlling the power flow to the grid, the DC-link voltage can be held constant. The presence of a fast control loop for the DC-link voltage makes it possible to reduce the size of the DC-link capacitor, without affecting inverter performance. In fact, the capacitor can be made small enough to be implemented with plastic film capacitors.

1.3.1 Issues associated with a small DC-link capacitor

The smallest size of the DC-link capacitor governed by the need to keep switch-frequent ripple at acceptable (i.e. small) levels. Fluctuations in the load cannot be smoothed in the converter, but must be accommodated by other means.

One alternative is to simply transfer such fluctuations to the power grid, but this may re-introduce the line-current harmonics the back-to-back converter is supposed to eliminate. However, load fluctuations will be random and thus relatively harmless compared to the in-phase harmonics generated by diode rectifiers.

Another alternative is to use the load itself. In a typical drive, the mechanical energy stored in the drive is several orders of magnitude larger than the electrical energy stored in the DC-link capacitor in a back-to-back converter. If the application does not need servo-class performance, there is no reason why the rotational speed cannot be allowed to fluctuate slightly. A pump drive, for instance, may be perfectly satisfactory if the speed regulation performance is comparable with a directly connected induction motor. (On the other hand, it may not. If a fixed-speed drive plus control valve is replaced with a variable speed drive, the variable speed drive must, in principle, have the same control performance as the control valve.)

The smallest feasible capacitor, chosen on the basis of switch-frequent voltage ripple, is too small to absorb (within voltage limits) even the [electromagnetic] energy stored in the main flux of a connected electrical drive. This places high demands on the controller which must be absolutely reliable. If the controller fails, the stored energy may raise the voltage of the DC-link beyond acceptable levels (enough to break the rectifier and/or the inverter). This may also result from circuit-breaker tripping.

To avoid DC-link overvoltage resulting from e.g controller failure,

also the back-to-back converter must have a voltage limiting device. This can consist of a traditional brake chopper. However, the *average* power rating needed is much smaller than for a conventional converter, although the peak power rating would probably be more than the rated power of the converter[3]. The chopper must be independent of the converter controller to be operational in event of a controller failure. Preferably, the chopper should operate directly from the DC-link voltage.

1.4 The controller hardware

For almost a decade, the department of Industrial Electrical Engineering and Automation (IEA) has used an analog control system built in generic modules for research and education. A module consists of an 100x220mm curcuit board mounted in a Eurocard box with type F back plane connector. These modules make up a rather flexible system that easily can be arranged to create almost any kind of electric drive control system. A drawback, however, is that the analog system is unwieldy when researching controller structures and algorithms not anticipated in the analog design.

To increase the flexibility, IEA has used a control system built with a Macintosh II as host computer and two standard add-in boards from National Instruments together with the above mentioned analog system. This combination works well, and has been used for measurements in three PhD theses and four Master theses.

An important drawback of systems built into host computers, is the physical inflexibility. It is desirable for the control hardware to work as a "stand alone" unit, e.g in an industrial evaluation of a prototype. This is impractical with systems in host computers.

To be able to design research converters, and try them in practical environments, a programmable digital control unit that fits in the existing analog system is desirable.

1.4.1 Controller demands

A self-contained digital control unit intended for electrical drives must, in terms of performance, be able to meet the requirements of demanding

[3]Peak power in this case means the power consumed by the resistor when connected to the nominal DC-link voltage.

drives. Control of a back-to-back converter was chosen as the reference application, given its demanding control tasks.

In the back-ti-bakc converter case, the controller has to control two AC systems, versus one for frequency converters with diode rectifiers. In addition, the DC link voltage has to be controlled, adding another control loop to the system. The AC systems can be controlled with space-vector controllers, which may require angular transforms in software. In total, there may be seven or eight control loops and a state-space model with six or more states to update.

1.4.2 The control computer

The IEA-MIMO[4] control computer presented in this thesis is designed to meet the above mentioned reqirements. The IEA-MIMO is built around a TMS320C30 floating-point signal processor and has:

- sixteen analog inputs that are sampled in parallel and converted in less than sixteen microseconds total,
- eight analog outputs,
- nine digital/logic inputs/outputs,
- a standard serial communication port and
- a 16-bit expansion bus for additional I/O.

The IEA-MIMO can control a back-to-back converter at 10 kHz sampling frequency (this assumes a relatively simple space-vector controller for the load). Achieveing this performance does not require programming in assembly language; the C programming language can be used. Being able to program in high-level language is desirable, since it is easier to focus on algorithms when implementation details are taken care of by a compiler. It should be noted, however, that programming in assembly can result in a significantly faster program.

The IEA-MIMO does not include a pulse-width modulator. This is beacuse a pulse-width modulator may not be needed for a particular application. There is a large number of converter modulation methods and just including one of them would be too inflexible. Furthermore,

[4]MIMO stands for Multiple-Input, Multiple-Output. This is a property of the processes the IEA-MIMO is designed to control.

some converter types (notably matrix converters) cannot be controlled with a simple multi-channel pulse-width modulator.

To be able to control the back-to-back converter, a separate module with a six-channel pulse-width modulator, the IEA-PWM6 has been designed. This module is connected to the expansion bus of the IEA-MIMO. The IEA-PWM6 is a digital carrier-wave modulator with 10 bits resolution. All six channels use the same carrier which means the output pulses are synchronous and centered. The latter is advantageous for back-to-back converters, since the synchronous switching reduces the DC-link voltage ripple.

1.5 Thesis outline

This thesis has two parts. Part I deals with back-to-back power converters, particularly the DC-link capacitor. In chapter 2, models for the source (or line-side) converter and the structure of the control system are presented. Chapter 3 analyses the dynamic behaviour of the controlled (closed-loop) converter in the continuous-time domain. Analytical expressions for transient DC-link voltage deviations and DC-link energy impulses are derived. The implications drawn from the results in chapter 3 for back-to-back converter design are summarized in chapter 4.

Part II is a description of the digital control hardware that has been built in the course of this work. Chapter 5 describes the IEA-MIMO control computer in detail, including design issues, feature set, usage and performance. In chapter 6 the IEA-PWM6 six-phase pulse-width modulator is discussed.

Part I

Back-to-back converters

Chapter 2

Modelling

A central subject for this thesis is the DC-link in back-to-back voltage-source converters. A back-to-back converter consists of a line converter and a load converter. Usually, but not necessarily, both the line and load converters are three-phase voltage-source converters. Under certain assumptions the line converter can be viewed and analysed like a 4-quadrant DC/DC boost converter. The results from this analysis can then be applied to the three-phase converter.

In the voltage transient analysis, the load model is a DC current sink with stepwise changes of its power consumption. This model is chosen because it makes the analysis simpler; the current sink has infinite impedance, which makes it invisible in the system dynamics. The use of this model is valid under the assumption of small variations in the DC-link voltage.

The impedance of real loads is of course not infinity, not even necessarily positive. A load consisting of a four-quadrant converter driving a DC servo actually has negative impedance, or rather: it has constant power consumption, i.e $P_{load} = U \cdot I = constant$. This type of load is used in the analysis of energy transients taken up in the DC-link.

This chapter describes the three-phase converter, the structure of the controller for the converter and the models used for the analysis in chapter 3. The analysis is performed on a model of a DC/DC-converter. The conversion between the analyzed model and three-phase AC/DC converters is described in this chapter.

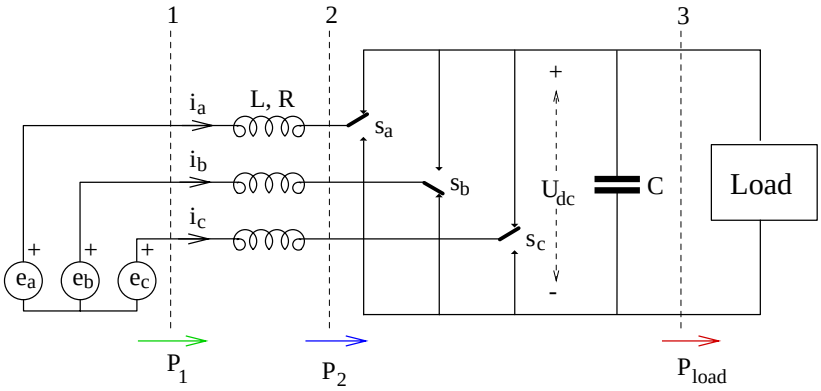

Figure 2.1: Three-phase converter with general load

Parameter	value	unit
Nominal power	6	kW
Mains voltage	400	V
Mains frequency	50	Hz
Line inductors	7	mH
Line resistance	0	Ω
DC-link capacitor	100	μF

Table 2.1: Simulation parameters

Simulation parameters

In this chapter and the following chapter, the theory is illustrated with simulations performed with SIMULINK and MATLAB. The model has been built using the above mentioned assumptions. Simulations has been performed with both DC/DC and AC/DC models.

If not otherwise stated, the model parameters used in simulations are according to table 2.1

2.1 The three-phase converter

The converter is an ordinary three-phase transistor bridge connected to the grid via "commutation inductors", see figure 2.2 on the facing page.

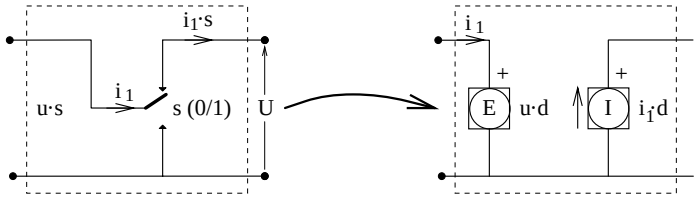

Figure 2.2: Averaging of a two-quadrant switch

The circuit can be thought of as a voltage-source inverter connected to the power grid.

The only difference between rectifier and inverter is the definition of power sign.

For the analysis, the circuit is modeled with averaged switch elements, see figure 2.2. This makes it possible to model the circuit in continuous time, by replacing all instantaneous values with their averaged counterparts. The switch frequency of the converter is assumed to be sufficiently high to make an average analysis valid. Sufficiently high in this case means that the switching ripple should be negligible compared to the averaged values.

2.1.1 Mathematical model

The circuit in figure 2.1 on the facing page can be modeled by the following system:

$$\begin{cases} L\dfrac{di_a}{dt} = e_a - u_a - Ri_a = e_a - u_{dc}\dfrac{2s_a - s_b - s_c}{3} - Ri_a \\ L\dfrac{di_b}{dt} = e_b - u_b - Ri_b = e_b - u_{dc}\dfrac{-s_a + 2s_b - s_c}{3} - Ri_b \\ L\dfrac{di_c}{dt} = e_c - u_c - Ri_c = e_c - u_{dc}\dfrac{-s_a - s_b + 2s_c}{3} - Ri_c \\ C\dfrac{du_{dc}}{dt} = s_a i_a + s_b i_b + s_c i_c - i_{load} \end{cases} \tag{2.1}$$

where $\{s_a, s_b, s_c\}$ indicate the switch positions of each phase; s can be either 0 or 1, with $s = 1$ indicating that the output is connected to the positive terminal of the DC-link capacitor.

The model in (2.1) is too detailed. By assuming fast switching, the

switch positions s_k can be replaced with the average d_k (d for duty-cycle). The equations then become:

$$\begin{cases} L\dfrac{di_a}{dt} = e_a - u_{dc}\dfrac{2d_a - d_b - d_c}{3} - Ri_a \\ L\dfrac{di_b}{dt} = e_b - u_{dc}\dfrac{-d_a + 2d_b - d_c}{3} - Ri_b \\ L\dfrac{di_c}{dt} = e_c - u_{dc}\dfrac{-d_a - d_b + 2d_c}{3} - Ri_c \\ C\dfrac{du_{dc}}{dt} = d_a i_a + d_b i_b + d_c i_c - i_{load} \end{cases} \tag{2.2}$$

This method can be further extended for low frequency switching, by introducing states for the switch-frequent ripple amplitude, and so on if needed. This is, however, outside the scope of this thesis.

The model can be further simplified, using "space-vector" theory. The three-phase circuit is then transformed to a virtual two-phase circuit. After voltages and currents are transformed using the power-invariant Park transform, the following equations result

$$\begin{cases} L\dfrac{di_\alpha}{dt} = e_\alpha - u_\alpha - Ri_\alpha \\ L\dfrac{di_\beta}{dt} = e_\beta - u_\beta - Ri_\beta \\ C\dfrac{du_{dc}}{dt} = \dfrac{u_\alpha}{u_{dc}} i_\alpha + \dfrac{u_\beta}{u_{dc}} i_\beta - i_{load} \end{cases} \tag{2.3}$$

which could also be written as a vector differential equation:

$$\begin{cases} \mathbf{L}\dfrac{d\vec{i}}{dt} = \vec{e} - \vec{u} - \mathbf{R}\vec{i} \\ C\dfrac{du_{dc}}{dt} = \dfrac{\vec{u}\cdot\vec{i}}{u_{dc}} - i_{load} \end{cases} \tag{2.4}$$

The states in this model vary sinusoidally with the line frequency. This means, that closed loop control of this system can not be considered as a standard problem, where the states are regulated around a steady state. To be able to apply standard linear control on steady-state variables, the model can be transformed from the fixed (α, β) space to the rotating (d, q) space.

The (d, q) space is so oriented that the integral of the voltage vector points in the d-axis direction. This means that reactive current (assuming sinusoidal currents and voltages) is measured along the d-axis and active current is measured along the q-axis.

The (α, β) to (d, q) transform is performed by subtracting the argument of the integrated line voltage vector (or line flux vector) from all vectors. If constant line-frequency f is assumed, i.e. (d, q)-space is rotating $\omega = 2\pi f$ rad/s, the transformed model becomes:

$$\begin{cases} L\dfrac{di_d}{dt} = -u_d - Ri_d - L\omega i_q \\ L\dfrac{di_q}{dt} = e_q - u_q - Ri_q + L\omega i_d \\ C\dfrac{du_{dc}}{dt} = \dfrac{u_d}{u_{dc}} i_d + \dfrac{u_q}{u_{dc}} i_q - i_{load} \end{cases} \tag{2.5}$$

Note that the transform introduces cross-coupling between the equations for the line current. Those terms introduce a nonlinearity in the model, which in some cases must be accounted for. In the derivation of the DC/DC-model parameters (section 2.2), however, it is assumed that the d-axis current is always regulated to zero, which makes the cross-term disappear from the active current equation.

2.1.2 Controller principles

There are many papers in the literature on control strategies for controlled-current three-phase rectifiers. Basically, the control problem is identical to synchronous-machine control. Since the converter control method is not the main point of this work, I will only give a brief description of some approaches found in the literature.

Hysteresis control Hysteresis control is also called tolerance-band or dead-band control. This controller type recognizes that voltage source converters can only have seven different output voltages. This leads naturally to a limit-cycle oscillation in the line current vector, which by the controller is kept inside a small area of some shape in the current vector space. The advantage is a known deviation from the current reference, but the switching pattern is more or less random, making it hard to predict converter losses.

Synchronous PI controllers This is one of the most popular control methods. The idea is to transform currents and voltages into a rotating reference frame, where the controlled currents are constant in "steady-state", use ordinary PI controllers on the transformed values, and transform the controller outputs back to the fixed reference frame. The drawbacks are the nonlinearities introduced in the transform and less than optimal control performance. The advantage is that it is simple to understand and simple to implement.

Minimum time control There is an excellent paper by Chui and Seui [**?**] who proposes a minimum-time controller. This controller is slightly better than synchronous PI control, which is shown with simulations and experiments in the paper. The controller uses reactive power impulses to improve the transient response. A later article by the same authors [**?**] applies the ideas to traditional synchronous PI controllers.

MRAS Model-reference adaptive control has been proposed by Takeshita and Matsui [**?**]. The approach has the advantage of not having to know the process parameters exactly, while still achieving good performance.

Synchronous PI controllers and minimum time control both work with averaged voltages and currents. The converter is controlled via a PWM-modulator that generates a switching pattern that corresponds to the desired average voltage.

In this thesis, the line current controller is assumed to be a synchronous PI controller. Its properties are well known in the power electronics area. Further, by assuming this type of controller, the three-phase converter can be modelled as two separate four quadrant converters. One for the active power and one for the reactive power. The reactive power is assumed to be zero, which means this part can be removed. See section 2.2 on page 27 for a DC-model of the converter.

2.1.3 Controller structure

The structure of the control system for the power converter is outlined in figure 2.3 on the facing page. To simplify the figure, conversions between three-phase values and space vectors are not shown. The controller is divided in a line-current controller and a DC-link voltage controller,

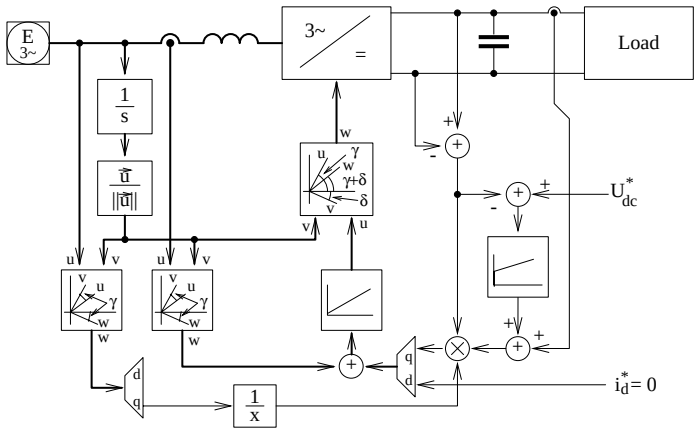

Figure 2.3: Simplified diagram of the controller structure

operating in cascade. The line-current controller is a PI-controller that operates on vectors in (d, q) space. The parameters are identical for both components.

The DC-link voltage controller is a proportional controller with a feed-forward from the load current (called PE-controller for the rest of this thesis). The output from the voltage controller is scaled with the quotient between the DC-link voltage and the line voltage.

The outlined closed-loop system (designated PE+PI) can be described with the following differential equation system:

$$
\begin{aligned}
L\frac{di_d}{dt} &= u_d - Ri_d - L\omega i_q \\
L\frac{di_q}{dt} &= e_q - u_q - Ri_q + L\omega i_d \\
C\frac{du_{dc}}{dt} &= \frac{u_d}{u_{dc}} i_d + \frac{u_q}{u_{dc}} i_q - i_{load} \\
\frac{dI_{i_q}}{dt} &= \frac{K_{p_i}}{T_{i_i}} \left[\frac{u_{dc}}{e_q} \left(K_{p_u} \cdot ({u_{dc}}^* - u_{dc}) + i_{load} \right) - i_q \right] \qquad (2.6) \\
\frac{dI_{i_d}}{dt} &= \frac{K_{p_i}}{T_{i_i}} \left[{i_d}^* - i_d \right] \qquad (2.7)
\end{aligned}
$$

where I_{i_q} and I_{i_d} are the integral terms of the PI controllers and

$$u_d = K_{p_i}\left[{i_d}^* - i_d\right] + I_{i_d} \tag{2.8}$$

$$u_q = K_{p_i}\left[\frac{u_{dc}}{e_q}\left(K_{p_u}\cdot\left({u_{dc}}^* - u_{dc}\right) + i_{load}\right) - i_q\right] + I_{i_q} \tag{2.9}$$

In the equations above, K_{p_i} and T_{i_i} is the proportional gain and integral time of the current controller, and K_{p_u} is the gain of the DC-link voltage controller.

One advantage of this controller is that it is easy to understand and analyse and the closed loop system is easily stabilized. Implementation is simplified by the lack of an integrator in the outher loop (see below). The obtainable performance, however is less than perfect. Since the integrator is in the inner loop, the control system cannot eliminate stationary errors in u_{dc} caused by errors in the feedforward path and/or resistance in the inductors.

A better control system is obtained if the integral part of the active current regulator, I_{i_q}, is removed and an integral term is inserted in the regulator for u_{dc}. This control system (called PIE+P onwards) eliminates stationary errors, but great care must be taken to eliminate integrator windup, which otherwise may cause large overshoots. However, if the anti-windup is properly designed, this controller has identical or better dynamic performance.

Without anti-windup, the proposed closed-loop system can be modelled with the following differential equations:

$$\begin{aligned}
L\frac{di_d}{dt} &= u_d - Ri_d - L\omega i_q \\
L\frac{di_q}{dt} &= e_q - u_q - Ri_q + L\omega i_d \\
C\frac{du_{dc}}{dt} &= \frac{u_d}{u_{dc}}i_d + \frac{u_q}{u_{dc}}i_q - i_{load} \\
\frac{dI_{u_{dc}}}{dt} &= \frac{K_{p_u}}{T_{i_u}}\left[{u_{dc}}^* - u_{dc}\right] && (2.10) \\
\frac{dI_{i_d}}{dt} &= \frac{K_{p_i}}{T_{i_i}}\left[{i_d}^* - i_d\right] && (2.11)
\end{aligned}$$

where $I_{u_{dc}}$ is the integral part of the DC-link voltage controller, and

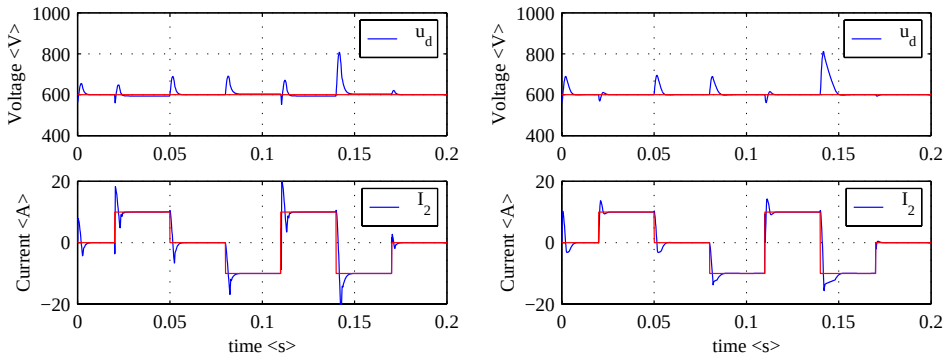

Figure 2.4: Performance of cascaded PE+PI (left) versus cascaded PIE+P (right) controllers

$$u_d = K_{p_i}\left[{i_d}^* - i_d\right] + I_{i_d} \tag{2.12}$$

$$u_q = K_{p_i}\left[\frac{u_{dc}}{e_q}\left(K_{p_u}\cdot\left({u_{dc}}^* - u_{dc}\right) + I_{u_{dc}} + i_{load}\right) - i_q\right] \tag{2.13}$$

Figure 2.4 on the next page compares the two presented controller structures. The graph to the left is a simulation of the PE+PI controller structure, while the graph to the right is for the proposed PIE+P structure. The controllers are tuned for good performance. In both simulations, the load current feedforward has a 5% measurement error, which causes the steady state voltage error in the left graph.

Proper anti-windup for the integrator $I_{u_{dc}}$ is not as straightforward as simply limiting the integrator. The integrator should remain unconstrained until the output voltage u_q reaches the converter limit, at which point the integrator should track the output voltage [**?**] [**?**]. For ordinary PI controllers this can be done according to:

$$\frac{dI}{dt} = \frac{K}{T_i}\left[y^* - y\right] - \frac{1}{T_r}\left[u^* - u\right] \tag{2.14}$$

$$u^* = K\left[y^* - y\right] + I \tag{2.15}$$

$$u = \lim(u^*) \tag{2.16}$$

Where I is the integral part of the controller. In a discrete-time

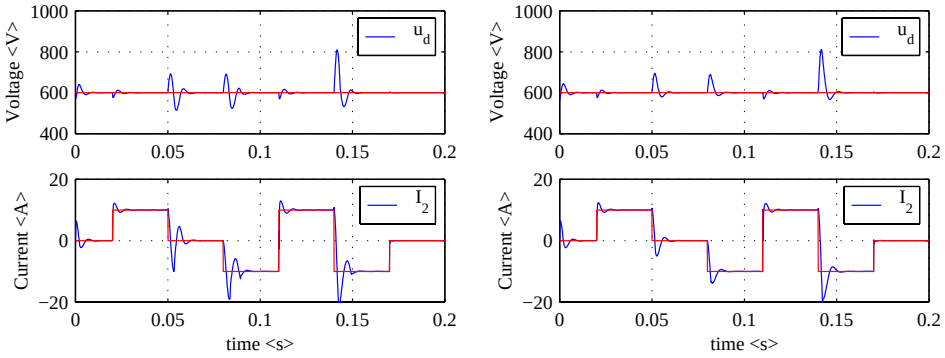

Figure 2.5: Simple saturation (left) versus proposed saturation (right)

implementation, the tracking time constant T_r should be selected somwhere between $2 \cdot T_s$ (T_s being the sampling interval) and T_i. $T_r = T_i/2$ is a good alternative that is used in the simulations.

It remains to derive the limited output of the DC-link voltage controller. Equation (2.13) can be rewritten into:

$$\frac{e_q}{u_{dc}} \left[\frac{u_q}{K_{p_i}} + i_q \right] - i_{load} = K_{p_u} \cdot ({u_{dc}}^* - u_{dc}) + I_{u_{dc}} \tag{2.17}$$

Where the RHS expression corresponds to (2.15) and the LHS expression corresponds to (2.16). Rewriting the integrator input (2.10) completes the anti-windup:

$$\frac{dI_{u_{dc}}}{dt} = \frac{K_{p_u}}{T_{i_u}} \left[{u_{dc}}^* - u_{dc} \right] - \frac{1}{T_{r_u}} \left[{i_c}^* - \frac{e_q}{u_{dc}} \left(\frac{u_q}{K_{p_i}} + i_q \right) - i_{load} \right] \tag{2.18}$$

where

${i_c}^* = K_{p_u} \cdot ({u_{dc}}^* - u_{dc}) + I_{u_{dc}}$

Figure 2.5 illustrates the difference between a fixed saturation of the voltage controller output (with anti-windup) versus using the proposed saturation.

The controller parameters are the same in both graphs. The fixed limit and the controller parameters are chosen for a clear difference. The difference is smaller for a well tuned controller.

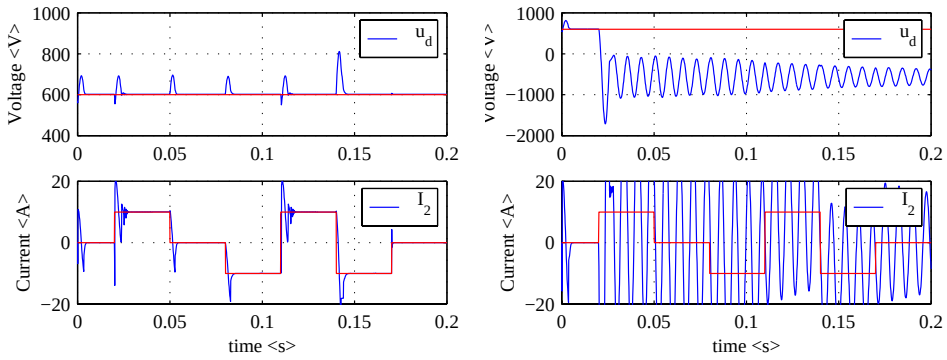

Figure 2.6: Limited (left) versus unlimited voltage controller output

Figure 2.6 on the next page illustrates the importance of limiting the active current command from the DC-link voltage controller. Cascaded proportional controllers are used in both simulations. Controller parameters are identical, but the gain is close to the stability limit (see section 3.1.2). In the left diagram, the voltage controller output is limited to a current corresponding to the nominal power of the converter, whereas it is unlimited to the right. The voltage collapses in the graph to the right since the unlimited current command grows faster than the input current, when the capacitor voltage drops.

It should be noted, however, that the controller parameters used in figure 2.6 is very close to the instability limit. Nevertheless, the simulation shows that the proposed anti-windup has to be combined with an absolute limit on the voltage controller output.

2.2 The equivalent four-quadrant DC/DC-converter.

The full three-phase converter in its present form can be studied and analyzed. The analysis can however be simplified by making some reasonable assuptions which allows modelling as a four-quadrant DC/DC boost converter. Furthermore, by establishing relationships between the three-phase converter circuit and the DC/DC boost converter the result of the DC/DC analysis can be transferred to the three-phase converter.

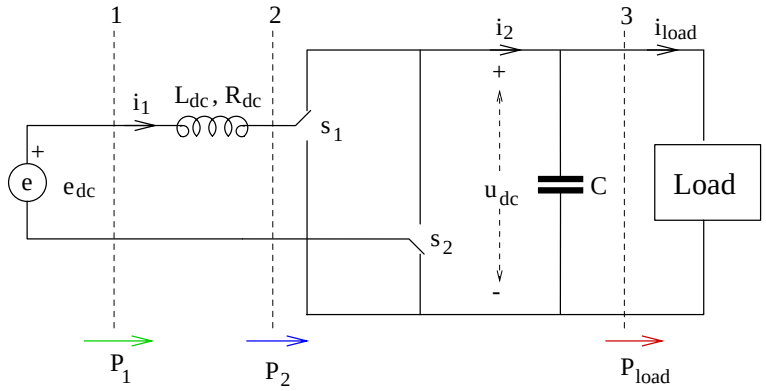

Figure 2.7: Four-quadrant DC/DC boost converter with general load

2.2.1 Mathematical model

The circuit in figure 2.7 on the next page is used to model the active power dynamics of a three-phase converter. For this circuit to be a valid model, the following assumptions must be made:

- Balanced three-phase system.
- Zero reactive power – Line currents always in phase with line voltages.
- No line current harmonics.

With these assumptions, the differential equation system (2.5) can be simplified to

$$\begin{cases} L_{ac}\dfrac{di_q}{dt} = e_q - u_q - R_{ac}i_q \\ C\dfrac{du_{dc}}{dt} = \dfrac{u_q}{u_{dc}}i_q - i_{load} \end{cases} \tag{2.19}$$

Where L_{ac} is the inductance and R_{ac} is the resistance of the inductors in the three-phase model, see figure 2.1. This model can be compared to the corresponding model for the DC/DC boost converter in figure 2.7:

$$\begin{cases} L_{dc}\dfrac{di_1}{dt} = e_{dc} - u_1 - R_{dc}i_1 \\ C\dfrac{du_{dc}}{dt} = \dfrac{u_1}{u_{dc}}i_1 - i_{load} \end{cases} \tag{2.20}$$

Where R_{dc} is the resistance of the inductor.

2.2.2 Relation between the AC and DC models

The relationship between the three-phase AC converter and the DC converter should have good physical interpretation; voltage and current levels should be the "natural" for both cases. This means that the line voltage of the DC/DC converter should be the peak-to-peak main voltage of the AC line.

Table 2.2 on the next page lists the conversions between three-phase AC/DC converters and DC/DC boost converters. The conversion factor for the line inductance are derived by identifying parameters in the equations for the line current. Compare the current equations in (2.19) and (2.20)

$$L_{ac}\frac{di_q}{dt} = e_q - u_q - R_{ac}i_q \tag{2.21}$$

$$L_{dc}\frac{di_1}{dt} = e_{dc} - u_1 - R_{dc}i_1 \tag{2.22}$$

Since AC voltages are multiplied by a $\sqrt{2}$ factor to get the corresponding DC voltage, (2.21) can be extended with $\sqrt{2}$, producing:

$$\sqrt{2}L_{ac}\frac{di_q}{dt} = \sqrt{2}e_q - \sqrt{2}u_q - \sqrt{2}R_{ac}i_q \tag{2.23}$$

Since power should be the same in both models, i.e $e_{dc} \cdot i_1 = \sqrt{2}e_q \cdot i_1 = e_q \cdot i_q$, then $i_q = \sqrt{2}i_1$. Equation (2.23) then becomes:

$$2L_{ac}\frac{di_1}{dt} = e_1 - u_1 - 2R_{ac}i_1 \tag{2.24}$$

Equation (2.24) is the same as (2.22), but with AC parameters. The DC parameters can now be identified, yielding the result in table 2.2 on the following page.

Parameter	AC/DC	DC/DC
Inactive U_{dc}	$\hat{e}_h = \sqrt{2} * E_h$	e_{dc}
Line voltage	E_h	$e_{dc} = \sqrt{2} \cdot E_h$
Power	$P_{ac} = e_h \cdot i_q$	$P_{dc} = e_{dc} \cdot i_{dc}$
Line current	i_q	$P_{dc} = P_{ac} \Rightarrow i_{dc} = \frac{i_q}{\sqrt{2}}$
Inductance	L_{ac}	$L_{dc} = 2L_{ac}$
Inductor resistance	R_{ac}	$R_{dc} = 2R_{ac}$

Table 2.2: Conversion between AC/DC and DC/DC converters

2.2.3 Controller structure

The controller for the DC/DC converter model is basically the same as for the AC/AC converter, without the reactive power part. The structure is further simplified by the lack of angular transforms.

Chapter 3

Analysis

In this chapter, the properties of an averaged model of a four quadrant DC/DC-converter are examined in detail. Section 3.1 examines the "small-signal" properties of the converter, when controlled by a state-feedback controller. The controlled system is non-linear, but the large-signal stability is not examined. Section 3.2 develops the large-signal transient response. The control-signal limitations disable the controller during power transient and the size of the output voltage transient is determined. In section 3.3 the output voltage is assumed to be held constant, and the amount of energy taken up by the DC-link voltage source during power transients is calculated.

3.1 Controller loop

As in the rest of this chapter, a continuous-time DC model of the converter is assumed. This is a serious simplification, since it implies that active and reactive line-current control is decoupled by synchronous PI controllers. Which is not the case, as is evident from equations (2.5), where the cross-coupling factor ωL can be seen.

Nevertheless, the cascaded controller structure described in section 2.1.3 is applied to the continuous DC/DC converter. Referring to equations (2.10), (2.13) and figure 2.7, the closed-loop system is described by the following set of non-linear differential equations:

$$L_{dc}\frac{di_1}{dt} = e_{dc} - u_1 - Ri_1 \tag{3.1}$$

$$C\frac{du_{dc}}{dt} = \frac{u_1}{u_{dc}}i_1 - i_{load} \tag{3.2}$$

$$\frac{dI_{u_{dc}}}{dt} = \frac{K_{p_u}}{T_{i_u}}\left[{u_{dc}}^* - u_{dc}\right] \tag{3.3}$$

where

$$u_1 = K_{p_i}\left[\frac{u_{dc}}{e_{dc}}\left(K_{p_u}\cdot\left({u_{dc}}^* - u_{dc}\right) + I_{u_{dc}} + \hat{i}_{load}\right) - i_1\right] \tag{3.4}$$

Note that the load feedforward, $\hat{i}_{load}$ in (3.4), may differ from the actual load i_{load} in (3.2).

3.1.1 Linearization

It is not straightforward to analyse this system. One way to handle the nonlinearities is to linearize around the operating point, (u_{dc_0}, i_{1_0}) and then apply linear analysis methods to the resulting system. Here it gives some insight in how to select controller parameters to avoid local instability, but does not say anything about global stability.

Introduce the linearized state:

$$\tilde{u}_{dc} = u_{dc} - u_{dc_0} \Leftrightarrow u_{dc} = u_{dc_0} + \tilde{u}_{dc} \tag{3.5}$$

$$\tilde{i}_1 = i_1 - i_{1_0} \Leftrightarrow i_1 = i_{1_0} + \tilde{i}_1 \tag{3.6}$$

Substituting (3.5) for u_{dc} and (3.6) for i_1 in equations (3.1) to (3.4) yields:

$$L_{dc}\frac{d\tilde{i}_1}{dt} = e_{dc} - u_1 - R(i_{1_0} + \tilde{i}_1) \tag{3.7}$$

$$C\frac{d\tilde{u}_{dc}}{dt} = \frac{u_1}{u_{dc_0} + \tilde{u}_{dc}}(i_{1_0} + \tilde{i}_1) - i_{load} \tag{3.8}$$

$$\frac{dI_{u_{dc}}}{dt} = \frac{K_{p_u}}{T_{i_u}}\left[{u_{dc}}^* - u_{dc_0} - \tilde{u}_{dc}\right] \tag{3.9}$$

where

$$u_1 = K_{p_i}\left[\frac{u_{dc_0}+\tilde{u}_{dc}}{e_{dc}}\left(K_{p_u}\cdot({u_{dc}}^* - u_{dc_0} - \tilde{u}_{dc}) + I_{u_{dc}} + \hat{i}_{load}\right) - i_{1_0} - \tilde{i}_1\right] \tag{3.10}$$

Linearizing around the setpoint, i.e $u_{dc_0} = {u_{dc}}^*$ and $i_{1_0} = i_{load}u_{dc}/e_{dc}$ simplifies (3.10) to

$$u_1 = K_{p_i}\left[\frac{u_{dc_0}+\tilde{u}_{dc}}{e_{dc}}\left(K_{p_u}\cdot(-\tilde{u}_{dc}) + I_{u_{dc}}\right) - \tilde{i}_1\right] \tag{3.11}$$

Substituting (3.11) into (3.7)–(3.9) yields:

$$L_{dc}\frac{d\tilde{i}_1}{dt} = e_{dc} - K_{p_i}\left[\frac{{u_{dc}}^* + \tilde{u}_{dc}}{e_{dc}}\left(-K_{p_u}\tilde{u}_{dc} + I_{u_{dc}}\right) - \tilde{i}_1\right] - R(\frac{{u_{dc}}^* + \tilde{u}_{dc}}{e_{dc}}i_{load} + \tilde{i}_1) \tag{3.12}$$

$$C\frac{d\tilde{u}_{dc}}{dt} = \frac{1}{{u_{dc}}^* + \tilde{u}_{dc}}K_{p_i}\left[\frac{{u_{dc}}^* + \tilde{u}_{dc}}{e_{dc}}\left(-K_{p_u}\tilde{u}_{dc}\right) + I_{u_{dc}}\right) - \tilde{i}_1\right](i_{1_0} + \tilde{i}_1) - i_{load} \tag{3.13}$$

$$\frac{dI_{u_{dc}}}{dt} = -\frac{K_{p_u}}{T_{i_u}}\tilde{u}_{dc} \tag{3.14}$$

Further expansion is straightforward, and is left as an exercise to the reader. To further simplify the calculations, an additional assumptions is made. If the load draws constant power instead of constant current (not unrealistic, see beginning of chapter 2), P_{load} can be substituted for $({u_{dc}}^* + \tilde{u}_{dc})i_{load}$. After this substitution and elimination of non-linear terms the equations become more manageable:

$$L_{dc}\frac{d\tilde{i}_1}{dt} = e + \frac{K_{p_i}K_{p_u}{u_{dc}}^*}{e_{dc}}\tilde{u}_{dc} - \frac{K_{p_i}{u_{dc}}^*}{e_{dc}}I_{u_{dc}} + (K_{p_i} - R)\tilde{i}_1 - R\frac{P_{load}}{e_{dc}} \tag{3.15}$$

$$C\frac{d\tilde{u}_{dc}}{dt} = -\frac{K_{p_i}K_{p_u}P_{load}}{e_{dc}^2}\tilde{u}_{dc} + \frac{K_{p_i}P_{load}}{e_{dc}^2}I_{u_{dc}} - \frac{K_{p_i}P_{load}}{{u_{dc}}^* e_{dc}}\tilde{i}_1 - \frac{P_{load}}{{u_{dc}}^*} \tag{3.16}$$

$$\frac{dI_{u_{dc}}}{dt} = -\frac{K_{p_u}}{T_{i_u}}\tilde{u}_{dc} \tag{3.17}$$

From this form it is possible to find the characteristic equation for the linearized system:

$$A(s) = s^3 + \frac{K_{p_i}K_{p_u}L_{dc}P_{load} + (R - K_{p_i})Ce_{dc}^2}{L_{dc}Ce_{dc}^2}s^2 + \frac{K_{p_i}K_{p_u}P_{load}}{L_{dc}Ce_{dc}^2}\left[\frac{L_{dc}}{T_{i_u}} + R\right]s + \frac{K_{p_i}K_{p_u}P_{load}R}{L_{dc}CT_{i_u}e_{dc}^2} \quad (3.18)$$

3.1.2 Stability

Since P_{load} is a factor in all coefficients of the characteristic equation of the closed-loop system, the poles of the linearized system move around with the load of the converter. Consequently, the controller parameters must be chosen to keep all poles in the LHP of the complex plane under all load conditions.

The stability can be examined with Routh's algorithm. The coefficients of a third-order characteristic equation

$$a_0s^3 + b_0s^2 + a_1s + b_1 = 0 \quad (3.19)$$

are arranged in a table according to:

$$\begin{array}{cc} a_0 & a_1 \\ b_0 & b_1 \\ a_1 - \frac{b_1}{b_0}a_0 & 0 \\ b_1 & 0 \end{array} \quad (3.20)$$

If all coefficients in the leftmost column are positive, the system is stable. If the coefficients of (3.18) are identified, the following stability criteria results:

$$1 > 0 \tag{3.21}$$

$$\frac{K_{p_i} K_{p_u} L_{dc} P_{load} + (R - K_{p_i}) C e_{dc}^2}{L_{dc} C e_{dc}^2} > 0 \tag{3.22}$$

$$\frac{1}{L_{dc} C e_{dc}^2} \left[\frac{L_{dc}}{T_{i_u}} + R \right] - \frac{R}{T_{i_u} \left(K_{p_i} K_{p_u} L_{dc} P_{load} + (R - K_{p_i}) C e_{dc}^2 \right)} > 0 \tag{3.23}$$

$$\frac{K_{p_i} K_{p_u} P_{load} R}{L_{dc} C T_{i_u} e_{dc}^2} > 0 \tag{3.24}$$

Inequality (3.24) suggests that the closed-loop is unstable for either positive or negative power if $R \neq 0$ or $T_{i_u} < \infty$. This is not necessarily the case for the real system. However, it indicates a problem, either with the linearization or with the non-linear closed-loop system.

The inequality (3.22) is more fundamental. (3.23) and (3.23) can be removed simply by assuming $T_{i_u} = \infty$ and $R = 0$. (3.22) then becomes:

$$\frac{K_{p_i} K_{p_u} L_{dc} P_{load} - K_{p_i} C e_{dc}^2}{L_{dc} C e_{dc}^2} > 0 \iff \tag{3.25}$$

$$|K_{p_u} L_{dc} P_{load}| < C e_{dc}^2 \text{ and} \tag{3.26}$$

$$K_{p_i} < 0 \tag{3.27}$$

The proportional gain K_{p_u} can be parameterized in $k_u C$. This removes the capacitor size C from inequality (3.26), which becomes:

$$|k_u| < \frac{e_{dc}^2}{L_{dc} |\max(P_{load})|} \tag{3.28}$$

Figure 3.1 on the next page illustrates (3.28). The figure shows the result of two simulations with different k_u. In the left simulation, $k_u = 0.95 \cdot e_{dc}^2 / L_{dc} / \max |P_{load}|$ and in the right $k_u = 1.05 \cdot e_{dc}^2 / L_{dc} / \max |P_{load}|$. The integral part in the controller is shut off, i.e. $T_{i_u} = \infty$ and the gain of the current controller is $K_{p_i} = -10^5 \cdot L_{dc}$.

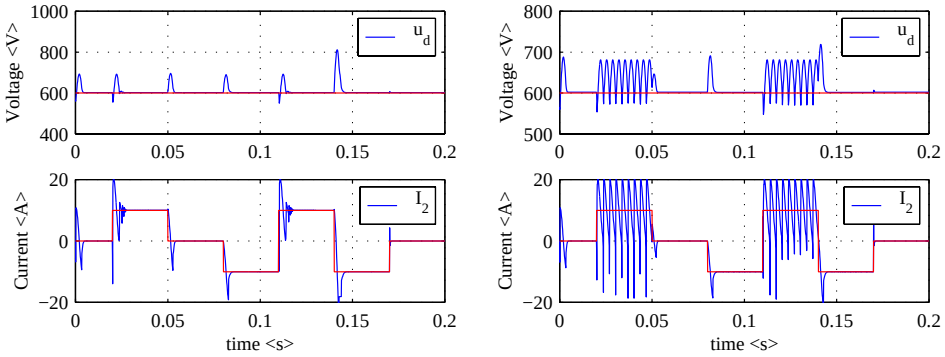

Figure 3.1: Stability depending on k_u.

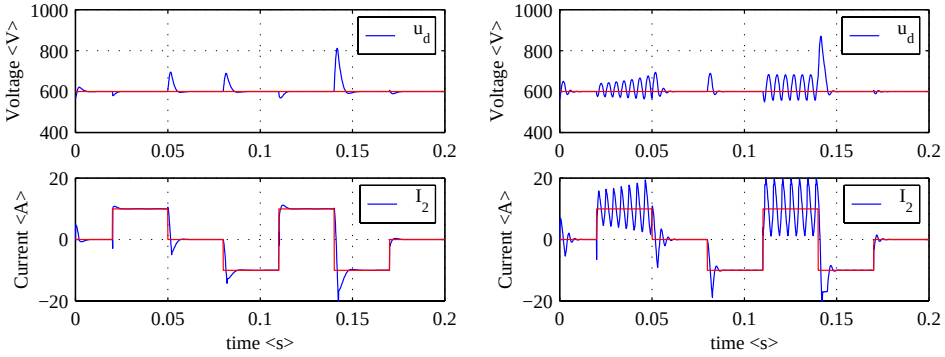

Figure 3.2: Stability depending on Ti.

Figure 3.2 on the facing page illustrates stability depending on T_{i_u}. In the left graph, $T_{i_u} = 1{\cdot}10^{-3}s$, versus in the right graph $T_{i_u} = 3{\cdot}10^{-4}s$. k_u is $0.3 \cdot e_{dc}^2 / L_{dc} / \max|P_{load}|$ and K_{p_i} is $-10^5 \cdot L_{dc}$ in both figures.

3.1.3 Stationary error

The closed loop system should eliminate stationary errors, both if there are errors in the $\hat{\imath}_{load}$ feedforward and in presence of resistance in the line inductors.

In the stationary condition, all state derivatives are zero. The differential equations to then become the following equation system:

$$0 = e_{dc} - K_{p_i}\left[\frac{u_{dc}}{e_{dc}}\left(K_{p_u}\cdot({u_{dc}}^* - u_{dc}) + I_{u_{dc}} + \hat{\imath}_{load}\right) - i_1\right] - Ri_1 \tag{3.29}$$

$$0 = \frac{1}{u_{dc}}K_{p_i}\left[\frac{u_{dc}}{e_{dc}}\left(K_{p_u}\cdot({u_{dc}}^* - u_{dc}) + I_{u_{dc}} + \hat{\imath}_{load}\right) - i_1\right] i_1 - i_{load} \tag{3.30}$$

$$0 = \frac{K_{p_u}}{T_{i_u}}\left[{u_{dc}}^* - u_{dc}\right] \tag{3.31}$$

Substituting (3.31) into (3.30) and (3.29) yields:

$$0 = e_{dc} - K_{p_i}\frac{{u_{dc}}^*}{e_{dc}}\left(I_{u_{dc}} + \hat{\imath}_{load}\right) + (K_{p_i} - R)i_1 \tag{3.32}$$

$$0 = \frac{K_{p_i}}{e_{dc}}\left(I_{u_{dc}} + \hat{\imath}_{load}\right) i_1 - \frac{K_{p_i}}{{u_{dc}}^*}i_1^2 - i_{load} \tag{3.33}$$

Rewriting equation (3.32) gives the following expression

$$\frac{K_{p_i}}{e_{dc}}\left(I_{u_{dc}} + \hat{\imath}_{load}\right) = \frac{e_{dc} + (K_{p_i} - R)i_1}{{u_{dc}}^*} \tag{3.34}$$

The RHS of (3.34) can then be inserted into (3.33) which yields:

$$\begin{aligned} 0 &= \frac{e_{dc} + (K_{p_i} - R)i_1}{{u_{dc}}^*}i_1 - \frac{K_{p_i}}{{u_{dc}}^*}i_1^2 - i_{load} \\ &= \left(e_{dc} + (K_{p_i} - R)i_1\right) i_1 - K_{p_i}i_1^2 - {u_{dc}}^* \cdot i_{load} \\ &= e_{dc}i_1 - Ri_1^2 - i_{load}{u_{dc}}^* \end{aligned} \tag{3.35}$$

Note that $\hat{\imath}_{load}$ is cancelled, this means that a load current transducer with low precision has no effect on the stationary error.

Equation (3.35) has the solutions:

$$i_1 = \frac{e \pm \sqrt{e^2 - 4R \cdot P_{load}}}{2R} \tag{3.36}$$

If the solutions are real, the stationary error is eliminated. This is true for:

$$P_{load} < \frac{e^2}{4R} \tag{3.37}$$

3.1.4 Discussion

Expression (3.28) has good physical interpretation. The controller gain parameter k_u has the dimension $< s^{-1} >$, and it can be viewed as the sampling frequency for a dead-beat controller, controlling the capacitor voltage. The LHS says that a large inductor makes a slow converter, but also that the inductor should be inversely proportional to the nominal power of the converter if performance is to be independent of nominal power.

The fact that the non-linear system is stable for both positive and negative power, despite (3.24) suggests that the analysis is insufficient. The stability of the closed loop system should be examined with methods for non-linear systems.

3.2 Transient response

This section is an analysis of the dynamic behaviour of the circuit during power transients. During transients, the controller output is limited by the converter. Wile the converter limits the control value, the circuit is essentially an uncontrolled, second order LC circuit. The differential equation for this circuit is solved analytically for stepwise changes in power flow. The output voltage exhibit transients whose size is only determined by component values together with voltage and power levels. The solution leads to design rules for the DC-link capacitor in a back-to-back converter.

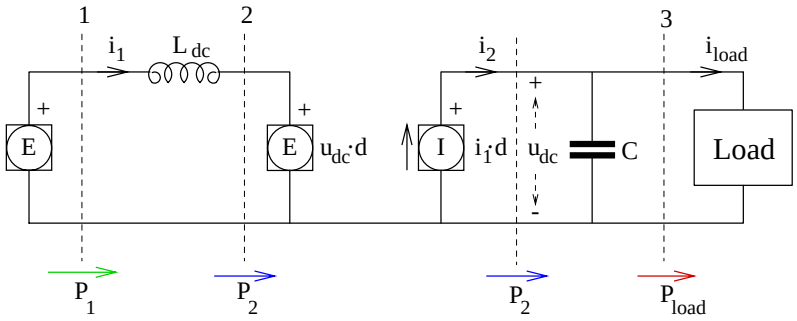

Figure 3.3: Time-averaged model of the circuit in figure 2.7

3.2.1 Circuit model

The circuit described in section 2.2 on page 27 can be modelled using the following equations:

$$\frac{du_{dc}}{dt} = \frac{1}{C}(d \cdot i_1(t) - i_{load}(t)) \tag{3.38}$$

$$\frac{di_1}{dt} = \frac{1}{L_{dc}}(d \cdot u_{dc}(t) - e_{dc}(t)) \tag{3.39}$$

where $d = d_1 - d_2$ is the difference in duty-cycle between the two switch legs of the circuit in figure 2.7 on page 28.

The voltage of the capacitor in the circuit, $u_{dc}(t)$, is assumed to be regulated to a quiescent voltage, U_{dc}. The source voltage is assumed to be constant, i.e $e_{dc}(t) = E_{dc}$.

Before the transients, the output power is P_0. At the start of the transients, the output power instantly changes to P^*. To simplify the analysis, a constant-current load is assumed. The load is assumed to be able to instantly change its power consumption. This makes the analysis simple and can also be considered a "worst case".

The controller for the converter is assumed to have a feed-forward from the load. The feedforward enables the controller to instantly respond to changes in output power.

3.2.2 Case 1: positive transients

A positive transient is a (begins with a) positive, stepwise change in the output power of the converter. For a sufficiently large positive power step, the controller will saturate the duty cycle d to -1.

During the power step then, the converter states can be described by the following equations: (substitute $d = -1$ into (3.38) and (3.39))

$$\frac{du_{dc}}{dt} = \frac{1}{C}(-i_1 - i_{load}) \tag{3.40}$$

$$\frac{di_1}{dt} = -\frac{1}{L_{dc}}(u_{dc} + e_{dc}) \tag{3.41}$$

Together with the following initial and final conditions:

$$\begin{aligned} \dot{u}_{dc}(0) &= \frac{1}{C}\left[-i_1(0) - i_{load}\right] \\ &= \frac{1}{C}\left[-\frac{P_0}{E_{dc}} - \frac{P^*}{U_{dc}}\right] \end{aligned} \tag{3.42}$$

$$i_1(0) = \frac{1}{L_{dc}}\left[U_{dc} + E_{dc}\right] \tag{3.43}$$

$$i_1(t_{final}) = \frac{P^*}{E_{dc}} \tag{3.44}$$

Differentiating (3.40) and then inserting (3.41) into the resulting equation yields a second-order differential equation,

$$\frac{d^2u_{dc}}{dt^2} + \frac{1}{L_{dc}C}\left[u_{dc} + e_{dc}\right] = 0. \tag{3.45}$$

Equation (3.45) is a lossless second-order differential equation. This class of differential equations can be solved by assuming a solution on the form

$$u_{dc} = A\cos\omega_c t + B\sin\omega_c t + f(t). \tag{3.46}$$

Inserting (3.46) into (3.45) yields

$$A{\omega_c}^2 \cos\omega_c t + B{\omega_c}^2 \sin\omega_c t = \\ = -\frac{1}{L_{dc}C}\left[A\cos\omega_c t + B\sin\omega_c t + f(t) + e_{dc}(t)\right] \quad (3.47)$$

Assuming constant source voltage, i.e. $e_{dc}(t) = E_{dc}$, identification of terms in (3.47) gives the following solution parameters

$${\omega_c}^2 = \frac{1}{L_{dc}C} \quad (3.48)$$

$$f(t) = -E_{dc} \quad (3.49)$$

Inserting (3.49) and $t = 0$ into (3.46) and rearranging the gives:

$$A = u_{dc}(0) + e_{dc}(0) = U_{dc} + E_{dc} \quad (3.50)$$

Substituting the time-derivative of (3.46) into (3.40) gives:

$$-A\omega_c \sin\omega_c t + B\omega_c \cos\omega_c t = \frac{1}{C}\left[-i_1(0) - i_{load}\right] \quad (3.51)$$

Inserting $t = 0$ yields:

$$B\omega_c = \frac{1}{C}\left[-i_1(0) - i_{load}\right] \quad (3.52)$$

Which can be further rearranged into:

$$B = -\frac{1}{\omega_c C}\left[i_1(0) + i_{load}\right] \\ = -\sqrt{\frac{L_{dc}}{C}}\left[\frac{P_0}{E_{dc}} + \frac{P^*}{U_{dc}}\right] \quad (3.53)$$

Here, the assumption of a constant-current load is important.

The coefficients of equation (3.46) have been found. It remains to find the solution for t_{final}. This, however, is quite simple. Equation (3.46) can be rewritten as:

$$u_{dc} = \sqrt{A^2 + B^2}\cos\left(\omega_c t + \arctan\frac{B}{A}\right) + f(t) \quad (3.54)$$

Differentiating (3.54), inserting the result into (3.40) and substituting the final condition (3.44) yields after rearranging:

$$i_1(t_{final}) = C \cdot \omega_c \sqrt{A^2 + B^2} \sin(*) - \frac{P^*}{U_{dc}} = \frac{P^*}{E_{dc}} \tag{3.55}$$

Solving (3.55) for $(*)$ gives:

$$(*) = \arcsin\left(\sqrt{\frac{L_{dc}}{C}} \frac{(E_{dc} + U_{dc})P^*}{E_{dc} \cdot U_{dc} \sqrt{A^2 + B^2}} \right) \tag{3.56}$$

The final value of u_{dc} can be found by substituting $\omega_c t_{final} + \arctan \frac{B}{A}$ for $(*)$ in (3.54). However, since $cos(*) = \sqrt{1 - \sin^2(*)}$, $u_{dc}(t_{final})$ can be found directly:

$$u_{dc}(t_{final}) = -E_{dc} + \sqrt{A^2 + B^2} \sqrt{1 - \frac{L_{dc}}{C} \frac{{P^*}^2 (E_{dc} + U_{dc})^2}{E_{dc}^2 \cdot {U_{dc}}^2 (A^2 + B^2)}} \tag{3.57}$$

$$= -E_{dc} + \sqrt{A^2 + B^2 - \frac{L_{dc}}{C} \frac{{P^*}^2 (E_{dc} + U_{dc})^2}{E_{dc}^2 \cdot {U_{dc}}^2}} \tag{3.58}$$

$$= -E_{dc} + \sqrt{(U_{dc} + E_{dc})^2 + \frac{L_{dc}}{C} \frac{(P_0 U_{dc} + P^* E_{dc})^2}{E_{dc}^2 \cdot {U_{dc}}^2} - \frac{L_{dc}}{C} \frac{{P^*}^2 (E_{dc} + U_{dc})^2}{E_{dc}^2 \cdot {U_{dc}}^2}} \tag{3.59}$$

$$= -E_{dc} + \sqrt{(U_{dc} + E_{dc})^2 + \frac{L_{dc}}{C} \frac{(P_0 U_{dc} + P^* E_{dc})^2 - {P^*}^2 (E_{dc} + U_{dc})^2}{E_{dc}^2 \cdot {U_{dc}}^2}} \tag{3.60}$$

3.2.3 Case 2: negative power step

The derivation of the transient output voltage for a negative power step is similar to the derivation for positive steps. It is not necessary to repeat the derivation in full detail.

For sufficiently large negative power steps, $P^* < P_0$, the duty-cycle difference d is set to 1.

The equations are in this case:

$$\frac{du_{dc}}{dt} = \frac{1}{C}(i_1 - i_{load}) \tag{3.61}$$

$$\frac{di_1}{dt} = \frac{1}{L_{dc}}(u_{dc} - e) \tag{3.62}$$

Initial and final conditions:

$$\begin{aligned}\frac{du_{dc}(0)}{dt} &= \frac{1}{C}\left[i_1(0) - i_{load}\right] \\ &= \frac{1}{C}\left[-\frac{P_0}{E_{dc}} - \frac{P^*}{U_{dc}}\right]\end{aligned} \tag{3.63}$$

$$\frac{di_1(0)}{dt} = \frac{1}{L_{dc}}\left[-U_{dc} + E_{dc}\right] \tag{3.64}$$

$$i_1(t_{final}) = \frac{P^*}{U_{dc}} \implies \frac{du_{dc}(t_{final})}{dt} = 0 \tag{3.65}$$

The final condition (3.65) may look a little strange. The point is that u_{dc} varies sinusoidally during the transient, and the peak value is reached when $\frac{du_{dc}(t_{final})}{dt} = 0$.

The parameters in the solution are:

$$A = u_{dc}(0) - e_{dc} = U_{dc} - E_{dc} \tag{3.66}$$

$$B = \sqrt{\frac{L_{dc}}{C}}\left[\frac{P_0}{e_{dc}} - \frac{P^*}{U_{dc}}\right] \tag{3.67}$$

$$f(t) = e_{dc}(t) = E_{dc} \tag{3.68}$$

From the final condition, $\dot{u}_{dc} = 0$, and (3.54) it is easy to see that the peak DC-link voltage is:

$$\begin{aligned}\hat{u}_{dc} &= \sqrt{A^2 + B^2} + E_{dc} \\ &= E_{dc} + \sqrt{(u_{dc}(0) - E_{dc})^2 + \frac{L_{dc}}{C}\left[\frac{P_0}{E_{dc}} - \frac{P^*}{U_{dc}}\right]^2} \\ &= E_{dc} + \sqrt{(U_{dc} - E_{dc})^2 + \frac{L_{dc}}{C} \cdot \frac{(P_0 U_{dc} - P^* E_{dc})^2}{{E_{dc}}^2 {U_{dc}}^2}}\end{aligned} \tag{3.69}$$

P_0	P^*	Voltage deviation		
$<$ kW $>$	$<$ kW $>$	anal.	DC sim.	AC+PWM sim.
-6.0	6.0	574.2	570.8	570.8
6.0	-6.0	811.9	812	807

Table 3.1: Voltage deviations for the simualtion example

3.2.4 Discussion

The above expressions are quite accurate. The calculated voltage deviations are the same as the result of simulations and measurements. See table 3.1 for a comparison between analytical results and simulations. The converter parameters are: $L_{ac} = 7\text{mH} \Leftrightarrow L_{dc} = 14\text{mH}$, $C = 100\mu\text{F}$, and the voltages are: $E_{dc} = 400 \cdot \sqrt{2}\text{V}$ and $U_{dc} = 600\text{V}$.

The actual deviations obtained are slightly dependent on the controller parameters. If the controller has too low gain to saturate the converter, the deviations will be larger. Further, for a positive power step, the result is the solution of the differential equation at t_{final}, the time when the controller should stop saturating the converter. Depending on controller parameters, the deviation may be slightly larger in this case.

The calculations and simulations are performed on ideal (i.e. lossless) models, with stepwise load changes. The deviation in real converters will differ from the theoretical result, from two reasons:

- A real load may not be able to change stepwise, but rather ramps up and down. This is particularly true for electrical drives.
- Real converters have resistance in the line inductances.

The experimental result in table 3.1 gives a hint on the difference between theoretical and practical deviations.

As mentioned before, the results are valid for tree-phase converters. This is true under the assumption of traditional synchronous PID controllers. However, the three-pase converter has an additional degree of freedom; reactive power. The transient performance of the converter can be improved if the reactive power is allowed to temporarily raise during the transient. This has been the subject of papers by Chui and Sui [**?**, **?**]. The obtained voltage deviation is smaller than the theoretical result, but the improvement is small with the converter parameters used by Chui and Sui.

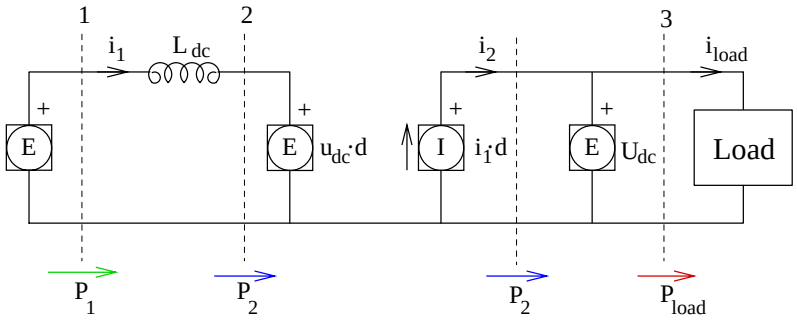

Figure 3.4: Time-averaged model of the circuit used for analysis of energy transients

Given voltage deviation limits and line filter inductor size, the results in this section can be used to determine the size of the DC-link capacitor in e.g. a back-to-back converter.

3.3 Energy transients

This section is a derivation of an expression for the energy received (or supplied) by the DC-link in a back-to-back converter. The idea is to assume constant DC-link voltage, and integrate the instantaneous power flowing into the voltage source during transitions between different power levels. The circuit model used in the analysis is shown in figure 3.4.

3.3.1 A qualitative description

Before the transient, the power transferred by the converter is P_0, equal to the load power. At $t = 0$, the load power instantly changes to P^*. The converter controller instantly changes the input voltage of the converter to drive the input current to the correct value.

The figures 3.5 and 3.6 illustrate a transition from full generation to full motoring, for two different duty-cycle values.

During the transient, energy (ΔW_{dc}) is lost from the DC-link to the load and the line inductors. After the desired input power level is reached, the lost energy must be regained, therefore the input power is raised above the output power for a short time.

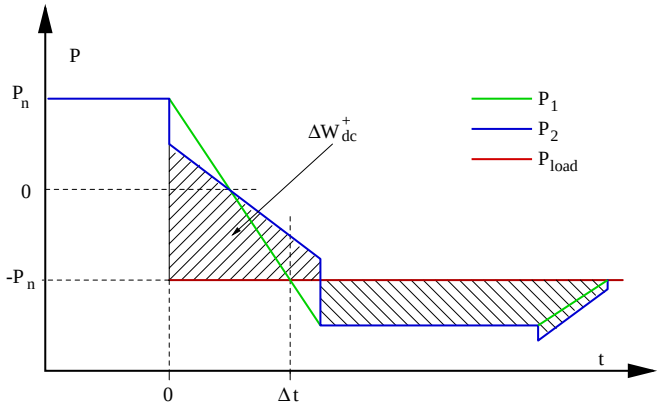

Figure 3.5: Input power and load power consumption during transition from full generation to full motoring, for $d = 0.5$.

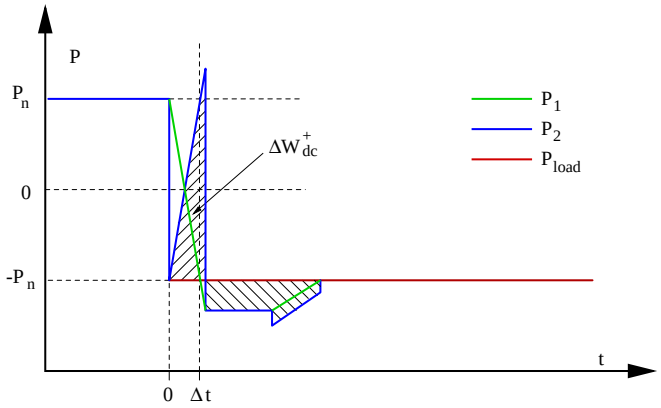

Figure 3.6: Input power and load power consumption during transition from full generation to full motoring, for $d = -1$.

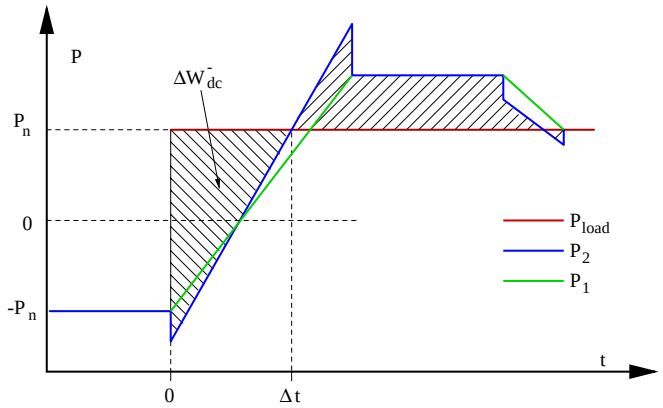

Figure 3.7: Input power and load power consumption during transition from full motoring to full generation for $d = 1$.

The energy delta (ΔW_{dc}) is equivalent to the area between the output power (P_{load}) and the converter input power (P_2). Both figures are drawn in the same timescale. Note the smaller energy delta in figure 3.6

Figure 3.7 illustrates a transition from full power motoring to full power generation (breaking). In this case, ΔW_{dc} is positive, and (more important) larger than in the two previous examples. This is due to the smaller voltage difference available to change the input current.

3.3.2 An expression for ΔW_{dc}

A derivation of ΔW_{dc} will now follow. Assume that the load power abruptly changes from P_0 to P^* at $t = 0$. During the transient, the following is valid:

$$P_{load}(t) = P^*$$
$$P_2(t) = i_1 \cdot u_1 = i_1(t) \cdot d(t) \cdot U_{dc} \tag{3.70}$$
$$\frac{dW_{dc}}{dt} = P_2(t) - P_{load}(t) = P_2(t) - P^*. \tag{3.71}$$

Assuming constant u_1 and e we get

$$\begin{aligned} i_1(t) &= i_1(0) + \int_0^t \frac{di_1}{dt} d\tau = \\ &= \frac{P_2(0)}{e_{dc}} + \int_0^t \frac{e - u_1}{L_{dc}} d\tau = \\ &= \frac{P_0}{e_{dc}} + \frac{e - u_1}{L_{dc}} \cdot t \end{aligned} \tag{3.72}$$

And then by inserting (3.72) into (3.71):

$$\frac{dW_{dc}}{dt} = \frac{P_0 u_1}{e_{dc}} + \frac{e_{dc} - u_1}{L_{dc}} \cdot u_1 \cdot t - P_{load}(t) \tag{3.73}$$

Inserting $P_{load}(t) = P^*$ into (3.73) and integrating yields

$$W_{dc}(t) = \frac{P_0 u_1}{e_{dc}} \cdot t + \frac{e_{dc} - u_1}{L_{dc}} \cdot u_1 \cdot \frac{t^2}{2} - P^* \cdot t \tag{3.74}$$

The transient response time t_{final} can be found from solving $\{\Delta i_1 \cdot e = \Delta P\}$ for Δi_1, inserting the solution into (3.72) and solve for t:

$$\Delta i = \frac{(P^* - P_0)}{e_{dc}} \implies t_{final} = \frac{L_{dc}(P^* - P_0)}{e_{dc}(e_{dc} - u_1)} \tag{3.75}$$

Inserting (3.75) in (3.74) yields

$$\begin{aligned} W_{dc,trans} &= \frac{u_1(e_{dc} - u_1)}{L_{dc}} \cdot \frac{L_{dc}^2 (P^* - P_0)^2}{2e_{dc}^2 (e_{dc} - u_1)^2} - \frac{L_{dc}(P^* - P_0)}{e_{dc}(e_{dc} - u_1)} \left[P^* - \frac{u_1}{e} P_0 \right] \\ &= \frac{L_{dc}(P^* - P_0)}{2e_{dc}^2 (e_{dc} - u_1)} \left[u_1 (P^* - P_0) - 2e_{dc} P^* + 2u_1 P_0 \right] \\ &= \frac{L_{dc}(P^* - P_0)}{2e_{dc}^2 (e - u_1)} \left[(u_1 - 2e_{dc})(P^* - P_0) + 2(u_1 - e_{dc}) P_0 \right] \\ &= -\frac{L_{dc}(P^* - P_0)^2}{2e_{dc}^2} \cdot \left[\frac{2e_{dc} - u_1}{e_{dc} - u_1} + \frac{2P_0}{P^* - P_0} \right] \end{aligned} \tag{3.76}$$

Equation (3.76) expresses the amount of energy forced into (or out of) the DC-link during a transient, assuming constant u_1 during the transient.

Since no assumptions were made on P^* and P_0 in the derivation, expression (3.76) is valid both for positive and negative power steps.

From (3.75) it is obvious that the value of u_1 is affected by the sign of $\Delta P = P^* - P_0$. With the assumptions $t > 0$ and $e > 0$, rewriting (3.75) yields:

$$t > 0, \quad e_{dc} > 0 \Rightarrow \frac{P^* - P_0}{e_{dc} - u_1} > 0 \Rightarrow$$
$$\begin{cases} u_1 < e_{dc} & \text{if } P^* > P_0 \\ u_1 > e_{dc} & \text{if } P^* < P_0 \end{cases} \tag{3.77}$$

3.3.3 Minimizing ΔW_{dc}

Differentiating (3.76) with respect to u_1 yields

$$\frac{\partial W_{dc}}{\partial u_1} = -\frac{L_{dc}(P^* - P_0)^2}{2e_{dc}(e_{dc} - u_1)^2} \tag{3.78}$$

which obviously is negative for all u_1. This means that expression (3.76) does not have a global minimum or maximum with regard to u_1. Minimizing ΔW_{dc} is then a matter of applying the maximum available u_1 with correct sign, given the constraint $|u_1| \leq u_{dc}$, equivalent to $u_1 = \pm u_{dc}$. Equation (3.77) then becomes:

$$t > 0, \quad e_{dc} > 0 \Rightarrow \frac{P^* - P_0}{e_{dc} - u_1} > 0 \Rightarrow$$
$$\begin{cases} u_1 = -U_{dc} \Leftrightarrow d = -1 & \text{if } P^* > P_0 \\ u_1 = U_{dc} \Leftrightarrow d = 1 & \text{if } P^* < P_0 \end{cases} \tag{3.79}$$

3.3.4 Discussion

Table 3.2 on the next page lists the energy taken up by the DC-link in the example converter. The u_1 value is the DC/DC equivalent. The three-phase AC voltage equivalent is $u_1/\sqrt{2}$.

Obviously the injected energy is much larger when $P_0 > P*$ than the opposite. This is because of the difference in current derivative and transient time. Compare with equation (3.72). The higher U_{dc} is chosen, the less difference. There is often an upper limit for u_{dc} which may not be exceeded. If the DC-link has a very small capacitor, a brake chopper will be needed to limit the DC-link voltage during transients. If the transient intensity (number of transients per second) can be estimated, equation (3.76) can be used to determine the power rating for the brake resistor.

P_0 < kW >	P^* < kW >	u_1 < V >	ΔW_{dc} < Ws >
0.0	6.0	−600	−1.17
−6.0	0.0	−600	0.41
−6.0	6.0	−600	−1.52
−6.0	6.0	−750	−1.35
0.0	−6.0	600	12.19
6.0	0.0	600	13.77
6.0	−6.0	600	51.93
6.0	−6.0	650	21.13
6.0	−6.0	750	9.67

Table 3.2: Energy taken up by the DC-link.

Chapter 4

Design

In the previous two chapters, analytical expressions have been derived for DC-link voltage deviations and DC-link energy transients. This chapter transforms the result into design suggestions and rules of thumb for back-to-back power converters.

The conclusion is that it is certainly feasible to build a converter with a very small DC-link capacitor, making the use of plastic capacitors possible (and necessary!). To be able to reduce the capacitor as much as possible, however, it is necessary to include a switched brake resistor in the design.

4.1 Line filter

The design of the line filter is outside the scope of this thesis. However, a simple derivation seen in this chapter. This does not mean that this is a simple task. The line filter serves two purposes:

1. Short term energy storage for the boost-type converter.
2. Keeping the switching noise away from the power grid.

Other issues are losses in the inductors, physical size, price, etc.

Since almost any size of the inductors gives sufficient energy storage, the main factor is RFI[1] and switch frequent noise. This makes it natural to look at the filtering properties.

[1] RFI = Radio Frequent Interference

Basically, the switching noise in the line currents are determined by the size of the inductors together with the converter output voltage. A very simple model for determining the size of the switching ripple in the active current is a simple DC/DC switch, where the converter output can be either $\sqrt{2/3}U_{dc}$ or zero, and the line voltage is E_h. If a lossless inductor is assumed, the current ripple amplitude becomes:

$$\Delta i = \frac{T_{sw}E_h}{L}\left[1 - \frac{E_h}{\sqrt{2/3}U_{dc}}\right] \tag{4.1}$$

For high-powered equipments, the guidelines for line current distortion are expressed in relative harmonic levels, see table 1.2 on page 8. The allowed line-current ripple is proportional to the nominal line current, or $\Delta i = k_d \cdot i_n$. The norms essentially give the allowed Fourier coefficients for the ripple.

The switch-frequent fundamental of the current ripple is smaller than the peak-to-peak amplitude. The Fourier series for the current ripple is:

$$b_k = \frac{T_{sw}E_h}{L}\frac{\sin(k\pi\sqrt{\frac{3}{2}}\frac{E_h}{U_{dc}})}{k^2\pi^2\sqrt{\frac{3}{2}}\frac{E_h}{U_{dc}}} \tag{4.2}$$

Given an allowed fourier coefficient b_k the size of the line inductor can be calculated:

$$L = \frac{T_{sw}E_h}{b_k \cdot i_n}\frac{\sin(k\pi\sqrt{\frac{3}{2}}\frac{E_h}{U_{dc}})}{k^2\pi^2\sqrt{\frac{3}{2}}\frac{E_h}{U_{dc}}} \tag{4.3}$$

or, if the nominal line current is expressed in nominal power, P_n:

$$L = \frac{T_{sw}{E_h}^2}{b_k \cdot P_n}\frac{\sin(k\pi\sqrt{\frac{3}{2}}\frac{E_h}{U_{dc}})}{k^2\pi^2\sqrt{\frac{3}{2}}\frac{E_h}{U_{dc}}} \tag{4.4}$$

Expression (4.4) can be used to calculate a rule of thumb for the size of the line inductor, expressed in Watts·Henry. Table 4.1 lists the result

	DC-link voltage			
b_k	600	650	700	750
0.10	10.8	15.0	18.7	22.0
0.05	21.6	30.0	37.5	44.0
0.02	54.1	75.0	93.7	110
0.006	180	250	312	366
0.0036	300	418	521	611

Table 4.1: Line inductance-power product for $E_h = 400$, $T_{sw} = 100\mu$s

for 400 volts main voltage, and 10 kHz apparent switching frequency (5 kHz carrier).

The last rows in the table are for ripple levels that comply with IEC 1000-3-4 and IEC 1000-3-2 (compare table 1.2 on page 8). The converter used in illustrations in this thesis does not comply with the norms, since the inductance-power product is only 42 WH (6kW·7mH).

This illustrates the necessity to use an LCL line filter configuration if a high bandwidth is desired. An LCL filter gives the designer more options for fine-tuning the performance. With an LCL filter the inductance-power product of the inductors can be made quite small, but this will also increase eddy-current losses in the inductors. It may be necessary to use litz wire on iron-powder cores for the "inner" inductor to reduce losses to acceptable levels.

4.2 DC-link capacitor limit

Power converters with controlled rectifiers have bidirectional power flow, together with a very wide control bandwidth mainly limited by the line filter. If those properties are used for regulation of the DC-link voltage, the DC-link capacitor can be quite small. This section derives the limiting factors for capacitor size. The minimum size is expressed in terms of the line filter and rated power of the converter.

4.2.1 Switch-frequent voltage ripple

The DC-link capacitor current is discontinuous. The input current is switched on and off with the switching frequency of the converter. This induces a voltage ripple in the DC-link. This voltage ripple must be

made small enough for the voltage to be virtually constant during a switch period. This sets a lower limit on the capacitor size.

A rough estimate (worst case!) on the ripple can be made by assuming a load that draws constant, continuous current, i_{load}, and an input converter boosting the input voltage a hundred times. The high boost rate of the input converter means that the capacitor current will be $-i_{load}$ for most of the time, with $99 \cdot i_{load}$ impulses. The ripple will be a sawtooth shape whose amplitude is:

$$\Delta u_{dc} = \frac{T_{sw}}{C} i_{load} \tag{4.5}$$

Real converters (electronic flashes exempted) do not use this kind of boost rates. At most, the input voltage is doubled, which makes the ripple amplitude half of that above. Expression (4.5) can be extended with the relation between input voltage e_{dc} and DC-link voltage u_{dc}:

$$\Delta u_{dc} = \left[1 - \frac{e_{dc}}{u_{dc}}\right] \frac{T_{sw}}{C} i_{load} \tag{4.6}$$

Synchronizing the switching of the input and output converters in a back-to-back converter reduces the ripple even further. Although both the input current and the output current are discontinuous in the DC-link, the pulses occur simultaneously, reducing the capacitor current ripple.

By inserting $P_{load} = u_{dc} i_{load}$ into (4.6) and solving for the capacitor size C, the following expression emerges:

$$C \geq \frac{T_{sw} P_{load}}{\Delta u_{dc} u_{dc}} \left[1 - \frac{e_{dc}}{u_{dc}}\right] \tag{4.7}$$

Table 4.2 on the facing page is an illustration of expression (4.7). The table lists the necessary capacitor size expressed in μF/kW converter power, for a converter connected to a 400V power grid that has a 10 kHz apparent switching frequency. For instance, the converter example, with 6 kW nominal power and 600 volts DC-link voltage needs a 10 μF DC-link capacitor to keep the voltage ripple below 1%

	DC-link voltage			
Δ (%)	600	650	700	750
2.0	0.79	1.53	1.96	2.18
1.0	1.59	3.07	3.91	4.37
0.5	3.18	6.14	7.83	8.73
0.2	7.94	15.3	19.6	21.8

Table 4.2: Capacitor size per nominal converter power in μF/kW

4.2.2 DC-link voltage deviation limit

The result of section 3.2 give expressions for the maximum voltage deviation during power transients. The derivation is done for stepwise changes, which is the worst case. If the load is a variable speed drive, the load power can change immediately from motoring to generation. The opposite is slower though, particularly near full speed. This means that the voltage deviation will be near the theoretical result for transitions from motoring to generation.

Another transient source is tripping of circuit breakers. If a circuit breaker on the load side trips during motoring, the DC-link voltage will rise shortly until the line converter has reduced input power to zero. The same occurs if a breaker trips on the line side during generation. In the latter case, the inductance of the load must be used in the expressions below.

Expression (3.69) estimates the highest DC-link voltage during a transient. The capacitor size can be solved from this expression, which then yields:

$$C = \frac{L\left(P_0 U_{dc} - P^* E_{dc}\right)^2}{{E_{dc}}^2 {U_{dc}}^2 \left[\left(\hat{u}_{dc} - E_{dc}\right)^2 - \left(U_{dc} - E_{dc}\right)^2\right]} \tag{4.8}$$

If a step change from positive nominal load $P_0 = P_n$ to negative nominal load $P^* = -P_n$ is considered, the expression can be simplified to:

$$C = \frac{L{P_n}^2\left(U_{dc} + E_{dc}\right)^2}{{E_{dc}}^2 {U_{dc}}^2 \left[\left(\hat{u}_{dc} - E_{dc}\right)^2 - \left(U_{dc} - E_{dc}\right)^2\right]} \tag{4.9}$$

	nominal DC-link voltage			
$\max(u_{dc})$	600	650	700	750
650	78.6	–	–	–
700	28.0	40.0	–	–
750	14.4	16.3	25.6	–
800	8.78	9.15	11.1	18.4

Table 4.3: DC-link capacitor size required to limit positive voltage transients.

Table 4.3 illustrates expression (4.9). The table lists the capacitor value resulting from (4.9) for $E_dc = 400\sqrt{2}$ V and $L = 40/P_n$ WH.

As mentioned before, positive power transients are slower, which means that the theoretical result may overestimate the deviation. Nevertheless, section 3.2 derives the DC-link voltage for transitions from generation to motoring, (3.60). Solving C from this expression yields:

$$C = L\frac{(P_0 U_{dc} + P^* E)^2 - P^{*2}(E + U_{dc})^2}{E^2 \cdot {U_{dc}}^2 \left[(u_{dc}(t_{final}) + E)^2 - (U_{dc} + E)^2\right]} \tag{4.10}$$

Making similar substitutions, $P_0 = -P_n$ and $P^* = P_n$, (4.10) yields:

$$C = \frac{LP_n^2 \left[(E - U_{dc})^2 - (E + U_{dc})^2\right]}{E^2 \cdot {U_{dc}}^2 \left[(\min(u_{dc}) + E)^2 - (U_{dc} + E)^2\right]} \tag{4.11}$$

Table 4.3 illustrates expression (4.9). The table lists the capacitor value resulting from (4.11) for $E_dc = 400\sqrt{2}$ V and $L = 40/P_n$ WH.

Depending on the actual configuration and switching frequency, the DC-link capacitor should be chosen from the largest of the three expressions. The capacitor size depends heavily on the inductance of the line inductors. Depending on the line filter design, the capacitor value must be found by inserting real filter values. The tables give only a hint on the reasonable capacitor size. *It is not recommended to base a real design on the tables only.*

The tables are calculated using assumptions on the line filter. A back-to-back converter in an electrical drive has an inductive load which from the converter perspective looks similar to the line side. The correct

	nominal DC-link voltage			
$\min(u_{dc})$	600	650	700	750
575	8.18	2.46	1.34	0.87
600	–	3.65	1.66	1.01
625	–	7.23	2.19	1.20
650	–	–	3.26	1.49
675	–	–	6.45	1.97
700	–	–	–	2.92

Table 4.4: DC-link capacitor size required to limit negative voltage transients.

dimensioning of the DC-link capacitor depends also on the inductance of the load. Particularly, a large inductance in the load can cause a DC-link voltage peak that breaks the converter in the event of circuit-breaker tripping on the line-side during generation, if the load inductance is not accounted for. Thus, the above expressions for the DC-link capacitor must be evaluated using the load-side parameters also.

4.3 Brake chopper

When designing a converter for a drive with large load inductances, the capacitor size obtained from the previous section may be larger then desired. Then if it is expression (4.9) that gives a substantially larger capacitor than both (4.6) and (4.11), the expression can be disregarded if a brake chopper is included in the converter.

In a traditional converter with a diode rectifier, the brake chopper is necessary to take care of the braking energy when the machine driven by the converter is stopped. This energy may be rather large. A 2 kW induction machine may have an inertia of 0.08 Nm/s^2 yielding a rotational energy of 2 kJ at 1500 r/m. This may require an average power rating for the brake resistor near the rated power of the converter.

In a back-to-back converter, a brake chopper can be used to limit the DC-link voltage during transients. The difference is the average power rating. Instead of consuming the whole rotational energy, only the transient must be taken care of by the brake resistor. Most of the energy is fed back to the power grid.

In fault situations, a brake chopper is useful to consume transients

$\max U_{dc}$	inductance-power product <WH>						
<V>	10	20	40	80	160	320	640
650	0.42	0.84	1.68	3.35	6.71	13.42	26.84
700	0.26	0.53	1.05	2.11	4.21	8.42	16.85
750	0.19	0.38	0.77	1.53	3.07	6.14	12.28
800	0.15	0.30	0.60	1.21	2.41	4.83	9.66

Table 4.5: Transient energy consumed in brake resistor in Joule per nominal converter power in kW

that would otherwise break the converter. In the worst case, all magnetic energy stored in a drive must be consumed by the DC-link capacitor. If the capacitor is small, the energy may result in a voltage higher than the breakdown voltage of the semiconductors. A correctly dimensioned brake chopper will save the converter bridges from breakdown, and the converter operator from costly repairs.

The energy that has to be consumed in the brake resistor can be calculated with expression (3.76). By the same substitutions as above, this expression can be simplified to:

$$W_{dc,trans} = -\frac{2LP_n{}^2}{e^2} \cdot \left[\frac{2e - \max(u_{dc})}{e - \max(u_{dc})} - 1\right] \tag{4.12}$$

Table 4.5 illustrates (4.12). The table lists the energy consumed by the brake resistor in terms of the nominal power of the converter. The table is calculated for 400 Volts mains voltage. The inductance-power product, $L \cdot P_n$ is substituted in expression (4.12) to give a linear relationship between the table and the energy.

The average power rating for the brake resistor can be determined by multiplying the energy consumed per transient, with the expected number of transients per second. If there are 10 full-power transients per second, a converter with a 320 WH line choke and 700 Volts voltage limit, will consume about 8.5 % of the rated power in the brake resistor.

4.4 Conclusion

Using the expressions derived in this thesis, the minimum size for the DC-link capacitor in a back-to-back converter can be determined. The

necessary capacitor size depends on the existence of a brake chopper. To be able to use small plastic capcitor types, a brake chopper is required. The average power rating of the brake resistor can be quite small, however.

Part II

Controller hardware

Chapter 5

A MIMO control computer

This chapter is a description of the IEA-MIMO control computer. It begins with an overview of the design, with motivations and design goals. Then the parts of IEA-MIMO are described in detail.

5.1 Overview

The department of industriel electrical engineering and automation had experience with a floating-point processor board from National Instruments that, together with a general I/O board, was situated inside of a Macintosh IIci computer. The processing performance of this combination is excellent, but the I/O handling is painfully slow. The I/O could cost as much as half the processing time per sample interval, for a typical electrical drive controller.

The result from this experience was a desire for a more powerful control computer. Perhaps not more powerful in processing, but the I/O should be much faster.

5.1.1 Design goals

The design goal was to design a control computer capable of controlling a back-to-back three-phase power converter in a high-performance servo drive, with 10 kHz sampling frequency.

operation	$x \pm y$	$x \cdot y$	x/y	$\sqrt{1/x}$
float x/y by newton	12	12	-	-
float $\sqrt{1/x}$ by newton	12	18	-	-
$\frac{u}{\|\|\vec{u}\|\|}$	1	4	-	1
2-d vector rotation	2	4	-	-
PI-controller	4	3	-	-
order n state observer	$3n(n-1)$	$3n^2$	-	-
$\sin(\phi/2)$ from cos	1	3	-	1
2-d vector limiter	2	7	-	1
2-3 phase transform	2	5	-	-
3-2 phase transform	1	3	-	-
1:st order filter	2	3	-	-
3-phase duty-cycle calc.	-	3	1	-
scaling	-	1	-	-
Line controller	30	70	1	4
U_{dc} controller	6	8	2	-
IM controller	100	150	1	4
Back-to-back controller	130	220	3	8

Table 5.1: Algorithm complexity

Processing demands

To define the processor demands, the complexity of the control algorithms were estimated. Table 5.1 shows one result. The upper part of the table lists the complexity for some controller building blocks, and the lower part for whole controllers. The numbers are approximate in the lower part.

The required processing speed was determined by assuming the number of flops needed per sampling interval was roughly the numbers for back-to-back controller in table 5.1 (about and dividing by the required sampling interval. If it is assumed that add/subtract and multiplication is equally fast, but division and square root must be perfomed with newtons algorithm, the back-to-back controller requires about 650 operations per sample interval. This would correspond to 6.5 million floating point operations per second if the sampling frequency is 10 kHz.

Application requirements

According to the above result and an estimated need for I/O, the requirements for the reference application were stated as follows:

- Processor capacity of (at least) 10 million floating-point operations per second in "real applications".
- At least nine high-speed analog inputs.
- Six pulse-width modulator channels.

In the initial discussions on the design, it was decided to leave out the pulse-width modulators. The motive was that including this function in the design would make the board less flexible. There are many ways of controlling power converters, and including just one of them would be a bad idea. Instead, the modulator should reside on a separate board, with some kind of link to the control computer.

It was also decided that means for communication should be included, as well as multiple analog outputs. The latter are primarily useful for monitoring, but some applications require analog control also.

5.1.2 Processor alternatives

After long consideration, the TMS320C30 was chosen, primarily because of previous experience and trust in Texas Instruments as a long-term supplier of processors. Also, the performance of the processor was thought to be sufficient; during scalar-product, the TMS320C30 performs 20 million multiplications per second. General calculations can be performed at about five million floating-point operations per second, if programmed in C.

Other processors taken into consideration was:

ADSP 21020 This processor, and in particular its cousin, ADSP2106X ("SHARK"), is a very powerful signal processor. The Harward architecture and the long instruction word (48 bits!) contributes to the speed of this processor. The ADSP2106X versions has large, reconfigurable, memories built in, and can at startup read a program from an ordinary 8-bit-wide EPROM. If the program is not too big, the only external memory needed is an EPROM. Unfortunately, ADSP2106X was "too new".

DSP 96002 The Motorola alternative had been used by NTH in a similar project. It is a splendid processor, with a very advanced bus interface. It works particularly well as a co-processor in larger systems. This processor was chosen initially, but when Motorola decided to stop further development of its floating-point signal processors, the TMS320C30 was chosen instead.

DSP 32c from AT&T This processor was never seriously considered an alternative. Not so positive experience from a neighbour department was a major factor in this decision.

PowerPC from IBM and Motorola: The PowerPC was quite new when this project was started. It is not a signal processor, but the floating-point unit is comparable in speed with the fastest signal processors available. The PowerPC can execute integer and floating-point operations in parallel, which improves performance for controller applications.

5.1.3 Inputs, outputs and communication

Apart from being a self-contained module, the [analog] I/O was considered the most important property of the control computer. The previous combination of processor and I/O boards had rather slow I/O performance. For instance, A/D conversion took about 30 μs to set up for each sample interval and had a 10 μs conversion time per channel. Furthermore, the analog inputs were not sampled simultaneously. Pulse-width modulation had similar timing.

Consequently, an important goal for IEA-MIMO was to have really fast and effective I/O. Shortening the time for I/O operations would give more time for control algorithms.

Analog input

Most important to speed up was the analog input. Two different configurations were considered:

- A multiplexed input, with separate sample/hold gates on each input.
- Multiple A/D converters operated in parallel.

The first alternative was eventually chosen. A multiplexed input gives sufficient performance, allows for a large number of channels on limited board space and uses less expensive components

The second is not a very attractive alternative, since multiple A/D converters may require large board space. For a multiple converter alternative to be interesting, a single converter should not take up more board space than an ordinary operational amplifier. These converters have serial interfaces, which are easy to handle if there are one or two converters, but a sixteen-channel input will be more complicated.

There are several A/D converter systems with built in multiplexer, but few of them has a conversion time shorter than 10 μs per channel. This is not faster than most general I/O boards. Consequently, using a complete converter system was no alternative.

When evaluating the A/D converters available on the market, it was found that the fastest available conversion rate was more than enough, even at 12 bits resolution, but that A/D converters faster than around 2 MSPS[1] were always pipelined.

A pipelined converter completes one full conversion per clock cycle, but the result is delayed e.g four clock cycles. Using a pipelined converter together with a multiplexer is tricky if it is not run continuously, especially when it comes to resolving channel information.

The hardest speed limit, however, was set by the available multiplexers. Very few multiplexers can switch between channels in less than 1 μs, while guaranteeing 12 bits resolution. The fastest available can switch in about 500 ns. Because of this fundamental limit, the conversion interval was chosen to around 1 μs. This interval allows conversion of 16 channels in 16 μs.

Analog output

Concerning the analog output, the only requirement was that there should be multiple channels. This requirement limits the number of alternative converter circuits, since only those with multiple converters in a single package would be acceptable in terms of board space.

It is also desirable to have the D/A converters double-buffered. Double-buffering means the outputs can be synchronously updated, which is desirable from a controller perspective.

These requirements lead to the choice of two quadruple D/A converters.

[1] MSPS = Million Samples Per Second

Communication ports

It is necessary to have some means of communication. Applications often require data transfers to/from a supervising computer or a host computer. There are basically three alternatives for this kind of communication:

- Asynchronous serial port.
- Ethernet.
- Token ring.

Of these alternatives, only the first was considered simple enough to implement. Although there are complete Ethernet controllers available, the ethernet controller requires access to part of the main memory for its buffers. An ethernet controller would also have required bus arbitration logic. This is by no means impossible to implement, but it was not considered worth the trouble.

The chosen alternative is a standard UART[2], with a separate electrical interface on a small daughter card.

5.1.4 Result: the IEA-MIMO

The control computer, IEA-MIMO is a single-board computer built around a floating-point processor from Texas Instruments, the TMS320C30. The computer is designed to solve demanding control problems in general and electrical drive control problems in particular. The computer is intended to be a part of a rack-mount system, where other boards contain transducers or actuators.

The I/O subsystems of IEA-MIMO have been designed with modern control theory in mind. Because of limited board space, only the most general I/O were included. Specialized inputs or outputs have been deferred to application specific boards. The I/O subsystems included are:

- Sixteen analog inputs (range: ± 10 Volts, resolution: 12 bits, conversion time: 16μs for all channels, synchronous (parallel) sampling).
- Eight analog outputs (range: ± 10 Volts, resolution: 12 bits, parallel updating).

[2]UART = Universal Asynchronous Receiver/Transmitter

- Eight digital inputs/outputs.
- One digital trigger input.
- A 16550 compatible UART.
- A display port for ascii LCD displays.
- Six digital signals for keypads or LED:s.
- Two synchronous serial ports for communication between multiple IEA-MIMO boards.

In addition, IEA-MIMO has been equipped with a DSPLINK bus for expansion boards. The DSPLINK bus is a 16-bit bus, with 16-bit address and separate memory and I/O spaces. Application specific I/O boards can with this bus get high-speed digital communication with IEA-MIMO. Examples on boards that use this bus are:

- A 6-channel PWM modulator for power electronics control (see chapter 6).
- A resolver board, for angle and speed measurements.
- Relay boards.

Since IEA-MIMO is primarily intended for research activities, the control logic is implemented in programmable circuits. This makes it possible to adapt the computer to applications not foreseen at the design phase.

5.2 Functional description

IEA-MIMO is built around a floating-point DSP from Texas Instruments inc., the TMS320C30. The chosen processor has two separate buses, a main bus intended for the memory system, and a secondary bus intended for I/O units. This separation has been used in IEA-MIMO, with the exception of the DSPLINK expansion bus.

Figure 5.1 on the next page is a block diagram of IEA-MIMO. It shows the electrical grouping of major parts around the CPU.

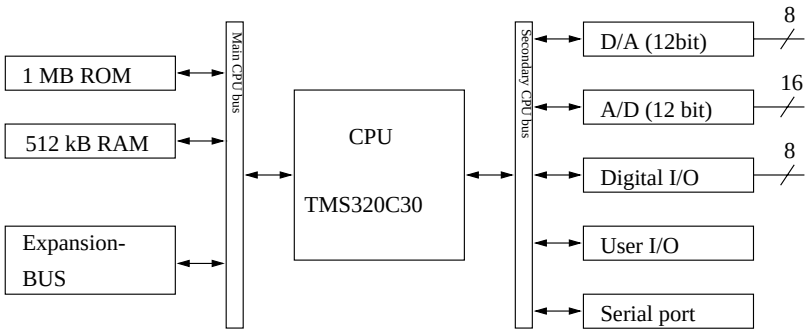

Figure 5.1: IEA-MIMO block diagram

5.2.1 Processor

The TMS320C30 is a RISC-like processor, in that its pipelined and can complete one instruction of most instruction types each clock cycle. It is intended for signal processing applications. For this reason it has special addressing modes, and instructions, that help implementation of signal processing algorithms. The TMS320C30 operates on floating-point numbers. This makes it easy to program, in contrast to fixed point processors where the programmer must think about the decimal point, scaling and overflow.

From the programmers perspective, the TMS320C30 is a conventional von Neumann architecture[3]. To improve performance for signal processing applications, the TMS320C30 uses multiple physical buses; Internally, there are three data buses and four address buses. The TMS320C30 can perform one transaction each clock cycle on each of its internal buses. There are two independent external buses connected to one internal bus each.

Thanks to the floating point support, IEA-MIMO can be programmed in the C programming language with decent performance. This makes it a very powerful research tool. A controller can be quickly developed. Even faster development can be achieved if C code generation tools, like Simulink Real-Time Workshop, are used (with decreased performance though).

[3]Program and data are stored in the same memory space.

Address map

The TMS32C30 has itself two address map configurations. One address configuration (microcomputer mode) maps the on-chip ROM into the lowest addresses in the memory map, and the other configuration (microprocessor mode) maps external memory into the address space. The IEA-MIMO uses the microprocessor mode, i.e. the on-chip rom is not mapped into the memory map. There is no way to configure the CPU in microcomputer mode.

Table 5.2 on the following page shows the memory map for IEA-MIMO. The following sections describe the I/O units and the memory configuration, including register bits.

Clock circuits

The IEA-MIMO computer is clocked by a 40 MHz crystal oscillator. The oscillator feeds the clock input of the CPU and one clock input of the board logic. The CPU in turn generates a 20 MHz two-phase clock, designated `h1` and `h3` respectively. Those clock signals are fed into the board logic. The `h1` clock signal also feeds the wait state generator for the main memory bus, and the `h3` clock signal feeds the debug port (see below).

Debug port

The TMS320C30 has a debugger port. An emulation pod can be connected to this port, and the processor can be controlled entirely through this port, acting as an In-Circuit Emulator for itself. This port is made available with the connector specified in TMS230C30 users manual.

Built-in I/O

The TMS320C30 has a few built-in peripherals. Some of them has been utilized on the IEA-MIMO computer. Others, notably the serial ports, are not used for any particular purpose, but their specific pins have been made available for future needs.

The CPU has two timers, that can be used for timing measurement, clock generation, and pulse counting. The timers have one dedicated pin each, which can be used both as an input and as an output. The `timer1` pin is connected to a clock input of the board logic, while the `timer0` pin is connected to a general I/O-port of the board logic. Currently,

Address	Function
0x000000 -- 0x03ffff	256 kWords of EPROM (memconf = 0)
0x000000 -- 0x01ffff	128 kWords of RAM (memconf = 1)
0x200000 -- 0x21ffff	128 kWords of RAM
0x400000 -- 0x43ffff	256 kWords of EPROM
0x804000 -- 0x804007	D/A load registers
0x804008 -- 0x804008	A write updates D/A outputs
0x80400C -- 0x80400c	A write resets D/A outputs
0x804010 -- 0x804010	A/D FIFO buffer (read-only), a write triggers conversion
0x804020 -- 0x804020	Digital I/O bits
0x804024 -- 0x804024	Digital I/O direction
0x804028 -- 0x804028	Interrupt mode register
0x80402c -- 0x80402c	Memory configuration (memconf)
0x804030 -- 0x804030	User button registers
0x804034 -- 0x804034	LED control register
0x804060 -- 0x804061	ASCII display port
0x804070 -- 0x804077	UART control registers
0x808000 -- 0x80801f	TMS320C30 dma registers
0x808020 -- 0x80802f	TMS320C30 timer0 registers
0x808030 -- 0x80803f	TMS320C30 timer1 registers
0x808040 -- 0x80804f	TMS320C30 serial port0 registers
0x808050 -- 0x80805f	TMS320C30 serial port0 registers
0x808060 -- 0x80806f	TMS320C30 bus control registers
0x809800 -- 0x809fff	2 kWords of internal RAM
0xa00000 -- 0xa0ffff	DSPLINK I/O strobe (data bits d16–d31 only)
0xc00000 -- 0xc0ffff	DSPLINK MEM strobe (data bits d16–d31 only)

Table 5.2: IEA-MIMO memory map

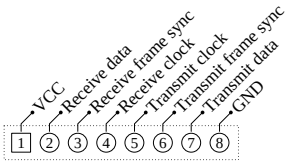

Figure 5.2: Pinout for TMS320C30 serial port connectors P7 and P8

those signals are only used to start A/D conversions (see figure 5.6 on page 78), but the board logic may be reprogrammed, e.g to interface to an incremental encoder using the internal timer/counter for pulse counting.

The two built-in serial ports are synchronous bidirectional ports, mainly intended for interfacing to A/D-converters and other TMS320C30 processors. The ports are currently not used for anything, but it is certainly possible to build a multiprocessing system using those ports for communication. The signals are available at connectors P7 and P8. The pinout of the connectors is shown in figure 5.2

5.2.2 Memory

Requirements

The on-board memory should only fulfill two requirements; There should be enough, and it should be as fast as possible. The latter called for static RAM.

Internal memory

The TMS320C30 has 2 kWords (2048 x 32 bits) of built-in memory. This memory can be accessed two times each clock-cycle, due to the multiple internal buses. The internal memory is small, but placing critical code and/or data in internal memory can considerably increase performance of an application.

External memory

Apart from memory built into the CPU, IEA-MIMO has two blocks of external memory. One block of 128 kWords static RAM, and another block of up to 256 kWords ROM.

The RAM memory block consists of four 1 Mbit static memory circuits in 128k x 8 organization. The designation varies between manufacturers, but the Integrated Device Technology ($\int dt$) designation is 71024-S20TY. The pin configuration of these types is compatible with 256 kbit memories, which also can be used.

The access time of the chosen memory circuits is less than 20 ns which enables the CPU to perform one read each instruction cycle. Due to the bus protocol, however, the CPU cannot write more often than than every other clock cycle, regardless of memory speed.

The ROM memory block consists of two 4 Mbit EPROM circuits, in 16-bit organisation (256k x 16). Also in this case, the circuit layout allows for smaller memories, with some exceptions. For EPROM memories there is a standard designation, 27Cxxx. Types that can be used are 27C1024, 27C2048 and 27C4096. Because of limited board space, memories in PLCC package is used. This further limits the alternatives, in particular regarding erasable memories. The only erasable memory in this package that is known to work is the HN27C4096ACC from Hitachi Semiconductors Inc. Due to the programming logic, the smaller HN27C1024ACC cannot be used without modifying the circuit board. If reprogramming is not necessary, OTP[4] memories from AMD works correctly in all sizes.

The ROM memory circuits must have less than 120 ns access time. An external wait state generator generates two wait states for ROM accesses, which means that the CPU can perform one read every third clock cycle.

5.2.3 Expansion bus

Since it was decided not to include application specific I/O on the IEA-MIMO board, there had to be means of expanding the capabilities of the control computer. This is accomplished by including a simple 16-bit bus interface for I/O boards.

Instead of inventing a bus, an existing bus interface was used, the DSPLINK bus. DSPLINK is a simple 16-bit bus defined by Loughborough Sound Images (LSI) Inc. for its line of signal processing boards.

The DSPLINK expansion bus is essentially a buffered version of a part of the CPU bus. The used parts are CPU data bits d16–d31 and CPU address bits a0–a15. The IOE and GME strobes are generated by

[4]One-Time Programmable – A designation for UV-erasable EPROM memories mounted in a package without quartz window, thus impossible to erase.

the on-board control logic. The external wait state generator controls the timing on the expansion bus.

5.2.4 System integration

In order to make the hardware as flexible as possible, programmable logic has been used for all control logic and state machines. The speed demand for the main bus required the use of fast PAL devices (5 ns propagation delay) for the main bus chip select and timing logic. The DSPLINK bus control is implemented in the same devices. All other logic is implemented in a single MACH435 device. This gives IEA-MIMO a large flexibility concerning the I/O functionality, since the device can be reprogrammed for new applications. The MACH435 device is a fairly large device, which has ample room for new functionality.

5.2.5 Power Supply circuits

IEA-MIMO uses a +5 Volts power supply for its digital circuitry, and a ±15 Volts power supply for analog circuits. IEA-MIMO consumes 1.1 A from the +5 Volt supply and about 200 mA from the ±15 Volts supply.

Many of the circuits chosen for the analog input cannot use the standard ±15 Volts power supply. For instance, the chosen sample/hold amplifiers requires a ±12 Volt supply. For the supply fo those components, linear voltage regulators have been used to reduce the voltage to ±12 Volts and ±5 Volts.

5.2.6 Analog input

The analog input consists of an input filter section, sixteen S/H amplifiers (one for each channel), a multiplexer followed by a buffer, and an A/D converter. The converted values are written into a FIFO-memory for later retrieval by the CPU. See figure 5.3 on the next page.

Signal path

The input filter is a first-order RC-filter. Apart from reducing high-frequency noise, the input filter reduces the input voltage from the nominal ±10 Volts to ±5 Volts. This reduction is needed because the S/H amplifiers cannot handle the full input range. The capacitor also reduces the high-frequency output impedance. The S/H amplifiers need

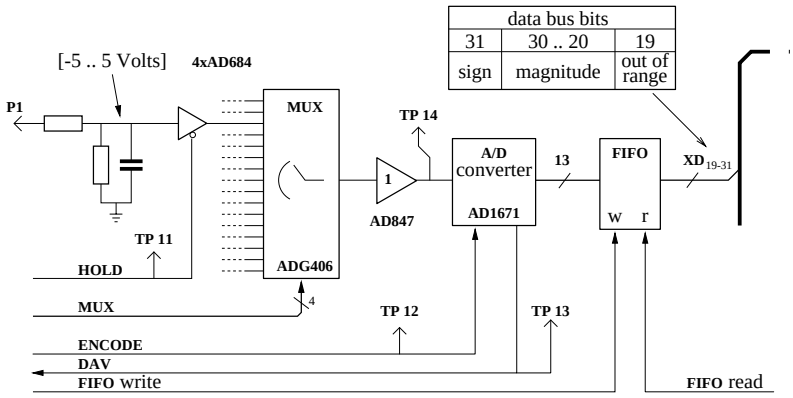

Figure 5.3: Analog input signal path of IEA-MIMO

a low-impedance source. Otherwise the charge-injection from the switch will introduce an offset in hold mode.

The S/H amplifiers are of the type AD684 from Analog Devices. This is one of very few quadruple S/H amplifiers available. The outputs of the S/H amplifiers are connected to an analog MUX with 16 channels. The performance of the MUX is crucial for the precision. It has to switch from one channel to the next in less than 900 ns, while keeping a 12-bit accuracy. The used multiplexer, ADG406, has a transition time of less than 250 ns over its entire temperature range.

The transition time is the time to reach 90% of the full transition between two channels, from the time of the address change. If we assume an internal delay of 50 ns, the RC time constant is 200ns/2.2 $\approx$ 90ns. This means the relative error will be $e^{-900\text{ns}\cdot 2.2/200\text{ns}} \approx 5 \cdot 10^{-5}$, well below the requirement, $2.5 \cdot 10^{-4}$

The multiplexer is followed by a buffer amplifier, in order to reduce the influence from the on-resistance. The buffer amplifier, AD847, is chosen for its speed and well-behaved transient response.

The A/D converter is the AD1671 from Analog devices. This converter performs one conversion in 0.8 μs, and has 12 bits resolution. The S/H built into AD1671 is used to improve the conversion speed. The MUX address is changed just after the conversion is started. This way, the whole conversion time of the A/D converter is used for the mux transition. Since the MUX requires about 0.9 μs to switch between

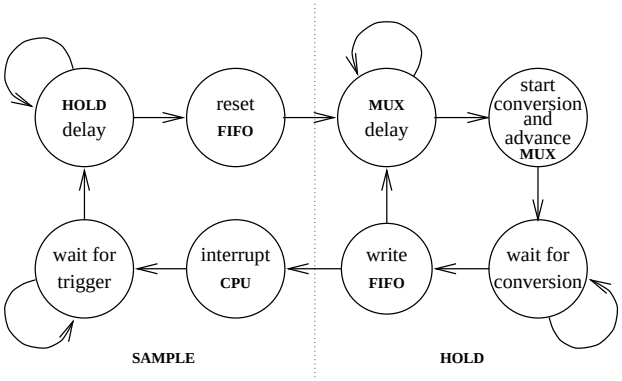

Figure 5.4: State machine controlling A/D-conversion on IEA-MIMO

channels, the A/D converter can operate at almost full speed.

The output from the A/D converter is connected to a FIFO buffer. The data is written to this buffer, an can later be read by the CPU.

Conversion sequence

The conversion sequence is controlled by a state machine. This state machine is implemented entirely in programmable logic, and can therefore be modified for new applications. The machine is divided into three smaller machines, to make the implementation more comprehensible. The main state machine takes care of the conversion sequence. The state diagram of the main machine is shown in figure 5.4.

The main state machine is supported by a channel counter, a delay timer and an asynchronous state machine that synchronizes the main machine to the A/D converter (see figure 5.5 on the next page).

See figure 5.5 on the following page for the state diagram of the asynchronous machine.

Programming

The operation of the A/D converter is controlled by a control register on the IEA-MIMO, see figure 5.6 on the next page. A conversion can be initiated by several sources, selected by the three least significant bits of the AD-MODE register. A conversion can also be initiated by a write to the AD-FIFO address.

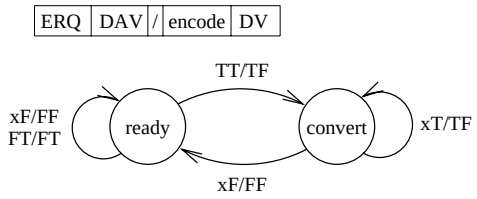

Figure 5.5: Asynchronous adapter machine for the A/D-converter

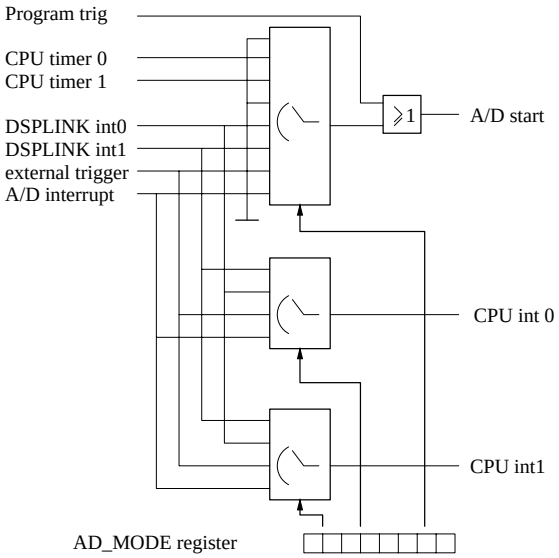

Figure 5.6: A/D trigger and CPU interrupt logic

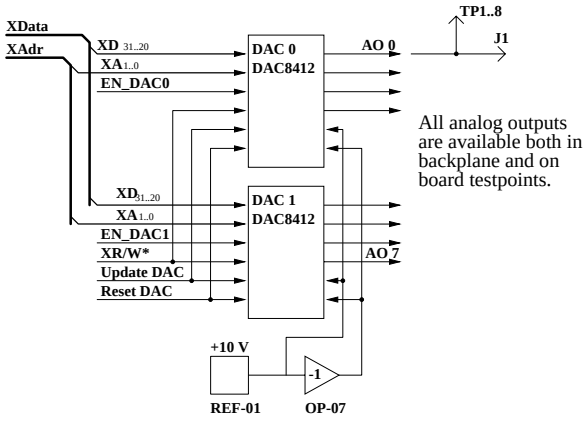

Figure 5.7: IEA-MIMO analog output circuit

When the conversion sequence has ended, the AD-FIFO contains the converted values in channel order. The AD-MODE register should be setup so that the CPU is interrupted when the conversion is done. There is no status register that can be read to find out when the conversion sequence has ended.

5.2.7 Analog output

The analog output is implemented with two DAC8412 circuits, which are quadruple D/A converters with 12-bits resolution, see figure 5.7. The converters use external references. The reference generator is a REF-01 voltage reference, which generates the positive reference, together with an operational amplifier that generates a tracking negative reference.

Programming

Table 5.3 on the next page shows the registers, and their format, of the D/A converter. The D/A converters use unsigned format. Writing a zero value yields -10 Volts output. To get zero output voltage, a value of `0x80000000` should be used.

The D/A converters are double-buffered. Writing the D/A registers does not affect the output directly; a write to the D/A-update address is needed for the change to take effect. The contents of the registers

Address	reg	CPU expansion bus data bits											
		XD31	XD30	XD29	XD28	XD27	XD26	XD25	XD24	XD23	XD22	XD21	XD20
0x804000	ch0	MSB ⟵ channel 0 output (read/write) ⟶ LSB											
0x804001	ch1	MSB ⟵ channel 1 output (read/write) ⟶ LSB											
0x804002	ch2	MSB ⟵ channel 2 output (read/write) ⟶ LSB											
0x804003	ch3	MSB ⟵ channel 3 output (read/write) ⟶ LSB											
0x804004	ch4	MSB ⟵ channel 4 output (read/write) ⟶ LSB											
0x804006	ch5	MSB ⟵ channel 5 output (read/write) ⟶ LSB											
0x804006	ch6	MSB ⟵ channel 6 output (read/write) ⟶ LSB											
0x804007	ch7	MSB ⟵ channel 7 output (read/write) ⟶ LSB											
0x80400C	load	a write updates all outputs, all data bits are ignored											

Table 5.3: IEA-MIMO D/A converter register map

can be read back for reference, but the value may not reflect the output voltage.

There is no way to reset all converters to mid-scale by software, other than writing the above mentioned value for zero output to all channels. However, all channels are reset to zero output voltage when IEA-MIMO is powered up and when IEA-MIMO receives a hardware reset.

5.2.8 Digital inputs and outputs

Apart from the analog I/O, IEA-MIMO has a number of logic-level inputs and outputs. There are nine (9) signals available in the backplane connector. In addition, there are six signals available for "user I/O". The current programming of the board logic controls three pushbuttons and three LED indicators. Other variants can also be, and have been, developed.

Backplane signals

The logic signals available in the backplane are nine TTL-level signals, with on-board 22 kΩ pull-up resistors. Eight of the signals can be individually configured as both inputs and outputs. The last signal is an input that can be used for triggering A/D conversion or an interrupt. See figure 5.8 on the facing page for connection information.

The digital I/O in the backplane is controlled from two registers; one data register, and one output-enable register.

	d	b	z	
32	Ain 0	Ain 1	Ain 2	
30	Ain 3	Ain 4	Ain 5	
28	Ain 6	Ain 7	Ain 8	
26	Ain 9	Ain 10	Ain 11	
24	Ain 12	Ain 13	Ain 14	
22	Ain 15	AGND	AGND	
20	-15 Volt	-15 Volt	-15 Volt	
18	GND	GND	GND	
16	+5 Volt	+5 Volt	+5 Volt	
14	+15 Volt	+15 Volt	+15 Volt	
12	Aout 0	Aout 1	Aout 2	
10	Aout 3	Aout 4	Aout 5	
8	Aout 6	Aout 7	NC	
6	D i/o 6	D i/o 3	D i/o 0	
4	D i/o 7	D i/o 4	D i/o 1	
2	D trig	D i/o 5	D i/o 2	

Figure 5.8: IEA-MIMO backplane connector `P1`

The data register contains one data bit for each signal, a total of 8 bits. Writing the data bits sets the desired output value on all signals at once. The state of the output enable register determines if a write actually has effect.

The output enable register contains one bit for each data bit. Setting an output enable bit to "one" configures the corresponding pin as an output. When configured as an output, the data register drives the pin. When reading the data register, the value is the actual signal levels, not the value written. This means the contents of the data register cannot be read, unless the pins are configured as outputs.

All output enable bits are reset to zero on reset.

The trigger signal is an active-low signal. When the signal is pulled low, it can trigger an A/D conversion or interrupt the CPU. The function depends on the AD-MODE register. See figure 5.6 on page 78.

On-board signals

The "internal" digital I/O is intended for front panel elements. The current version of the board logic handles three pushbuttons and three LED indicators. The front panel elements should be connected to connector `P4`, see figure 5.9 on the following page for pin configuration.

The signals are controlled by one write-only register controlling the LED indicators, and one read-only register that contains the button positions. The board logic interrupts the CPU (`int3`) when any of the buttons changes state.

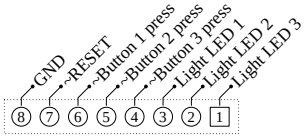

Figure 5.9: IEA-MIMO on-board (internal) i/o connector P4

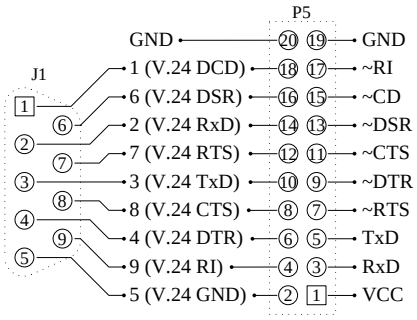

Figure 5.10: IEA-MIMO communication port interface connectors P5 and J1

5.2.9 The serial port

To be able to communicate with other computers, the IEA-MIMO control computer has a TL16C750 UART. The chosen UART is fully compatible with the standard 16C550 which is used in IBM-PC-compatible computers. The TL16C750, however, has 64-byte receive and transmit buffers while the 16C550 has 16-byte buffers.

Circuit details

The electrical interface is situated on a small daughter card, which can implement for instance RS232 electrical levels. The daughter card is connected through a 20-pin DIN41651 connector. The external connector is a standard 9-pin d-sub connector. See figure 5.10 for pin configurations.

Programming

The 16C750 UART has 12 (twelve) registers, which are listed in table 5.4 on the facing page. The registers have the following functions:

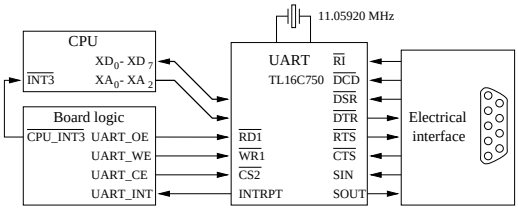

Figure 5.11: IEA-MIMO communication port circuit diagram

Address	reg	CPU expansion bus data bits									
		access	XD31..XD08	XD07	XD06	XD05	XD04	XD03	XD02	XD01	XD00
0x804070	THR	W		MSB			transmit data				LSB
	RBR	R	random garbage when read	MSB			receive data				LSB
	DLL	R/W	random garbage when read	frequency divider low byte (when DLAB=1)							LSB
0x804071	IER	R/W	random garbage when read			LOWP	SLEEP	EDSSI	ELSI	ETEBEI	ERBI
	DLM	R/W	random garbage when read	MSB frequency divider high byte (when DLAB=1)							
0x804072	FCR	W		RTM	RTL	EN64		EDMA	TXFR	RCFR	EFIFO
	ISR	R	random garbage when read	FIFOE	FIFOE	64BE		IID3	IID2	IID1	NOINT
0x804073	LCR	R/W	random garbage when read	DLAB	BREAK	Stick parity	EVEN parity	PEN	STB	WLS1	WLS0
0x804074	MCR	R/W	random garbage when read			AFE	loopback mode	OUT2	OUT1	RTS	DTR
0x804075	LSR	R	random garbage when read	QERR	TEMT	THRE	BRKI	FERR	PERR	OERR	DRDY
0x804076	MSR	R	random garbage when read	~DCD	~RI	~DSR	~CTS	dDCD	TERI	dDSR	dCTS
0x804077	SPR	R/W	random garbage when read								

Table 5.4: 16C750 UART registers on IEA-MIMO

RBR Receiver buffer register; Contains the next character received, if any.

THR Transmitter hold register; Data written to this register will be sent. When FIFOs are enabled, 16 or 64 bytes can be written without waiting for the transmitter.

IER Interrupt enable register; Determines which events should cause an interrupt (data received, nothing to transmit, line status change and modem status change).

FCR FIFO control register; controls mode and operation of the receiver and transmitter FIFOs.

DLL and DLM Divisor latch. The baud rate is determined by the crystal frequency and the contents of those two registers, according to:

$$\text{baudrate}[s^{-1}] = \frac{\text{crystalfrequency}[Hz]}{16 \times < \text{DLMDLL} >}$$

The divisor latch can only be accessed if the DLAB bit in LCR is set.

ISR Interrupt status register. The UART generates only one interrupt. This register contains detailed information on the interrupt cause.

LCR Line control register; the bits in this register controls parity generation, word length and access to the divisor latch.

MCR Modem control register; this register controls the modem handshake signals, DTR, RTS, OUT1, OUT2.

LSR Line status register; this register reports parity, overrun, and framing errors associated with the byte currently in RHR.

MSR Modem status register; this register reports status and status changes of the modem handshake signals.

SCR Scratch pad register; has no special function but can be used for intermediate data storage.

The programming principles of the TL16C750 is detailed in the manufacturers data sheet and will not be repeated here.

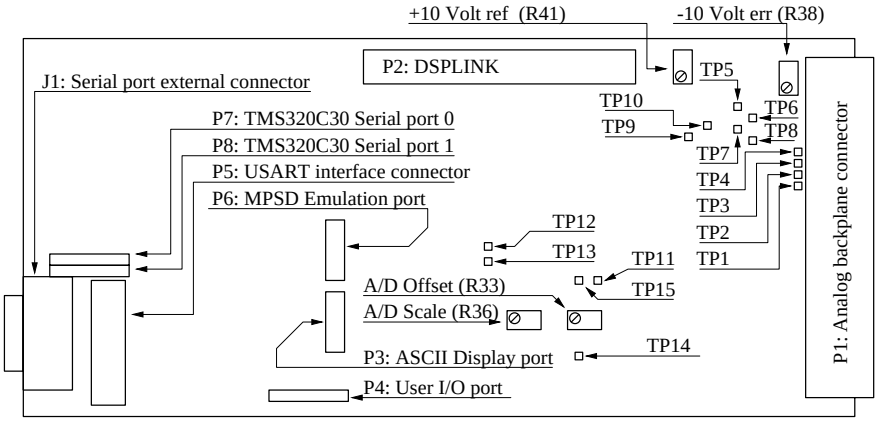

Figure 5.12: IEA-MIMO connectors, test points and trim points

The crystal frequency of the UART is $11.0592MHz$. This enables baudrates up to 230.4 kBaud (using a divisor latch value of 3). The TL16C750 is capable of up to 16 MHz crystal frequency, yielding a 1 Mbaud maximum speed. However, most standard baudrates can be factorized in $2^i \times 3^j \times 5^k$, where $i \geq 0$, $3 \geq j \geq 0$ and $3 \geq k \geq 1$. The chosen crystal frequency has the factorization $2^{14} \times 3^3 \times 5^3$, which consequently is divisible with almost all standard baudrates. If higher baudrates are desired, a $14.7456 \cdot 10^6[\text{Hz}] = 2^{16} \times 3^2 \times 5^3[\text{Hz}]$ crystal can be used.

5.3 Physical implementation

IEA-MIMO is constructed on a 100x220mm circuit board (long eurocard). Figure 5.13 on the next page shows the placemant of main components. Figure 5.12 shows placement and naming of all connectors, test points and trim points of the board.

The "backplane" connector `P1` is a male DIN41617 form F connector with 48 pins. The signal configuration of the connector can be seen in figure 5.8 on page 81.

The DSPLINK bus is accessible through connector P2. This connector is a male DIN41651 IDC header for flat cable connectors. The bus is a

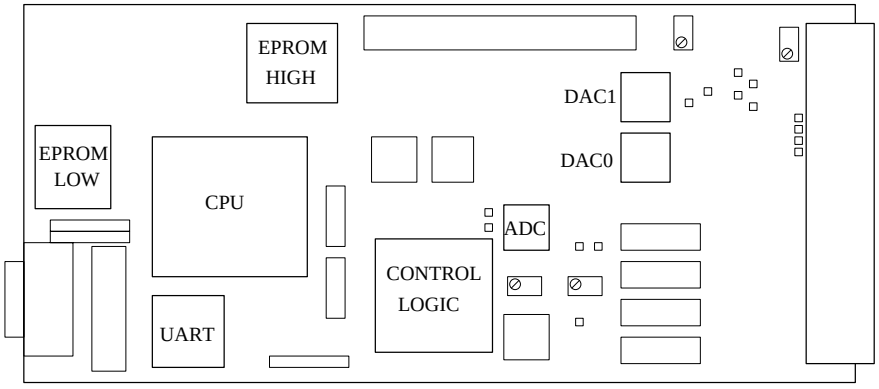

Figure 5.13: IEA-MIMO main components

little clumsy, since the flat cable must be connected after the card is mounted in the rack.

5.4 Future versions

The IEA-MIMO computer is becoming a successful product, despite its shortcomings. However, within five years, there should be a replacement for it, with considerably higher processor performance. In preparation for the development of the next control computer, the author has collected some ideas that would be nice to implement.

The IEA-MIMO has some shortcomings, notably:

- Number crunching capacity is too low, and there is no upgrade path for the CPU.
- Non-volatile memory consists only of EPROM memories.
- The RAM memory is limited and built with expensive static memories.
- IEA-MIMO lacks a real-time clock.
- The DSPLINK-bus is a little bit too clumsy for inter-board communication in the current rack-mount system.

- The programmable logic cannot be reprogrammed without using a device programmer. Modern logic can be reprogrammed in place.
- There are four trim points in the analog circuitry. There should be ways to automatically calibrate the analog circuitry.
- The analog inputs has too low input impedance.
- There should be more than one channel for communication with a host computer or within a system.
- The grounding system is less than perfect.

The reasons for those shortcomings are mainly lack of board space and lack of experience. The current board is quite full of components. Modern microprocessors have even larger buses (moving up to 64 bits) and sometimes also larger footprints. Dispensing with the DSPLINK bus will save a lot of board space that can be used for new or better features, but this space may very well be consumed by the board space requirements for a modern microprocessor.

Some ideas for a new board are:

- Use a general processor, preferably a low-power variant intended for "laptop" computers. PowerPC is a good alternative.
- Use standard SIMM or DIMM sockets for the main memory. This will save board space and open up a wide selection of memory sizes.
- The chosen processor should be able to execute programs stored in 8-bit wide memory. This would save a lot of board space since only one circuit would be needed for non-volatile memory.
- Non-volatile memory should use a combination of FLASH memory and battery-backed static RAM (with built in real-time clock).
- The analog inputs should use DMA to transfer data directly to system memory instead of using FIFO:s
- Some analog comparators with outputs connected to programmable logic would extend the usability.
- Automatic calibration of analog outputs and inputs can be implemented with "programmable resistors", analog switches, and a precision reference. Ideally, there should be no trimmers.

- Programmable logic that controls functionality not vital for CPU operation should be reconfigurable by software. This can be done by using RAM-based programmable logic.
- Vast amounts of programmable logic will increase flexibility.
- Use serial communication instead of the somewhat clumsy DSPLINK bus. IEEE-1394 is a serial bus intended for high-speed peripherals which is likely to become standard on personal computers. It can transfer up to 400 Mbits/s on a six-wire interface (DSPLINK: 160 Mbit/s).
- It would be great to have Ethernet on-board, though this is not so important.

Finally, a system related suggestion: Modify the backplane. There should be only one supply voltage in the backplane, with separate converters in each module. There should also be a clear separation between power supply ground and signal ground.

Using a single power supply (e.g 24 Volts DC) would have the following advantages:

- Free up nine pins in the backplane connector (assuming a separate signal ground).
- The module designer can chose the best set of supply voltages for his module.
- The main power supply will be simpler.
- Less noise and interference.

The drawback is increased module complexity, increased board space, and higher unit cost. A simple analog module would need a converter to produce +/- 15 Volts for the operational amplifiers. However, a complex module like IEA-MIMO already needs extra converters.

Chapter 6

A six-phase pulse-width modulator

This chapter is about the six-phase pulse-width modulator. This modulator is intended for the commutation of two three-phase bridge converters, but can easily be modified for other purposes.

6.1 Functional description

The pulse width modulator, IEA-PWM6 is a six-channel digital pulse-width modulator. The six channels all share a common reference frequency, and are consequently fully synchronous. IEA-PWM6 is controlled via the DSPLINK bus. In addition to the six PWM-channels IEA-PWM6 can generate an interrupt, synchronised with the PWM outputs, on the DSPLINK bus.

6.1.1 Modulation principle

The modulation method is triangle-wave carrier modulation. This method is used since it gives less current (or torque) ripple compared to other modulation methods, for a given switching frequency. Another good property of triangle-wave carrier modulation is that currents in a controlled converter cross their average when the carrier reaches its endpoints. By synchronizing controller samples with the carrier, the current averages can be measured without the use of moving-average filters.

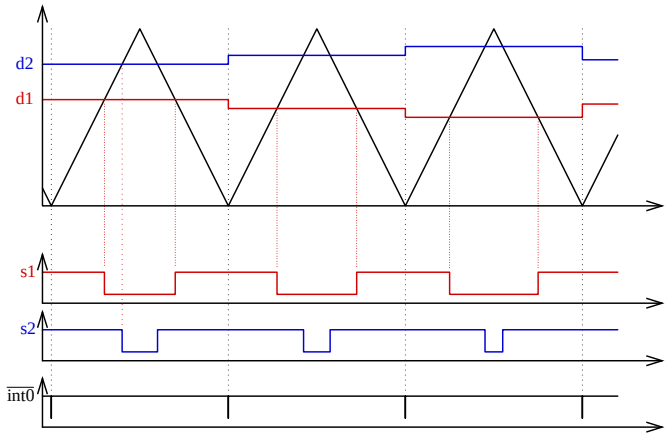

Figure 6.1: Example on pulse-width modulation with a triangle-wave carrier

Figure 6.1 illustrates the modulation method. The pulses are centred with respect to each other. In addition, the interrupt/update signal $\bar{int}0$ is centred and synchronised with the carrier wave.

6.1.2 Functional blocks

Figure 6.2 on the facing page gives an overview of the main functional units of the IEA-PWM6 modulator. The board consists of a carrier generator with an interrupt generator, six digital comparators with double-buffered compare registers, an address decoder that controls read and write access to the internal registers, and finally alarm and watchdog circuitry.

One channel of the modulator consists of an input register, an output register, a comparator, the enable circuit, and an output driver. Of these parts, only the output driver is implemented in fixed electronics. The rest is implemented in programmable logic. Figure 6.3 on the next page shows a block diagram for a channel. The blocks inside the dotted line are implemented in programmable logic.

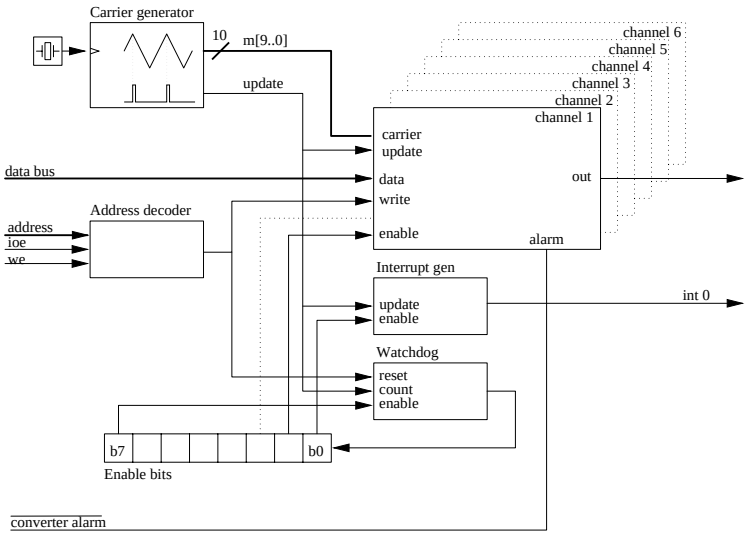

Figure 6.2: Block diagram for the complete IEA-PWM6 modulator board

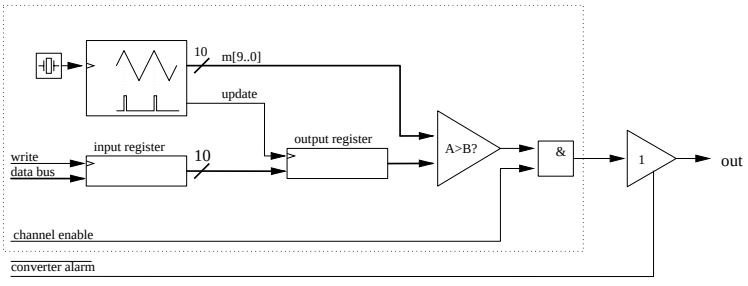

Figure 6.3: Block diagram for one channel of the IEA-PWM6 modulator

Safety measures

Power converters normally include overcurrent and overvoltage protection. IEA-PWM6 handles this via an enable input, that can be connected to an alarm signal of a controlled converter. The enable signal controls all PWM channels. When the enable input is shorted to ground, all channels are shut off.

When using microprocessors for real-time control, there is a concern for the reliability of the programming, and the microprocessor (especially in a research environment). This is handled by a "watchdog" which shuts off all PWM channels if the processor misses two subsequent updates.

Power supply

The IEA-PWM6 modulator uses a +5 Volt power supply for the logic circuitry. If output voltages other than 0/+5 Volts are needed, optional positive and negative power supplies can be used (see below). With the carrier frequency set to 6 kHz, the power consumption is about 2.5 Watts (0.5 Ampere).

Output voltage

The output voltage of the IEA-PWM6 modulator can be selected with jumpers JP1 through JP4. Valid jumper settings are listed in table 6.1. See also figure 6.4 on page 94 for the position of the jumper block.

	Bipolar: -15 Volts and +15 Volts
	Bipolar: +5 Volts and -15 Volts
	Unipolar: 0 Volts and +15 Volts
	Unipolar: 0 Volts and +5Volts

Table 6.1: IEA-PWM6 output voltage jumper settings

6.1.3 Programming

Register set

The IEA-PWM6 modulator board is controlled via the DSPLINK interface. The registers are listed in table 6.2 on the facing page. The registers are either write-only or read-only registers, i.e a register that can be written to cannot be read from and vice versa.

Address	Register	Data bits									
		b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
base+0	enable			watch-dog	ch6	ch5	ch4	ch3	ch2	ch1	inter-rupt
base+1	ch1	MSB ⟵ channel 1 duty cycle ⟶ LSB									
base+2	ch2	MSB ⟵ channel 2 duty cycle ⟶ LSB									
base+3	ch3	MSB ⟵ channel 3 duty cycle ⟶ LSB									
base+4	ch4	MSB ⟵ channel 4 duty cycle ⟶ LSB									
base+5	ch5	MSB ⟵ channel 5 duty cycle ⟶ LSB									
base+6	ch6	MSB ⟵ channel 6 duty cycle ⟶ LSB									
base+7	status									wtchdg tripped	cnvrtr alarm

Table 6.2: IEA-PWM6 register set

The function of the registers are as follows

enable (write-only) The enable register holds enable bits for all functional blocks. If one (1) is written to a bit; the corresponding function is switched on. If the watchdog is enabled, bits 0 through 7 are reset to zero when the watchdog trips.

ch1–ch6 (write-only) Output PWM duty-cycle registers for each channel. A write takes effect from the beginning of the next carrier period. The duty-cycle resolution is 10 bits; a value of decimal 512, or hexadecimal 0x200, gives a 50% duty cycle. When the watchdog is active, at least one of these registers must be written at least every other carrier period, otherwise the watchdog will trip. When the watchdog trips, the duty cycle registers are reset to zero.

status (read-only) The status register holds the alarm status bits. If a bit is set, the corresponding alarm has been activated.

Addressing

The IEA-PWM6 modulator uses the DSPLINK I/O-area. Of the 16 address bits, the three least significant bits are used for register selection, and address bits 8 thru 11 for I/O space selection.

SW 1 setting	base address
	DSPLINK IOE + 0x000
	DSPLINK IOE + 0x400
	DSPLINK IOE + 0xF00

Table 6.3: IEA-PWM6 base address settings

The base address of the register set is the base address of the DSPLINK I/O area plus N*0x100 where N is determined by the DIP-switch situated in the lower left corner of the IEA-PWM6 board (see figure 6.4 on the next page). Table 6.3 on the following page lists a few example settings and the corresponding base address. Note the orientation of the DIP-switch.

6.2 Hardware and Firmware

The modulator hardware is built on a 100x220mm circuit board. The circuit board has two layers with through-plated holes. The placement of components most important for users of the board is depicted in figure 6.4.

The "backplane" connector is a 48-pole DIN 41612 form F male connector. The connections available in the backplane are depicted in figure 6.5 on the facing page.

The DSPLINK bus is connected through a supplementary 50-pole DIN 41651 IDC header. The bus is directly connected to the two MACH435 devices. The DSPLINK interface is handled entirely in devices U5 and U8 without any additional logic.

The carrier generator, registers, comparators and logic is implemented in programmable logic consisting of two AMD MACH435 CPLD devices, U5 and U8. These devices consist of eight "PAL33V16" blocks with a common switch matrix. A PAL block consists of a logic input matrix with 33 inputs and 90 product term outputs, a logic allocator, sixteen flip-flop macrocells which can accept up to twelve product terms,

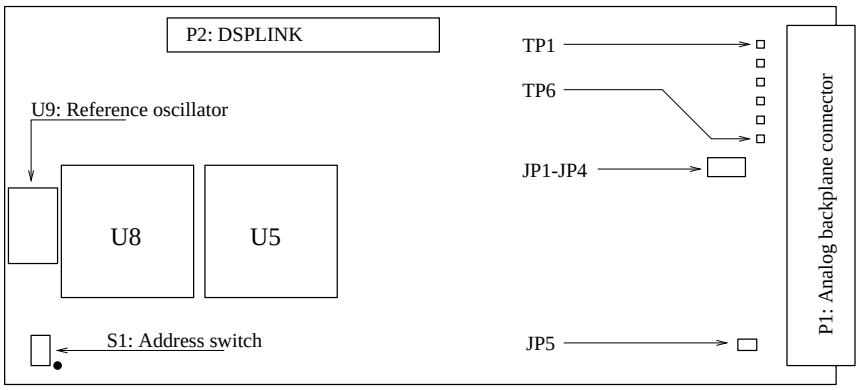

Figure 6.4: Placement of main components on IEA-PWM6

	2	4	6	8	10	12	14	16	18	20	22	24	26	28	30	32
d	out1	out2	out3	out4	out5	out6	+15 Volt	+5 Volt	GND	-15 Volt					GND	alarm
b	out1	out2	out3	out4	out5	out6	+15 Volt	+5 Volt	GND	-15 Volt					GND	alarm
z	out1	out2	out3	out4	out5	out6	+15 Volt	+5 Volt	GND	-15 Volt					GND	alarm

Figure 6.5: IEA-PWM6 backplane connector

and eight output pins. The macrocell outputs and the pin signals are all fed back into the central switch matrix.

The programming of U5 and U8 is described in section 6.2.1 on the next page.

The MACH435 devices generate two separate pulse-trains for each channel; one signal for the upper half of a controlled bridge leg and one for the lower half. The pulse-width modulated outputs are connected to a pair of NAND gates, which are used for blocking the modulation on a converter alarm. The output goes into a high-impedance state when the modulation is shut off through the gates [by a converter alarm].

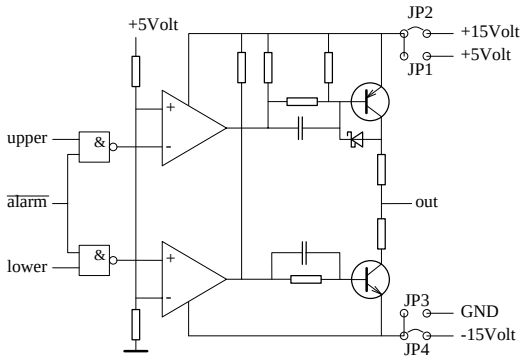

Figure 6.6: IEA-PWM6 output stage

The outputs from the NAND gates are connected to the inputs of a pair of comparators, which drive a push-pull output stage capable of driving 150 mA into the converter input. See figure 6.6 on the following page for detailed schematics on the output stage. The output stage can be configured for different output voltage levels, using jumpers JP1 through JP4.

6.2.1 Firmware

The two MACH435 devices were programmed with a programming tool from AMD, MACHXL2. This tool is fairly outdated today, but still usable. The input to the programming tool is a "program" consisting of a device description, a pinout description, and a logic description. An optional simulation/testing program can also be included.

The pinout can be "floating" during firmware development. This makes it easier to "fit" the construction into a given device. Further analysis of the compilation results can give good hints on how to select the final pinout. A short example on the pinout declaration for one of the circuits is shown in listing 6.2.1

```
PIN     17..19,24       adr[3..0]       ; Register selector
PIN     25..31,33..35   data[9..0]      ; 10-bit input
PIN     20              /ce

; Input registers (for double buffering)
NODE    ?               ain[9..0]       LATCHED
NODE    ?               oe[7,3..0]      LATCHED

; Compare registers, updates on each carrier turn
NODE    ?               a[9..0]         LATCHED

; Carrier generator
PIN     37..40,45..50   m[0..9]         REGISTERED
PIN     62              pwm_clk
PIN     65              update

; Output comparators. The outputs are registered to avoid race
; conditions which would otherwise cause glitches in the output
NODE    ?               pa[9..1]
NODE    ?               out[3..1]
PIN     56,68,77        pout[3..1]      REGISTERED
PIN     59,71,80        nout[3..1]      REGISTERED
```

Listing 6.1: Excerpt of the pin declaration for device u5 in IEA-PWM6

A NODE is an internal signal declaration while a PIN is an external signal. signals can be declared REGISTERED which means they are updated by a clock signal, see for instance the declaration of `a[9..0]`.

The carrier generator is implemented with "T" flip-flops. An example on the code (but for a 4-bit generator) is listing 6.2. This implementation works well, and allows a maximum input frequency (`pwm_clk` in the figure) of over 60 MHz, well above the need for this application.

The comparators are the most demanding logic in the modulators. An example on a four-bit comparator is shown in listing 6.3. The comparator is implemented with a macro cell depth of two. The first level

```
up.clkf = pwm_clk
up = up */(m[3] * m[2] * m[1] */m[0]) +
          /m[3] */m[2] */m[1] * m[0]

m[3..0].clkf = pwm_clk
m[0].T =  VCC
m[1].T =  /up */m[0] +
           up * m[0]
m[2].T =  /up */m[1] */m[0] +
           up * m[1] * m[0]
m[3].T =  /up */m[2] */m[1] */m[0] +
           up * m[2] * m[1] * m[0]
```

Listing 6.2: 4-bit triangle wave generator code example

```
pa[3..1] = a[3..1] :*: m[3..1]
out[1] = oe[1]*a[0]*/m[0]*pa[1]*pa[2]*pa[3] +
         oe[1]*a[1]*/m[1]*pa[2]*pa[3] +
         oe[1]*a[2]*/m[2]*pa[3] +
         oe[1]*a[3]*/m[3]
```

Listing 6.3: 4-bit comparator code example

is XNOR gates, xnor is denoted `:*:` in the code, calculating a "compare result propagator". The second level calculates the compare result ($a > m$) for each bit and uses the previously calculated propagator to decide which bit will give the final compare result.

```
pout.clkf = pwm_clk
nout.clkf = pwm_clk

pout = oe[1]*{ out[1]}
nout = oe[1]*{/out[1]}
```

Listing 6.4: IEA-PWM6 modulator output code

Listing 6.4 shows the code for one output. The modulator generates two outputs for each channel. When enabled, the outputs are the inverse of each other. When disabled, both outputs are zeroed. This makes the output stage go into a high impedance state.

The outputs are registered to avoid race conditions in the comparator that cause the compare result to switch back and forth when many bits in the carrier generator switch at the same instant. Since the comparators are two macrocells deep, the clock frequency must be lower than the maximum counter frequency.

6.3 Conclusion

6.3.1 Performance

In general, the modulator has excellent performance. Clock frequencies up to 40.00 MHz (corresponding to the carrier frequency 19.52 kHz) has been used without problems. The 10-bit resolution is more than sufficient for most applications, which makes it excellent as a research tool. The only drawback with the modulator is perhaps the inherent delays, which can break the accuracy of synchronised current measurements.

The delays in the modulator itself are illustrated in figure 6.7 on the page before. The total delay from comparator output to modulator output is about 0.35 μs. In addition, the converter itself can add between 1 and 5 μs to the total delay. Finally, the current transducers can introduce delays up to 10 μs. The total delay can thus be as much as 15 μs. If the current is sampled the same instant the interrupt is

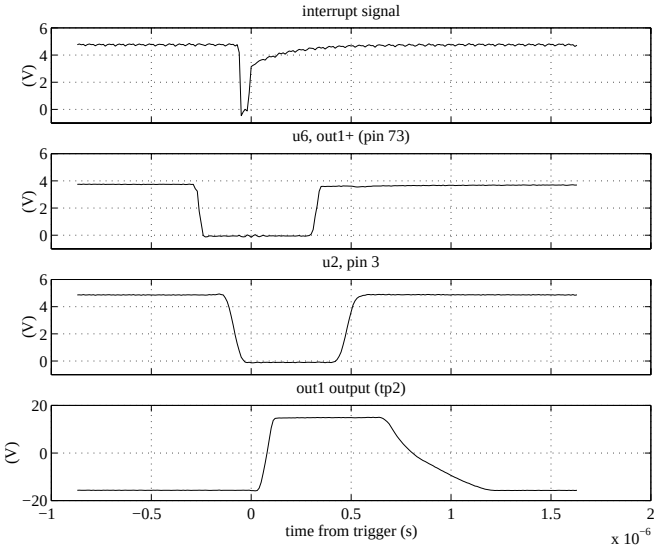

Figure 6.7: Signal delays in the IEA-PWM6 modulator

generated, the current measurement will be incorrect. There are three possible workarounds to this problem:

- A programmable delay on the interrupt.
- A programmable hardware delay on the A/D converter trig.
- A software delay for the the A/D converter trig.

It is the author's opinion that the best solution is a programmable delay in the A/D converter. Mostly because this is the most general solution, and because it does not cost any extra CPU time.

6.3.2 Reliability

The reliability of the MACH435 devices has been less then optimal. If proper precautions against electrostatic discharge are observed the reliability is ok concerning day-to-day handling, but the MACH435 devices are quite sensitive; since these devices are electrically programmable and erasable, small charges injected into them can cause fatal programming errors. The device must then be reprogrammed before it will work correctly again.

Another problem is that the bus is handled directly by the MACH435 devices. A long cable will cause ringings that may actually destroy the devices. A proper termination should have been included to reduce or eliminate ringing on the bus lines. In the current design, the cable length should not exceed 30cm for proper operation.

6.3.3 Future development

The design goal was to make a rather flexible modulator board, with high precision in the modulation. Unfortunately the flexibility is slightly impaired since the two MACH435s just barely have room for the full modulator program. To create e.g a random carrier modulator would either require larger devices, or a reduction in precision.

The current resolution is ten bits, which might be reduced to nine or even eight. This would leave room for a programmable carrier-frequency, but the reduction in resolution would probably lead to higher noise, in addition to the intentionally introduced noise. It remains to find out if an eight-bit resolution is enough.

The converter interface of the current design is a little bit too simple. The alarm interface in particular should have room for more signals,

to enable detailed monitoring of the converter through the modulator interface. Separating the firing pulses for the upper and lower converter branches would also be a good idea.

An idea for a really flexible board is a board with a programmable carrier generator, analog comparators fed by A/D-converters for the modulation, programmable blanking time compensation, and finally, reconfigurable for dead-band modulation instead of carrier modulation. This board would not require large cplds and would probably be more reliable.

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