The Emerging World of Massively Broadband Devices: 60 GHz and Above

Keynote Address: 2009 Wireless@VT

Prof. Theodore S. Rappaport

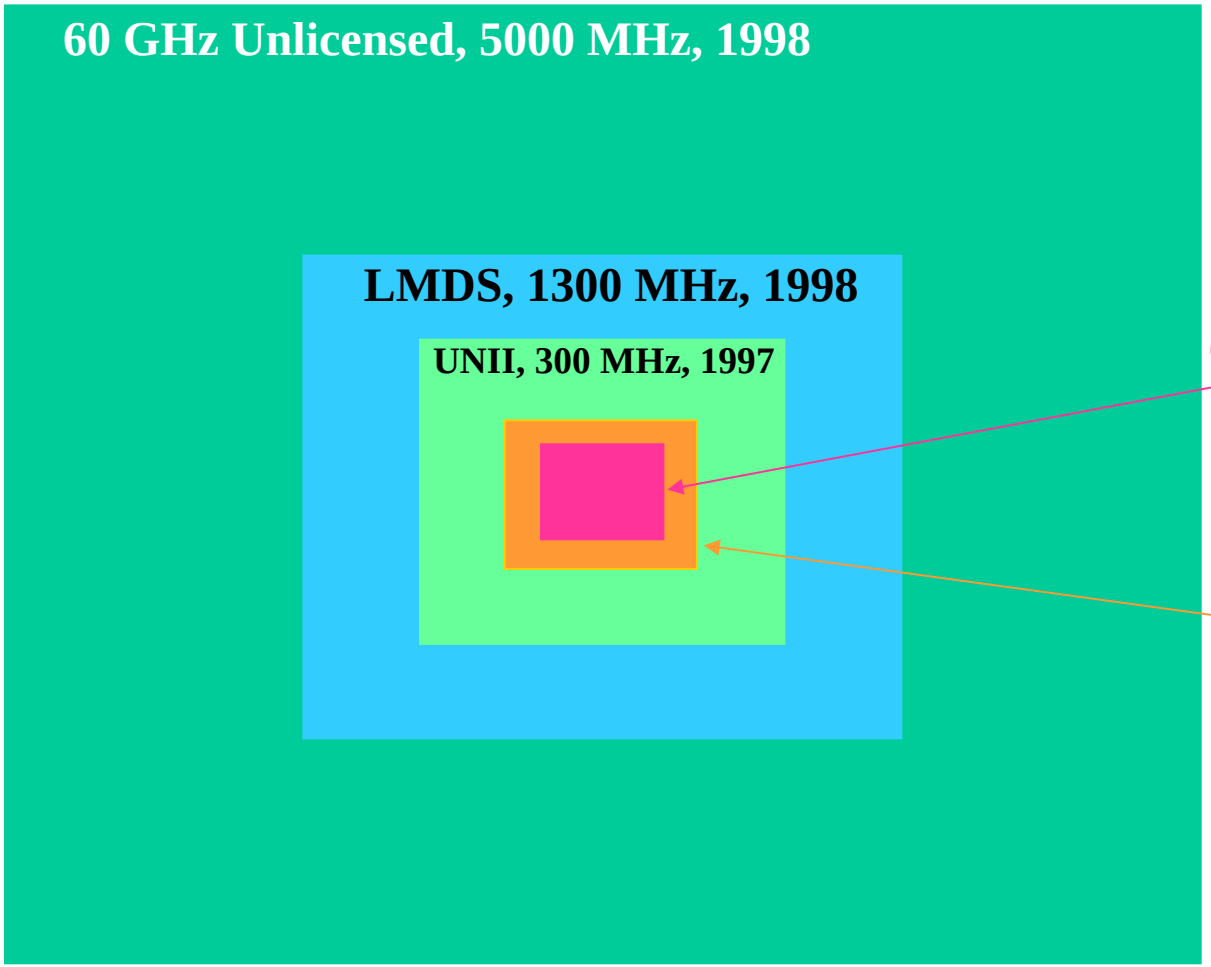
Felix Gutierrez

Wireless Networking and Communications Group (WNCG)

The University of Texas at Austin

Thursday, June 4, 2009

Recent U.S. Spectrum Allocations



- A voice channel occupies ~ 10 kHz of spectrum.
- A TV channel occupies ~ 5 MHz of spectrum.

60 GHz Global Opportunity

- **5 GHz** of unlicensed bandwidth around 60 GHz throughout the world
- Transistors capable of 60+ GHz with 130 nm CMOS technology and smaller

- CMOS Transistor state-of-the-art (ITRS):
  - 45 nm mass production in 2007-2009
  - 32 nm in 2009-2011
  - 22 nm in 2011-2013
  - 16 nm, 11 nm within the coming decade
- Free space wavelength @ 60 GHz: 5mm
- Wavelength shortened to 2.5 mm in standard integrated circuits (ICs) because of dielectric (silicon has epsilon of 3.9)

- Antenna size becomes on the order of the IC chip size
  - Antennas can be fabricated directly on-chip!

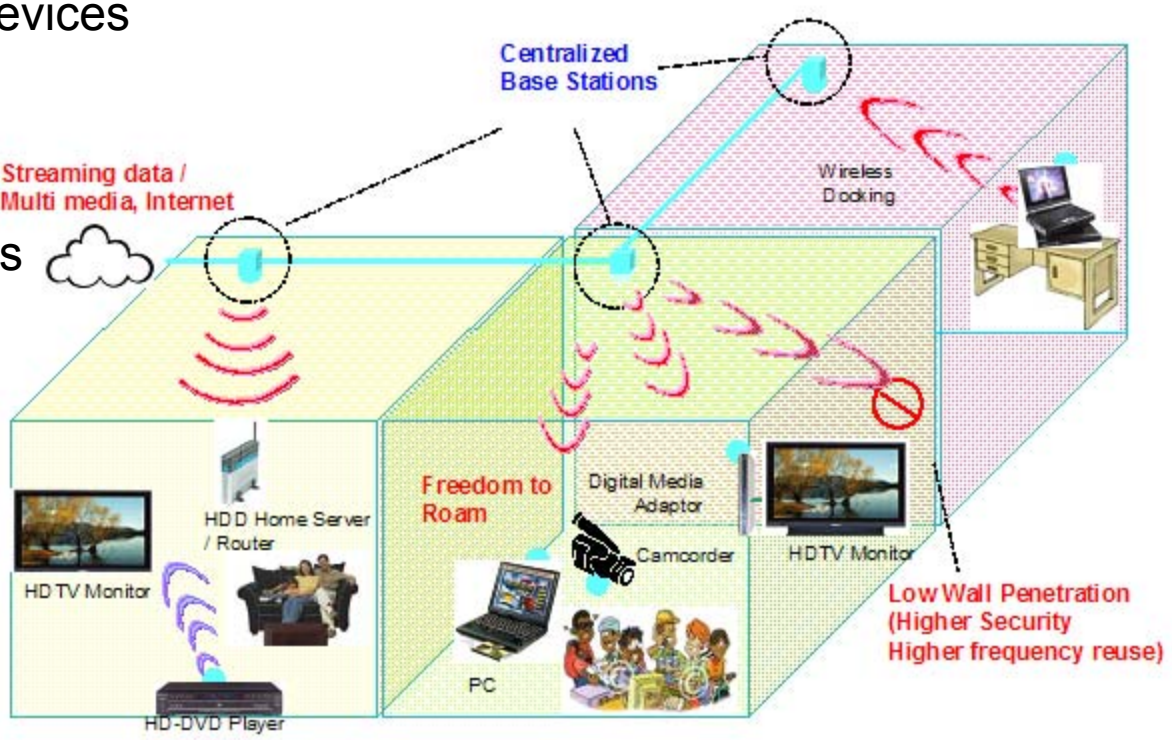
60 GHz Applications

- Personal Area Networks (PANs)
  - Cable Replacement (HDMI)
  - Media interconnectivity
  - Intra-vehicular networking
- Wireless Local Area Networks (LANs)
  - Multi-gigabit/s data transfer rates
  - Wire replacement for in-building networks
  - IEEE 802.11 VHT
- Fixed Wireless Access (FWA)
  - Line of Sight (LOS) between buildings
  - Similar to Free Space Optics (FSO)

Wireless Home Networking

Redefining Home Networks with mmWave

- Interconnectivity of media devices
- High data rates, fast transfers
- Streaming uncompressed High-Definition content



Credit by: IBM

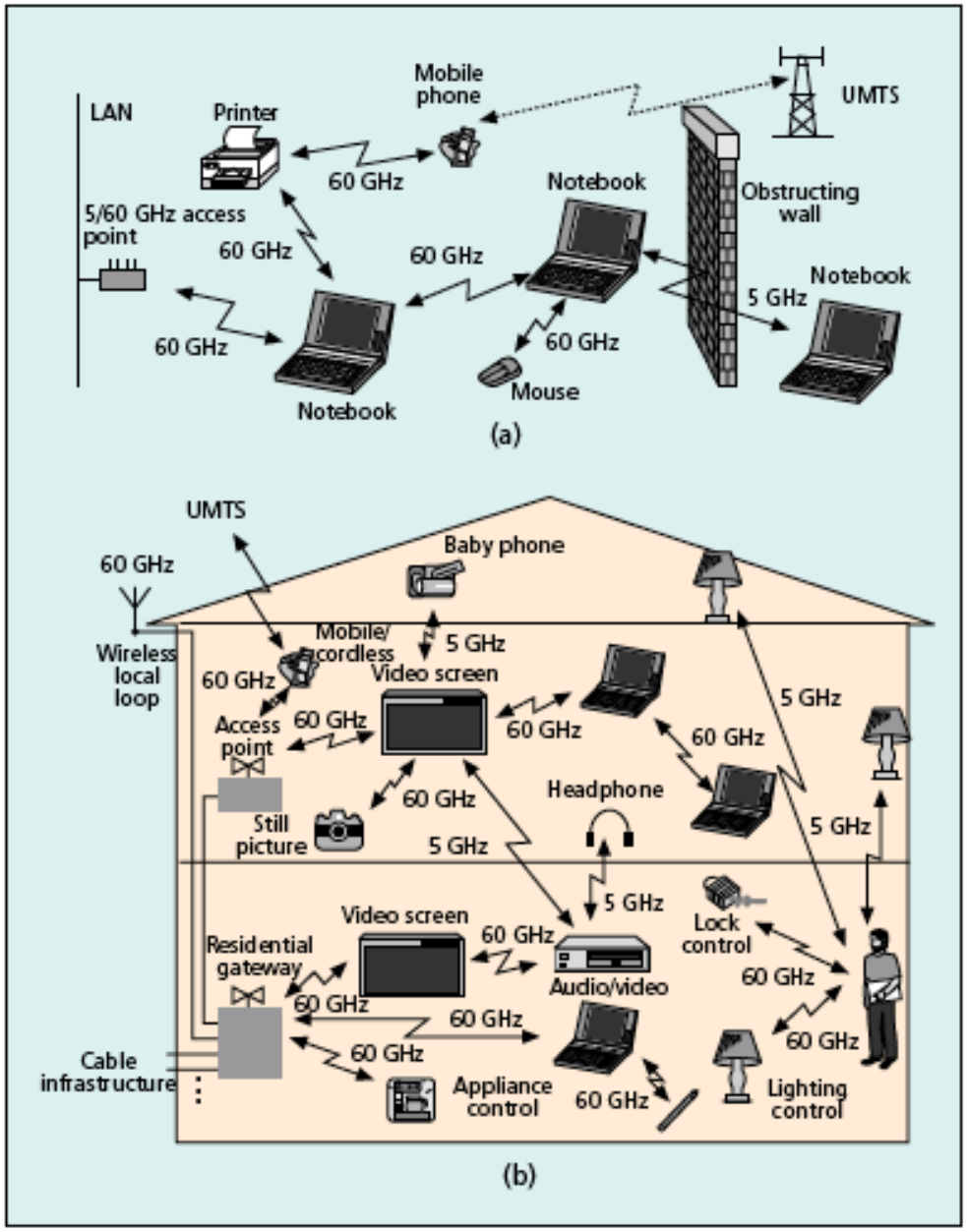


Figure 3. *a) 5/60 GHz system scenario in office environment; b) 5/60 GHz system scenario in home environment.*

P. Smulders, "Exploiting the 60 GHz band for local wireless multimedia access: prospects and future directions," Communications Magazine, IEEE, vol. 40, 2002, pp. 140-147.

- Transfer live HD television/video between set top boxes, PCs, terminals, HDMI

- High data rates allow uncompressed transfer
- No aggressive signal processing
- Less hardware, low cost, latency, consumer mkt.

Wireless Books and Media

Amazon Kindle 2
Credit : mobileread.com

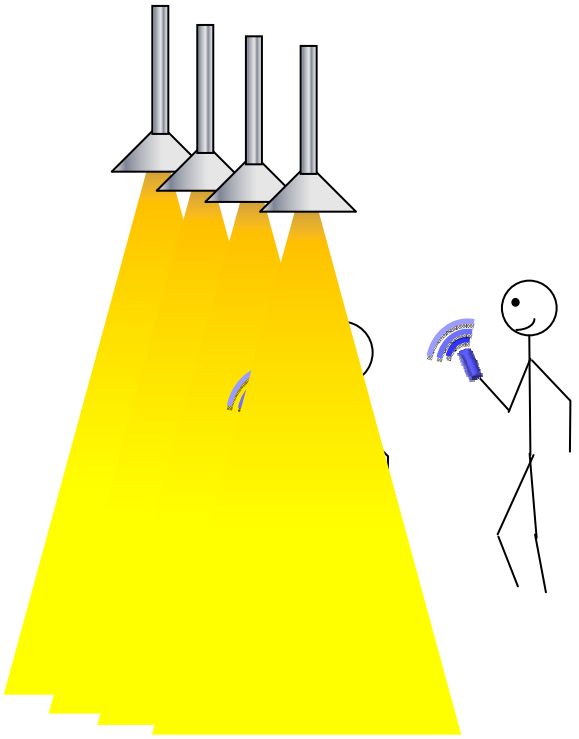
- Streaming libraries of data to personal devices
- Wireless Post-it note – RFID tags replace paper and magnetic media
- Eliminate the need to carry bulky textbooks or newspapers
- Greener solution with less paper/weight

Wireless Pills

iPill
Credit : Philips

- Real-time video capture to monitor digestive system, internal organs
- Applying medication to target specific areas with video assistance and remote control
- On-board biosensors to perform lab tests and provide fast results

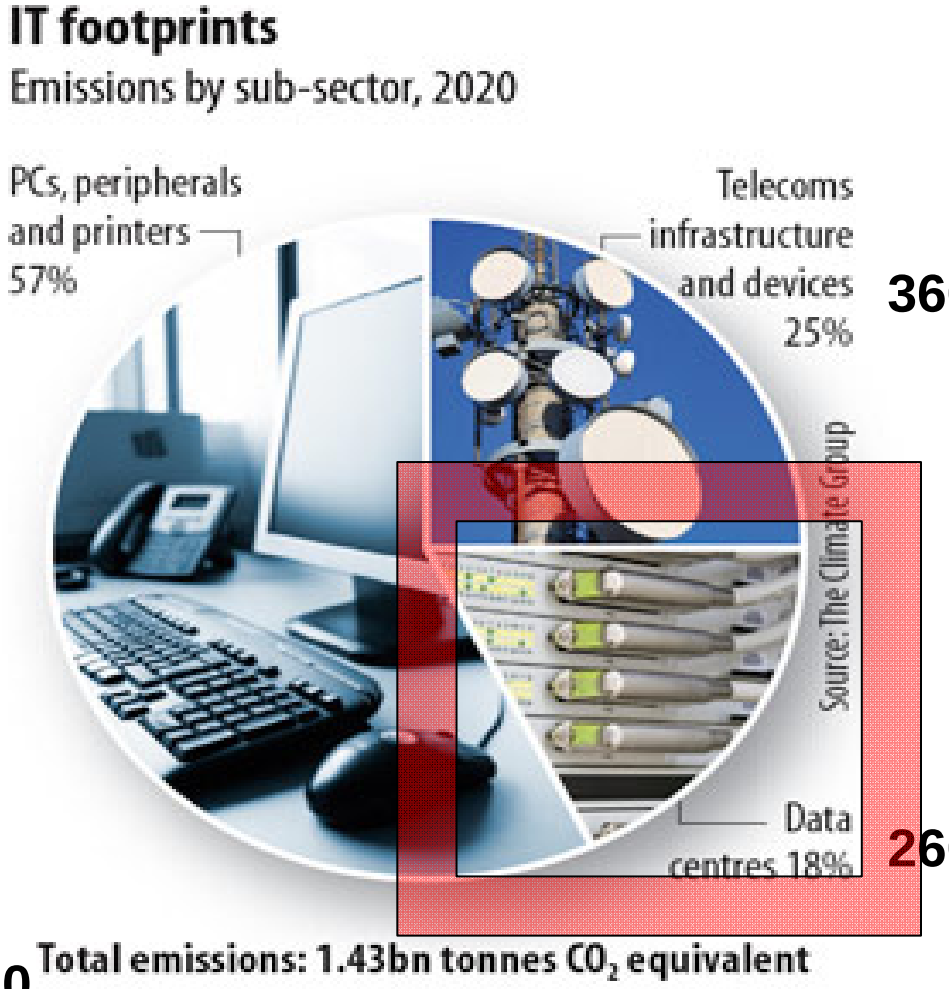
Information Shower



- "Showered" with information on forward and/or reverse link
- Access points will be mounted on ceilings, walls, doorways, vehicles
- Massive Gbps data transfers while moving through a small area

2020 IT Carbon Footprint

820m tons CO_2



360m tons CO_2

2007 Worldwide IT carbon footprint:

2% = 830 m tons CO_2
Comparable to the global aviation industry

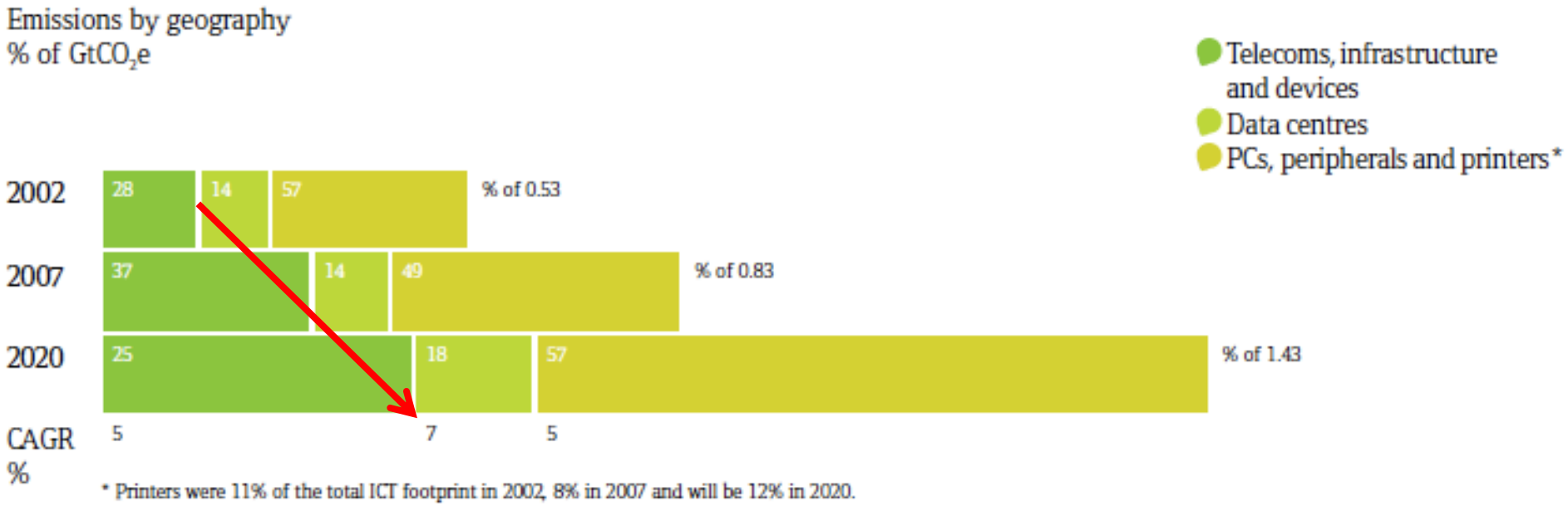
Expected to grow to 4% of world by 2020

260m tons CO_2

2020 IT Carbon Footprint

"SMART 2020: Enabling the Low Carbon Economy in the Information Age", The Climate Group

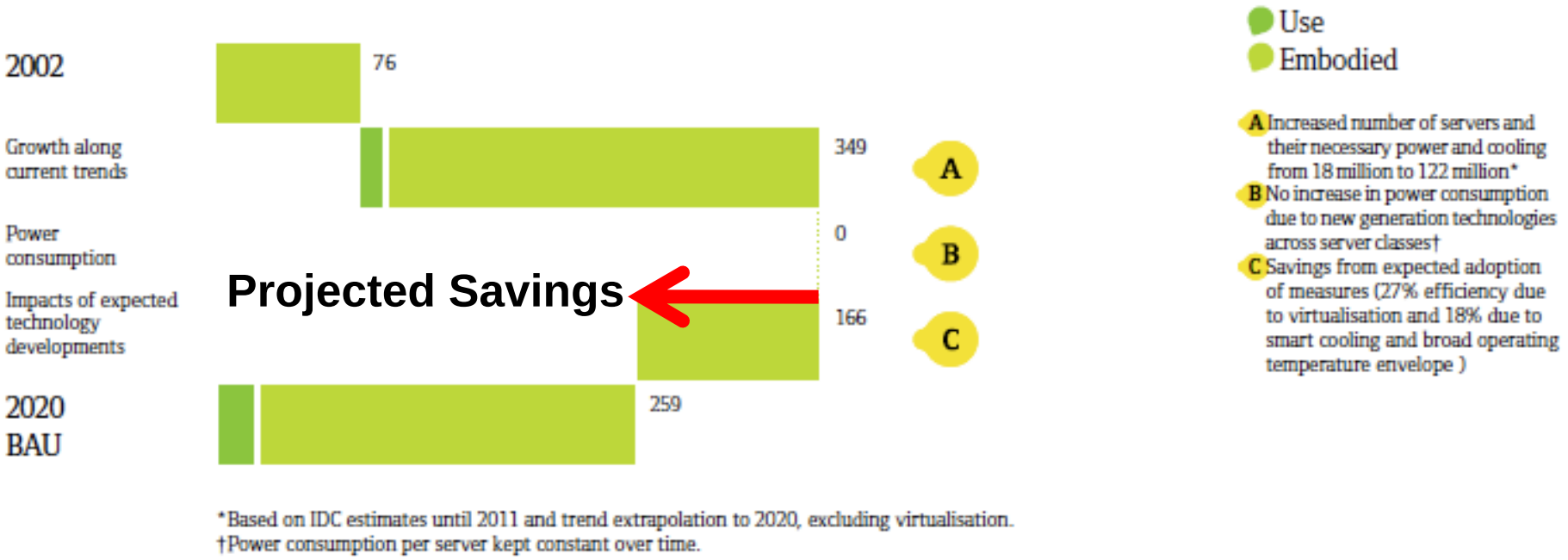
Fig. 2.3 The global footprint by subsector



2020 IT Carbon Footprint

"SMART 2020: Enabling the Low Carbon Economy in the Information Age", The Climate Group

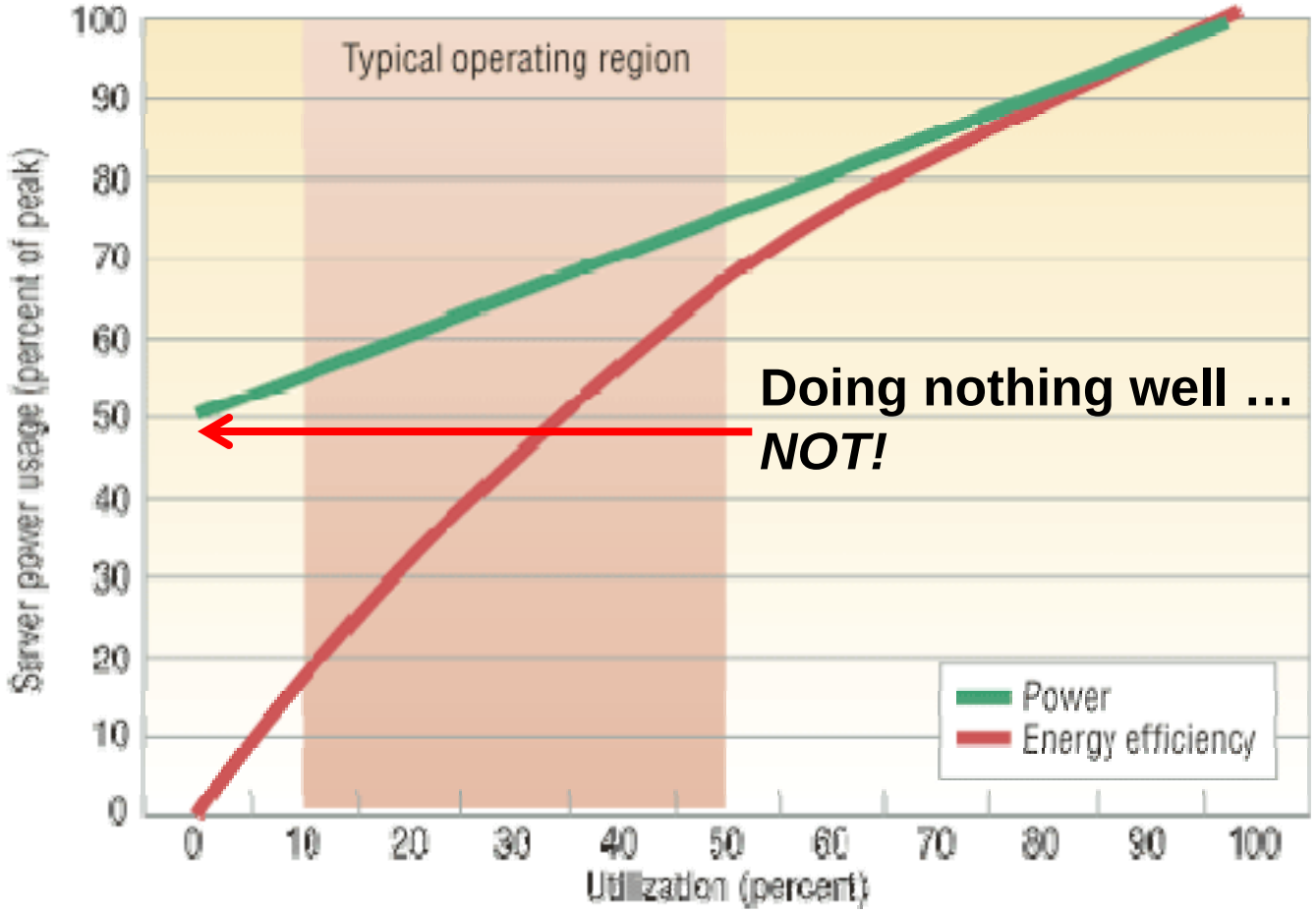
Fig. 4.1 The global data centre footprint



*Based on IDC estimates until 2011 and trend extrapolation to 2020, excluding virtualisation.
†Power consumption per server kept constant over time.

Energy Proportional Computing

"The Case for Energy-Proportional Computing,"
Luiz André Barroso,
Urs Hölzle,
IEEE Computer
December 2007

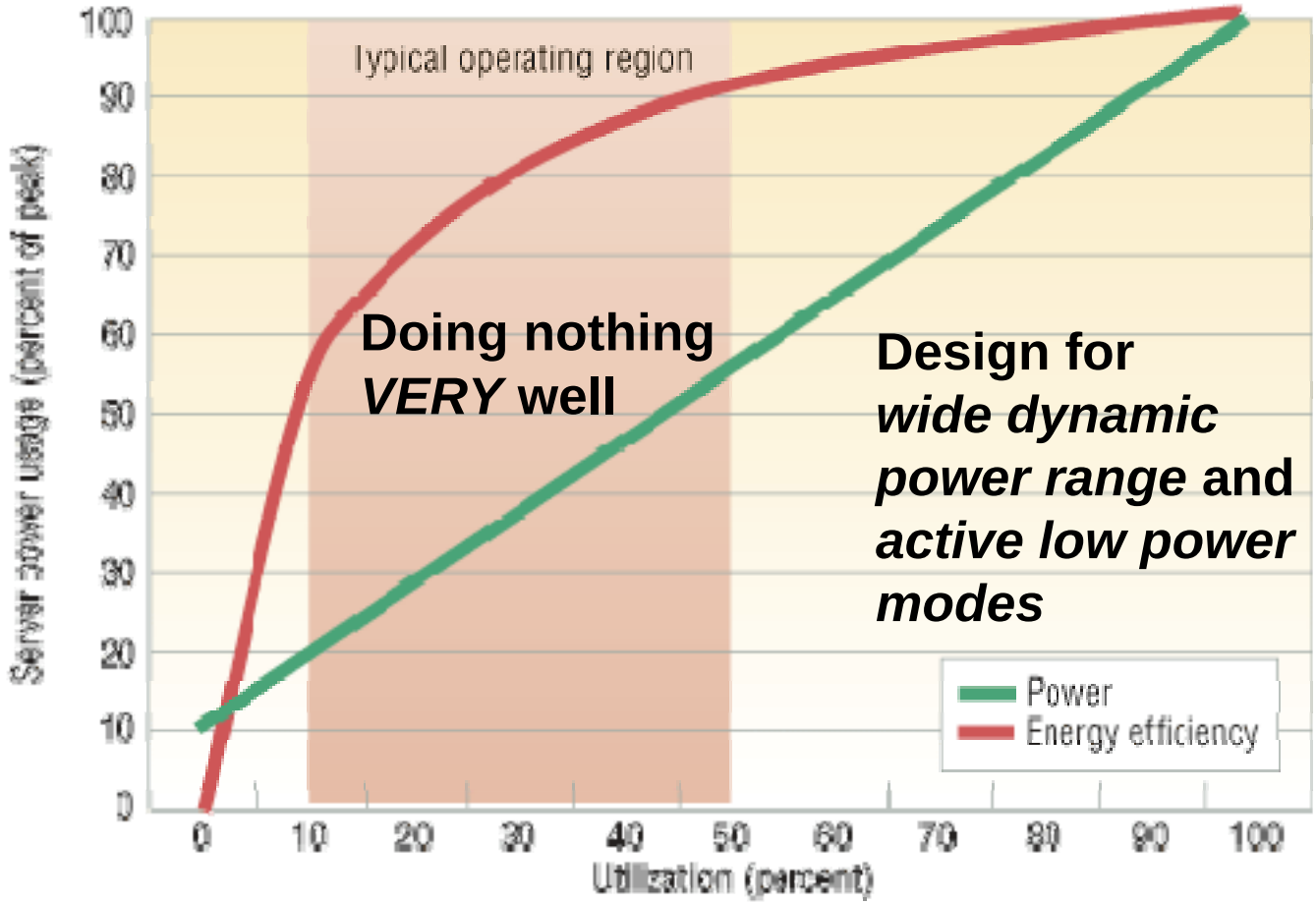


Energy Efficiency = Utilization/Power

Figure 2. Server power usage and energy efficiency at varying utilization levels, from idle to peak performance. Even an energy-efficient server still consumes about half its full power when doing virtually no work.

Energy Proportional Computing

"The Case for Energy-Proportional Computing,"
Luiz André Barroso, Urs Hölzle,
IEEE Computer
December 2007



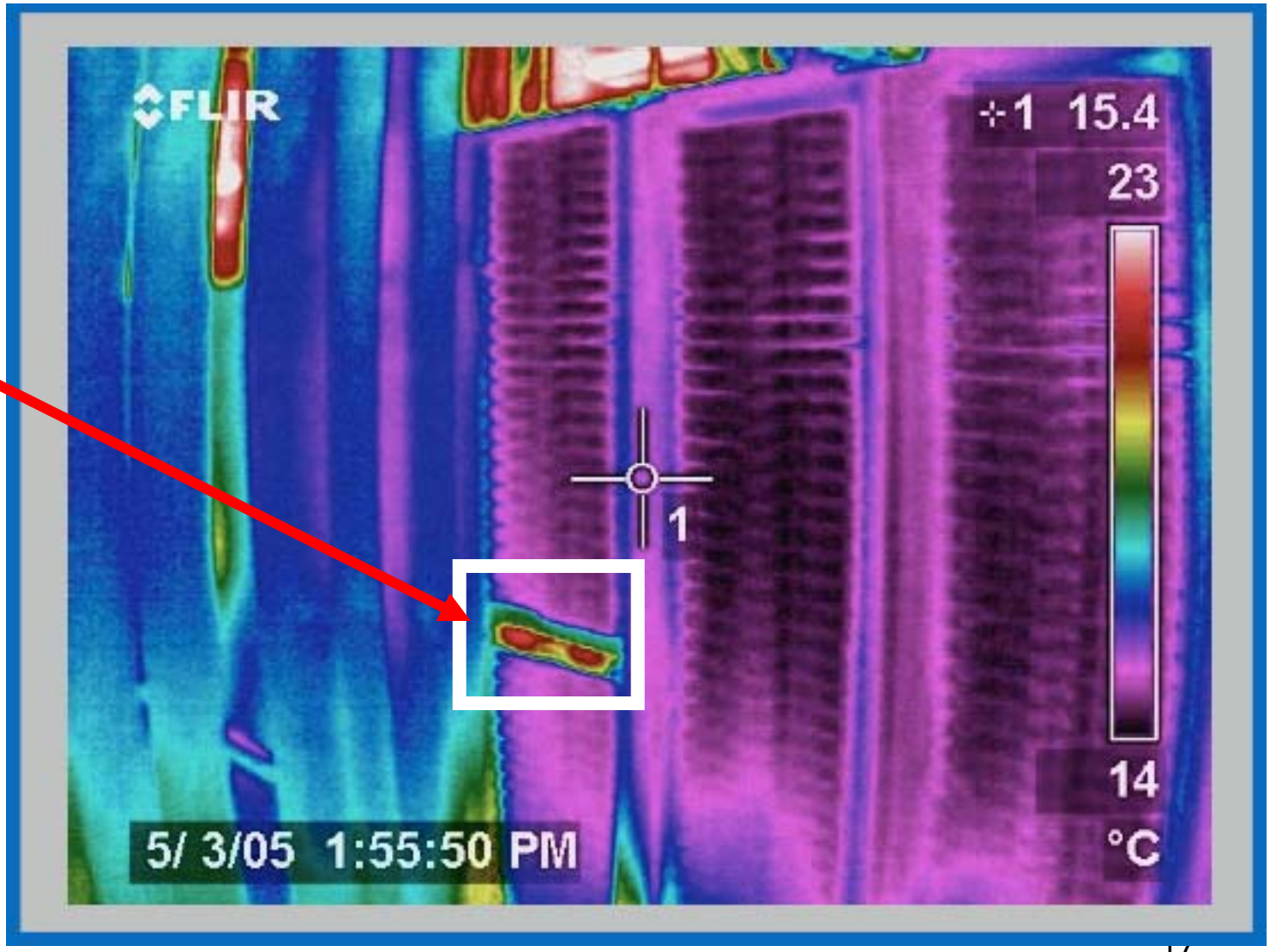
Energy Efficiency = Utilization/Power

Figure 4. Power usage and energy efficiency in a more energy-proportional server. This server has a power efficiency of more than 80 percent of its peak value for utilizations of 30 percent and above, with efficiency remaining above 50 percent for utilization levels as low as 10 percent.

Computers + Net + Storage + *Power + Cooling*

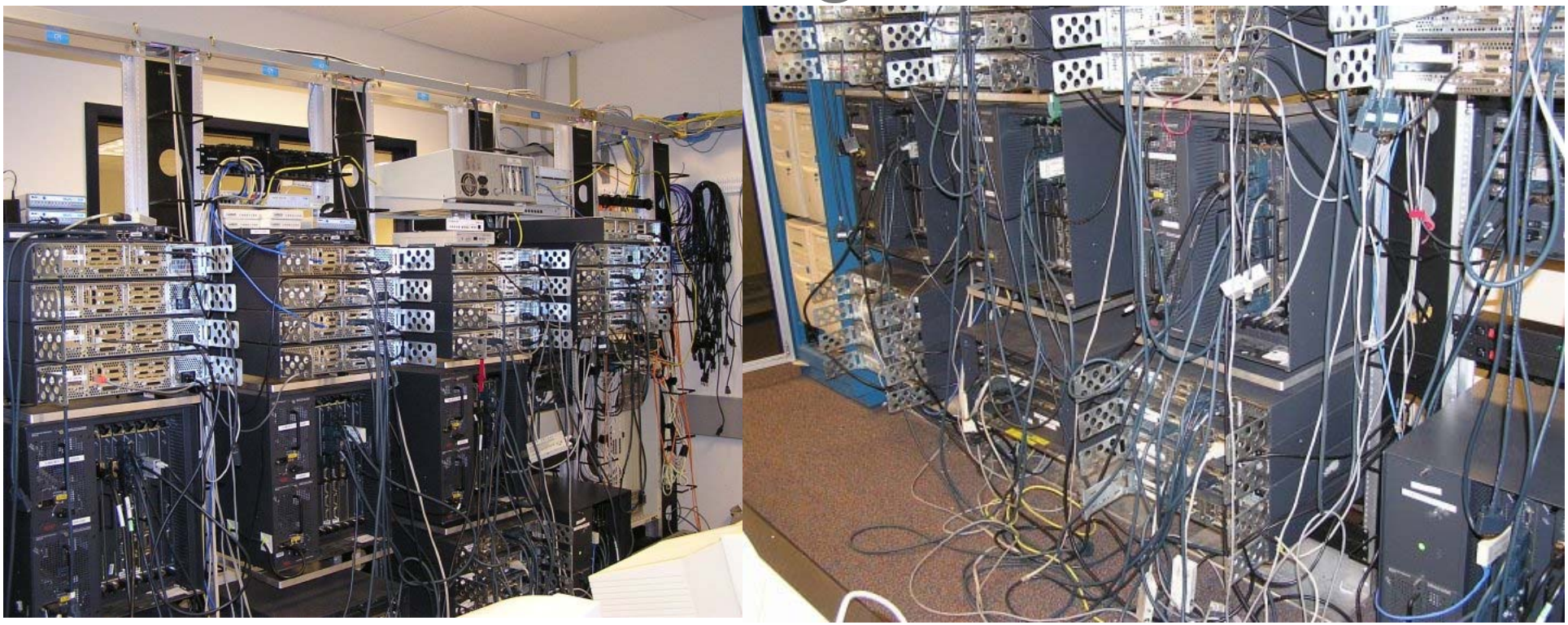
Thermal Image of typ.Cluster Rack

Rack Switch



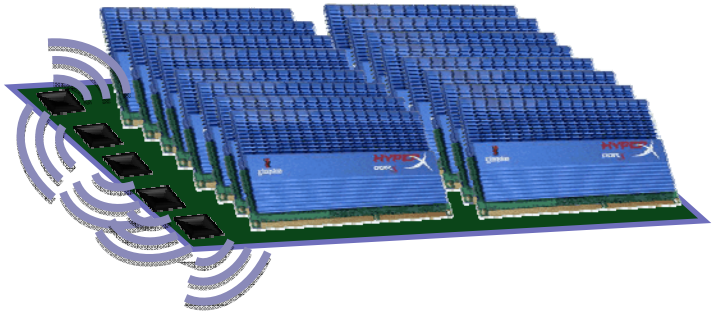
M. K. Patterson, A. Pratt, P. Kumar,
"From UPS to Silicon: an end-to-end evaluation of datacenter efficiency", Intel Corporation

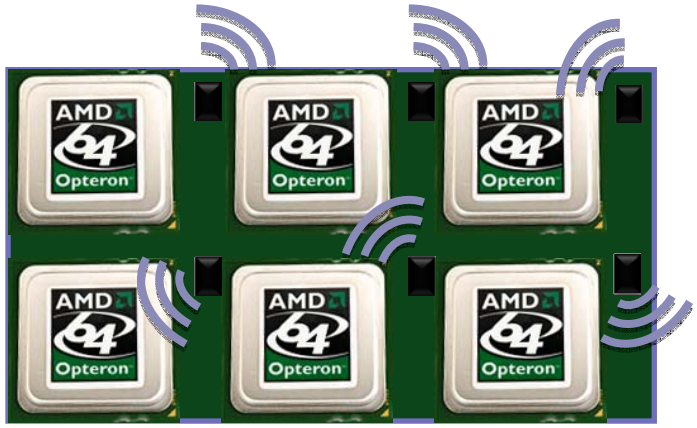
DC Networking and Power



- 96 x 1 Gbit port Cisco datacenter switch consumes around 15 kW -- approximately 100x a typical dual processor Google server @ 145 W
- High port density drives network element design, but such high power density makes it difficult to tightly pack them with servers
- Alternative distributed processing/communications topology under investigation by various research groups

Decentralized Computing





- Replace interconnects with wireless
- Applications in warehouse data centers, PCs, servers
- Cooling servers is paramount problem
- Decentralize and focus cooling on heat-intensive components
- Increase efficiency

Data Center Growth

- Explosion in growth of data centers this decade
- Future of **cloud computing** driving data center growth
- "colossal warehouses packed with tens of thousands of servers"[1]
- Largest contributors
  - Microsoft
  - Google
  - Yahoo
  - Amazon
- Microsoft Data Center
  - Quincy, Washington
  - 43K sq. meters ≅ 10 football fields
  - 48 MWatts consumed ≅ 40K homes

[1]Katz, R.H., "Tech Titans Building Boom," *Spectrum, IEEE* , vol.46, no.2, pp.40-54, Feb. 2009.

Data Centers

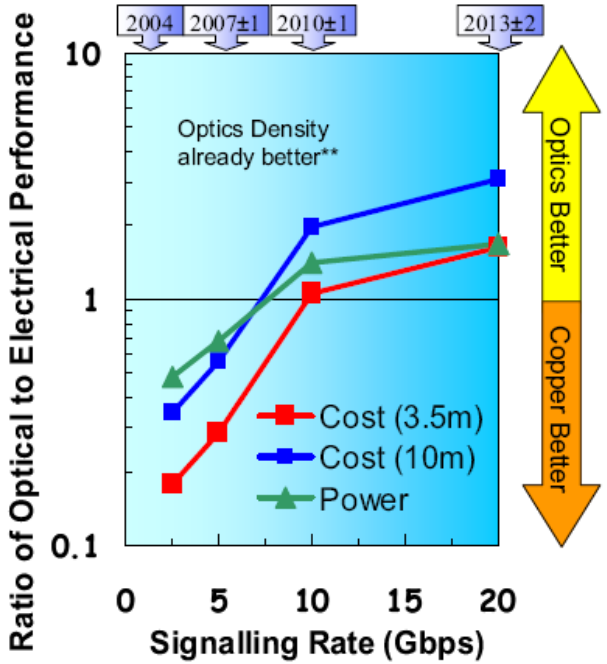


Fig. 1. Ratio of optical to electrical performance (cost, power) versus the data rate for short cabled interconnects. For electrical interconnects, much of the cost is in the cable and connectors, while for optics the cost is mainly in the transceivers. Electrical power consumption increases more rapidly with bitrate than optics due to the need for signal processing (i.e., equalization).

Pepeljugoski, P.; Doany, F.; Kuchta, D.; Schares, L.; Schow, C.; Ritter, M.; Kash, J., "Data Center and High Performance Computing Interconnects for 100 Gb/s and Beyond," *Optical Fiber Communication and the National Fiber Optic Engineers Conference, 2007. OFC/NFOEC 2007. Conference on* , vol., no., pp.1-3, 25-29 March 2007

- 3 types of communications:
  - chip-to-chip
  - shelf-to-shelf
  - rack-to-rack (<100m).
- Electrical downside
  - lower BW
  - higher dielectric losses in FR4
- Optical downside
  - No infrastructure to build quickly
  - Waveguides – "high absorptive losses", no standards
  - Fibers – can be costly $$,
- Optical seems choice for >50 m interconnect and > 2.5 Gbps (rack to rack)
- 3 factors that should be considered are **"power consumption, density, and (most importantly) cost"**

Data Centers

• 80% of all cables in the data center are less than 30m in length

• Principal interconnect options:
- •10GBASE-SR
- •10GBASE-T
- •CX4

•10GBase-SR: Optical multi-mode fiber.
- •Operating at as little as 1W.
- • Expensive lasers and transceiver electronics
- • Link cost of $500,
- • 10G based on optical is 2-3 times more than copper.

•10GBase-CX4: 8 twin-axial copper pairs.
- •Designed up to 15m.
- •Thick heavy cable.
- •High overall link cost

• 10GBase-T: Uses existing CAT5 copper cable
- •Employs RJ45 (or similar) connector.
- •High link cost.
- •4W per 30m link end.

• Active Twin-ax: Unable to support (usually) required 10Gbps data rate. Smaller link cost provides main advantage.

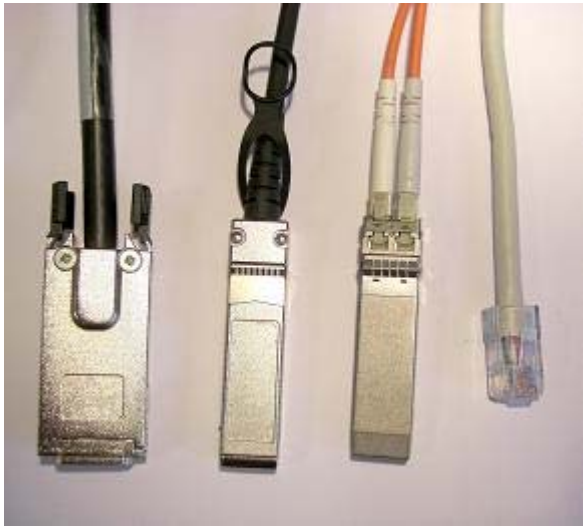


Figure 1: The different cable ends: left to right: SFF8470 connector for CX4, SFP+ for active twin-ax, SFP+ for optical fiber and RJ45 plug for 10GBASE-T.

http://datacenterjournal.com/index.php?option=com_content&task=view&id=1807&Itemid=41

The Data Center Journal. Article published 09 July, 2008. “Copper cabling can resolve the cost / power equation”

Data Centers

Solution	Power per port [W]	Port type	Reach	Interconnect	Link Cost
CX4	up to 1.6W	Dedicated copper SAS SFF8470	up to 15m	4 lanes of 3.125G copper in heavy gauge casing	$250
10GBASE-T	c. 4W	Dedicated copper RJ45	30m (or 100m)	CAT5/CAT6 copper cable	$500
Active Twin-ax	1W	Hot pluggable SFP+ or XFP	up to 30m	Thin gauge twin-ax copper cable	$150
10GBASE-SR	1W	Hot pluggable SFP+ or XFP	up to 300m	Optical Glass Fibre	$500

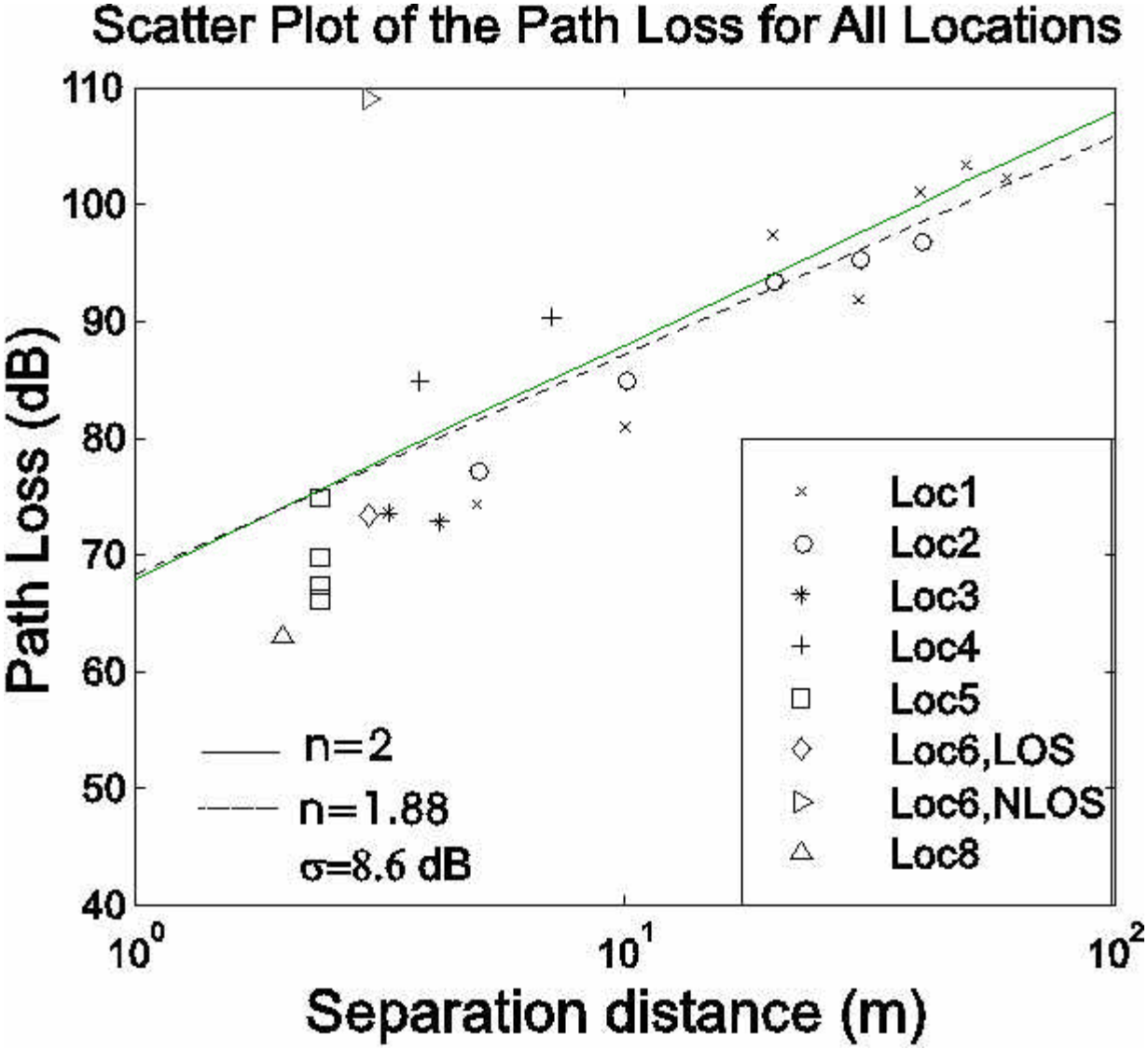
Solution	Power per port	California Elec $/kWh	Cost per year	CO2 per year per 160(ports [tonne]	OPEX cost per year pe datacenter cluster [$k
CX4	up to 1.6W	20.72	$291	17	465
10GBASE-T	c. 4W	20.72	$727	42	1162
Active Twin-ax	1W	20.72	$182	11	291
10GBASE-SR	1W	20.72	$182	11	291

http://datacenterjournal.com/index.php?option=com_content&task=view&id=1807&Itemid=41
The Data Center Journal. Article published on 09 July, 2008. “Copper cabling can resolve the cost / power equation”

60 GHz Sample Link Budget

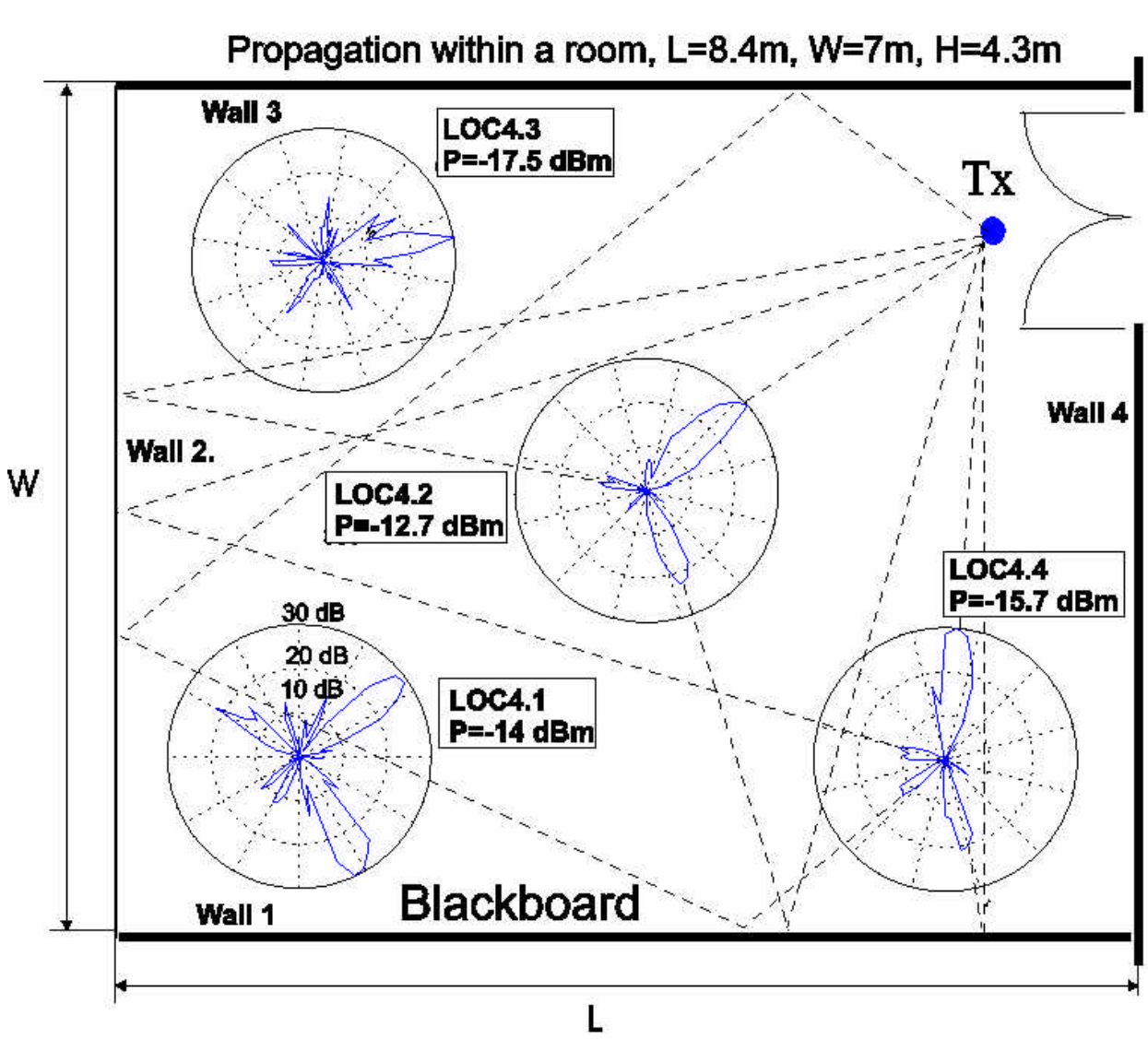
Example Link Budget	
Receiver Power (circuit)	200 mW
Transmitter Power before PA (circuit)	200 mW
Power to Antenna (PA)	600 mW x 50% efficient = 24.8 dBm
Overall Link Power	**1W (same as optics/copper)**
Free Space Path Loss @ 60 GHz	1 meter = -68 dB 10 meters = -88 dB
Modulation (**10 Gbps** over 2.5 GHz)	16-QAM (Gray Coded) (example)
SNR needed	**24 dB or better** for BER 10^-12, AWGN
Noise Power	kTB = 1x10^-11 J @ 2.5 GHz = -80 dBm
RX Signal Power Needed	-56 dBm or better
Received Power = Transmit Power + Antenna Gains (**assume 0 dBi**) – Path Loss	
Rx Power @ 1 meter	-43 dBm => SNR = **+37 dB**
Rx Power @ 10 meter	-63 dBm => SNR = **+17 dB** (will handle **5 Gbps** - QPSK)

*Similar link setup in Yang, L.L.; Park, M., "Applications and Challenges of Multi-band Gigabit Mesh Networks," *Sensor Technologies and Applications, 2008. SENSORCOMM '08. Second International Conference on*, vol., no., pp.813-818, 25-31 Aug. 2008.



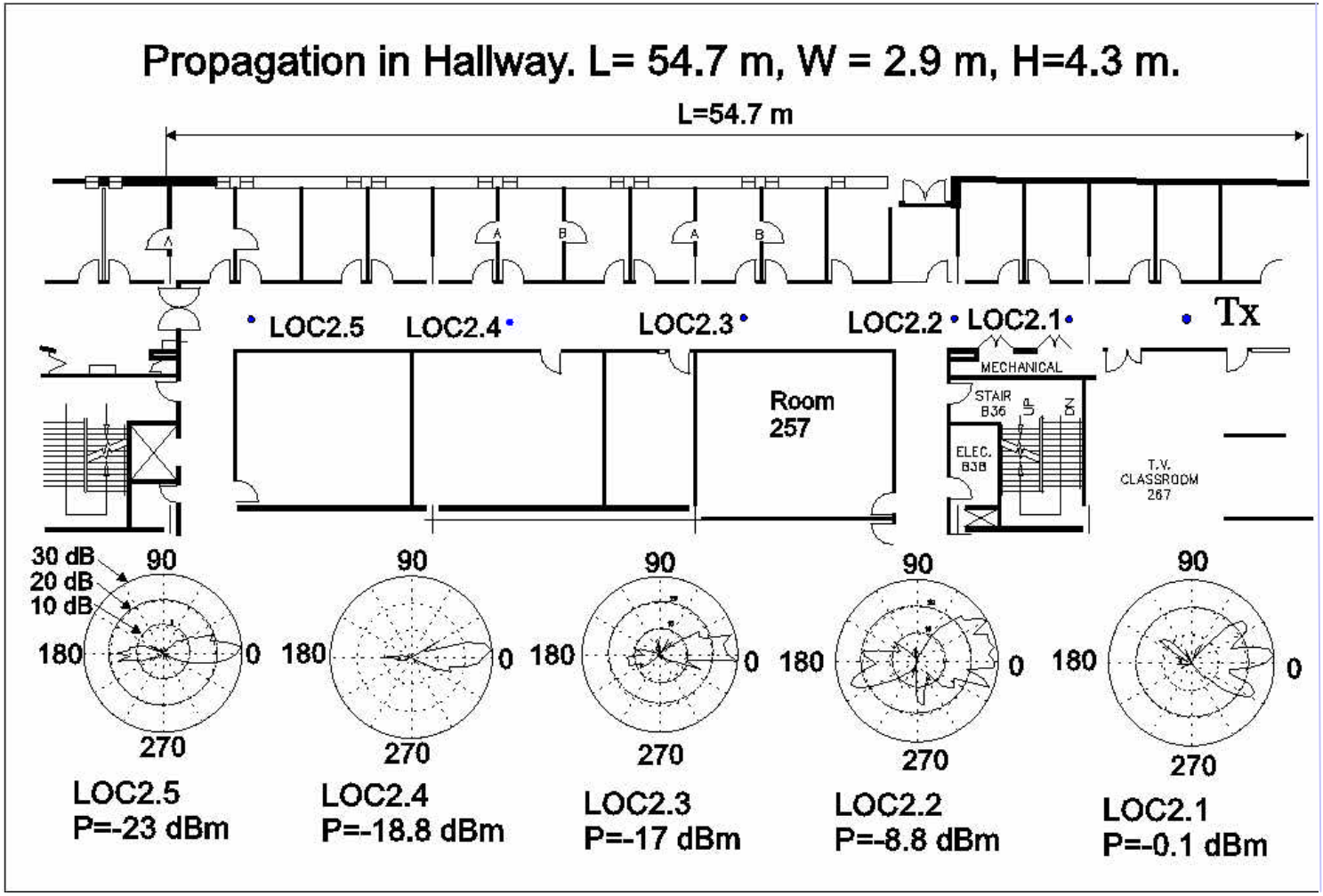
Scatter Plot of the Measured Path Loss Values

H. Xu, V. Kukshya, T. S. Rappaport, "Spatial and Temporal Characteristics of 60 GHz Indoor Channels," *IEEE Journal on Selected Areas in Communications*, Vol. 20, No. 3, April 2002, pp. 620 -630.



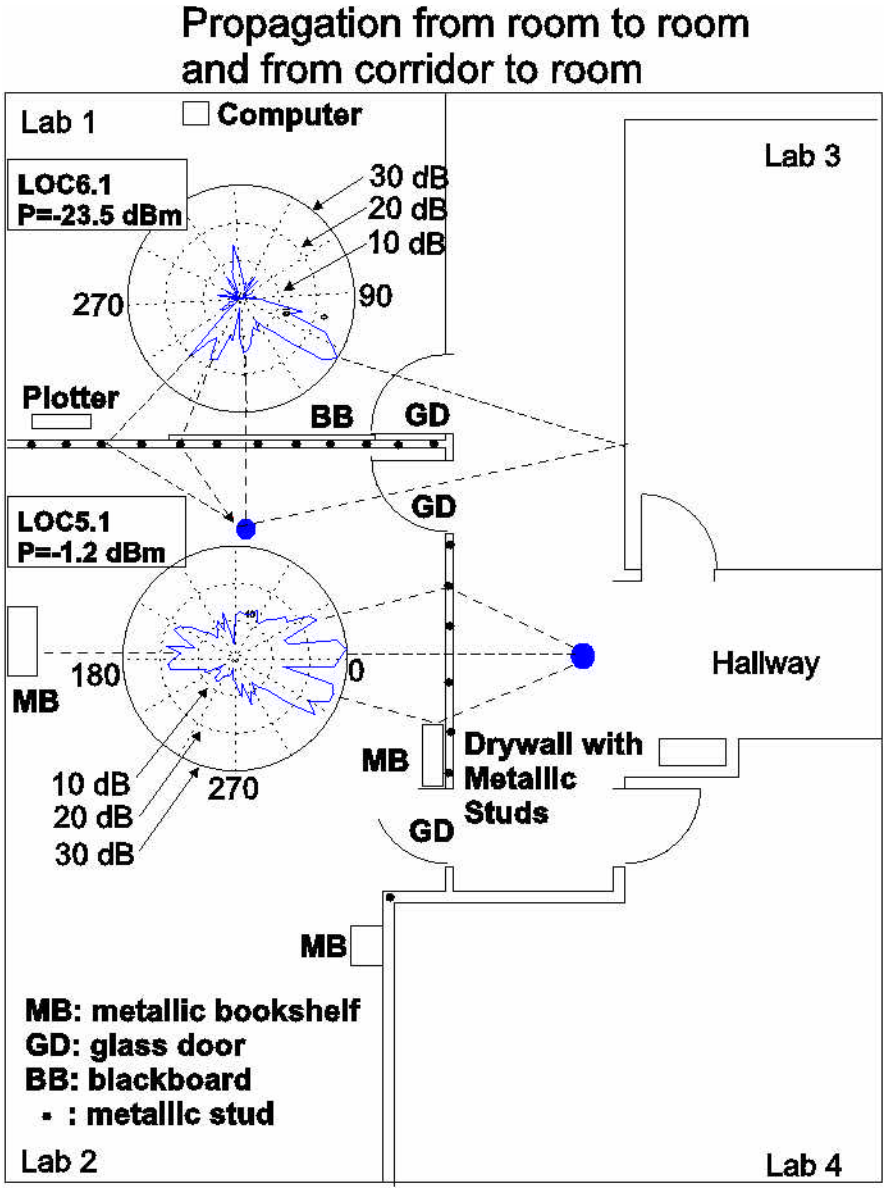
AOA measurements for propagation within a room (location 4), relative power levels given in polar plots and peak multipath power (P) given in text. Rays are shown only for locations 4.2 and 4.4 in the ¯gure, similar procedure can be performed for all the locations.

H. Xu, V. Kukshya, T. S. Rappaport, "Spatial and Temporal Characteristics of 60 GHz Indoor Channels," *IEEE Journal on Selected Areas in Communications*, Vol. 20, No. 3, April 2002, pp. 620 -630.



AOA measurements for propagation along a hallway (location 2), relative power levels given in polarplots and peak multipath power (P)

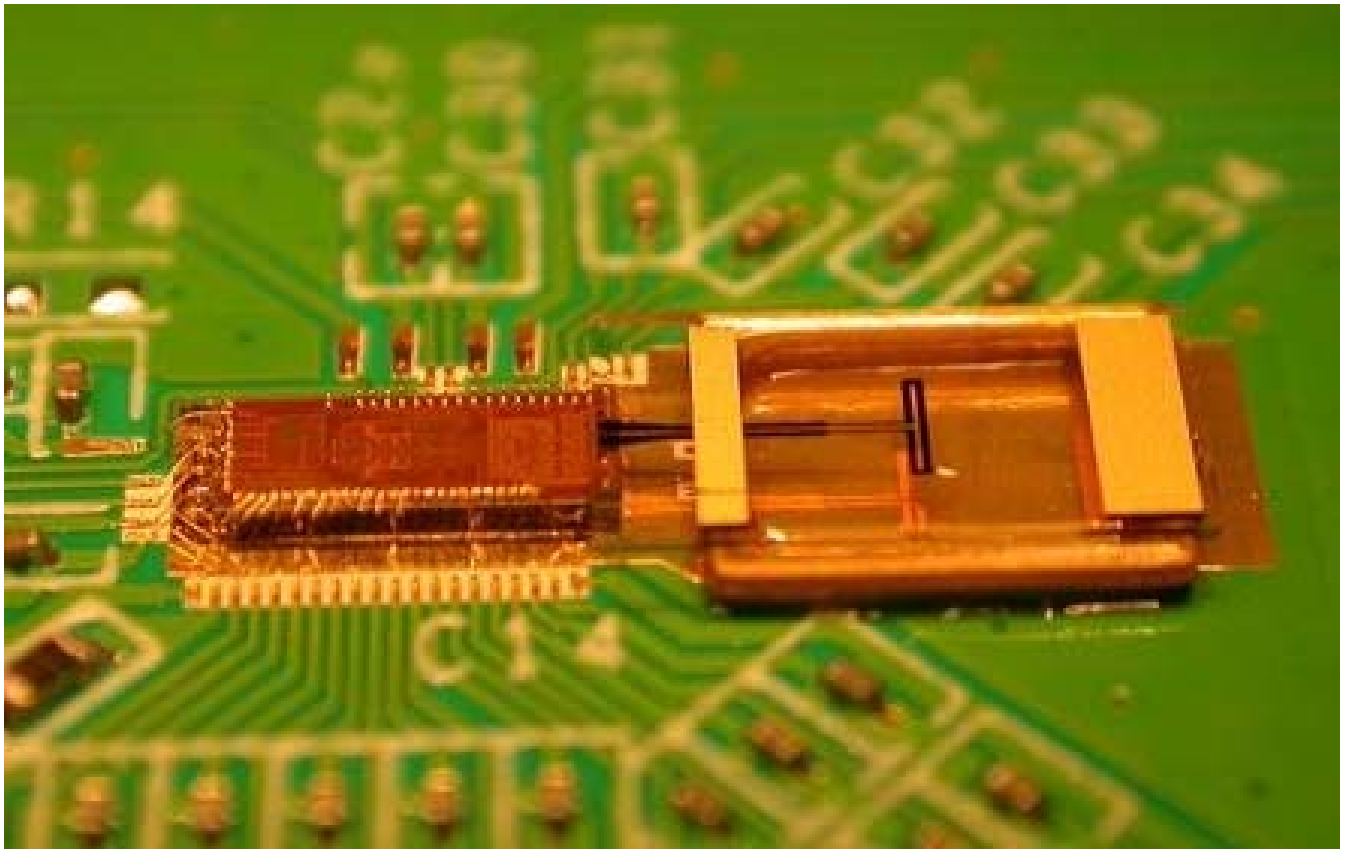
H. Xu, V. Kukshya, T. S. Rappaport, "Spatial and Temporal Characteristics of 60 GHz Indoor Channels," *IEEE Journal on Selected Areas in Communications*, Vol. 20, No. 3, April 2002, pp. 620 -630.



AOA measurements for propagation into rooms (locations 5 and 6), relative power levels given in polar plots and peak multipath power (P)

C. R. Anderson, T.S. Rappaport, "In-building wideband partition loss measurements at 2.5 and 60 GHz," IEEE Trans. Wireless Communications, Vol. 3, No. 3, May 2004, pp. 922 - 928

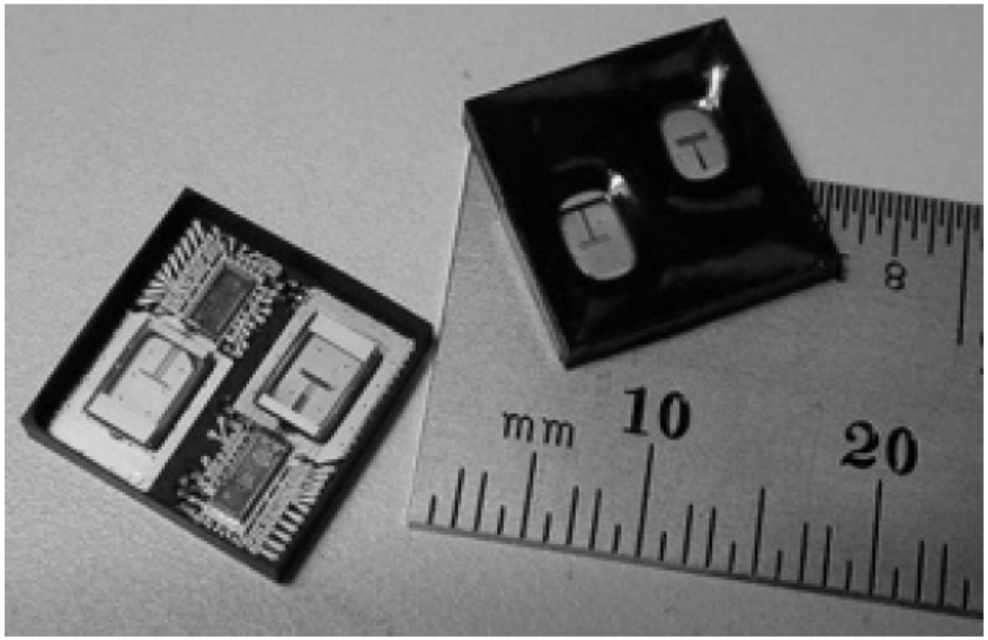
H. Xu, V. Kukshya, T. S. Rappaport, "Spatial and Temporal Characteristics of 60 GHz Indoor Channels," *IEEE Journal on Selected Areas in Communications*, Vol. 20, No. 3, April 2002, pp. 620 -630.

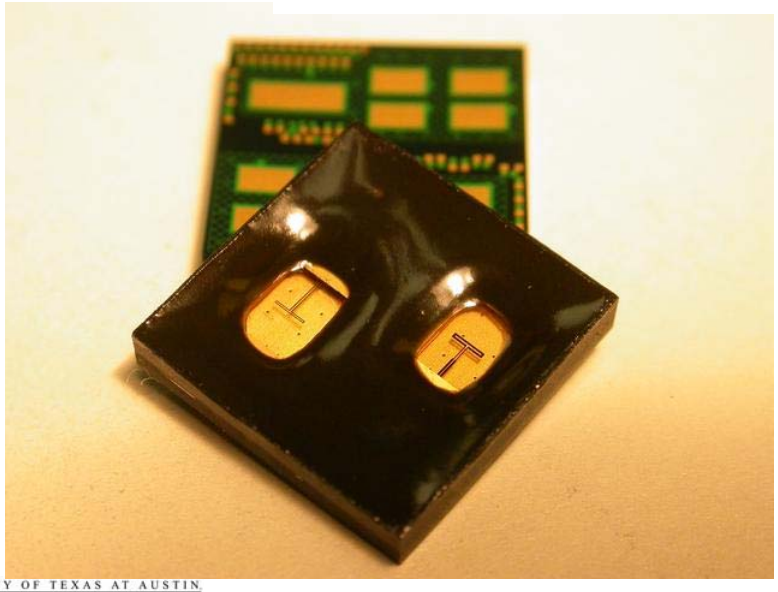


Credit by IBM

- IBM 60 GHz transceiver made in SiGe (2006)
- Size of a U.S. dime
- 630 Mbps throughput at a maximum range of 10 meters

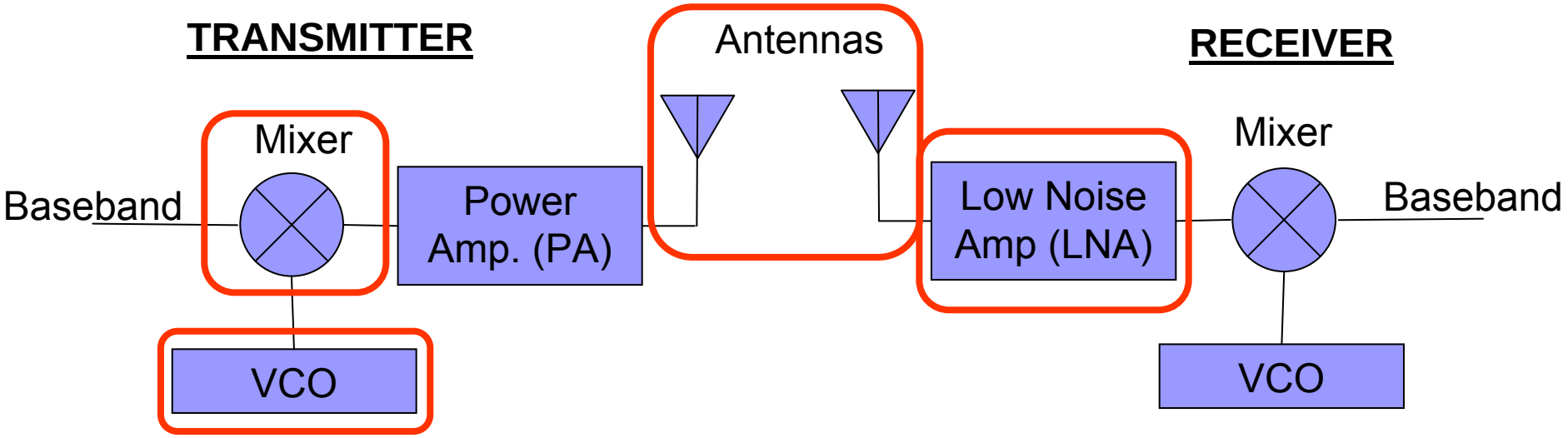
Reynolds, S.K.; Floyd, B.A.; Pfeiffer, U.R.; Beukema, T.; Grzyb, J.; Haymes, C.; Gaucher, B.; Soyuer, M., "A Silicon 60-GHz Receiver and Transmitter Chipset for Broadband Communications," *Solid-State Circuits, IEEE Journal of* , vol.41, no.12, pp.2820-2831, Dec. 2006





•IBM 60 GHz transceiver made in SiGe (2006)

RF Blocks at 60 GHz



Low Noise Amplifiers (LNAs)

- Challenges involved:
  - High Gains and Low Noise Figure desired
    - Difficult to achieve at mm-wave frequencies using CMOS
  - Inductors
    - Crucial component of LNAs at high frequencies
      - Lumped inductors – low Q
      - T-Lines – more area
  - Transistor layout and sizing
    - Minimize parasitic components
  - Input Matching with the antenna

LNAs State of the Art (CMOS)

Reference	Tech.	Power Gain (dB)	Noise Figure (dB)	P 1-dB (dBm)	Power Dissipation (mW)
A. Natarajan, ISSCC 2008	65-nm	15	5.9	15.1	30.8
C. Weyers, ISSCC 2008	65-nm	19.3	6.1	-16	35
E. Cohen, RFIC Symposium 2008	90-nm	15	4.4	-18	3.9
B. Razavi, JSSC 2008	90-nm	13.8	4.4	-25.5	6.4
T. Yao, JSSC 2007	90-nm	14.6	5.5	-6.8	24

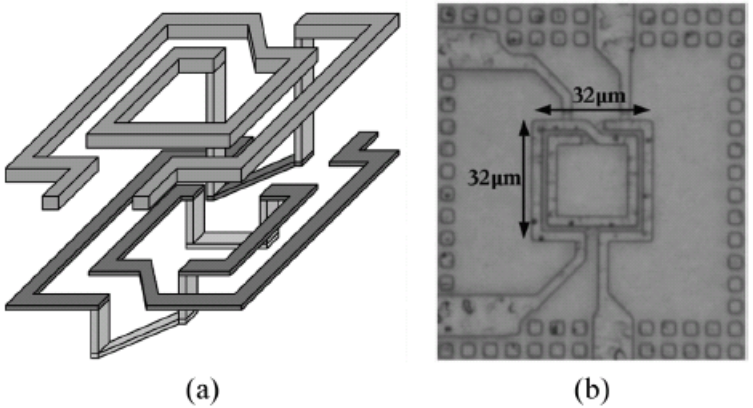
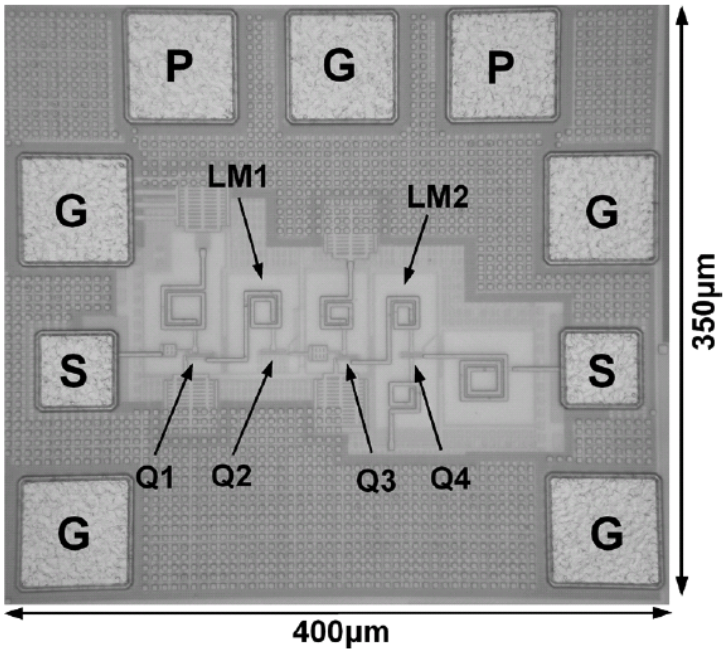


Fig. 7. (a) Design and (b) die micrograph of 1:1 vertically stacked 32 μm × 32 μm transformer in 90-nm CMOS.



- T. Yao, M. Gordon, K. Tang, et al.
- University of Toronto (2007)
- CMOS 90nm – 60 GHz

- 2-stage design

- 16mA @ 1.5 V supply = **24 mW**

- Power Gain: 14.6 dB
- NF: 5.5 dB

Terry Yao; Gordon, M.Q.; Tang, K.K.W.; Yau, K.H.K.; Ming-Ta Yang; Schvan, P.; Voinigescu, S.P., "Algorithmic Design of CMOS LNAs and PAs for 60-GHz Radio," *Solid-State Circuits, IEEE Journal of* , vol.42, no.5, pp.1044-1057, May 2007

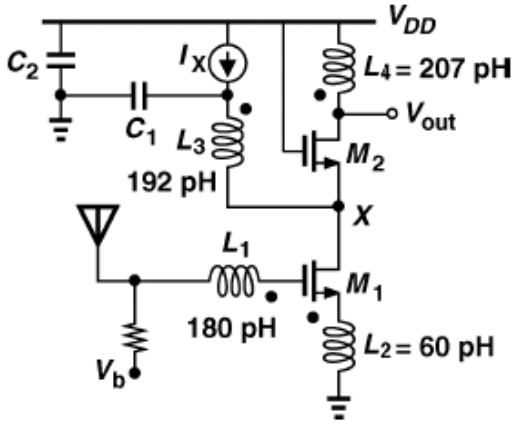


Fig. 3. LNA implementation.

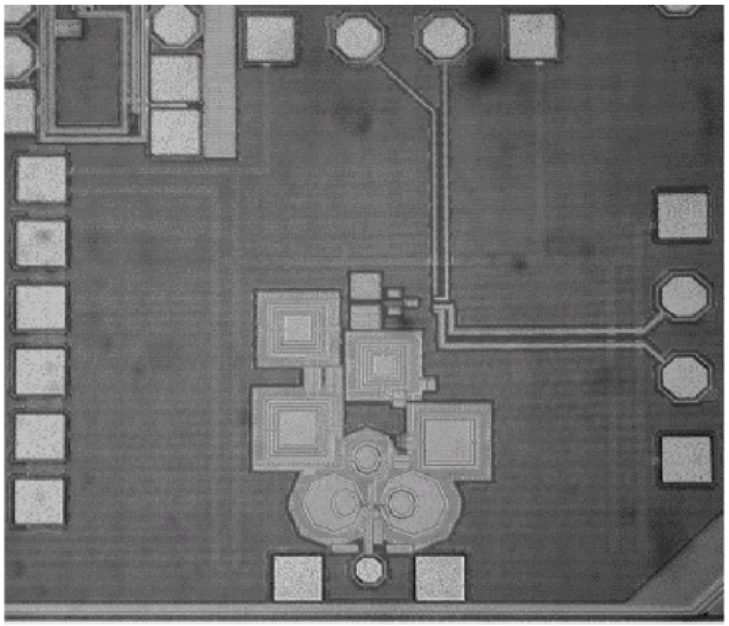


Fig. 11. Receiver die photograph.

- Behzad Razavi
- UCLA (2008)
- CMOS 90nm – 60 GHz

- Single stage design

- 1.8 V supply = **6.4 mW**

- Power Gain: 13.8 dB
- NF: 4.4 dB

Razavi, B., "A Millimeter-Wave CMOS Heterodyne Receiver With On-Chip LO and Divider," *Solid-State Circuits, IEEE Journal of* , vol.43, no.2, pp.477-485, Feb. 2008

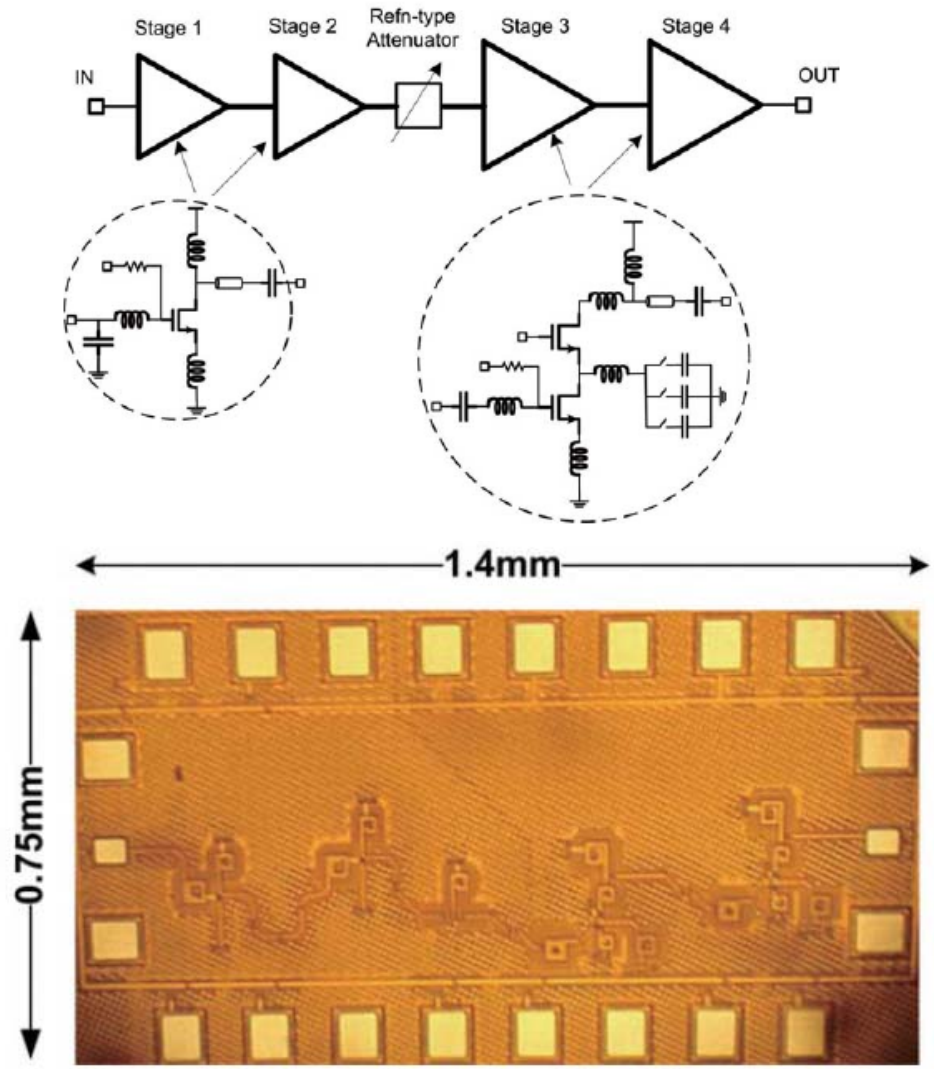


Fig. 5. Die photograph of 60GHz LNA

- A. Natarajan, et al.
- IBM (2008)
- CMOS 65nm – 60 GHz
- 1.5 V supply = **30.8 mW**
- 4-stage LNA
- Power Gain: 15 dB
- NF: 5.9 dB

Natarajan, A.; Nicolson, S.; Ming-Da Tsai; Floyd, B., "A 60GHz variable-gain LNA in 65nm CMOS," *Solid-State Circuits Conference, 2008. A-SSCC '08. IEEE Asian* , vol., no., pp.117-120, 3-5 Nov. 2008

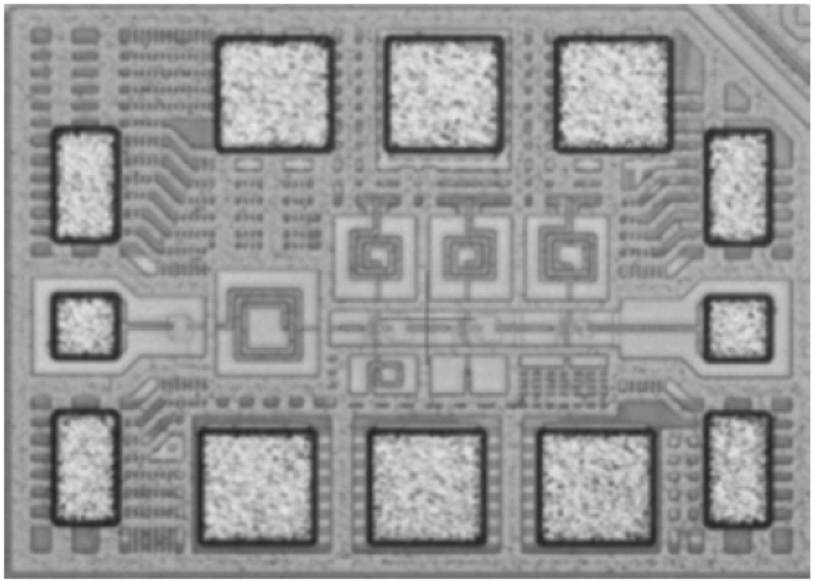


Fig. 6. LNA die 440 um x 320 um.

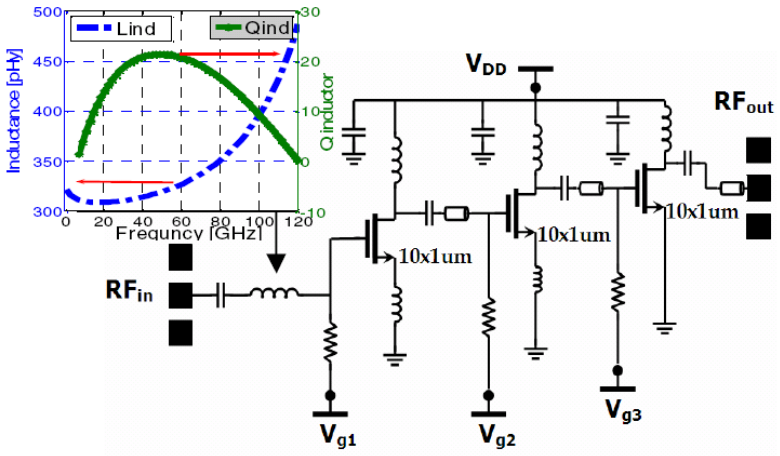


Fig. 5. Schematic of 3 stage CS design with input inductor.

- E. Cohen et al.
- Intel (2008)
- CMOS 90nm – 60 GHz
- 1.3 V supply = **3.9 mW**
- 3-stage LNA
- Power Gain: 15 dB
- NF: 4.4 dB

Cohen, E.; Ravid, S.; Ritter, D., "An ultra low power LNA with 15dB gain and 4.4db NF in 90nm CMOS process for 60 GHz phase array radio," *Radio Frequency Integrated Circuits Symposium, 2008. RFIC 2008. IEEE* , vol., no., pp.61-64, June 17 2008-April 17 2008

Mixers

- Challenges Involved
  - Isolation between LO, RF and IF ports at high frequencies
  - Low Noise Figures desired as LNA gains are not very high at mm-wave frequencies

Mixers State of the Art (CMOS)

Reference	Tech.	Conversion Gain (dB)	Noise Figure (dB)	LO-RF Isolation	Power Dissipation (mW)
Chung-Yu Wu, IEEE MWCL 2008	130-nm	1	-	-37 dB	3.6
B. Razavi, JSSC 2008	90-nm	10.2	12.5	-	23.4
W. Shieh, RFIC Symposium 2007	130-nm	2	-	-36 dB	7.2

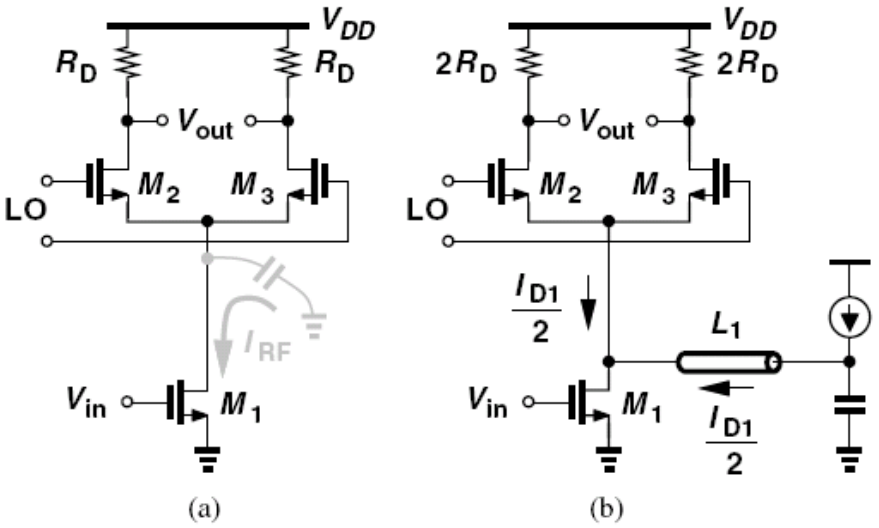
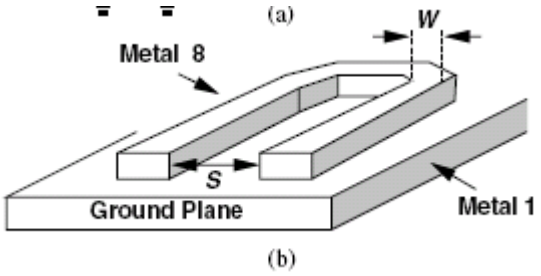


Fig. 3. (a) Conventional and (b) proposed mixer topologies.



- Behzad Razavi
- UCLA (2006)
- CMOS 130nm – 60 GHz
- 1.2 V supply = **9 mW**
- Folded microstrips as inductors

Razavi, B., "CMOS transceivers for the 60-GHz band," *Radio Frequency Integrated Circuits (RFIC) Symposium, 2006 IEEE* , vol., no., pp.4 pp.-, 11-13 June 2006

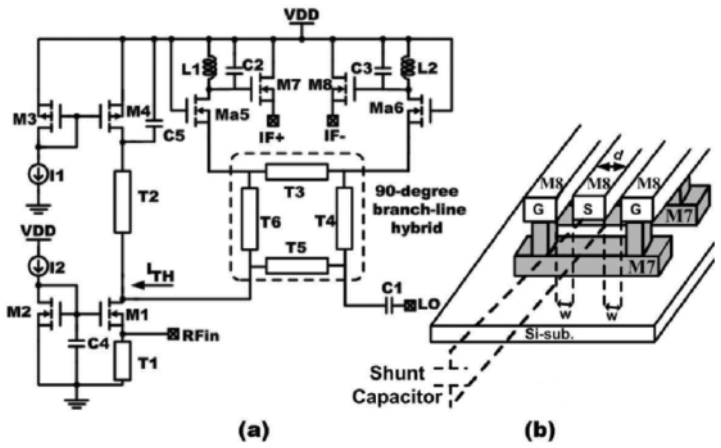
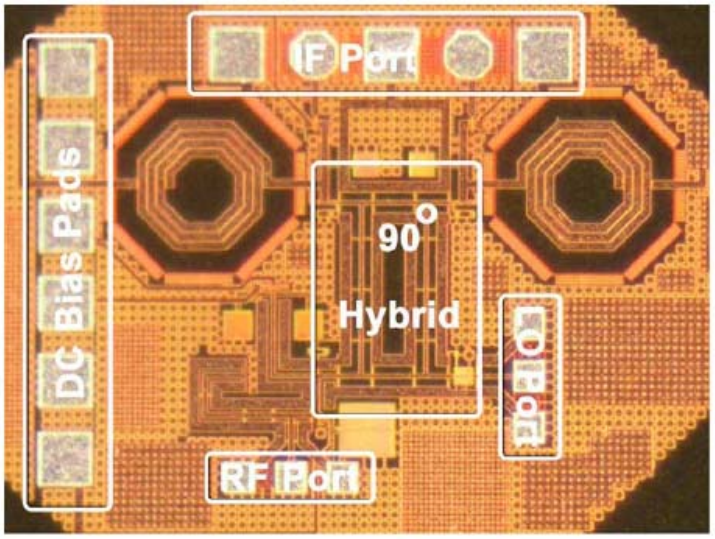


Fig. 2. (a) Circuit diagram of the CMOS quadrature-balanced current-mode mixer. (b) Coplanar waveguide transmission lines with the shunt capacitor.



- F. Shahroury, C.-Y. Wu.
- National Chiao-Tung University (2008)
- CMOS 130nm – 60 GHz
- 3ma @ 1.2 V supply = **3.6 mW**
- Improve LO/RF isolation with hybrid coupler and quadrature-balanced architecture

Shahroury, F.R.; Chung-Yu Wu, "The Design of Low LO-Power 60-GHz CMOS Quadrature-Balanced Self-Switching Current-Mode Mixer," *Microwave and Wireless Components Letters, IEEE* , vol.18, no.10, pp.692-694, Oct. 2008

Voltage Controlled Oscillators (VCOs)

- Challenges Involved
  - Fundamental oscillation frequency limited by unity gain frequency of the transistor
  - Low parasitic, high Q resonator
    - Large Tuning Range BUT high phase noise
  - Low parasitic, high gain transistors
  - Inductor and varactor design forms the crux
    - Lumped elements – low Q but also small area

VCOs State of the Art (CMOS)

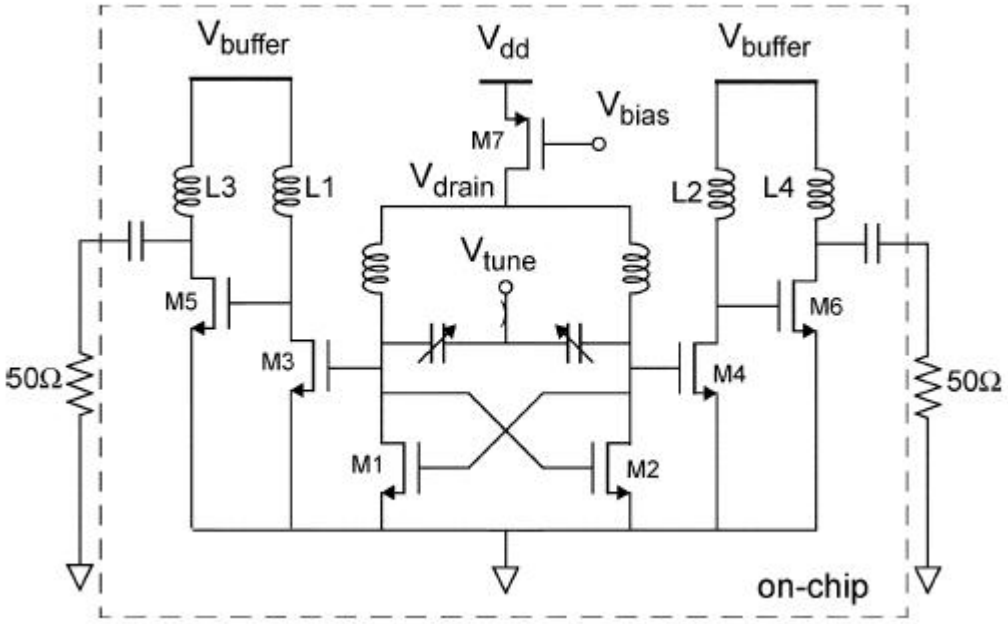
Reference	Tech.	Tuning Range	Phase Noise (dBc/Hz)	Power Dissipation (mW)
Shey-Shi Lu, IEEE MWCL 2008	130-nm	4.5% @ 68 GHz	-98.4 @ 1 MHz Offset	4.32
Kenneth O., JSSC 2006	130-nm	6.3% @ 60 GHz	-109 @ 10 MHz Offset	9.75
Kenneth O., IEEE MWCL 2006	90-nm	0.9% @ 140 GHz	-85 @ 2 MHz Offset	9.6
B. Razavi, JSSC 2008	90-nm	Operates at 128 GHZ	-105 @ 10 MHz Offset	9
K. Ishibashi, VLSI Circuits Symposium, 2007	90-nm	7% @ 76.5 GHz	-110.6 @ 10 MHz Offset	13.6

TABLE I

PERFORMANCE COMPARISON OF STATE-OF-THE-ART MILLIMETER-WAVE VCO

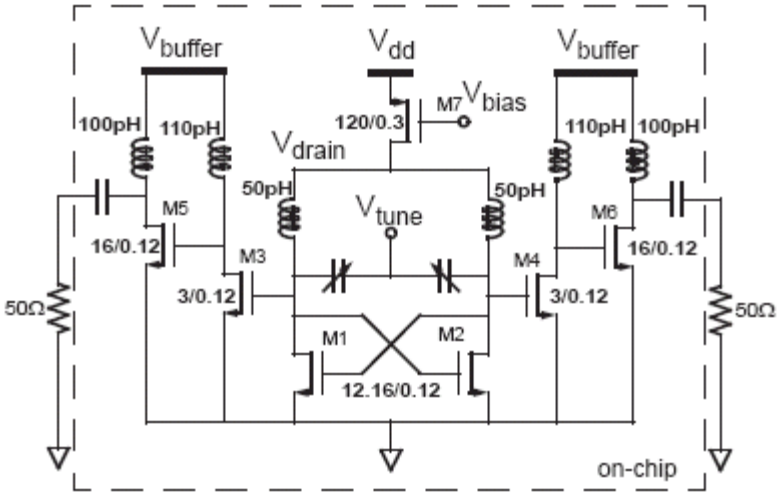
Ref.	Technology [μm]	Technique Note	f_o [GHz]	FTR [%]	PN [dBc/Hz]		Power [mW]	FOM [dBc/Hz]		FOM_t [dBc/Hz]	
					1MHz	10MHz		1MHz	10MHz	1MHz	10MHz
[1] ISSCC 2001	CMOS 0.25	MOS-Var.	50	2	-97	/	13 @1.3V	-179.8	/	-165.8	/
[2] JSSC 2006	CMOS 0.13	MOS-Var.	56.5	10.27	-89	-108	9.8 @1.5V	-174.13	-173.13	-174.36	-173.36
			98.5	2.54	/	-102.7	7 @1.5V	/	-174.12	/	-161.63
[3] ISSCC 2005	CMOS 0.12	Differential MOS-Var.	44	9.8	-101	/	7.5 @1.5V	-185	/	-184.8	/
[4] ISSCC 2007	CMOS 0.065	MOS-Var.	70.2	9.55	/	-106.14	5.4 @1.2V	/	-175.76	/	-175.36
[5] ISSCC 2005	CMOS 0.13	Push-Push MOS-Var.	114	2.11	/	-107.6	8.4 @1.2V	/	-179.5	/	-165.96
[6] EL 2006	CMOS 0.13	Push-Push MOS-Var.	192.1	0.68	/	-100	16.5 @1.5V	/	-173.49	/	-150
[8] ISSCC 2006	CMOS 0.09	Resonator	60	0.2	-100	/	1.9 @1.0V	-193	/	-158.8	/
This Work	CMOS 0.13	Intrinsic Cap.	69.8	4.5	-98.4	-115.2	4.32 @0.6V	-188.9	-185.7	-182	/-178.8

Hsien-Ku Chen; Hsien-Jui Chen; Da-Chiang Chang; Ying-Zong Juang; Shey-Shi Lu, "A 0.6 V, 4.32 mW, 68 GHz Low Phase-Noise VCO With Intrinsic-Tuned Technique in 0.13 um CMOS," *Microwave and Wireless Components Letters, IEEE* , vol.18, no.7, pp.467-469, July 2008



- Changhua Cao, Kenneth K. O
- University of Florida (June 2006)
- CMOS 130nm – 60 GHz
- Consumes 6.5mA @ 1.5 V = **9.75 mW**
- Limited by Q of the capacitors
- Accurate characterizing and modeling of varactors is crucial.

Changhua Cao; O, K.K., "Millimeter-wave voltage-controlled oscillators in 0.13-μm CMOS technology," *Solid-State Circuits, IEEE Journal of* , vol.41, no.6, pp. 1297-1304, June 2006



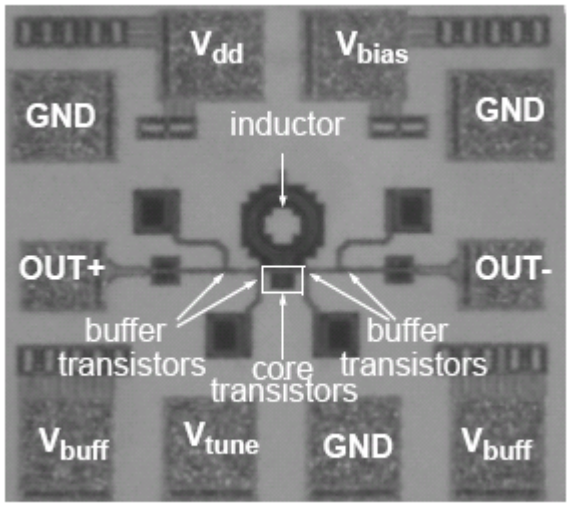


Fig. 4. A die micro-photograph of the VCO.

- Changhua Cao, Kenneth K. O
- University of Florida (June 2005)
- CMOS 130nm – 90 GHz

- Consumes 5-10.5mA @ 1.5 V

- If a “push-push” configuration was used, able to achieve nearly 200 GHz

Changhua Cao; O, K.K., "A 90-GHz voltage-controlled oscillator with a 2.2-GHz tuning range in a 130-nm CMOS technology," *VLSI Circuits, 2005. Digest of Technical Papers. 2005 Symposium on* , vol., no., pp. 242-243, 16-18 June 2005

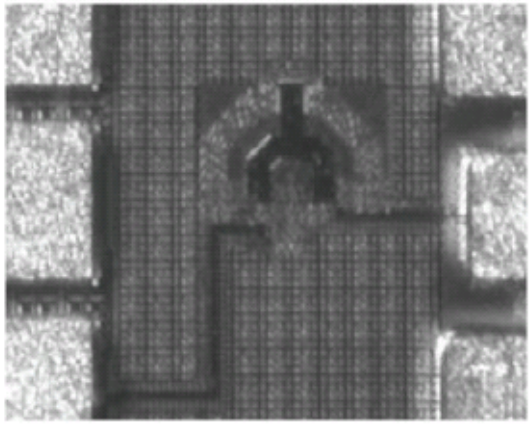


Fig. 5. Chip micrograph of W-band CMOS VCO.

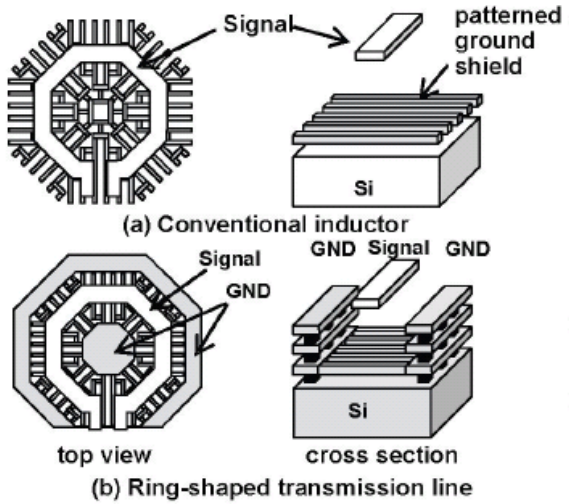


Fig. 2. Schematic view of a conventional inductor and a ring-shaped transmission line.

- Ishibashi, K., Motoyoshi, M., et al.
- University of Tokyo (2007)
- CMOS 90nm – 76 GHz

- Consumes 19.4mA @ 0.7V = **13.6 mW**

- Used “half-ring low-loss inductors” to double tuning range

Ishibashi, K.; Motoyoshi, M.; Kobayashi, N.; Fujishima, M., "76GHz CMOS Voltage-Controlled Oscillator with 7% Frequency Tuning Range," *VLSI Circuits, 2007 IEEE Symposium on* , vol., no., pp.176-177, 14-16 June 2007

On-chip Antennas at mmWaves

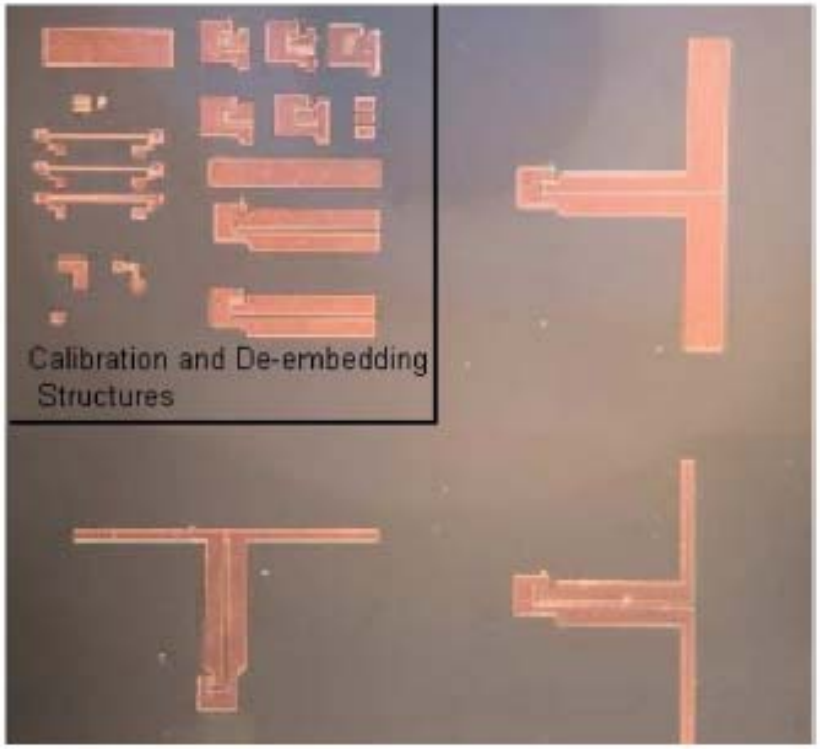


Fig. 4. Microphotograph of the copper antenna and balun structure.

• Atif Shamim, Langis Roy, Neric Fong, N. Garry Tarr (2008)

•Carleton University, Ottawa, Canada

•On-chip dipole antenna for 24 GHz
  •Bulk Si

• **Gain: about -8 to -10.5 dBi**

•Reported interesting graphs of Gain vs.
  •Substrate Thickness
  •Oxide Thickness
  •Metal Thickness
  •Substrate Resistivity

•3mm x .5 mm

Shamim, A.; Roy, L.; Fong, N.; Tarr, N.G., "24 GHz On-Chip Antennas and Balun on Bulk Si for Air Transmission," *Antennas and Propagation, IEEE Transactions on* , vol.56, no.2, pp.303-311, Feb. 2008.

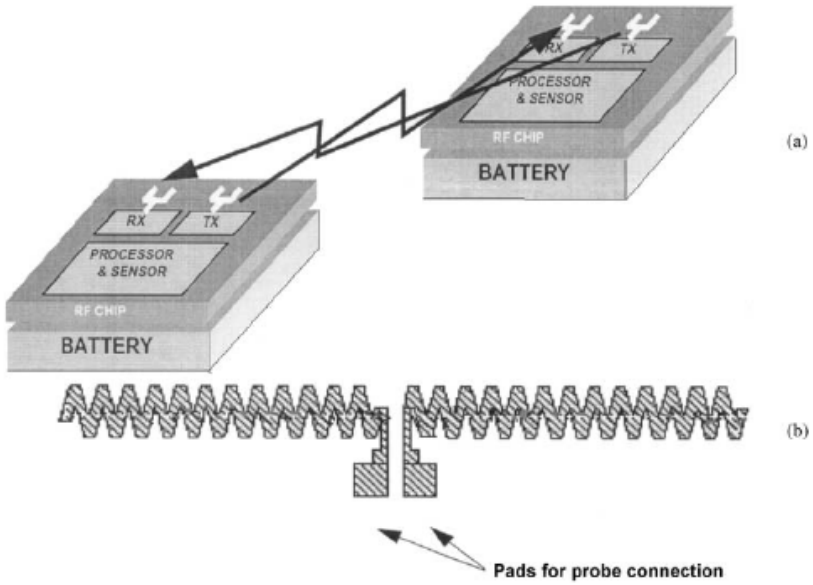


Fig. 1. (a) μNode: a true single chip radio. The working range can be up to 5 m. (b) Layout of a 2-mm zigzag dipole antenna.

- Jau-Jr Lin, Li Gao, Ken O et. al (2004)
- University of Florida – Gainesville

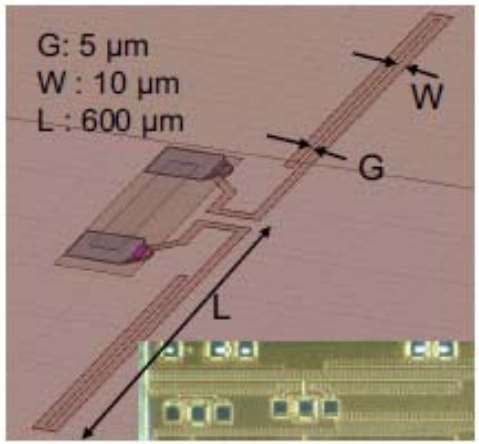
- On-chip zigzag dipole antenna for CMOS 24 GHz

- Gain: about -10 to -14 dBi

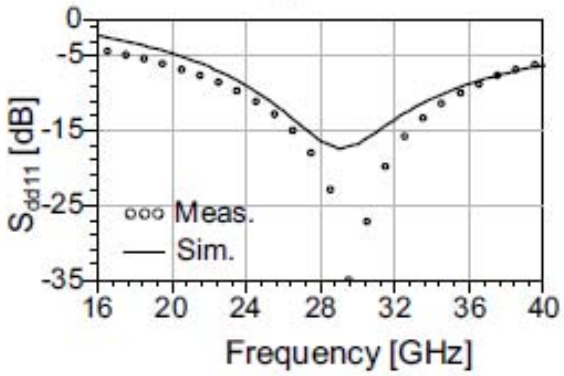
- Efficiency: 10-15%
  - Reported higher efficiency of zigzag than straight linear dipole

- 2 mm long antenna

Lin, J.-J.; Li Gao; Sugavanam, A.; Xiaoling Guo; Ran Li; Brewer, J.E.; O, K.K., "Integrated antennas on silicon substrates for communication over free space," *Electron Device Letters, IEEE* , vol.25, no.4, pp. 196-198, April 2004



(a)



(b)

Figure 4. (a) Designed folded dipole antenna. (b) measured and simulated differential return loss (S_{dd11}) of the antenna.

- Piljae Park; Yue, C.P., (2008)
- University of California, Santa Barbara
- On-chip folded dipole antenna for 24 GHz
- Fabricated on 8-metal standard CMOS
- Gain: -22.6 dBi
- Bandwidth: 13.5 GHz
- 1.2 mm x 25 um

Piljae Park; Yue, C.P., "A feasibility study of on-wafer wireless testing," *VLSI Design, Automation and Test, 2008. VLSI-DAT 2008. IEEE International Symposium on* , vol., no., pp.299-302, 23-25 April 2008.

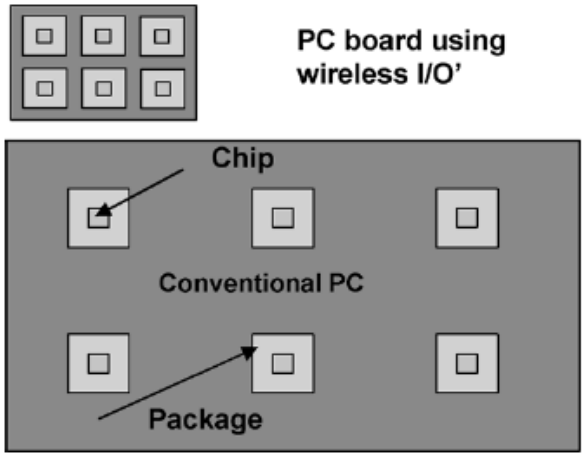


Fig. 3. Printed circuit board with circuits utilizing wireless interconnects.

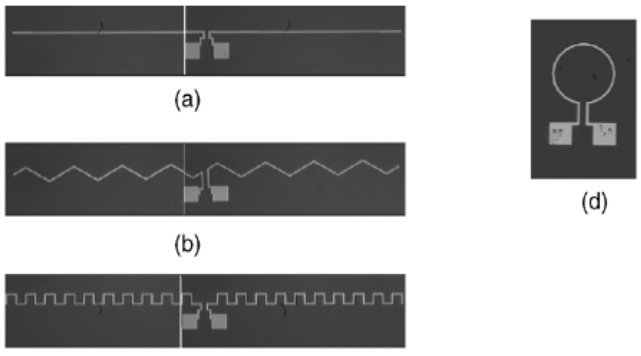


Fig. 4. (a)–(d) Linear, zigzag, and meander, and loop antennas fabricated on silicon. (e) A cross-section.

- Ken O et. al (2005)
- University of Florida – Gainesville
- Proposes ideas for antennas and applications
- CMOS technology @ 10+ GHz
- Intra-Chip Wireless
- Clock Distribution
- Inter-Chip Wireless
- 2mm antennas

O, K.K.; Kihong Kim; Floyd, B.A.; Mehta, J.L.; Hyun Yoon; Chih-Ming Hung; Bravo, D.; Dickson, T.O.; Xiaoling Guo; Ran Li; Trichy, N.; Caserta, J.; Bomstad, W.R., II; Branch, J.; Dong-Jun Yang; Bohorquez, J.; Seok, E.; Li Gao; Sugavanam, A.; Lin, J.-J.; Jie Chen; Brewer, J.E., "On-chip antennas in silicon ICs and their application," *Electron Devices, IEEE Transactions on* , vol.52, no.7, pp. 1312-1323, July 2005

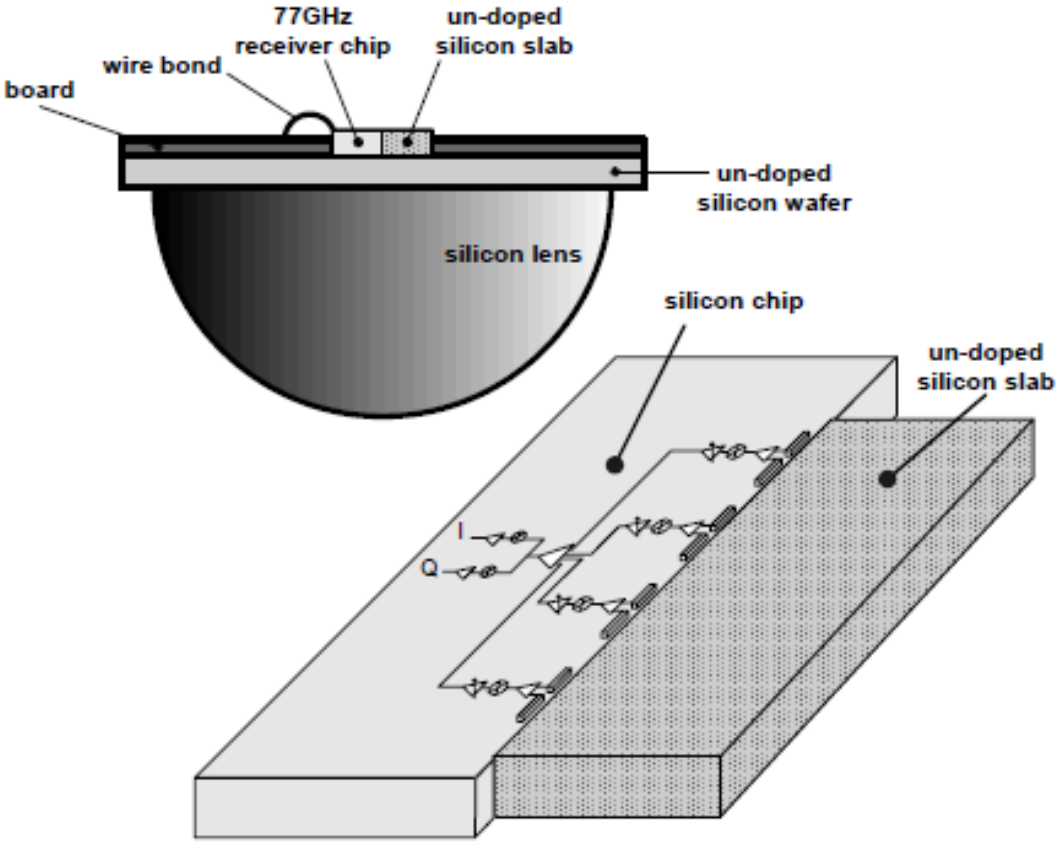


Figure 10.1.1: Chip, board, and lens antenna setup configuration.

- Babakhani, A.; Guan, X.; Komijani, A.; Natarajan, A.; Hajimiri, A., (2006)

- California Institute of Technology–Pasadena

- 4-element array of on-chip dipoles for 77 GHz using 120nm SiGe BiCMOS

- Silicon lensing technique to boost gains

- Gain: +2 dBi

- Antenna area less than 0.02mm^2

Babakhani, A.; Guan, X.; Komijani, A.; Natarajan, A.; Hajimiri, A., "A 77GHz 4-Element Phased Array Receiver with On-Chip Dipole Antennas in Silicon," *Solid-State Circuits Conference, 2006. ISSCC 2006. Digest of Technical Papers. IEEE International* , vol., no., pp.629-638, 6-9 Feb. 2006.

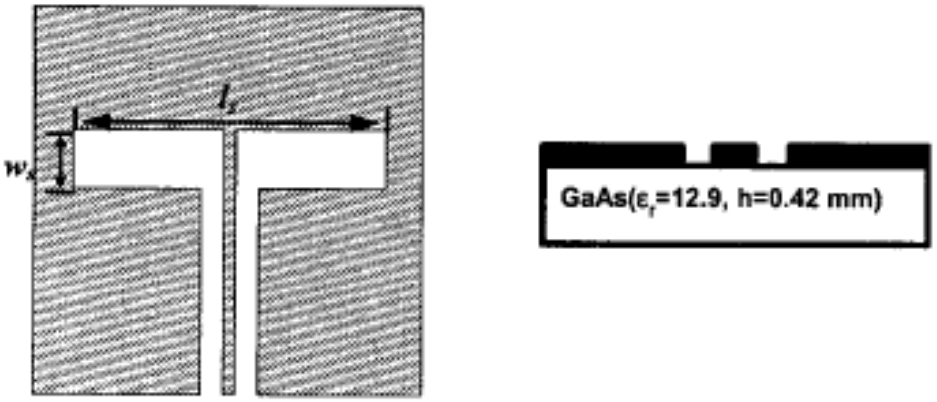


Fig. 1. The configuration of CPW fed slot dipole antenna.

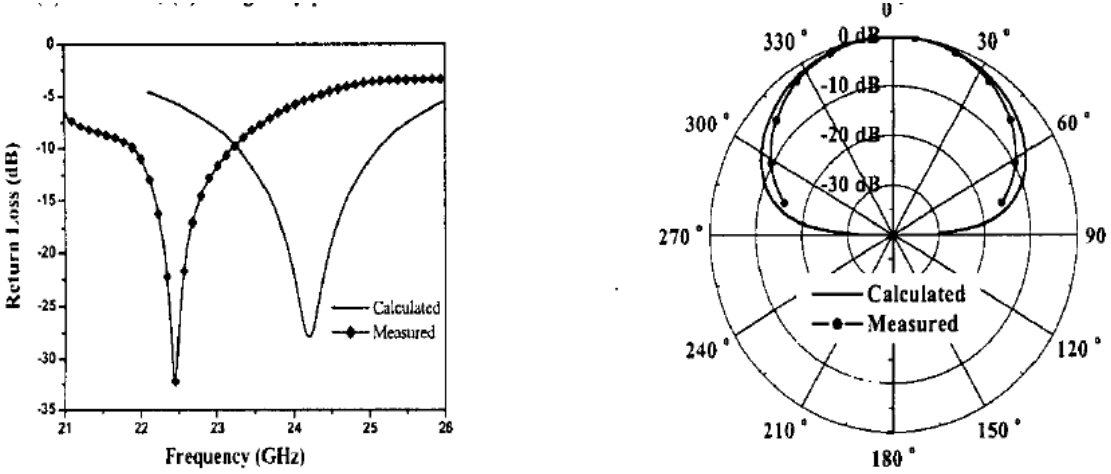
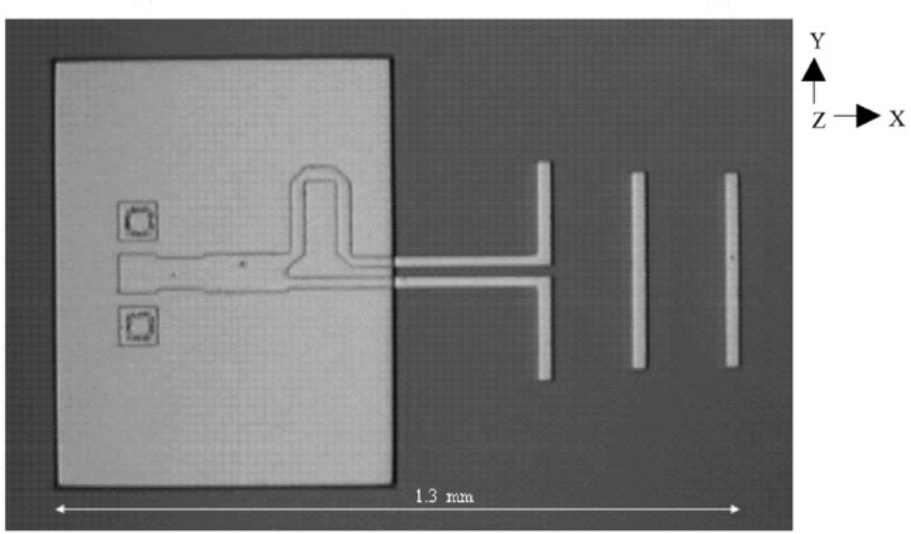


Fig. 4. Measured performance of antenna, (a) S-parameter, radiation pattern measurements in H-plane.

- S. K. Padhi, N.C . Karmakar and C.L. Law (2002)
- Nanyang Technological University, Singapore
- Slot Dipole for mmWaves on GaAs substrate @ 24 GHz
- Bandwidth: 6.1%
- Gain: +2 dBi
- 3.67 mm x 1.2 mm

Padhi, S.K.; Karmakar, N.C.; Law, C.L., "CPW fed MMIC slot dipole for MM-wave applications," *Antennas and Propagation Society International Symposium, 2002. IEEE* , vol.1, no., pp. 414-417 vol.1, 2002 .



•Y.P. Zhang, M. Sun, L.H. Guo

•Yagi antenna on-chip

• Nanyang Technological University, Singapore (2005)

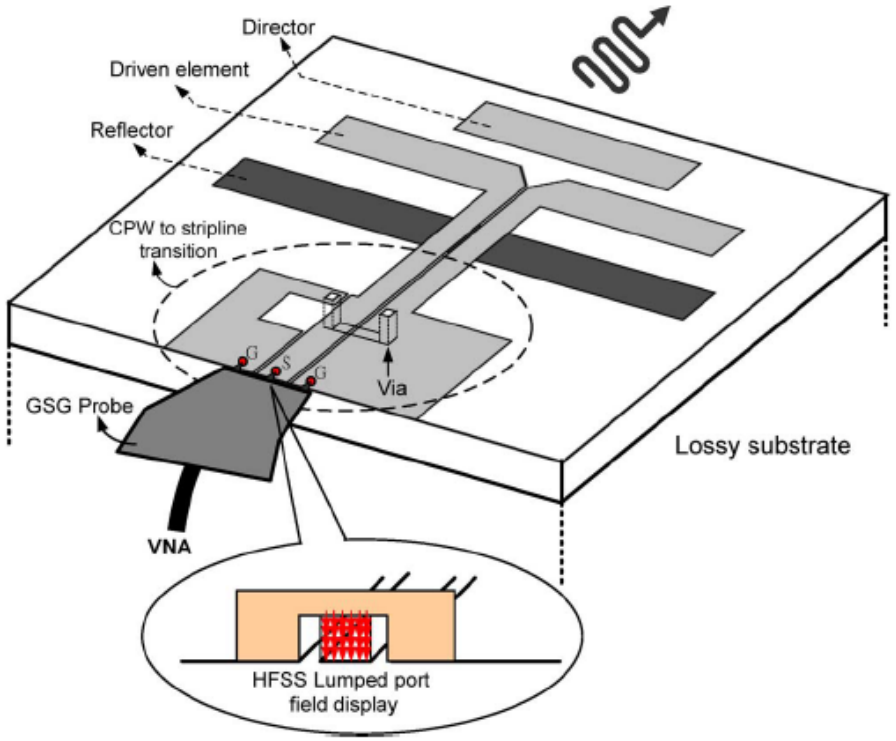
•Gain: -12.5 dBi

•Efficiency: 2%

•CMOS with post-BEOL process @ 60 GHz

•1.3 mm x .7 mm

Zhang, Y.P.; Sun, M.; Guo, L.H., "On-chip antennas for 60-GHz radios in silicon technology," *Electron Devices, IEEE Transactions on* , vol.52, no.7, pp. 1664-1668, July 2005



- Shun-Sheng Hsu, Kuo-Chih Wei, Cheng-Ying Hsu, Huey Ru-Chuang
- National Cheng Kung University (2008)
- CMOS .18 um technology
- Gain: - 10.6 dBi
- Efficiency: 10% (simulated)
- Chip size: 1.05 mm^2

Shun-Sheng Hsu; Kuo-Chih Wei; Cheng-Ying Hsu; Huey Ru-Chuang, "A 60-GHz Millimeter-Wave CPW-Fed Yagi Antenna Fabricated by Using 0.18 um CMOS Technology," *Electron Device Letters, IEEE* , vol.29, no.6, pp.625-627, June 2008

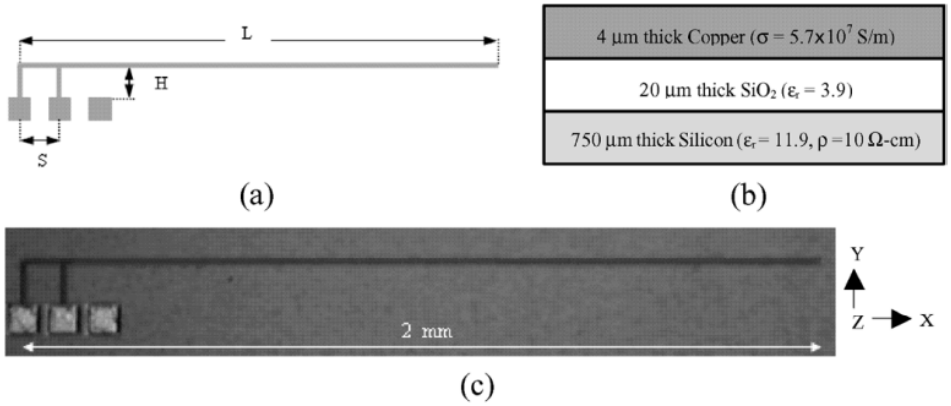


Fig. 1. On-chip inverted-F antenna: (a) layout, (b) cross-sectional view, and (c) top view photograph.

•Y.P. Zhang, M. Sun, L.H. Guo

•Planar Inverted F Antenna

• Nanyang Technological University, Singapore (2005)

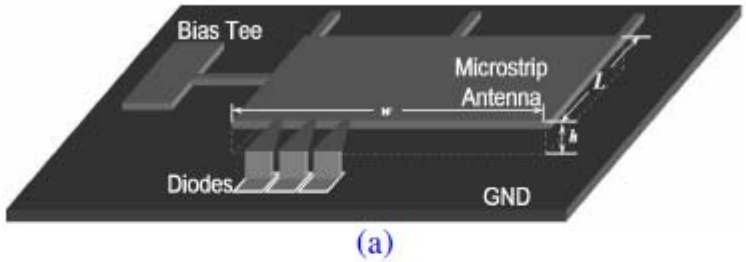
•Gain: -19 dBi

• Efficiency: 1.7%

•CMOS with post-BEOL process @ 60 GHz

•2 mm x 0.1 mm

Zhang, Y.P.; Sun, M.; Guo, L.H., "On-chip antennas for 60-GHz radios in silicon technology," *Electron Devices, IEEE Transactions on* , vol.52, no.7, pp. 1664-1668, July 2005



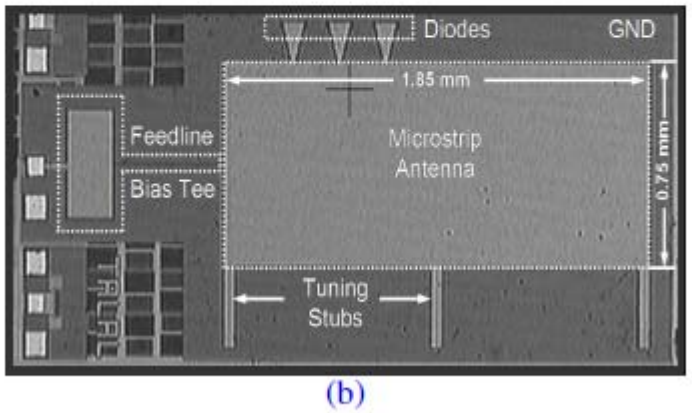


Fig. 4. Monolithic IMPATT transmitter in standard CMOS technology. (a) Layout of the integrated transmitter. (b) Die photo.

- Al-Attar, Talel; Hassibi, Arjang; Lee, Thomas
- Stanford University
- Standard 0.18 um CMOS @ 77 GHz
- Simulated Gain: -11 dBi
- Efficiency: 10% (simulated)
- Antenna size: 750 um x 1850 um

Al-Attar, T.; Hassibi, A.; Lee, T.H., "A 77GHz monolithic IMPATT transmitter in standard CMOS technology," *Microwave Symposium Digest, 2005 IEEE MTT-S International* , vol., no., pp. 4 pp.-, 12-17 June 2005.

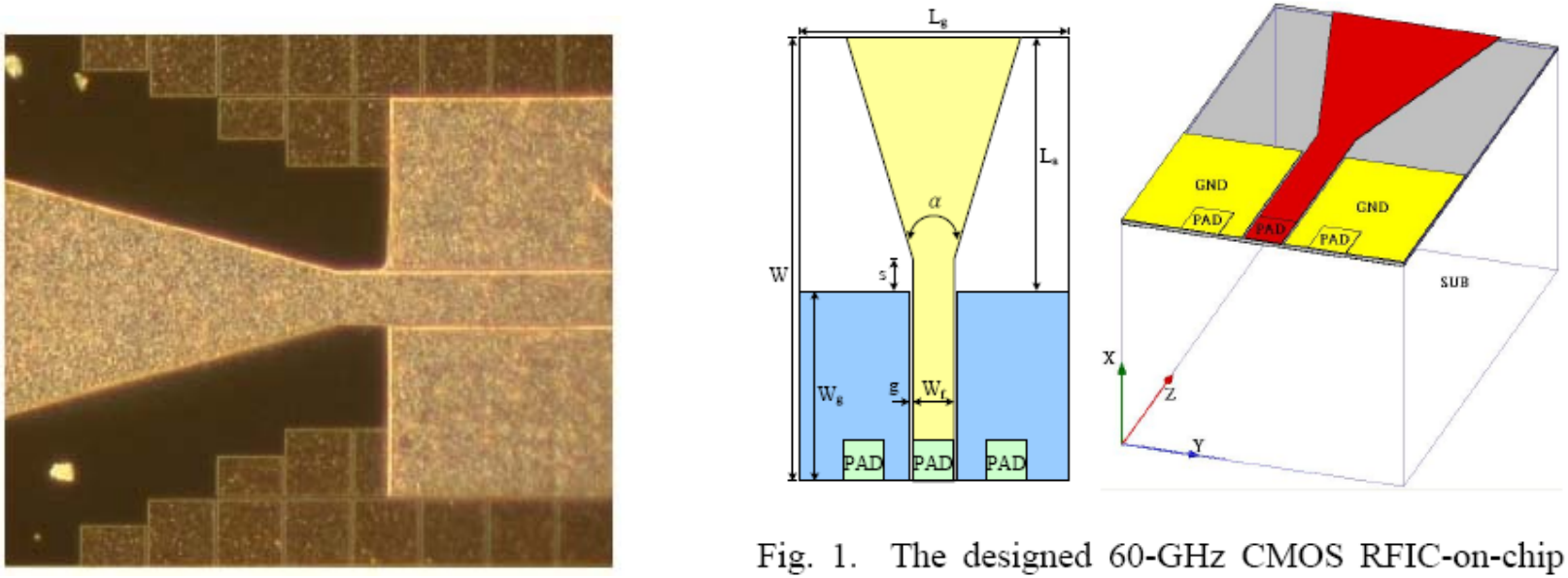


Fig. 1. The designed 60-GHz CMOS RFIC-on-chip triangular monopole antenna: (a) the geometry and (b) the HFSS simulation scheme.

- P.C. Kuo, S.S. Hsu, C.C. Lin, C.Y. Hsu, H.R. Chuang

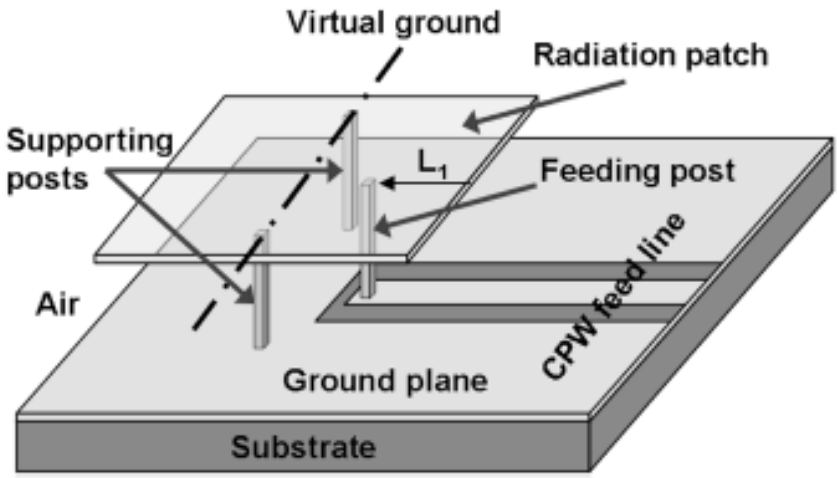
- National Cheng Kung University (2008)
- 0.18 um CMOS @ 60 GHz
- Gain: - 9.4 dBi

- Simulated Efficiency: 12%

- Chip size: 1.0 x 0.81 mm^2

Kuo, P.-C.; Hsu, S.-S.; Lin, C.-C.; Hsu, C.-Y.; Chuang, H.-R., "A 60-GHz Millimeter-Wave Triangular Monopole Antenna Fabricated Using 0.18-m m CMOS Technology," *Innovative Computing Information and Control, 2008. ICICIC '08. 3rd International Conference on* , vol., no., pp.237-237, 18-20 June 2008

Other Antennas at mmWaves



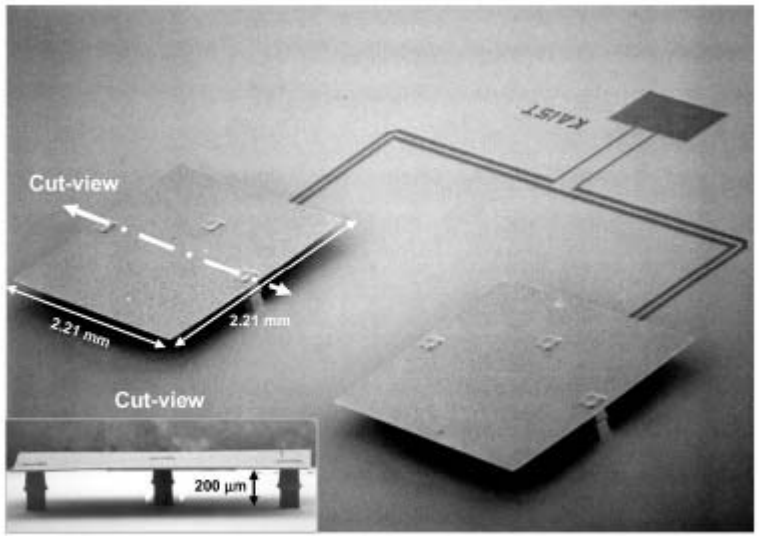


Fig. 3. Fabricated 2 × 1 patch array antenna.

- Jeong-Geun Kim; Hyung Suk Lee; Ho-Seon Lee; Jun-Bo Yoon; Hong, S.,
- Korean Advanced Institute of Science and Technology, Daejeon, Korea(2005)
- Small posts that were micro-machined to support the patch antenna
- Bandwidth: 4.6 GHz @ 60 GHz
- Gain: 8.7 dBi
- Efficiency: 96%
- Patch Size: 2.1 mm x 2.1 mm
- 2 x 1 array
  - Gain: 9.9 dBi
  - Efficiency: 94%

Jeong-Geun Kim; Hyung Suk Lee; Ho-Seon Lee; Jun-Bo Yoon; Hong, S., "60-GHz CPW-fed post-supported patch antenna using micromachining technology," *Microwave and Wireless Components Letters, IEEE* , vol.15, no.10, pp. 635-637, Oct. 2005.

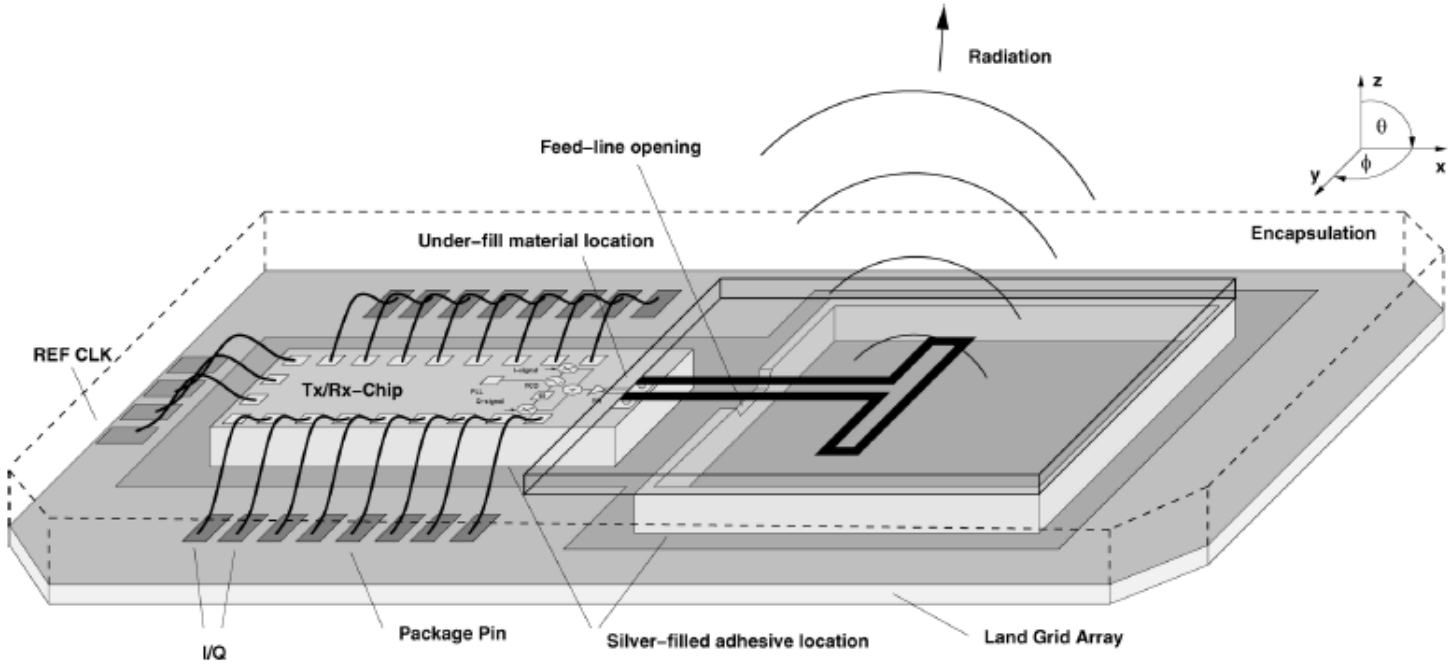


Fig. 3. Conceptional drawing for the buildup of the LGA. Standard wire bonding is used, except for the 60-GHz RF signal. A fused silica antenna is flipped to the chip providing the shortest possible interconnect. Silver-filled adhesive is used for chip and antenna attachment. An under-fill material is dispensed locally between the antenna substrate and the die surface, as indicated. The mold material in the antenna feed-line opening, as well as the package encapsulation material, are omitted for better clarity.

- Ullrich R. Pfeiffer, Janusz Grzyb, Duixian Liu, Brian Gaucher, et al.

- IBM T.J. Watson Research Center (2006)
- SiGe @ 60 GHz
- 7 mm x 11 mm encapsulation
- a metal cavity with a suspended folded dipole antenna
- Gain: 7 dBi gain , Efficiency: over 90%, 30% Bandwidth

Pfeiffer, U.R.; Grzyb, J.; Duixian Liu; Gaucher, B.; Beukema, T.; Floyd, B.A.; Reynolds, S.K., "A chip-scale packaging technology for 60-GHz wireless chipsets," *Microwave Theory and Techniques, IEEE Transactions on* , vol.54, no.8, pp.3387-3397, Aug. 2006.

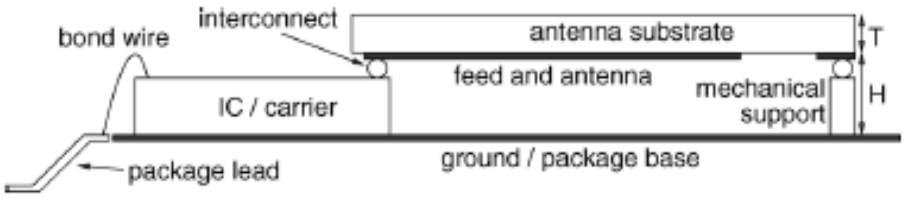


Fig. 1. Concept of antenna together with IC or carrier (side view, not to scale).

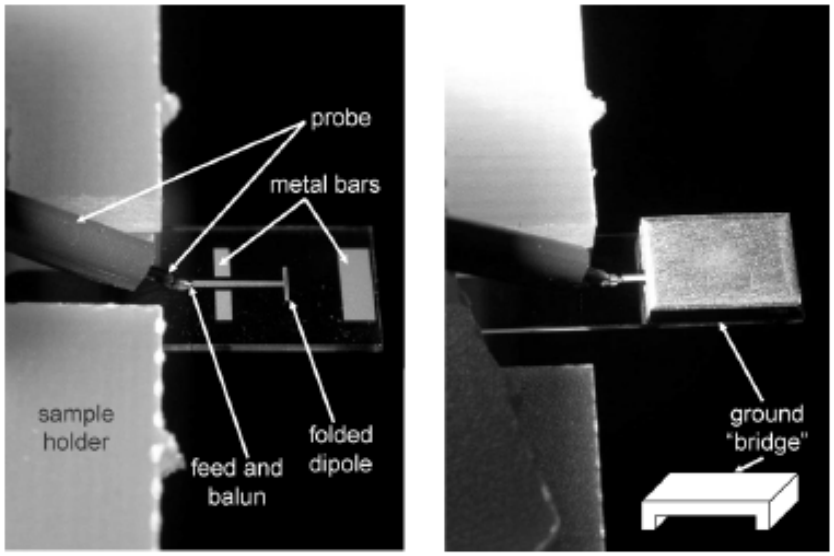


Fig. 4. Photograph of single-folded dipole in measurement setup (left side: without ground "bridge"; right side: with ground "bridge").

•Thomas Zwick*, Duixian Liu, and Brian P. Gaucher,*
• IBM T.J. Watson Research Center (2006)

• Broadband planar folded dipole where a superstrate of fused silica was used.
• SiGe @ 60 GHz
• Gain: 7-9 dBi gain , Efficiency: over 80%, 10% Bandwidth
•2.5 mm x 1.4 mm

Zwick, T.; Duixian Liu; Gaucher, B.P., "Broadband Planar Superstrate Antenna for Integrated Millimeterwave Transceivers," *Antennas and Propagation, IEEE Transactions on* , vol.54, no.10, pp.2790-2796, Oct. 2006

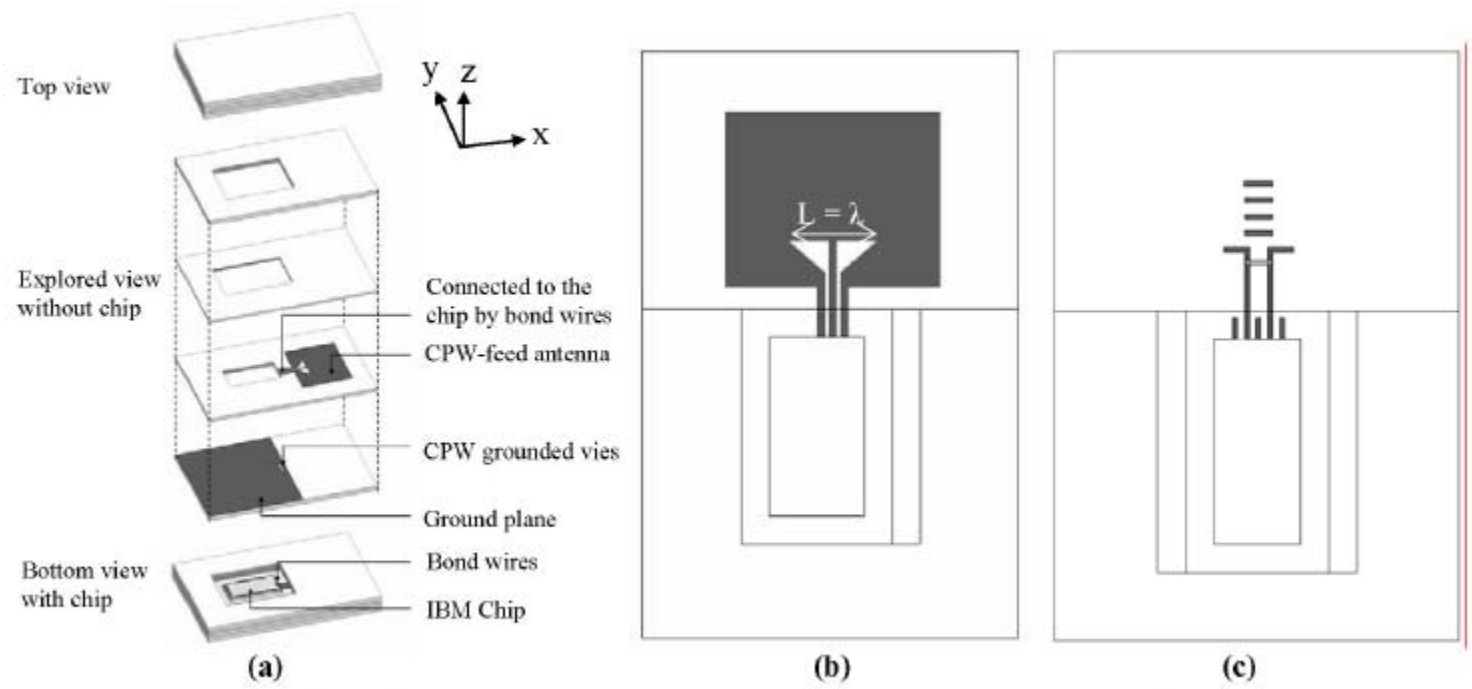


Fig. 1 60-GHz AiPs: (a) WB-triangle 3D view, (b) WB-triangle layout, and (c) Yagi layout.

- Antenna-in-Package in LTCC
- Nanyang Technological University, Singapore (2007)
- 60 GHz LTCC package: 12.5 mm x 8 mm
- WB-Triangle Gain: 5.1 – 7 dBi
- Yagi Gain: no result
- Efficiency: 93%

Zhang, Y.P.; Sun, M.; Chua, K.M.; Wai, L.L.; Liu, D.; Gaucher, B.P., "Antenna-in-Package in LTCC for 60-GHz Radio," *Antenna Technology: Small and Smart Antennas Metamaterials and Applications, 2007. IWAT '07. International Workshop on* , vol., no., pp.279-282, 21-23 March 2007

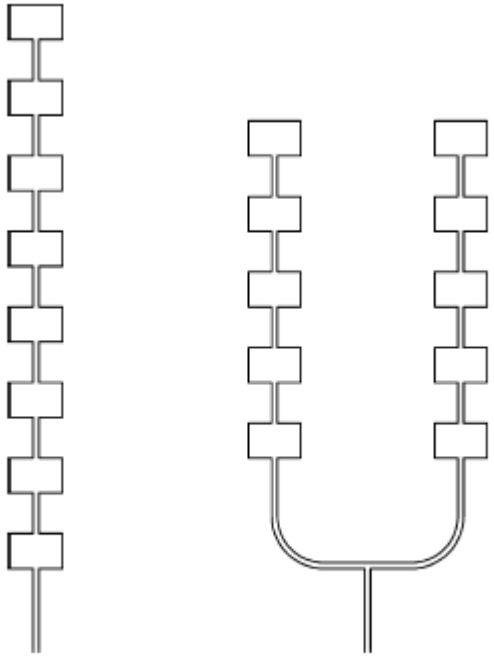


Fig. 6. Etched patterns for the two designed antenna arrays. (*left*) Single array and (*right*) double array for equal beamwidths in both planes.

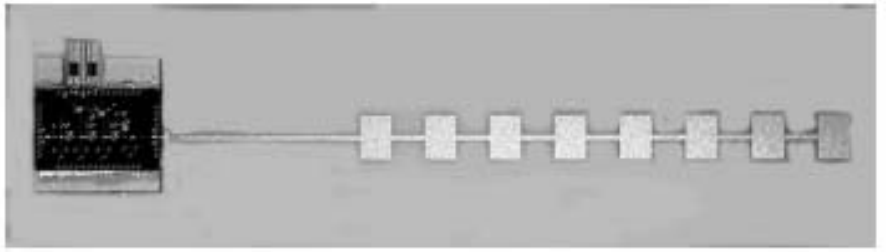


Fig. 16. Integrated design with single array antenna.

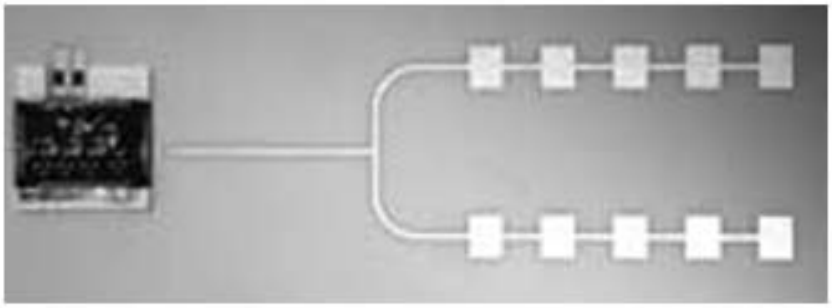


Fig. 17. Integrated design with double array antenna.

- Camilla Kärnfelt, Paul Hallbjörner, Herbert Zirath, and Arne Alping

- Chalmers University of Technology, Göteborg, Sweden (2006)
- 60 GHz high gain active microstrip antenna array (8-10 antennas)
- Alumina substrate
- Array Gain: 12-13 dBi, Array Size: 5mm x 10mm

Karnfelt, C.; Hallbjorner, P.; Zirath, H.; Alping, A., "High gain active microstrip antenna for 60-GHz WLAN/WPAN applications," *Microwave Theory and Techniques, IEEE Transactions on* , vol.54, no.6, pp.2593-2603, June 2006.

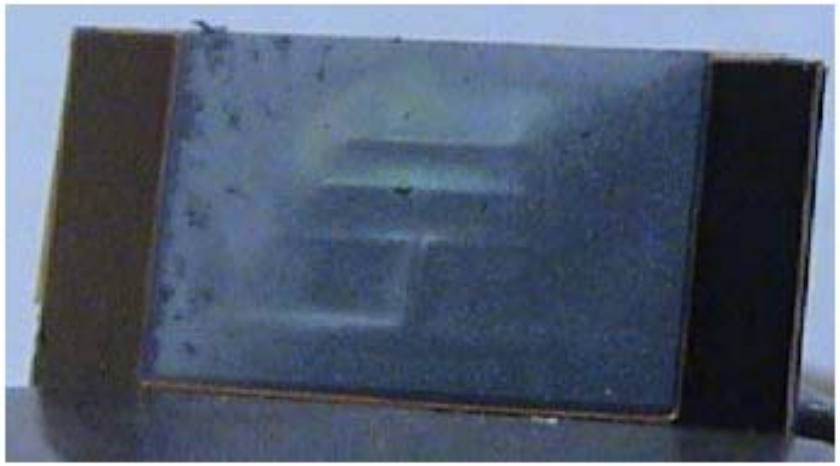


Figure 3. Backside photo of the fabricated 60 GHz Yagi-Uda antenna structure

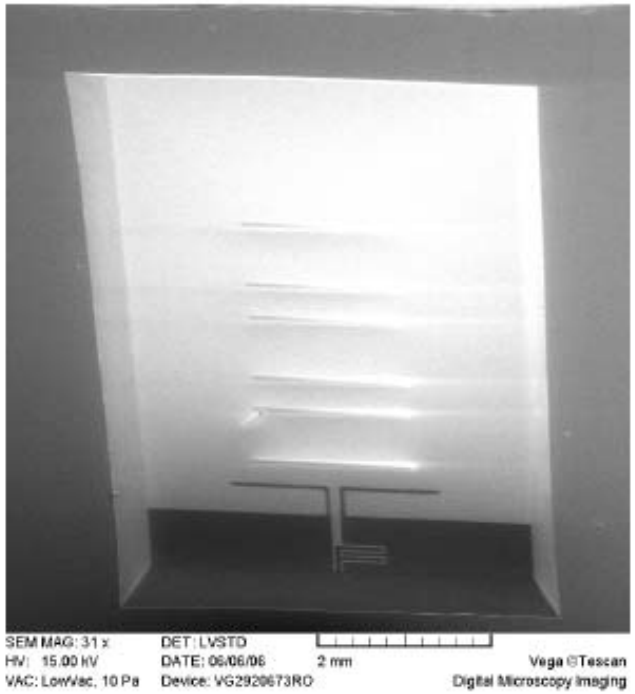


Figure 5. SEM photo of the backside of the 77 GHz Yagi-Uda antenna structure

- D. Neculoiu, G. Konstantinidis, L. Bary, A. Muller, D. Vasilache, A. Stavinidris, P. Pons, R. Plana
- IMT Bucharest, Romania, *MRG-IESL-FORTH Heraklion, Greece* (2006)
- 60 and 77 GHz membrane-supported Yagi antenna on semi-insulating GaAs substrate
- 2 mm x 3.1 mm
- Gain: 7-11 dBi

Neculoiu, D.; Konstantinidis, G.; Bary, L.; Muller, A.; Vasilache, D.; Stavinidris, A.; Pons, P.; Plana, R., "Membrane-supported Yagi-Uda MM-Wave antennas," *Antennas and Propagation, 2006. EuCAP 2006. First European Conference on* , vol., no., pp.1-5, 6-10 Nov. 2006.

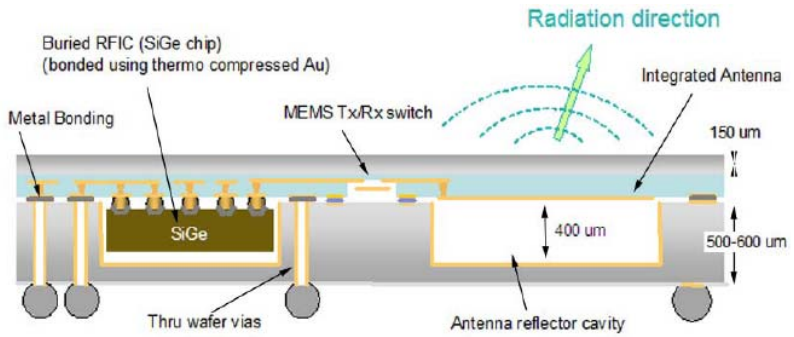


Fig. 1. Schematic of an all Si-based low-cost package for 60GHz transceiver. The package might incorporate RF passives such as resistors, inductors, MEMS switches and antennas. (Note: drawing not to scale)

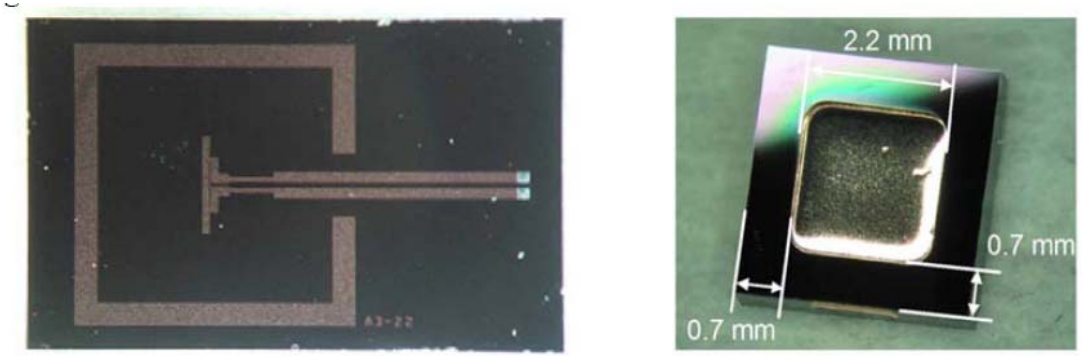


Fig. 2. Photograph of antenna (left) and cavity (right). The antenna is fabricated using a 1.2 μm Cu damascene process. The cavity is 400 μm deep and metallized with a 8 μm thick Cu layer.

- N. Hoivik, D. Liu, C. V. Jahnes, J. M. Cotte, et al.

- Antenna with micromachining techniques
- Use of cavity

- IBM T.J. Watson Research Center (2007)

- 2.2 mm x 2.2 mm
- Gain: 4-8 dBi
- Efficiency: >90% assumed

Hoivik, N.; Liu, D.; Jahnes, C.V.; Cotte, J.M.; Tsang, C.; Patel, C.; Pfeiffer, U.; Grzyb, J.; Knickerbocker, J.; Magerlein, J.H.; Gaucher, B., "High-efficiency 60 GHZ antenna fabricated using low-cost silicon micromachining techniques," *Antennas and Propagation Society International Symposium, 2007 IEEE* , vol., no., pp.5043-5046, 9-15 June 2007

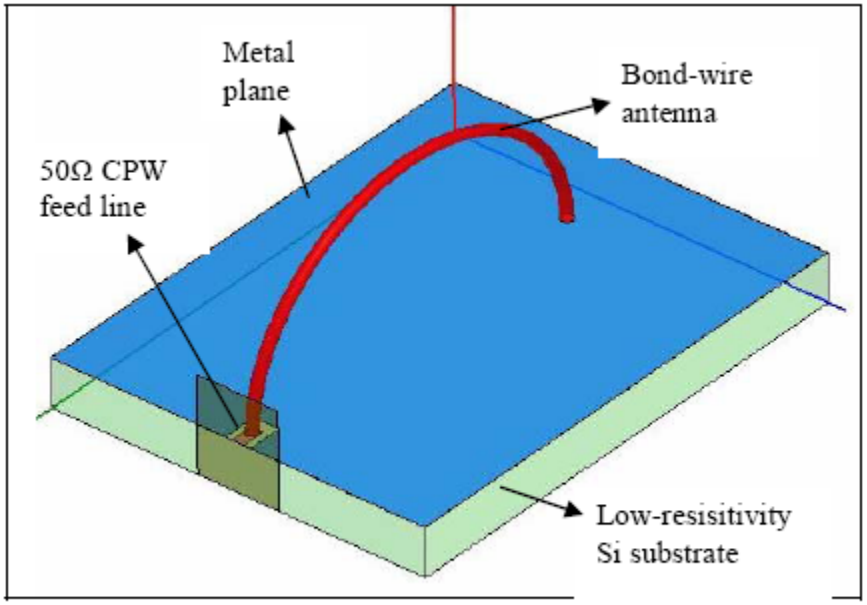


Fig. 2. Simulation setup of a bond-wire antenna.

- N. Varanasi, B. Jung, D. Peroulis
- Purdue University (2008)
- 30 GHz
- Gain: 0.22 dBi
- Efficiency 74%
- Low resistive silicon substrate

Varanasi, N.; Byunghoo Jung; Peroulis, D., "On-chip bond-wire antennas on CMOS-grade silicon substrates," *Antennas and Propagation Society International Symposium, 2008. AP-S 2008. IEEE* , vol., no., pp.1-4, 5-11 July 2008

Metamaterials

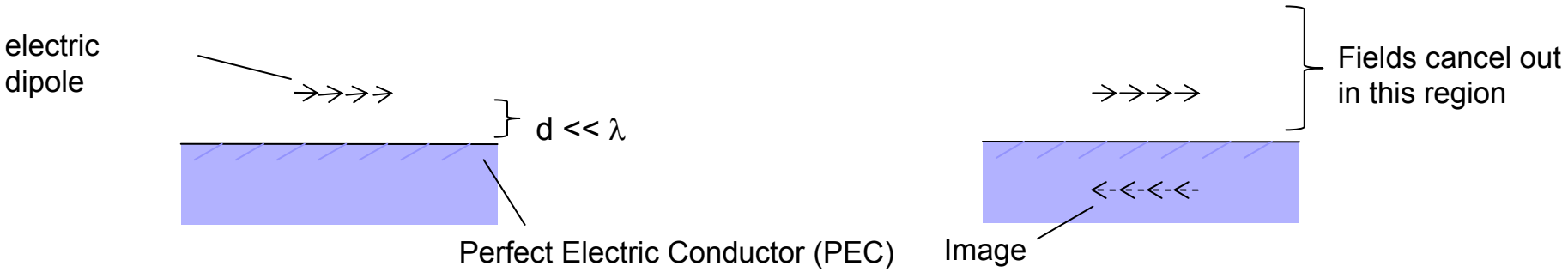
- Greek word “meta” which means “beyond”
- Adjust the relative permittivity and the relative permeability of materials

- create a type of metamaterial that mimics a magnetic conductor
    - only for a certain range of frequencies

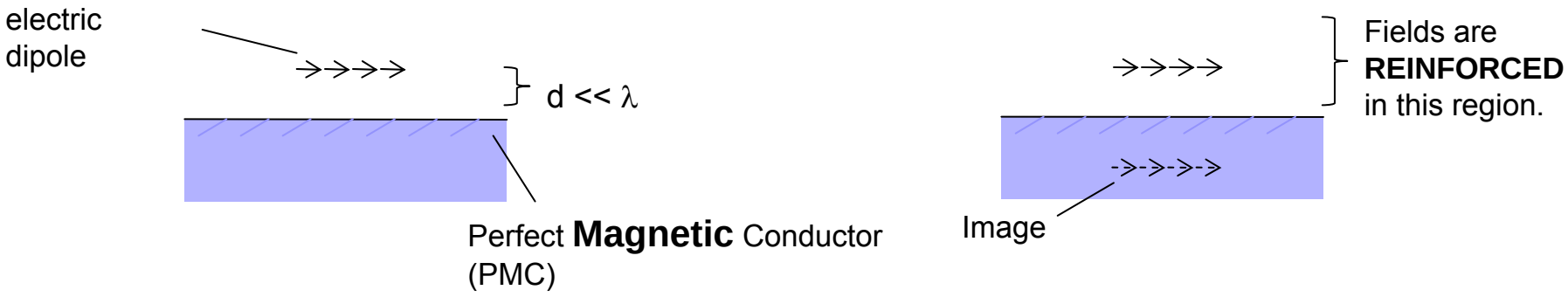
- denoted as “Frequency Selective Surface”

Metamaterials

- Problem:
  - Electric dipole “short circuits” over ground plane (electric conductor)
  - Fields reflect with 180° degree phase shift
  - Radiated and reflected fields destructively interfere



Frequency Selective Surfaces



- Frequency Selective Surface – creates a **magnetic** conductor
- FSS produce 0° phase shift over a narrow band of frequencies
- Wide-open research field, many applications for mmWave RFICs

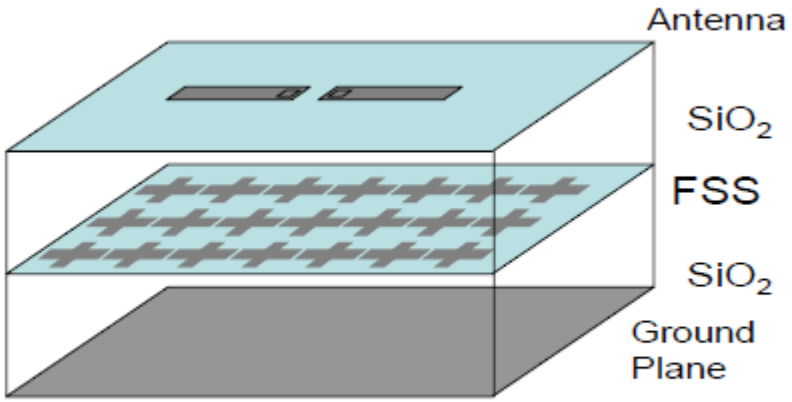


Fig. 1. On-chip antenna mounted over a FSS

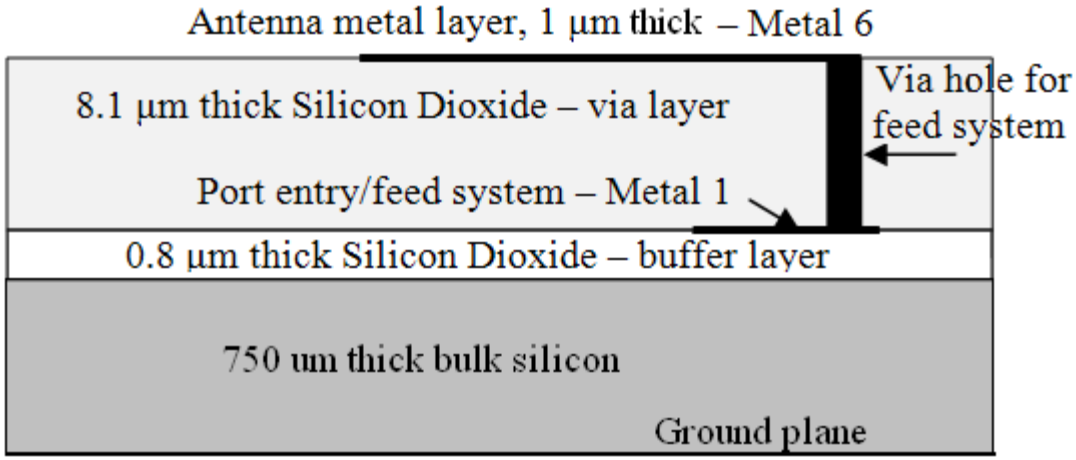
- Lawrence Ragan, Arjang Hassibi, Theodore S. Rappaport, Craig L. Christianson, VTC 2007 proposed this concept
- UT-Austin (2007)
- Create FSS using very small, planar, periodic dipoles/loops in desired material
- IC fabrication can create small dipole/loops easily in any of the metal layers

Ragan, L.; Hassibi, A.; Rappaport, T.S.; Christianson, C.L., "Novel On-Chip Antenna Structures and Frequency Selective Surface (FSS) Approaches for Millimeter Wave Devices," *Vehicular Technology Conference, 2007. VTC-2007 Fall. 2007 IEEE 66th* , vol., no., pp.2051-2055, Sept. 30 2007-Oct. 3 2007

Application of HF Antennas at 60 GHz

- Scale HF Antennas to 60 GHz
  - Half-wave dipole, Yagi, Rhombic, Loop
- Investigation of performance on-chip
  - How performance is a function of on-chip position
  - Design guidelines for IC antennas compared to HF antennas
  - Optimized antennas to maximize gain and direction of radiation

HFSS Simulation Model

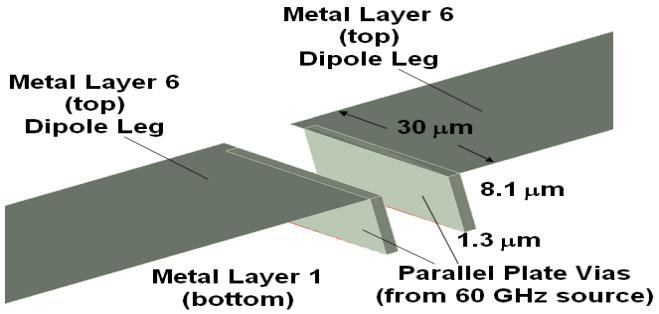


$$\lambda_{eff} = \frac{1}{\sqrt{\epsilon\mu}f} = \frac{1}{\sqrt{\epsilon_0\epsilon_r\mu_0}f} = \frac{\lambda_{freespace}}{\sqrt{\epsilon_r}}$$

$\lambda_{effective}$ = 2.53 mm

5 mm x 5 mm standard 0.18μm CMOS substrate

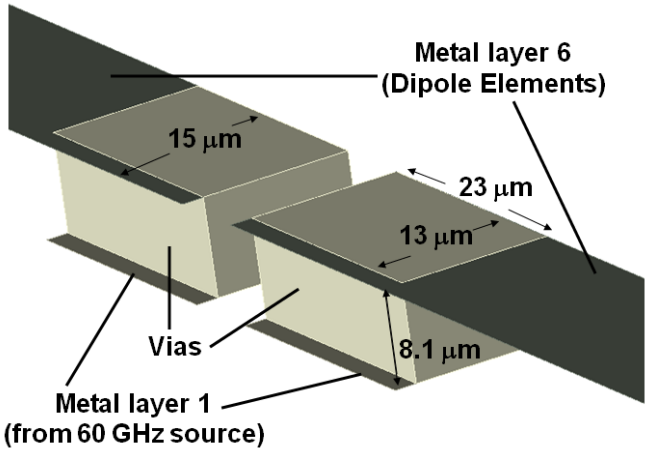
Feed Systems for 50Ω Matching



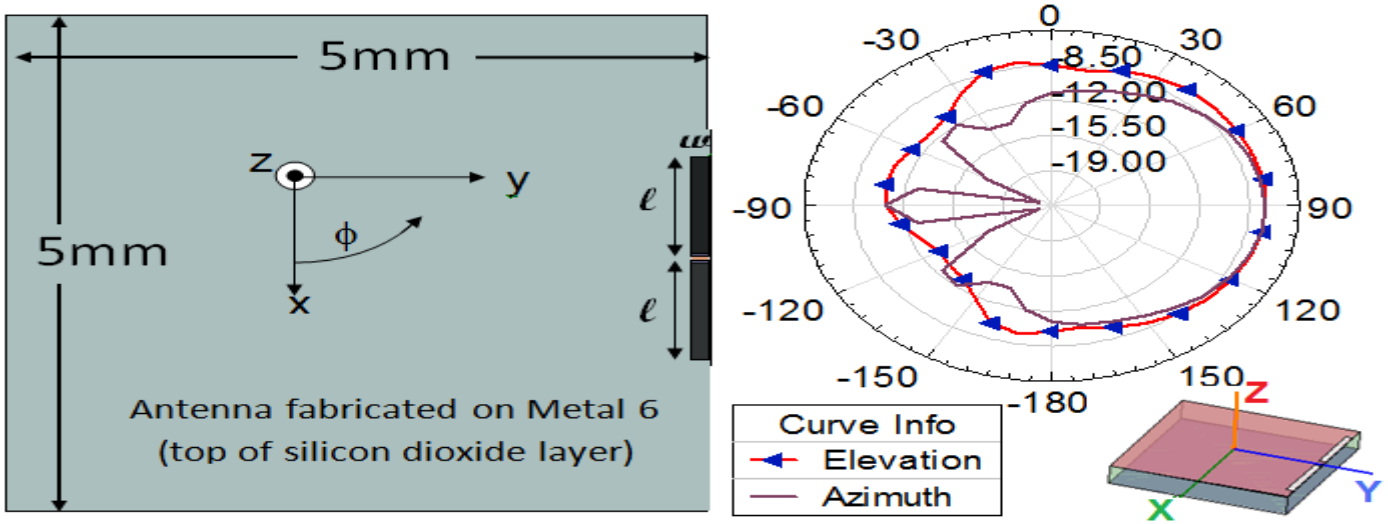
Dipole feed

$$Z_o = \eta \frac{b}{w}$$

Yagi feed

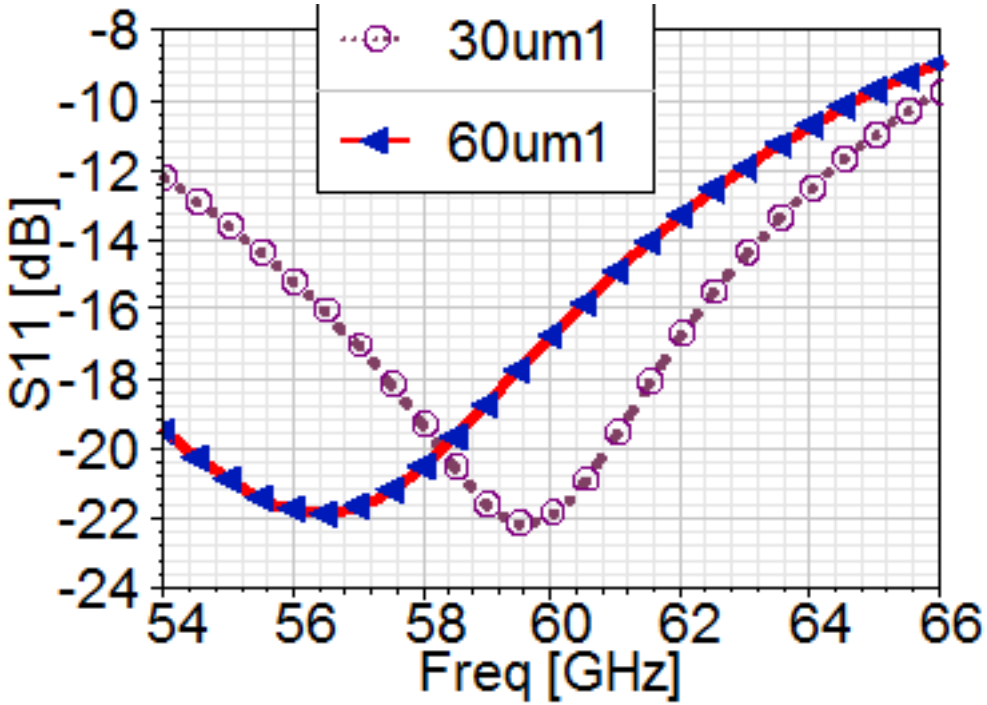


Optimized Dipole Antenna



Dipole Experiments

- Impedance matching changed by altering element thickness



Dipole Experiments

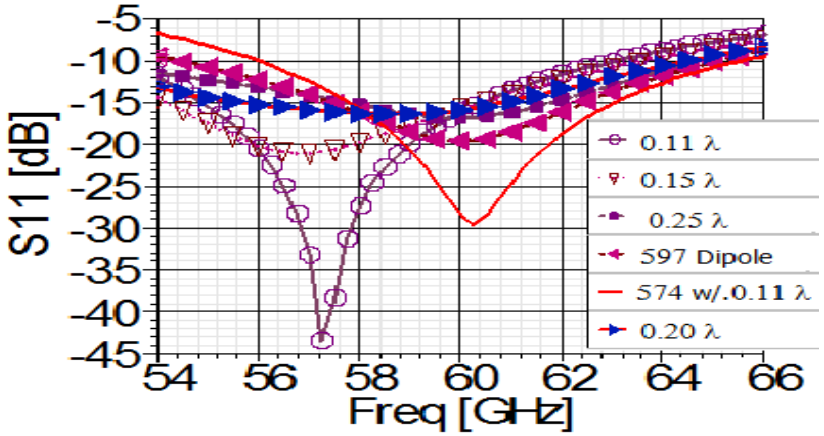
- Length and thickness adjusted for resonance
  - 570 μm length, 30 μm width for impedance match
- Position of antenna
  - Centered on chip: -13.6 dBi
  - Edge-mounted: -7.3 dBi
- Width increased to 60 μm
  - Edge-mounted gain now -6.7 dBi

Optimized Yagi

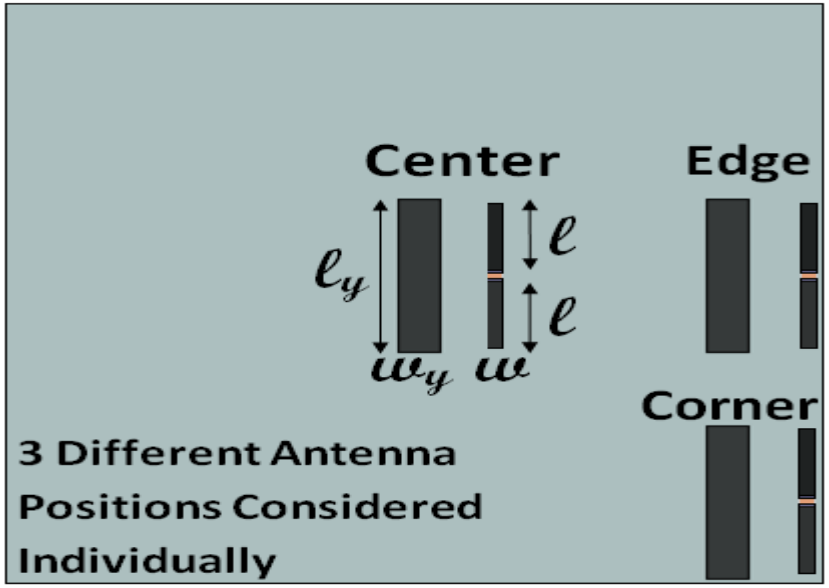
- Gain is a function of on-chip position
  - Along the right corner of the chip
    - -3.55 dBi gain
    - Front-to-back ratio of 10.4 dB
    - Maximum intensity 20° above the horizon
    - Efficiency of 15.8%
    - 7.65 dB better than if centered on chip

Yagi Experiments

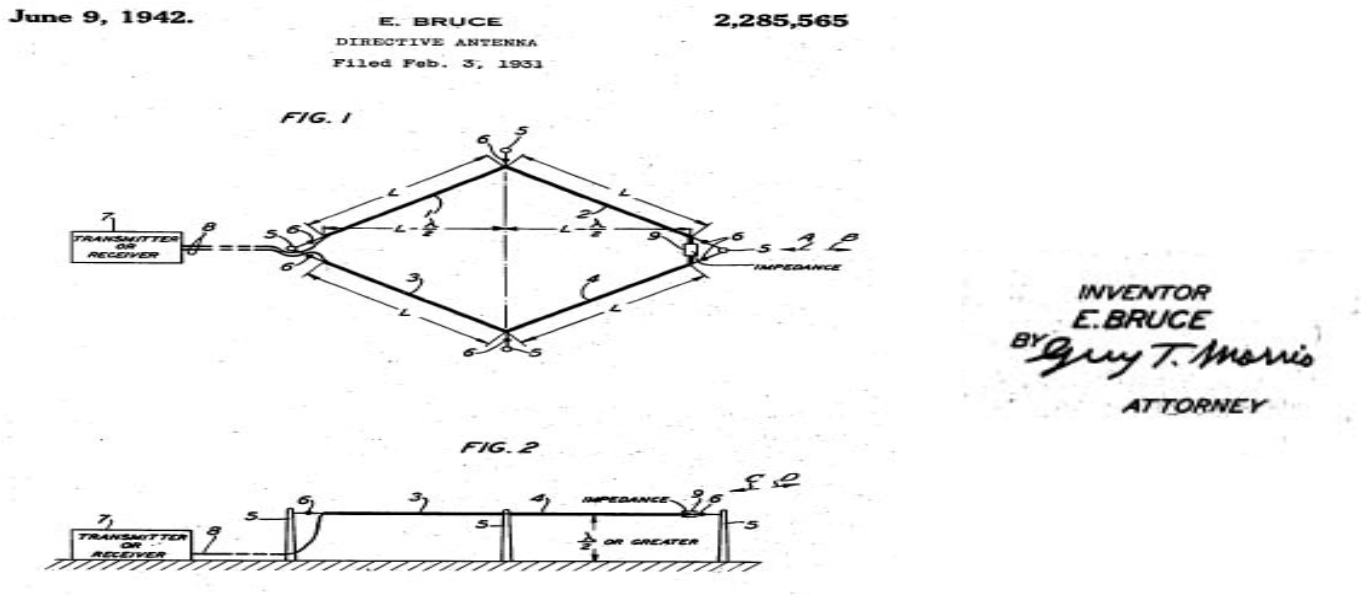
- S11 as a function of spacing between reflecting and driving elements



Yagi Experiments



HF Rhombic Antenna



June 9, 1942. E. BRUCE 2,285,565

DIRECTIVE ANTENNA

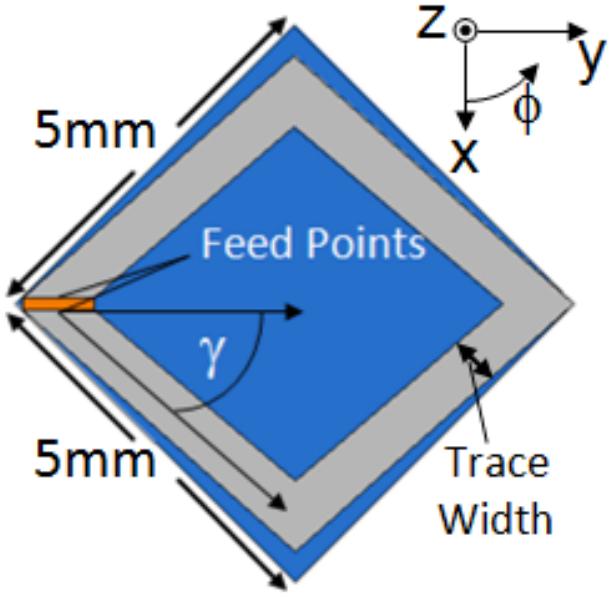
Filed Feb. 3, 1931

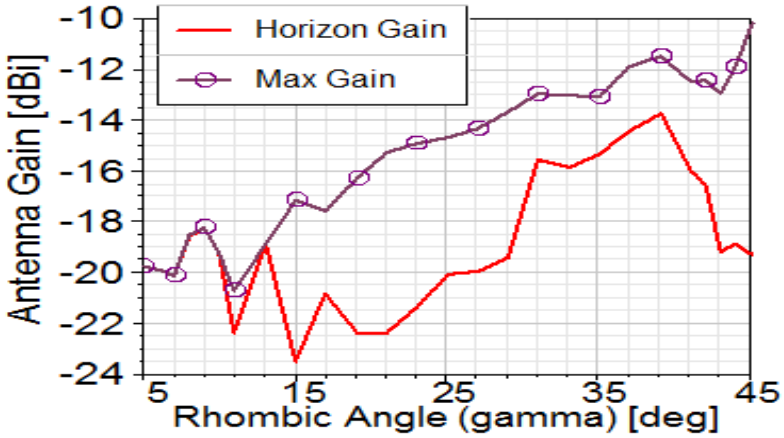
FIG. 1

INVENTOR
E. BRUCE
BY Guy T. Morris
ATTORNEY

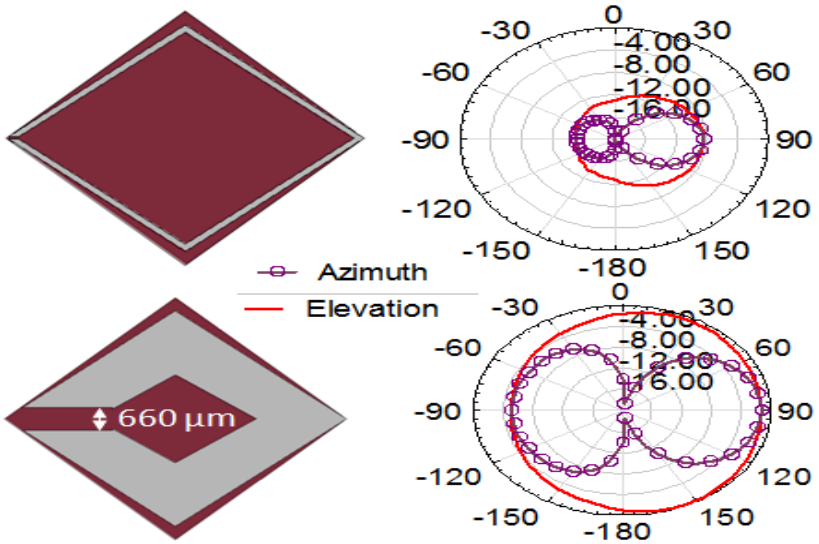
FIG. 2

Rhombic Antenna





Rhombic Antenna



- Simulated to find optimal angle, substrate thickness
- Thin antenna
  - 200 µm width
  - -8 dBi horizontal gain
- Thick antenna
  - 1.445 mm width
  - 0 dBi horizontal gain

Summary of Results

Antenna	Max Gain	Horizontal Gain	∠ of Max Gain*	Efficiency	F/B	Approximate Area
Antennas developed in this paper						
Dipole	-7.3 dBi	-7.3 dBi	0°	9%	3 dB	0.13 mm^2
Yagi	-3.55 dBi	-3.8 dBi	20°	15.8%	10.4 dB	0.9 mm^2 (including spacing)
Rhombic	-0.2 dBi	-1.27 dBi	39°	85%	3.7 dB	3.5 mm^2 (metal only)
Past works						
Quasi-Yagi	-12.5 dBi			5.6%	"Poor"	
Inverted F	-19 dBi			3.5%		
CPW-Fed Yagi	-10 dBi			10%	9 dB	
Triangle	-9.4 dBi			12%		

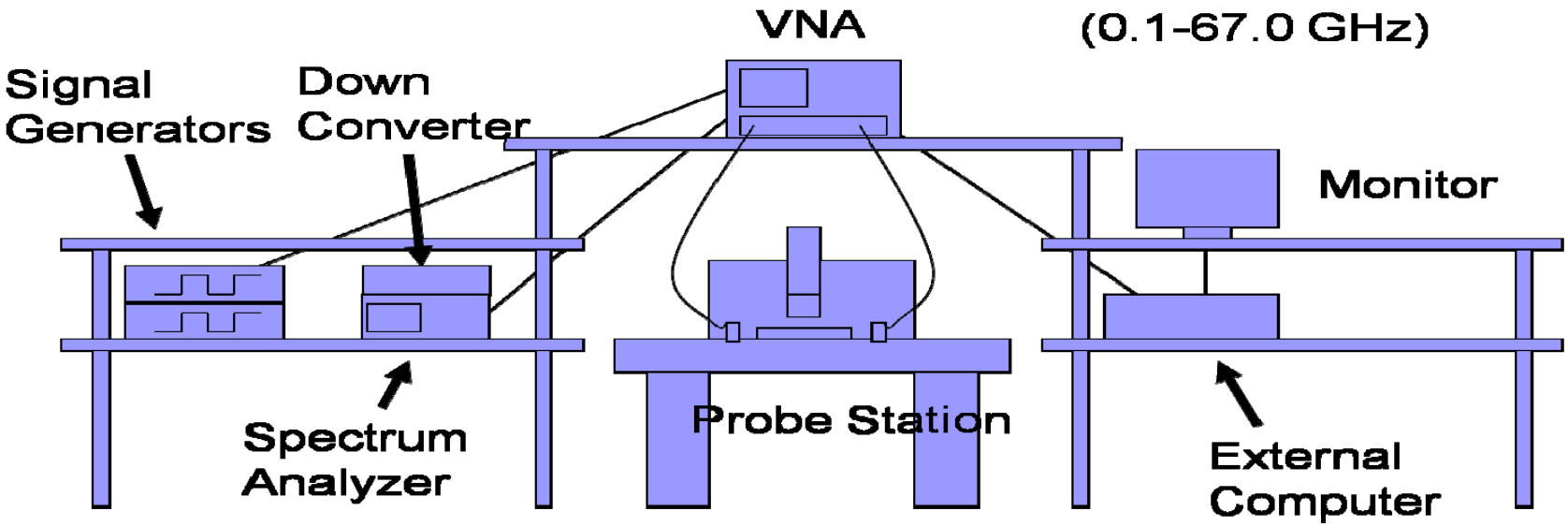
•Y. Zhang, M. Sun, and L. Guo, "On-chip antennas for 60-GHz radios in silicon technology," IEEE Trans. on Electron Devices, vol. 52, no. 7, pp. 1664–1668, July 2005.

•S.-S. Hsu, K.-C. Wei, C.-Y. Hsu, and H. Ru-Chuang, "A 60-GHz Millimeter-Wave CPW-Fed Yagi Antenna Fabricated by Using 0.18m CMOS Technology," IEEE Electron Device Letters, vol. 29, no. 6, pp. 625–627, June 2008.

•C.-C. Lin, S.-S. Hsu, C.-Y. Hsu, and H.-R. Chuang, "A 60-GHz millimeter-wave CMOS RFIC-on-chip triangular Monopole Antenna for WPAN applications," IEEE Antennas and Propagation Society International Symposium, 2007, pp. 2522–2525, June 2007.

*above horizon

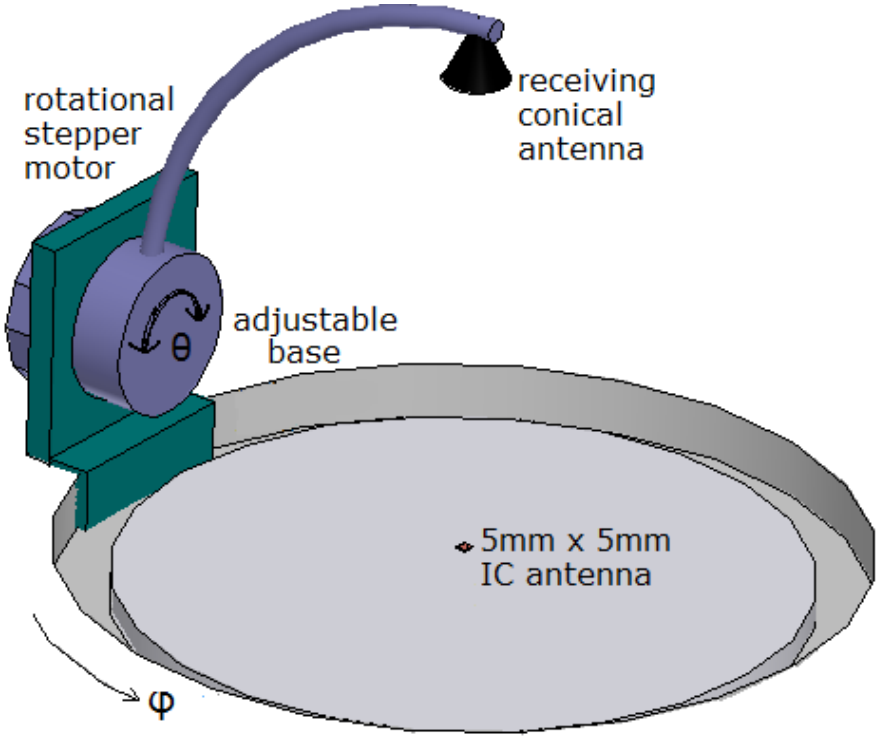
Antenna Measurement



Research Work for Gbps Era

Antenna Pattern Measurements

- Confirm antenna simulations
- Testing and validating RFICs and switched arrays
- Measuring EMI
  - Near field and far field measurements
- Validating effects of packaging materials
- Automated for ease of use and quick, comparative results



60 GHz Standards

- IEEE 802.15.3C (Sept./Oct. 2009)
  - Cordless interconnection
- ECMA TC48 (ECMA 387 Summer 2009)
  - PHY, MAC, PAL for WLAN
- Wireless HD/HDMI (est. Nov. 2009)
  - Cordless interconnection/ HD video
- WiGig (est. 2009/2010)
  - Networking/ multi-device connection
- IEEE 802.11 VHT (est. 2011/2012)
  - Wireless LAN future vision

IEEE 802.15.3C

•Sponsor ballot approved by RevCom in **September 2009**
•4 RF Channels
•Maximum Data Rate: at least 2Gb/s (3Gb/s optional)
•Maximum Coverage: ~20 m
•Mode 1: OFDM for data rates of more than 3Gb/s
•Mode 2: SC for data rate of 1-2Gb/s

Five usage models (UMs) have been generated that define 60 GHz WPAN applications and environments:

•**UM1** Single set uncompressed video streaming
•**UM2** Multi set uncompressed video streaming
•**UM3** Office desktop data transfer
•**UM4** Conference ad hoc data transfer
•**UM5** Kiosk file-downloading

WiGig

Wireless Gigabit Alliance

- All products will be capable of at least 1 Gbps at a typical range of 10 m
- Some implementations will be capable of speeds more than 6 Gbps at great distances
- Ratify by 2009, Compliance testing in 2010

Atheros Communications, Inc.
Broadcom Corporation
Dell, Inc.
Intel Corporation
LG Electronics Inc.
Marvell International LTD.
MediaTek Inc.
Microsoft Corporation
NEC Corporation
Nokia Corporation
Panasonic Corporation
Samsung Electronics Co.
Wilocity

Wireless Gigabit Alliance website, http://wirelessgigabitalliance.org, accessed June 2, 2009.

WirelessHD

•Promote a cable-free form of HDMI

•Will use the IEEE 802.15.3c physical layer as the basis for its upper-layer protocols

•Over a distance of up to 10m, transmit full uncompressed 1080p video and audio

•Bandwidth ~3Gb/s.

Broadcom Corporation	NEC Corporation
Intel Corporation	Samsung Electronics, Co., LTD
LG Electronics Inc.	SiBEAM, Inc.
Panasonic Corporation	Sony Corporation
Philips Electronics	Toshiba Corporation

Araki, Lucas. "60 Ghz Communication." PowerPoint presentation.

IEEE 802.11 VHT

•Expected Date of Submission for Initial Sponsor Ballot: Dec. 2011

•Projected Completion Date for Submittal to RevCom: Dec. 2012

•Enables a maximum throughput of at least 1 Gbps

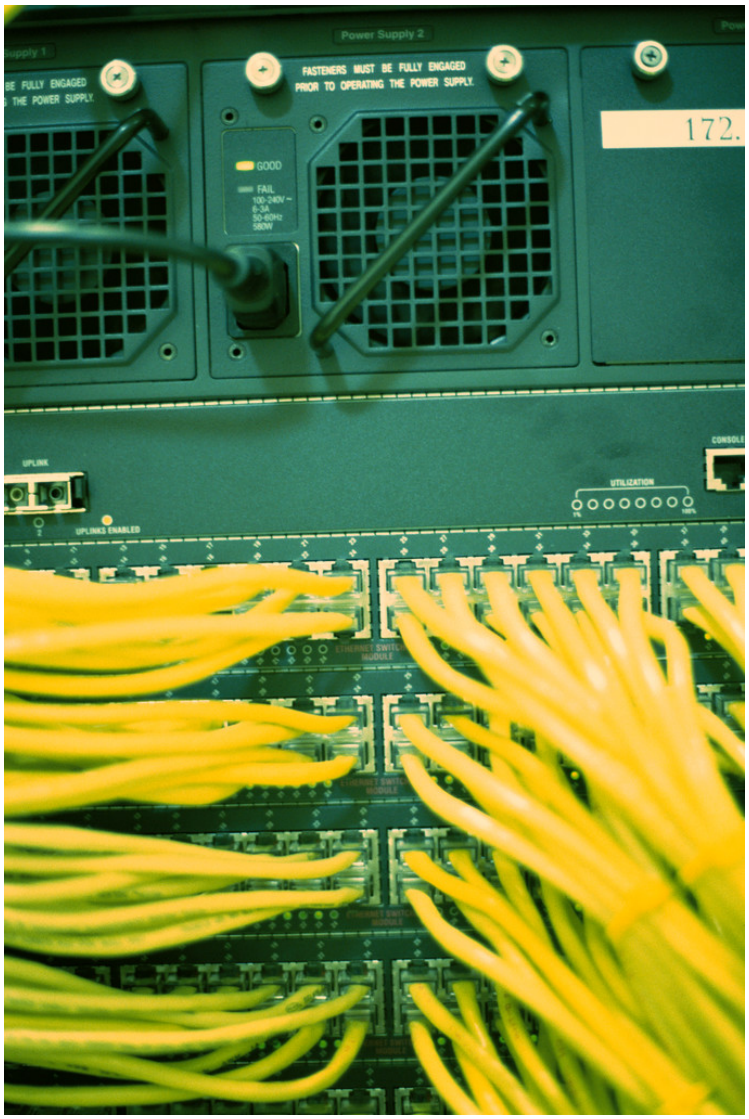
•Enables fast session transfer between PHYs

•Maintains the 802.11 user experience

•Provides mechanisms that enable coexistence with other systems in the band including IEEE 802.15.3c systems

•Dependent on 802.11n (MIMO)

Araki, Lucas. "60 Ghz Communication." PowerPoint presentation.



- Gigabit Ethernet popular choice to interconnect servers
- 60 GHz Wireless will replace Gigabit Ethernet interconnects
- Also monitors server health and ambient conditions (temperature, humidity, etc.)
- Data backup with fast transfers and mobility, new physical architectures
- PCs and Servers replace magnetic harddrives with RF post-it notes

Final Thoughts

- The edge will continue to become wireless, obviating print and magnetic media, wired connections, in revolutionary ways
- Rich research field for low power MAC with DF/beam switching, on-chip antennas, RF interconnects, networking, and applications
- It took us 30 years to go one decade in frequency (450 MHz to 5.8 GHz), yet we will advance another decade within 5 years (5.8 GHz to 60 GHz). By 2020, we will have devices well above 100 GHz and 20 Gbps.
- Academia and Industry will need to prototype RF systems using silicon fabrication at 60GHz + to avoid expensive interconnects, determine true power consumption, and to conduct in-situ measurements