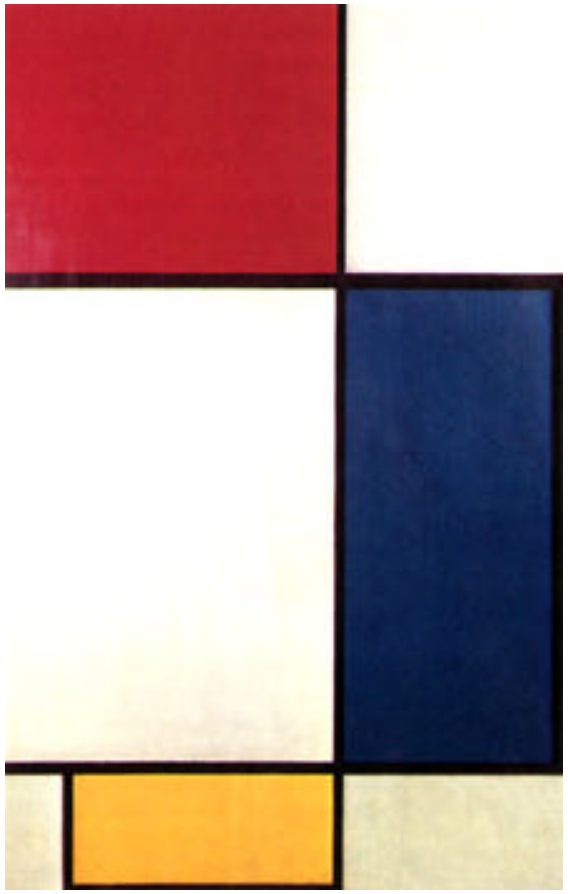
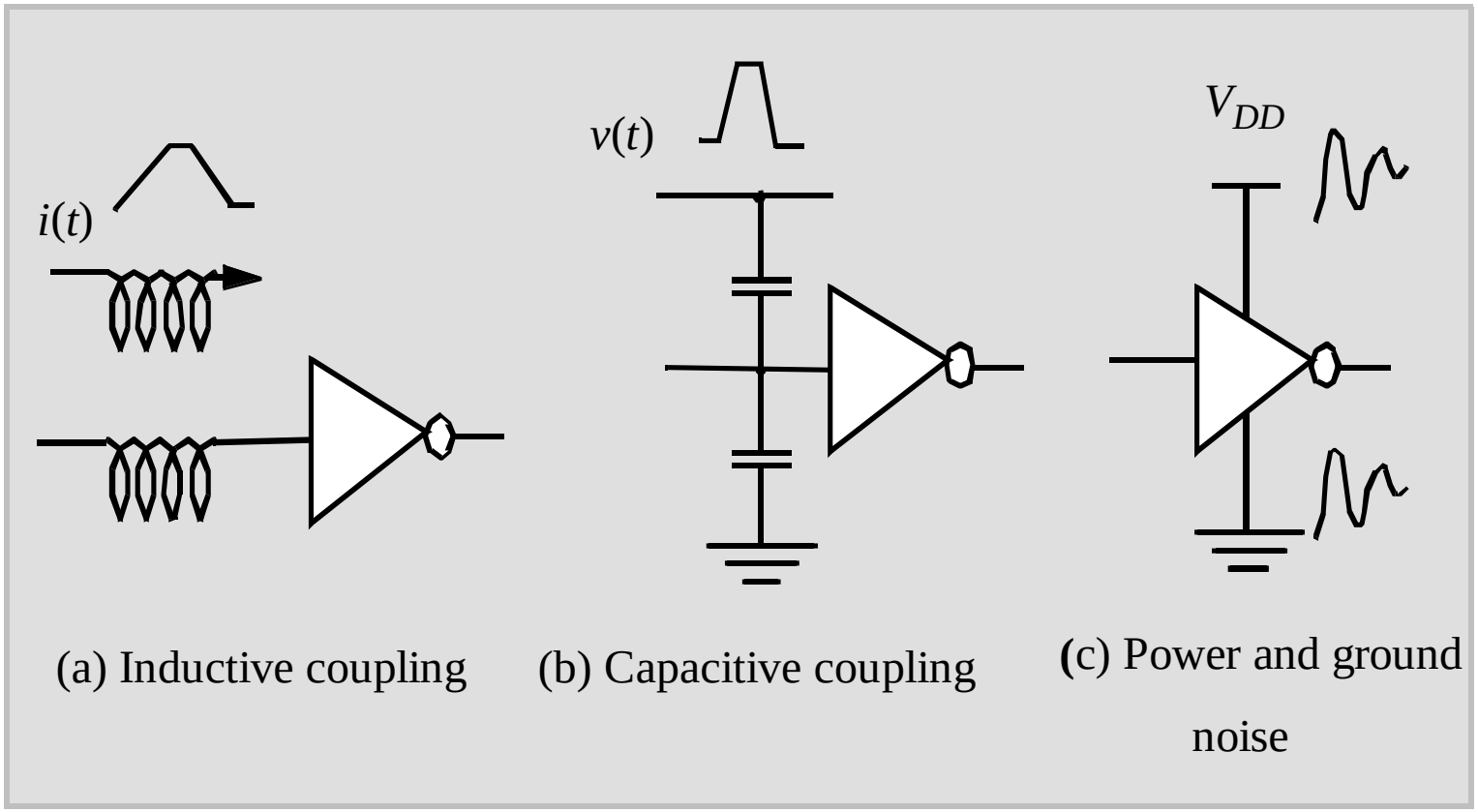
THE INVERTERS



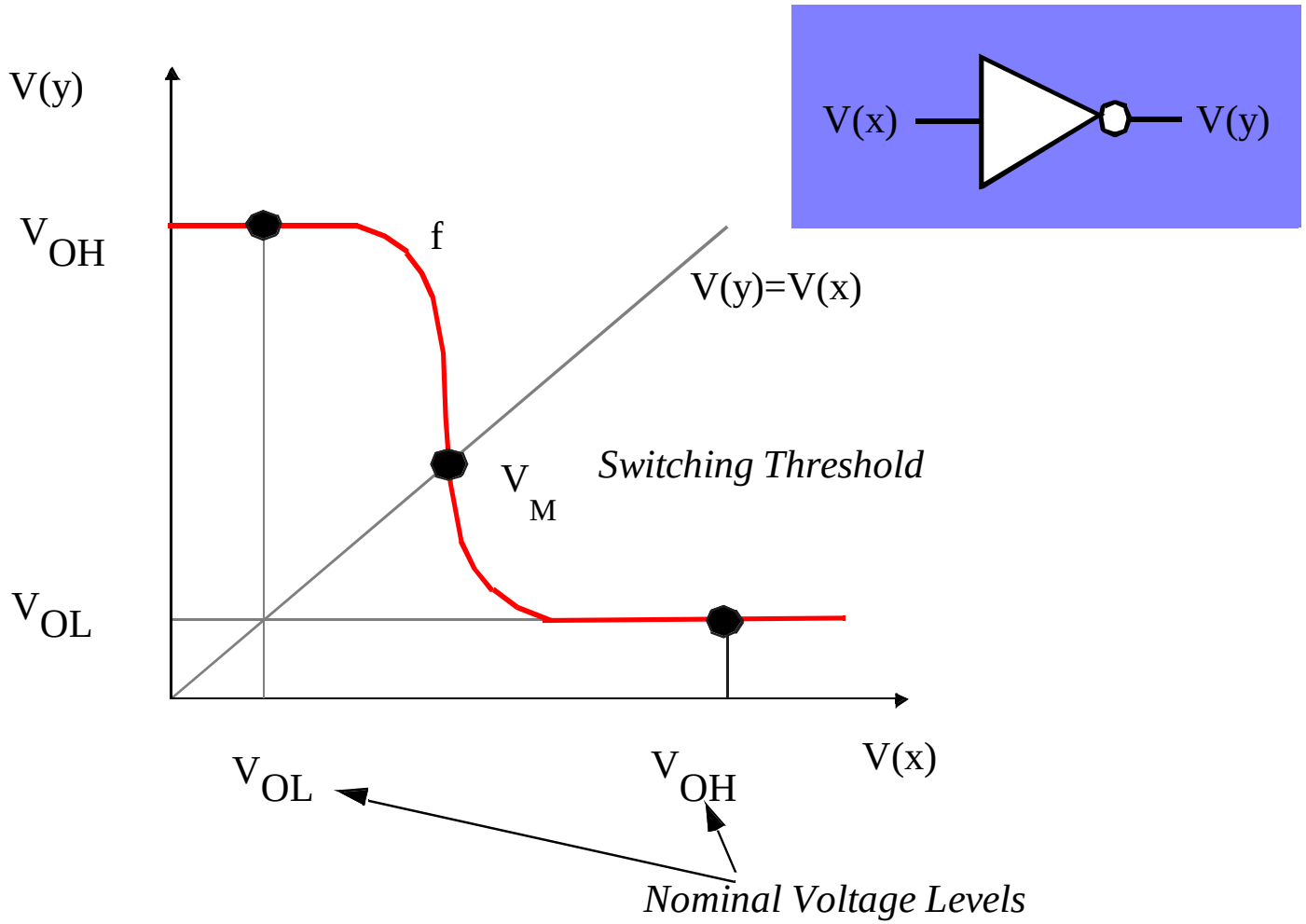
DIGITAL GATES
Fundamental Parameters

- Functionality
- Reliability, Robustness
- Area
- Performance
  - » Speed (delay)
  - » Power Consumption
  - » Energy

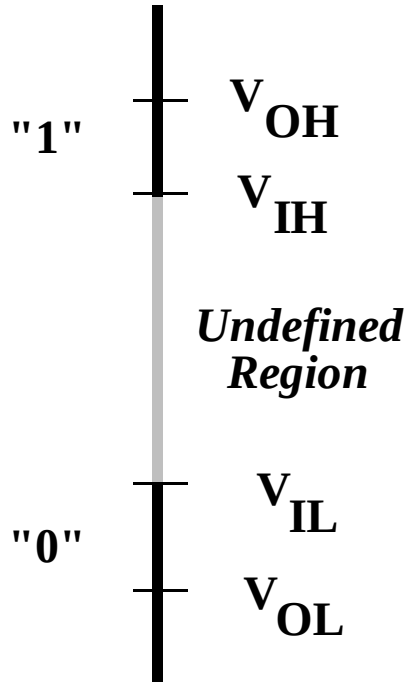
Noise in Digital Integrated Circuits

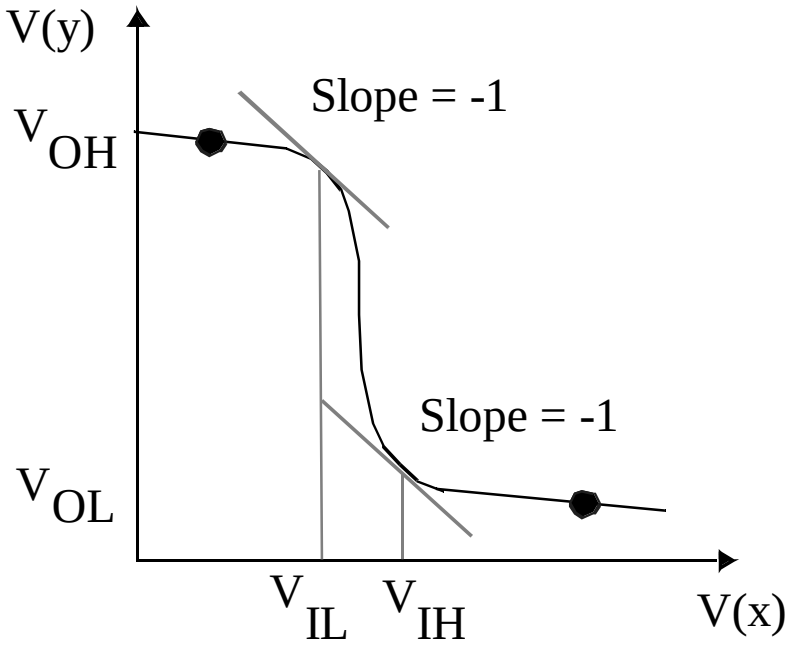


DC Operation: Voltage Transfer Characteristic

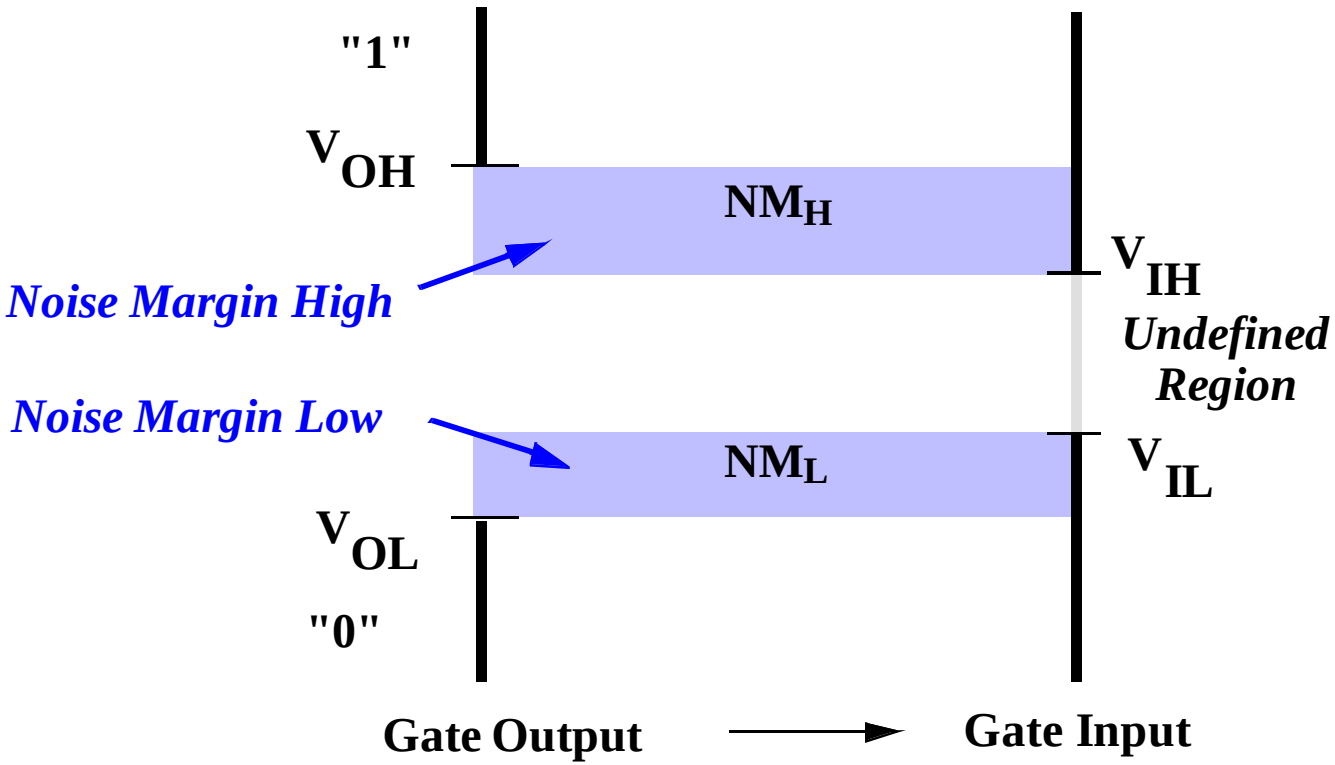


Mapping between analog and digital signals

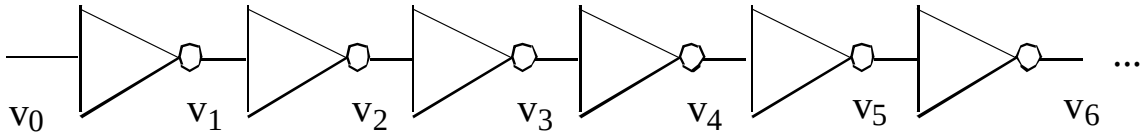




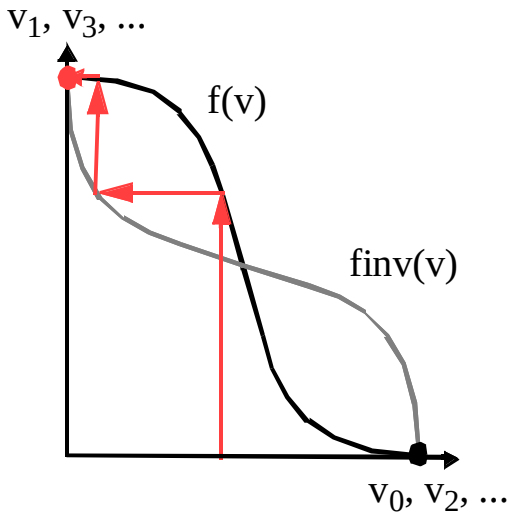
Definition of Noise Margins



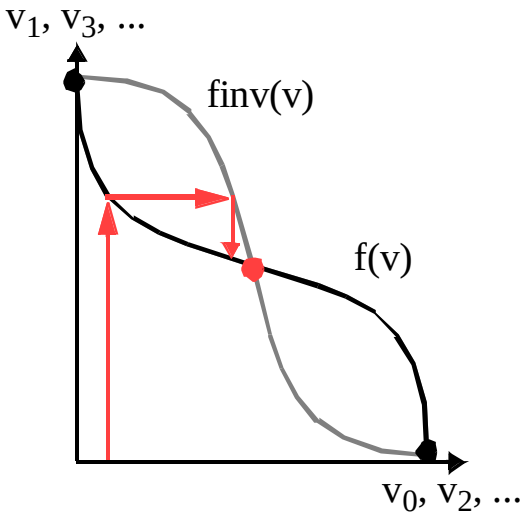
The Regenerative Property



(a) A chain of inverters.

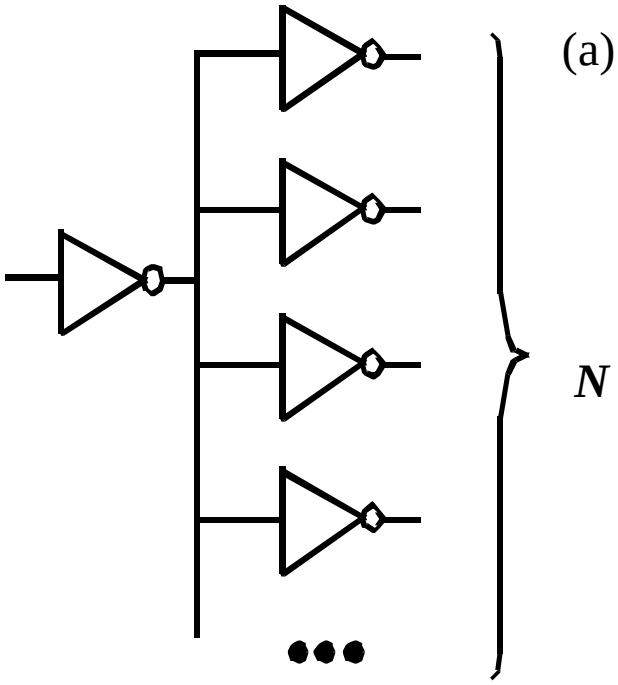


(b) Regenerative gate

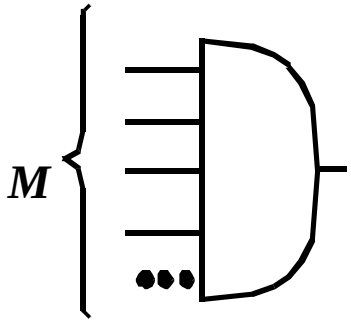


(c) Non-regenerative gate

Fan-in and Fan-out

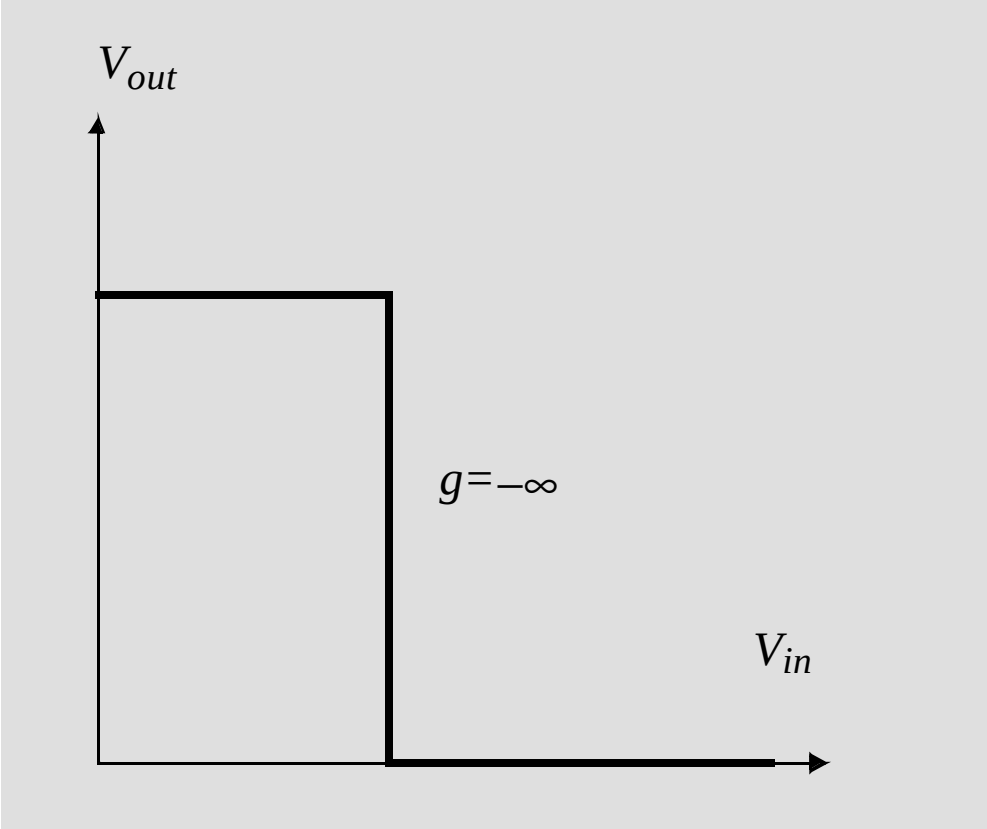


(a) Fan-out *N*



(b) Fan-in *M*

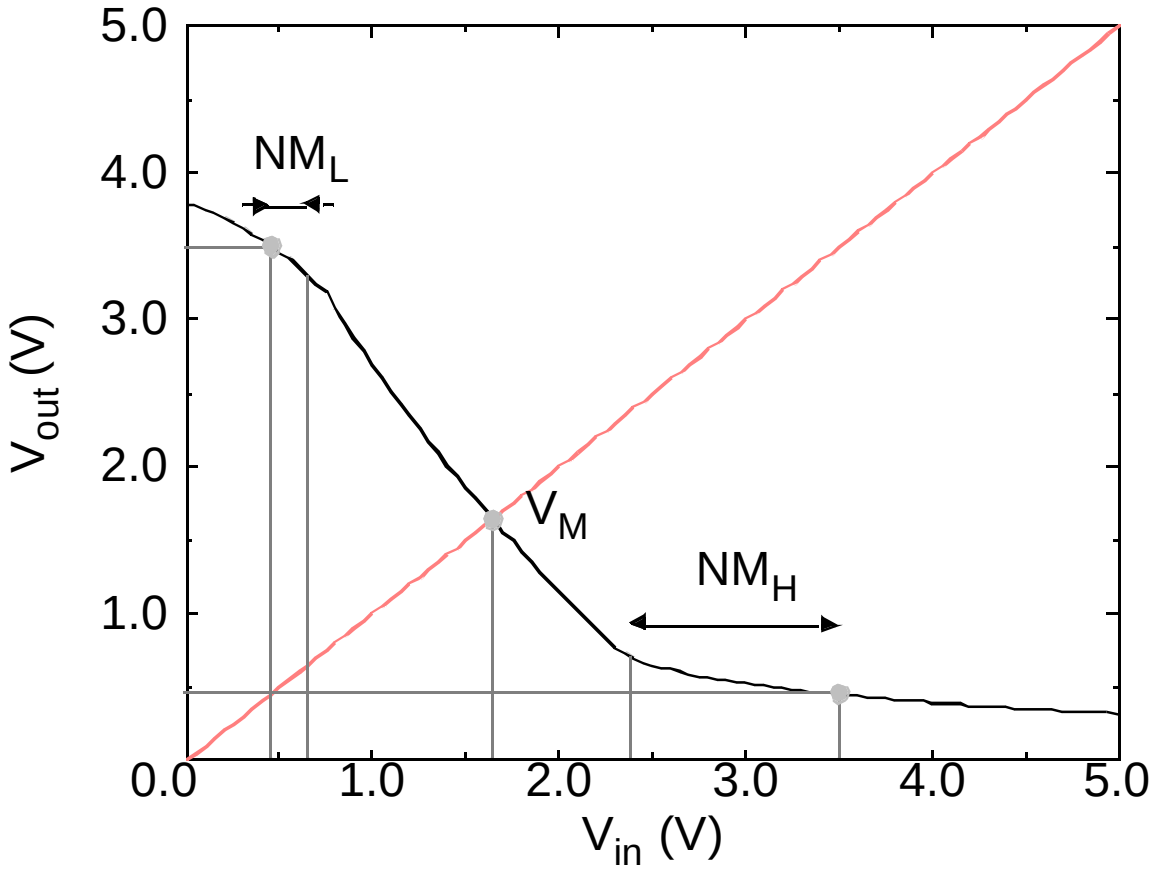
The Ideal Gate



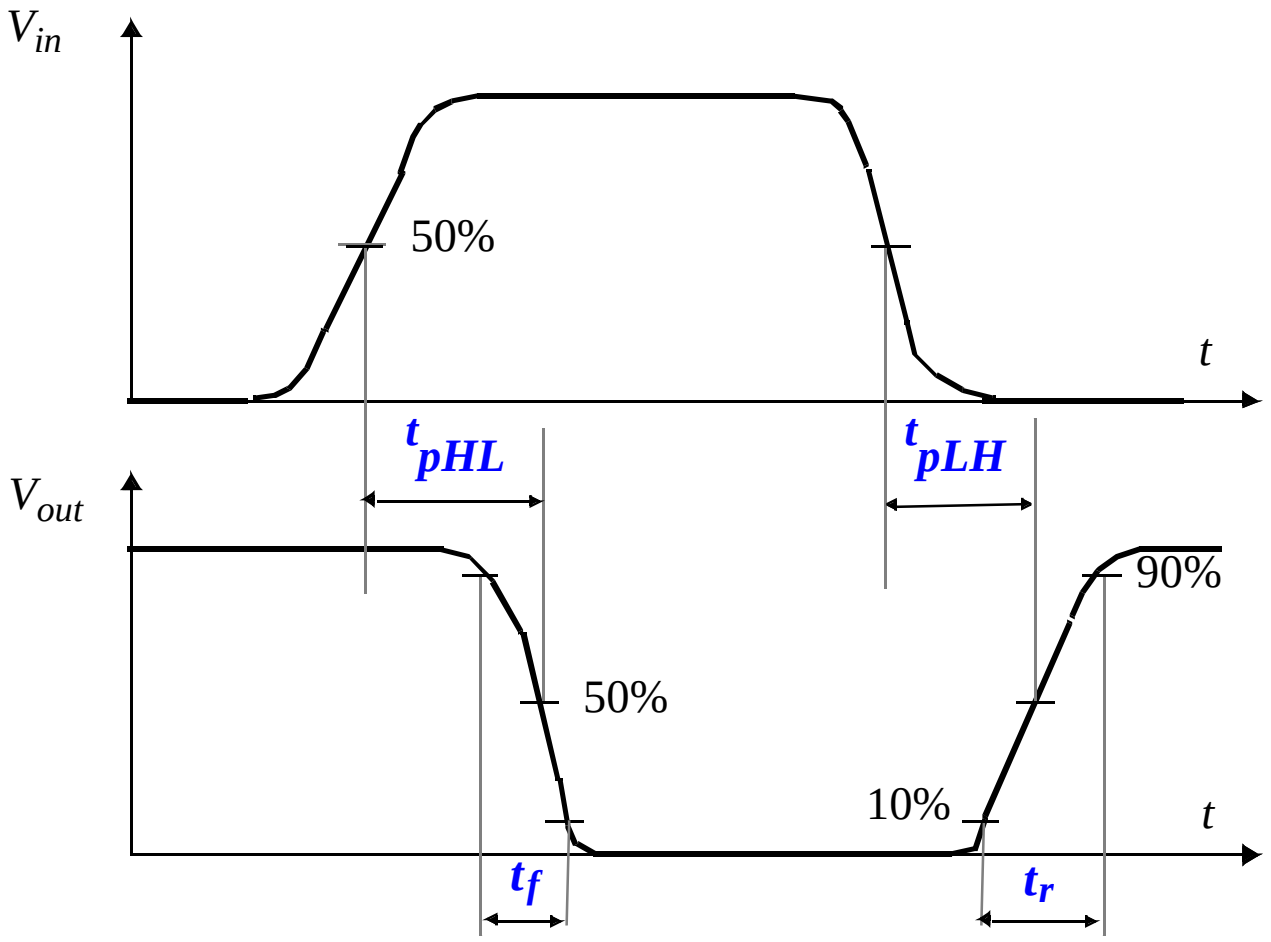
$R_i = \infty$

$R_o = 0$

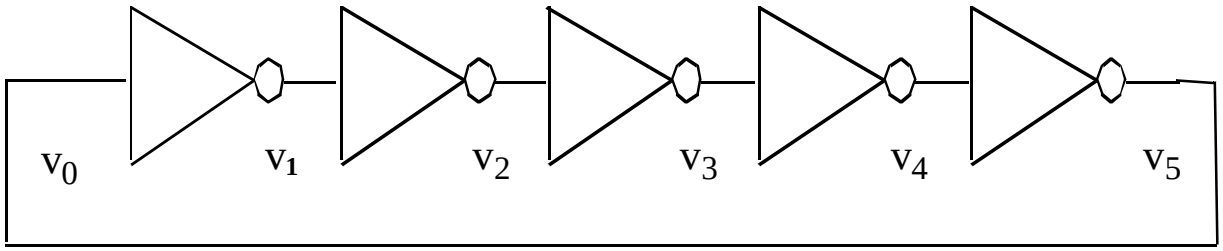
VTC of Real Inverter

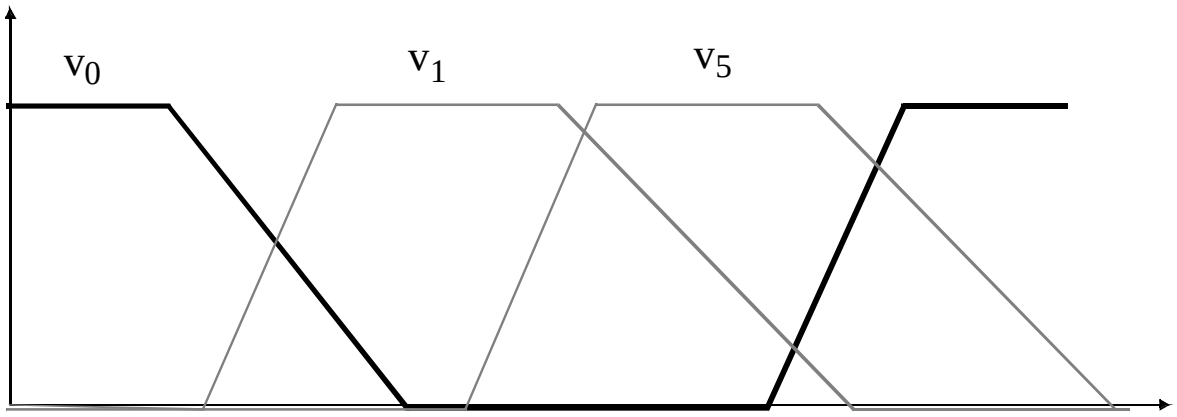


Delay Definitions



Ring Oscillator





$$T = 2 \times t_p \times N$$

Power Dissipation

$$P_{peak} = i_{peak} V_{supply} = max(p(t))$$

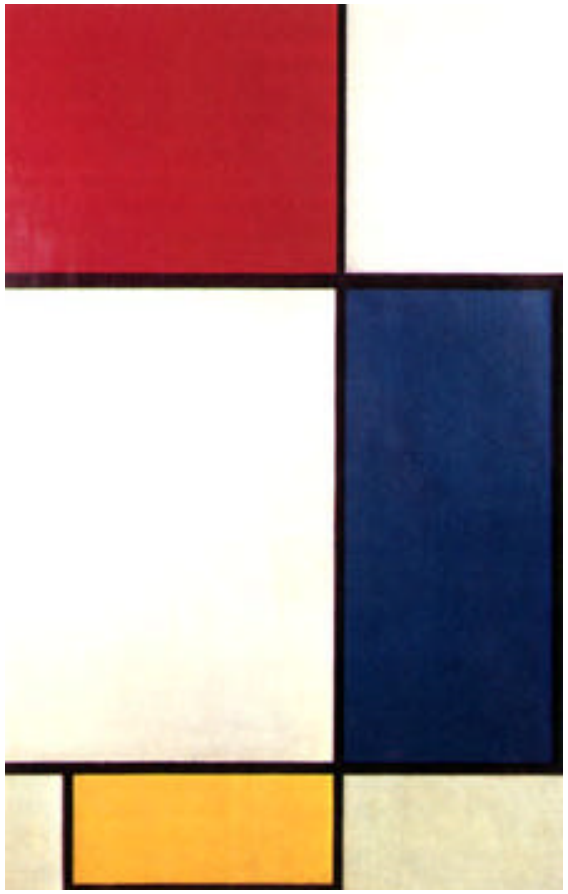
$$P_{av} = \frac{1}{T}\int_0^T p(t)dt = \frac{V_{supply}}{T}\int_0^T i_{supply}(t)dt$$

Power-Delay Product

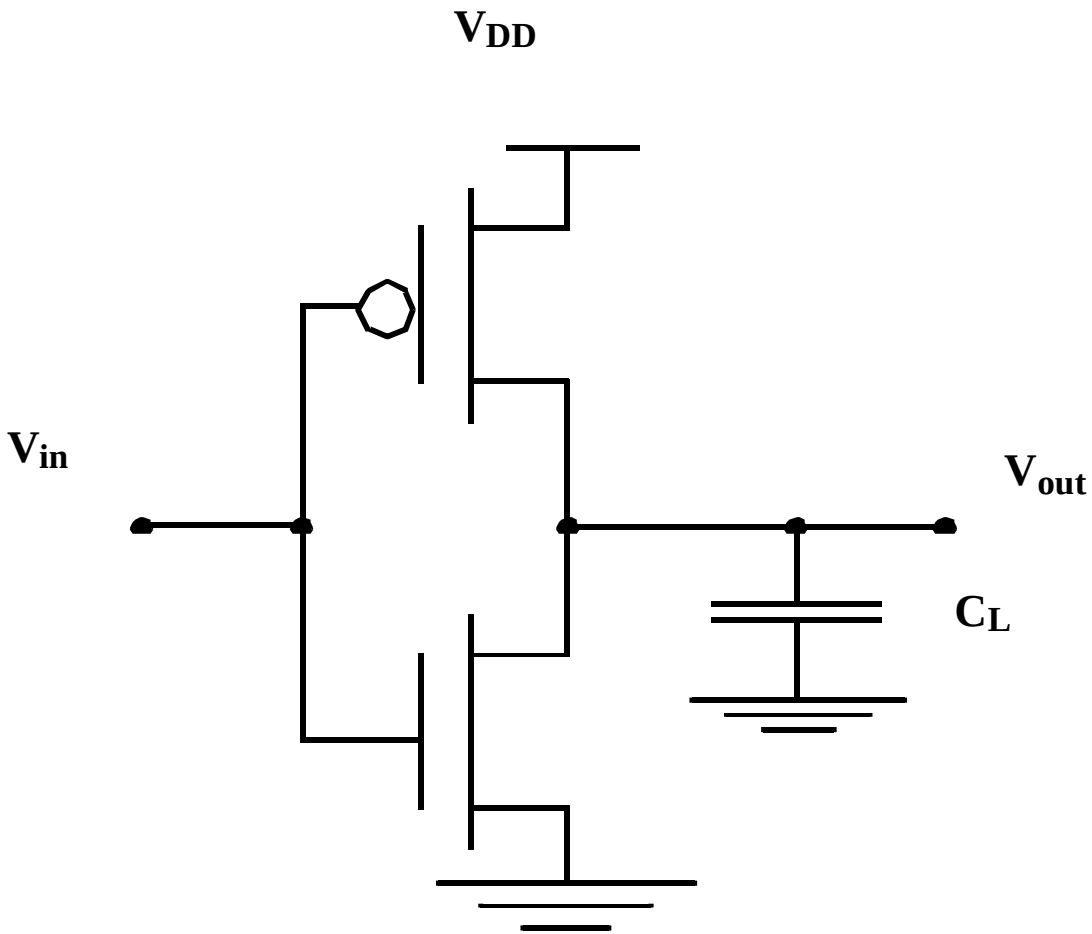
$$PDP = t_p \times P_{av}$$

= Energy dissipated per operation

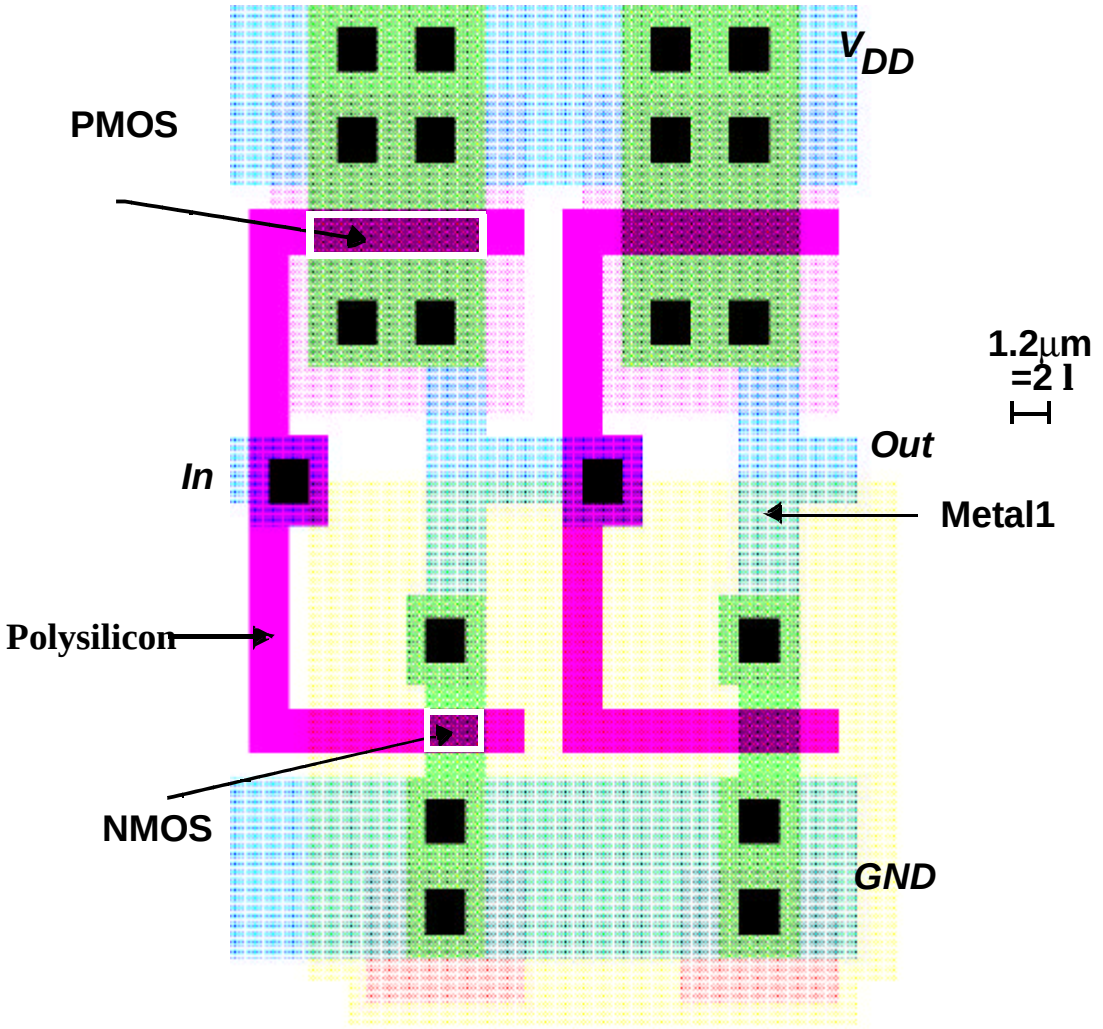
CMOS INVERTER



The CMOS Inverter: A First Glance

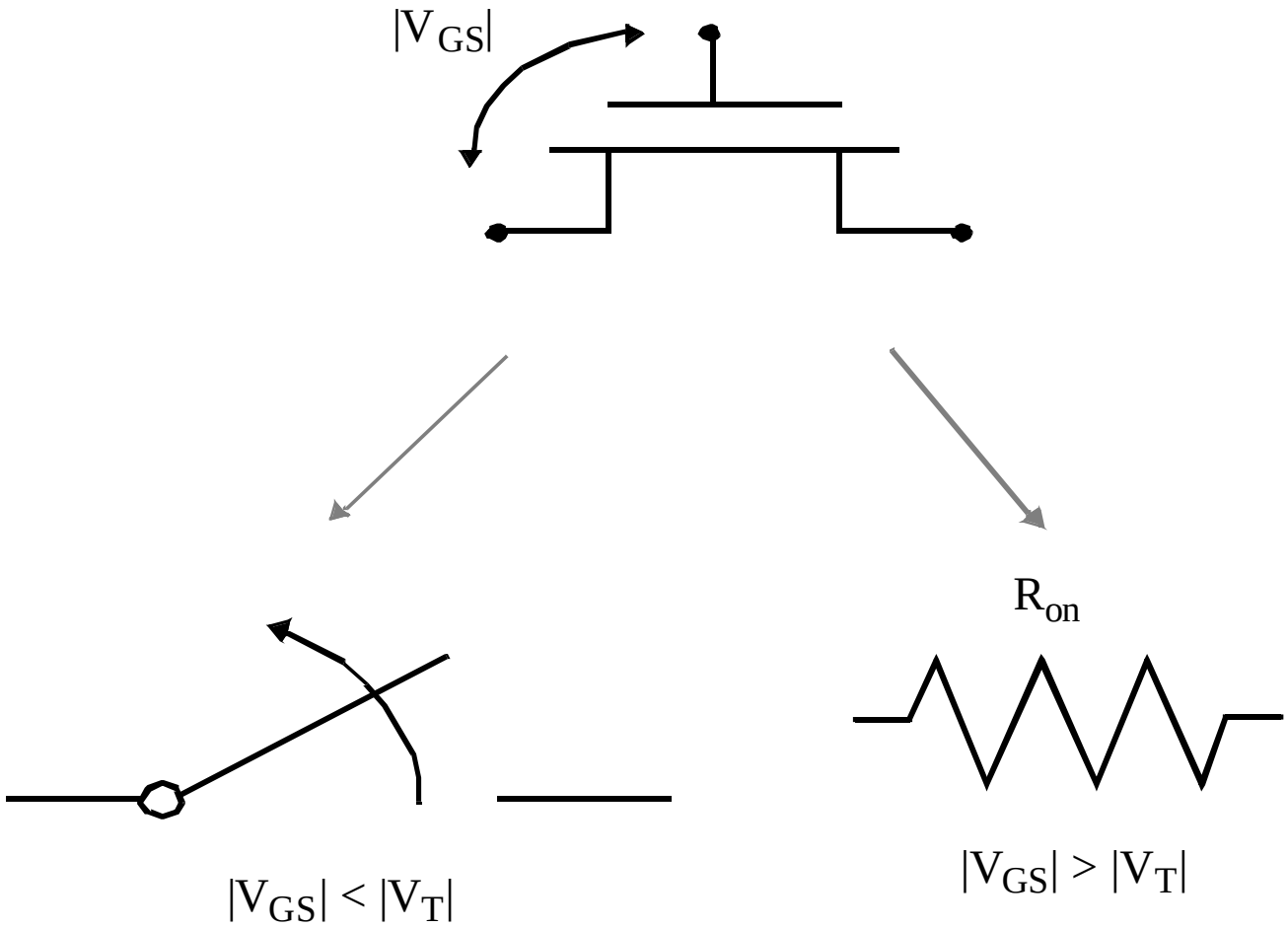


CMOS Inverters

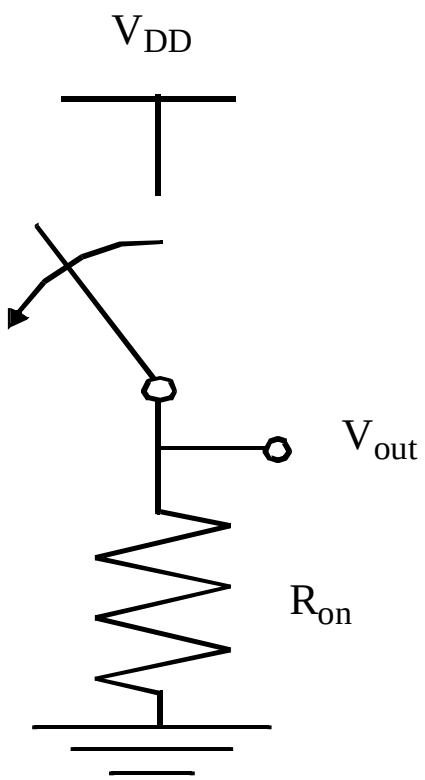


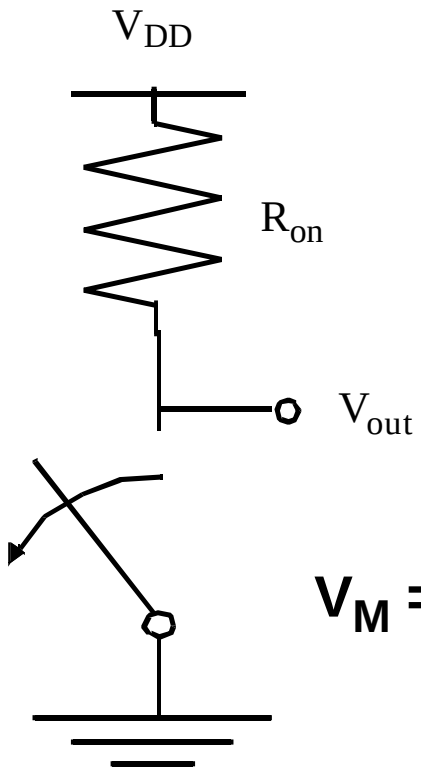
Inverter

Switch Model of CMOS Transistor



CMOS Inverter: Steady State Response



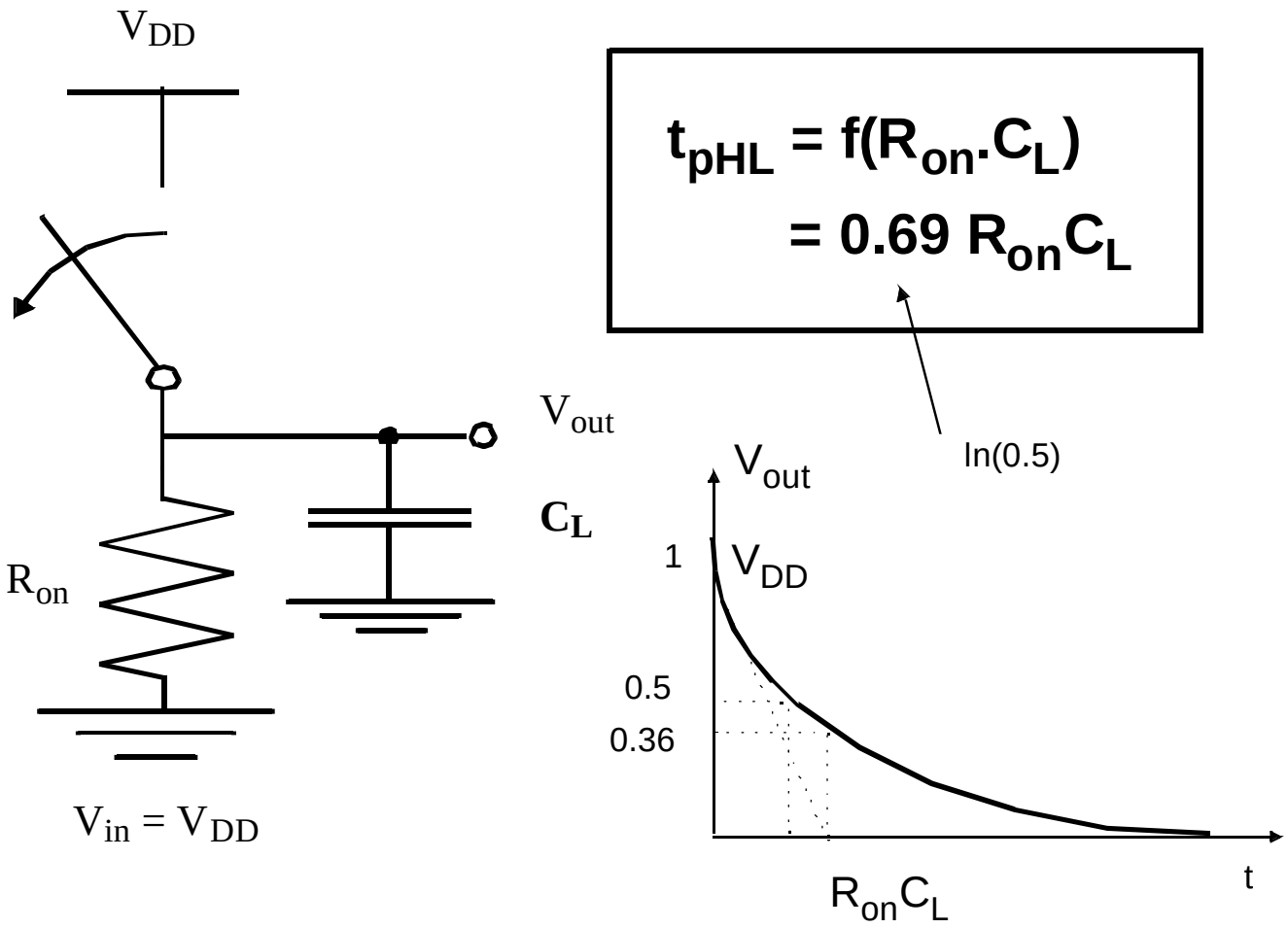


$V_{OH} = V_{DD}$

$V_{OL} = 0$

$V_M = f(R_{onn}, R_{onp})$

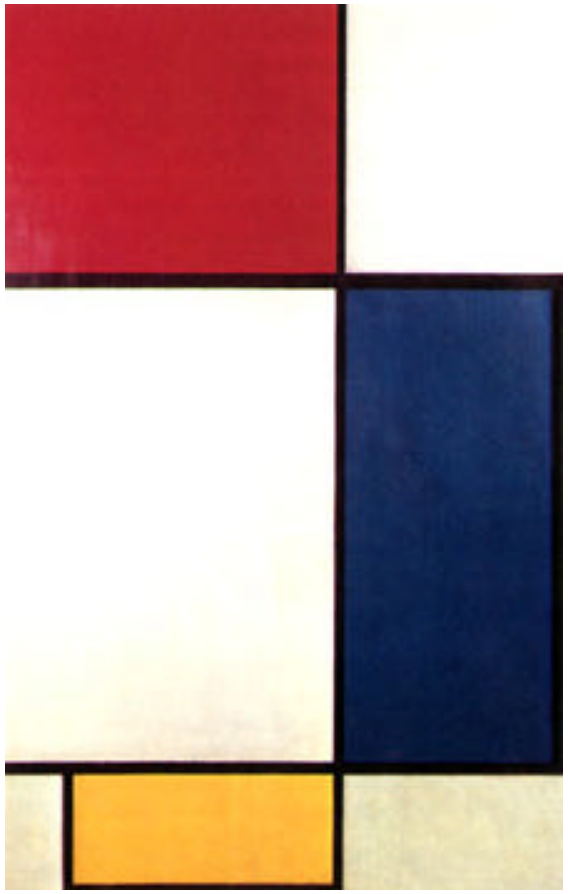
CMOS Inverter: Transient Response



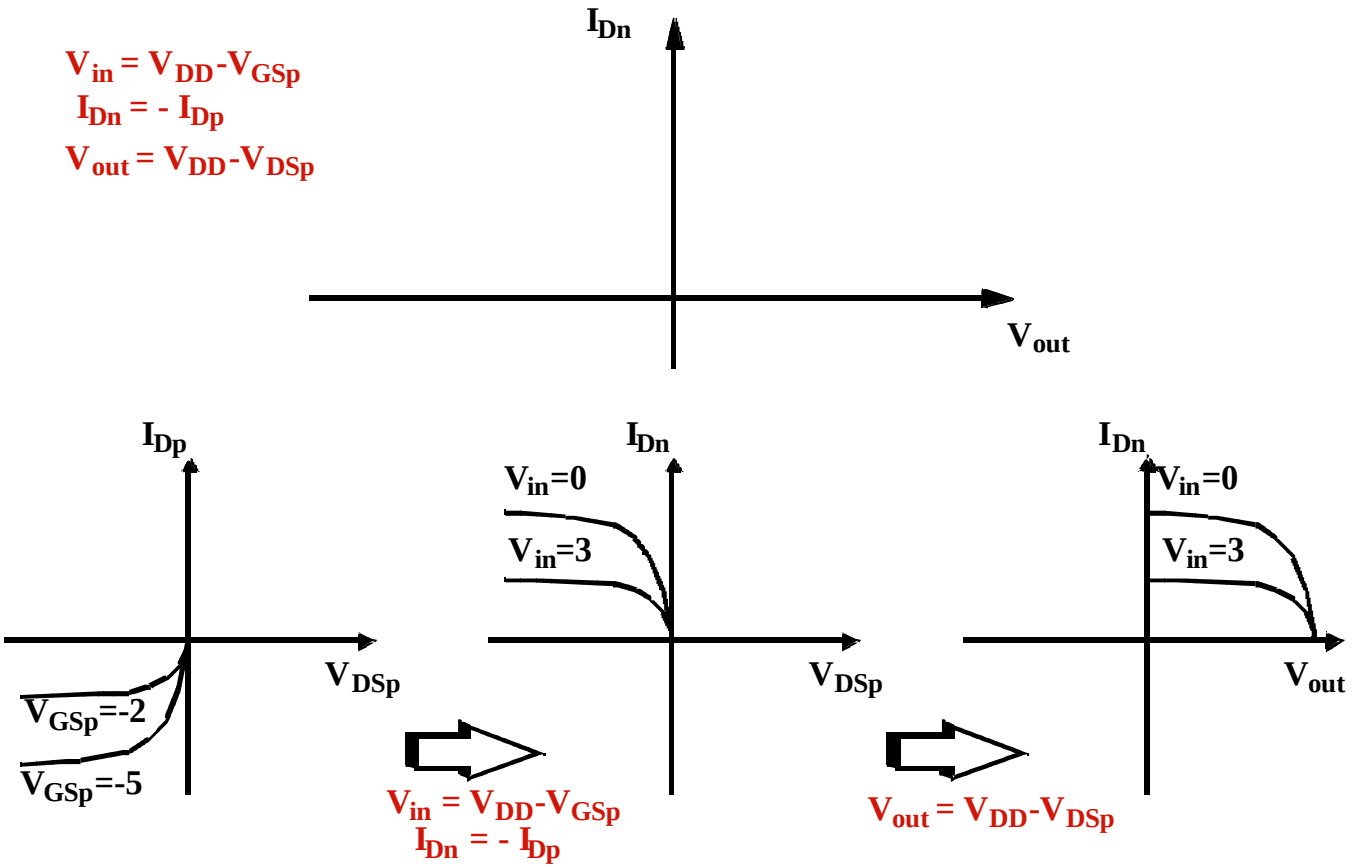
CMOS Properties

- Full rail-to-rail swing
- Symmetrical VTC
- Propagation delay function of load capacitance and resistance of transistors
- No static power dissipation
- Direct path current during switching

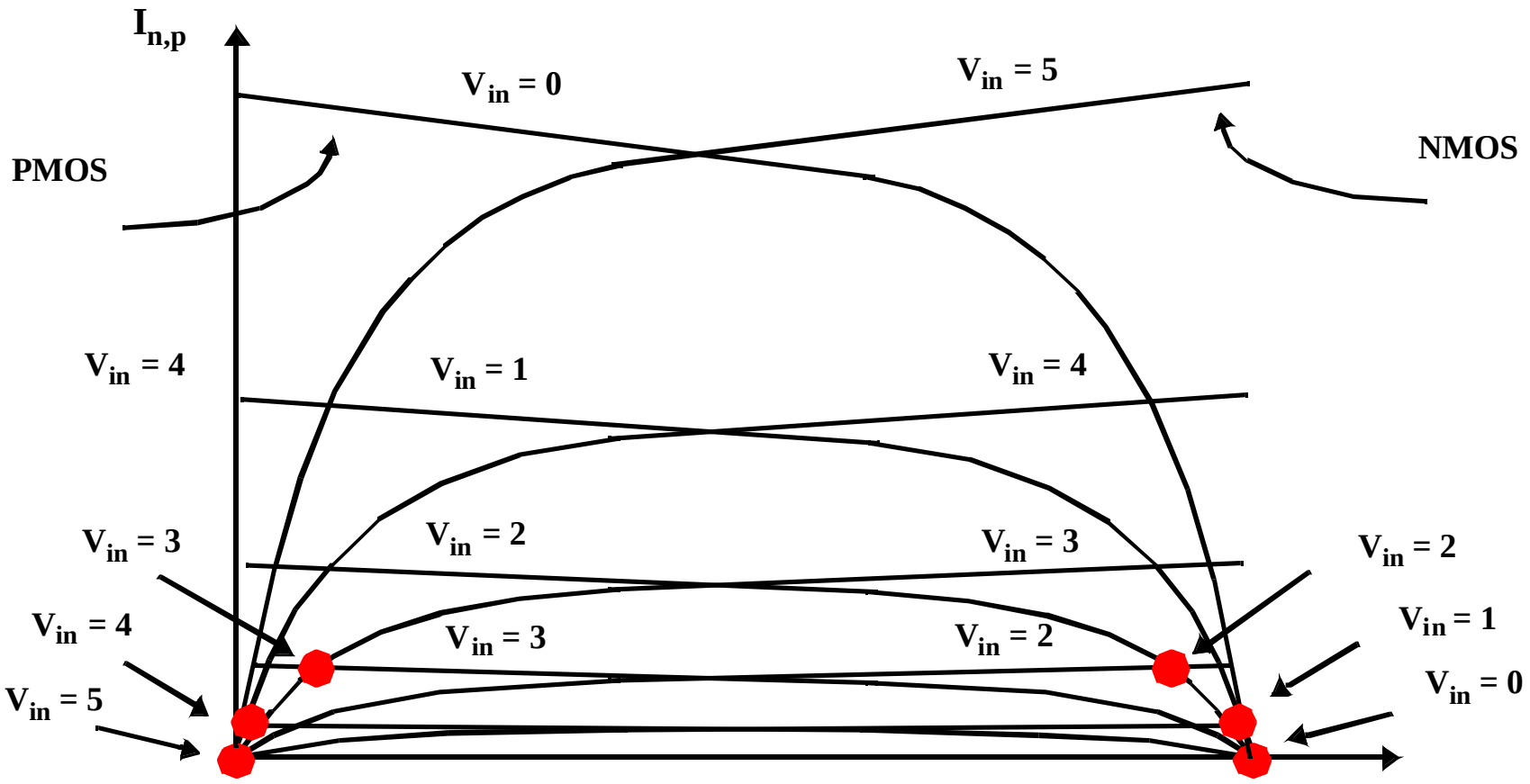
Voltage Transfer Characteristic



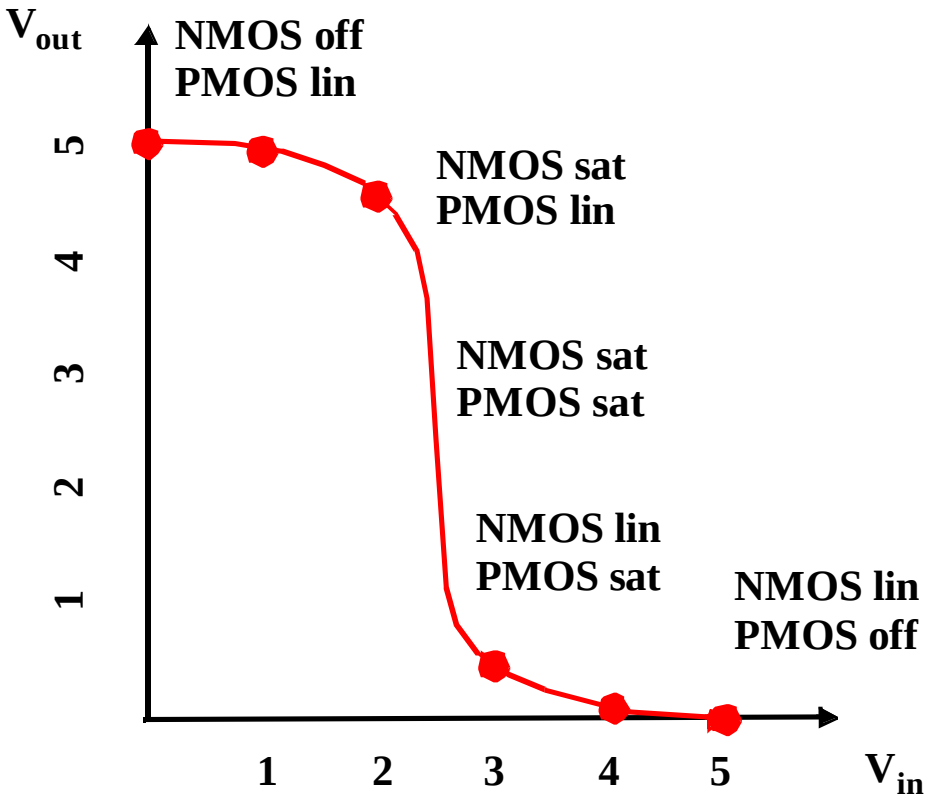
PMOS Load Lines



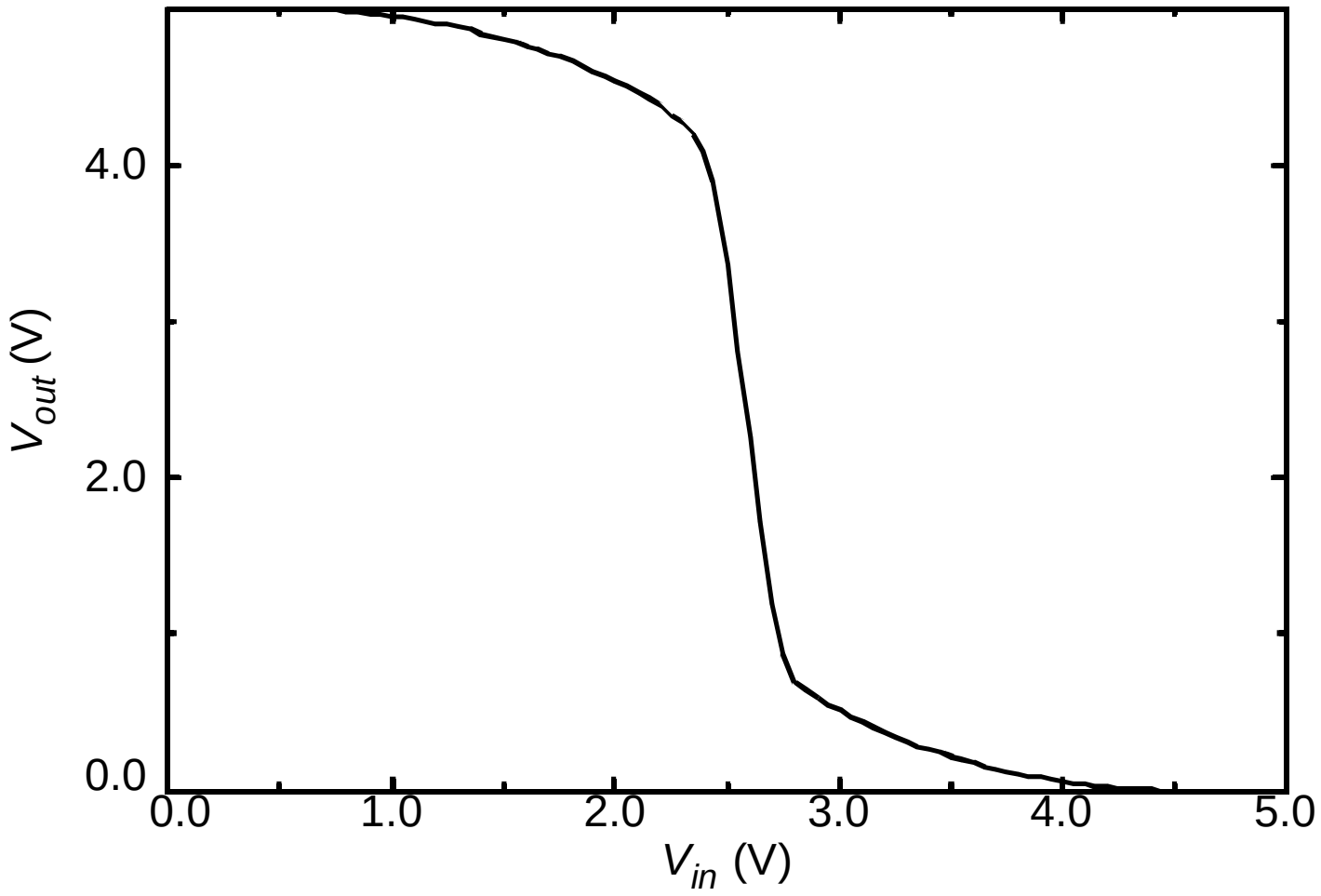
CMOS Inverter Load Characteristics



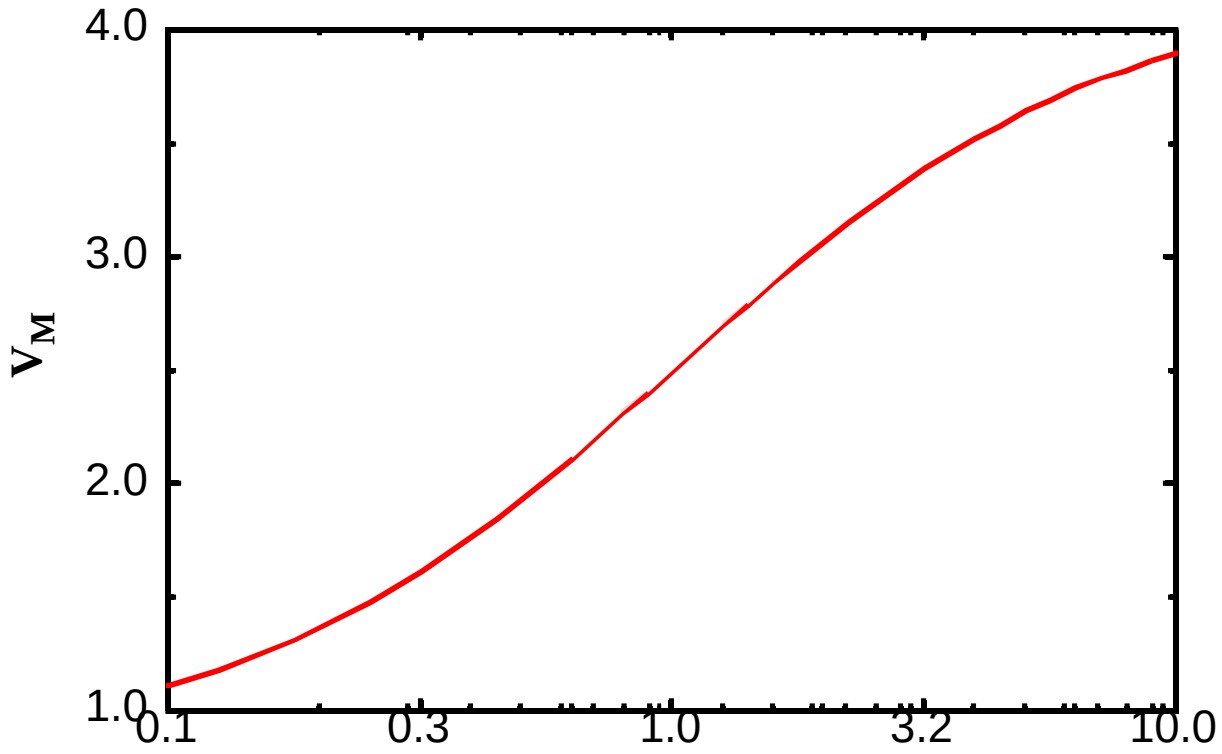
CMOS Inverter VTC



Simulated VTC

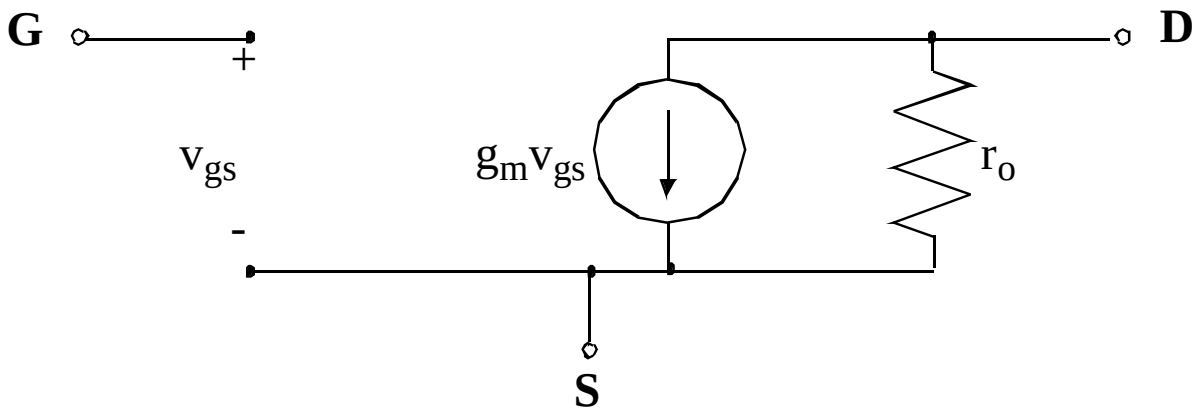


Gate Switching Threshold



$$V_M = \frac{r(V_{DD} - |V_{Tp}|) + V_{Tn}}{1 + r} \quad \text{with} \quad r = \sqrt{\frac{k_p}{k_n}}$$

MOS Transistor Small Signal Model

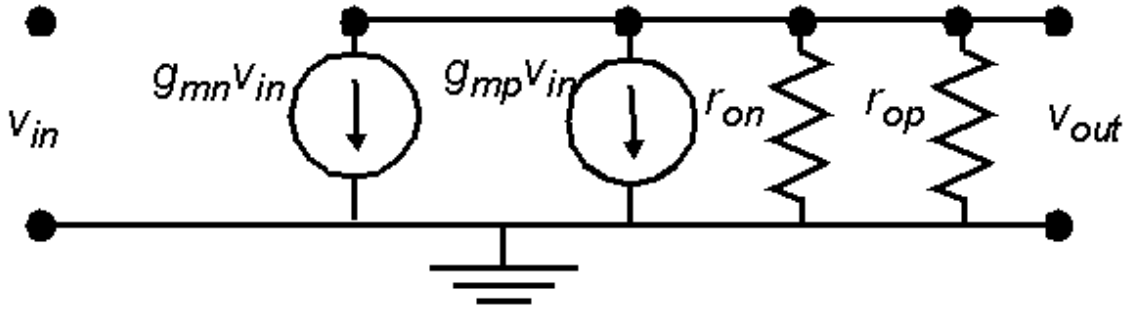


	g_m	r_o
linear	kV_{DS}	$[k(V_{GS}-V_T-V_{DS})]^{-1}$
saturation	$k(V_{GS}-V_T)$	$1/\lambda I_D$

Determining V_{IH} and V_{IL}

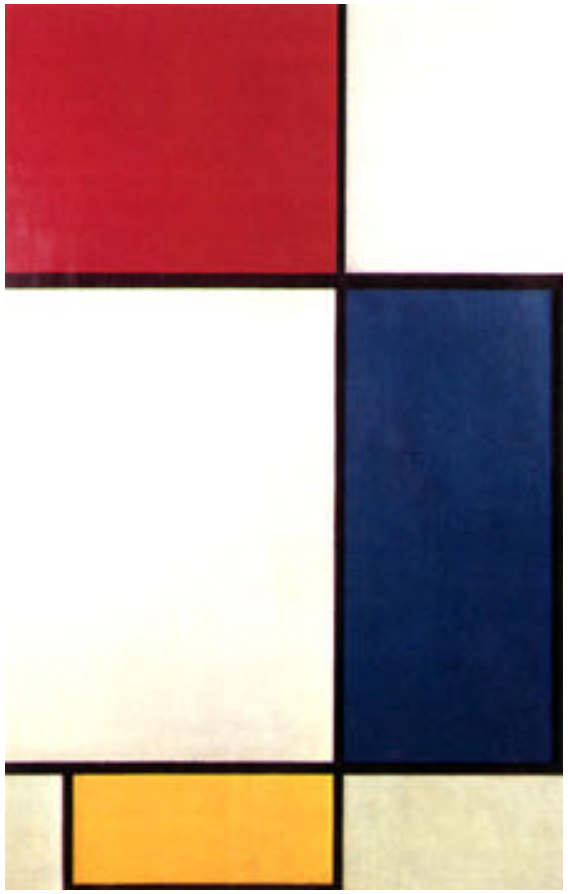
At V_{IH} (V_{IL}): $$\frac{\partial V_{out}}{\partial V_{in}} = -1$$

small-signal model of inverter

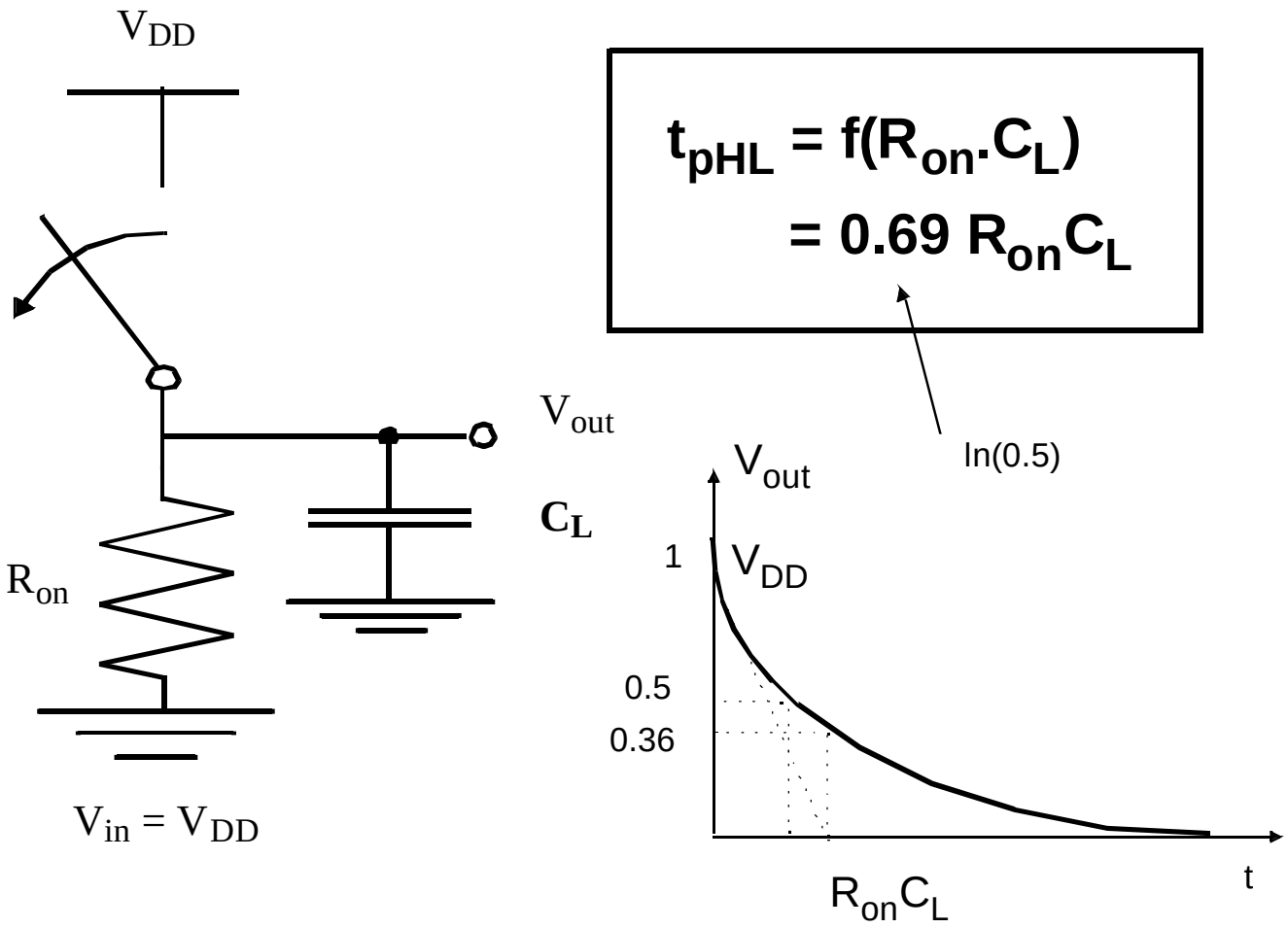


$$g = \frac{v_{out}}{v_{in}} = -(g_{mn} + g_{mp}) \times (r_{on} \| r_{op}) = -1$$

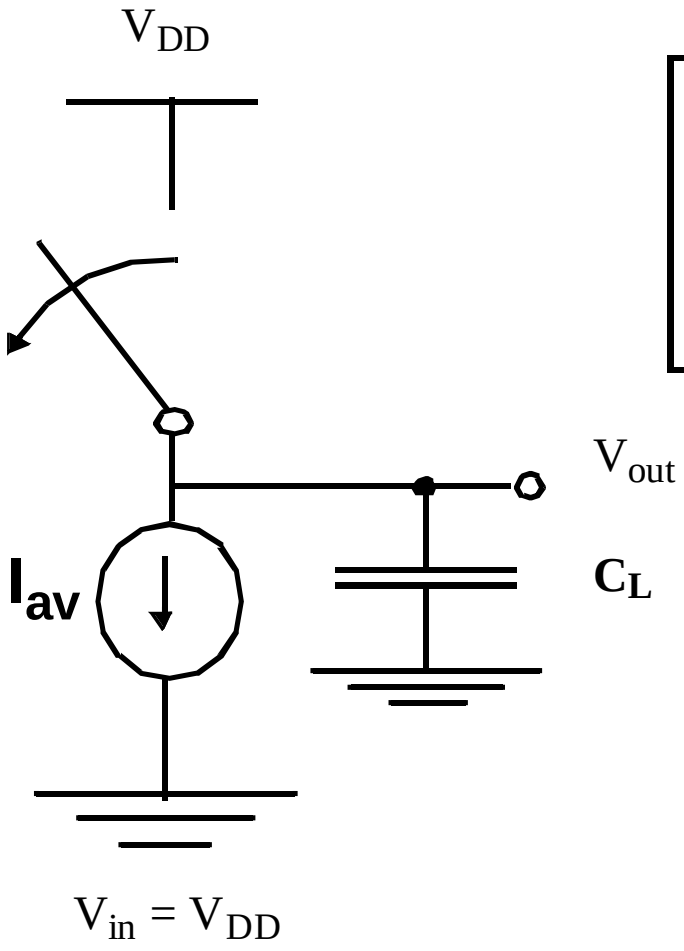
Propagation Delay



CMOS Inverter: Transient Response



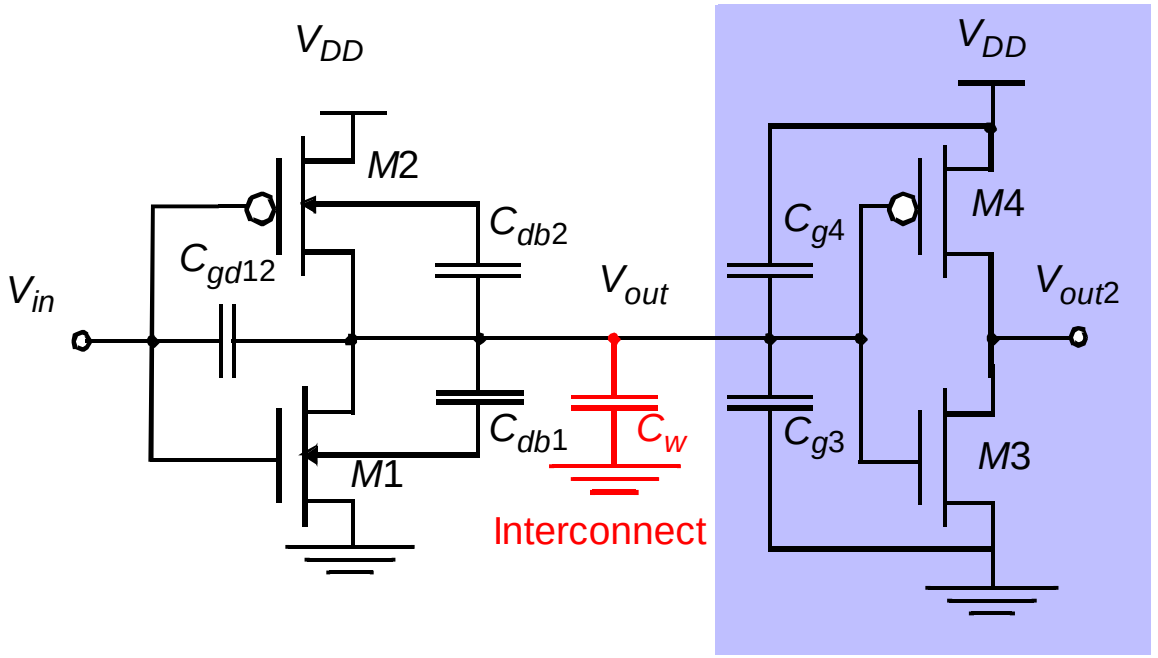
CMOS Inverter Propagation Delay



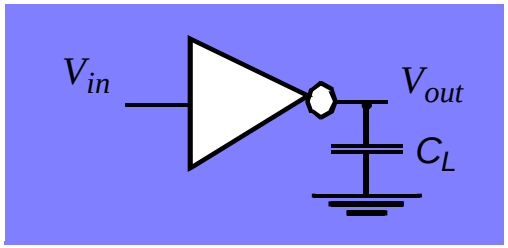
$$t_{pHL} = \frac{C_L \, V_{swing}/2}{I_{av}}$$

$$\sim \frac{C_L}{k_n \, V_{DD}}$$

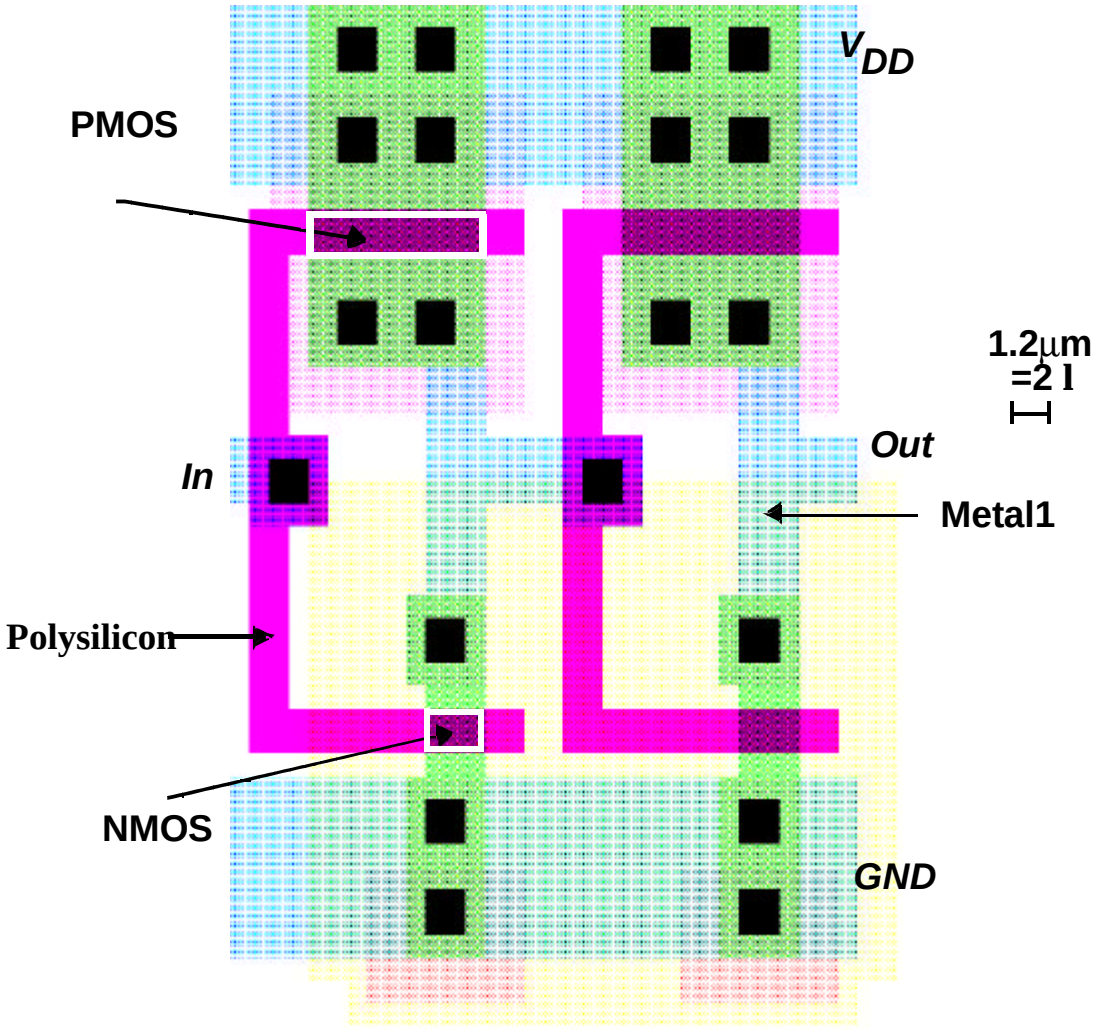
Computing the Capacitances



Simplified Model

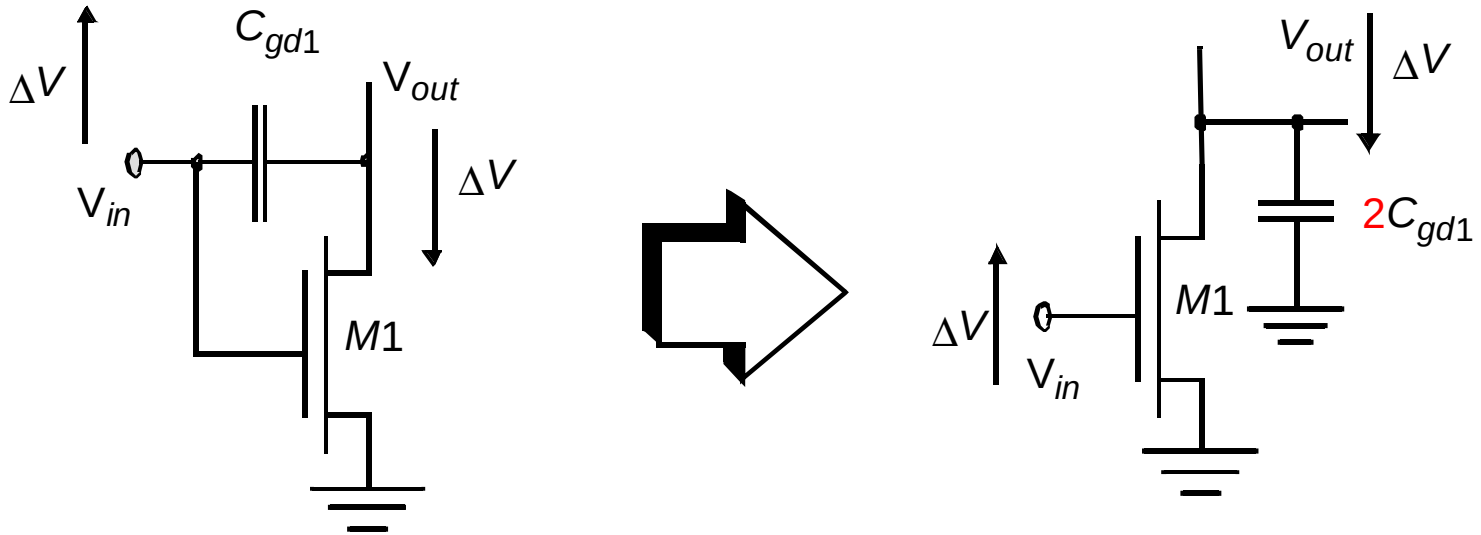


CMOS Inverters



Inverter

The Miller Effect

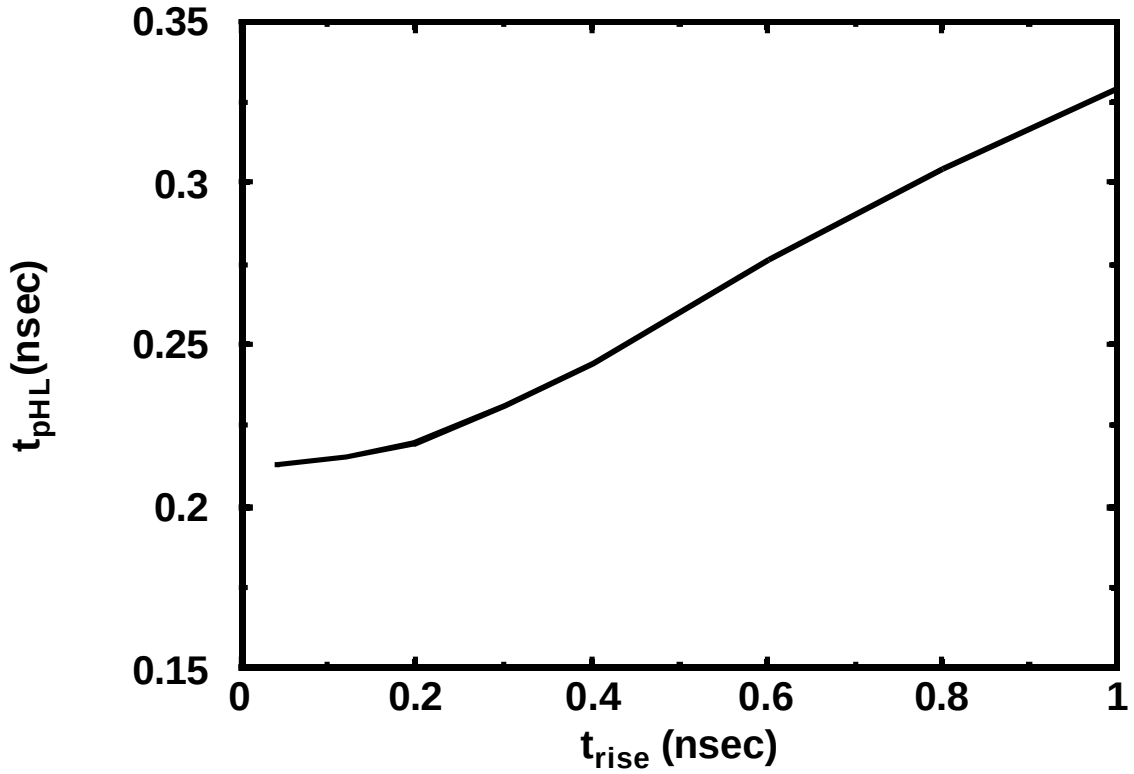


"A capacitor experiencing identical but opposite voltage swings at both its terminals can be replaced by a capacitor to ground, whose value is two times the original value."

Computing the Capacitances

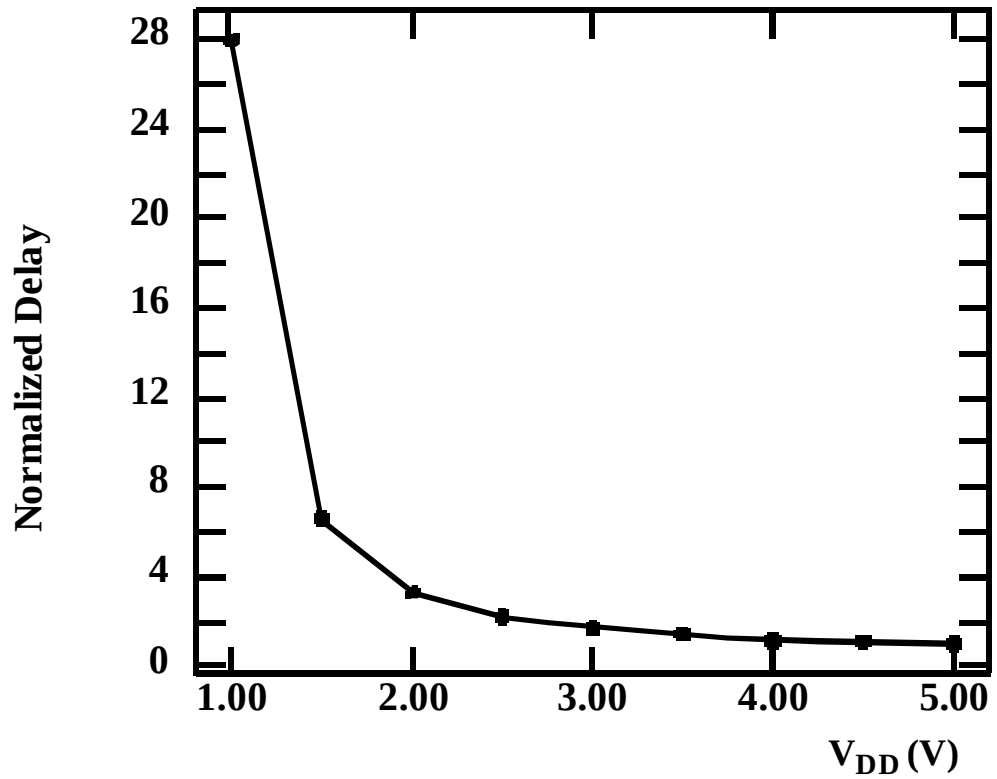
Capacitor	Expression
C_{gd1}	2 CGD0 W_n
C_{gd2}	2 CGD0 W_p
C_{db1}	K_{eqn} (AD_n CJ + PD_n CJSW)
C_{db2}	K_{eqp} (AD_p CJ + PD_p CJSW)
C_{g3}	C_{ox} W_n L_n
C_{g4}	C_{ox} W_p L_p
C_w	From Extraction
C_L	Σ

Impact of Rise Time on Delay



$$t_{pHL} = \sqrt{t_{pHL(step)}^2 + (t_r/2)^2}$$

Delay as a function of V_{DD}



Where Does Power Go in CMOS?

- **Dynamic Power Consumption**

  Charging and Discharging Capacitors

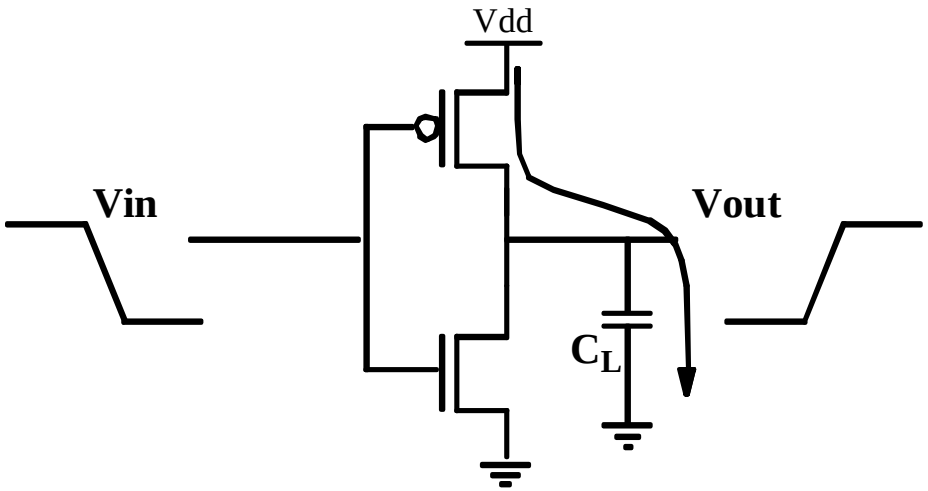
- **Short Circuit Currents**

  Short Circuit Path between Supply Rails during Switching

- **Leakage**

  Leaking diodes and transistors

Dynamic Power Dissipation

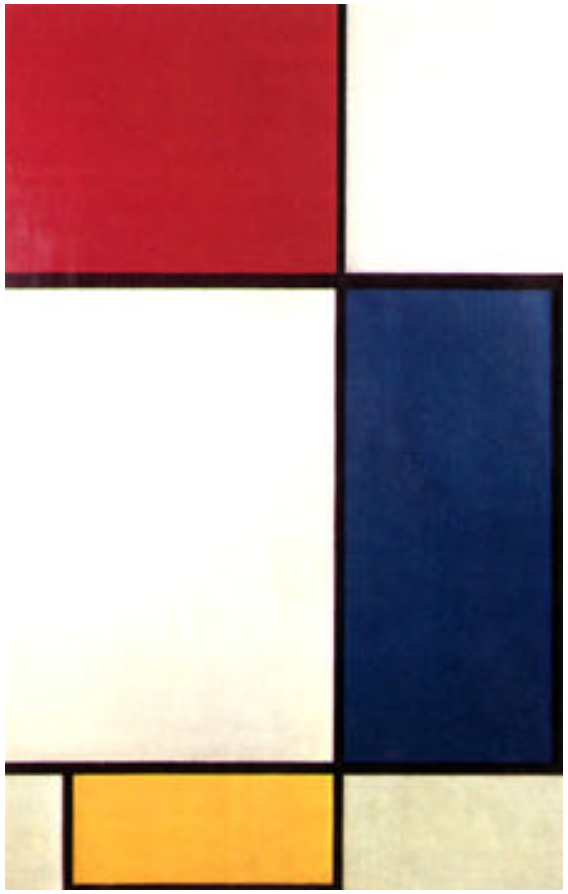


Energy/transition = $C_L * V_{dd}^2$

Power = Energy/transition * f = $C_L * V_{dd}^2 * f$

- **Not a function of transistor sizes!**
- **Need to reduce C_L, V_{dd}, and f to reduce power.**

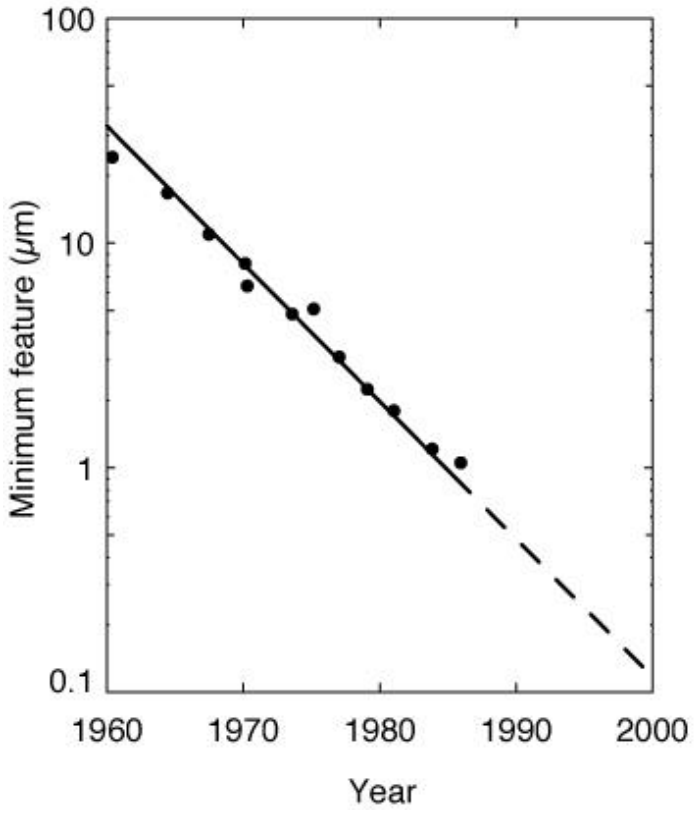
Impact of Technology Scaling



Technology Evolution

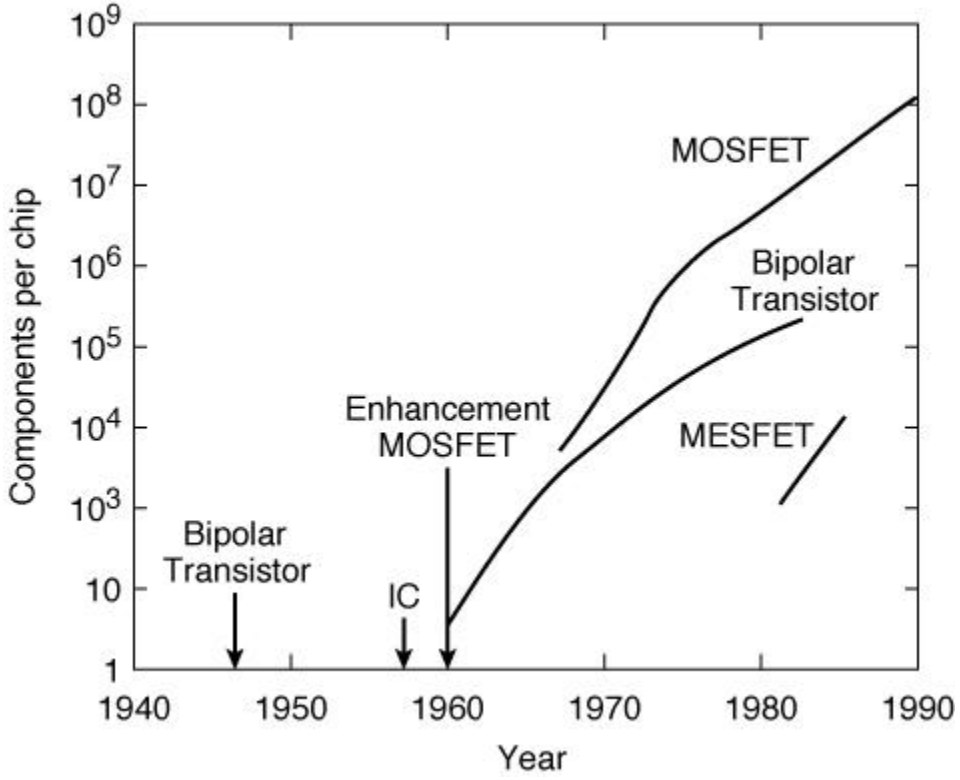
Year of Introduction	1994	1997	2000	2003	2006	2009
Channel length (μm)	0.4	0.3	0.25	0.18	0.13	0.1
Gate oxide (nm)	12	7	6	4.5	4	4
V_{DD} (V)	3.3	2.2	2.2	1.5	1.5	1.5
V_T (V)	0.7	0.7	0.7	0.6	0.6	0.6
NMOS I_{Dsat} (mA/μm) (@ $V_{GS} = V_{DD}$)	0.35	0.27	0.31	0.21	0.29	0.33
PMOS I_{Dsat} (mA/μm) (@ $V_{GS} = V_{DD}$)	0.16	0.11	0.14	0.09	0.13	0.16

Technology Scaling (1)



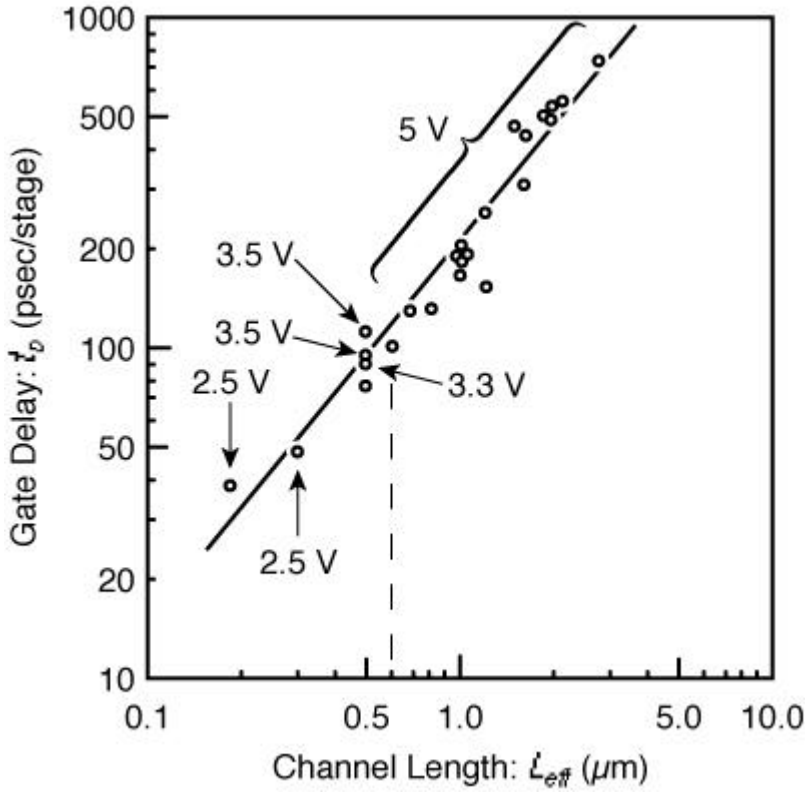
Minimum Feature Size

Technology Scaling (2)



Number of components per chip

Propagation Delay Scaling



Technology Scaling Models

- **Full Scaling (Constant Electrical Field)**

  ideal model — dimensions and voltage scale together by the same factor *S*

- **Fixed Voltage Scaling**

  most common model until recently — only dimensions scale, voltages remain constant

- **General Scaling**

  most realistic for todays situation — voltages and dimensions scale with different factors

Scaling Relationships for Long Channel Devices

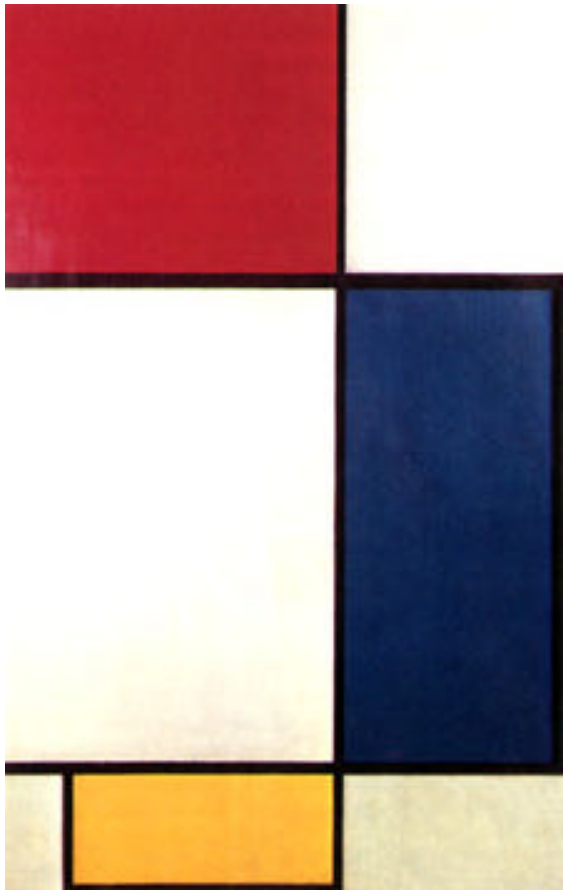
Parameter	Relation	Full Scaling	General Scaling	Fixed Voltage Scaling
W, L, t_{ox}		1/S	1/S	1/S
V_{DD}, V_T		1/S	1/U	1
N_{SUB}	V/W_{depl}^2	S	S^2/U	S^2
Area/Device	WL	$1/S^2$	$1/S^2$	$1/S^2$
C_{ox}	$1/t_{ox}$	S	S	S
C_L	$C_{ox}WL$	1/S	1/S	1/S
k_n, k_p	$C_{ox}W/L$	S	S	S
I_{av}	$k_{n,p} V^2$	1/S	S/U^2	S
t_p (intrinsic)	$C_L V / I_{av}$	1/S	U/S^2	$1/S^2$
P_{av}	$C_L V^2 / t_p$	$1/S^2$	S/U^3	S
PDP	$C_L V^2$	$1/S^3$	$1/SU^2$	1/S

Table 3.1: Scaling Relationships for Long Channel Devices

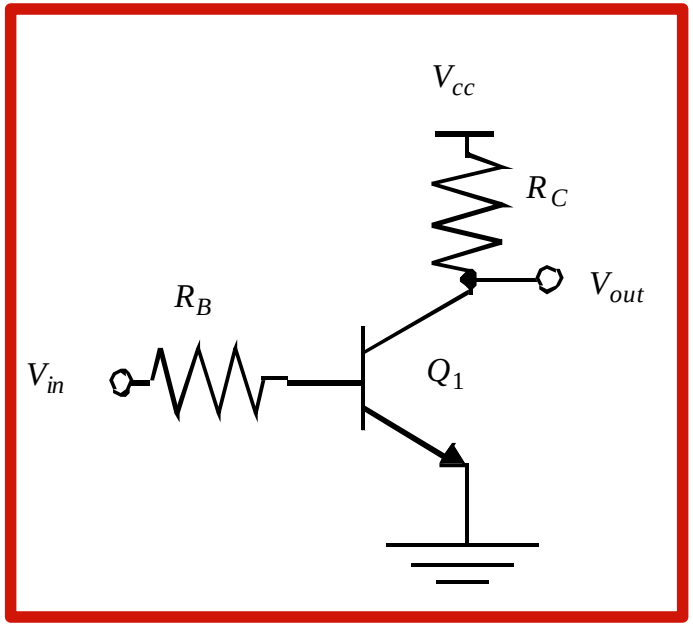
Scaling of Short Channel Devices

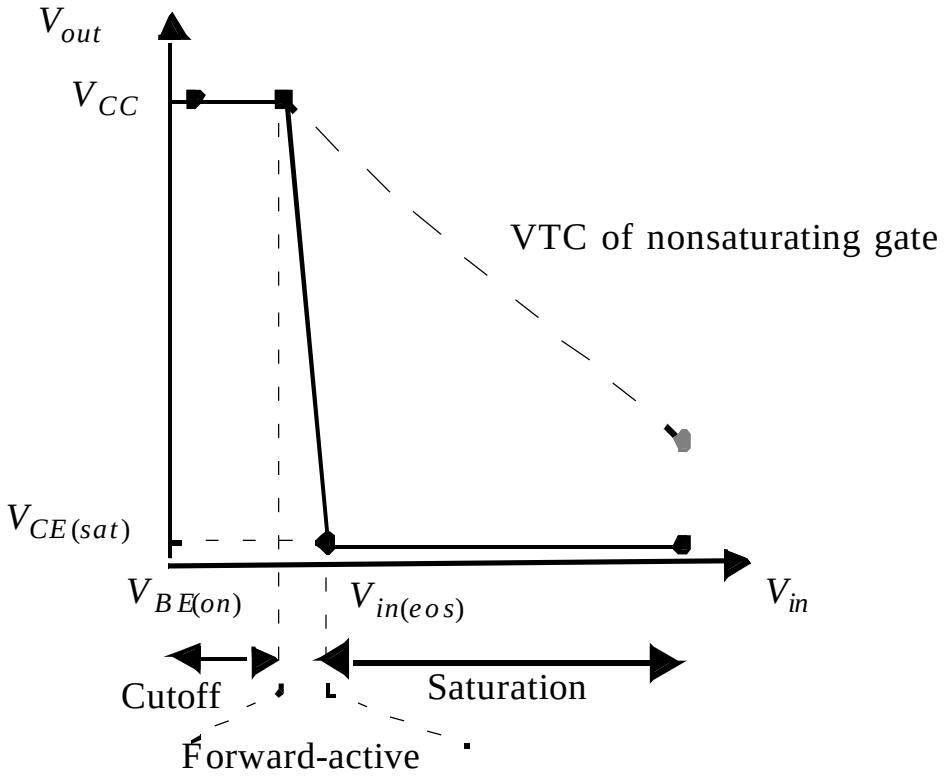
Parameter	Relation	Full Scaling	General Scaling	Fixed Voltage Scaling
I_{av}	$C_{ox}WV$	1/S	1/U	1
J_{av}	I_{av}/Area	S	S^2/U	S^2
t_p (intrinsic)	C_LV / I_{av}	1/S	1/S	1/S
P_{av}	C_LV^2 / t_p	$1/S^2$	$1/U^2$	1

BIPOLAR INVERTERS

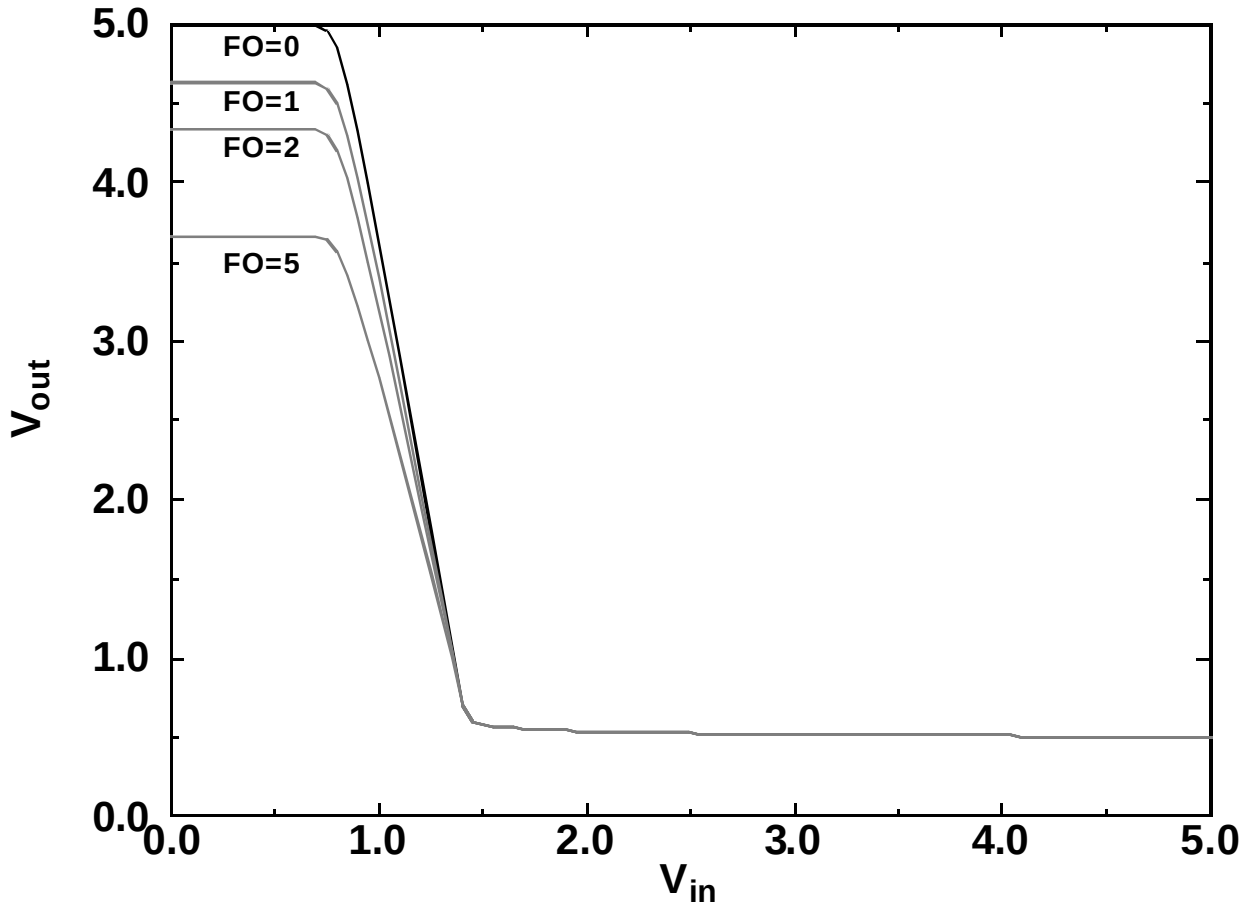


Resistor-Transistor Logic



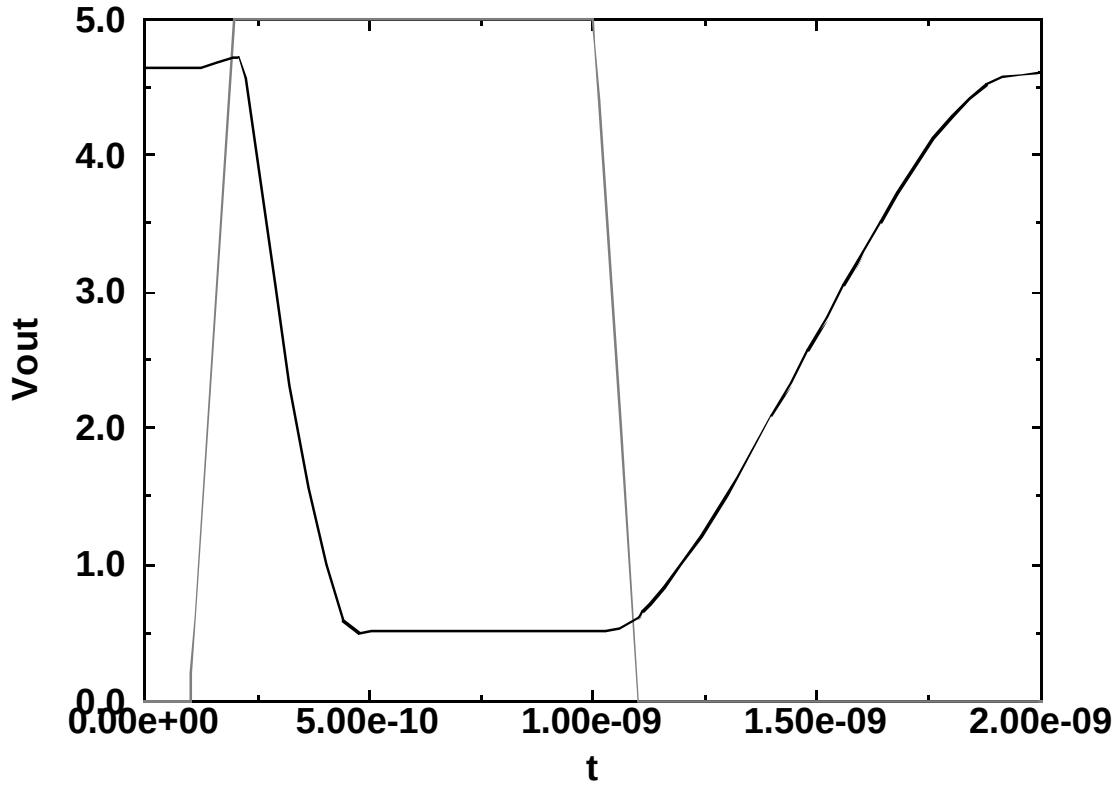


VTC of RTL Inverter



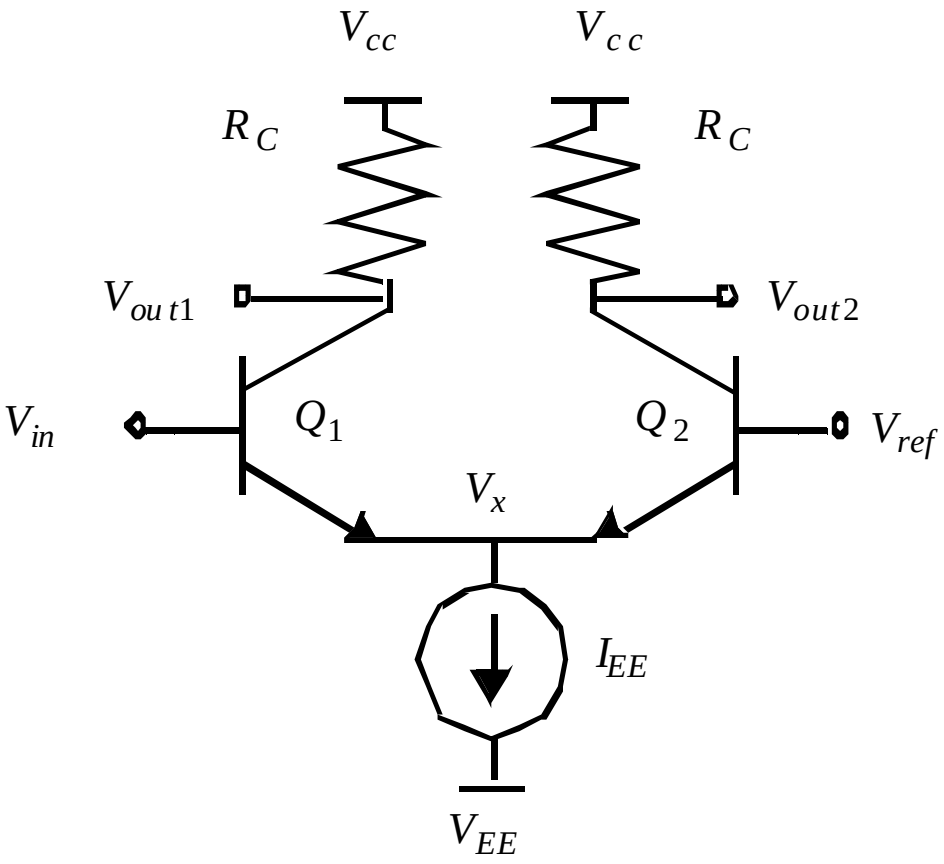
VOH is function of fan-out

Transient Response of RTL Inverter



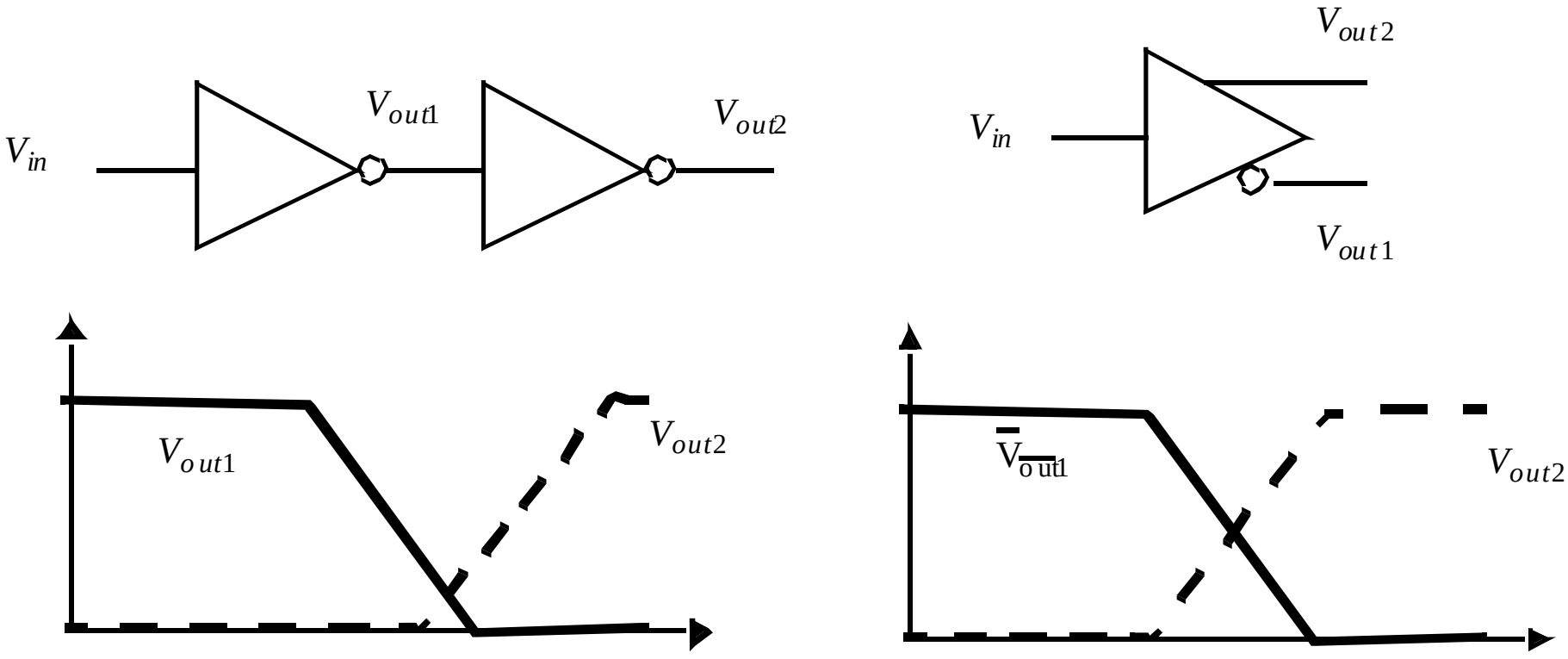
t_p = 290 psec !!!!

The ECL Gate at a Glance



Core of gate:
The differential pair
or “current switch”

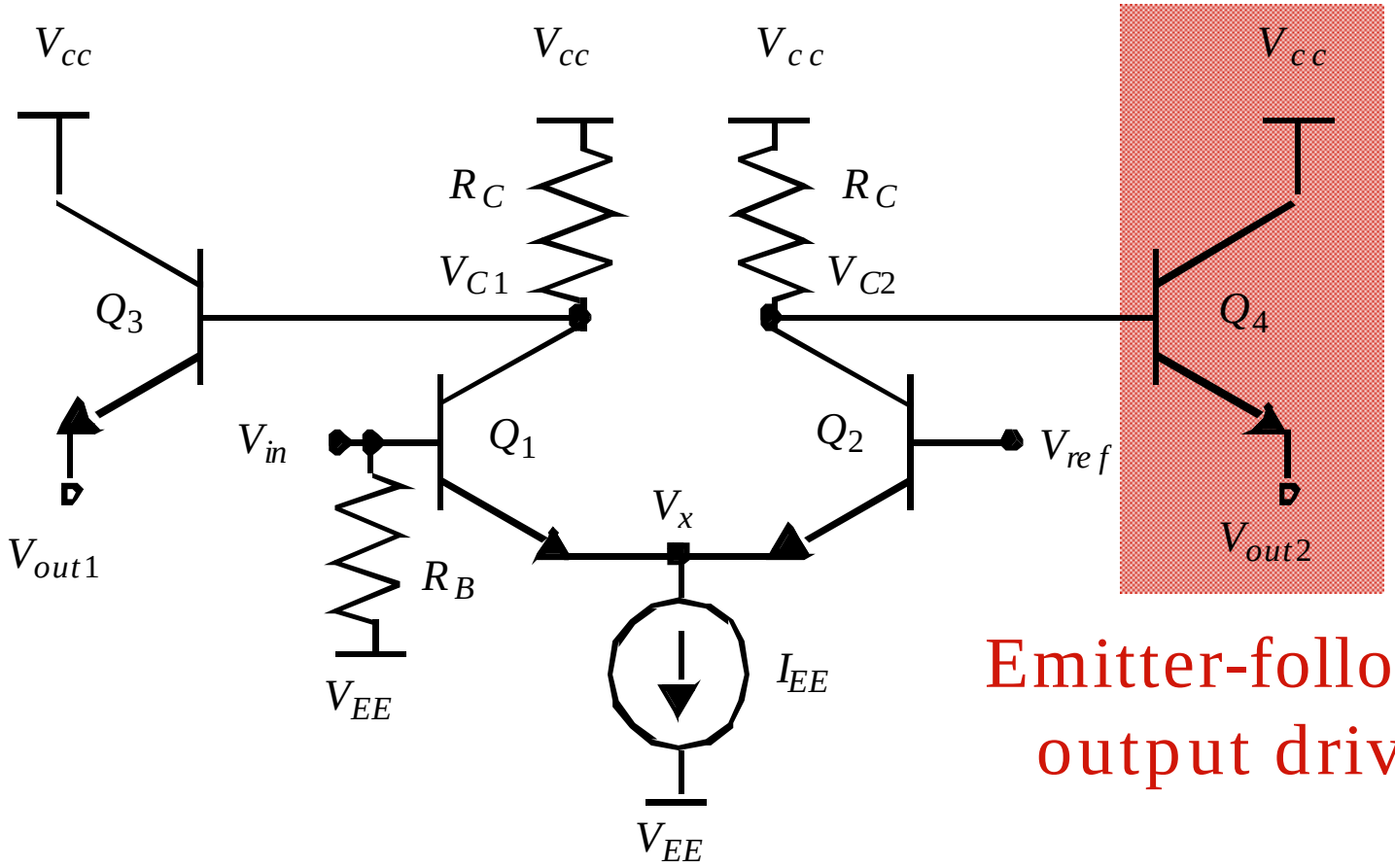
Single-ended versus Differential Logic



Single-ended

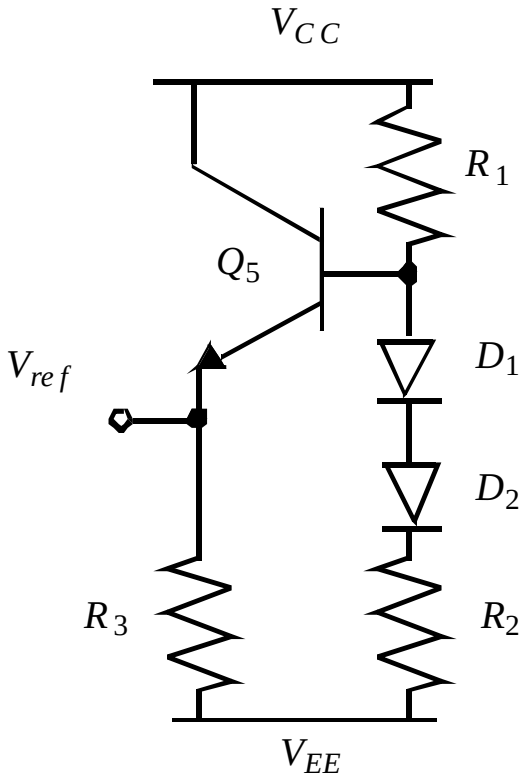
Differential

Complete ECL Gate



Emitter-follower output driver

The Bias Network



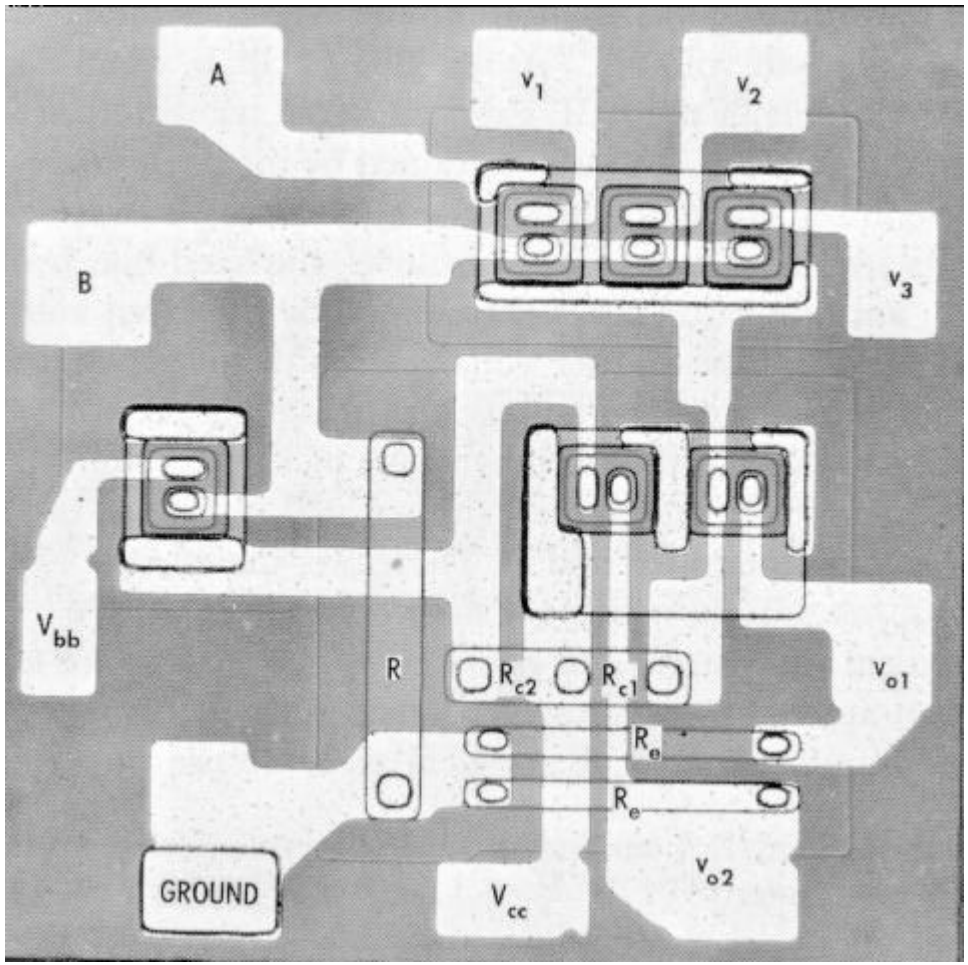
$$V_{ref} = V_{B5} - V_{BE(on)}$$

$$V_{B5} = V_{CC} - \frac{R_1}{R_1 + R_2}(V_{CC} - 2V_D - V_{EE})$$

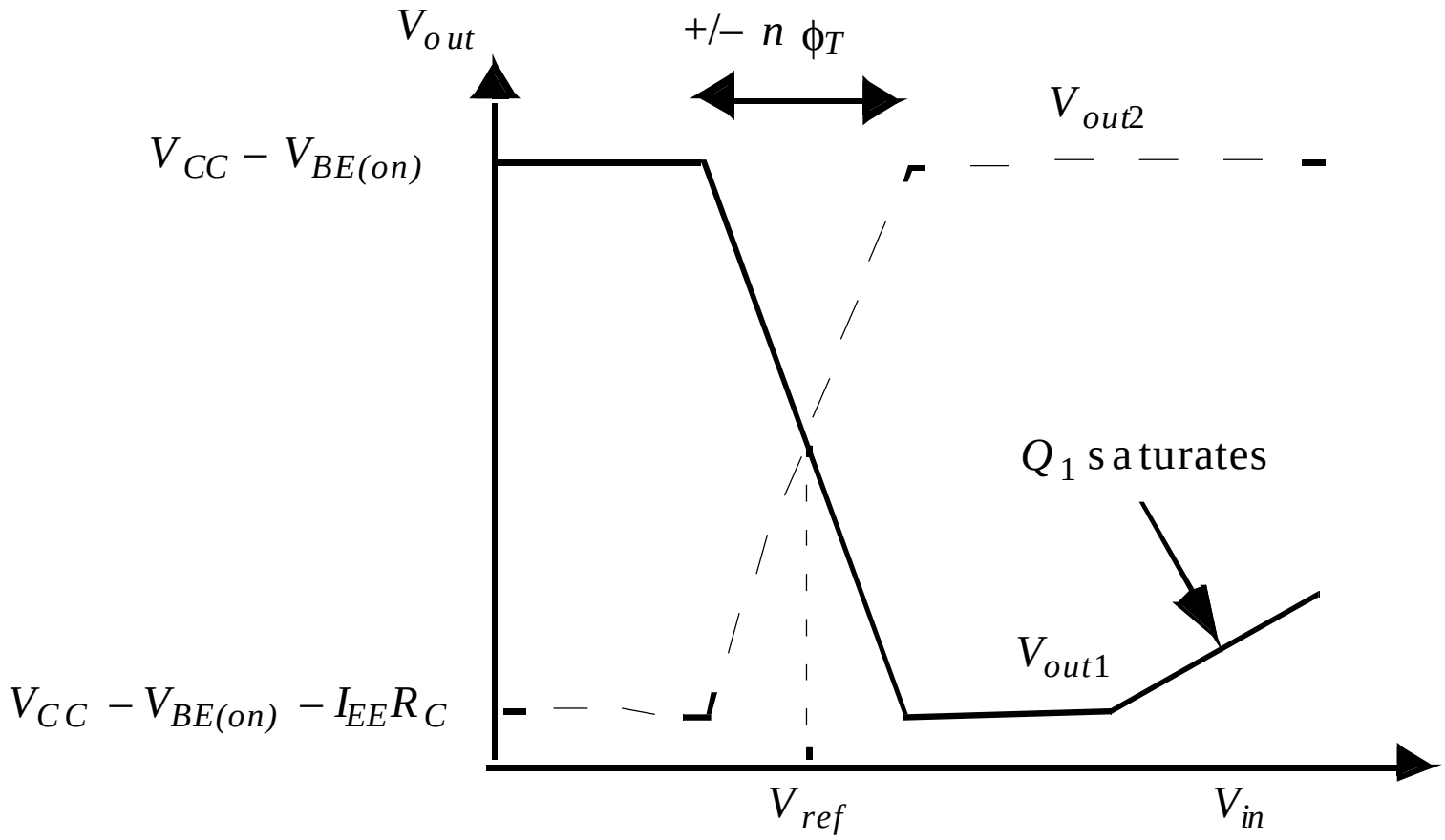
Issues:

- Temperature variations
- Device variations

Photomicrograph of early ECL Gate (1967)



ECL VTC



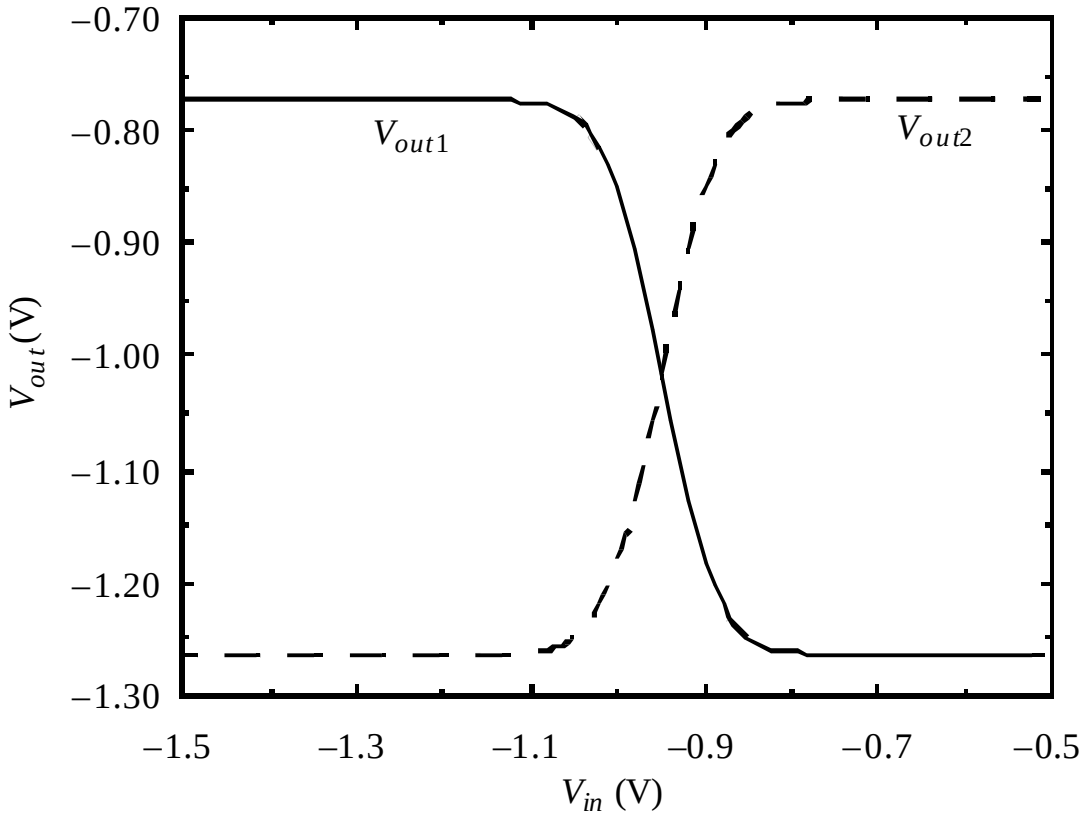
ECL VTC

$$V_{swing} = I_{EE} R_C$$

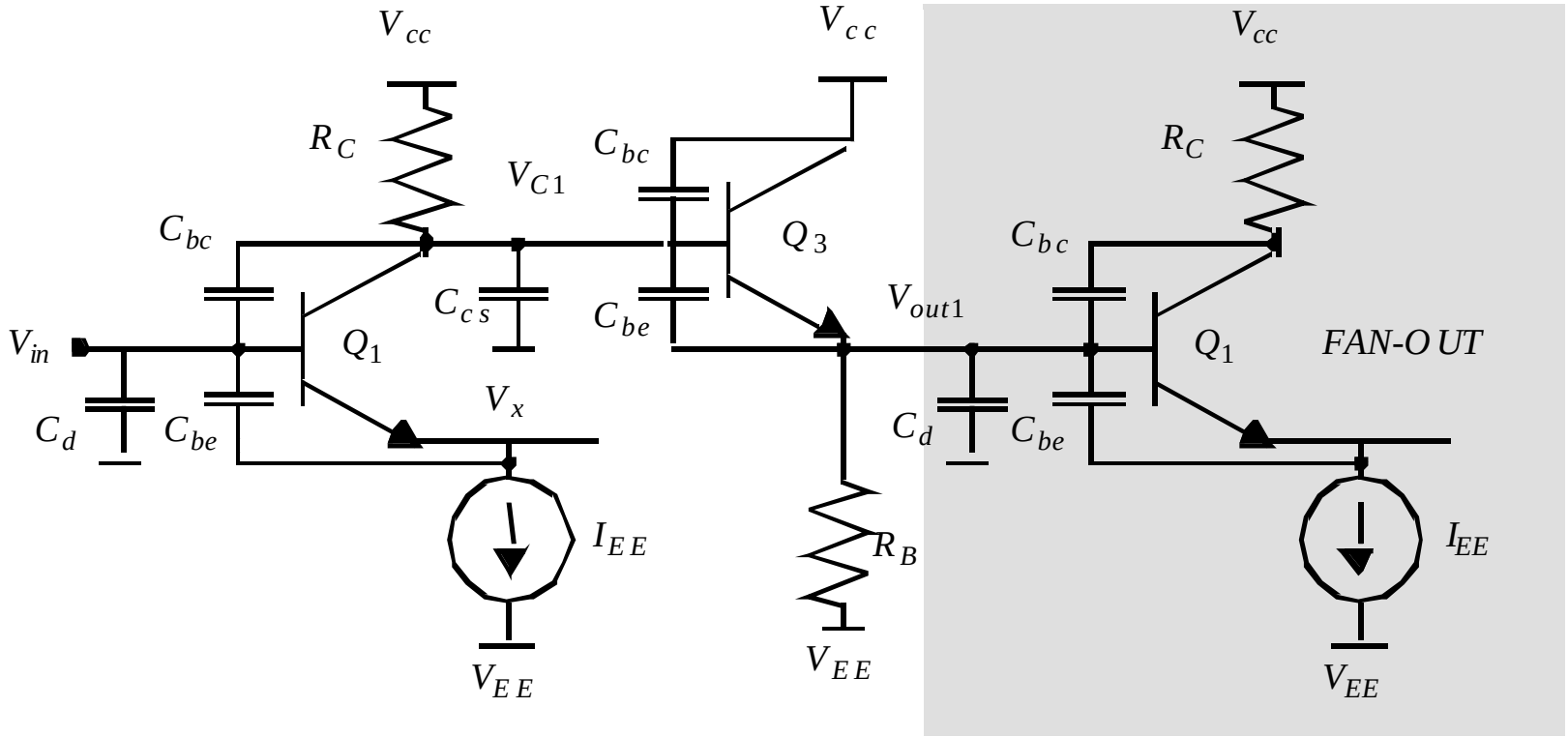
$$\frac{I_{C1}}{I_{EE}} = \frac{e^x}{1 + e^x} = \alpha = 0.01$$

$$V_{IL,IH} = V_{ref} \pm \phi_T ln\left(\frac{\alpha}{1 - \alpha}\right)$$

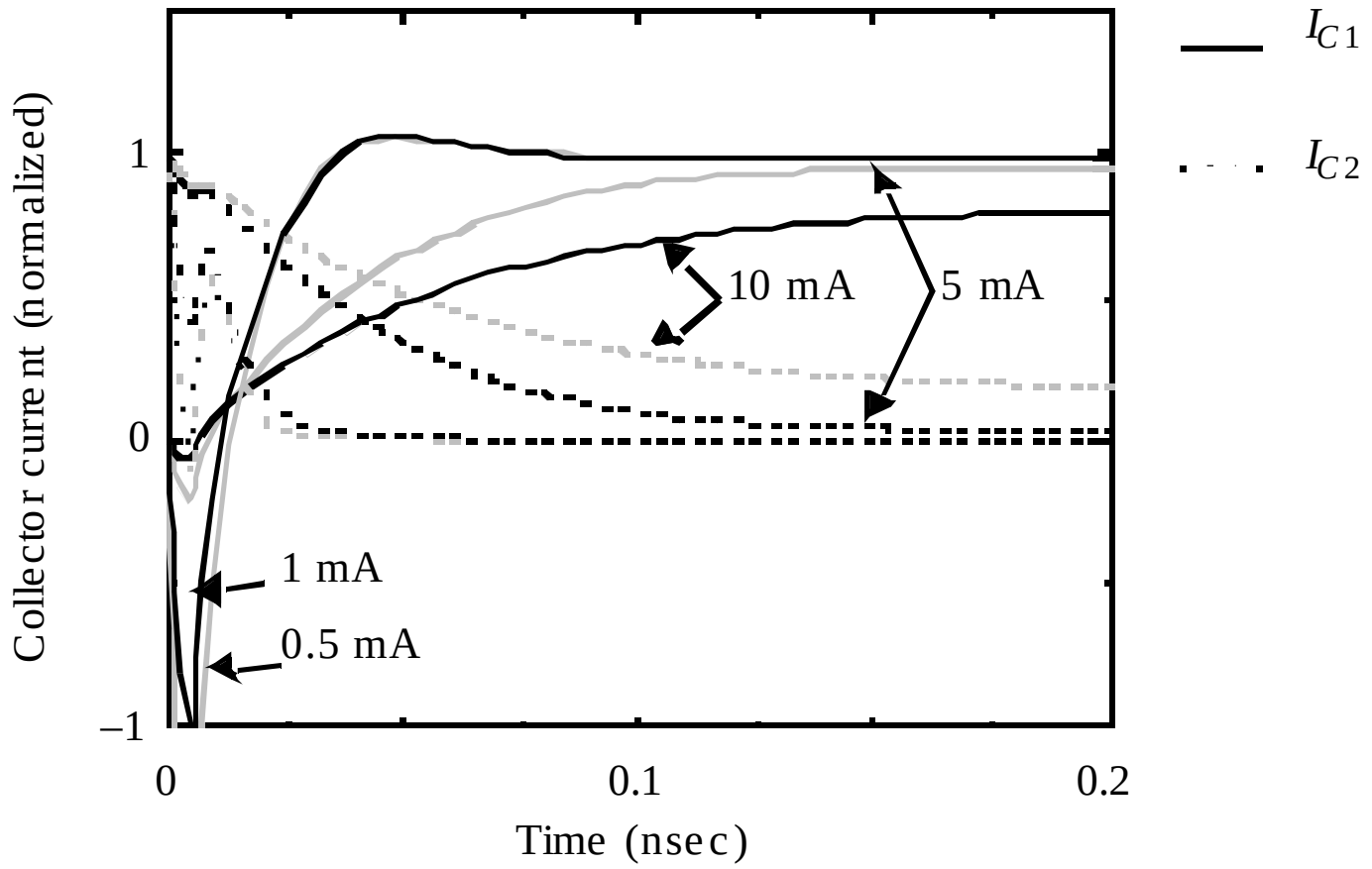
Simulated VTC of ECL Gate



ECL Gate with Single Fan-out



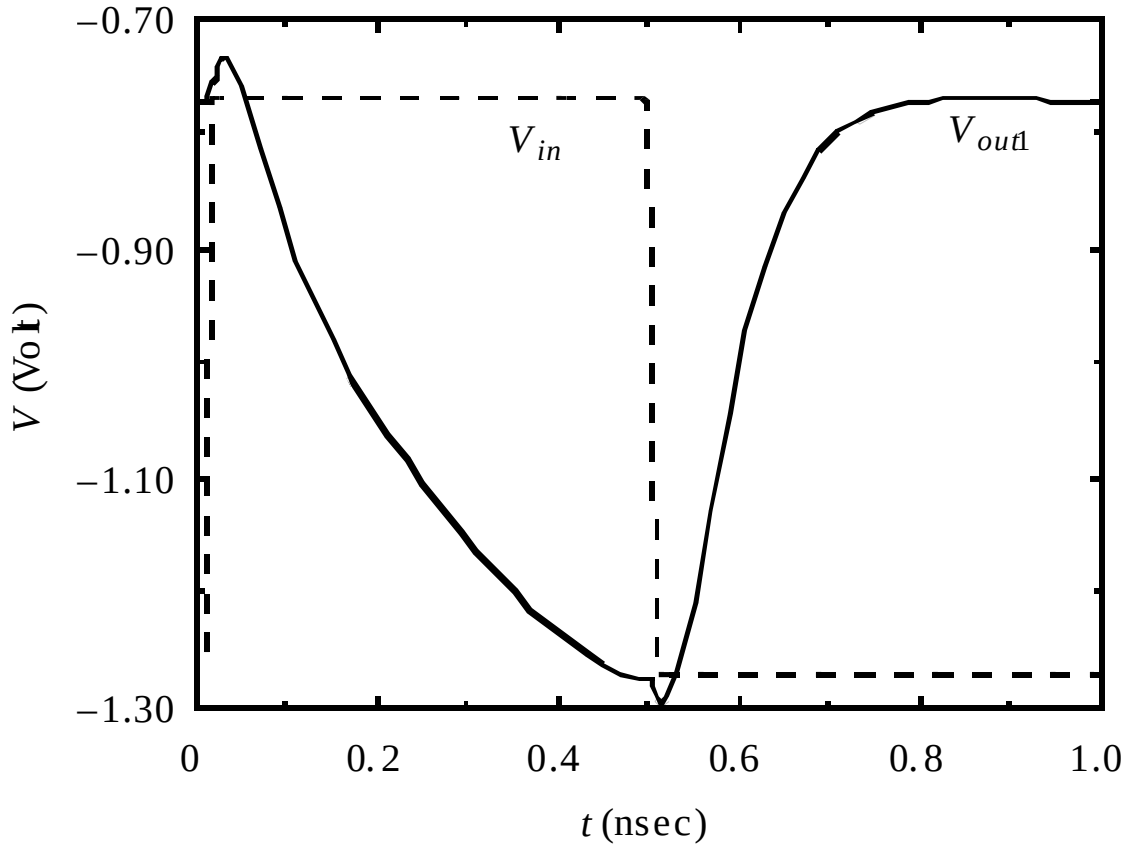
Simulated Collector Currents of Differential Pair



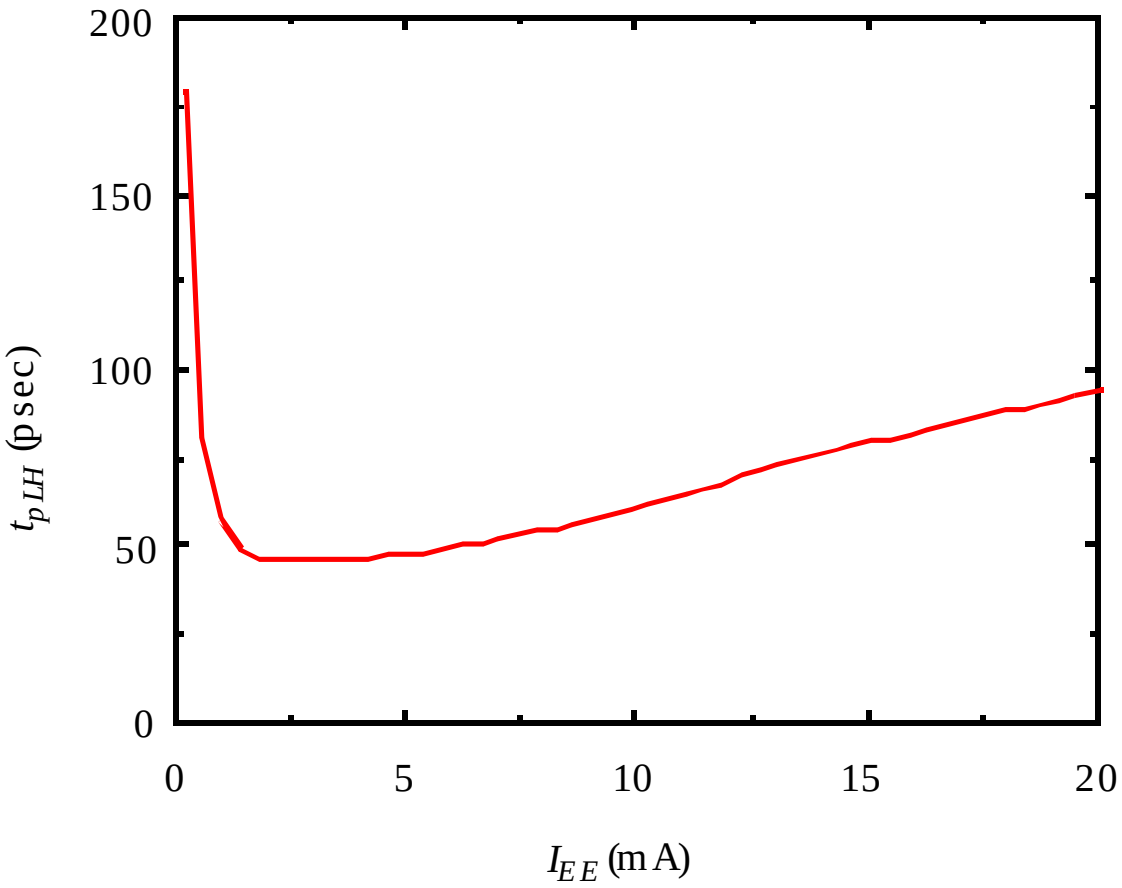
Propagation Delay of ECL Gate

		Switching the differential pair	Capacitive (dis)charge
t_{pHL}	$R_B C_L >> R_C C_c$	$r_B(2.2C_{inj} + \alpha C_{D1})$	$0.5 C_L R_B \left(\frac{V_{swing}}{V_{CC} - V_{EE}} \right)$
	$R_B C_L << R_C C_c$		$0.69 \left(\frac{R_C}{\beta_F + 1} \parallel R_B \right) (C_C(\beta_F + 1) + C_L)$
t_{pLH}		$r_B(2.2C_{inj} + \alpha C_{D1})$	$0.69 \left(\frac{R_C}{\beta_F + 1} \parallel R_B \right) (C_C(\beta_F + 1) + C_L)$

Simulated Transient Response of ECL Inverter



Propagation Delay as a Function of Bias Current



ECL Power Dissipation

$$P_{stat} = (V_{CC} - V_{EE})\left(I_{EE} + \frac{I_{bias}}{N} + 2\frac{\frac{V_{OH} + V_{OL}}{2} - V_{EE}}{R_B}\right)$$

$$P_{dyn} = C_T(V_{CC} - V_{EE})V_{swing}f$$

Scaling Model for Bipolar Inverter

Parameter	Scaling Factor
A_E	$1/S^2$
w_B	$1/S^{0.8}$
V_{supply} V_{swing}	1
J	S^2
I	1
C_d C_j	$1/S$
t_p	$1/S$
P	1

Bipolar Scaling