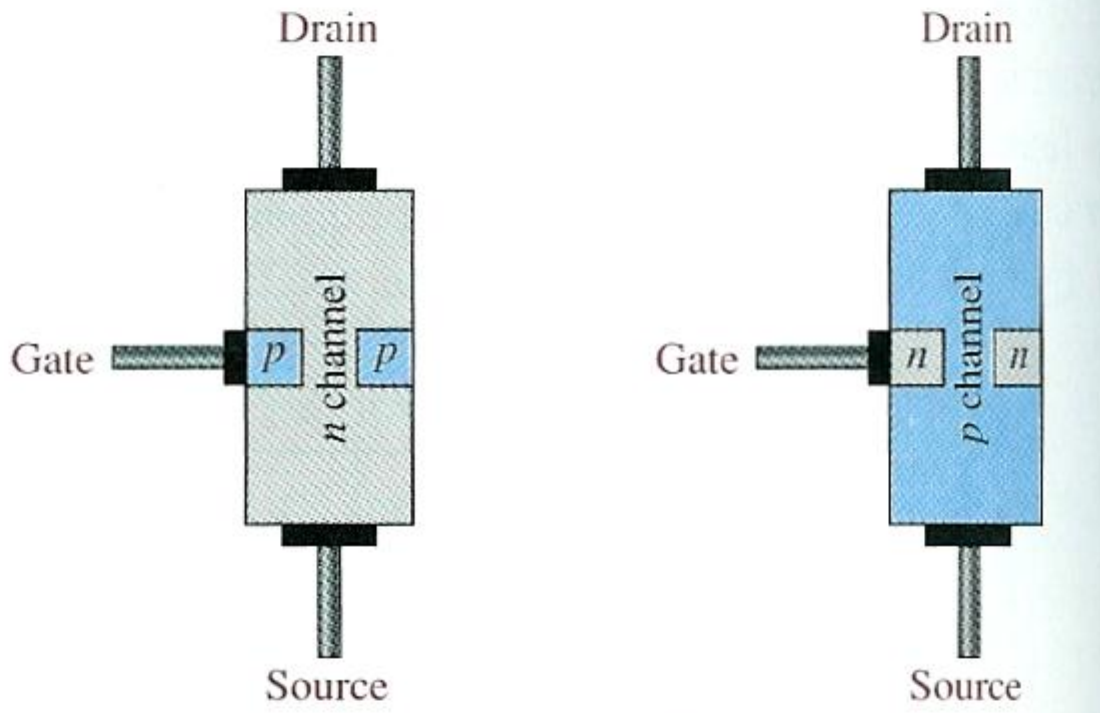
The JUNCTION FIELF EFFECT TRANSISTOR (JFET)

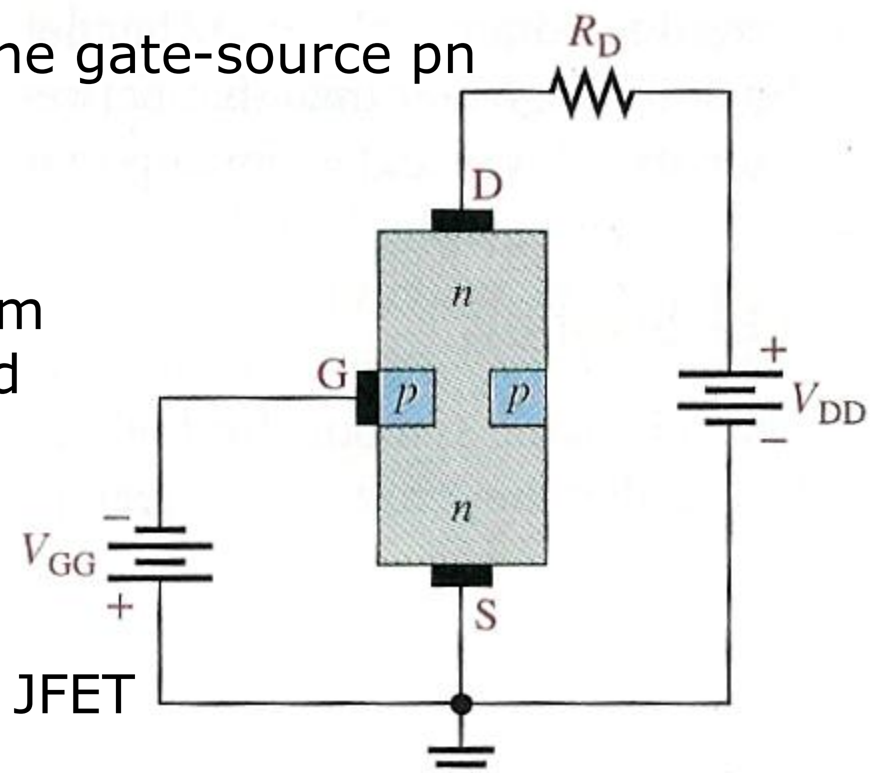
- n channel JFET
- p channel JFET



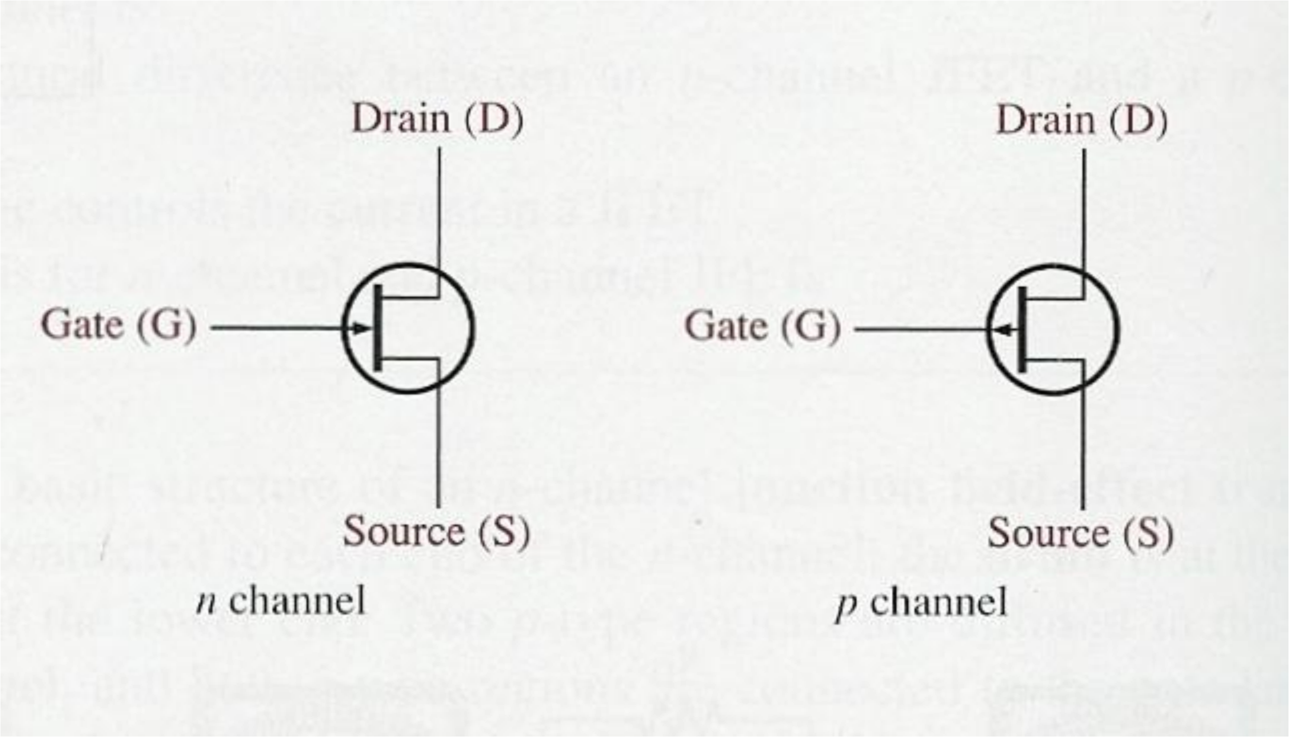
(a) *n* channel (b) *p* channel

The BIASED JFET

- VDD provides a drain-to-source voltage and supplies current from drain to source
- VGG sets the reverse-biased voltage between gate and source
- JFET is always operated with the gate-source pn junction reverse-biased.
- the gate current IG=0
- Input resistance
  Rin = VGG / IG = infinitive ohm
- Typical JFET has Rin is hundred of mega-ohm
- JFET is in application where a high input impedance is required
- one of the most importance of JFET is the source follower



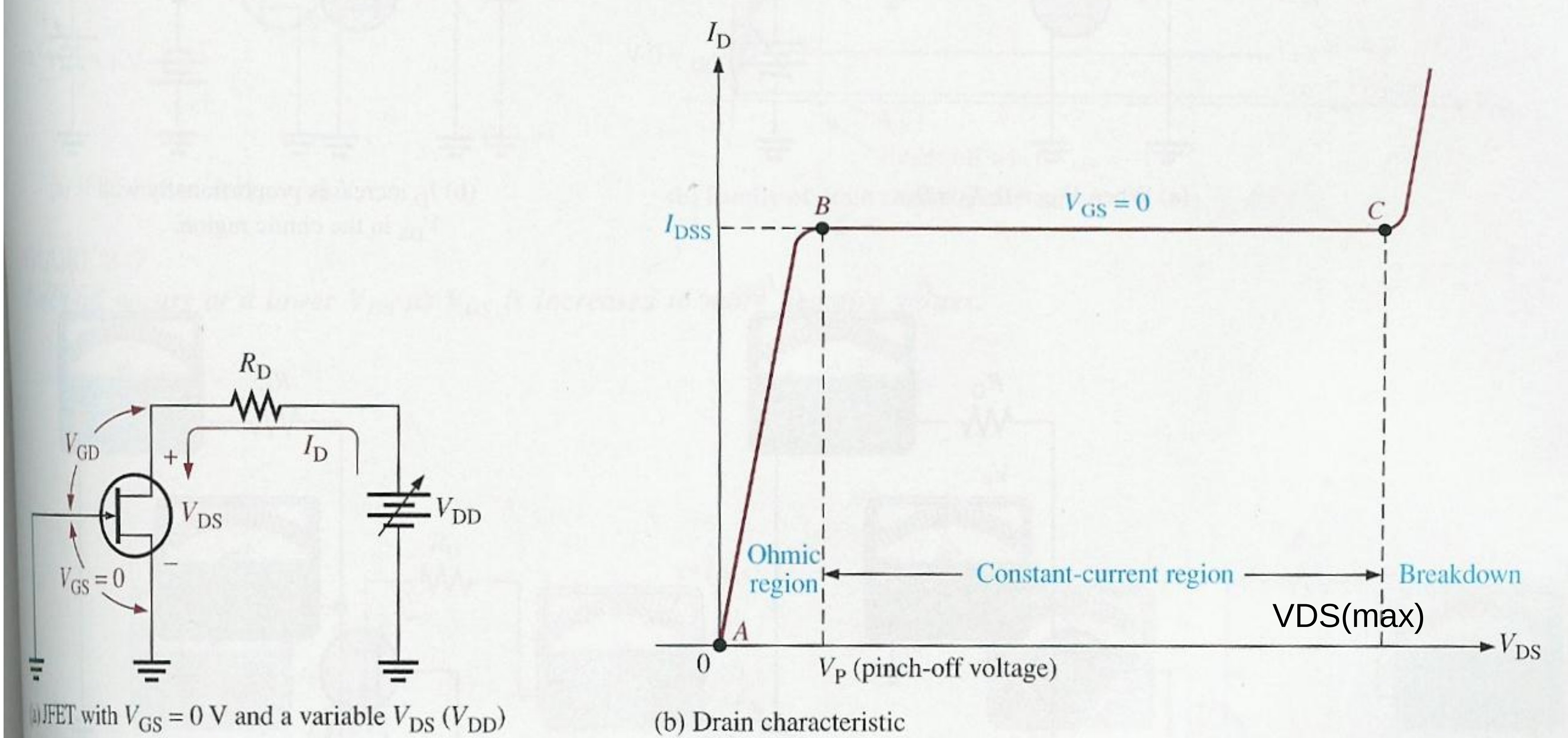
JFET schematic symbols



DRAIN CURVES

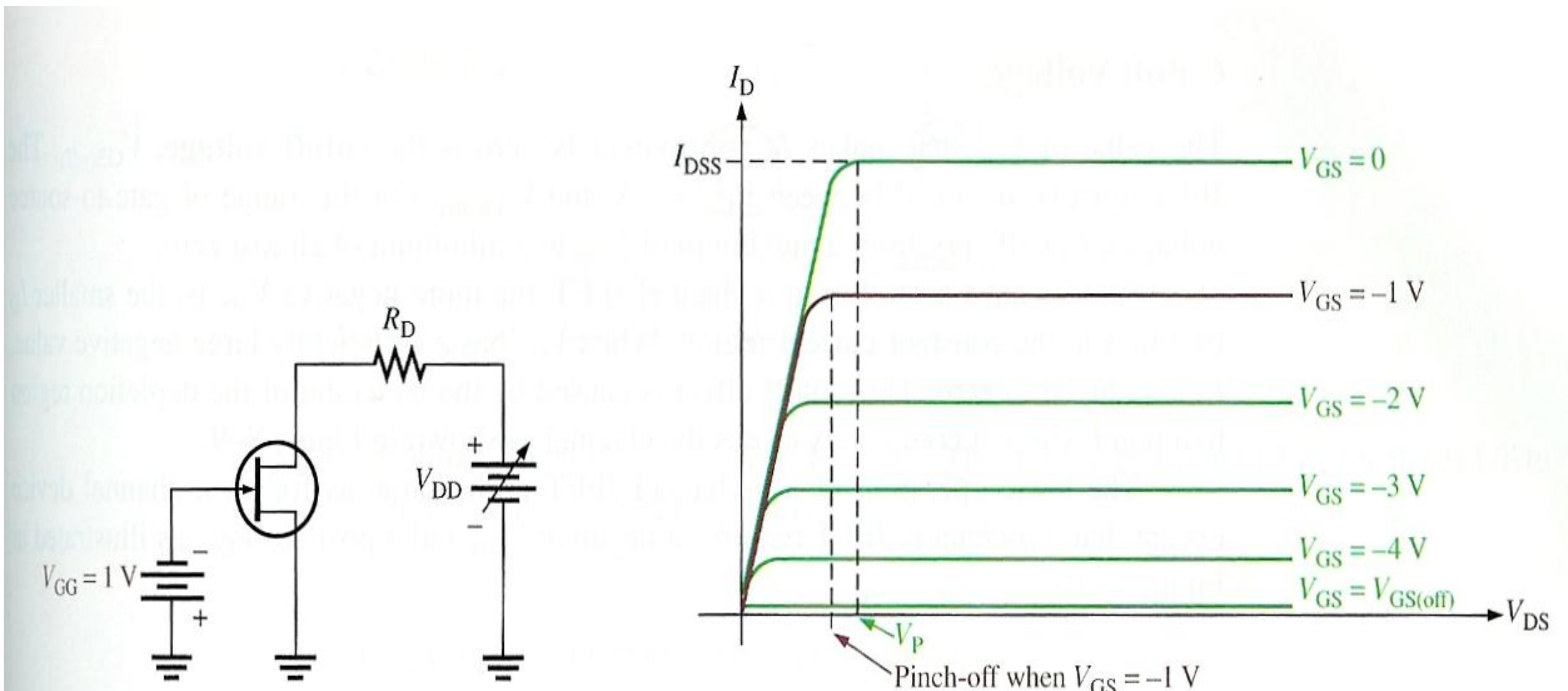
- The maximum drain current out of JFET occurs when the GATE-SOURCE voltage is zero
- The drain current is almost constant in the region between VP and VDS (max)
- If the drain voltage is too large, the JFET breaks down
- JFET acts like current source when it is operating along the almost horizontal part of the drain curve.
  (between minimum of VP and maximum of VDS (max))
- The minimum voltage of VP is called *PINCHOFF* voltage
- The maximum voltage VDS (max) is called *breakdown* voltage
- Between PINCHOFF and breakdown the JFET acts like current source with the value of IDSS.
- IDSS stands for the current from drain to source with shorted gate [VGS=0]
- **The OHMIC region**
- The almost vertical part of the drain curve is called OHMIC region, that
  equivalent to the saturation region of bipolar transistor

- When operated in the OHMIC region, the JFET acts as small resistor with the value is **RDS = VP / IDSS**
- **DRAIN CURVES**



(a) JFET with $V_{GS} = 0$ V and a variable V_{DS} (V_{DD})
(b) Drain characteristic

VGS controls ID



(a) JFET biased at $V_{GS} = -1$ V

(b) Family of drain characteristic curves

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Cutoff Voltage

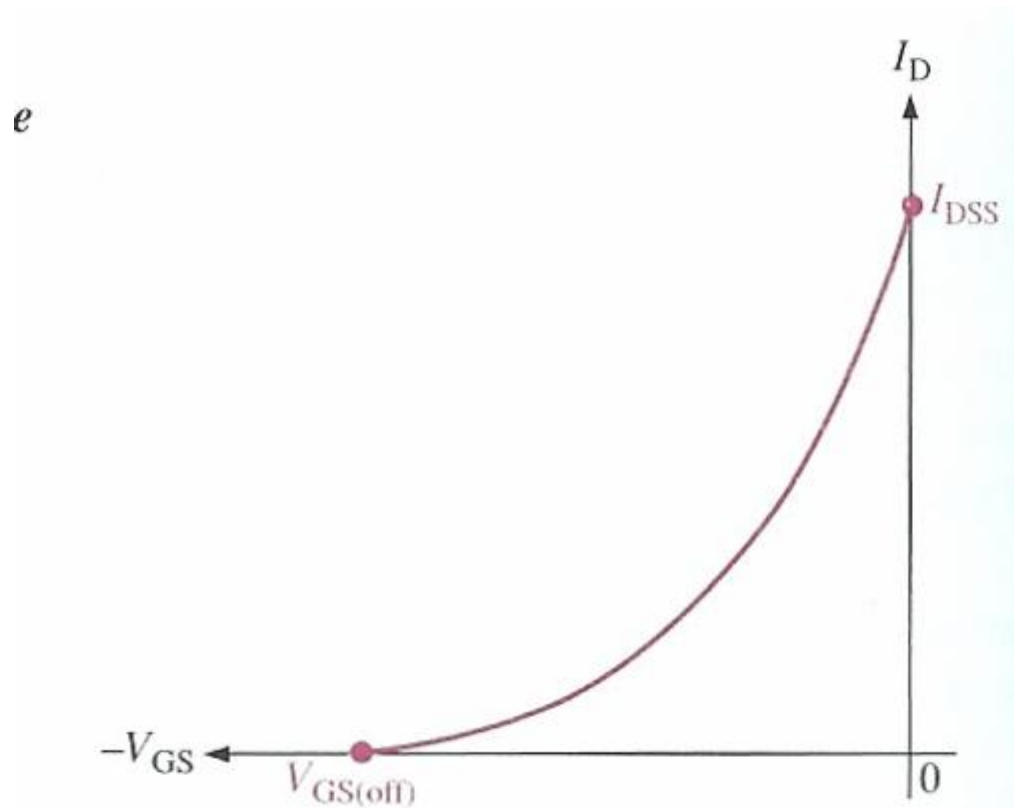
- The value of VGS that makes ID approximately zero is the cutoff voltage, VGS(off).
- The JFET must be operated between VGS=0 V and VGS(off)

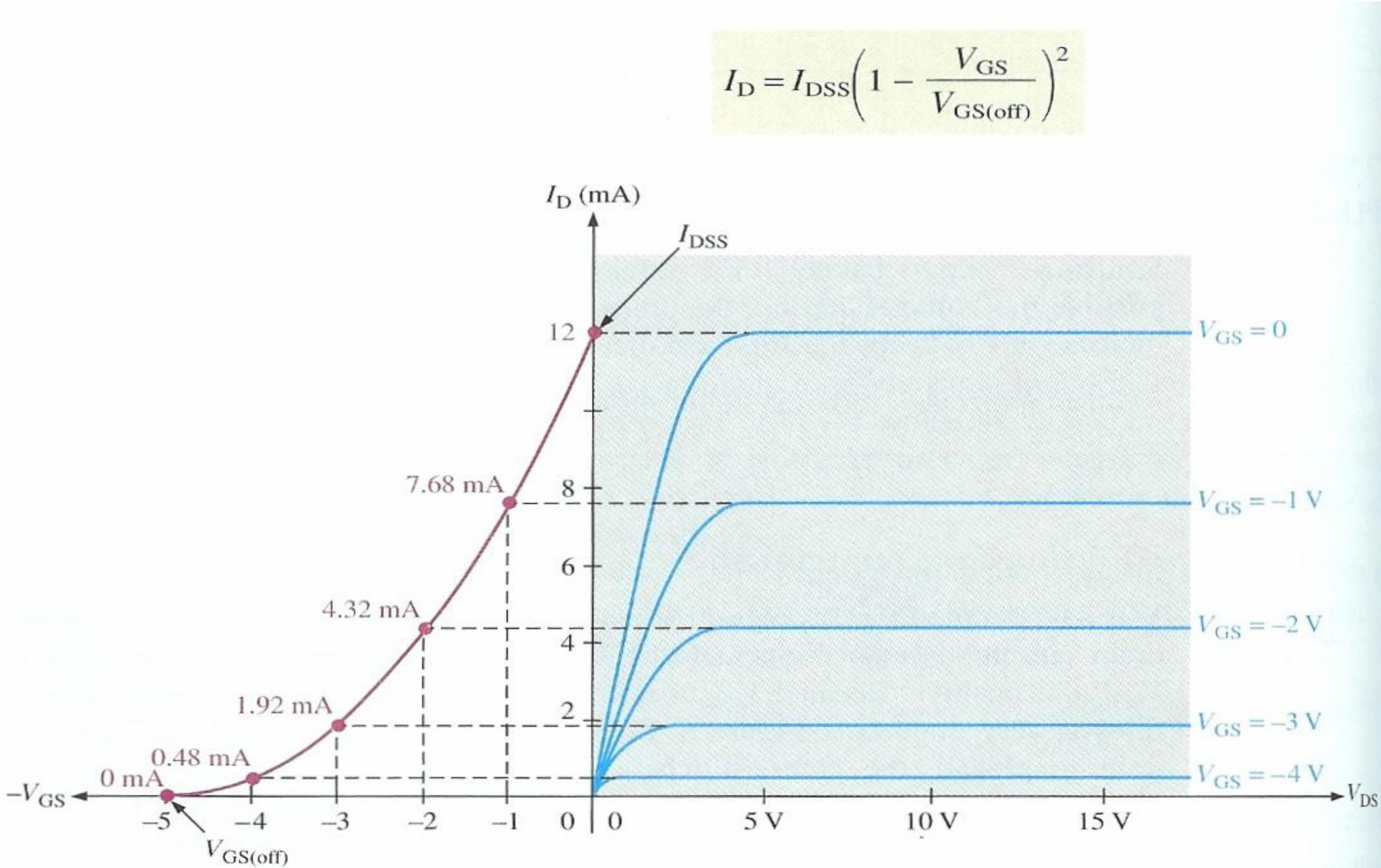
Comparison of Pinch-off and cutoff

- Vp is the value of VDS at which the drain current becomes constant and is always measured at VGS=0
- VGS and VP are always equal in magnitude but opposite in sign.
- Data sheet usually will give either VGS(off) or VP but not both

JFET TRANSFER CHARACTERISTIC

- Remember ID=0 when VGS=VGS(off) and
- ID=IDSS When VGS=0




$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$
I_D (mA)
I_{DSS}
12
8
6
4
2
7.68 mA
4.32 mA
1.92 mA
0.48 mA
0 mA
$-V_{GS}$
–5
–4
–3
–2
–1
0
$V_{GS(off)}$
0
5 V
10 V
15 V
V_{DS}
$V_{GS} = 0$
$V_{GS} = -1$ V
$V_{GS} = -2$ V
$V_{GS} = -3$ V
$V_{GS} = -4$ V

Example#3:

The data sheet of JFET 2N5459 indicates that typically IDSS=9 mA and VGS(off)=-8V(maximum). Determine the drain current for VGS=0V, -1V, and -4V.

Solution:

JFET FORWARD TRANSCONDUCTANCE

The forward transfer conductance gm is the change in drain current (ΔID) for a given change in gate-to-source voltage (ΔVGS) with the drain-to-source voltage constant. It is expressed as a ratio and has the unit of siemens (S)

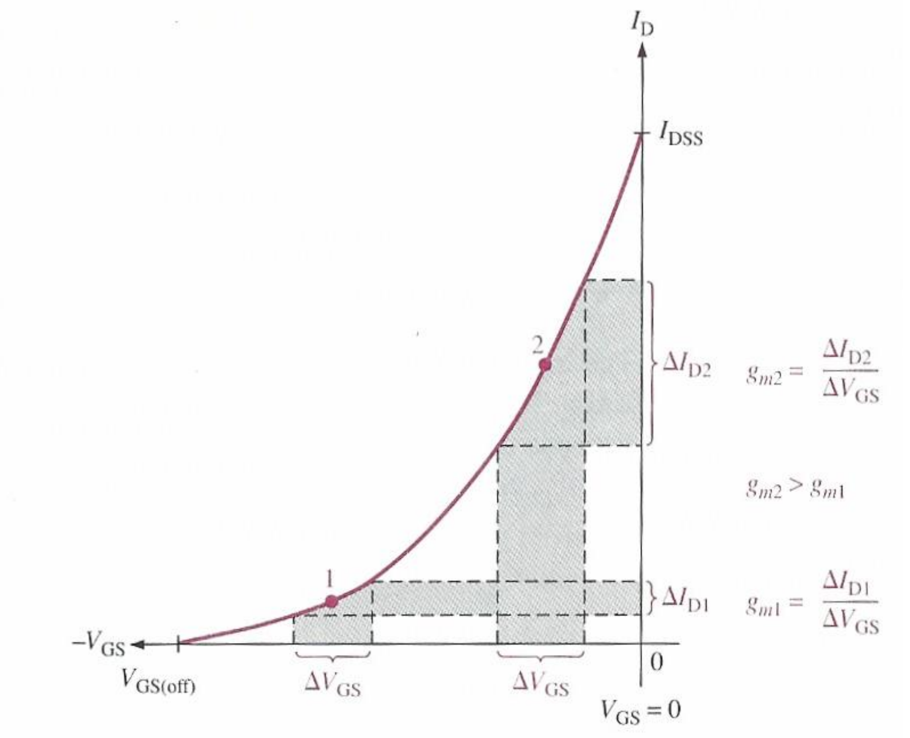
$$gm = (\Delta ID) / \Delta VGS$$

- Data sheet normally gives the value of g_m measured at VGS=0 (g_{m0})
- Given gm0 then calculate gm at any point on the transfer characteristic curve, using the following formula:

$g_m = g_{m0}(1- VGS/ VGS(off))$

- If value of gm0 is not available, then calculate gm0 as following:

$g_{m0} = 2IDSS/|VGS(off)|$



- **INPUT RESISTANCE AND CAPACITANCE:**

$$R_{IN} = | V_{GS} / I_{GSS} |$$

Example#5:

A certain JFET has an IGSS of 2 nA for VGS=-20V. Determine the input resistance

Solution:

$$R_{IN} = | V_{GS} / I_{GSS} | = 10000 \text{ MegaOhm}$$

- **DRAIN-TO-SOURCE RESISTANCE**

$$r_d = \Delta V_{DS} / \Delta I_D$$

JFET BIASING

- SELF-BIAS
- **For p-channel**:

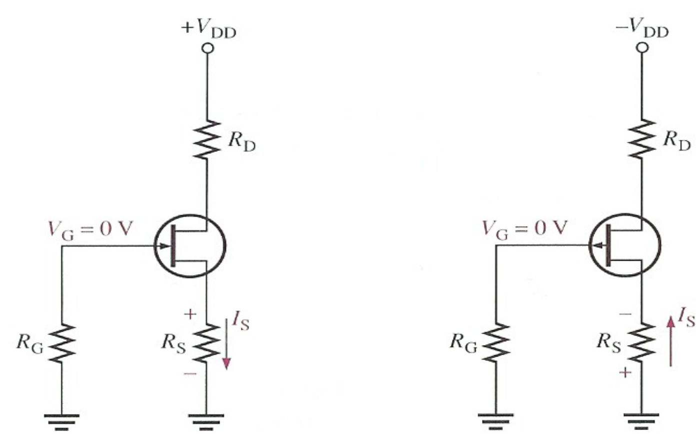
$VGS = +I_D \times R_S$

$VD = VDD - I_D R_D$

$VDS = VD - VS = VDD - ID(R_D + R_S)$

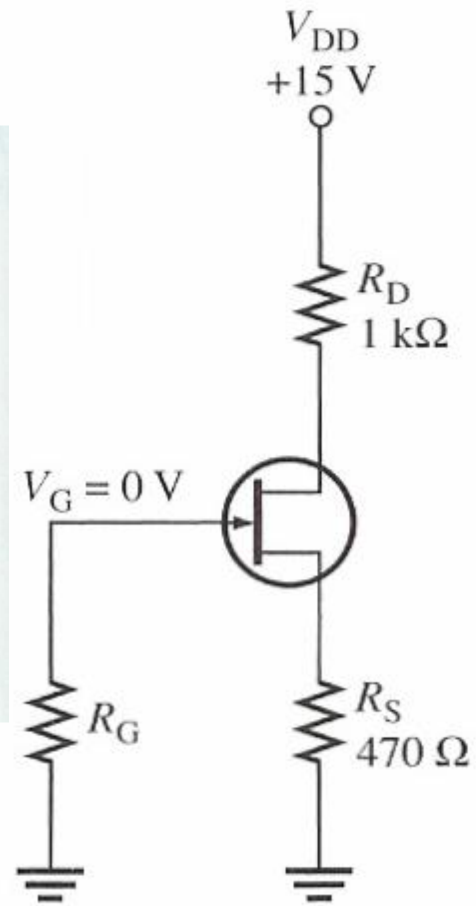
$$V_{GS} = V_G - V_S = 0 - I_D R_S$$

$$V_{GS} = -I_D R_S$$



(a) n channel (b) p channel

Example#6:For the circuit shown, find VDS and VGS, given that ID=5mA



Solution

$$V_S = I_D R_S = (5\text{ mA})(470\ \Omega) = 2.35\text{ V}$$

$$V_D = V_{DD} - I_D R_D = 15\text{ V} - (5\text{ mA})(1\text{ k}\Omega) = 15\text{ V} - 5\text{ V} = 10\text{ V}$$

Therefore,

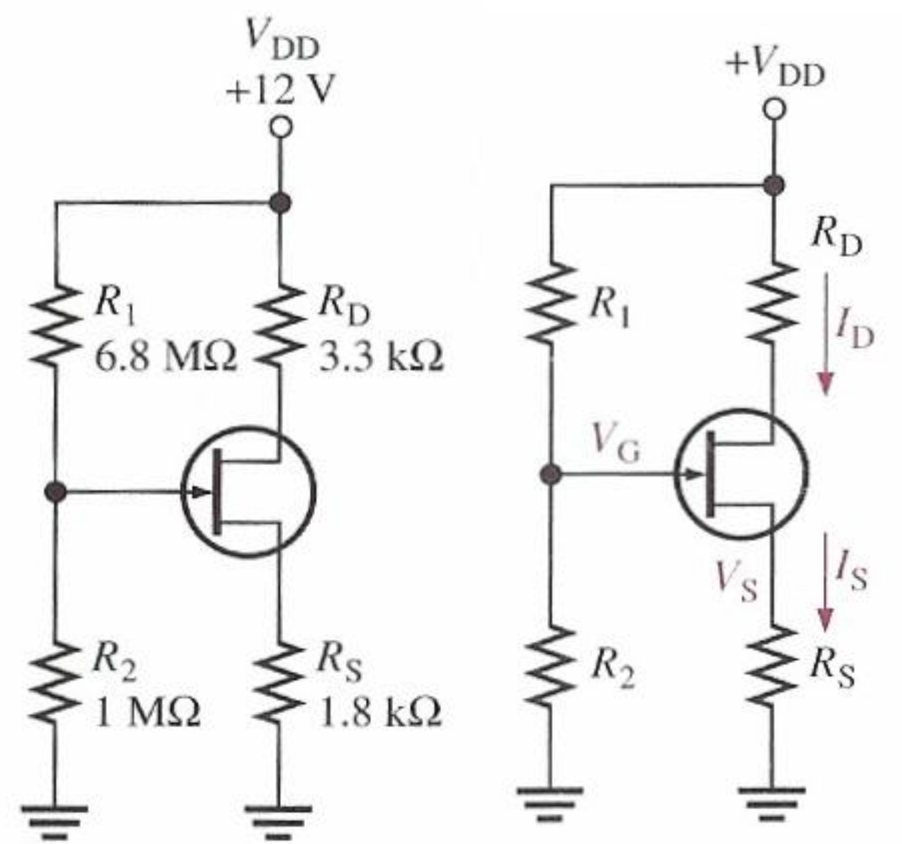
$$V_{DS} = V_D - V_S = 10\text{ V} - 2.35\text{ V} = 7.65\text{ V}$$

Since $V_G = 0$ V,

$$V_{GS} = V_G - V_S = 0\text{ V} - 2.35\text{ V} = -2.35\text{ V}$$

Voltage-Divider Bias

- $V_S = I_D \times R_S$ or $I_D = V_S / R$
- $V_{GS} = V_G - V_S$
- $V_S = V_G - V_{GS}$
- $I_D = V_S / R_S = (V_G - V_{GS}) /$



Example#8:
Determine ID and VGS for the
With voltage divider shown
Given that VD=7V.
Solution:

Graphical Analysis of a JFET with voltage divider bias

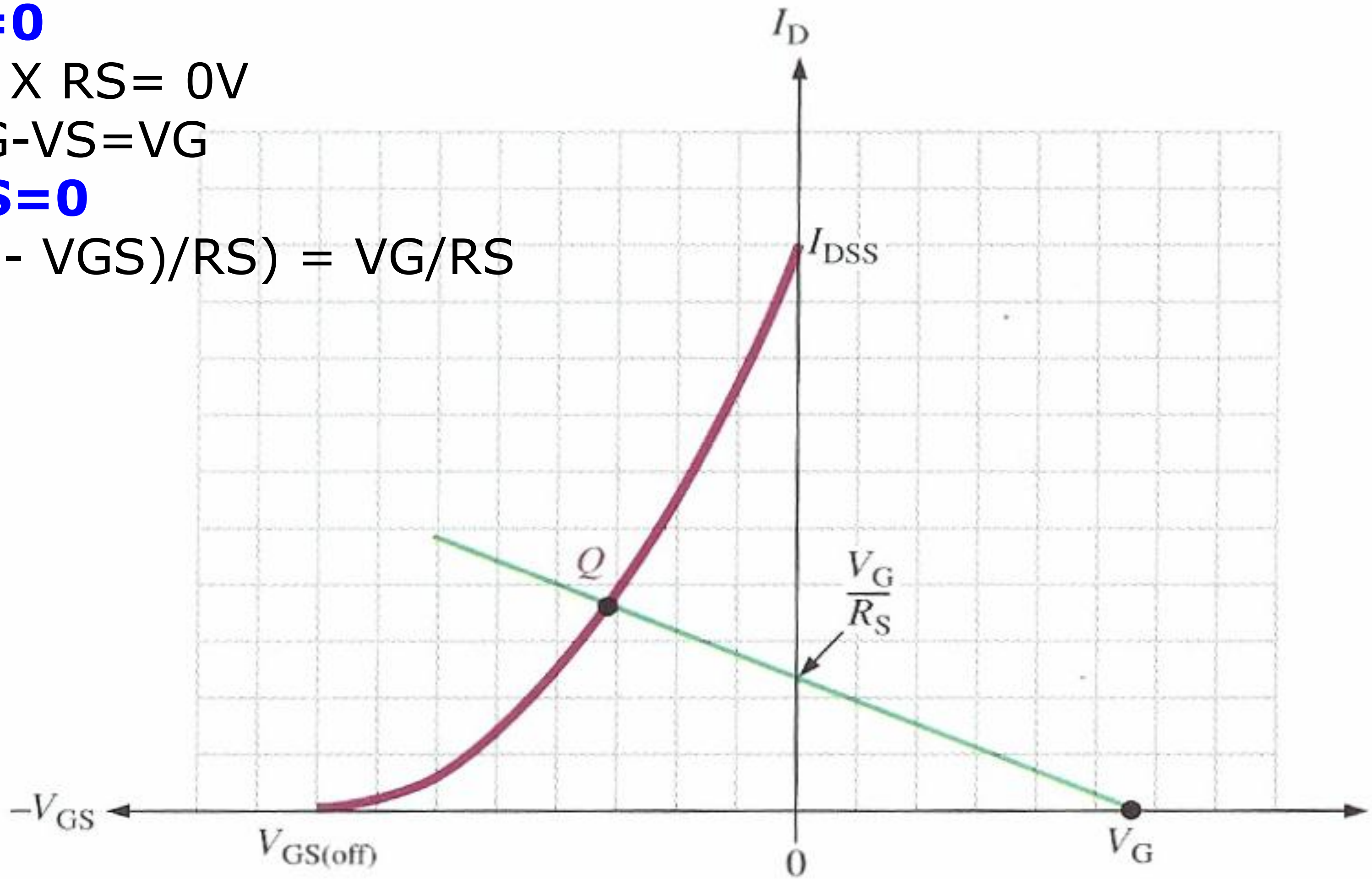
For ID=0

VS = ID X RS= 0V

VGS=VG-VS=VG

For VGS=0

ID= (VG- VGS)/RS) = VG/RS



Determine the Q-point for the JFET with voltage-divider bias in Figure 8–26(a), give the transfer characteristic curve in Figure 8–26(b).

Solution First, establish the two points for the bias line.

For $I_D = 0$,

$$V_{GS} = V_G = \left(\frac{R_2}{R_1 + R_2}\right)V_{DD} = \left(\frac{2.2\ \text{M}\Omega}{4.4\ \text{M}\Omega}\right)8\ \text{V} = 4\ \text{V}$$

The first point is at $I_D = 0$ and $V_{GS} = 4$ V.

For $V_{GS} = 0$,

$$I_D = \frac{V_G - V_{GS}}{R_S} = \frac{V_G}{R_S} = \frac{4\ \text{V}}{3.3\ \text{k}\Omega} = 1.2\ \text{mA}$$

The second point is at $I_D = 1.2$ mA and $V_{GS} = 0$.

The load line is drawn in Figure 8–26(b), and the Q-point values of $I_D = 1.7$ mA and $V_{GS} = -2$ V are picked off the graph, as indicated.

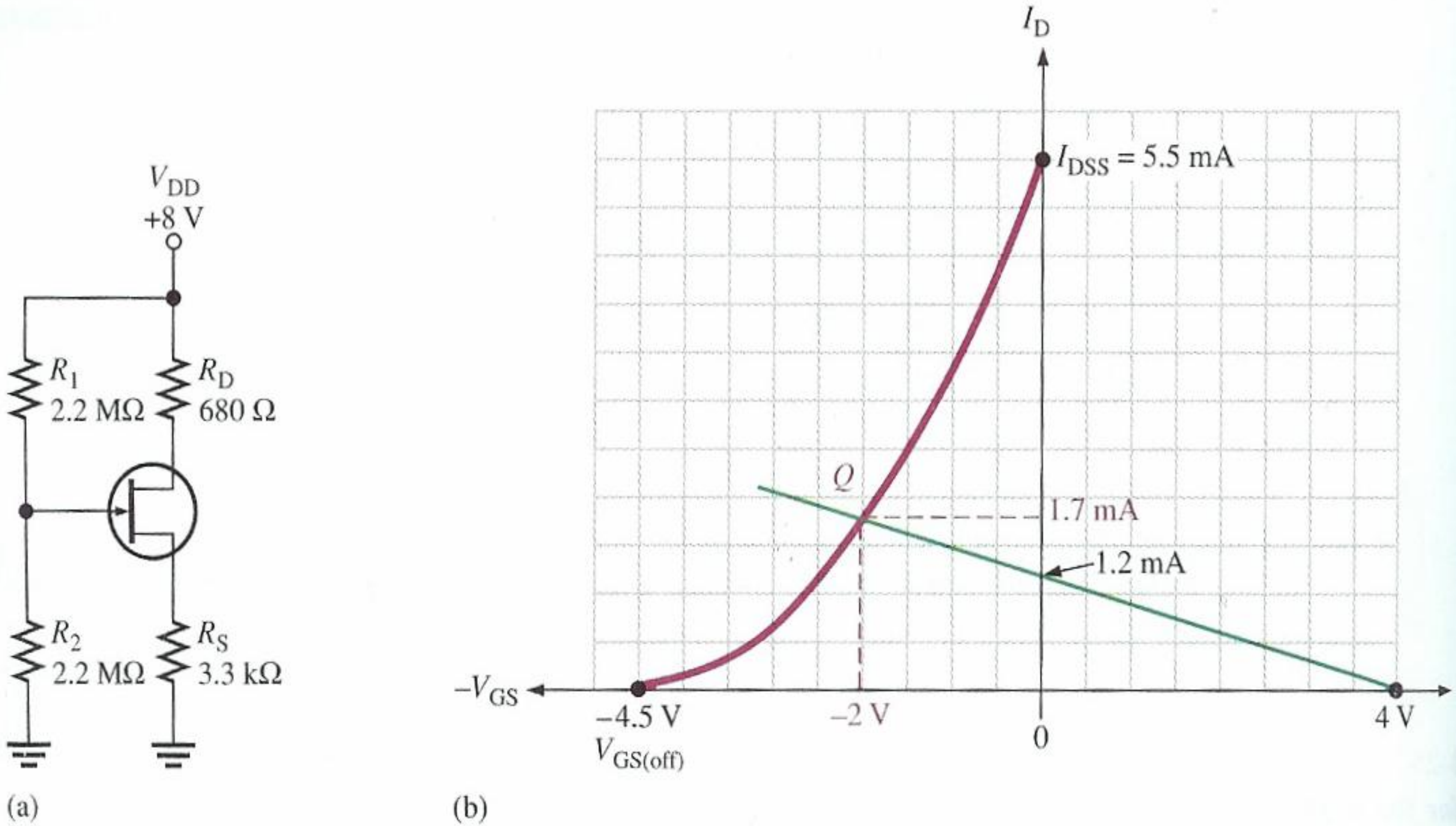

V_{DD}
+8 V
R_1
2.2 MΩ
R_D
680 Ω
R_2
2.2 MΩ
R_S
3.3 kΩ
(a)
I_D
I_{DSS} = 5.5 mA
Q
1.7 mA
1.2 mA
$-V_{GS}$
−4.5 V
$V_{GS(off)}$
−2 V
0
4 V
(b)

FIGURE 8–26

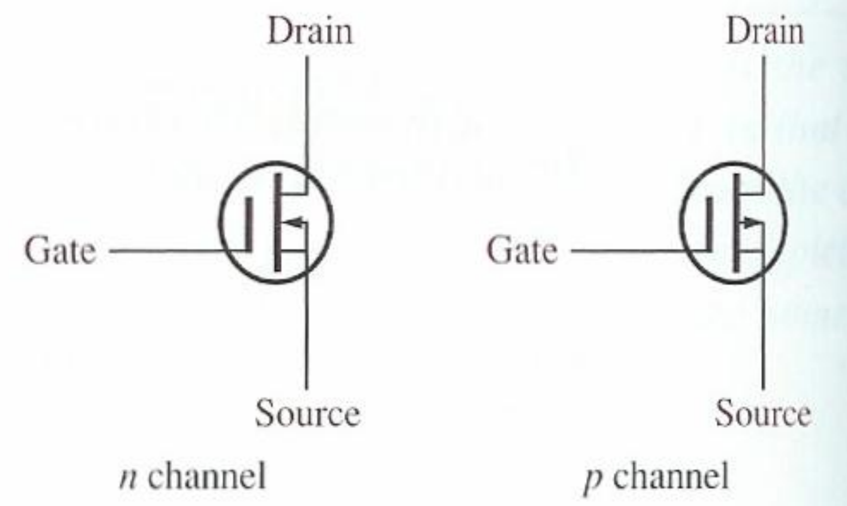
THE METAL OXIDE SEMICONDUCTOR FET (MOSFET)

- The D-MOSFET can be operated of two modes:

1. The depletion mode
2. the enhancement mode

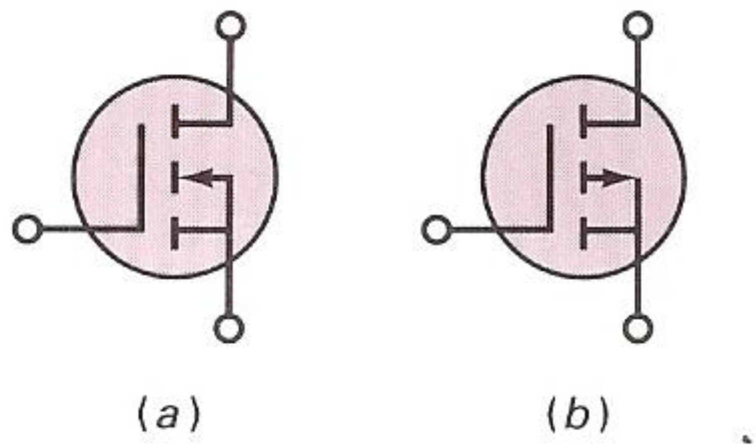
Sometimes called
Depletion enhancement MOSFET

- Either positive or negative Gate voltage can be applied
- Depletion mode: when negative gate-to-source voltage is applied.
- enhancement mode: when positive gate-to-source voltage is applied.
- Generally operate in the depletion mode



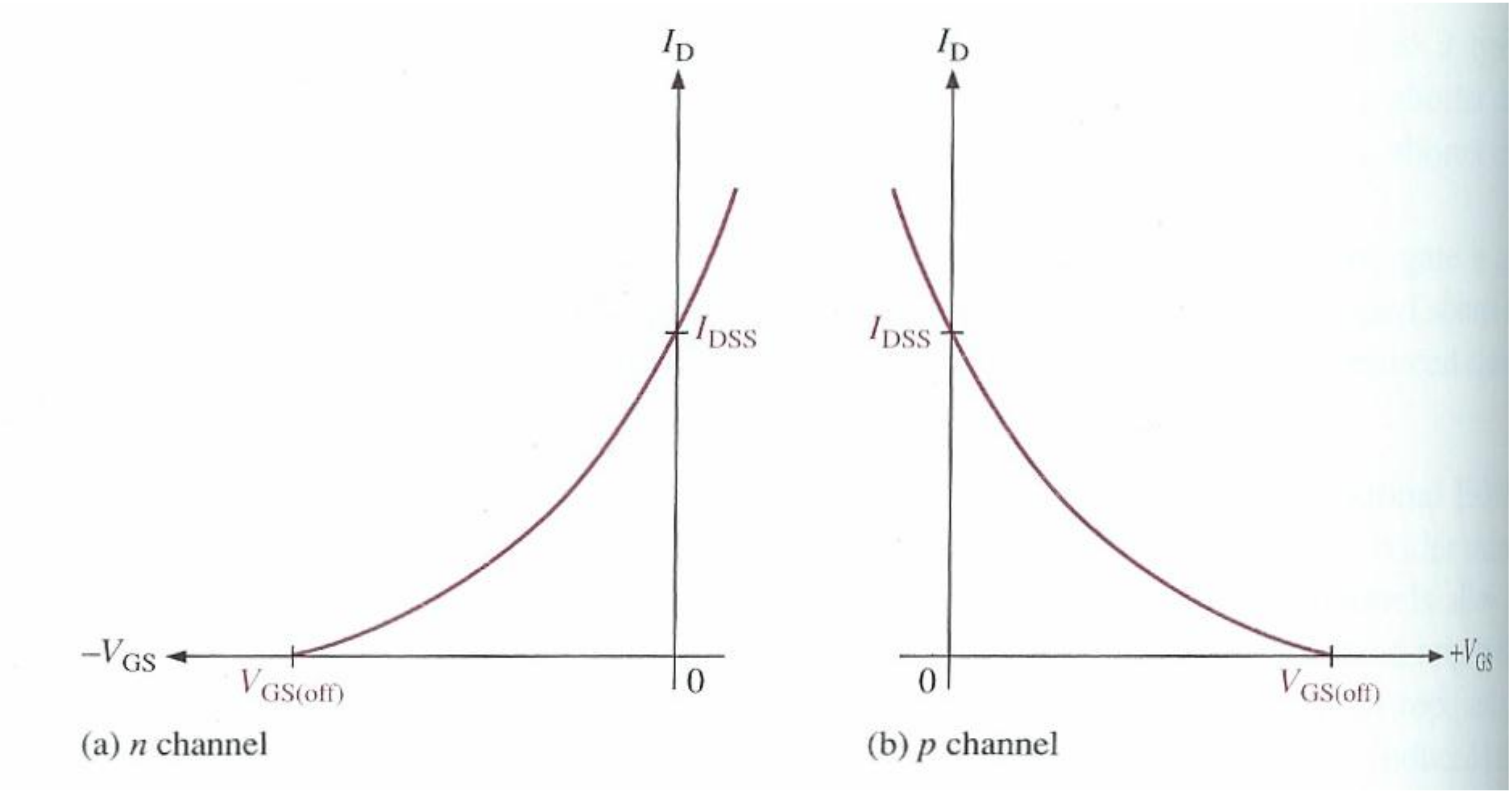
Enhancement MOSFET (E-MOSFET)

- Operates only in the enhancement mode



Schematic symbols: (*a*) *n*-channel; (*b*) *p*-channel.

- N-channel required positive gate-to-source voltage
- P-channel required negative gate-to-source voltage
- Equation transfer characteristic curve differs from that of JFET and D-MOSFET



D-MOSFET transfer characteristic curves.

Example:

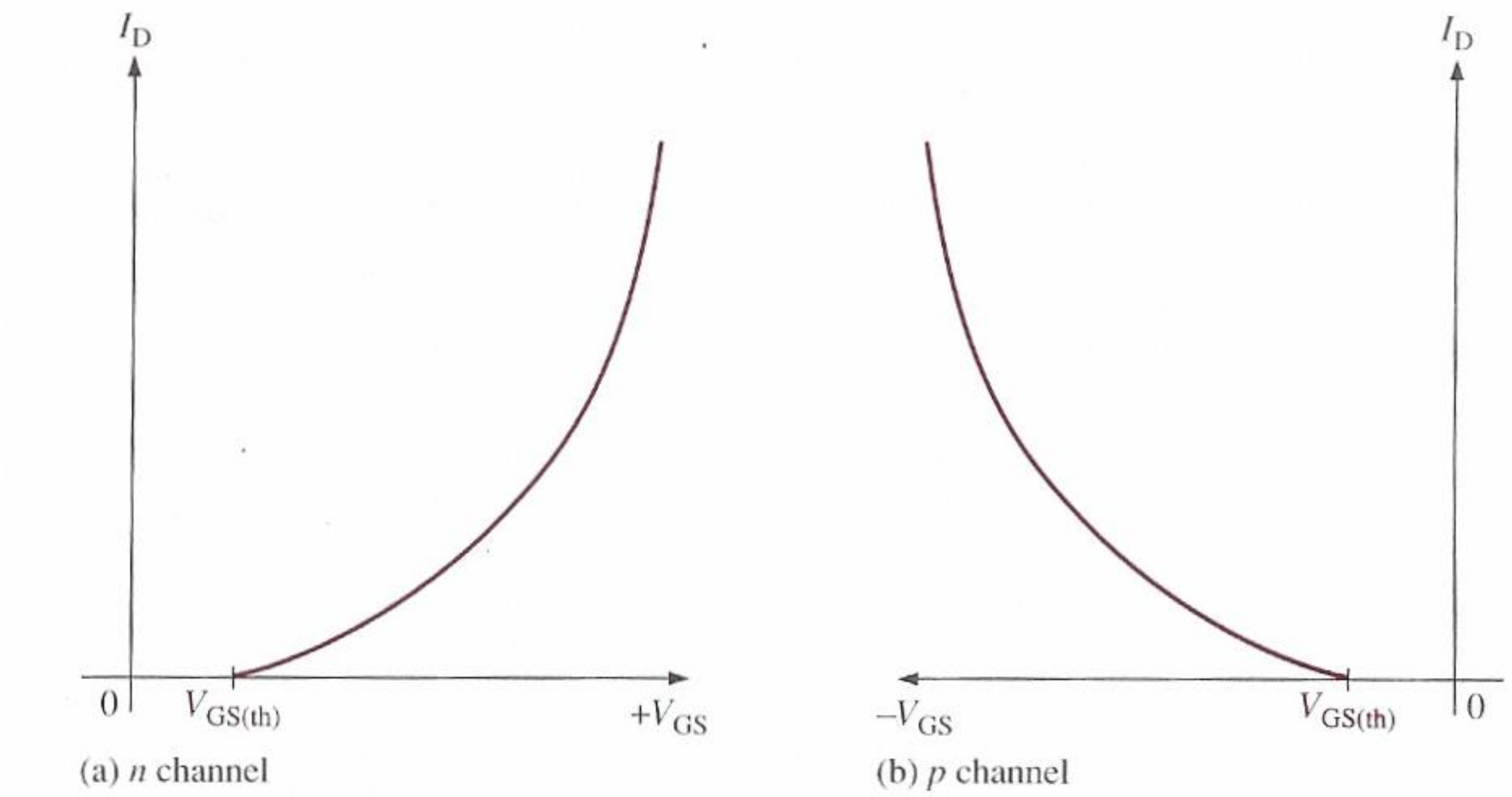
For a certain D-MOSFET, IDSS = 10 mA and VGS(off) = -8 V.

1. Is this an n-channel or p-channel?
2. Calculate ID at VGS=-3 V
3. Calculate ID at VGS=+3 V

Related Exercise:

For a certain D-MOSFET, IDSS=18 mA and VGS(OFF)=+10 V

1. Is this an n-channel or p-channel?
2. Calculate ID at VGS=+4 V
3. Calculate ID at VGS=-4 V



E-MOSFET transfer characteristic curves.

Enhancement MOSFET (E-MOSFET) continue

- The equation for the E-MOSFET transfer characteristic is:

  $$I_D = K\ (\ V_{GS} - V_{GS(th)}\ )^2$$

- the constant K depends on the particular MOSFET
- Can be determined from data sheet by taking the specified value of ID, called ID(ON) at the given value of VGS

Example:

The data sheet of a 2N7008 E-MOSFET gives ID(ON)=500 miiliAmp at VGS=10 V and Vth=1 V . Determine the drain current for VGS=5 V.

Solution:

Related Exercise:

The data sheet of a 2N7008 E-MOSFET gives ID(ON)=100 miiliAmp at VGS=8 V and VGS(th)=4 V . Determine the drain current for VGS=6 V.

HANDLING Precautions:

- All MOS devices are subject to damage from electrostatic discharge (ESD)
- MOS devices should be shipped and stored in conductive foam
- All instruments and metal benches used in assembly or test should be connected to earth GND.
- The assembler's or handler's wrist should be connected to earth GND with the length of wire and a high value series resistor.
- Never remove an MOS device from the circuit while power is ON
- Do not apply signals while the DC power is OFF

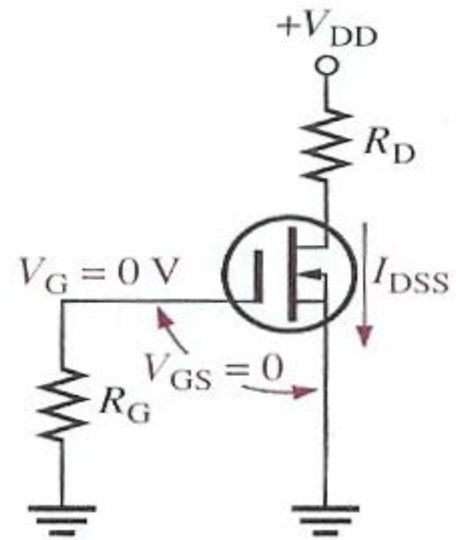
MOSFET BIASING

1. D-MOSFET Biasing

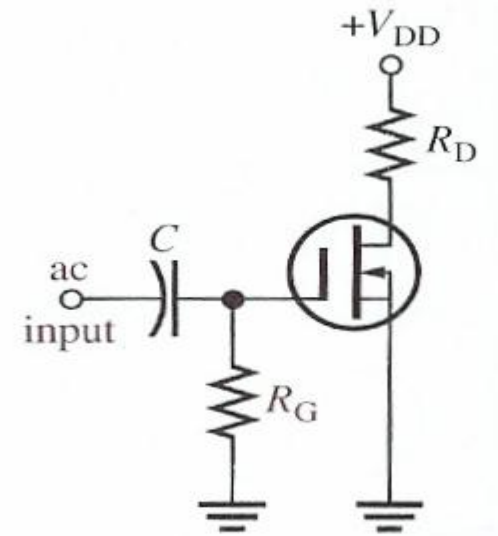
The circuit MOSFET with zero bias shown.

VGS=0 and ID=IDSS

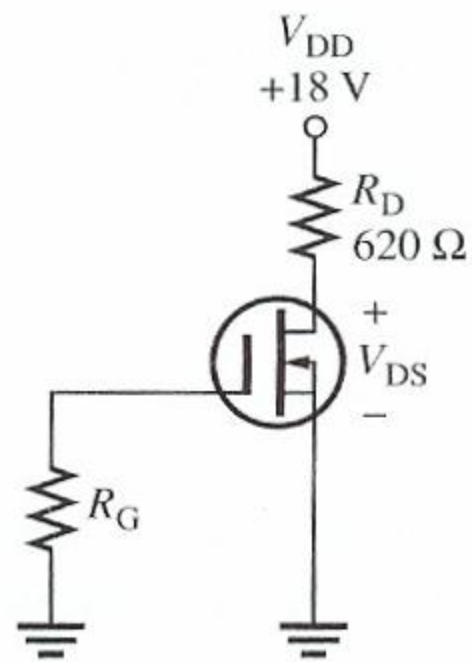
VDS = VDD – IDSS x RD



The purpose of RG in the secon
is to accommodate an ac signal
input by isolating it from GND
Since there is no dc gate
current, RG does not affect
The zero gate-to-source bias



Example:
Determine the drain-to-source voltage in the circuit shown.
The MOSFET data sheet gives VGS(off)=-8 V and IDSS=12 milliA
Solution:
VDS=10.6 V



Example:

Determine VGS and VDS in the circuit shown.

The data sheet for this particular MSFET minimum value of ID(on)=500 milliA at VGS=10V and VGS(th) = 1 V.

Solution:

VGS=(R2/(R1+R2) x VDD = 3.13V

Find K:

$K=ID(on) / (VGS-VGS(th))^2 = 6.17$ milliA/V^2

Calculate ID:

$ID=K(VGS-VGS(th))^2=28$ milliA

VDS=VDD-ID x RD = 10.8V