



## **Spheretek Wafer Bumping**

### **The Low Cost and Reliable Solution to Production Wafer Packaging**

#### **The Problems.**

Packaging Production engineers and their CFO's have to date been disappointed in the results of their collective efforts to reduce packaging costs while simultaneously increasing product performance. Although solder bumping has provided some performance improvements - and commensurate cost reductions - by eliminating die bonding, lead frame and plastic encapsulation expenses, the promise of true low cost wafer packaging has yet to be achieved. This is due, in large measure, to the need for significant capital equipment outlays and the slow and often unreliable process technologies characteristic of current solder bump methodologies.

Further, current industry standard solder bump methodologies suffer from considerable process limitations and inflexibilities, and resultant reliability issues. Key limitations and known problems associated with typical wafer and substrate solder bumping process methodologies are summarized below.

1. Printed Solder Bump (PSB) Processes. Costly equipment; slow process throughput; bump inconsistency; bump height non-uniformity; voids and other solder reflow inconsistencies. PSB processes cannot support all solder alloys reliably. Additionally, this process may require expensive under fills and related processes. PSB is not able to produce 40 $\mu$  bumps demanded for FLASH memory and are not able to meet reliability targets needed for high I/O count applications. PSB processes may also require expensive reliability testing. Rework is costly and labor intensive.
2. Electroplated Solder Bump (ESB) Processes. Costly equipment; slow process throughput; bump height non-uniformity; poor alloy control; micro cracks; craters; process inconsistencies from chemistry fluctuations and other inconsistencies inherent in all plating processes. ESB processes cannot produce 40 $\mu$  bumps demanded for FLASH memory and are not able to meet reliability targets needed for high I/O count applications.
3. Ball or Sphere Drop (BSD) Processes. Costly equipment; unreliable surface adhesion; requires adhesion testing; slow process throughput. BSD processes require highly trained engineers. BSD processes cannot produce 40 $\mu$  bumps demanded for FLASH memory and are not able to meet reliability targets needed for high I/O count applications.

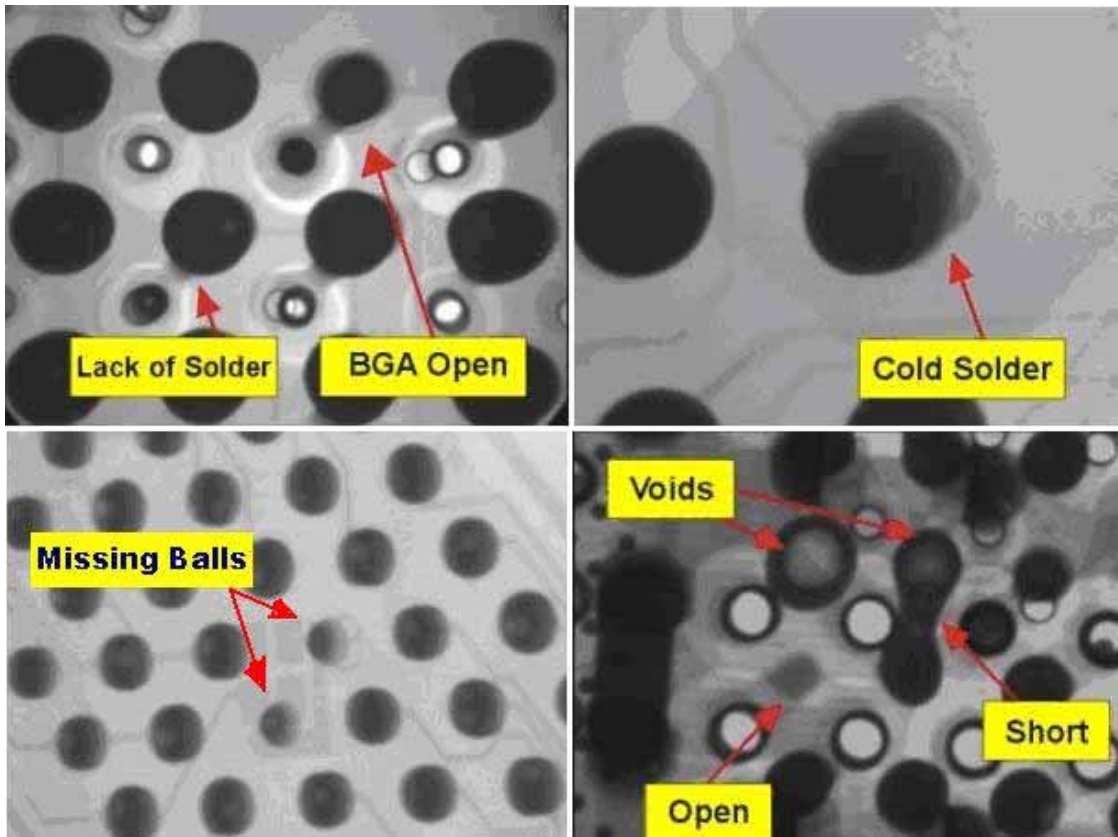


Figure 1: Typical solder transfer problems with current solder bumping methods

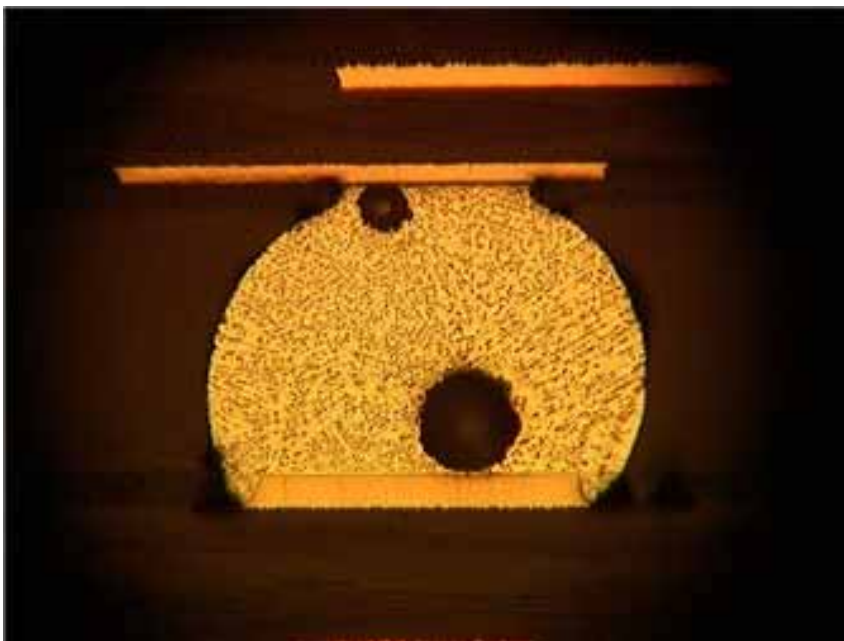


Figure 2: Optical image of voids in lead-free ball after reflow

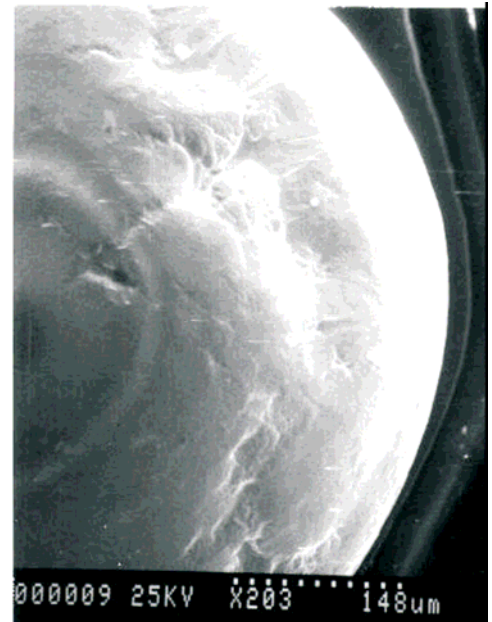


Figure 3: Cracked solder ball

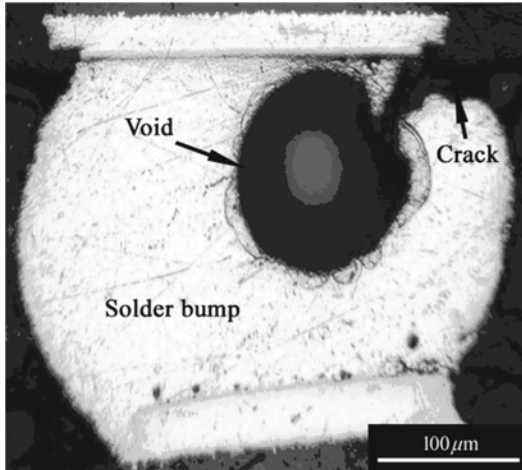


Figure 2A: Xray image of voids in lead-free ball after reflow

### **The Solution.**

Spheretek has developed a methodology and associated tool set that successfully addresses the problems and limitations plaguing Solder Bumping methods currently in use.

The patented Spheretek Precision Wafer Bumping™ (PWB) Technology utilizes Spheretek's Liquid Interference Transfer™ (LIT) Process. LIT consistently produces precision solder bumps (<+/-1% height variation and <+/-1% volume variation) from as small as 40µm to as large as 1250µm at a substantially lower per unit cost than competing technologies. Spheretek's LIT process is compatible with all solderable materials, wafers and substrates, and does not exhibit any of the process issues commonly encountered with other solder bumping technologies. And this process is capable of overcoming substantial surface topology irregularities typically found in non-silicon substrates.

### **The Complete Process.**

The Spheretek PWB Process consists of the following three operations:

1. Aqueous based Dry Film photomasking.
2. Reliable, robust Tri-Metal Under Bump Metallization (UBM).
3. Liquid Interference Transfer™ solder bump deposition process.

The PWB process comprises the most reliable and cost effective solder bumping methodologies currently available. The Precision Wafer Bumping™ process produces near perfect bumps (i.e., <+/-1% bump height variation and <+/-1% bump volume variation) on any size wafer.



In a particularly demanding application, Spheretek's PWB process repeatably (i.e.,  $\pm 1\mu\text{m}$  height variation and with  $<0.05\%$  missing bumps) produced approximately 10,000  $40\mu\text{m}$  bumps on  $90\mu\text{m}$  centers. The PWB process provides the versatility needed for the latest memory and processor high I/O pin count requirements.

The Spheretek<sup>®</sup> Precision Wafer Bumping<sup>™</sup> Technology features a screen printed Inverted Captured Cell<sup>™</sup> methodology (ICC) utilizing Spheretek's patented Liquid Interface Transfer<sup>™</sup> process. This results in the creation of consistently smooth uniform solder bumps suitable for integrated interconnection product applications, such as: wafer level packaging, (WLCSP), Chip Scale Package (CSP), Flip Chip CSP, Flip Chip and BGA production. With the ability to create spheres as small as  $40\mu$ , the Spheretek<sup>®</sup> Precision Wafer Bumping<sup>™</sup> Technology offers true WLCSP capabilities.

### **Under Bump Metalization**

The UBM is critical to the formation of reliable solder bumps. Spheretek has determined that sputtering provides the most robust UBM and has developed a proprietary Tri-Metal UBM for use with its LIT solder bumping process. The key advantages of Spheretek's Tri-Metal UBM are:

1. Reliable and predictable adhesion with known film thickness.
2. Pre-deposition sputter etch and subsequent tri-metal depositions performed in the same system pump down.
3. Compatibility with all known bond pad metallizations.
4. Single pump down deposition method eliminates intermetallic oxidation, thereby eliminating the possibility of intermetallic delamination.
5. Allows the use of low cost Dry Film photomasking techniques with no photoresist preconditioning bake cycles needed.
6. Pre-deposition Sputter etch removes surface oxidation in the target solder bump regions.
7. Tri-Metal UBM can also be used for Redistribution Layer (RDL) formation.
8. No metal etch required. Dry Film liftoff using low cost proprietary aqueous based chemistries with no hazardous waste disposal. Spheretek's Dry Film photomasking process eliminates unreliable corrosive metal etch chemistries and associated disposal issues.
9. Lowest cost UBM.

### **Liquid Interference Transfer<sup>™</sup>.**

The fundamental challenge to be addressed by every solder bump technology is the creation of uniform solder bumps absent of voids, micro cracks, craters, contaminants and any other



inconsistencies detrimental to the end usage: proper soldering of the solder bumped substrate to the end application material.

Spheretek accomplished this by first developing a reliable UBM process. Once an adequate UBM was established, Spheretek addressed the issues of micro-cracks, craters, etc., by developing a solder bump deposition process that created the solder bump by transferring the solder while in a liquefied (not paste) state at the point and time of solder transfer.

This innovative solder deposition technique eliminates the shortcomings exhibited by other solder mask processes. The solder mask pattern is comprised of fully open solder apertures. During liquid solder transfer, the solder mask does not come into contact with the UBM surface bump area or the substrate. The LIT process equipment is designed to maintain an "Interference Gap" between the solder mask and the UBM surface. Only the liquid solder transits the Interference Gap and contacts the UBM to complete the Liquid Interference Transfer™ of the solder to the bond pad.

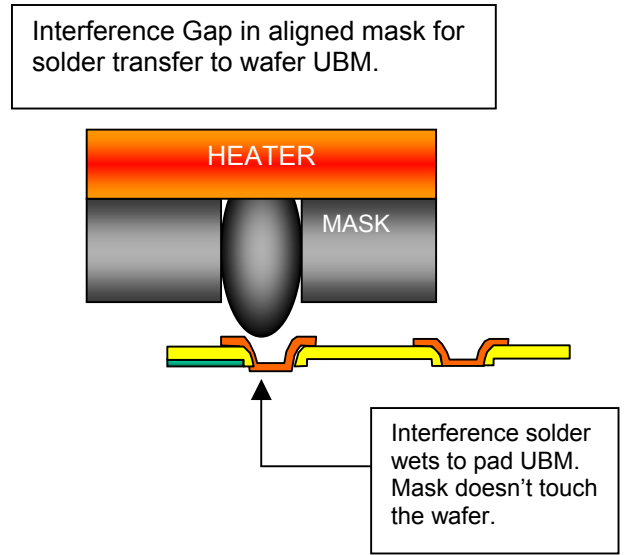


Figure 4: View of Interference Gap

A significant advantage of this technique is that the solder out gasses naturally as the solder liquefies prior to contact with the UBM surface bump area. Solder Bump attachment to the UBM occurs in a neutral environment, thereby creating a solder/UBM interface region that is free of residual solder flux, partially oxidized solder, metallization constituents or other interface weakening contaminants. The Spheretek Liquid Interference Transfer™ process is compatible with both flux and flux-less solders. Solder transfer can also be performed in a neutral flux atmosphere.

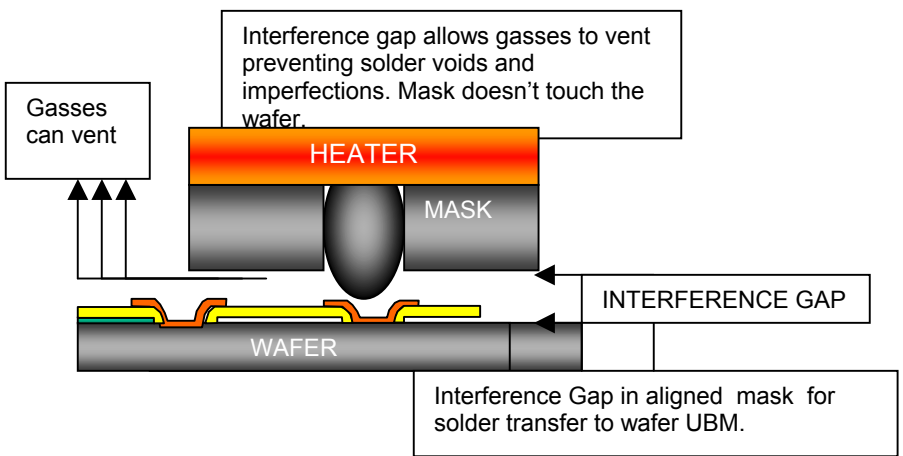


Figure 5: View of Interference Gap with Gasses Venting

The Spheretek LIT process eliminates the reliability problems common with all other methods of solder transfer. Solder bump height is controlled to within +/- 1% of nominal and is inherent to



the Spheretek process. In the unlikely event of an incompletely filled solder mask cell, no liquid solder transfer will occur. Also, if the UBM is flawed (contaminated, missing, etc.), no solder transfer will occur. Post solder transfer inspection is reduced to a simple low cost visual inspection. Either solder bumps are formed or no solder is transferred. It is easy to visually determine whether a solder bump is present. If UBM is properly metallized then solder ball or solder bump can be re-worked with the Spheretek process.

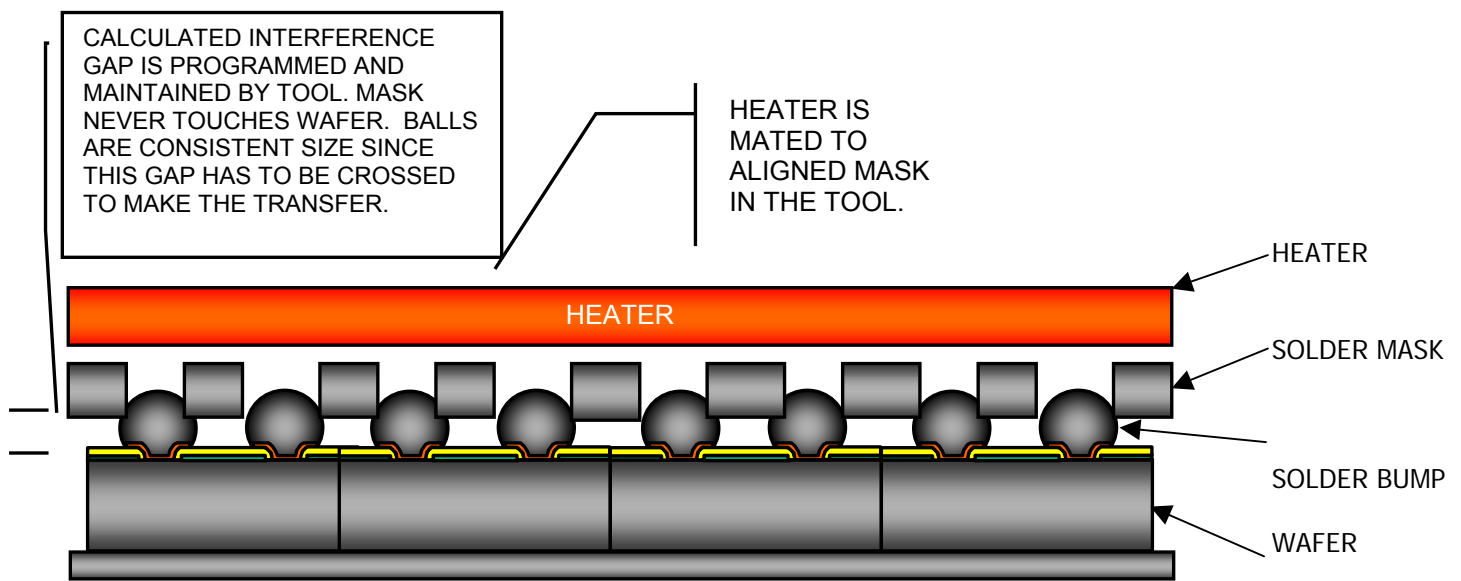


Figure 6: Cross section of HEATER ASSEMBLY mated to SOLDER MASK during liquid solder transfer to UBM located on the substrate. Note that the SOLDER MASK and HEATER ASSEMBLY do not come into contact with the UBM material or the substrate during solder transfer.

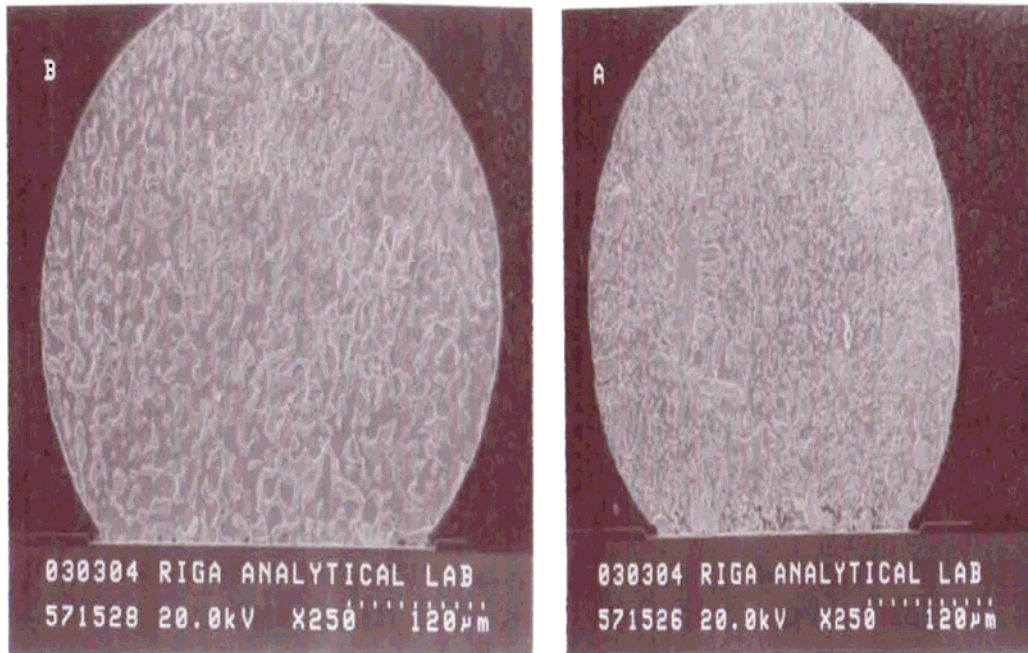


Figure 7: Cross section of Spheretek's Liquid Transfer Solder Bump.

### The Inverted Captured Cell™ (ICC) Methodology

The ICC Methodology is a key concept and is a critical element of Spheretek's Liquid Interference Transfer™ process. The ICC Methodology creates the required solder paste volume control and thermal management necessary for uniform and repeatable transfer of the liquid solder to the UBM. The ICC Methodology is comprised of the following two components:

1. Solder mask (containing various solder apertures).
2. Heater stage.

It is the unique combination of both these components that form the Inverted Captured Cell Methodology™ concept.

Control of the solder bump dimensions (height, width, volume, etc.) is accomplished by utilizing a precision double blade print assembly process that precisely deposits a calculated solder volume into each aperture on the solder mask. The double blade is specifically engineered to prevent print voids, "drag out" or "scoop out" of the solder paste as the blade moves the solder paste across the mask.



The solder paste is applied to the solder mask when the mask is in contact with the heater stage and while the heater stage is de-activated. The heater is only activated after completion of the application of solder paste. The LIT equipment then inverts the solder mask / heater stage combination and brings them into close proximity with the UBM surface while precisely maintaining the required Interference Gap.

The dimension of each solder mask aperture is determined by the volume of solder paste needed to create the proper amount of liquid solder to transit the Interference Gap maintained by the LIT

equipment between the solder mask and the UBM surface. The solder mask aperture dimensions (length, width and solder mask thickness) control the volume of solder paste contained in the aperture. Uniform solder volume ensures that the solder bumps deposited onto the UBM surface are of uniform volume and that the resultant bumps are co-planar.

The flux between the solder mask and heater chuck provides sufficient thermal connectivity to ensure uniform heat distribution within the solder mask.

The Inverted Captured Cell™ technique allows venting of any gasses and volatiles generated during solder liquefaction out through the Interference Gap, thereby preventing voids and aiding in the formation of uniform solder bumps on the UBM surface.

A good seal between the solder mask and the heater chuck is essential to prevent solder seepage and to ensure that all the liquefied solder is transferred to the UBM surface.

Once the liquid solder has transferred to the UBM, the heater stage is de-activated and the LIT equipment retracts the solder mask/heater stage from the UBM surface and returns the solder mask/heater stage to the non-inverted position.

### Repeatability, Reliability and Uniformity

The patented Spheretek Precision Wafer Bumping™ process has reliability designed in. The Interference Gap allows for flux and solder formula gasses to be released during the solder liquefaction process. This keeps any gasses from creating voids and imperfections at the solder/UBM interface that could contribute to future cold solder failures.

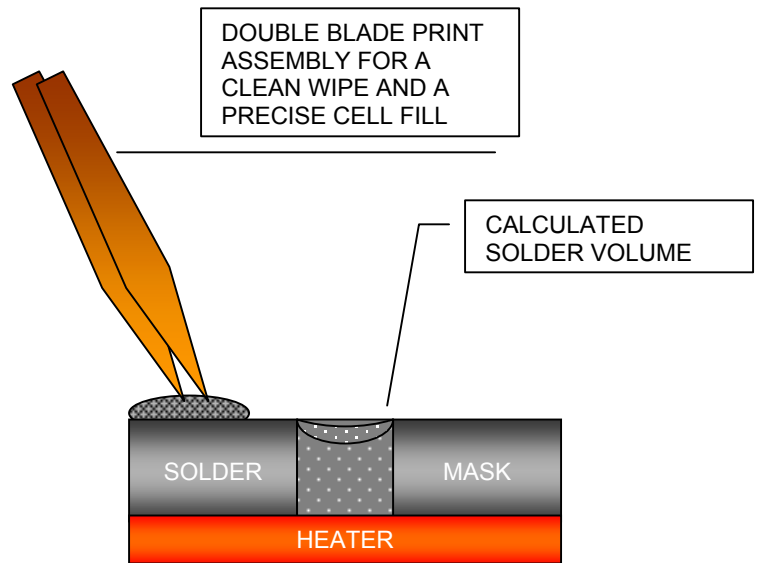


Figure 8: Captured Cell Assy.





If, for whatever reason, the liquefied solder is not sufficient to transit the Interference Gap, or the UBM cannot be wetted, no solder is transferred. The Spheretek PWB process cannot, by design, create an under or over sized solder bump nor can it create a bump that does not have a proper intermetallic connection to the UBM. Further, any missing bumps can be found by simple, low magnification visual inspection. Missing bumps can be easily identified and remedied by rectifying any contaminated UBM and/or adjusting the Interface Gap and repeating the liquid solder transfer sequence.

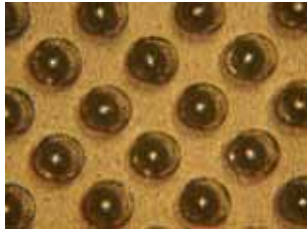


Figure 9A:  
Image of substrate with solder bumps  
bump

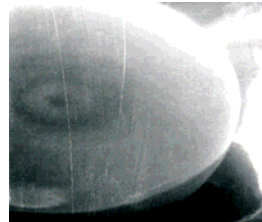


Figure 9B:  
High magnification of solder  
bump

## Re-Work

Previously bumped substrates that are missing solder bumps can be re-worked using Spheretek's LIT solder bumping process – provided that the un-bumped regions have a satisfactory (i.e., no contamination, no missing metal, etc) UBM. Solder will only attach to UBM regions that are clean and free of defects or contamination. Substrates containing solder bumps deposited using Spheretek's Liquid Interference Transfer process can be reworked to attach solder bumps to UBM areas where liquid solder previously failed to transfer. Rework will not adversely affect existing solder bumps already deposited.

The rework starts with the mask being placed over the existing wafer, die or substrate. The bumps that are good fit into the mask. (See Figure 9A) Solder is wiped into the mask and the existing good bumps block solder. Where there is no or little solder, the mask is refilled with solder. Then the heater is realigned to create the captured cell and a new perfect bump is formed. (See Figure 9B)

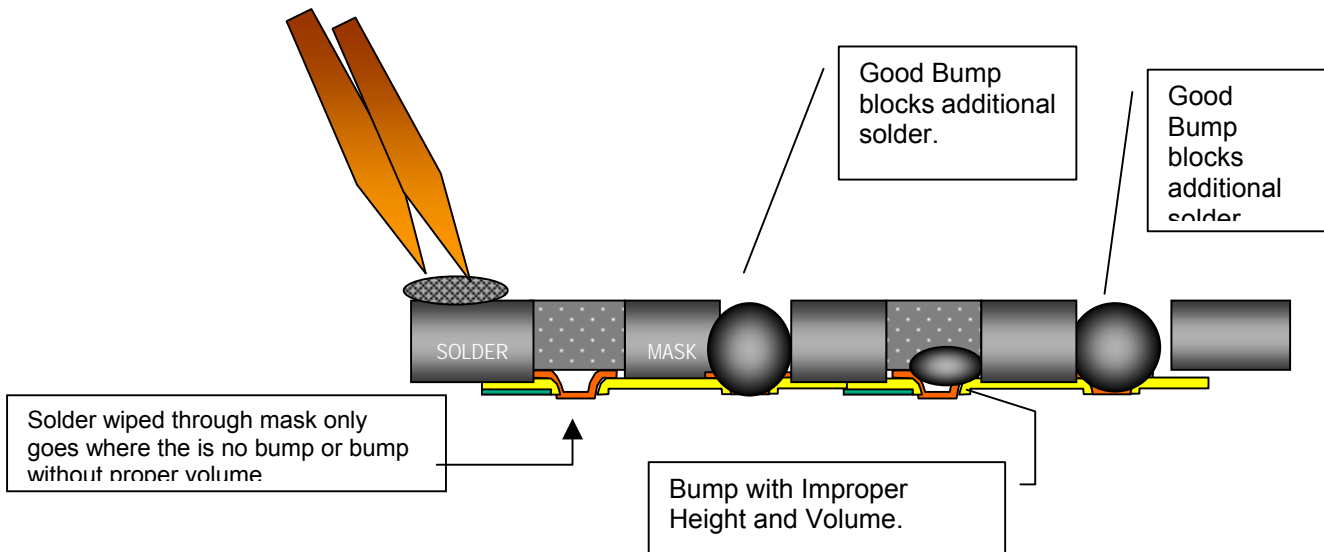


Figure 9A Mask with malformed bump and missed bump. Solder rewiped into mask.

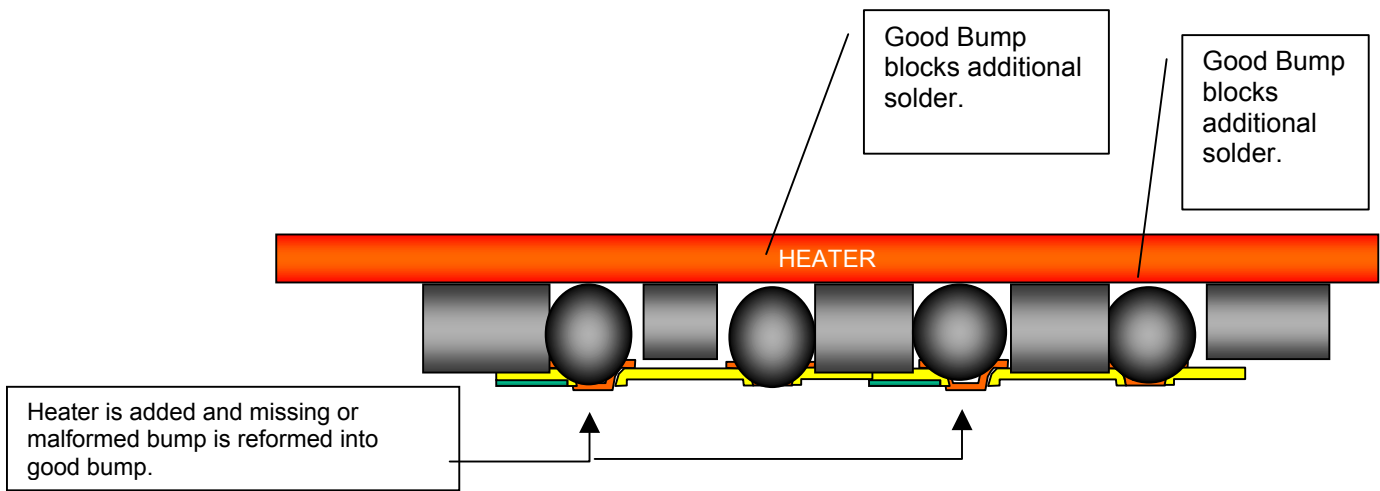


Figure 9B Mask with malformed bump and missed bump after rework and reflowed.



## Summary

Spheretek has developed a flexible and reliable solder bumping process that remedies the reliability and uniformity issues common to currently available solder bumping processes.

The tooling required is inexpensive and can be reused many times. The PWB process is compatible with any solderable substrate material.

Spheretek's Precision Wafer Bumping™ process is the lowest cost solder bumping process available commercially.

## Process Advantages.

Summary of the advantages of the Spheretek Precision Wafer Bumping™ process:

- Compatible with any solderable substrate materials.
- Lowest material cost.
- Lowest tooling cost.
- Highest reliability.
- No trapped flux.
- Solder balls from 40µm to 1250µm.
- Fewest process steps.
- Easy solder bump visual inspection.
- Process produces no voids.
- Consistent solder ball heights and excellent co-planarity.
- Can overcome non-silicon substrate surface topology issues

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Spheretek Patents:

US 7007833 Forming solder balls on substrates  
US 7604153 Forming solder balls on substrates  
US 7288471 Bumping electronic components using transfer substrates  
US 6609652 Ball bumping substrates, particularly wafers  
US 6293456 Methods for forming solder balls on substrates  
US 6126059 Captured-cell solder printing and reflow methods and apparatuses  
US 5988487 Captured-cell solder printing and reflow methods

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