THE UNIVERSITY OF TEXAS AT AUSTIN
Cockrell School of Engineering

FULL NAME: David Z. Pan

TITLE: Professor, Silicon Laboratories Endowed Chair in Electrical Engineering

DEPARTMENT: Electrical and Computer Engineering, The University of Texas at Austin

EDUCATION:

University of California, Los Angeles	Computer Science	Ph.D.	Fall 2000
University of California, Los Angeles	Computer Science	M.S.	Fall 1998
University of California, Los Angeles	Atmospheric Sciences	M.S.	Fall 1994
Peking University, China	Physics	B.S.	Spring 1992

CURRENT AND PREVIOUS ACADEMIC POSITIONS:

The University of Texas at Austin	Professor, Silicon Labs Endowed Chair in Electrical Engineering	09/2020 –
The University of Texas at Austin	Professor, Engineering Foundation Endowed Professorship #1	09/2014 – 08/2020
Massachusetts Institute of Technology	Visiting Professor, EECS Department; Visiting Scientist, Microsystems Technology Laboratories	06/2019 – 12/2019
The University of Texas at Austin	Professor, Brasfield Endowed Faculty Fellow	09/2013 – 08/2014
The University of Texas at Austin	Associate Professor	09/2008 – 08/2013
The University of Texas at Austin	Assistant Professor	09/2003 – 08/2008

OTHER PROFESSIONAL EXPERIENCES:

IBM T. J. Watson Research Center	Research Staff Member	10/2000 – 08/2003

CONSULTING:

- I have served as an advisor / consultant to a number of major technology companies and startups in semiconductor, EDA, AI, and computing related industries (e.g., Cadence, Dell, Google, Pyxis, Qualcomm, Tabula).

- I have served as an expert witness / legal consultant to several law firms (e.g., Cooley LLP, Fish & Richardson, Hogan Lovells, Latham & Watkins).

HONORS AND AWARDS (SELECTED):

General Awards/Honors:

- 2021 **ACM Fellow**, for contributions to electronic design automation, including design for manufacturing and physical design
- 2017 **SPIE Fellow**, for achievements in IC design for manufacturing with advanced lithography
- 2014 **IEEE Fellow**, for contributions to design for manufacturability in integrated circuits

- 2020- **Silicon Laboratories Endowed Chair in Electrical Engineering,** UT Austin

- 2020 **IEEE CEDA Outstanding Service Recognition**, "for outstanding service to the EDA community as ICCAD General Chair in 2019"
- 2019 **Cadence Academic Collaboration Award**, "for contributions to design for manufacturing and physical design of integrated circuits and systems, and educating a diverse body of outstanding EDA professionals to industry"
- 2019-2021 IEEE Council on Electronic Design Automation (CEDA) **Distinguished Lecturer**
- 2014-2020 **Engineering Foundation Endowed Professorship #1**, UT Austin
- 2014 **RAISE Faculty Excellence Award** -- Recognizing Asian & Asian American Faculty & Staff Instilling Strength and Excellence, The University of Texas at Austin
- 2013 **SRC Technical Excellence Award**, for "Nanometer IC Design for Manufacturability" with the citation "In recognition of your key contributions to technology that have significantly enhanced the productivity of the semiconductor industry"
- 2013-2014 Earl N. & Margaret Brasfield Endowed Faculty Fellowship in Engineering, UT Austin
- 2010, 2006, 2005, 2004 **IBM Faculty Award**
- 2009 UCLA School of Engineering and Applied Science, **Distinguished Young Alumnus Award** (a.k.a. **Rising Professional Achievement Award**), which honors the early career achievements of alumni who are under the age of 40
- 2008-2009 IEEE Circuits & Systems (CAS) Society **Distinguished Lecturer**
- 2008, 2000 Semiconductor Research Corporation (SRC) Inventor Recognition Award
- 2008 Association for Computing Machinery (ACM) Recognition of Service Award
- 2007 National Science Foundation (NSF), **Faculty Early Career Development (CAREER) Award**
- 2007 Association for Computing Machinery (ACM) Recognition of Service Award
- 2005 **ACM/SIGDA Outstanding New Faculty Award**
- 2003 IBM Research Bravo Award
- 2001 **Outstanding Ph.D. Award**, UCLA Computer Science Department
- 2000 Dimitris Chorafas Foundation Award
- 1999-2000 IBM Research Fellowship

Best Paper Awards, Prolific Author Awards, etc.:

- 2021 **IEEE Transactions on Computer-Aided Design Donald O. Pederson Best Paper Award**
- 2020 **Best Poster Award**, NSF Workshop on Machine Learning Hardware (Student: Jiaqi Gu)
- 2020 **Best Paper Award**, ACM International Symposium on Physical Design (ISPD)
- 2020 **Best Paper Award**, ACM/IEEE Asian and South Pacific Design Automation Conference (ASP-DAC)
- 2020 **ASP-DAC Prolific Author Award** - for having published 25 or more papers at the 25th Asian and South Pacific Design Automation Conference (ASP-DAC) – I have published 44 papers as of 2020 in ASP-DAC, which is ranked #3 in the world in ASP-DAC history
- 2020 ASP-DAC 10-Year Retrospective Most Influential Paper Award Finalist
- 2019 **Best Paper Award**, ACM/IEEE Design Automation Conference (DAC)
- 2018 **Best Paper Award**, ACM Great Lakes Symposium on VLSI (GLSVLSI)
- 2018 **Best Paper Award**, Integration – the VLSI Journal
- 2017 **Best Paper Award**, IEEE International Symposium on Hardware Oriented Security and Trust (HOST)
- 2016 SPIE Advanced Lithography Franco Cerrina Memorial **Best Student Paper Award**
- 2015 **Best Paper in Session Award**, SRC Techcon Conference
- 2015 Asian and South Pacific Design Automation Conference (**ASP-DAC**) **Frequently Cited Author Award** (given to the top 3 cited authors in ASP-DAC's 20-year history)
- 2015 ASP-DAC 10-Year Retrospective Most Influential Paper Award Finalist
- 2014 **Best Paper Award**, ACM International Symposium on Physical Design (ISPD)
- 2014 Communications of the ACM (CACM) **Research Highlights**, for "Full-Chip Mechanical Reliability Analysis and Optimization for 3D ICs"
- 2013 IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), **Keynote Paper** for "Design for Manufacturing with Emerging Nanolithography"

- 2013 **William J. MacCalla Best Paper Award**, IEEE/ACM International Conference on Computer Aided Design (ICCAD)
- 2013 **DAC Top 10 Author in Fifth Decade**, for being one of the top 10 most prolific authors in DAC's fifth decade
- 2013 **DAC Prolific Author Award** - DAC 25 Club, for having published 25 or more papers at the Design Automation Conference
- 2012 **Best Paper in Session Award**, SRC Techcon Conference
- 2012 **Best Paper Award**, ACM/IEEE Asian and South Pacific Design Automation Conference (ASP-DAC)
- 2011 **Best Paper Award**, ACM International Symposium on Physical Design (ISPD)
- 2010 **IBM Research Pat Goldberg Memorial Best Paper Award** in Computer Science, Electrical Engineering and Math (4 awardees across all fields of CS, EE, and Math among all papers published/co-authored by IBM Research)
- 2010 **Best Paper Award**, ACM/IEEE Asian and South Pacific Design Automation Conference (ASP-DAC)
- 2009 **Best Student Paper Award**, IEEE International Conference on IC Design and Technology
- 2009 **Best Paper (IP) Award**, IEEE/ACM Design Automation & Test in Europe (DATE)
- 2007 **Best Paper in Session Award**, SRC Techcon Conference
- 1998 **Best Paper in Session Award**, SRC Techcon Conference
- **18 additional Best Paper Award Candidates/Finalists/Nominations**: DAC 2021, CICC 2021, DAC 2020, ASP-DAC 2020, DAC'19, ISPD'19, DATE'19, DAC'14, ASP-DAC'13, DAC'12, ISPD'12, ICCAD'11, DAC'11, ISPD'10, ICCAD'08, ASP-DAC'08, DAC'06, ASP-DAC'06

Contest Awards and Student Awards:

- 2022 **Robert S. Hilbert Memorial Optical Design Competition Winner** (Students: Chenghao Feng, Jiaqi Gu, and Hanqing Zhu) $3,000
- 2017 ACM International Symposium on Physical Design **(ISPD) Contest: 1st Place**
- 2016 ACM International Symposium on Physical Design **(ISPD) Contest: 1st Place**
- 2013 ICCAD CAD Contest Award (the 2nd Place) in "Mask Optimization"
- 2012 ICCAD CAD Contest Award in "Fuzzy Pattern Matching for Physical Verification", 2nd Place
- 2009 **Grand Prize ($25,000),** eASIC Placement Worldwide Contest
- 2007 IEEE CEDA Award for the Open Source BoxRouter 2.0
- 2007 ACM International Symposium on Physical Design (ISPD) Routing Contest Awards: the 2nd place in 3D and the 3rd place in 2D

- 2022 Spring UT-ECE Senior Capstone Design **1st Place** - *Entrepreneurial Category* Winning Team HitStick (students: Nick Canga, Alex Kremer, Austin Rath, Connor Smith, Abhi Sridhar, Zane Zwanenburg), Faculty Mentor
- 2022 Honor for PhD Student Wei Ye: European Design and Automation Association (EDAA) **Outstanding Dissertation Award**
- 2021 Honor for PhD Student Jiaqi Gu (co-advised by Prof. Ray Chen): **First Place, ACM Student Research Competition Grand Finals** (Graduate Category)
- 2021 Honor for PhD Student Zhoufeng Ying (co-advised with Prof. Ray Chen): **Margarida Jacome Dissertation Prize**, Department of Electrical and Computer Engineering, UT Austin (one per year for the entire ECE Dept.)
- 2021 Honor for PhD Student Ahmet Budak (co-advised by Prof. Nan Sun): ADI Outstanding Student Designer Award
- 2020 Honor for PhD Student Jiaqi Gu: ACM/SIGDA Student Research Competition **Gold Medal** (Graduate Category) at ICCAD 2020
- 2019 Honor for PhD Student Meng Li: **Margarida Jacome Dissertation Prize**, Department of Electrical and Computer Engineering, UT Austin (one per year for the entire ECE Dept.)
- 2019 Honor for PhD Student Meng Li: European Design and Automation Association (EDAA) **Outstanding Dissertation Award**

- 2018 Honor for PhD Student Wuxi Li: ACM/SIGDA Student Research Competition Silver Medal (Graduate Category) at ICCAD 2018
- 2018 Honor for PhD Student Meng Li: **First Place, ACM Student Research Competition Grand Finals** (Graduate Category) – the award was presented at the Turing Award banquet
- 2018 Honor for PhD Student Xiaoqing Xu: **ACM Outstanding PhD Dissertation Award in EDA**
- 2017 Honor for PhD Student Meng Li: ACM/SIGDA Student Research Competition **Gold Medal** (Graduate Category) at ICCAD 2017
- 2016 Honor for PhD Student Xiaoqing Xu: ACM/SIGDA Student Research Competition **Gold Medal** (Graduate Category) at ICCAD 2016
- 2015 Honor for PhD Student Bei Yu: European Design and Automation Association (EDAA) **Outstanding Dissertation Award**
- 2013 Honor for PhD Student Bei Yu: ACM/SIGDA Student Research Competition Silver Medal (Graduate Track) at ICCAD 2013
- 2013 Honor for PhD Student Duo Ding: **ACM Outstanding PhD Dissertation Award in EDA**
- 2012 Fall UT-ECE Senior Design Open House, the 1st Place Winning Team, Faculty Mentor

MEMBERSHIPS IN PROFESSIONAL AND HONORARY SOCIETIES:

Fellow, ACM (Association for Computing Machinery), class of 2021
Fellow, IEEE (Institute of Electrical and Electronics Engineers), class of 2014
Fellow, SPIE (International Society for Optical Engineering), class of 2017

PROFESSIONAL SOCIETY AND MAJOR GOVERNMENTAL COMMITTEES:

Editorship

- Senior Associate Editor, ACM Transactions on Design Automation of Electronic Systems (TODAES), 2014-present
- Subject Editor, Physical Synthesis and Design for Manufacturing, Elsevier Integration – The VLSI Journal, 2020-present
- Associate Editor, IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD), 2006-2011, 2018-present
- Associate Editor, IEEE Design & Test, 2016-present
- Associate Editor, IET Computers & Digital Techniques, 2014-present
- Associate Editor, Science China Information Sciences, 2013-present
- Subject Area Editor (in VLSI Design), Journal of Computer Science and Technology (JCST), 2010-present
- Associate Editor, Journal of Microelectronic Manufacturing (JoMM), 2019-
- Associate Editor, IEEE Circuits and Systems Society (CASS) Newsletters, 2007-2016
- Associate Editor, IEEE Transactions on Very Large Scale Integration Systems (TVLSI), 2007-2014
- Associate Editor, IEEE Transactions on Circuits and Systems, I: Regular Papers (TCAS-I), 2008-2009
- Guest Editor, IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD), Special Section of International Symposium on Physical Design, 2007 and 2008
- Associate Editor, IEEE Transactions on Circuits and Systems, II: Express Briefs (TCAS-II), 2006-2007

Service to Professional Society and Government/Agencies

- IEEE CAS Society IC Design and Test for Emerging Circuits and Systems Standards (CAS/ICSC) Committee, 2022-2024

- ACM/SIGDA Outstanding PhD Dissertation Award Committee Chair, 2022
- ACM/TODAES Best Paper Award Committee, 2022
- Steering Committee, ACM Special Interest Group on Embedded Systems (SIGBED) China, 2021-
- IEEE Computer Society Fellow Evaluation Committee, 2021
- ACM Special Interest Group on Design Automation (SIGDA), Executive Committee (Award Chair), 2018-2021
- IEEE Electron Devices Society (EDS) Representative to IEEE Council on Electronic Design Automation (CEDA), 2016-2019
- IEEE Council on Electronic Design Automation (CEDA) Fellow Evaluation Committee, 2017
- IEEE Council on Electronic Design Automation (CEDA), Distinguished Lecturer Program Committee, 2016-2019
- EDAA Outstanding Dissertation Award Jury Member, 2019, 2020, 2021
- ACM/SIGDA Outstanding New Faculty Award Committee, 2017
- ACM/TODAES Best Paper Award Committee, 2016, 2017, 2019
- ACM/SIGDA Outstanding PhD Dissertation Award Committee, 2014
- Advisor Board, Chinese American Semiconductor Professional Association (华美半导体协会), Austin Chapter, 2013 -
- IEEE Council on Electronic Design Automation (CEDA), Publicity Committee, 2012-present
- IEEE Admission & Advancement Committee Senior Member Review Panel, Feb. 2013
- ACM/SIGDA Technical Committee on Physical Design, Chair, 2009-2015
- Semiconductor Industry Association, International Technology Roadmap for Semiconductors (ITRS), Design Technology Working Group, 2004-2015
- ACM/SIGDA Outstanding PhD Dissertation Award Committee, 2012
- IEEE Computer-Aided Network Design (CANDE) Committee: Past Chair, 2010; Chair, 2009; Secretary, 2008
- IEEE Council on EDA (CEDA) Working Group for Educational Certification Program in China, 2007
- IEEE Guillemin-Cauer and Darlington Best Paper Awards Nomination Committee, 2007
- IEEE TCAS-II EDICS Committee, 2006
- NYSTAR (New York State) Microelectronics Design Center (MDC) Industrial Liaison, 2002-2003
- Semiconductor Research Corporation (SRC) Industrial Liaison, 2001-2003

Services to Professional Conferences

Various Chair/Leadership/Advisory Positions

- **Executive Committee Member and Technical Program Vice Chair**, ACM/IEEE Design Automation Conference (DAC), 2023
- **Executive Committee Member and Panel Chair**, ACM/IEEE Design Automation Conference (DAC), 2022
- Local Arrangement Co-Chair, 55th IEEE International Symposium on Circuits and Systems (ISCAS), Austin, Texas, 2022
- Academic Chair of EDA Events at the 24th International Conference on Theory and Applications of Satisfiability Testing (SAT2021), 2021
- Advisory Chair, International Conference on Integrated Circuits and Microsystems (ICICM), 2020, 2021
- Executive Committee (Past Chair), IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2020
- **General Chair**, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2019
- Advisory Board, IEEE International Conference on Omni-layer Intelligent Systems (COINS), 2019-2022

- **Program Chair**, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2018
- Subcommittee Chair for "Physical Design and Verification, Lithography and DFM", Design Automation Conference (DAC), 2020, 2021
- CAD Track Chair, International Symposium on Low Power Electronics & Design (ISLPED), 2018
- Vice Program Chair, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2017
- **Technical Program Chair**, ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC), 2017
- Executive Committee Member and Special Session/Tutorial Chair, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2016
- International Advisory Committee Co-Chair, IEEE International Conference on Ubiquitous Wireless Broadband (ICUWB), Oct. 16-19, 2016
- Subcommittee Chair for "Physical Verification, Lithography and DFM", Design Automation Conference (DAC), 2016
- Steering Committee Member, ACM International Symposium on Physical Design (ISPD), 2016, 2017, 2018, 2019, 2020, 2021
- Technical Program Committee Vice Chair, ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC), 2016
- Executive Committee Member and Workshop Chair, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2015
- Executive Committee Member and Tutorial Chair, ACM/IEEE Design Automation Conference (DAC), 2014
- Organizing Committee Chair, IEEE Texas Workshop on Integrated Systems Exploration (TexasWISE), 2014
- Co-Chair, IEEE/ACM Workshop on Variability Modeling and Characterization (VMC), 2013, 2014 (co-located with ICCAD)
- Co-Chair, NSF/SRC/DFG Cross Domain Resilience Workshop, Austin, July 11-12, 2013
- Technical Program Co-Chair, the 1st IEEE International High Speed Interconnect Symposium (From Silicon to Systems), Dallas, April 30, 2013
- Organizing Committee, the 1st IEEE Texas Workshop on Integrated Systems Exploration (TexasWISE), 2013
- Conference Co-Chair, 13th International CAD/Graphics Conference, 2013
- EDA Track Co-Chair, 31st IEEE International Conference on Computer Design (ICCD), 2013
- ASP-DAC 10-Year Retrospective Most Influential Paper Award Committee Member, 2013
- Technical Advisory Board Member, International System-on-Chip (SoC) Conference & Exhibit, 2007-present
- Design for Manufacturability Track Chair, International Conference on Computer Aided Design (ICCAD), 2012
- CAD and Design Tools Track Chair, International Symposium on Low Power Electronics & Design (ISLPED), 2012, 2013, 2014
- Design for Manufacturability Subcommittee Chair, Design Automation Conference (DAC), 2012
- DFM and Statistical Design, Subcommittee Chair, Asian and South Pacific Design Automation Conference (ASP-DAC), 2012, 2013
- EDA Subcommittee Chair, International Symposium on VLSI Design, Automation & Test (VLSI-DAT), 2010, 2011, 2012, 2013, 2014
- EDA Subcommittee Co-Chair, IEEE International Conference on Integrated Circuit Design and Technology (ICICDT), 2012, 2013, 2014
- Award Chair, IEEE International Conference on Integrated Circuit Design and Technology (ICICDT), 2009-2012
- Biological, Nanoscale and Post-CMOS Systems, Subcommittee Chair, International Conference on Computer-Aided Design (ICCAD), 2011

- Physical Design & Manufacturability Subcommittee Chair, Design Automation Conference (DAC), 2011
- Physical Design Track Chair, Asian and South Pacific Design Automation Conference (ASP-DAC), 2011
- Exhibits Chair, International Symposium on Low Power Electronics & Design (ISLPED), 2010
- Best Paper Award Committee Member, IEEE/ACM International Symposium on Networks-on-Chip (NOCS), 2009
- Steering Committee Chair, ACM International Symposium on Physical Design (ISPD), 2009
- DFM Track Chair, Asian and South Pacific Design Automation Conference (ASP-DAC), 2009
- General Co-Chair, Austin Conference on Integrated Systems and Circuits (ACISC), 2009
- Chair for Electronic Design Automation (EDA) track, First Asian Symposium on Quality Electronic Design (ASQED), 2009
- **General Chair**, ACM International Symposium on Physical Design (ISPD), 2008
- Program Co-Chair, Austin Conference on Integrated Systems and Circuits (ACISC), 2008
- Publication Chair, SLIP Workshop, 2008
- Co-Chair for Design of Reliable Circuits and Systems (DFR) track, International Symposium on Quality Electronic Design (ISQED), 2007 and 2008
- Local Arrangement Chair/Steering Committee Member, IEEE International Conference on Integrated Circuit Design and Technology (ICICDT), 2007
- **Program Chair**, ACM International Symposium on Physical Design (ISPD), 2007
- IEEE CANDE Workshop Chair, 2007
- CAD track Co-Chair, International Symposium on Circuits and Systems (ISCAS), 2006, 2007
- Invited Speakers/Panel Chair, Austin Conference on Integrated Systems and Circuits (ACISC), 2006, 2007
- Publication Chair, ACM International Symposium on Physical Design (ISPD), 2006
- Publicity Chair, ACM International Symposium on Physical Design (ISPD), 2005
- Publicity Co-Chair, SLIP Workshop, 2003
- Local Arrangement Chair, Great Lakes Symposium on VLSI (GLSVLSI), 2002
- Session Chair for DAC, ICCAD, ISPD, ASP-DAC, ISQED, SLIP, ICICDT, ICSICT, etc.

Program Committee Member

- IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2022
- ACM/IEEE Workshop on Machine Learning for CAD (MLCAD), 2020, 2021, 2022
- SPIE Advanced Lithography Symposium – DFM Conference Committee, 2012-present
- SPIE Photonics West – Optoelectronic Interconnect XII Conference Committee, 2012
- ACM/IEEE International Symposium on Low Power Electronics & Design (ISLPED), 2011-present
- IEEE International Conference on Computer Design (ICCD), 2011-2014
- ACM/SIGDA Student Research Competition at ICCAD 2013, 2014
- ACM/IEEE Design Automation Conference (DAC), 2009-2012
- IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2003-2005, 2009-2012
- ACM/IEEE Asian and South Pacific Design Automation Conference (ASP-DAC), 2003-2005, 2007, 2009-2013, 2015
- IEEE International Symposium on VLSI Design, Automation & Test (VLSI-DAT), 2008-2015
- IEEE International Workshop on Design for Manufacturability & Yield (DFM&Y), 2007-2011
- IEEE International Conference on Integrated Circuit Design and Technology (ICICDT), 2005-2014
- ACM International Workshop on System Level Interconnect Prediction (SLIP), 2003-2011
- SASIMI Workshop, 2009-2010
- IEEE International Symposium on Quality Electronic Design (ISQED), 2006-2009
- Austin Conference on Integrated Systems and Circuits (ACISC), 2006-2008
- International Semiconductor Technology Conference, 2008

- IEEE/ACM International Conference on VLSI Design (VLSID), 2008
- IEEE/ACM Design, Automation and Test in Europe (DATE), 2006, 2007
- International Symposium on Circuits and Systems (ISCAS), 2004-2007
- ACM International Symposium on Physical Design (ISPD), 2004-2007
- ACM Great Lakes Symposium on VLSI (GLSVLSI), 2002-2006

Proposal Review Panels

- National Science Foundation (NSF) Panelist
- External reviewer for European Research Council
- Germany DFG Panelist
- External reviewer for Swiss National Science Foundation (SNSF)
- External reviewer for Austrian Science Fund (FWF)
- External reviewer for Research Grants Council, Hong Kong
- External reviewer for Qatar National Research Fund
- External reviewer for California MICRO Program
- External reviewer for Louisiana Board of Regents
- External reviewer for University of Missouri Research Board

PUBLICATIONS:

Google citation page http://scholar.google.com/citations?user=3aLIroEAAAAJ
Citations 12,600, h-index 58, i-10 index 276, as of August 6, 2022

A. Refereed Journal Articles

[J1] Xiaohan Gao, Haoyi Zhang, Mingjie Liu, Linxiao Shen, David Z. Pan, Yibo Lin, Runsheng Wang, Ru, "Interactive Analog Layout Editing with Instant Placement and Routing Legalization," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Date of Publication: 12 July 2022

[J2] Jiaqi Gu, Chenghao Feng, Hanqing Zhu, Zheng Zhao, Zhoufeng Ying, Mingjie Liu, Ray T. Chen, and David Z. Pan, "SqueezeLight: A Multi-Operand Ring-Based Optical Neural Network with Cross-Layer Scalability," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Date of Publication: 08 July 2022

[J3] Hanqing Zhu, Jiaqi Gu, Chenghao Feng, Mingjie Liu, Zixuan Jiang, Ray T. Chen, and David Z. Pan, "ELight: Towards Efficient and Aging-Resilient Photonic In-Memory Neurocomputing," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Date of Publication: 13 June 2022

[J4] Keren Zhu, Hao Chen, Mingjie Liu, and David Z. Pan, "Tutorial and Perspectives on MAGICAL: A Silicon-Proven Open-Source Analog IC Layout System," *IEEE Transactions on Circuits and Systems II: Express Briefs (TCAS-II)*, 2022. (**Invited**)

[J5] Jiaqi Gu, Chenghao Feng, Hanqing Zhu, Ray T. Chen, and David Z. Pan, "Light in AI: Toward Efficient Neurocomputing with Optical Neural Networks - A Tutorial," *IEEE Transactions on Circuits and Systems II: Express Briefs (TCAS-II)*, 2022. (**Invited**)

[J6] Ahmet F. Budak, Miguel Gandara, Wei Shi, David Z. Pan, Nan Sun and Bo Liu, "An Efficient Analog Circuit Sizing Method Based on Machine Learning Assisted Global Optimization," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 41, No. 5, pp. 1209-1221, May 2022

[J7] Ki Yong Kim, David Z. Pan, and Ranjit Gharpurey, "A Broadband Spectrum Channelizer with PWM-LO Based Sub-Band Gain Control," *IEEE Journal of Solid-State Circuits (JSSC)*, Vol. 57, No. 3, pp. 781-792, Jan. 2022,

[J8] Martin Rapp, Hussam Amrouch, Yibo Lin, Bei Yu, David Z. Pan, Marilyn Wolf, and Jeorg Henkel, "MLCAD: A Survey of Research in Machine Learning for CAD," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Date of publication Nov. 2021 (**Keynote Paper**)

[J9] Chenghao, Feng, Zhoufeng Ying, Zheng Zhao, Jiaqi Gu, David Z. Pan, and Ray T. Chen, "Towards high-speed and energy-efficient computing: A WDM-based scalable on-chip silicon integrated optical comparator," *Laser & Photonics Reviews*, Jun. 2021

[J10] Yibo Lin, Zixuan Jiang, Jiaqi Gu, Wuxi Li, Shounak Dhar, Haoxing Ren, Brucek Khailany, and David Z. Pan, "DREAMPlace: Deep Learning Toolkit-Enabled GPU Acceleration for Modern VLSI Placement," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 40, no. 4, pp. 748-761, April 2021. (**Donald O. Pederson Best Paper Award**)

[J11] Hao Chen*****, Mingjie Liu*****, Biying Xu*****, Keren Zhu*****, Xiyuan Tang, Shaolan Li, Yibo Lin, Nan Sun and David Z. Pan**, "**MAGICAL: An Open-Source Fully Automated Analog IC Layout System from Netlist to GDSII," *IEEE Design & Test*, Vol. 38, No. 2, April, 2021 (* indicates equal contributions in alphabetical order)

[J12] Junzhe Cai, Changhao Yan, Yudong Tao, Yibo Lin, Shengguo Wang, David Z. Pan, and Xuan Zeng, "A Novel and Unified Full-chip CMP Model Aware Dummy Fill Insertion Framework with SQP-Based Optimization Method," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 40, no. 3, pp. 603-607, March 2021.

[J13] Mohamed Baker Alawieh, Yibo Lin, Zaiwei Zhang, Meng Li, Qixing Huang, and David Z. Pan, "GAN-SRAF: Sub-Resolution Assist Feature Generation using Generative Adversarial Networks," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 40, no. 2, pp. 373-385, Feb. 2021.

[J14] Yibai Meng, Wuxi Li, Yibo Lin and David Z. Pan, "elfPlace: Electrostatics-based Placement for Large-Scale Heterogeneous FPGAs," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Publication date Jan. 2021

[J15] Wei Li, Yuzhe Ma, Qi Sun, Lu Zhang, Yibo Lin, Iris Hui-Ru Jiang, Bei Yu, and David Z. Pan, "OpenMPL: An Open Source Layout Decomposer", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Publication Dec. 2020.

[J16] Xiyuan Tang, Xiangxing Yang, Wenda Zhao, Chen-Kai Hsu, Jiaxin Liu, Linxiao Shen, Abhishek Mukherjee, Wei Shi, Shaolan Li, David Z. Pan, and Nan Sun, "A 13.5-ENOB, 107-μW Noise-Shaping SAR ADC with PVT-Robust Closed-Loop Dynamic Amplifier," *IEEE Journal of Solid-State Circuits (JSSC)*, Vol. 55, No. 12, pp. 3248-3259, Dec. 2020.

[J17] Ying, Zhoufeng, Chenghao Feng, Zheng Zhao, Jiaqi Gu, Richard Soref, David Z. Pan, and Ray T. Chen, "Sequential logic and pipelining in chip-based electronic-photonic digital computing," *IEEE Photonics Journal*, Vol. 12, no. 6, Dec. 2020

[J18] Yibo Lin, Wuxi Li, Jiaqi Gu, Haoxing Ren, Brucek Khailany, "ABCDPlace: Accelerated Batch-based Concurrent Detailed Placement on Multi-threaded CPUs and GPUs," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 39, no. 12, pp. 5083-5096, Dec. 2020.

[J19] Hao Chen*, Mingjie Liu*, Xiyuan Tang*, Keren Zhu*, Nan Sun and David Z. Pan, "Challenges and Opportunities Toward Fully Automated Analog Layout Design," *Journal of Semiconductors*, Vol. 41, no. 11, Nov. 2020 **(Invited Paper)** (* in alphabetic order)

[J20] Jiaqi Gu, Zheng Zhao, Chenghao Feng, Zhoufeng Ying, Mingjie Liu, Ray T. Chen, and David Z. Pan, "Towards Hardware-Efficient Optical Neural Networks: Beyond FFT Architecture via Joint Learnability," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Publication Date: Sept. 2020

[J21] Chenghao Feng, Zhoufeng Ying, Zheng Zhao, Jiaqi Gu, David Z. Pan, and Ray T. Chen, "Wavelength-division-multiplexing (WDM)-based integrated electronic–photonic switching network (EPSN) for high-speed data processing and transportation," *Nanophotonics,* Vol. 9, No. 15*,* Sept. 2020.

[J22] Xiyuan Tang, Shaolan Li, Xiangxing Yang, Linxiao Shen, Wenda Zhao, Randall P. Williams, Jiaxin Liu, Zhichao Tan, Neal A. Hall, David Z. Pan, and Nan Sun, "An Energy-Efficient Time-Domain Incremental Zoom Capacitance-to-Digital Converter," *IEEE Journal of Solid-State Circuits (JSSC)*, Vol. 55, No. 11, pp. 3064-3075, Nov. 2020.

[J23] Jing Chen, Mohamed Baker Alawieh, Yibo Lin, Maolin Zhang, Jun Zhang, Yufeng Guo, and David Z. Pan, "Automatic Selection of Structure Parameters of Silicon on Insulator Lateral Power Device Using Bayesian Optimization," *IEEE Electron Device Letters*, vol. 41, no. 9, pp. 1288-1291, Sept. 2020.

[J24] Shaolan Li, David Z. Pan, and Nan Sun, "An OTA-Less Second-Order VCO-Based CT ΔΣ Modulator Using an Inherent Passive Integrator and Capacitive Feedback," *IEEE Journal of Solid-State Circuits (JSSC)*, Vol. 55, No. 5, pp. 1337-1350, May 2020.

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B. Refereed Conference Proceedings

[C1] Hanqing Zhu, Keren Zhu, Jiaqi Gu, Harrison Jin, Ray Chen, Jean Anne Incorvia, and David Z. Pan, "Fuse and Mix: MACAM-Enabled Analog Activation for Energy-Efficient Neural Acceleration," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Diego, CA, Oct. 30–Nov. 3, 2022.

[C2] Keren Zhu, Hao Chen, Walker Turner, George Kokai, Po-Hsuan Wei, David Z. Pan, and Haoxing Ren, "TAG: Learning Circuit Spatial Embedding From Layouts," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Diego, CA, Oct. 30–Nov. 3, 2022.

[C3] Wei Shi, Hanrui Wang, Jiaqi Gu, Mingjie Liu, David Z. Pan, Song Han, and David Z. Pan, "RobustAnalog: Fast Variation-Aware Analog Circuit Design Via Multi-task RL," *ACM/IEEE Workshop on Machine Learning for CAD (MLCAD)*, Snowbird, Utah, Sept. 12-13, 2022.

[C4] Zixuan Jiang, Mingjie Liu, Zizheng Guo, Shuhan Zhang, Yibo Lin, and David Z. Pan, "A Tale of EDA's Long Tail: Long-Tailed Distribution Learning for Electronic Design Automation," *ACM/IEEE Workshop on Machine Learning for CAD (MLCAD)*, Snowbird, Utah, Sept. 12-13, 2022.

[C5] Jiaqi Gu, Hanqing Zhu, Chenghao Feng, Zixuan Jiang, Mingjie Liu, Shuhan Zhang, Ray T. Chen, and David Z. Pan, "ADEPT: Automatic Differentiable DEsign of Photonic Tensor Cores," *ACM/IEEE Design Automation Conference (DAC)*, San Francisco, CA, July 10-14, 2022.

[C6] Hanrui Wang, Zirui Li, Jiaqi Gu, Yongshan Ding, David Z. Pan, and Song Han, "QOC: Quantum On-Chip Training with Parameter Shift and Gradient Pruning," *ACM/IEEE Design Automation Conference (DAC)*, San Francisco, CA, July 10-14, 2022.

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[C8] Zizheng Guo*, Mingjie Liu*, Jiaqi Gu, Shuhan Zhang, David Z. Pan, and Yibo Lin, "A Timing Engine Inspired Graph Neural Network Model for Pre-Routing Slack Prediction," *ACM/IEEE Design Automation Conference (DAC)*, San Francisco, CA, July 10-14, 2022. (* indicates equal contributions)

[C9] Jiaqi Gu, Hyoukjun Kwon, Dilin Wang, Wei Ye, Meng Li, Yu-Hsin Chen, Liangzhen Lai, Vikas Chandra, and David Z. Pan, "Multi-Scale High-Resolution Vision Transformer for Semantic Segmentation," *IEEE/CVF Conference on Computer Vision and Pattern Recognition (CVPR)*, New Orleans, Louisiana, Jun. 21-24, 2022.

[C10] Venkata Suresh Rayudu, Ki Yong Kim, David Z. Pan, and Ranjit Gharpurey, "A Feedback-Based N-Path Receiver with Reduced Input-Node Harmonic Response," *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Denver, CO, Jun. 19-21, 2022.

[C11] Gracieli Posser, Evangeline F.Y. Young, Stephan Held, Yih-Lang Li, and David Z. Pan, "Challenges and Approaches in VLSI Routing," *ACM International Symposium on Physical Design (ISPD),* 2022. **(Invited Paper)**

[C12] Hao Chen, Walker J. Turner, Sanquan Song, Keren Zhu, George F. Kokai, Brian Zimmer, C. Thomas Gray, Brucek Khailany, David Z. Pan, and Haoxing Ren, "AutoCRAFT: Layout Automation for Custom Circuits in Advanced FinFET Technologies," *ACM International Symposium on Physical Design (ISPD),* 2022. **(Invited Paper)**

[C13] Hao Chen, Walker J. Turner, David Z. Pan, and Haoxing Ren, "Routability-Aware Placement for Advanced FinFET Mixed-Signal Circuits using Satisfiability Modulo Theories," *IEEE Design, Automation & Test in Europe (DATE) Conference*, March 14-23, 2022.

[C14] Hanrui Wang, Yongshan Ding, Jiaqi Gu, Yujun Lin, David Z. Pan, Fred Chong, and Song Han, "QuantumNAS: Noise-Adaptive Search for Robust Quantum Circuits," *The 28th IEEE International Symposium on High-Performance Computer Architecture (HPCA-28)*, Feb. 12-16, Seoul, South Korea, 2022.

[C15] Ahmet F. Budak*, Zixuan Jiang*, Keren Zhu, Azalia Mirhoseini, Anna Goldie, and David Z. Pan, "Reinforcement Learning for Electronic Design Automation: Case Studies and Perspectives," *IEEE/ACM Asian and South Pacific Design Automation Conference (ASP-DAC)*, Jan. 17-20, 2022. (**Invited Paper**) (* equal contributions in alphabetic order)

[C16] Keren Zhu, Hao Chen, Mingjie Liu, and David Z. Pan, "Automating Analog Constraint Extraction: From Heuristics to Learning," *IEEE/ACM Asian and South Pacific Design Automation Conference (ASP-DAC)*, Jan. 17-20, 2022. (**Invited Paper**)

[C17] Keren Zhu, Hao Chen, Mingjie Liu, Xiyuan Tang, Wei Shi, Nan Sun, and David Z. Pan, "Generative-Adversarial-Network-Guided Well-Aware Placement for Analog Circuits," *IEEE/ACM Asian and South Pacific Design Automation Conference (ASP-DAC)*, Jan. 17-20, 2022.

[C18] Rachel Selina Rajarathnam, Mohamed Baker Alawieh, Zixuan Jiang, Mahesh Iyer, and David Z. Pan, "DREAMPlaceFPGA: an open-source analytical placer for large scale heterogeneous FPGAs using deep-learning toolkit," *IEEE/ACM Asian and South Pacific Design Automation Conference (ASP-DAC)*, Jan. 17-20, 2022.

[C19] Hanqing Zhu, Jiaqi Gu, Chenghao Feng, Mingjie Liu, Zixuan Jiang, Ray T. Chen, and David Z. Pan, "ELight: Enabling Efficient Photonic In-Memory Neurocomputing with Life Enhancement," *IEEE/ACM Asian and South Pacific Design Automation Conference (ASP-DAC)*, Jan. 17-20, 2022.

[C20] Jiaqi Gu, Hanqing Zhu, Chenghao Feng, Zixuan Jiang, Ray T. Chen, and David Z. Pan, "L2ight: Enabling On-Chip Learning for Optical Neural Networks via Efficient in-situ Subspace Optimization," *Conference on Neural Information Processing Systems (NeurIPS)*, Dec. 7-10, 2021.

[C21] Jiaqi Gu, Hanqing Zhu, Chenghao Feng, Mingjie Liu, Zixuan Jiang, Ray T. Chen, and David Z. Pan, "Towards Memory-Efficient Neural Networks via Multi-Level in situ Generation**,"** *International Conference on Computer Vision (ICCV)*, Oct. 10-17, 2021.

[C22] Mingjie Liu, Xiyuan Tang, Keren Zhu, Hao Chen, Nan Sun, and David Z. Pan, "OpenSAR: An Open Source Automated End-to-end SAR ADC Compiler," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, November 1-4, 2021

[C23] Zixuan Jiang, Ebrahim Songhori, Shen Wang, Anna Goldie, Azalia Mirhoseini, Joe Jiang, Young-Joon Lee, and David Z. Pan, "Delving into Macro Placement with Reinforcement Learning," *ACM/IEEE Workshop on Machine Learning for CAD (MLCAD)*, Aug. 31 – Sept. 2, 2021.

[C24] Mohamed Baker Alawieh and David Z. Pan, "ADAPT: An Adaptive Machine Learning Framework with Application to Lithography Hotspot Detection," *ACM/IEEE Workshop on Machine Learning for CAD (MLCAD)*, Aug. 31 – Sept. 2, 2021.

[C25] Ahmet F. Budak, Prateek Bhansali, Bo Liu, Nan Sun, David Z. Pan, and Chandramouli V. Kashyap, "DNN-Opt: An RL Inspired Optimization for Analog Circuit Sizing using Deep Neural Networks," *ACM/IEEE Design Automation Conference (DAC),* San Francisco, CA, Dec. 5-9, 2021. (**one of the five Best Paper Candidates, out of 900+ submissions**)

[C26] Hao Chen, Keren Zhu, Mingjie Liu, Xiyuan Tang, Nan Sun, and David Z. Pan, "Universal Symmetry Constraint Extraction for Analog and Mixed-Signal Circuits with Graph Neural Networks," *ACM/IEEE Design Automation Conference (DAC),* San Francisco, CA, Dec. 5-9, 2021.

[C27] Xiaohan Gao, Mingjie Liu, David Z. Pan and Yibo Lin, "Interactive Analog Layout Editing with Instant Placement Legalization," *ACM/IEEE Design Automation Conference (DAC),* San Francisco, CA, Dec. 5-9, 2021.

[C28] Jason Midkiff, Ali Rostamian, Kyoung Min Yoo, Aref Asghari, Chao Wang, Chenghao Feng, Zhoufeng Ying, Jiaqi Gu, Haixia Mei, Ching-Wen Chang, James Fang, Alan Huang, Jong-Dug Shin, Xiaochuan Xu, Michael Bukshtab, David Z. Pan, and Ray T. Chen, "Integrated Photonics for Computing, Interconnects and Sensing", *Conference on Lasers and Electro-Optics,* May 2021. **(Invited Paper)**

[C29] Xiangxing Yang, Keren Zhu, Xiyuan Tang, Meizhi Wang, Mingtao Zhan, Nanshu Lu, Jaydeep P. Kulkarni, David Z. Pan, Yongpan Liu and Nan Sun, "An In-Memory-Computing Charge-Domain Ternary CNN Classifier," *IEEE Custom Integrated Circuits Conference (CICC),* April 25-30, 2021. (**Best Student Paper Award Candidate**)

[C30] Hao Chen*, Mingjie Liu*, Xiyuan Tang*, Keren Zhu*, Abhishek Mukherjee, Nan Sun and David Z. Pan, "MAGICAL 1.0: An Open-Source Fully-Automated AMS Layout Synthesis Framework Verified With a 40-nm 1GS/s ΔΣ ADC," *IEEE Custom Integrated Circuits Conference (CICC),* April 25-31, 2021. (* equal contributions in alphabetic order)

[C31] Xiangxing Yang, Keren Zhu, Xiyuan Tang, Meizhi Wang, Mingtao Zhan, Nanshu Lu, Jaydeep P. Kulkarni, David Z. Pan, Yongpan Liu and Nan Sun, "An In-Memory-Computing Charge-Domain Ternary CNN Classifier," *IEEE Custom Integrated Circuits Conference (CICC)*, April 25-31, 2021.

[C32] Jiaqi Gu, Chenghao Feng, Zheng Zhao, Zhoufeng Ying, Ray T. Chen and David Z. Pan, "Efficient On-Chip Learning for Optical Neural Networks Through Power-Aware Sparse Zeroth-Order Optimization," *Association for the Advancement of Artificial Intelligence (AAAI)*, Feb. 2-9, 2021.

[C33] Shubham Rai, Walter Lau Neto, Yukio Miyasaka, Xinpei Zhang, Mingfei Yu, Qingyang Yi Masahiro Fujita, Guilherme B. Manske, Matheus F. Pontes, Leomar S. da Rosa Junior, Marilton S. de Aguiar, Paulo F. Butzen, Po-Chun Chien, Yu-Shan Huang, Hoa-Ren Wang, Jie-Hong R. Jiang, Jiaqi Gu, Zheng Zhao, Zixuan Jiang, David Z. Pan, Brunno A. de Abreu, Isac de Souza Campos, Augusto Berndt, Cristina Meinhardt, Jonata T. Carvalho, Mateus Grellert, Sergio Bampi, Aditya Lohana, Akash Kumar, Wei Zeng, Azadeh Davoodi, Rasit O. Topaloglu, Yuan Zhou, Jordan Dotzel, Yichi Zhang, Hanyu Wang, Zhiru Zhang, Valerio Tenace, Pierre-Emmanuel Gaillardon, Alan Mishchenko and Satrajit Chatterjee, "Logic Synthesis Meets Machine Learning: Trading Exactness for Generalization," *IEEE/ACM Design, Automation & Test in Europe (DATE) Conference*, Feb. 1-5, 2021 **(Invited Paper)** https://arxiv.org/pdf/2012.02530.pdf

[C34] Jiaqi Gu, Chenghao Feng, Zheng Zhao, Zhoufeng Ying, Mingjie Liu, Ray T. Chen and David Z. Pan, "SqueezeLight: Towards Scalable Optical Neural Networks with Multi-Operand Ring Resonators," *IEEE Design, Automation & Test in Europe (DATE) Conference*, Feb. 1-5, 2021.

[C35] Jiaqi Gu, Zheng Zhao, Chenghao Feng, Zhoufeng Ying, Ray T. Chen and David Z. Pan, "O2NN: Optical Neural Networks with Differential Detection-Enabled Optical Operands," *IEEE Design, Automation & Test in Europe (DATE) Conference*, Feb. 1-5, 2021.

[C36] Mingjie Liu, Walker Turner, George Kokai, Brucek Khailany, David Z. Pan and Haoxing Ren, "Parasitic-Aware Analog Circuit Sizing with Graph Neural Networks and Bayesian Optimization," *IEEE Design, Automation & Test in Europe (DATE) Conference*, Feb. 1-5, 2021.

[C37] Xiaohan Gao, Chenhui Deng, Mingjie Liu, Zhiru Zhang, David Z. Pan, and Yibo Lin, "Layout Symmetry Annotation for Analog Circuits with Graph Neural Networks," *IEEE/ACM Asian and South Pacific Design Automation Conference (ASP-DAC)*, Jan. 18-21, 2021.

[C38] Keren Zhu, Mingjie Liu, Hao Chen, Zheng Zhao and David Z. Pan, "Exploring Logic Optimizations with Reinforcement Learning and Graph Convolutional Network," *ACM/IEEE Workshop on Machine Learning for CAD (MLCAD)*, November 16-20, 2020.

[C39] Keren Zhu, Hao Chen, Mingjie Liu, Xiyuan Tang, Nan Sun and David Z. Pan, "Effective Analog/Mixed-Signal Circuit Placement Considering System Signal Flow," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, November 02-05, 2020. (**Best Paper Award Nomination from Track)**

[C40] Hao Chen, Keren Zhu, Mingjie Liu, Xiyuan Tang, Nan Sun and David Z. Pan, "Toward Silicon-Proven Detailed Routing for Analog and Mixed-Signal Circuits," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, November 02-05, 2020.

[C41] Jiaqi Gu, Zixuan Jiang, Yibo Lin and David Z. Pan, "DREAMPlace 3.0: Multi-Electrostatics Based Robust VLSI Placement with Region Constraints," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, November 02-05, 2020.

[C42] Mohamed Baker Alawieh, Wei Ye, and David Z. Pan, "Re-examining VLSI Manufacturing and Yield through the Lens of Deep Learning," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, November 02-05, 2020 (**Invited Paper**)

[C43] Rachel Selina Rajarathnam, Yibo Lin, Yier Jin, and David Z. Pan, "ReGDS: A Reverse Engineering Framework from GDSII to Gate-level Netlist," *IEEE International Symposium on Hardware Oriented Security and Trust (HOST)*, San Jose, Dec. 6-9, 2020

[C44] Zixuan Jiang, Keren Zhu, Mingjie Liu, Jiaqi Gu, and David Z. Pan, "An Efficient Training Framework for Reversible Neural Architectures," *European Conference on Computer Vision (ECCV)*, Aug. 23-28, 2020

[C45] Jiaqi Gu, Zheng Zhao, Chenghao Feng, Wuxi Li, Ray T. Chen and David Z. Pan, "FLOPS: Efficient On-Chip Learning for Optical Neural Networks through Stochastic Zeroth-Order Optimization," *ACM/IEEE Design Automation Conference (DAC)*, July 19-23, 2020. **(Best Paper Candidate;** total 6 best paper candidates, from nearly 1,000 submissions**)**

[C46] Mingjie Liu, Keren Zhu, Xiyuan Tang, Biying Xu, Wei Shi, Nan Sun and David Z. Pan, "Closing the Design Loop: Bayesian Optimization Assisted Hierarchical Analog Layout Synthesis", *ACM/IEEE Design Automation Conference (DAC),* July 19-23, 2020.

[C47] Mohamed Baker Alawieh, Duane Boning and David Z. Pan, "Wafer Map Defect Patterns Classification using Deep Selective Learning," *ACM/IEEE Design Automation Conference (DAC),* July 19-23, 2020.

[C48] Navid Khoshavi, Arman Roohi, Connor Broyles, Saman Sargolzaei, Yu Bi and David Z. Pan, "SHIELDeNN: Online Accelerated Framework for Fault-Tolerant Deep Neural Network Architectures," *ACM/IEEE Design Automation Conference (DAC)*, July 19-23, 2020.

[C49] Chenghao Feng, Zheng Zhao, Zhoufeng Ying, Jiaqi Gu, David Z Pan, and Ray T Chen, "Compact Design of On-chip Elman Optical Recurrent Neural Network," *OSA Conference on Lasers and Electro-Optics (CLEO)*: Applications and Technology, May 10-15, 2020. https://doi.org/10.1364/CLEO_AT.2020.JTh2B.8

[C50] Chenghao Feng, Zhoufeng Ying, Zheng Zhao, Jiaqi Gu, David Z. Pan, and Ray T. Chen, "Integrated WDM-based Optical Comparator for High-speed Computing," *OSA Conference on Lasers and Electro-Optics (CLEO)*: Science and Innovations, pp. SM3O.1. May 10-15, 2020. https://doi.org/10.1364/CLEO_SI.2020.SM3O.1

[C51] Wei Ye, Mohamed Baker Alawieh, Yuki Watanabe, Shigeki Nojima, Yibo Lin and David Z. Pan, "TEMPO: Fast Mask Topography Effect Modeling with Deep Learning," *ACM International Symposium on Physical Design (ISPD),* 2020. **(Best Paper Award)** https://doi.org/10.1145/3372780.3375565

[C52] Mingjie Liu*, Keren Zhu*, Jiaqi Gu, Linxiao Shen, Xiyuan Tang, Nan Sun and David Z. Pan, "Towards Decrypting the Art of Analog Layout, Placement Quality Prediction via Transfer Learning," *IEEE Design, Automation & Test in Europe (DATE)*, Mar. 09-13, 2020. (* indicates equal contributions in alphabetical order) https://doi.org/10.23919/DATE48585.2020.9116330

[C53] Jiaqi Gu, Zheng Zhao, Chenghao Feng, Hanqing Zhu, Ray T. Chen, David Z. Pan, "ROQ: A Noise-Aware Quantization Scheme Towards Robust Optical Neural Networks with Low-bit Controls," *IEEE Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Grenoble, France, Mar. 09-13, 2020

[C54] Chenghao Feng, Zhoufeng Ying, Zheng Zhao, Jiaqi Gu, David Z. Pan, and Ray T. Chen, "Wavelength-division-multiplexing-based electronic-photonic network for high-speed computing," *SPIE OPTO Proceedings Volume 11284, Smart Photonic and Optoelectronic Integrated Circuits XXII;* 112840H, March 9, 2020. https://doi.org/10.1117/12.2551323

[C55] Xiyuan Tang, Xiangxing Yang, Wenda Zhao, Chen-Kai Hsu, Jiaxin Liu, Linxiao Shen, Abhishek Mukherjee, Wei Shi, David Z. Pan and Nan Sun, "A 13.5b-ENOB Second-Order Noise-Shaping SAR with PVT-Robust Closed-Loop Dynamic Amplifier," *IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, Feb. 16-20, 2020.

[C56] Jiaqi Gu, Zheng Zhao, Chenghao Feng, Mingjie Liu, Ray T. Chen, David Z. Pan, "Towards Area-Efficient Optical Neural Networks: An FFT-based Architecture," *IEEE/ACM Asian and South Pacific Design Automation Conference (ASP-DAC)*, Beijing, China, Jan. 13-16, 2020. **(Best Paper Award)**

[C57] Mingjie Liu, Wuxi Li, Keren Zhu, Biying Xu, Yibo Lin, Linxiao Shen, Xiyuan Tang, Nan Sun and David Z. Pan, "S^{3}DET: Detecting System Symmetry Constraints for Analog Circuits with Graph Similarity," *IEEE/ACM Asian and South Pacific Design Automation Conference (ASP-DAC)*, Beijing, China, Jan. 13-16, 2020. **(Best Paper Award Nomination)**

[C58] Mohamed Baker Alawieh, Wuxi Li, Yibo Lin, Love Singhal, Mahesh Iyer and David Z. Pan, "High-Definition Routing Congestion Prediction for Large-Scale FPGAs," *IEEE/ACM Asian and South Pacific Design Automation Conference (ASP-DAC)*, Beijing, China, Jan. 13-16, 2020.

[C59] Biying Xu, Mingjie Liu, Keren Zhu, Yibo Lin, Shaolan Li, Xiyuan Tang, Nan Sun, and David Z. Pan, "MAGICAL: Toward Fully Automated Analog IC Layout Leveraging Human and Machine Intelligence," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Westminster, CO, Nov. 4-7, 2019 **(Invited Paper)**

[C60] Zheng Zhao, Zhoufeng Ying, Chenghao Feng, Jiaqi Gu, Ray T. Chen, and David Z. Pan, "Design Technology for Scalable and Robust Photonic Integrated Circuits," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Westminster, CO, Nov. 4-7, 2019 **(Invited Paper)**

[C61] Keren Zhu, Mingjie Liu, Yibo Lin, Biying Xu, Shaolan Li, Xiyuan Tang, Nan Sun and David Z. Pan, "GeniusRoute: A New Analog Routing Paradigm Using Generative Neural Network Guidance," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Westminster, CO, Nov. 4-7, 2019 **(Best Paper Award Nomination from Track)**

[C62] Wuxi Li, Yibo Lin, and David Z. Pan, "elfPlace: Electrostatics-based Placement for Large-Scale Heterogeneous FPGAs," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Westminster, CO, Nov. 4-7, 2019

[C63] Chengyue Gong, Zixuan Jiang, Dilin Wang, Yibo Lin, Qiang Liu and David Z. Pan, "Mixed Precision Neural Architecture Search for Energy Efficient Deep Learning," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Westminster, CO, Nov. 4-7, 2019

[C64] Kaveh Shamsi, David Z. Pan and Yier Jin, "IcySAT: Improved SAT-based Attacks on Cyclic Locked Circuits," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Westminster, CO, Nov. 4-7, 2019

[C65] Shounak Dhar, Love Singhal, Mahesh A. Iyer and David Z. Pan, "FPGA Accelerated Spreading for Global Placement," 23rd *IEEE High Performance Extreme Computing Conference (HPEC)***,** Boston, September 24-26, 2019

[C66] Shounak Dhar, Love Singhal, Mahesh A. Iyer and D. Z. Pan, "*FPGA Accelerated FPGA Placement*," 29th International Conference on Field Programmable Logic and Applications (FPL), Barcelona, Spain, September 9-11, 2019

[C67] Yibo Lin, Shounak Dhar, Wuxi Li, Haoxing Ren, Brucek Khailany and David Z. Pan, "DREAMPlace: Deep Learning Toolkit Enabled GPU Acceleration for Modern VLSI Placement," *ACM/IEEE Design Automation Conference (DAC)*, Las Vegas, NV, Jun. 2-6, 2019. **(Best Paper Award)**

[C68] Wei Ye, Mohamed Baker Alawieh, Yibo Lin, and David Z. Pan, "LithoGAN: End-to-End Lithography Modeling with Generative Adversarial Networks," *ACM/IEEE Design Automation Conference (DAC)*, Las Vegas, NV, Jun. 2-6, 2019. **(Best Paper Award Candidate)**

[C69] Biying Xu, Yibo Lin, Xiyuan Tang, Shaolan Li, Linxiao Shen, Nan Sun and David Z. Pan, "WellGAN: Generative-Adversarial-Network-Guided Well Generation for Analog/Mixed-Signal Circuit Layout," *ACM/IEEE Design Automation Conference (DAC)*, Las Vegas, NV, Jun. 2-6, 2019.

[C70] Mohamed Baker Alawieh, Yibo Lin, Zaiwei Zhang, Meng Li, Qixing Huang and David Z. Pan, "GAN-SRAF: Sub-Resolution Assist Feature Generation using Conditional Generative Adversarial Networks," *ACM/IEEE Design Automation Conference (DAC)*, Las Vegas, NV, Jun. 2-6, 2019.

[C71] Mohamed Baker Alawieh, Sinead Williamson and David Z. Pan, "Rethinking Sparsity in Performance Modeling for Analog and Mixed Circuits using Spike and Slab Models," *ACM/IEEE Design Automation Conference (DAC)*, Las Vegas, NV, Jun. 2-6, 2019.

[C72] Kaveh Shamsi, David Z. Pan and Yier Jin, "On the Impossibility of Approximation-Resilient Circuit Locking," *IEEE International Symposium on Hardware Oriented Security and Trust (HOST)*, Tysons Corner, USA, May 6-10, 2019

[C73] Shaolan Li, Wenda Zhao, Biying Xu, Xiangxing Yang, Xiyuan Tang, Linxiao Shen, Nanshu Lu, David Z. Pan and Nan Sun, "A 0.025mm^2 0.8V 78.5dB SNDR VCO-based Sensor Readout Circuit Using a Hybrid PLL-$\Delta\Sigma$ Structure," *IEEE Custom Integrated Circuits Conference (CICC)*, Austin, TX, Apr. 14-17, 2019.

[C74] Shaolan Li, Biying Xu, David Z. Pan and Nan Sun, "A 60-fJ/step 11-ENOB VCO-based CTDSM Synthesized from Digital Standard Cell Library," *IEEE Custom Integrated Circuits Conference (CICC)*, Austin, TX, Apr. 14-17, 2019

[C75] Biying Xu, Shaolan Li, Chak-Wa Pui, Derong Liu, Linxiao Shen, Yibo Lin, Nan Sun, and David Z. Pan, "Device Layer-Aware Analytical Placement for Analog Circuits," *ACM International Symposium on Physical Design (ISPD),* San Francisco, CA, April 14-17, 2019. **(Best Paper Award Nomination)**

[C76] Kaveh Shamsi, Meng Li, David Z. Pan and Yier Jin, "KC2: Key-Condition Crunching for Fast Sequential Circuit Deobfuscation," *IEEE Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Florence, Italy, March 25-29, 2019. **(Best Paper Award Candidate)**

[C77] Wei Ye, Mohamed Baker Alawieh, Meng Li, Yibo Lin, and David Z. Pan, "Litho-GPA: Gaussian Process Assurance for Lithography Hotspot Detection," *IEEE Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Florence, Italy, March 25-29, 2019.

[C78] Zheng Zhao, Derong Liu, Zhoufeng Ying, Biying Xu, Chenghao Feng, Ray T. Chen. and David Z. Pan, "Exploiting Wavelength Division Multiplexing for Optical Logic Synthesis," *IEEE Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Florence, Italy, March 25-29, 2019.

[C79] Zhoufeng Ying, Zheng Zhao, Chenghao Feng, Rohan Mital, Shounak Dhar, David Z. Pan, Ray T. Chen, "Automated logic synthesis for electro-optic computing in integrated photonics," *SPIE OPTO Proceedings Volume 10924, Optical Interconnects XIX*; 109240H (March 2019) https://doi.org/10.1117/12.2510363

[C80] Wuxi Li, Mehrdad Eslami Dehkordi, Stephen Yang and David Z. Pan, "Simultaneous Placement and Clock Tree Construction for Modern FPGAs," *ACM International Symposium on Field-Programmable Gate Arrays (FPGA)*, Seaside, CA, February 24 - 26, 2019.

[C81] Wei Ye, Yibo Lin, Meng Li, Qiang Liu, and David Z. Pan, "LithoROC: lithography hotspot detection with explicit ROC optimization," *IEEE/ACM Asian and South Pacific Design Automation Conference (ASP-DAC)*, Tokyo, Jan. 21–24, 2019 **(Invited Paper)**

[C82] Shounak Dhar, Love Singhal, Mahesh A. Iyer and David Z. Pan, "A Shape-Driven Spreading Algorithm Using Linear Programming for Global Placement," *IEEE/ACM Asian and South Pacific Design Automation Conference (ASP-DAC)*, Tokyo, Jan. 21–24, 2019.

[C83] Wei Ye, Mohamed Baker Alawieh, Yibo Lin, and David Z. Pan, "Tackling Signal Electromigration with Learning-Based Detection and Multistage Mitigation," *IEEE/ACM Asian and South Pacific Design Automation Conference (ASP-DAC)*, Tokyo, Jan. 21–24, 2019.

[C84] Ying Chen, Yibo Lin, Tianyang Gai, Yajuan Su, Yayi Wei, and David Z. Pan, "Semi-Supervised Hotspot Detection with Self-Paced Multi-Task Learning," *IEEE/ACM Asian and South Pacific Design Automation Conference (ASP-DAC)*, Tokyo, Jan. 21–24, 2019.

[C85] Mohamed Baker Alawieh, Xiyuan Tang and David Z. Pan, "S^2-PM: Semi-Supervised Learning for Efficient Performance Modeling of Analog and Mixed Signal Circuits," *IEEE/ACM Asian and South Pacific Design Automation Conference (ASP-DAC)*, Tokyo, Jan. 21–24, 2019.

[C86] Zheng Zhao, Derong Liu, Meng Li, Zhoufeng Ying, Biying Xu, Lu Zhang, Bei Yu, Ray T. Chen, and David Z. Pan, "Hardware-software Co-design of Slimmed Optical Neural Networks," *IEEE/ACM Asian and South Pacific Design Automation Conference (ASP-DAC)*, Tokyo, Jan. 21–24, 2019.

[C87] Yibo Lin, Mohamed Baker Alawieh, Wei Ye, and David Z. Pan, "Machine Learning for Yield Learning and Optimization," *IEEE International Test Conference (ITC)*, Oct. 2018 **(Invited Paper)**

[C88] Meng Li, Kaveh Shamsi, Yier Jin, and David Z. Pan, "TimingSAT: Decamouflaging Timing-based Logic Obfuscation," *IEEE International Test Conference (ITC)*, Oct. 2018

[C89] Shounak Dhar and David Z. Pan, "GDP: GPU accelerated Detailed Placement," *IEEE High Performance Extreme Computing Conference (HPEC)*, Boston, Sept. 25-27, 2018

[C90] Derong Liu, Zheng Zhao, Zheng Wang, Zhoufeng Ying, Ray T. Chen, and David Z. Pan, "OPERON: Optical-electrical Power-efficient Route Synthesis for On-chip Signals," *ACM/IEEE Design Automation Conference (DAC)*, San Francisco, June 24-28, 2018

[C91] Kaveh Shamsi, Meng Li, David Z. Pan, and Yier Jin, "Cross-Lock: Dense Layout-Level Interconnect Locking using Cross-bar Architectures," *ACM Great Lakes Symposium on VLSI* (*GLSVLSI*), Chicago, Illinois, May 23-25, 2018. **(Best Paper Award)**

[C92] Biying Xu, Bulent Basaran, Ming Su, and David Z. Pan, "Analog Placement Constraint Extraction and Exploration with the Application to Layout Retargeting," *ACM International Symposium on Physical Design (ISPD),* Monterey, CA, Mar. 25-28, 2018.

[C93] Wei Ye, Meng Li, Kai Zhong, Bei Yu, and David Z. Pan, "Power Grid Reduction by Sparse Convex Optimization," *ACM International Symposium on Physical Design (ISPD),* Monterey, CA, Mar. 25-28, 2018.

[C94] Yibo Lin, Yuki Watanabe, Taiki Kimura, Tetsuaki Matsunawa, Shigeki Nojima, Meng Li, and David Z. Pan, "Data Efficient Lithography Modeling with Residual Neural Networks and Transfer Learning," *ACM International Symposium on Physical Design (ISPD),* Monterey, CA, Mar. 25-28, 2018.

[C95] Meng Li, Bei Yu, Yibo Lin, Xiaoqing Xu, Wuxi Li, and David Z. Pan, "A Practical Split Manufacturing Framework for Trojan Prevention via Simultaneous Wire Lifting and Cell Insertion," *IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Jeju Island, Korea, Jan. 22-25, 2018.

[C96] Zheng Zhao, Zheng Wang, Zhoufeng Ying, Shounak Dhar, Ray T. Chen, and David Z. Pan, "Logic Synthesis for Energy-Efficient Photonic Integrated Circuits," *IEEE/ACM Asian and South Pacific Design Automation Conference (ASP-DAC)*, Jeju Island, Korea, Jan. 22-25, 2018.

[C97] Che-Lun Hsu, Shaofeng Guo, Yibo Lin, Xiaoqing Xu, Meng Li, Runsheng Wang, Ru Huang, and David Z. Pan, "Layout-Dependent Aging Mitigation for Critical Path Timing," *IEEE/ACM Asian and South Pacific Design Automation Conference (ASP-DAC)*, Jeju Island, Jan. 22-25, 2018.

[C98] Wuxi Li, Meng Li, Jiajun Wang, and David Z. Pan, "UTPlaceF 3.0: A Parallelization Framework for Modern FPGA Global Placement," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Irvine, CA, Nov. 13-16, 2017. **(Invited Paper)**

[C99] Jiaojiao Ou, Xiaoqing Xu, Brian Cline, Greg Yeric, and David Z. Pan, "DTCO for DSA-MP Hybrid Lithography with Double-BCP Materials in Sub-7nm Node," *IEEE International Conference on Computer Design (ICCD)*, Boston, MA, Nov. 5-8, 2017.

[C100] Yibo Lin, Peter Debacker, Darko Trivkovic, Ryoung-han Kim, Praveen Raghavan, and David Z. Pan, "Patterning Aware Design Optimization of Selective Etching in N5 and Beyond," *IEEE International Conference on Computer Design (ICCD)*, Boston, MA, Nov. 5-8, 2017.

[C101] Zheng Zhao, Zheng Wang, Zhoufeng Ying, Shounak Dhar, Ray T. Chen, and David Z. Pan, "Optical Computing on Silicon-on-Insulator-Based Photonic Integrated Circuits," *IEEE International Conference on ASIC (ASICON)*, Guiyang, China, Oct. 25-28, 2017. **(Invited Paper)**

[C102] Zheng Wang, Zhoufeng Ying, Shounak Dhar, Zheng Zhao, David Pan, and Ray T. Chen, "Nanophotonic devices for power-efficient computing and optical interconnects," *In IEEE Photonics Society Summer Topical Meeting Series (SUM), pp. 7-8,* July 2017. **(Invited Paper)**

[C103] Wei Ye, Yibo Lin, Xiaoqing Xu, Wuxi Li, Yiwei Fu, Yongsheng Sun, Canhui Zhan, and David Z. Pan, "Placement Mitigation Techniques for Power Grid Electromigration," *IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, Taipei, July 24-26, 2017.

[C104] Meng Li, Liangzhen Lai, Vikas Chandra, and David Z. Pan, "Cross-level Monte Carlo Framework for System Vulnerability Evaluation against Fault Attack," *ACM/IEEE Design Automation Conference (DAC)*, Austin, TX, June 18-22, 2017.

[C105] Biying Xu, Shaolan Li, Nan Sun, and David Z. Pan, "A Scaling Compatible, Synthesis Friendly VCO-based Delta-sigma ADC Design and Synthesis Methodology," *ACM/IEEE Design Automation Conference (DAC)*, Austin, TX, June 18-22, 2017.

[C106] Xiaoqing Xu, Yibo Lin, Vinicius Livramento, and David Z. Pan, "Concurrent Pin Access Optimization for Unidirectional Routing," *ACM/IEEE Design Automation Conference (DAC)*, Austin, TX, Jun. 18-22, 2017.

[C107] Derong Liu, Vinicius Livramento, Salim Chowdhury, Duo Ding, Huy Vo, Akshay Sharma, and David Z. Pan, "Streak: Synergistic Topology Generation and Route Synthesis for On-Chip Performance-Critical Signal Groups," *ACM/IEEE Design Automation Conference (DAC),* Austin, TX, June 18-22, 2017.

[C108] Travis Meade, Zheng Zhao, Shaojie Zhang, David Z. Pan, and Yier Jin**, "**Revisit Sequential Logic Obfuscation: Attacks and Defenses," *IEEE International Symposium on Circuits and Systems (ISCAS)*, Baltimore, MD, USA, May 28-31, 2017 **(Invited Paper)**

[C109] Zheng Wang, Zhoufeng Ying, Shounak Dhar, Zheng Zhao, David Z. Pan, and Ray T. Chen, "Optical Switches Based Carry-Ripple Adder for Future High-Speed and Low-Power Consumption Optical Computing," *In CLEO: Science and Innovations, pp. STh1N-2. Optical Society of America*, May 2017.

[C110] Zhoufeng Ying, Zheng Wang, Shounak Dhar, Zheng Zhao, David Z. Pan, and Ray T. Chen, "On-chip Microring Resonator Based Electro-optic Full Adder for Optical Computing," *In CLEO: QELS_Fundamental Science, pp. JW2A-147. Optical Society of America*, May 2017.

[C111] Kaveh Shamsi, Meng Li, Travis Meade, Zheng Zhao, David Z. Pan and Yier Jin, "Cyclic Obfuscation for Creating SAT-Unresolvable Circuits," *ACM Great Lakes Symposium on VLSI* (*GLSVLSI*), Banff, Alberta, Canada, May 10-12, 2017.

[C112] Kaveh Shamsi, Meng Li, Travis Meade, Zheng Zhao, David Z. Pan, and Yier Jin, "AppSAT: Approximately Deobfuscating Integrated Circuits," *IEEE International Symposium on Hardware Oriented Security and Trust (HOST)*, McLean, VA, USA, May 1-4, 2017 **(Best Paper Award)**

[C113] Jiaojiao Ou, Bei Yu, Xiaoqing Xu, Joydeep Mitra, Yibo Lin and David Z. Pan. "DSAR: DSA aware Routing with Simultaneous DSA Guiding Pattern and Double Patterning Assignment," *ACM International Symposium on Physical Design (ISPD),* Portland, OR, Mar. 19-22, 2017.

[C114] Biying Xu, Shaolan Li, Xiaoqing Xu, Nan Sun and David Z. Pan, "Hierarchical and Analytical Placement Techniques for High-Performance Analog Circuits," *ACM International Symposium on Physical Design (ISPD),* Portland, OR, Mar. 19-22, 2017.

[C115] Shounak Dhar, Mahesh Iyer, Saurabh Adya, Love Singhal, Nikolay Rubanov and David Pan, "An Effective Timing-Driven Detailed Placement Algorithm for FPGAs," *ACM International Symposium on Physical Design (ISPD)*, Portland, OR, Mar. 19-22, 2017.

[C116] Joydeep Mitra, Andres Torres, and David Z. Pan, "Process, Design Rule, and Layout Co-optimization for DSA Based Patterning of Sub-10nm Finfet Devices," *SPIE Intl. Symp. Advanced Lithography Conference*, San Jose, CA, Feb. 26 - Mar. 2, 2017

[C117] Joydeep Mitra, Andres Torres, and David Z. Pan, "Model Based Guiding Pattern Synthesis for On-target and Robust Assembly of Via and Contact layers using DSA," *SPIE Intl. Symp. Advanced Lithography Conference*, San Jose, CA, Feb. 26 - Mar. 2, 2017.

[C118] Taiki Kimura, Tetsuaki Matsunawa, Chikaaki Kodama, Shigeki Nojima and David Z. Pan, "SOCS-based post-layout optimization for multiple patterns with light interference prediction," *SPIE Intl. Symp. Advanced Lithography Conference*, San Jose, CA, Feb. 26 - Mar. 2, 2017.

[C119] Jiaojiao Ou, Brian Cline, Greg Yeric and David Z. Pan. "Efficient DSA and DP Hybrid Lithography Conflict Detection and Guiding Template Assignment", *SPIE Intl. Symp. Advanced Lithography Conference*, San Jose, CA, Feb. 26 - Mar. 2, 2017.

[C120] Wuxi Li, Shounak Dhah, and David Z. Pan, "UTPlaceF: A Routability-Driven FPGA Placer with Physical and Congestion Aware Packing," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Austin, TX, Nov. 7-10, 2016 (**Invited Paper; 1st Place Winner of ISPD'16 Contest**)

[C121] Yibo Lin, Bei Yu, Xiaoqing Xu, Jhih-Rong Gao, Natarajan Viswanathan, Wen-Hao Liu, Zhuo Li, Charles J. Alpert and David Z. Pan, "MrDP: Multiple-row Detailed Placement of Heterogeneous-sized Cells for Advanced Nodes," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Austin, TX, Nov. 7-10, 2016

[C122] Meng Li, Kaveh Shamsi, Travis Meade, Zheng Zhao, Bei Yu, Yier Jin and David Z. Pan, "Provably Secure Camouflaging Strategy for IC Protection," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Austin, TX, Nov. 7-10, 2016

[C123] Shounak Dhar, Saurabh Adya, Love Singhal, Mahesh A. Iyer and David Z. Pan, "Detailed Placement for Modern FPGAs using 2D Dynamic Programming," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Austin, TX, Nov. 7-10, 2016

[C124] Yudong Tao, Changhao Yan, Yibo Lin, Shengguo Wang, David Z. Pan, and Xuan Zeng, "A Novel Unified Dummy Fill Insertion Framework with SQP-Based Optimization Method," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Austin, TX, Nov. 7-10, 2016

[C125] Travis Meade, Shaojie Zhang, Zheng Zhao, David Z. Pan, and Yier Jin, "Gate-Level Netlist Reverse Engineering Tool Set for Functionality Recovery and Malicious Logic Detection," *International Symposium for Testing and Failure Analysis (ISTFA)*, Fort Worth, Texas, USA, Nov. 6-10, 2016

[C126] Yibo Lin, Bei Yu, and David Z. Pan, "Detailed Placement in Advanced Technology Nodes: A Survey," *IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, Hangzhou, China, October 25-28, 2016. **(Invited Paper)**

[C127] Derong Liu, Bei Yu, Salim Chowdhury, and David Z. Pan, "Incremental Layer Assignment for Critical Path Timing," *ACM/IEEE Design Automation Conference (DAC)*, Austin, TX, June 5-9, 2016

[C128] Meng Li, Jin Miao, Kai Zhong, and David Z. Pan, "Practical Public PUF Enabled by Solving Max-Flow Problem on Chip," *ACM/IEEE Design Automation Conference (DAC)*, Austin, TX, June 5-9, 2016

[C129] Jiaojiao Ou, Bei Yu and David Z. Pan, "Concurrent Guiding Template Assignment and Redundant Via Insertion for DSA-MP Hybrid Lithography," *Proceedings ACM International Symposium on Physical Design (ISPD)*, Santa Rosa, CA, April 3-6, 2016

[C130] Xiaoqing Xu, Tetsuaki Matsunawa, Shigeki Nojima, Chikaaki Kodama, Toshiya Kotani and David Pan, "A Machine Learning Based Framework for Sub-Resolution Assist Feature Generation," *Proceedings ACM International Symposium on Physical Design (ISPD)*, Santa Rosa, CA, April 3-6, 2016

[C131] Yibo Lin, Xiaoqing Xu, Bei Yu, Ross Baldick, and David Z. Pan, "Triple/Quadruple Patterning Layout Decomposition via Novel Linear Programming and Iterative Rounding," *Proc. SPIE 9781, Design-Process-Technology Co-optimization for Manufacturability X*, San Jose, CA, Feb. 21-25, 2016 (**Franco Cerrina Memorial Best Student Paper Award)**

[C132] Xiaoqing Xu, Brian Cline, Greg Yeric, and David Z. Pan, "Standard Cell Pin Access and Physical Design in Advanced Lithography," *SPIE Advanced Lithography Conference*, San Jose, CA, Feb. 21-25, 2016 **(Invited Paper)**

[C133] Taiki Kimura, Tetsuaki Matsunawa, Shigeki Nojima, and David Z. Pan, "Hybrid Hotspot Detection using Regression Model and SOCS Kernels," *Proc. SPIE 9781, Design-Process-Technology Co-optimization for Manufacturability X*, San Jose, CA, Feb. 21-25, 2016

[C134] Tetsuaki Matsunawa, Bei Yu, and David Z. Pan, "Laplacian Eigenmaps and Bayesian Clustering Based Layout Pattern Sampling and Its Applications to Hotspot Detection and OPC," *IEEE/ACM Asian and South Pacific Design Automation Conference (ASP-DAC)*, Macau, Jan. 25-28, 2016.

[C135] Yibo Lin, Bei Yu, Yi Zou, Zhuo Li, Charles J. Alpert, and David Z. Pan, "Stitch Aware Detailed Placement for Multiple E-Beam Lithography," *IEEE/ACM Asian and South Pacific Design Automation Conference (ASP-DAC)*, Macau, Jan. 25-28, 2016.

[C136] Pengpeng Ren, Xiaoqing Xu, Peng Hao, Junyao Wang, Runsheng Wang, Ming Li, Jianping Wang, Weihai Bu, Jingang Wu, Walsum Wong, Shaofeng Yu, Hanming Wu, Shiuh-Wuu Lee, David Z. Pan, and Ru Huang, "Adding the Missing Time-Dependent Layout Dependency into Device-Circuit-Layout Co-Optimization -- New Findings on the Layout Dependent Aging Effects," *IEEE International Electron Devices Meeting (IEDM)*, Washington DC, Dec. 7-9, 2015

[C137] Andrew B. Kahng, Mulong Luo, Gi-Joon Nam, Siddhartha Nath, David Z. Pan, and Gabriel Robins, "Toward Metrics of Design Automation Research Impact," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Austin, TX, November 2-6, 2015. (**Invited Paper**)

[C138] Bei Yu, Derong Liu, Salim Chowdhury, and David Z. Pan, "TILA: Timing-Driven Incremental Layer Assignment," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Austin, TX, November 2-6, 2015.

[C139] Yibo Lin, Bei Yu, Biying Xu, and David Z. Pan, "Triple Patterning Aware Detailed Placement Toward Zero Cross-Row Middle-of-Line Conflict," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Austin, TX, November 2-6, 2015.

[C140] Chen-Hsuan Lin, Subhendu Roy, Chun-Yao Wang, David Z. Pan, and Deming Chen, "CSL: Coordinated and Scalable Logic Synthesis Techniques for Effective NBTI Reduction," *IEEE International Conference on Computer Design (ICCD)*, Oct. 18-21, 2015

[C141] David Z. Pan, Lars Liebmann, Bei Yu, Xiaoqing Xu, Yibo Lin, "Pushing Multiple Patterning in Sub-10nm: Are We Ready?" *ACM/IEEE Design Automation Conference (DAC),* San Francisco, CA, June 7-11, 2015 (**Invited Paper**)

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[C304] J. Cong, David Z. Pan, Lei He, Cheng-Kok Koh, and Kei-Yong Khoo, "Interconnect Design for Deep Submicron ICs," *Proceedings ACM/IEEE International Conference on Computer-Aided Design (ICCAD)*, pp. 478-485, San Jose, CA, November 9-13, 1997. Available at: http://dx.doi.org/10.1109/ICCAD.1997.643579

C. Other Refereed Conference/Workshop Papers/Posters (without proceeding) (Partial List)

[W1] Xiaoqing Xu, Bei Yu, Jhih-Rong Gao, Che-Lun Hsu, and David Z. Pan, "PARR: Pin Access Planning and Regular Routing for Self-Aligned Double Patterning," *SRC Techcon Conference*, Austin, TX, September 2015. **(Best Paper in Session Award)**

[W2] Tetsuaki Matsunawa, Jhih-Rong Gao, Bei Yu, and David Z. Pan, "Machine Learning Based High-Accurate Hotspot Detection with Boosting Algorithm," *ACM/IEEE Design Automation Conference (DAC)* Designer Track, 2014 (**Best Designer Track Finalist**)

[W3] Jiwoo Pak, Mohit Pathak, Sung Kyu Lim, David Z. Pan, "Modeling and Prediction of Chip-Level Electromigration for TSV-Based 3D ICs," *SRC Techcon Conference*, Austin, TX, September 2012. **(Best Paper in Session Award)**

[W4] Yen-Hung Lin, Bei Yu, David Z. Pan, and Yih-Lang Li, "TRIAD: Triple Patterning Lithography Aware Detailed Router," *the 6th IEEE International Workshop on Design for Manufacturability and Yield (DFM&Y)*, June 4, 2012

[W5] Bei Yu, Yen-Hung Lin, Gerard Luk-Pat, Kevin Lucas, and David Z. Pan, "A High-Performance Triple Patterning Layout Decomposer," *the 6th IEEE International Workshop on Design for Manufacturability and Yield (DFM&Y)*, June 4, 2012

[W6] T. Luo, D. Newmark, and David Z. Pan, "Effective Power Optimization combining Placement, Sizing and Multi-Vt techniques," *SRC Techcon Conference*, Austin, TX, September 2007. **(Best Paper in Session Award)**

[W7] P. Yu and David Z. Pan, "TIP-OPC: A New Topological Invariant Paradigm for Pixel Based Optical Proximity Correction," *Proceedings SRC Techcon Conference*, Austin, TX, September 2007.

[W8] A. Ramalingam, A. K. Singh, S. R. Nassif, G.-J. Nam, M. Orshansky, and David Z. Pan, "Accurate Waveform Modeling using Singular Value Decomposition with Applications to Timing Analysis," *ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU)*, Austin, TX, February 2007.

[W9] J. Cong, David Z. Pan, and P.V. Srinivas, "Improved Crosstalk Modeling for Noise Constrained Interconnect Optimization," *ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU)*, Austin, TX, December 2000.

[W10] C.-C. Chang, J. Cong, David Z. Pan, and X. Yuan, "Interconnect-Driven Floorplanning with Fast Global Wiring Planning and Optimization," *Proceedings SRC Techcon Conference*, Phoenix, AZ, September 2000.

[W11] J. Cong, David Z. Pan, and P.V. Srinivas, "Improved Crosstalk Modeling with Applications to Noise Constrained Interconnect Optimization," *Proceedings SRC Techcon Conference*, Phoenix, AZ, September 2000.

[W12] J. Cong and David Z. Pan, "Interconnect Delay and Area Estimation for Multiple-Pin Nets," *Proceedings ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU)*, Monterey, CA, March 1999.

[W13] J. Cong and David Z. Pan, "Interconnect Delay Estimation Models for Logic and High Level Synthesis," *SRC Techcon Conference*, Las Vegas, NV, September 1998. **(Best Paper in Session Award)**

[W14] J. Cong and David Z. Pan, "Interconnect Performance Estimation Models for Synthesis and Design Planning," *ACM/IEEE International Workshop on Logic Synthesis*, Lake Tahoe, CA, June 1998.

D. Books/Book Chapters and Dissertation

[B1] Wei Ye, Mohamed Baker Alawieh, Che-Lun Hsu, Yibo Lin, and David Z. Pan, "Dealing with Aging and Yield in Scaled Technologies," *Dependable Embedded Systems*, edited by Jörg Henkel and Nikil Dutt, Springer, 2021

[B2] Meng Li and David Z. Pan, ***A Synergistic Framework for Hardware IP Privacy and Integrity Protection*****,** Springer, 2020

[B3] Bei Yu and David Z. Pan*,* ***Design for Manufacturability with Advanced Lithography*****,** Springer, 2016

[B4] Yibo Lin and David Z. Pan, "Machine Learning in Physical Verification, Mask Synthesis, and Physical Design," *Machine Learning in VLSI Computer-Aided Design*, edited by Abe Elfedel, Duane Boning and Xin Li, Springer, 2018

[B5] Bei Yu and David Z. Pan, "Layout Decomposition for Triple Patterning," in *Encyclopedia of Algorithms*, edited by M.-Y. Kao, Springer, 2015

[B6] Minsik Cho and David Z. Pan, "Global Routing," in *Encyclopedia of Algorithms*, edited by M.-Y. Kao, Springer, 2015

[B7] M. Cho, J. Mitra, and David Z. Pan, "Manufacturability Aware Routing" in *The Handbook of Algorithms for VLSI Physical Design Automation* (edited by Charles J. Alpert, Dinesh P. Mehta, and Sachin S. Sapatnekar), CRC Press, 2009. (Invited book chapter)

[B8] David Z. Pan, B. Halpin, and H. Ren, "Timing-Driven Placement" in *The Handbook of Algorithms for VLSI Physical Design Automation* (edited by Charles J. Alpert, Dinesh P. Mehta, and Sachin S. Sapatnekar), CRC Press, 2009. (Invited book chapter)

[B9] T. Luo and David Z. Pan, "DPlace: Anchor Cell based Quadratic Placement with Linear Objective" in *Modern Circuit Placement: Best Practices and Results* (edited by Jason Cong and Gi-Joon Nam), Springer, 2007. (Invited book chapter)

[B10] David Z. Pan and M. Stan, "Physical Design and Interaction with Technology" in *CAD Algorithms, Methods and Tools for Low-Power Circuits and Systems* (edited by Enrico Macii), IEEE Technology Survey, 2006

[B11] Zhigang Pan, *Interconnect Synthesis and Planning for High-Performance IC Designs*, PhD Dissertation, University of California at Los Angeles, 2000

PATENTS:

[P1] David Zhigang Pan and Peng Yu, "Method and System for Performing Optical Proximity Correction with Process Variations Considerations." US Patent, No. 7,711,504, Granted May 4, 2010.

[P2] Minsik Cho and David Zhigang Pan, "Method and System for Performing Global Routing on an Integrated Circuit Design." US Patent, No. 7,661,085, Granted on February 9, 2010.

[P3] Anthony Correale, Jr., David S. Kung, Douglas T. Lamb, David Zhigang Pan, Ruchir Puri, and David Wallach, "Multiple Voltage Integrated Circuit and Design Method Therefore." US Patent, No. 7,480,883, Granted on January 20, 2009.

[P4] Anthony Correale, Jr., Rajeev Joshi, David S. Kung, David Zhigang Pan, and Ruchir Puri, "Single Supply Level Converter." US Patent, No. 7,119,578, Granted on October 10, 2006.

[P5] Anthony Correale, Jr., David S. Kung, Douglas T. Lamb, David Zhigang Pan, Ruchir Puri, and David Wallach, "Multiple Voltage Integrated Circuit and Design Method Therefor." US Patent, No. 7,111,266, Granted on September 19, 2006.

[P6] Anthony Correale, Jr., David S. Kung, David Zhigang Pan, and Ruchir Puri, "Method and Program Product of Level Converter Optimization." U.S. Patent, No. 7,089,510, Granted on August 8, 2006.

[P7] Jingsheng Cong, David Zhigang Pan, and P.V. Srinivas, "Method and Apparatus for Calculation of Crosstalk Noise in Integrated Circuits." U.S. Patent, No. 7,013,253, Granted March 2006.

[P8] Jingsheng Cong and David Zhigang Pan, "Wire Width Planning and Performance Optimization for VLSI Interconnects." U.S. Patent No. 6,408,427, Granted June 2002.

ORAL PRESENTATIONS:

Invited Tutorials/Talks, Special Sessions, Panels at Conferences/Workshops

[O1] Panelist, "How to Prepare and Apply for Fellow", The 5th ACSIC Symposium on Frontiers in Computing (SOFC), Aug. 6, 2022

[O2] "Agile and Intelligent Design Automation for Future Circuits and Systems," IEEE International Workshop for Future Intelligent Circuits and Systems (IW-FICAS), Singapore, 3-5 August 2022 (in person and online)

[O3] **Keynote**, "Agile and Intelligent Design Automation for Digital/Analog/Mixed-Signal ICs", 15th IEEE Dallas Circuits and Systems Conference (DCAS), June 17-19, 2022 (online)

[O4] **Keynote**, "Agile and Intelligent Design Automation for Digital/Analog/Mixed-Signal ICs", China Semiconductor Technology International Conference (CSTIC), June 14-17, 2022 (online)

[O5] **Keynote,** "Machine Learning for Agile, Intelligent and Open-Source EDA", IEEE International Workshop on Electronic Design Automation and Machine Learning (EDAML), Jun 3, 2022 (Co-located with 36th IEEE International Parallel and Distributed Processing Symposium (IPDPS) May 30 – June 3, 2022, Ecole Normale Supérieure de Lyon Lyon, France) (virtual)

[O6] **Tutorial** (1.5-hour) "Toward Agile, Intelligent and Open-Source Design Automation of Digital, Analog and Mixed-Signal ICs," IEEE Custom Integrated Circuits Conference (CICC) Education Session, April 24, 2022

[O7] Panelist on "Automatic Circuit Generation and AI-Driven Design: Future of Circuit Design?" IEEE CICC, April 25, 2022
[O8] "Integrating Human and Machine Intelligence into Analog Routing", ISPD 2022 Routing Panel, March 30, 2022
[O9] "Reinforcement Learning for Electronic Design Automation: Case Studies and Perspectives," ASP-DAC 2022 Special Session, Jan. 19, 2022
[O10] "Automating Analog Constraint Extraction: From Heuristics to Learning," ASP-DAC 2022 Special Session, Jan. 17, 2022
[O11] "Reinforcement Learning for Electronic Design Automation", The 6th Future Chips Forum, Dec. 17, 2021 (virtual)
[O12] **Keynote,** "Light in AI: Toward Efficient Neurocomputing with Optical Neural Networks," ICCAD Workshop on Hardware and Algorithms for Learning On-a-chip (HALO), Nov. 4, 2021 (virtual)
[O13] **Keynote,** "Closing the Virtuous Cycle of AI for IC and IC for AI," *IEEE 14th International Conference on ASIC*, October 26-29, 2021 (virtual)
[O14] **Keynote,** "Toward Agile and Open Design Automation of Digital / Analog / Mixed-Signal ICs," *The 6th International Conference on Integrated Circuits and Microsystems (ICICM)*, October 22-24, 2021 (Virtual)
[O15] **Keynote,** "Toward Agile and Open Electronic Design Automation," *The 6th China DA Forum*, July 11, 2021 (Virtual)
[O16] **IEEE CEDA Distinguished Lecturer Program** – 2021 Virtual Webinar Series, "Closing the Virtuous Cycle of AI for IC and IC for AI", June 24, 2021, https://www.youtube.com/watch?v=xKMj2TFbq3A
[O17] "Machine Learning for Agile IC Design and Manufacturing," *2021 Symposium on VLSI Circuits* – Workshop 1 – AI/Machine Learning for Circuit Design and Optimization, June 13, 2021 (**my talk is among the most watched videos at the 2021 VLSI Symposium**)
[O18] **Keynote,** "Toward Agile and Open Electronic Design Automation," *CCF Agile Design and Open EDA Forum*, May 14, 2021
[O19] "Light for AI: Hardware-Software Codesign in Optical Neural Networks," *Optical/Photonic Interconnects for Computing Systems (OPTICS) Workshop*, April 15, 2021
[O20] **Keynote**, "Toward Agile and Open Electronic Design Automation," 2021 International Workshop on Electronic Design Automation, March 27, 2021
[O21] **Plenary**, "MAGICAL: An Open-Source Automated Analog IC Layout System Leveraging Human and Machine Intelligence," The 5th Future Chips Forum, Dec. 18, 2020 (Beijing, Virtual)
[O22] Panelist, "EDA Tools and Methodologies Panel," NSF Workshop on Micro/Nano Circuits and Systems Design, Dec. 14, 2020
[O23] Panelist, "ML for CAD – Where is the Treasure Hiding?" *the 2nd ACM/IEEE Workshop on Machine Learning for CAD (MLCAD)*, Nov. 20, 2020
[O24] "Re-examining VLSI Manufacturing and Yield through the Lens of Deep Learning," *ICCAD 2020 Special Session 1D.1*, Nov. 2, 2020
[O25] "AI for IC and IC for AI: Closed-Loop Perspectives and Recent Results," ICCAD Workshop -- ACCAD, Nov. 6, 2020 (through Zoom)
[O26] **Keynote,** "AI for IC and IC for AI: Closed-Loop Perspectives and Recent Results," 2020 IEEE ICICM-International Conference on Integrated Circuits and Microsystems, Oct. 24, 2020 (online)
[O27] **Keynote,** "AI for IC and IC for AI: Closed-Loop Perspectives and Recent Results," CCF Integrated Circuit Design and Automation Conference, Aug. 11, 2020 (online)
[O28] **Keynote,** "AI for IC and IC for AI: A Closed-Loop Perspective," The 20th CASPA Summer Symposium, July 25, 2020 (onine)
[O29] "AI-Enabled Agile IC Physical Design and Manufacturing," ACM SIGDA / IEEE CEDA The First Design Automation WebiNar (DAWN) on Machine Learning for EDA, May 7, 2020 https://www.youtube.com/watch?v=hXWgwXJbxS0
[O30] "AI and Intelligent IC/Accelerator Design: A Synergistic Approach," Future Chip Forum, Beijing, Dec. 16, 2019
[O31] "Artificial Intelligence & Integrated Circuit: A Synergistic Approach," S. T. Yau Science Forum (丘成桐科学论坛), Beijing, Dec. 15, 2019

[O32] "MAGICAL: Toward Fully Automated Analog IC Layout Leveraging Human and Machine Intelligence," ICCAD 2019 Special Session, Denver Area, Nov. 6, 2019
[O33] **"**AI-Enabled Agile IC Design and Manufacturing," IEEE Electronic Design Process Symposium (EDPS), Milpitas, CA, Oct. 3-4, 2019
[O34] "Deep Learning for Agile Physical Design and Manufacturing," 1st ACM/IEEE Workshop on Machine Learning for CAD (MLCAD), September 3-4, 2019, Canmore (Banff Area), Canada
[O35] "Machine Learning and Its Applications in IC Physical Design," ACM/SIGDA Seasonal School on Physical Design, Beijing, China, July 28, 2019
[O36] "Deep Learning for Agile Physical Design and Manufacturing," 1st ACM/IEEE Workshop on Machine Learning for CAD (MLCAD), September 3-4, 2019, Canmore, Canada
[O37] Panelist in "How to Build an Impactful Research Group?" ACM/IEEE Design Automation Conference Early Career Workshop, June 2, 2019
[O38] Panelist in "The Future of Interconnect Planning and Prediction (IPP)—Models, Methods, Applications and Topologies," SLIP'19, June 2, 2019
[O39] "Hardware-Software Co-design of Optical Neural Networks," The 5th International Workshop on Optical/Photonic Interconnects for Computing Systems (OPTICS), Co-located with DATE 2019, Florence, Italy, March 29, 2019
[O40] "MAGICAL: Machine Generated Analog IC Layout," Emerging Technologies in EDA Workshop, Hsinchu, Taiwan, March 21, 2019
[O41] "Provably Secure Camouflaging Strategy for IC Protection," *The First Workshop on **Top Picks** in Hardware and Embedded Security*, San Diego, Nov. 8, 2018
[O42] "Analog Layout Constraint Extraction and Exploration with Application to Layout Retargeting," *International Workshop on Design Automation for Analog and Mixed-Signal Circuit*, San Diego, Nov. 8, 2018
[O43] "Machine Learning for Yield Learning and Optimization," *IEEE International Test Conference (ITC)*, Oct. 31, 2018
[O44] **Keynote** "AI and Intelligent IC Design/Manufacturing," *IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, Chengdu, China, Oct. 27, 2018
[O45] "Optical Computing on Photonic Integrated Circuits," OPTICS Workshop at MICRO 51, Fukuoka, Japan, Oct. 21, 2018
[O46] **Keynote** "AI and Intelligent IC Design/Manufacturing," IEEE International Test Conference in Asia (ITC-Asia), Harbin, China, Aug. 2018
[O47] "BDD-Based Logic Synthesis for Energy-Efficient Photonic Integrated Circuits," JST CREST International Workshop on Optics for Computing, Tokyo, 7/18/2018
[O48] "Machine Learning for Lithography Modeling, Mask Synthesis and Physical Design," DAC Workshop on Machine Learning in Design Automation (MALENDA), San Francisco, CA, June 24, 2018
[O49] Panelist in "Research Collaboration Panel," *The Second ACSIC Symposium on Frontiers in Computing* (**第二届北美计算机华人学者年会/暨计算技术前沿研讨会)**, Dallas, TX, June 1, 2018
[O50] **Plenary Talk** "AI and Intelligent IC Design/Manufacturing," Duke Kunshan University AI Forum, Kunshan, China, May 22, 2018
[O51] "Optical Computing on Silicon-on-Insulator Based Photonic Integrated Circuits," *North American Workshop on Silicon Photonics for High Performance Computing*, Fort Collins, Colorado, May 17-18, 2018
[O52] "Machine Learning for IC Design & Technology Co-Optimization in Extreme Scaling," *VLSI-DAT/TSA* Joint Special Session, Hsinchu, Taiwan, April 17, 2018
[O53] **Keynote** "Machine Learning for Lithography and Physical Design", China S*emiconductor Technology International Conference (CSTIC) - Symposium II and Symposium XI-DTCO Joint session*, China, March 2018
[O54] **Tutorial** "IC Design and Technology Co-Optimizations (DTCO) in Extreme Scaling," *ACM/IEEE Asian and South Pacific Design Automation Conference (ASP-DAC),* Jan. 22-25, 2018
[O55] "Smarter Design for Manufacturing, Reliability & Security in the IoT Era," 第二届硅谷北京国际物联网高峰论坛, Santa Clara, CA, Jan. 13, 2018
[O56] "AI Applications and Security Panel", *Future Chips Forum,* Tsinghua University, Dec. 18-19, 2017

[O57] "Nanometer IC Design and Technology Co-Optimizations – Challenges and Practices," The 1st West Lake Semiconductor Process Technology Workshop, Hangzhou, Oct. 30, 2017
[O58] "Machine Learning for Mask/Wafer Hotspot Detection and Mask Synthesis," *SPIE Photomask Technology + Extreme Ultraviolet Lithography Conference*, Monterey, CA, Sept. 2017
[O59] Panelist, "Early/Mid-Career Academic Panel," *DAC'17 Early Career Workshop*, Austin, TX, June 18, 2017.
[O60] "Toward Unidirectional Routing Closure in Extreme Scaling," *IEEE/ACM System Level Interconnect Prediction (SLIP) Workshop*, Austin, TX, June 17, 2017.
[O61] Panelist in "Academic/Industry Collaboration Panel," *The First ACSIC Symposium on Frontiers in Computing* (**第一届北美计算机华人学者年会/暨计算技术前沿研讨会**), Chicago, June 9, 2017
[O62] Panel Moderator, "Panel on IoT and Security", *TexasWISE Workshop*, Dallas, TX, April 21, 2017
[O63] "Toward Synergistic Academic/Industry Collaboration for Future EDA Research and Talent Pipeline," *CDNLive*, April 12, 2017, Santa Clara, CA
[O64] **Vision Talk**, "Bridging Nanometer IC Design and Technology Gaps for Manufacturability, Reliability, and Security", *The First Future Chip Summit*, Beijing, Dec. 13-14, 2016
[O65] Panel Moderator, "The Dawn of EDA R&D in China," *The First Future Chip Summit*, Beijing, Dec. 13-14, 2016
[O66] Panelist, "Industry and Academic Collaboration in EDA," *The First Future Chip Summit*, Beijing, Dec. 13-14, 2016
[O67] **SIGDA Live,** "How to Survive & Thrive in Academia: My Personal Take on Promotion & Tenure," Dec. 8, 2016, https://www.youtube.com/watch?v=NhM4714z1N4
[O68] **Keynote,** "Smarter Manufacturing and Design for Reliable/Secure IC and IoT," *China-US Smart Manufacturing Summit*, Washington DC, Nov. 1, 2016
[O69] Panelist, "Smart Manufacturing and Wireless Factory," *China-US Smart Manufacturing Summit*, Washington DC, Nov. 1, 2016
[O70] **Plenary Talk,** "Bridging Design & Technology Gaps for Future Chips," *16th IEEE International Conference on Ubiquitous Wireless Broadband*, Nanjing, Oct. 17, 2016
[O71] "Bridging Design and Technology Gap for Manufacturability, Reliability, and Security," *The First ShanghaiTech Workshop on Emerging Devices, Circuits and Systems (SWEDCS)*, June 30, 2016
[O72] **Panelist, "**TSVs ARE SO 2010 - THE REALITY OF 3D-IC," *ACM/IEEE Design Automation Conference*, Austin, TX, June 6-9, 2016
[O73] **Visionary Talk,** "DFX: on Deep Nanoscale Design for Manufacturability, Reliability, and Security," *IEEE International Workshop on Design Automation for Cyber-Physical Systems* (co-located with DAC), Austin, TX, June 5, 2016 http://www.ieee-cps.org/CPSDA-2016/program.html
[O74] **Keynote**, "Nanolithography and Design Technology Co-optimization in Extreme Scaling," China S*emiconductor Technology International Conference (CSTIC) - Symposium II and Symposium XI-DTCO Joint session*, Shanghai, March 13-14, 2016
[O75] Invited talk, "Standard Cell Pin Access and Physical Design in Advanced Lithography," *SPIE Advanced Lithography Conference*, San Jose, CA, Feb. 21-25, 2016
[O76] Panelist -- "From EDA to DA: Can we evolve beyond our E-roots?" ICCAD, Austin, Nov. 2-6, 2015
[O77] "Toward Cross-Layer Technology, EDA and System Power/Performance/Reliability Optimizations," Samsung Low Power Forum, Austin, TX, Oct. 8, 2015
[O78] "Cross-Layer Reliability in Extreme Scaling & Beyond," Reliability and Design (ZuE) Workshop, Siegen, Germany, September 21-23, 2015
[O79] "Pushing Multiple Patterning in Sub-10nm: Are We Ready?" *ACM/IEEE Design Automation Conference (DAC)*, San Francisco, CA, June 11, 2015. (**Special Session)**
[O80] "Technology, EDA and System Power/Performance/Reliability Optimization with a Cross-Layer Case Study," DAC 2015 SEAK Workshop, June 7, 2015
[O81] "Design for Manufacturing in Extreme Scaling and Beyond," *edaWorkshop*, Dresden, May 21, 2015
[O82] "Design for Manufacturability & Reliability in Extreme Scaling and Beyond," CSTIC, March 16, 2015
[O83] "Machine Learning and Pattern Matching in Physical Design," *IEEE/ACM Asian and South Pacific Design Automation Conference (ASP-DAC)*, Japan, Jan. 19-22, 2015 (**Special Session**)

[O84] IEEE CEDA All Japan Joint Chapter, "My Take on ASP-DAC on its 20th Anniversary," ASP-DAC 2015
[O85] **Keynote**, "CAD Tool and Methodology for Reliable 3D-IC Integration," TwinLab 3DSC Workshop, 11/11/2014
[O86] Invited talk, "Evolving Challenges and Techniques for Nanometer SoC Clock Network Synthesis," IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), Oct. 28-31, 2014, Guilin, China
[O87] Invited talk, "Manufacturable and Reliable Interconnect in Extreme Scaling," IEEE SLIP Workshop, June 1, 2014
[O88] Invited talk, "Design for Manufacturability and Reliability in Extreme Scaling and Beyond," *China Semiconductor Technology International Conference (CSTIC)*, Shanghai, March 16, 2014
[O89] **Opening Plenary**, "Mathematical Methods in Nanometer Design for Manufacturability," *International Workshop on Mathematical Methods in Chip Design Automation*, Fuzhou, March 14-16, 2014
[O90] Invited talk, "Bridging the Gap from Mask to Physical Design for Multiple Patterning Lithography," *SPIE International Symposium on Advanced Lithography - Design-Process-Technology Co-optimization for Manufacturability VIII*, San Jose, CA, Feb. 23-27, 2014
[O91] 2013 BIMS 北京微电子国际研讨会特邀讲员，"未来集成电路的智能设计与制造,"Beijing, China, Oct. 31, 2013
[O92] Invited talk, "Lithography Hotspot Detection and Mitigation in Nanometer VLSI," 2013 *IEEE ASICON*, Shenzhen, China, Oct. 29, 2013
[O93] SRC e-Workshop, "CAD Tool and Methodology for Reliable 3D-IC Integration" (jointly presented with Prof. Sung Kyu Lim at Georgia Tech), July 18, 2013
[O94] Invited talk, "VLSI Design and Nanolithography in 14nm and Beyond", 2013 *CMOS Emerging Technologies Research Symposium*, Whistler, Canada, July 17, 2013
[O95] Invited talk, "Cross-Layer Robustness in Extreme Scaling", The first NSF/SRC/DFG International Workshop on Cross-Layer Resilience, Austin, July 11 and 12, 2013
[O96] **Keynote**, "Cross-Layer Resilient Design for Extreme Scaling and Beyond", ACM/IEEE International Workshop on Logic and Synthesis (IWLS), Austin, TX, June 7, 2013
[O97] Roundtable Panelist in "Who Will Pay for Low Power – Chip Manufacturers, Tool Providers or Consumers?" hosted by Ed Sperling of Low Power Engineering, held during DAC, June 5, Austin, TX, 2013
[O98] Invited talk, "Design for Manufacturability and Reliability in TSV-based 3D-IC", ACM/IEEE DFM&Y Workshop, Austin, TX, June 3, 2013
[O99] "CAD in Extreme Scaling and Emerging Technologies", NSF/CCC/SIGDA Workshop, Austin, TX, June 2, 2013
[O100] "Modeling and Layout Optimization for Robust 3D-IC Integration with TSVs", the 1st IEEE International High Speed Interconnect Symposium (From Silicon to Systems), Dallas, April 30, 2013
[O101] "Dealing with IC Manufacturability in Extreme Scaling", ICCAD Embedded Tutorial, Nov. 2012
[O102] "Lithography Aware Physical Design," 2012 Lithography Workshop, Williamsburg, VA, June 2012
[O103] "Reliability Modeling and Design Issues for TSV-based 3D Integration," *4th Design for 3D Silicon Integration Workshop (D43D)*, Lausanne, Switzerland, June 25, 2012
[O104] Panelist on "Future Interconnect Technologies," SLIP 2012, co-located with DAC'12 in San Francisco, CA, June 2012
[O105] Special Session talk on "VLSI CAD for Emerging Nanolithography," VLSI-DAT, Hsinchu, Taiwan, April 2012
[O106] "Design for Manufacturability with Emerging Nanolithography," ASP-DAC 2012 Tutorial, Sydney, Australia, January 2012
[O107] Special Session talk on "Physical CAD for Robust Designs," ASP-DAC 2012, Sydney, Australia, January 2012
[O108] Special Session talk on "Design for Manufacturability & Reliability for TSV-based 3D-ICs," ASP-DAC 2012, Sydney, Australia, January 2012

[O109] "Design for Manufacturability and Reliability in Extreme CMOS Scaling and 3D-IC," Global COE Workshop on "Ambient SoC Education and Research for New Leaders," co-located with ASP-DAC 2012, Sydney, Australia, January 30, 2012 (Invited talk)
[O110] "Robust and Energy Efficient Design-Process Integration in Sub-22nm CMOS and 3D-IC," Pacific Rim Outlook Forum for IC Technology (PROFIT) Workshop, Inner Mongolia, China, August 2011
[O111] "'More Moore' and 'More than Moore', beyond 22nm: Challenges and Opportunities," The 11th Emerging Information & Technology Conference, Chicago, IL, July 28-29, 2011
[O112] "Reliability and Variability in TSV-based 3D-IC Designs," The 3rd Design for 3D Silicon Integration Workshop (D43D), Grenoble, France, June 2011
[O113] **Keynote Speaker,** "Nanolithography and Design-Technology Co-optimization Beyond 22nm," TAU Workshop, Santa Barbara, CA, March 2011
[O114] "Double Patterning Lithography Layout Decomposition and Routing," IEEE Lithography Workshop, Kauai, HI, November 2010
[O115] Invited Tutorial on "Design for Resilience in Beyond-22nm CMOS & 3D-IC," IEEE Dallas CAS Workshop, Dallas, TX, October 18, 2010
[O116] "Design for Manufacturability and Reliability in TSV-based 3D-IC," ASP-DAC TPC Workshop, Seoul, Korea, September 11, 2010
[O117] "Voltage and Frequency Island Optimizations for Many-Core/ Networks-on-Chip Designs," the first International Conference on Green Circuits & Systems (ICGCS), Shanghai, China, June, 2010
[O118] "CAD for Double Patterning Lithography," IEEE ICICDT, Grenoble, France, June 3, 2010
[O119] "Layout Optimizations for Double Patterning Lithograph," IEEE ASICON, Changsha, China, October 23, 2009
[O120] "Nanometer & Emerging Design Automation Research at UTDA," ASP-DAC TPC Workshop, Tokyo, Japan, September 7, 2009
[O121] "More Moore's Law through Computational Scaling - and EDA's Role," invited talk at the **NSF Workshop on the Future of Electronic Design Automation**, Washington DC, July 8, 2009
[O122] Organizer/Presenter, "Nanolithography and CAD Challenges for 32nm/22nm (and Beyond?)," half-day tutorial at ICCAD, San Jose, CA, November 12, 2008
[O123] Invited Talk, "EDA Education and Research at UT Austin," the first EDA Education & Research Workshop, held at ICCAD 2008, San Jose, CA, November 9, 2008
[O124] Invited Talk, "Lithography Friendly Routing: From Construct-by-Correction to Correct-by-Construction," ICSICT, Beijing, China, October 21, 2008
[O125] Invited Tutorial, "Synergistic Modeling and Optimization for Nanometer IC Design/Manufacturing Integration," SBCCI, Gramado, Brazil, September 1, 2008
[O126] Invited Talk, "Lithography Friendly Routing: From Construct-by-Correction to Correct-by-Construction," SBCCI, Gramado, Brazil, September 2, 2008
[O127] **Keynote Speaker**, "Design for Manufacturability – Practices and Perspectives for 45/32nm and Beyond," 2008 Freescale Physical Design and Design for Manufacturing (DFM) Conference, Austin, TX, May 13-16, 2008
[O128] Special Session Organizer/Presenter, "Tackling Manufacturability/Variability for 32nm and Below," *ASP-DAC*, Seoul, Korea, January 2008
[O129] Tutorial Organizer/Presenter, "DFM Routing and Clock Distribution," *ICCAD*, San Jose, CA, November 2007
[O130] "Design and CAD for Manufacturability." *ACM/SIGDA Design Automation Summer School*, San Diego, CA, June 2-3, 2007 (held with IEEE/ACM Design Automation Conference)
[O131] "Nanometer Physical Design for Manufacturability and Variability," 3-hour Tutorial at the *VLSI-DAT* Conference, Taiwan, April 27, 2007
[O132] "DFM: Impact of Manufacturing Reality on Design," Half-day Tutorial at ICCAD, San Jose, CA, November 9, 2006
[O133] Panelist – "What Will Make or Break DFM&Y," *The First IEEE Design for Manufacturability & Yield Workshop (DFM&Y)*, San Jose, CA, October 26, 2006
[O134] Tutorial on "Lithography and Design for Variability," *Austin Conference on Integrated Systems and Circuits* (with Dr. Chris Mack), Austin, TX, May 18, 2006
[O135] Panelist – "Design for Manufacturability (DFM)," *SPIE Microlithography, Design and Process Integration Conference*, San Jose, CA, March 4, 2005

[O136] "Lithography and CMP Aware Routing," *IEEE Design for Manufacturability & Yield Workshop (DFM&Y)*, San Jose, CA, October 26, 2006
[O137] "Design for Manufacturability with Deep Sub-wavelength Lithography," *International Center on Design for Nanotechnology (IC-DFN) Workshop*, Hangzhou, China, August 16, 2006
[O138] "Manufacturability Aware Physical Layout Optimizations," *International Conference on IC Design and Technology (ICICDT)*, Austin, TX, May 2005
[O139] "Lithography Aware Physical Design," *IEEE International Conference on ASIC (ASICON)*, Shanghai, China, October 27, 2005
[O140] "Nanometer Physical Design Research at UT Austin," *International Center for System-on-Chip (IC-SOC) Workshop*, Changsha, China, August 6, 2004
[O141] "Diffusion-Based Placement Migration," *IEEE Electronic Design Process Symposium (EDPS)*, Monterey, CA, April 7, 2005
[O142] "Optimizing Power in Performance Constraints," *IEEE International Conference on Integrated Circuit Design and Technology (ICICDT)*, Austin, TX, May 19, 2004

Invited Talks at Various Institutions and Companies

[O143] "Light-AI Interaction: The Convergence of Photonic Deep Learning and Cross-Layer Design Automation," ACCESS and CEDA Joint Seminar, Hong Kong, July 29, 2022
[O144] "Closing the Virtuous Cycle of AI for IC and IC for AI," **Samsung Forum**, April 12, 2022
[O145] "Closing the Virtuous Cycle of AI for IC and IC for AI," ECE Department **Distinguished Lecture**, Stevens Institute, March 9, 2022
[O146] "Closing the Virtuous Cycle of AI for IC and IC for AI," **NSF National AI Research Institute** – TILOS Seminar Series, Dec. 15, 2021
[O147] "Toward Agile, Intelligent, and Open-Source Design Automation of Digital/Analog/Mixed-Signal ICs," **ShanghaiTech SIST Distinguished Lecture**, Nov. 29, 2021
[O148] "Toward Agile, Intelligent, and Open-Source Design Automation of Digital/Analog/Mixed-Signal ICs," Qualcomm Education Seminar, Nov. 17, 2021
[O149] "Closing the Virtuous Cycle of AI for IC and IC for AI," ML + X Seminar, UT Austin, Nov. 12, 2021
[O150] "Toward Agile and Intelligent Design & Manufacturing Closure," Intel Labs Seminar, Oct. 27, 2021
[O151] "FPGA Placement: Recent Progress and Road Ahead," Featured Seminar at the Intel/VMware Crossroads 3D-FPGA Academic Research Center, Oct. 22, 2021
[O152] "Toward Agile and Open-Source Design Automation of Digital/Analog/Mixed-Signal ICs," USC Ming Hsieh Institute Seminar Series (Integrated Systems), Oct. 8, 2021
[O153] "Toward Agile and Open Electronic Design Automation," National Microelectronics Security Training (MEST) Center Webinar, Univ. of Florida, Oct. 6, 2021
[O154] "MAGICAL: An Open-Source Automated Analog IC Layout System Leveraging Human and Machine Intelligence," Synopsys (online talk), July 22, 2021
[O155] "MAGICAL: An Open-Source Automated Analog IC Layout System Leveraging Human and Machine Intelligence," CHIPS Alliance, June 1, 2021
[O156] "VTR3D: Scalable and Flexible Physical CAD for Architecture Exploration," (co-presented with Prof. Vaughn Betz, Univ. of Toronto), Intel PSG CTO Tech Talk, May 4, 2021
[O157] "AI for IC and IC for AI: Closed-Loop Perspectives and Recent Results," Google, Feb. 12 2021
[O158] "AI for IC and IC for AI: Closed-Loop Perspectives and Recent Results," Rutgers ECE Colloquium, Dec. 2, 2020
[O159] "MAGICAL: Toward Fully Automated Analog IC Layout Leveraging Human and Machine Intelligence," Nvidia Research, Oct. 28, 2020
[O160] "AI for IC and IC for AI: Closed-Loop Perspectives and Recent Results," IEEE CEDA Hong Kong Chapter, Sept. 30, 2020
[O161] "AI for IC and IC for AI: Closed-Loop Perspectives and Recent Results," IEEE CASS Rio Grande do Sul Chapter, Sept. 11, 2020
[O162] "Machine Learning for Digital/Analog IC and FPGA Physical Design," Xilinx, July 31, 2020
[O163] "AI-Enabled Agile IC Physical Design and Manufacturing," AMD, July 17, 2020 (online seminar)
[O164] "Machine Learning for Physical Design & Manufacturing," Synopsys DG Tech Talk, July 8, 2020 (online)
[O165] "DREAMPlace and Beyond," Google, June 26, 2020 (online)

[O166] "AI for IC and IC for AI: A Closed-Loop Perspective," Austin Big Data Forum, June 25, 2020 (online)
[O167] "MAGICAL: Toward Fully Automated Analog IC Layout Leveraging Human and Machine Intelligence," TSMC (online seminar), May 26, 2020
[O168] "Machine Learning for Modern IC Design and Manufacturing," Apple Lonestar Design Center, Feb. 14 2020
[O169] "AI and Intelligent IC/Accelerator Design: A Synergistic Approach," Peking University, CECA Seminar, Beijing, Dec. 18, 2019
[O170] "AI and Intelligent IC/Accelerator Design: A Synergistic Approach," George Washington University, ECE Seminar, Washington DC, Dec. 4, 2019
[O171] "AI and Intelligent IC/Accelerator Design: A Synergistic Approach," Northeastern University, **ECE Distinguished Speaker Series**, Boston, Nov. 13, 2019
[O172] "AI and Intelligent IC/Accelerator Design: A Synergistic Approach," Facebook, Boston, Nov. 1, 2019
[O173] "AI-Enabled Agile IC Design and Manufacturing," MIT Lincoln Lab, Boston, Oct. 30, 2019
[O174] **"**AI-Enabled Agile IC Design and Manufacturing," Cadence AI Forum, San Jose, Oct. 15, 2019
[O175] "AI and Intelligent IC/Accelerator Design: A Synergistic Approach," University of Pennsylvania, ESE Colloquium, Oct. 1, 2019
[O176] "MAGICAL: Machine Generated Analog IC Layout," Silicon Labs, Austin, TX, June 12, 2019
[O177] "AI and Intelligent IC Design: A Synergistic Approach," MIT, Cambridge, MA, May 8, 2019
[O178] "AI and Intelligent IC Design/Manufacturing," TSMC and National Tsinghua University, Hsinchu, Taiwan, March 22, 2019
[O179] "AI and Intelligent IC Design/Manufacturing," Rice University, Houston, August 8, 2018
[O180] "Toward Machine Generated Analog IC Layout", Cirrus Logic Tech Talk, Austin, July 31, 2018
[O181] "AI and Intelligent IC Design/Manufacturing," China-Netherland Forum, Tsinghua University, China, July 11, 2018
[O182] "AI and Intelligent IC Design/Manufacturing," Peking University, China, July 10, 2018
[O183] "AI and Intelligent IC Design/Manufacturing," Shanghai Tech University, China, May 31, 2018
[O184] "AI and Intelligent IC Design/Manufacturing," John Hopcroft Center for Computer Science, Shanghai Jiaotong University, China, May 30, 2018
[O185] "AI and Intelligent IC Design/Manufacturing," Nanjing University, China, May 29, 2018
[O186] "Machine Learning for IC Design & Technology Co-Optimization in Extreme Scaling," TSMC, Silicon Valley, CA, May 4, 2018
[O187] "Intelligent Design and Manufacturing in the Era of Extreme Scaling and Internet of Everything," Peking University Shenzhen Graduate School, Shenzhen, China, March 14, 2018
[O188] "Design for X (DFx) in Extreme Scaling and Emerging Technologies," Peking University, Beijing, China, Dec. 22, 2017
[O189] "Design for X (DFx) in Extreme Scaling and Emerging Technologies," Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China, Dec. 22, 2017
[O190] "Design for X (DFx) in Extreme Scaling and Emerging Technologies," Tsinghua University, Beijing, China, Dec. 21, 2017
[O191] "Machine Learning for VLSI Design and Verification," Cirrus Logic, Austin, TX, Aug. 8, 2017
[O192] "Bridging IC Design & Technology Gaps for Manufacturability, Reliability, and Security," Xi'an Jiaotong University, May 27, 2017
[O193] "Machine Learning for Electronic Design Automation," Fudan University, Shanghai, May 22, 2017
[O194] "Machine Learning for Electronic Design Automation," University of Calgary, Canada, May 9, 2017
[O195] "Bridging IC Design & Technology Gaps for Manufacturability, Reliability, and Security in Extreme Scaling," UC Riverside, April 28, 2017
[O196] **Distinguished Lecture**, "Bridging Design & Technology Gaps for Future Chip Manufacturability, Reliability, and Security," Oklahoma State University, Stillwater, OK, April 20, 2017
[O197] **Distinguished Lecture**, "Bridging Design & Technology Gaps for Future Chip Manufacturability, Reliability, and Security," University of Kansas (KU), Lawrence, KS, April 14, 2017
[O198] **Distinguished Speaker Series**, "Bridging IC Design, Manufacturing and Security Gaps in Extreme Scaling," Cadence, San Jose, CA, April 12, 2017

[O199] "Bridging Design & Technology Gaps for Future Chip Manufacturability, Reliability, and Security," Boston University, March 30, 2017
[O200] "Bridging Design & Technology Gaps for Future IC and Systems," Fudan University, Shanghai, China, Dec. 28, 2016
[O201] "Bridging Design & Technology Gaps for Future Chips," Nantong University, China, Dec. 19, 2016
[O202] "Machine Learning in IC Design for Manufacturability & Security," Peking University, China, Dec. 15, 2016
[O203] "Machine Learning and Pattern Matching in VLSI CAD," Texas State University, San Marcos, Texas, Dec. 2, 2016
[O204] **Distinguished Lecture,** "Bridging IC Design and Technology Gaps for Manufacturability, Reliability, and Security," Michigan Technological University, Oct. 7, 2016
[O205] **Distinguished Lecture,** "Bridging IC Design and Technology Gaps for Manufacturability, Reliability, and Security," Old Dominion University, Sept. 19, 2016
[O206] "Robust Standard Cell Design and Layout Regularity Study with Nanolithography," SRC eWorkshop, August 10, 2016
[O207] "Bridging Design and Technology Gaps for Manufacturability, Reliability, and Security," Univ. of Utah, June 16, 2016
[O208] "Design & Process Technology Co-optimizations in Extreme Scaling," NVIDIA, Austin, June 13, 2016
[O209] "Challenges and Opportunities IC Design and Manufacturing in Deep Nano-Scaling and Beyond," Univ. of Science and Technology of China (USTC), Hefei, China, May 16, 2016
[O210] "Challenges and Opportunities IC Design and Manufacturing in Extreme Scaling and Beyond," Jiangnan University, Wuxi, China, May 10, 2016
[O211] "Challenges and Opportunities of IC Design & Manufacturing in Extreme Scaling and Beyond," Tsinghua University (Institute of Microelectronics), May 5, 2016
[O212] "IC Design and Technology Co-Optimization and Exploration in Extreme Scaling and Beyond," Institute of Microelectronics, Chinese Academy of Science, May 3, 2016
[O213] "Machine Learning and Pattern Matching in VLSI-CAD Applications," Intel Strategic CAD Lab Online Seminar, April 19, 2016
[O214] "Standard Cell Pin Access and Physical Design in Advanced Lithography," Intel Corporation, Hillsboro, Oregon, April 8, 2016
[O215] "Lithography Hotspot Detection and Mask Synthesis in Extreme Scaling," Intel Corporation, Hillsboro, Oregon, April 8, 2016
[O216] "Machine Learning and Pattern Matching in VLSI CAD," Chongqing University, China, March 21, 2016
[O217] "Toward Cross-Layer Power/Performance/Reliability Optimizations," School of Microelectronics, Southeast University, Nanjing, China, March 17, 2016
[O218] "Machine Learning and Pattern Matching in VLSI CAD," School of Computer Science, Southeast University, Nanjing, China, March 17, 2016
[O219] "Toward Cross-Layer Power/Performance/Reliability Optimizations," School of Microelectronics, Fudan University, Shanghai, China, March 15, 2016
[O220] "纳米集成电路设计与制造的挑战、机遇与展望 Nanometer IC Design and Manufacturing: Challenges, Opportunities, and Outlooks," University of Macao, Jan. 28, 2016
[O221] "纳米集成电路设计与制造的挑战、机遇与展望 Nanometer IC Design and Manufacturing: Challenges, Opportunities, and Outlooks," PKU-Shenzhen, China, Jan. 21, 2016
[O222] "Machine Learning and Pattern Matching in VLSI CAD," City University of Hong Kong, Hong Kong, China, Jan. 18, 2016
[O223] "Machine Learning and Pattern Matching in VLSI CAD," Chinese University of Hong Kong, Hong Kong, China, Jan. 18, 2016
[O224] "Pushing Multiple Patterning and Hybrid Lithography in Extreme Scaling," IMEC, Leuven, Belgium, Oct. 5, 2015
[O225] "Nanometer IC Design and Manufacturing Closure in Extreme Scaling and Beyond," TU Eindhoven, Netherlands, Oct. 2, 2015
[O226] "Design for Manufacturability & Reliability in Extreme Scaling and Beyond," KIT, Karlsruhe, Germany, September 28, 2015

[O227] "Multiple Patterning & Physical Design in Extreme Scaling," Univ. of Bonn, Germany, September 24, 2015
[O228] "Design for Manufacturability and Reliability in Nanometer IC and Beyond," SMIC, Shanghai, September 2, 2015
[O229] "Pushing Multiple Patterning and Hybrid Lithography in Extreme Scaling," TSMC, Hsinchu, September 1, 2015
[O230] "Pushing Multiple Patterning and Hybrid Lithography in Sub-10nm: What's the Limit?" National Tsinghua University, Taiwan, September 1, 2015
[O231] "Technology, EDA and System Power/Performance/Reliability Optimization with a Cross-Layer Case Study," Cirrus Logic, Austin, TX, August 4, 2015
[O232] "Design for Reliability in Nanometer IC and Beyond," Infineon, Munich, Germany, July 17, 2015
[O233] "Design for Manufacturability/Reliability Research at UTDA," TU Vienna, Austria, June 23, 2015
[O234] "Design for Manufacturability & Reliability in Extreme Scaling and Beyond," TUM, Munich, Germany, June 2, 2015
[O235] "Nanometer IC Design and Manufacturing: Challenges, Opportunities, and Outlooks," Huazhong University of Science and Technology, March 24, 2015
[O236] "CAD Tool and Methodology for Reliable 3D-IC and Optical Integration," Wuhan University, March 23, 2015
[O237] "Nanometer IC Design, Manufacturing and Applications: Challenges, Opportunities, and Outlooks," Nanjing University of Science and Technology, March 18, 2015
[O238] "Standard Cell Pin Access and Cell Layout Co-Optimizations," Fudan University, March 16, 2015
[O239] "Design for Manufacturability and Reliability in Extreme Scaling and Beyond," CMU ECE Colloquium, Feb. 5, 2015
[O240] "Design for Reliability in Nanometer VLSI," Hisilicon, Jan. 16, 2016
[O241] "Cross-Layer Optimizations for Nanometer VLSI in Extreme Scaling and Beyond," Peking University, Jan. 15, 2015
[O242] "Nanometer IC Design for Manufacturability and Reliability in Extreme Scaling and Beyond," Tsinghua University, EE Dept., Jan. 14, 2015
[O243] "Machine Learning and Pattern Matching in VLSI Design and Verification," HK PolyU, Jan. 8, 2015
[O244] "Cross-Layer Design for Manufacturability and Reliability in Extreme Scaling and Beyond," Chinese University of Hong Kong, Jan. 8, 2015
[O245] "Mask Synthesis and Physical Design for Nanolithography," GlobalFoundries, Dec. 12, 2014
[O246] "Mask Synthesis and Physical Design for Nanolithography," ASML, Nov. 6, 2014
[O247] "Nanometer IC Design and Manufacturing: Challenges, Opportunities, and Outlooks," Nanjing University of Posts & Telecommunications, Oct. 27, 2014
[O248] 'Design Techniques for Monolithic 3D Integration," IBM, Webinar, Oct. 3, 2014
[O249] "Mask and Physical Design Optimizations for Multiple Patterning Lithography," Samsung Electronics Future Technology Seminar, Seoul, S. Korea, Aug. 22, 2014
[O250] "Nanometer IC Design Challenges & Opportunities in Extreme Scaling and Beyond," LG Electronics, Seoul, S. Korea, Aug. 22, 2014
[O251] "Nanometer IC Design and Manufacturing in Extreme Scaling and Beyond," Shanghai Jiaotong University, Shanghai, China, July 23, 2014
[O252] "Physical Design and Manufacturing Closure for 22nm/14nm IC and Beyond," Nanjing University of Posts & Telecommunications, July 10, 2014
[O253] Design for Manufacturability & Reliability in Extreme Scaling and Beyond, Southeast University, Nanjing, China, July 8, 2014
[O254] "Physical Design and Manufacturing Closure for 22nm/14nm IC and Beyond," Nanjing University of Science and Technology, July 8, 2014
[O255] "Reclaiming Over-the-IP-Block Routing Resources for Routability and Timing," IBM EDA Seminar, Austin, TX, June 10, 2014
[O256] "Design for Manufacturability and Reliability in Extreme Scaling and Beyond," Harvard University, May 5, 2014
[O257] "Design for Manufacturability and Reliability in Extreme Scaling and Beyond," MIT, May 2, 2014
[O258] "Physical Design and Manufacturing Closure for Nanometer VLSI," Cirrus Logic, Austin, TX, April 17, 2014

[O259] "New Trends in Physical Design for Nanoscale, 3D, and Optical Integration," Fudan University, China, Jan. 10, 2014
[O260] "Intelligent Design and Manufacturing of Future Integrated Circuits," Nanjing University of Science and Technology, China, Jan. 7, 2014
[O261] "Nanometer IC Design for Manufacturability and Reliability in Extreme Scaling and Beyond," Zhejiang University, China, Jan. 6, 2014
[O262] "Design and Manufacturing Closure for Nanometer VLSI," Broadcom, Sunnyvale, Dec. 12, 2013
[O263] "Nanometer IC Design for Manufacturability and Reliability in Extreme Scaling and Beyond," IEEE CEDA Central Texas Chapter, Nov. 12, 2013
[O264] "Nanometer IC Design for Manufacturability and Reliability in Extreme Scaling and Beyond," Institute of Microelectronics, Chinese Academy of Sciences, Beijing, China, Oct. 31, 2013
[O265] "Design for Manufacturability and Reliability in Extreme CMOS Scaling and Beyond," IEEE CAS Victoria Chapter, Univ. of Victoria, July 22, 2013
[O266] "Design for Manufacturability and Reliability in Extreme CMOS Scaling and Beyond," IEEE CAS Vancouver Chapter, UBC, July 15, 2013
[O267] "Cross-Layer Resilient Design for Extreme Scaling and Beyond," Qualcomm, San Diego, CA, July 8, 2013
[O268] "CAD for Nanolithography," School of Microelectronics, Fudan University, China, June 24, 2013
[O269] "Cross-Layer Resilient Design for Extreme Scaling and Beyond," Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China, June 20, 2013
[O270] "Physical Design and Manufacturability/Reliability in Extreme Scaling and Beyond," Huada Empyrean Software Co., Beijing, China, June 20, 2013
[O271] "Cross-Layer Resilient Design for Extreme Scaling and Beyond," Peking University, Beijing, China, June 18, 2013
[O272] "Cross-Layer Resilient Design for Extreme Scaling and Beyond," Fudan University, Shanghai, China, June 13, 2013
[O273] "Design Technologies for Extreme Scaling and Beyond," Texas Instruments, Dallas, Texas, April 29, 2013
[O274] "Design and Manufacturing Closure for Next-Generation Microprocessors," Oracle Labs Tea Talk, Redwood City, CA, April 24, 2013
[O275] "Design for Robustness in Extreme Scaling and 3D-IC," Princeton University – EE Department, March 13, 2013
[O276] "Design for Robustness in Extreme Scaling and 3D-IC," Columbia University - EE, New York, March 12, 2013
[O277] "Dealing with IC Manufacturability and Design Enablement in Extreme Scaling and Beyond," IBM Research Design Automation PIC Seminar, Yorktown Heights, March 11, 2013
[O278] "Dealing with IC Manufacturability in Extreme Scaling," Toshiba, Japan, Jan. 21, 2013
[O279] "Next Generation VLSI CAD for "More Moore" and "More than Moore," Globalfoundries, San Jose, CA, Nov. 8, 2012
[O280] "Design Technologies for "More Moore" and "More than Moore"," Oracle, Santa Clara, CA, Nov. 7, 2012
[O281] "Next Generation VLSI CAD for "More Moore" and "More than Moore," Mentor Graphics, San Jose, CA, Nov. 6, 2012
[O282] "The 'Moore', The Merrier!" Peking University, China, August 21, 2012
[O283] "The 'Moore', The Merrier!" National Taiwan University, Taipei, Taiwan, July 27, 2012
[O284] "Synergistic Design & Technology Co-Optimization for 'More Moore' and 'More than Moore'," National Tsing Hua University, Hsinchu, Taiwan, July 26, 2012
[O285] "Nanolithography and CAD Challenges beyond 14nm," Taiwan Semiconductor Manufacturing Company (TSMC), Hsinchu, Taiwan, July 25, 2012
[O286] "Nanolithography and CAD Challenges beyond 14nm," Yuan Ze University, Taoyuan, Taiwan, July 25, 2012
[O287] "Nanolithography and CAD Challenges beyond 14nm", EPFL EE Summer Research Institute, Lausanne, Switzerland, June 22, 2012
[O288] "Physical Design in Extreme Scaling/3D Integration and Datapath-Aware Placement," Tabula, Santa Clara, CA, June 7, 2012

[O289] "Challenges and Opportunities for Physical Design in 14nm and Beyond," Samsung Austin Research Center (SARC), Austin, TX, May 29, 2012
[O290] "Design for Manufacturability/Reliability in beyond-14nm/3D-IC Integration and Datapath-aware Placement," IBM Austin Research Lab, Austin, TX, May 11, 2012
[O291] "Nanolithography and CAD Challenges beyond 14nm," National Cheng Kung University, Tainan City, Taiwan, April 26, 2012
[O292] "Design for Manufacturability & Reliability in TSV-based 3D-IC," National Cheng Kung University, Tainan City, Taiwan, April 26, 2012
[O293] "High-Performance VLSI Placement with Automatic Datapath Extraction and Evaluation," National Tsing Hua University and National Chiao Tung University, Hsinchu, Taiwan, April 23, 2012
[O294] "Design for Manufacturability and Reliability in Extreme CMOS Scaling and 3D-IC Integration," Department of Electrical Engineering, University of Southern California, Los Angeles, CA, April 13, 2012
[O295] "Resilient Design in Extremely-Scaled CMOS and 3D-IC Integration," ARM Inc., Austin, TX, April 11, 2012
[O296] "Design for Manufacturability and Reliability in Beyond-14nm Lithography and 3D-IC Integration," Fudan University, Shanghai, China, Jan. 10 2012
[O297] 'More Moore' and 'More than Moore' in Sub-20nm CMOS and 3D-IC," Peking University, Beijing, China, December 30, 2011
[O298] "'More Moore' and 'More than Moore' in Sub-20nm CMOS and 3D-IC," Tsinghua University, Beijing, China, December 29, 2011
[O299] "Resilient Design in Nanoscale CMOS and 3D-IC," Globalfoundries, Sunnyvale, CA, November 11, 2011
[O300] "Resilient Design Closure in Nanoscale CMOS and 3D-IC," Oracle, Sunnyvale, CA, November 9, 2011
[O301] "Resilient Design Closure in Nanoscale CMOS and 3D-IC," ARM, San Jose, CA, November 8, 2011
[O302] "Resilient Design Closure in Nanometer CMOS and 3D-IC," Freescale, Austin, TX, October 19, 2011
[O303] "'More Moore' and 'More than Moore' in Nanometer CMOS and 3D-IC," Shangdong University, Shangdong, China, July 19, 2011
[O304] "'More Moore' and 'More than Moore' in sub-22nm CMOS and 3D-IC," Zhejiang University, Zhejiang, China, July 12, 2011
[O305] "Physical Design and DFM in Sub-22nm and 3D," Politecnico di Torino, Torino, Italy, July 1, 2011
[O306] "Design and Technology Integration in beyond-22nm CMOS and 3D-IC," IMEC, Leuven, Belgium, June 27, 2011
[O307] "'More Moore' and 'More than Moore' beyond 22nm: Challenges and Opportunities," Katholieke Universiteit Leuven, Leuven, Belgium, June 27, 2011
[O308] "Recent Results in Nanometer Physical CAD," AMD, Austin, TX, May 19, 2011
[O309] "Nanometer Physical Design and Technology Co-optimization: A Synergistic Perspective," Samsung Austin Research Center, Austin, TX, May 5, 2011
[O310] "Design and Technology Co-optimization in beyond-22nm CMOS and 3D-IC Integration," Qualcomm, San Diego, CA, April 1, 2011
[O311] "Design and Technology Integration in beyond-22nm CMOS and 3D-IC," Globalfoundries, Sunnyvale, CA, February 4, 2011
[O312] "Design for Manufacturability and Reliability in beyond-22nm CMOS and 3D-IC Integration," Fujitsu Labs, Kawasaki, Japan, January 26, 2011
[O313] "Design for Resilience in Beyond-22nm CMOS and 3D-IC," UIUC ECE Colloquium, Urbana Champaign, IL, September 30, 2010
[O314] "Design for Resilience in Nanometer CMOS and 3D-IC," Samsung, Korea, September 9, 2010
[O315] "Design for Resilience in Nanometer CMOS and 3D-IC," Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, September 8, 2010
[O316] "Design for Resilience in Nanometer CMOS and 3D-IC," Design Automation PIC Seminar Series, IBM T. J. Watson Research Center, Yorktown Heights, NY, July 22, 2010
[O317] "Challenges and Opportunities in Nanometer VLSI and 3D-IC," Fuzhou University, Fuzhou, China, July 4, 2010

[O318] "Design for Manufacturability and Resilience in Nanometer CMOS and 3D-IC," TSMC, Hsinchu, Taiwan, April 28, 2010
[O319] "Design for Resilience in Nanometer CMOS and 3D-IC," at Springsoft, National Chiao Tung University, April 29; at Fudan University and Shanghai Jiaotong University, June 25; at Peking University and Tsinghua University, June 29; at Institute of Computing Technology, Chinese Academy of Sciences, June 30, 2010
[O320] "Design for Manufacturability and Robustness in Nanometer CMOS, 3D-IC, and Emerging Technologies," ITRI, Hsinchu, Taiwan, April 28, 2010
[O321] "Recent Results in Design for Manufacturing and Robustness," Freescale, Austin, TX, April 9, 2010
[O322] "Low Power Design and Challenges in Nanometer Multicore Era," IEEE CAS Melbourne and Victoria University, Melbourne, Australia, August 20, 2009
[O323] **IEEE Distinguished Lecture**, "Synergistic Modeling and Optimization for Nanometer IC Design/Manufacturing Integration," IEEE CAS Melbourne, Melbourne, Australia, August 20, 2009
[O324] **IEEE Distinguished Lecture**, "Synergistic Modeling and Optimization for Nanometer IC Design/Manufacturing Integration," IEEE CAS Sydney, Sydney, Australia, August 14, 2009
[O325] "Synergistic Modeling and Optimization for Nanometer IC Design/Manufacturing Integration," Institute of Microelectronics, Singapore, July 14, 2009
[O326] **IEEE Distinguished Lecture**, "Synergistic Modeling and Optimization for Nanometer IC Design/Manufacturing Integration," IEEE CAS Singapore Chapter, Singapore, July 13, 2009
[O327] "Unified Analysis, Characterization and Optimization of Systematic and Random Variations with Variational Litho-Modeling," SRC e-Workshop, Austin, TX, April 22, 2009
[O328] "On Clock Mesh Design," Sun Microsystems, Austin, TX, March 9, 2009
[O329] "On Graduate Research and Education in US," Zhejiang University, Hangzhou, China, January 12, 2009
[O330] "Synergistic Modeling and Optimization for Nanometer IC Design & Manufacturing Closure," Tsinghua University, Beijing, China, October 24, 2008
[O331] **IEEE Distinguished Lecture**, "Synergistic Modeling and Optimization for Nanometer IC Design/Manufacturing Integration," IEEE CAS Taiwan, Kaohsiung, Taiwan, September 10 and 11, 2008
[O332] "Nanometer Physical Design and DFM," SpringSoft, Hsinchu, Taiwan, September 9, 2008
[O333] "On Nanometer VLSI Physical Design and Manufacturing Closure: What, Why, and How?," UFRGS, Porto Alegre, Brazil, August 13, 2008
[O334] "Physical Design Issues in Microfluidic Biochips," Technical University of Dresden, Germany, July 4, 2008
[O335] **IEEE Distinguished Lecture**, "Synergistic Modeling and Optimization for Nanometer IC Design/Manufacturing Integration," IEEE Los Angeles Council, Los Angeles, CA, June 9, 2008
[O336] "New Faculty Seminar on NSF CAREER," FIC, Cockrell School of Engineering, UT Austin, Austin, TX, May 21, 2008
[O337] "Modeling and Optimization for Nanometer IC Design and Manufacturing Integration," AMD, Austin, TX, March 28, 2008
[O338] "Synergistic Modeling and Optimization for Nanometer Design for Manufacturing," Texas Instruments, Dallas, TX, February 15, 2008
[O339] "Synergistic Modeling and Optimization for Physical and Electrical DFM," UT Dallas, Dallas, TX, February 14, 2008
[O340] "Synergistic Modeling and Optimization for Physical and Electrical DFM," UC Santa Barbara, CA, February 8, 2008
[O341] "Synergistic Modeling and Optimization for Physical and Electrical DFM," Seoul National University LSI Workshop, Seoul, Korea, January 25, 2008
[O342] "Synergistic Modeling and Optimization for Physical and Electrical DFM," Samsung Electronics, Seoul, Korea, January 21, 2008
[O343] "Synergistic Modeling and Optimization for Physical and Electrical DFM," Stanford University, Stanford, CA, November 30, 2007
[O344] "Synergistic Modeling and Optimization for Physical and Electrical DFM," University of California at Berkeley, CA, November 30, 2007

[O345] "Synergistic Modeling and Optimization for Physical and Electrical DFM," Mentor Graphics, San Jose, CA, November 29, 2007
[O346] "Challenges and Opportunities for Nanometer VLSI Design and Manufacturability," Tongji University, Shanghai, China, August 23, 2007
[O347] "Synergistic Modeling and Optimization for Physical and Electrical DFM," Tsinghua University and Peking University, Beijing, China, August 22, 2007
[O348] "Challenges and Opportunities for Nanometer IC Design and Manufacturability," Shangdong University, Jinan, China, August 20, 2007
[O349] "Challenges and Opportunities for Nanometer IC Design and Manufacturability," Southeast University, Nanjing, China, August 10, 2007
[O350] "Recent Results and Physical and Electrical DFM," Qualcomm, San Diego, CA, July 11, 2007
[O351] "Synergistic Modeling and Optimization for Physical and Electrical DFM," **Cadence Distinguished Seminar Series**, San Jose, CA, July 11, 2007
[O352] "Recent Research Highlights at UTDA," Cadence Berkeley Lab, Berkeley, CA, July 11, 2007
[O353] "DFM and Physical CAD Research at UTDA," Taiwan Semiconductor Manufacturing Company (TSMC), Hsinchu, Taiwan, April 25, 2007
[O354] "Modeling & Optimization for Physical and Electrical DFM," National Tsing-hua University, Hsinchu, Taiwan, April 24, 2007
[O355] "Modeling & Optimization for Physical and Electrical DFM," National Taiwan University, Taipei, Taiwan, April 23, 2007
[O356] "Tackling Design for Manufacturability/Variability from Root Causes," Intel Corporation, Santa Clara, CA, February 28, 2007
[O357] "Recent Research on Physical CAD and DFM at UT Design Automation (UTDA) Lab," System LSI Design Workshop, Fukuoka, Japan, September 9, 2006
[O358] "Modeling and Optimization for Nanometer Physical Design and Manufacturability," Fudan University, Shanghai, China, August 24, 2006
[O359] "Physical Design and Manufacturability Closure for Nanometer VLSI/SOC," 6th Emerging Information Technology Conference (EITC), Dallas, TX, August 10, 2006
[O360] "Modeling and Optimization for Nanometer Physical Design and Manufacturability," IBM T. J. Watson Research Center, Yorktown Heights, NY, July 21, 2006
[O361] "The Real DFM - Physical Design for Manufacturability/Variability," Freescale Seminar, Austin, TX, July 13, 2006
[O362] "The True DFM - Physical Design For Manufacturability" (part two), IBM EDA Seminar Series, Fishkill, NY, May 2, 2006 (given through conference call & online)
[O363] "The True DFM - Physical Design For Manufacturability" (part one), IBM EDA Seminar Series, Fishkill, NY, April 25, 2006 (given through conference call & online)
[O364] "New Ideas in Nanometer Physical CAD & DFM," Intel, Santa Clara, CA, February 24, 2006
[O365] "A New LP Based Incremental Timing Driven Placement for High Performance Designs," IBM Austin CAS Conference, Austin, TX, February 17, 2006
[O366] "Nanometer Physical Design for Manufacturability," STARC, Kawasaki, Japan, January 25, 2006
[O367] "Physical Design for Manufacturability," Fujitsu Corporation, Kawasaki, Japan, January 23, 2006
[O368] "New Ideas in Nanometer Physical CAD & Manufacturability," Tsinghua University, Beijing, China, October 28, 2005
[O369] "Challenges and Opportunities in Nanometer VLSI Physical Design & Manufacturing Closure," Peking University, Beijing, China, October 28, 2005
[O370] "Physical Design for Manufacturability," Zhejiang University, Hanzhou, China, October 24, 2005
[O371] "New Ideas in Nanometer Physical Synthesis & DFM," IBM T. J. Watson Research Center, Yorktown Heights, NY, August 8, 2005
[O372] "Litho-Aware Routing & Diffusion-Based Placement," Cadence, San Jose, CA, July 28, 2005
[O373] "New Ideas in Nanometer Physical CAD," Sun Microsystems, Austin, TX, July 21, 2005
[O374] "New Ideas in Placement & Variation-Tolerant Clock Designs," Intel Strategic CAD Lab, Hillsboro, OR, July 8, 2005
[O375] "New Ideas in Placement & DFM," Synopsys Advanced Technology Group, Hillsboro, OR, July 7, 2005
[O376] "True Manufacturability Aware Physical Design," Freescale, Austin, TX, May 27, 2005

[O377] "Physical CAD Research on Nanometer Design and Manufacturing Closure," Texas Instruments, Dallas, TX, March 18, 2005
[O378] "Diffusion-Based Placement Migration," IBM Austin CAS Conference, Austin, TX, February 25, 2005
[O379] "Nanometer Physical Synthesis for Multi-Objective Design Closure and Manufacturability," Magma Design Automation, Santa Clara, CA, November 5, 2004
[O380] "Nanometer Physical Synthesis for Multi-Objective Design Closure and Manufacturability," Cadence Berkeley Lab, Berkeley, CA, November 5, 2004
[O381] "Nanometer Physical Synthesis for VLSI Design Closure," University of Maryland at College Park, MD, October 22, 2004
[O382] "Recent Results of Physical Synthesis with Nanometer Effects," IBM Austin Research Lab Seminar, Austin, TX, October 8, 2004
[O383] "Holistic Approaches for Multi-Objective Design Closure with Nanometer Effects," AMD, Austin, TX, October 5, 2004
[O384] "Nanometer Physical Synthesis for Timing, Signal Integrity, and Low Power Optimizations," Synopsys Advanced Technology Group, Hillsboro, OR, October 1, 2004
[O385] "Nanometer Physical Synthesis for Timing, Signal Integrity, and Low Power Optimizations," Intel Strategic CAD Lab, Hillsboro, OR, September 30, 2004
[O386] "Integrated Placement with Nanometer Timing and Signal Integrity Closure," Electrical Engineering Department, Texas A&M University, College Station, TX, September 28, 2004
[O387] "Recent Results of Physical Synthesis with Nanometer Effects," Intel, Austin, TX, September 9, 2004
[O388] "Nanometer VLSI Designs: Challenges, Opportunities and Optimizations," Shanghai Jiaotong University, Shanghai, China, August 17, 2004
[O389] "Holistic Approaches of Next-Generation Physical Design to Cope with Nanometer Effects," Fudan University, Shanghai, China, August 17, 2004
[O390] "Physical Synthesis in Nanometer VLSI Designs," Tsinghua University, China, August 12, 2004
[O391] "Physical Design with Integrity." Agere Systems, Allentown, PA, July 27, 2004
[O392] "Recent Results of Physical Synthesis with Nanometer Effects," IBM T. J. Watson Research Center, Design Automation PIC Seminar, Yorktown Heights, NY, July 26, 2004
[O393] "Nanometer Physical Synthesis for Performance, Power and Predictability," AMD, Austin, TX, March 4, 2004
[O394] "Physical Synthesis for Nanometer Designs," IEEE CAS/SSC Joint Chapter Meeting, Austin, TX, February 26, 2004
[O395] "Physical Synthesis for Nanometer Designs," Motorola SPS (Freescale), Austin, TX, February 19, 2004
[O396] "Interconnect-Centric Design Closure for High Performance and Low Power VLSI," ECE Department, Yale University, New Haven, CT, May 12, 2003
[O397] "Interconnect-Centric Design Closure for High Performance and Low Power VLSI," ECE Department, University of Wisconsin at Madison, Madison, WI, May 1, 2003
[O398] "Physical Design Closure for High Performance and Low Power VLSI," ECE Seminar, Purdue University, West Lafayette, IN, April 17, 2003
[O399] "Physical Design Closure for High Performance and Low Power VLSI," EE-Systems, University of Southern California, Los Angeles, CA, April 14, 2003
[O400] "Physical Design Closure for High Performance and Low Power VLSI," Department of Electrical and Computer Engineering, UT Austin, Austin, TX, April 7, 2003
[O401] "Physical Design Closure for High Performance and Low Power VLSI," Division of Engineering, Brown University, Providence, RI, April 2, 2003
[O402] "Challenges and Opportunities for Nanometer Design Closure," VLSI Seminar Series, University of Michigan, Ann Arbor, MI, October 28, 2002
[O403] "Interconnect Prediction and Planning for Design Closure," EE Seminar, Fudan University, Shanghai, China, November 26, 2001

MEDIA COVERAGE:

- AI's design speedups, with and without machine learning
  https://www.techdesignforums.com/blog/2021/06/14/vlsi-symposia-ai-eda-workshop/
- MIT Technology Review - DeepTech 深科技, April 12, 2020, "谷歌又一野心浮现：用 AI"反哺"芯片设计," https://mp.weixin.qq.com/s/B-71EH6aOqWl9zZI8SgA0Q
- EE Times, April 6, 2017, "ISPD Predicts Chip Futures," http://www.eetimes.com/document.asp?doc_id=1331563 (covered my UT group as the "ISPD'17 Clock-aware FPGA Placement Contest" 1st Place Winner)
- Semiconductor Engineering, September 7, 2016, "Joint R&D Has Its Ups and Downs," http://semiengineering.com/joint-rd-has-its-ups-and-downs/
- EE Times, April 8, 2016, "Machine Learning Routes Chips," http://www.eetimes.com/document.asp?doc_id=1329391 (covered my students and I as the ISPD'16 FPGA Placement Contest 1st Place Winners)
- EE Times, April 9, 2014,"ISPD-14 Focuses on FinFETs, Security, Supply Chain," http://www.eetimes.com/document.asp?doc_id=1321843 (covered our ISPD'14 Best Paper)
- SRC Press Release, "2013 Technical Excellence Award Presented to David Pan from UT/Austin" http://www.src.org/award/tech-excellence/2013/
- Stanford and UT Austin Professors to Be Honored for Advancing Chip Research at Annual SRC TECHCON Event
  - http://www.src.org/newsroom/press-release/2013/499/
  - Business Wire Article: http://www.businesswire.com/news/home/20130905005318/en/Stanford-UT-Austin-Professors-Honored-Advancing-Chip
  - + other media coverage (Yahoo Finance, Market Watch, etc.)
- June 2013, DAC Roundtable "Experts at the Table: Who Pays for Low Power?" hosted by System-Level Design Editor-in-Chief Ed Sperling http://lp-hp.com/blog/2013/07/11/experts-at-the-table-who-pays-for-low-power/
- Synopsys Conversation Central, "CAD Research and Education in Extreme Scaling and Beyond," hosted by Karen Bartleson, June 2013 (Synopsys web site, YouTube, Podcast)
  - Show Notes page: http://bit.ly/13jZHFb
  - YouTube Video: http://youtu.be/06mz2HLkWpk
  - iTunes Page: http://bit.ly/QPtlHr
- EE Times, April 13, 2011: "ISPD spots 3-D, maskless-lithography trends," http://www.eetimes.com/electronics-news/4215124/ISPD-reveals-3-D--maskless-lithography-trends-
- March 20, 2010: Interview by Prof. Patrick Madden, ACM/SIGDA Chair, on the ASP-DAC 2010 Best Paper on *"A Multi-Objective Min-Cut Based Layout Decomposition Framework for Double Patterning Lithography,"* http://www.youtube.com/watch?v=N76t3YNQoPc
- May 19, 2009: "The IEEE CANDE Committee Elects Officers", Reuters, Yahoo Finance, etc. http://www.reuters.com/article/pressRelease/idUS155240+19-May-2009+BW20090519
- EE Times, April 21, 2008, "Lab-on-chip design automation takes cue from EDA," http://www.eetimes.com/electronics-news/4076826/Lab-on-chip-design-automation-takes-cue-from-EDA
- EE Times, April 17, 2008, "Future of chip design revealed at ISPD," http://www.eetimes.com/showArticle.jhtml?articleID=207400313
- EE Times (China/Taiwan), April 30, 2007, "VLSI-DAT 盛况空前，业界专家布道前瞻新技术" (in Chinese), http://www.eetchina.com/ART_8800462927_480401_NT_0f306e22.HTM
- EE Times, April 2, 2007, "Rethinking statistical timing analysis," http://eetimes.com/news/design/showArticle.jhtml?articleID=198700121
- EE Times, March 22, 2007, "IC routing contest boosts CAD research," http://eetimes.com/news/design/showArticle.jhtml?articleID=198500084
- EE Times, June 19, 2006, "Chip designers feel the heat - Accurate thermal analysis cools the effects of sub-90-nm design," http://www.eetimes.com/news/design/showArticle.jhtml?articleID=189400781

- EE Times, April 17, 2006, "Paths to better timing analysis," http://www.eet.com/news/latest/showArticle.jhtml?articleID=185302541
- EE Times, October 28, 2005, "EDA startup forms technical advisory board," http://www.eetimes.com/news/design/showArticle.jhtml?articleID=172901367
- EE Times, July 11, 2005, "Shift to 65 nm has its costs," http://www.eetimes.com/news/latest/showArticle.jhtml?articleID=165701002

CURRENT PHD/MS STUDENTS, POST-DOCs AND VISITING SCHOLARS:

- **Students admitted to Ph.D. candidacy**:
  - Jiaqi Gu (co-supervised by Prof. Ray Chen)
  - Zixuan Jiang
  - Mingjie Liu
- **Post M.S. students preparing to take Ph.D. qualifying exam**:
  - Ahmet F. Budak (co-supervised by Prof. Nan Sun)
  - Hyunsu Chae
  - Hao Chen
  - Chenghao Feng (co-supervised with Prof. Ray Chen)
  - Chen-Hao Hsu
  - Rachel Selina Rajarathnam
  - Vivek Varier (co-supervised by Prof. Nan Sun)
  - Yang Yang
- **M.S. in progress:**
  - Xuyang Jin
  - Hanqing Zhu
  - Souradip Poddar
- **Post-docs:**
  - Shuhan Zhang
  - Keren Zhu
- **Visiting Scholars:**

PH.D. SUPERVISIONS COMPLETED:

Name	PhD Dissertation	Semester	First job after PhD and current position (with selected awards)
1. Haoxing Ren	Incremental Placement for Modern VLSI Design Closure	Spring 2006	Research Staff Member, IBM T. J. Watson Research; now Senior Manager, Design Automation Research and Principal Research Scientist, Nvidia
2. Gang Xu	Layout Optimization Algorithms for VLSI Design and Manufacturing	Summer 2007	R&D Engineer, Mentor Graphics; now Software Engineer, Google
3. Tao Luo	Nanometer VLSI Placement and Optimization for Multi-Objective Design Closure	Fall 2007	Sr. MTS, Magma; now Engineering Leader/Manager at Uber (2007 SRC Techcon Best Paper in Session)
4. Anand Ramalingam	Analysis Techniques for Nanometer Digital Integrated Circuits	Fall 2007	Member of Consulting Staff, Magma DA; now Staff Engineer at Synopsys

5. Minsik Cho	Physical Synthesis for Nanometer VLSI and Emerging Technologies	Summer 2008	Research Staff Member, IBM T. J. Watson Research Center; now Siri R&D, AI/ML at Apple (ISPD'13 Best Paper Award; IBM Research 2010 Pat Goldberg Memorial Best Paper Award; 2008 SRC Inventor Recognition Award; 2007 IBM PhD Scholarship; ISPD'07 Global Routing Contest Awards)
6. Anand Rajaram	Synthesis of Variation Tolerant Clock Distribution Networks	Fall 2008	Member of Consulting Staff, Magma DA; now Sr. Staff R&D Engineer, Synopsys
7. Peng Yu	Fast and Accurate Lithography Simulation and Optical Proximity Correction for Nanometer Design for Manufacturing	Spring 2009	Post-Doc Researcher, Baylor College of Medicine; then Assistant Professor, Texas A&M University (2008-09 UT Graduate School Continuing Fellowship; 2008 SPIE Education Scholarship; 2008 SRC Inventor Recognition Award)
8. Xiaokang (Sean) Shi	Modeling and Optimization to Connect Layout with Silicon for Nanoscale IC	Fall 2009	Sr. Component Engineer, Intel Corporation; now Engineer at Bloomberg (2009 IBM PhD Scholarship)
9. Kun Yuan	VLSI Physical Design Automation for Double Patterning and Emerging Lithography	Fall 2010	Sr. Member of Technical Staff, Cadence; now Sr. Software Engineer at Airbnb (ISPD'11 Best Paper Award; IBM Research 2010 Pat Goldberg Memorial Best Paper Award)
10. Ashutosh Chakraborty	Mechanical Stress and Circuit Aging Aware VLSI CAD	Fall 2010	Senior Hardware Engineer, Oracle; now Software Engineer at Google (2009 DATE Best Paper/IP Award; 2009-10 UT Graduate School Continuing Fellowship; 2009 eASIC Placement Contest 1st Prize)
11. Jae-Seok Yang	Nanometer VLSI Design-Manufacturing Interface for Large Scale Integration	Spring 2011	Senior Engineer, Samsung; now Principal Engineer, Samsung (2010 ASP-DAC Best Paper Award; IBM Research 2010 Pat Goldberg Memorial Best Paper Award)
12. Wooyoung Jang	Architecture and Physical Design for Advanced Networks-on-Chip	Spring 2011	Senior Engineer, Samsung; now Associate Professor, Dankook University, S. Korea (2006-2011 Samsung Scholarship)
13. Yongchan (James) Ban	Lithography Variability Driven Cell Characterization and Layout Optimization for Manufacturability	Spring 2011	Senior Engineer, Intel; now MTS, Synopsys (2010 SPIE Education Scholarship)
14. Duo Ding	CAD for Nanolithography and Nanophotonics	Summer 2011	Senior Hardware Engineer, Oracle; now Senior Staff Software Engineer at Samsung Austin Research Center (2013 ACM Outstanding PhD Dissertation Award in EDA; 2012 ASP-DAC Best Paper Award; 2009 ICICDT Best Student Paper Award)

15. Samuel Ward	Physical Design Automation of Structured High-Performance Integrated Circuits	Fall 2013	Data Scientist/Fraud Manager, Apple (IBM Master Inventor in 2011)
16. Jhih-Rong (Jerrica) Gao	Lithography Aware Physical Design and Layout Optimization for Manufacturability	Spring 2014	Senior Member of Technical Staff, Cadence; now Senior Principal eFPGA Software Developer at Flex Logix Tech. (ICCAD'13 Best Paper Award, ICCAD'12 and ICCAD'13 CAD Contest Awards, SPIE 2013 Scholarship)
17. Jiwoo Pak	Electromigration Modeling and Layout Optimization for Advanced VLSI	Spring 2014	Senior Member of Technical Staff, Cadence; now Sr. Principal Software Engineer at Cadence (SRC Techcon 2012 Best in Session Award, 2013 Grace Hopper Celebration Scholarship)
18. Bei Yu	Design for Manufacturing with Advanced Lithography	Summer 2014	Post-doc Researcher, UT Austin; now Associate Professor at Chinese University of Hong Kong (EDAA Outstanding Dissertation Award, ICCAD'13 Best Paper Award, ASP-DAC'12 Best Paper Award, 2013 Chinese Government Award for Outstanding Self-Financed Students Abroad, 2013/2012 ICCAD CAD Contest 2nd Place Awards, Silver Medal in ACM Student Research Contest, SPIE Optics and Photonics Education Scholarship, 2012 IBM Ph.D. Scholarship)
19. Yilin Zhang	Interconnect Optimizations for Nanometer VLSI Design	Summer 2014	Software Scientist, Rocket Fuel Inc., now Software Engineer, Google
20. Subhendu Roy	Logic and Clock Network Optimization in Nanometer VLSI Circuits	Summer 2015	Principal Software Engineer, Cadence (ISPD 2014 Best Paper Award; TexasWISE 2014 Best Student Poster Award)
21. Xiaoqing Xu	Standard Cell Optimization and Physical Design in Advanced Technology Nodes	Spring 2017	Senior Research Engineer, ARM Research; now Senior Hardware Engineer at Google X (Gold Medal at ACM/SIGDA Student Research Competition 2016; Best in Session Award at SRC Techcon 2015)
22. Yibo Lin	Bridging Design and Manufacturing Gap through Machine Learning and Machine-Generated Layout	Spring 2018	Post-doc Researcher, UT Austin; now Assistant Professor at Peking University (DAC'19 Best Paper Award; Integration – the VLSI Journal Best Paper Award 2018; UT Graduate Continuing Fellowship 2017; SPIE'16 Franco Cerrina Memorial Best Student Paper Award)
23. Jiaojiao Ou	Design for Manufacturing with Directed Self-Assembly Lithography	Spring 2018	Senior R&D Engineer, Synopsys (2017 SPIE BACUS Scholarship)
24. Derong Liu	Layer Assignment and Routing Optimization for Advanced Technologies	Summer 2018	Lead Software Engineer, Cadence (ISPD'18 Best Paper Award)

25. Meng Li	A Synergistic Framework for Hardware IP Privacy and Integrity Protection	Summer 2018	Research Scientist, Facebook On-Device AI (First Place of ACM Student Research Competition Grand Finals 2018; EDAA Outstanding Dissertation Award 2018; GLSVLSI'18 Best Paper Award; Gold Medal of ACM/SIGDA Student Research Competition 2017; HOST'17 Best Paper Award; (UT-ECE 2018-2019 Jacome Dissertation Prize)
26. Biying Xu	Layout Automation for Analog and Mixed-Signal Integrated Circuits	Spring 2019	Lead Software Engineer, Cadence (Cadence Women in Technology Scholarship 2018)
27. Joydeep Mitra	Mask Synthesis Techniques for Directed Self-Assembly	Spring 2019	Senior Software Architect, Cadence; now Principal Machine Learning Engineer/Senior Director at Visa
28. Wuxi Li	Placement Algorithms for Large-Scale Heterogeneous FPGAs	Summer 2019	Staff Software Engineer, Xilinx (DAC'19 Best Paper Award, ISPD 2017 and 2016 Contests First Place)
29. Shounak Dhar	Modern FPGA Placement Techniques with Hardware Acceleration	Summer 2019	SoC Design Engineer, Intel (DAC'19 Best Paper Award, ISPD 2016 Contest First Place)
30. Zhoufeng Ying (co-supervised with Prof. Ray Chen)	Monolithic and Hybrid Nanophotonic Chips for High-speed and Power-Efficient Optical Computing and Interconnects	Spring 2020	Senior Silicon Photonics Designer, Alpine Optoelectronics (UT-ECE 2019-2020 Jacome Dissertation Prize)
31. Zheng Zhao (co-supervised by Prof Ray Chen)	Design Automation for Optical Computing: Boolean Logic and Neural Networks	Spring 2020	Senior Software Engineer, Synopsys (Cadence Women in Technology Scholarship in 2019)
32. Wei Ye	Design for Manufacturability and Reliability through Learning and Optimization	Spring 2020	Research Scientist, Facebook On-Device AI (ISPD 2020 Best Paper Award, Cadence Women in Technology Scholarship in 2018)
33. Mohamed Baker Alawieh	Machine Learning for VLSI Computer Aided Design	Fall 2020	Senior R&D Engineer, Synopsys (ISPD 2020 Best Paper Award)
34. Sungjin Hong (co-supervised by Prof. Nan Sun)	Design of Portable CMOS NMR System	Spring 2021	Analog/Mixed-Signal Design Engineer, Uhnder
35. Miguel Francisco Gandara (co-supervised by Prof. Nan Sun)	Utilizing Digital Design Techniques and Circuits to Improve Energy and Design Efficiency of Analog and Mixed-Signal Circuits	Spring 2021	Staff Engineer, MediaTek
36. Wei Shi (co-supervised by Prof. Nan Sun)	Design and Automation Techniques for High-Performance Mixed-Signal Circuits	Spring 2022	Research Scientist, Meta (Facebook)
37. Ki Yong Kim (co-supervised by Prof. Ranjit Gharpurey)	Circuits and Architectures for Broadband Spectrum Channelizers with Sub-band Gain Control	Summer 2022	Principal Engineer, Samsung Electronics

38. Keren Zhu	Fully-Automated Layout Synthesis for Analog and Mixed-Signal Integrated Circuits	Summer 2022	Post-doc Researcher, UT Austin (Harry Philip Whitworth Endowed Graduate Fellowship 2021)

POST-DOC SUPERVISIONS COMPLETED:

1. Dr. Xiyuan Tang (postdoc 09/2019 – 05/2021), Assistant Professor, Peking University
2. Arman Roohi (postdoc 08/2019 - 07/2020), Assistant Professor at Department of Computer Science and Engineering, University of Nebraska – Lincoln
3. Shaolan Li (postdoc 06/2018 - 07/2019), Assistant Professor at Department of Electrical and Computer Engineering, Georgia Institute of Technology
4. Yibo Lin (postdoc 06/2018 - 06/2019), Assistant Professor at Department of Computer Science and Center for Energy-Efficient Computing and Applications (CECA), Peking University
5. Bei Yu (postdoc 08/2014 - 07/2015), Assistant Professor at Department of Computer Science and Engineering, Chinese University of Hong Kong

M.S. SUPERVISIONS COMPLETED (with Thesis or Report):

1. Jun Liu, August 2005
2. Andy Havlir, December 2005
3. Emiliano Lozano, May 2008
4. Varsha Dadlani, May 2008
5. Duo Ding, May 2008
6. Ashutosh Chakraborty, May 2008
7. Sean Xiaokang Shi, December 2008
8. Katrina Lu, December 2008
9. Tony Quan, August 2009
10. Anurag Kumar, December 2009
11. Boyang Zhang, May 2012
12. Wen Zhang, August 2012
13. Jagmohan Singh, August 2013
14. Yunfei Sun, May 2021

BS and REU Alumni:

- Joshua Gnanayutham
- Saanika Kenkare
- Rohan Tanna
- Miranda M. Pacheco
- August Shi
- Michael Booker
- Doug Ilijev
- Marc Anthony Gonzalez (B.S. 2011)
- Dhruv Mehrotra (B.S. in Jan. 2004)

Visiting Scholars/Students Alumni:

- Tung-Chieh Chen (National Taiwan University, Taiwan), Jan. – Dec. 2007
- Shanhu Shen (Zhejiang University, China), Sept. 2007 to Aug. 2008
- Ou He (Tsinghua University, China), October 2009 – October 2010
- Yen-Hung Lin (National Chiao Tung University, Taiwan), Mar. to Dec. 2011 (now TSMC)

- Prof. Weifeng Lv (Hangzhou Dianzi University, China), Sept. 2013 – Feb. 2014
- Dr. Junhyung Um (Samsung Electronics Principal Engineer), Jan. to Dec. 2014
- Wei Ye (Zhejiang University), Internship, July to Dec. 2014
- Dr. Tetsuaki Matsunawa (Toshiba), Oct. 2013 – April, 2015
- Vinícius dos Santos Livramento (Federal University of Santa Catarina, Brazil), Jan.– June 2016
- Taiki Kimura (Toshiba, Japan), May 2015 – October 2016
- Prof. Ronghua Jiang (Sichuan University, China), March 2016 – March 2017
- Zhijian Pan (Tsinghua University), Oct. 2016 - April 2017
- Prof. Jun Liu (Hefei University of Technology), Sept. 2016 – Aug. 2017
- Jun Zhang (Nanjing University of Posts & Telecommunications), Nov. 2016 - Oct. 2017
- Prof. Peiyong Zhang (Zhejiang University), Dec. 2016-Dec. 2017
- Prof. Hui Xu (Anhui University of Science & Technology), Oct. 2017 – Sept. 2018
- Prof. Zhiguo Yu (Jiangnan University), Dec. 2017 – Dec. 2018
- Meng Liu (Institute of Automation, Chinese Academy of Sciences), Feb. 2018-Nov. 2018
- Ying Chen (Institute of Microelectronics, Chinese Academy of Sciences), Oct. 2017 – March 2019
- Prof. Kun Ren, Hangzhou Dianzi University, Oct. 2018 to Sept. 2019
- Prof. Wei Hu, Xidian University, Dec. 2018 to Dec. 2019
- Prof. Wooyoung Jang, Dankook University, Jan. 2019 to Feb. 2020
- Jing Chen (NJUPT), July 2018 – September 2020
- Prof. Jae-Joon Kim, Pohang University of Science and Technology, Sept. 2019 to Aug. 2020

David Z. Pan's IEEE Biography:

David Z. Pan (S'97–M'00–SM'06–F'14) received his B.S. degree from Peking University, and his M.S. and Ph.D. degrees from University of California, Los Angeles (UCLA). From 2000 to 2003, he was a Research Staff Member with IBM T. J. Watson Research Center. He is currently a Full Professor and holder of the Silicon Laboratories Endowed Chair in Electrical Engineering at The University of Texas at Austin. His research interests include electronic design automation, synergistic AI/IC co-optimizations, domain-specific accelerators, design for manufacturing, hardware security, and design/CAD for analog/mixed-signal and emerging technologies. He has published over 450 peer-reviewed journal and conference papers, and is the holder of 8 U.S. patents. He has held various advisory, consulting, or visiting positions in academia and industry, such as MIT and Google. He has graduated 43 PhDs/postdocs who are holding key academic and industry positions.

He has served as a Senior Associate Editor for ACM Transactions on Design Automation of Electronic Systems (TODAES), an Associate Editor for IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD), IEEE Transactions on Very Large Scale Integration Systems (TVLSI), IEEE Transactions on Circuits and Systems PART I (TCAS-I), IEEE Transactions on Circuits and Systems PART II (TCAS-II), IEEE Design & Test, Science China Information Sciences, Journal of Computer Science and Technology, IEEE CAS Society Newsletter, etc. He has served in the Executive and Program Committees of many major conferences. He is the ISPD 2008 General Chair, ASP-DAC 2017 Program Chair, ICCAD 2018/2019 Program/General Chair, DAC 2022 Panel Chair, and DAC 2023 Program Vice-Chair.

He has received many prestigious awards for his research contributions, including the SRC Technical Excellence Award in 2013, DAC Top 10 Author in Fifth Decade, DAC Prolific Author Award, ASP-DAC Frequently Cited Author Award, ASP-DAC Prolific Author Award, 20 Best Paper Awards at premier venues (TCAD 2021, ISPD 2020, ASP-DAC 2020, DAC 2019, GLSVLSI 2018, VLSI Integration 2018, HOST 2017, SPIE 2016, ISPD 2014, ICCAD 2013, ASP-DAC 2012, ISPD 2011, IBM Research 2010 Pat Goldberg Memorial Best Paper Award, ASP-DAC 2010, DATE 2009, ICICDT 2009, SRC Techcon in 1998, 2007, 2012 and 2015) and over 18 additional Best Paper Award candidates/finalists, Communications of the ACM Research Highlights (2014), ACM/SIGDA Outstanding New Faculty Award (2005), NSF CAREER Award (2007), SRC Inventor Recognition Award three times, IBM Faculty Award four times, UCLA Engineering Distinguished Young Alumnus Award (2009), UT Austin RAISE Faculty Excellence Award (2014), Cadence Academic Collaboration Award (2019), and many international CAD contest awards, among others. His

students have also won many awards, including the First Place of ACM Student Research Competition Grand Finals (twice, in 2018 and 2021), ACM/SIGDA Student Research Competition Gold Medal (thrice, in 2016, 2017, and 2020), ACM Outstanding PhD Dissertation in EDA (twice, in 2013 and 2018), EDAA Outstanding Dissertation Award (thrice, in 2015, 2019, and 2022), and so on. He is a Fellow of ACM, IEEE, and SPIE.