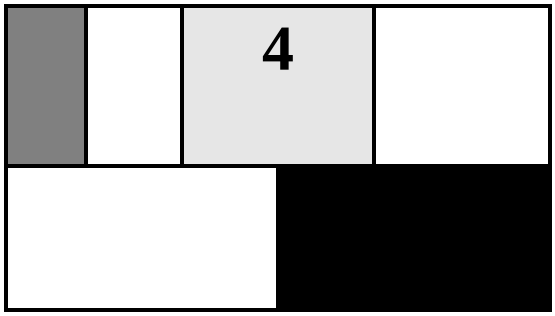
CHAPTER



THE WIRE

Determining and quantifying interconnect parameters

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Introducing circuit models for interconnect wires

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Detailed wire models for SPICE

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Technology scaling and its impact on interconnect

4.1 Introduction

Throughout most of the past history of integrated circuits, on-chip interconnect wires were considered to be second class citizens that had only to be considered in special cases or when performing high-precision analysis. With the introduction of deep-submicron semiconductor technologies, this picture is undergoing rapid changes. The parasitics effects introduced by the wires display a scaling behavior that differs from the active devices such as transistors, and tend to gain in importance as device dimensions are reduced and circuit speed is increased. In fact, they start to dominate some of the relevant metrics of digital integrated circuits such as speed, energy-consumption, and reliability. This situation is aggravated by the fact that improvements in technology make the production of ever-larger die sizes economically feasible, which results in an increase in the average length of an interconnect wire and in the associated parasitic effects. A careful and in-depth analysis of the role and the behavior of the interconnect wire in a semiconductor technology is therefore not only desirable, but even essential.

4.2 A First Glance

The designer of an electronic circuit has multiple choices in realizing the interconnections between the various devices that make up the circuit. State-of-the-art processes offer multiple layers of Aluminum, and at least one layer of polysilicon. Even the heavily doped n^+ or p^+ layers, typically used for the realization of source and drain regions, can be employed for wiring purposes. These wires appear in the schematic diagrams of electronic circuits as simple lines with no apparent impact on the circuit performance. In our discussion on the integrated-circuit manufacturing process, it became clear that this picture is overly simplistic, and that the wiring of today's integrated circuits forms a complex geometry that introduces capacitive, resistive, and inductive parasitics. All three have multiple effects on the circuit behavior.

1. An increase in propagation delay, or, equivalently, a drop in performance.
2. An impact on the energy dissipation and the power distribution.
3. An introduction of extra noise sources, which affects the reliability of the circuit.

A designer can decide to play it safe and include all these parasitic effects in her analysis and design optimization process. This conservative approach is non-constructive and even unfeasible. First of all, a "complete" model is dauntingly complex and is only applicable to very small topologies. It is hence totally useless for today's integrated circuits with their millions of circuit nodes. Furthermore, this approach has the disadvantage that the "forest gets lost between the trees". The circuit behavior at a given circuit node is only determined by a few dominant parameters. Bringing all possible effects to bear, only obscures the picture and turns the optimization and design process a "trial-and-error" operation rather than an enlightened and focused search.

To achieve the latter, it is important that the designer has a clear insight in the parasitic wiring effects, their relative importance, and their models. This is best illustrated with the simple example, shown in Figure 4.1. Each wire in a bus network connects a transmit-

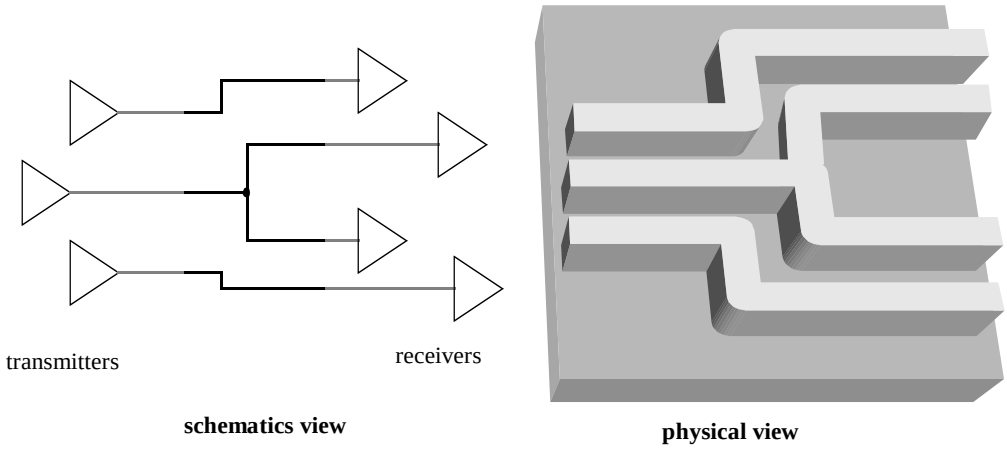


Figure 4.1 Schematic and physical views of wiring of bus-network. The latter shows only a limited area (as indicated by the shadings in the schematics).

ter (or transmitters) to a set of receivers and is implemented as a link of wire segments of various lengths and geometries. Assume that all segments are implemented on a single interconnect layer, isolated from the silicon substrate and from each other by a layer of dielectric material. Be aware that the reality may be far more complex.

A full-fledged circuit model, taking into account the parasitic capacitance, resistance, and the inductance of the interconnections, is shown in Figure 4.2a. Observe that these extra circuit elements are not located in a single physical point, but are distributed over the length of the wire. This is a necessity when the length of the wire becomes significantly larger than its width. Notice also that some parasitics are inter-wire, hence creating coupling effects between the different bus-signals that were not present in the original schematics.

Analyzing the behavior of this schematic, which only models a small part of the circuit, is slow and cumbersome. Fortunately, substantial simplifications can often be made, some of which are enumerated below.

- Inductive effects can be ignored if the resistance of the wire is substantial — this is for instance the case for long Aluminum wires with a small cross-section — or if the rise and fall times of the applied signals are slow.
- When the wires are short, the cross-section of the wire is large, or the interconnect material used has a low resistivity, a capacitance-only model can be used (Figure 4.2b).
- Finally, when the separation between neighboring wires is large, or when the wires only run together for a short distance, inter-wire capacitance can be ignored, and all the parasitic capacitance can be modeled as capacitance to ground.

Obviously, the latter problems are the easiest to model, analyze, and optimize. The experienced designer knows to differentiate between dominant and secondary effects. The goal of this chapter is to present the reader the basic techniques to estimate the values of

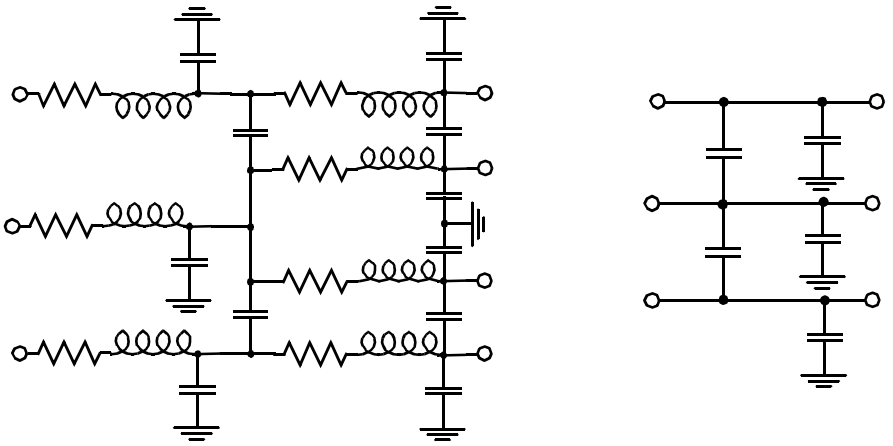


Figure 4.2 Wire models for the circuit of Figure 4.1. Model (a) considers most of the wire parasitics (with the exception of interwire resistance and mutual inductance), while model (b) only considers capacitance.

the various interconnect parameters, simple models to evaluate their impact, and a set of rules-of-thumb to decide when and where a particular model or effect should be considered.

4.3 Interconnect Parameters — Capacitance, Resistance, and Inductance

4.3.1 Capacitance

An accurate modeling of the wire capacitance(s) in a state-of-the-art integrated circuit is a non-trivial task and is even today the subject of advanced research. The task is complicated by the fact that the interconnect structure of contemporary integrated circuits is three-dimensional, as was clearly demonstrated in the process cross-section of FIGURE (CHAPTER 2). The capacitance of such a wire is a function of its shape, its environment, its distance to the substrate, and the distance to surrounding wires. Rather than getting lost in complex equations and models, a designer typically will use an advanced extraction tool to get precise values of the interconnect capacitances of a completed layout. Most semiconductor manufacturers also provide empirical data for the various capacitance contributions, as measured from a number of test dies. Yet, some simple first-order models come in handy to provide a basic understanding of the nature of interconnect capacitance and its parameters, and of how wire capacitance will evolve with future technologies.

Consider first a simple rectangular wire placed above the semiconductor substrate, as shown in Figure 4.3. If the width of the wire is substantially larger than the thickness of the insulating material, it may be assumed that the electrical-field lines are orthogonal to the capacitor plates, and that its capacitance can be modeled by the *parallel-plate capaci-*

tor model (also called *area capacitance*). Under those circumstances, the total capacitance of the wire can be approximated as[1]

$$c_{int} = \frac{\varepsilon_{di}}{t_{di}} WL \tag{4.1}$$

where W and L are respectively the width and length of the wire, and t_{di} and ε_{di} represent the thickness of the dielectric layer and its permittivity. SiO_2 is the dielectric material of choice in integrated circuits, although some materials with lower permittivity, and hence lower capacitance, are coming in use. Examples of the latter are organic polyimides and aerogels. ε is typically expressed as the product of two terms, or $\varepsilon = \varepsilon_r \varepsilon_0$. $\varepsilon_0 = 8.854 \times 10^{-12}$ F/m is the permittivity of free space, and ε_r the relative permittivity of the insulating material. Table 4.1 presents the relative permittivity of several dielectrics used in integrated circuits. In summary, the important message from Eq. (4.1) is that the capacitance is proportional to the overlap between the conductors and inversely proportional to their separation.

Table 4.1 Relative permittivity of some typical dielectric materials.

Material	ε_r
Free space	1
Aerogels	~1.5
Polyimides (organic)	3-4
Silicon dioxide	3.9
Glass-epoxy (PC board)	5
Silicon Nitride (Si_3N_4)	7.5
Alumina (package)	9.5
Silicon	11.7

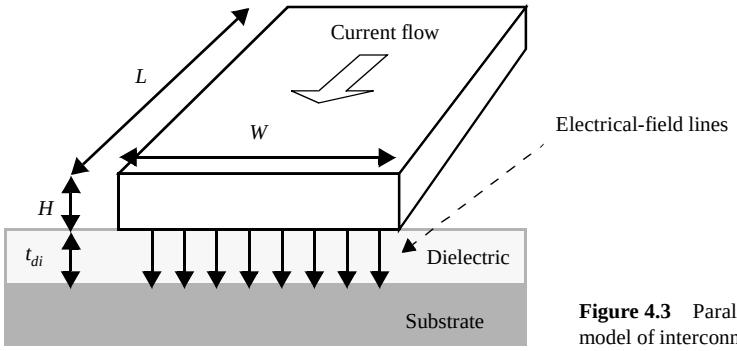
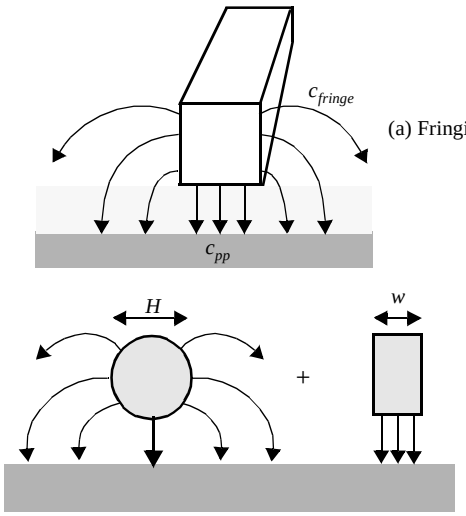


Figure 4.3 Parallel-plate capacitance model of interconnect wire.

[1] To differentiate between distributed (per unit lenght) wire parameters versus total lumped values, we will use lowercase to denote the former and uppercase for the latter.

In actuality, this model is too simplistic. To minimize the resistance of the wires while scaling technology, it is desirable to keep the cross-section of the wire ($W \times H$) as large as possible — as will become apparent in a later section. On the other hand, small values of W lead to denser wiring and less area overhead. As a result, we have over the years witnessed a steady reduction in the W/H-ratio, such that it has even dropped below unity in advanced processes. This is clearly visible on the process cross-section of FIGURE. Under those circumstances, the parallel-plate model assumed above becomes inaccurate. The capacitance between the side-walls of the wires and the substrate, called the *fringing capacitance*, can no longer be ignored and contributes to the overall capacitance. This effect is illustrated in Figure 4.4a. Presenting an exact model for this difficult geometry is hard. So, as good engineering practice dictates, we will use a simplified model that approximates the capacitance as the sum of two components (Figure 4.4b): a parallel-plate capacitance determined by the orthogonal field between a wire of width w and the ground plane, in parallel with the fringing capacitance modeled by a cylindrical wire with a dimension equal to the interconnect thickness H. The resulting approximation is simple and works fairly well in practice.



(a) Fringing fields

(b) Model of fringing-field capacitance.

Figure 4.4 The fringing-field capacitance. The model decomposes the capacitance into two contributions: a parallel-plate capacitance, and a fringing capacitance, modeled by a cylindrical wire with a diameter equal to the thickness of the wire.

$$c_{wire} = c_{pp} + c_{fringe} = \frac{w\varepsilon_{di}}{t_{di}} + \frac{2\pi\varepsilon_{di}}{\log(t_{di}/H)} \tag{4.2}$$

with $w = W - H/2$ a good approximation for the width of the parallel-plate capacitor. Numerous more accurate models (e.g. [Vdmeijs84]) have been developed over time, but these tend to be substantially more complex, and defeat our goal of developing a conceptual understanding.

To illustrate the importance of the fringing-field component, Figure 4.5 plots the value of the wiring capacitance as a function of (W/H). For larger values of (W/H) the total capacitance approaches the parallel-plate model. For (W/H) smaller than 1.5, the fringing

component actually becomes the dominant component. The fringing capacitance can increase the overall capacitance by a factor of more than 10 for small line widths. It is interesting to observe that the total capacitance levels off to a constant value of approximately 1 pF/cm for line widths smaller than the insulator thickness. In other words, the capacitance is no longer a function of the width.

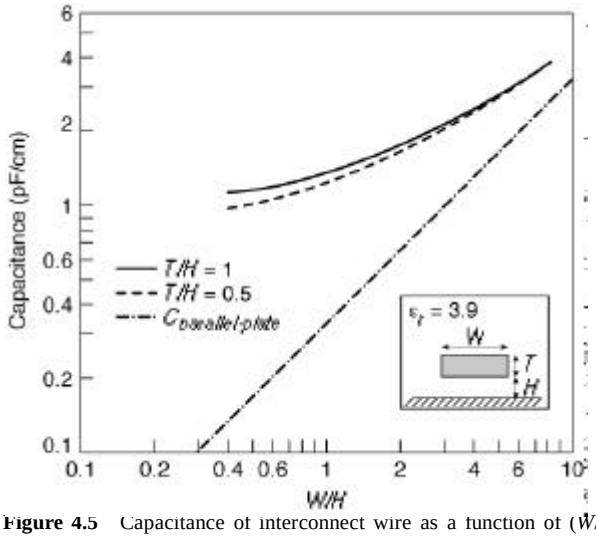


Figure 4.5 Capacitance of interconnect wire as a function of (W/H), including fringing-field effects (from [Schaper83]). Two values of T/H are considered.

So far, we have restricted our analysis to the case of a single rectangular conductor placed over a ground plane. This structure, called a *microstripline*, used to be a good model for semiconductor interconnections when the number of interconnect layers was restricted to 1 or 2. Todays processes offer many more layers of interconnect, which are packed quite densily in addition. In this scenario, the assumption that a wire is completely isolated from its surrounding structures and is only capacitively coupled to ground, becomes untenable. This is illustrated in Figure 4.6, where the capacitance components of a wire embedded in an interconnect hierarchy are identified. Each wire is not only coupled to the grounded substrate, but also to the neighboring wires on the same layer and on adjacent layers. To a first order, this does not change the total capacitance connected to a given wire. The main difference is that not all its capacitive components do terminate at the grounded substrate, but that a large number of them connect to other wires, which have dynamically varying voltage levels. We will later see that these *floating capacitors* form not only a source of noise (crosstalk), but also can have a negative impact on the performance of the circuit.

In summary, interwire capacitances become a dominant factor in multi-layer interconnect structures. This effect is more outspoken for wires in the higher interconnect layers, as these wires are farther away from the substrate. The increasing contribution of the interwire capacitance to the total capacitance with decreasing feature sizes is best illustrated by Figure 4.7. In this graph,which plots the capacitive components of a set of parallel wires routed above a ground plane, it is assumed that dielectric and wire thickness are

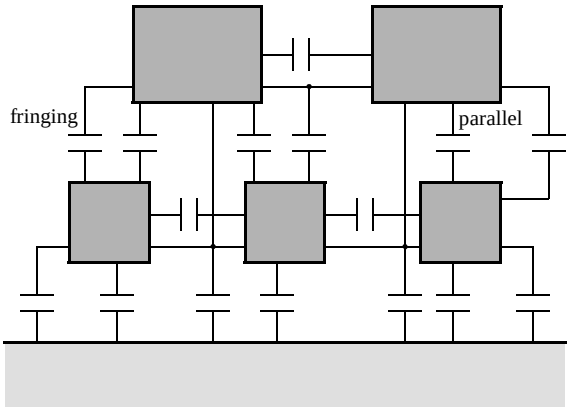


Figure 4.6 Capacitive coupling between wires in interconnect hierarchy.

held constant while scaling all other dimensions. When W becomes smaller than 1.75 H, the interwire capacitance starts to dominate.

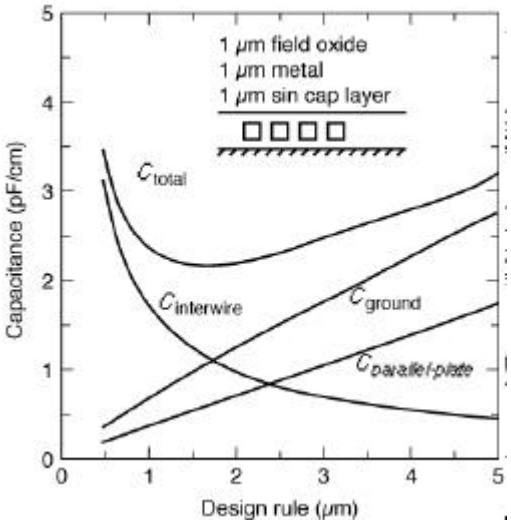


Figure 4.7 Interconnect capacitance as a function of design rules. It consists of a capacitance to ground and an inter-wire capacitance (from [Schaper83]).

Interconnect Capacitance Design Data

A set of typical interconnect capacitances for a standard 0.25 μm CMOS process are given in Table 4.2. The process supports 1 layer of polysylicon and 5 layers of Aluminum. Metal layers 1 to 4 have the same thickness and use a similar dielectric, while the wires at metal layer 5 are almost twice as thick and are embedded in a dielectric with a higher permittivity. When placing the wires over the thick field oxide that is used to isolate different transistors, use the "Field" column in the table, while wires routed over the active area see a higher capacitance as seen in the "Active" column. Be aware that the presented values are only indicative. To obtain more

accurate results for actual structures, complex 3-dimensional models should be used that take the environment of the wire into account.

Table 4.2 Wire area and fringe capacitance values for typical 0.25 μm CMOS process. The table rows represent the top plate of the capacitor, the columns the bottom plate. The area capacitances are expressed in aF/μm^2, while the fringe capacitances (given in the shaded rows) are in aF/μm.

	Field	Active	Poly	Al1	Al2	Al3	Al4
Poly	88						
	54						
Al1	30	41	57				
	40	47	54				
Al2	13	15	17	36			
	25	27	29	45			
Al3	8.9	9.4	10	15	41		
	18	19	20	27	49		
Al4	6.5	6.8	7	8.9	15	35	
	14	15	15	18	27	45	
Al5	5.2	5.4	5.4	6.6	9.1	14	38
	12	12	12	14	19	27	52

Table 4.3 tabulates indicative values for the capacitances between parallel wires placed on the same layer with a minimum spacing (as dictated by the design rules). Observe that these numbers include both the parallel plate and fringing components. Once again, the capacitances are a strong function of the topology. For instance, a ground plane placed on a neighboring layer terminates a large fraction of the fringing field, and effectively reduces the interwire capacitance. The polysilicon wires experience a reduced interwire capacitance due to the smaller thickness of the wires. On the other hand, the thick Al5 wires display the highest interwire capacitance. It is therefore advisable to either separate wires at this level by an amount that is larger than the minimum allowed, or to use it for global signals that are not that sensitive to interference. The supply rails are an example of the latter.

Table 4.3 Interwire capacitance per unit wire length for different interconnect layers of typical 0.25 μm CMOS process. The capacitances are expressed in aF/μm, and are for minimally-spaced wires.

Layer	Poly	Al1	Al2	Al3	Al4	Al5
Capacitance	40	95	85	85	85	115

Example 4.1 Capacitance of Metal Wire

Some global signals, such as clocks, are distributed all over the chip. The length of those wires can be substantial. For die sizes between 1 and 2 cm, wires can reach a length of 10 cm and have associated wire capacitances of substantial value. Consider an aluminum wire of 10 cm long and 1 μm wide, routed on the first Aluminum layer. We can compute the value of the total capacitance using the data presented in Table 4.2.

Area (parallel-plate) capacitance: $(0.1 \times 10^6\ \mu m^2) \times 30\ aF/\mu m^2 = 3\ pF$

Fringing capacitance: $2 \times (0.1 \times 10^6\ \mu m) \times 40\ aF/\mu m = 8\ pF$

Total capacitance: 11 pF

Notice the factor 2 in the computation of the fringing capacitance, which takes the two sides of the wire into account.

Suppose now that a second wire is routed alongside the first one, separated by only the minimum allowed distance. From Table 4.3, we can determine that this wire will couple to the first with a capacitance equal to

$$C_{inter} = (0.1 \times 10^6\ \mu m) \times 95\ aF/\mu m = 9.5\ pF$$

which is almost as large as the total capacitance to ground!

A similar exercise shows that moving the wire to Al4 would reduce the capacitance to ground to 3.45 pF (0.65 pF area and 2.8 pF fringe), while the interwire capacitance would remain approximately the same at 8.5 pF.

4.3.2 Resistance

The resistance of a wire is proportional to its length L and inversily proportional to its cross-section A. The resistance of a rectangular conductor in the style of Figure 4.3 can be expressed as

$$R = \frac{\rho L}{A} = \frac{\rho L}{HW} \tag{4.3}$$

where the constant ρ is the resistivity of the material (in Ω-m). The resistivities of some commonly-used conductive materials are tabulated in Table 4.4. Aluminum is the interconnect material most often used in integrated circuits because of its low cost and its compatibility with the standard integrated-circuit fabrication process. Unfortunately, it has a large resistivity compared to materials such as Copper. With ever-increasing performance targets, this is rapidly becoming a liability and top-of-the-line processes are now increasingly using Copper as the conductor of choice..

Table 4.4 Resistivity of commonly-used conductors (at 20 C).

Material	r (W-m)
Silver (Ag)	1.6×10^{-8}

Table 4.4 Resistivity of commonly-used conductors (at 20 C).

Material	r (W-m)
Copper (Cu)	1.7×10^{-8}
Gold (Au)	2.2×10^{-8}
Aluminum (Al)	2.7×10^{-8}
Tungsten (W)	5.5×10^{-8}

Since H is a constant for a given technology, Eq. (4.3) can be rewritten as follows,

$$R = R_{\square} \frac{L}{W} \tag{4.4}$$

with

$$R_{\square} = \frac{\rho}{H} \tag{4.5}$$

the *sheet resistance* of the material, having units of Ω/❑ (pronounced as Ohm-per-square). This expresses that the resistance of a square conductor is independent of its absolute size, as is apparent from Eq. (4.4). To obtain the resistance of a wire, simply multiply the sheet resistance by its ratio (L/W).

Interconnect Resistance Design Data

Typical values of the sheet resistance of various interconnect materials are given in Table 4.5.

Table 4.5 Sheet resistance values for a typical 0.25 μm CMOS process.

Material	Sheet Resistance (Ω/❑)
n- or p-well diffusion	1000 – 1500
n^+, p^+ diffusion	50 – 150
n^+, p^+ diffusion with silicide	3 – 5
n^+, p^+ polysilicon	150 – 200
n^+, p^+ polysilicon with silicide	4 – 5
Aluminum	0.05 – 0.1

From this table, we conclude that Aluminum is the preferred material for the wiring of long interconnections. Polysilicon should only be used for local interconnect. Although the sheet resistance of the diffusion layer (n^+, p^+) is comparable to that of polysilicon, the use of diffusion wires should be avoided due to its large capacitance and the associated *RC* delay.

Advanced processes also offer silicided polysilicon and diffusion layers. A silicide is a compound material formed using silicon and a refractory metal. This creates a highly conductive material that can withstand high-temperature process steps without melting. Examples of silicides are WSi_2, $TiSi_2$, $PtSi_2$, and TaSi. WSi_2, for instance, has a resistivity ρ of 130 $\mu\Omega$-cm, which is approximately eight times lower than polysilicon. The silicides are most often used in a configuration called a *polycide*, which is a simple layered combination of polysilicon and a silicide. A typical polycide consists of a lower level of polysilicon with an upper coating of silicide and combines the best properties of both materials—good adherence and coverage (from the poly) and high conductance (from the silicide). A MOSFET fabricated with a polycide gate is shown in Figure 4.8. The advantage of the silicided gate is a reduced gate resistance. Similarly, silicided source and drain regions reduce the source and drain resistance of the device.

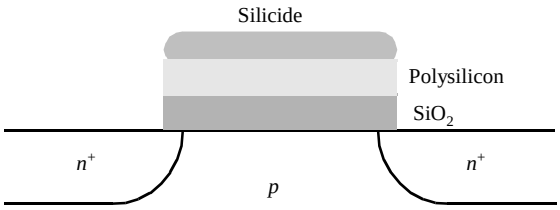


Figure 4.8 A polycide-gate MOSFET.

Transitions between routing layers add extra resistance to a wire, called the *contact resistance*. The preferred routing strategy is thus to keep signal wires on a single layer whenever possible and to avoid excess contacts or vias. It is possible to reduce the contact resistance by making the contact holes larger. Unfortunately, current tends to concentrate around the perimeter in a larger contact hole. This effect, called *current crowding*, puts a practical upper limit on the size of the contact. The following *contact resistances* (for minimum-size contacts) are typical for a 0.25 μm process: 5-20 Ω for metal or polysilicon to n^+, p^+, and metal to polysilicon; 1-5 Ω for via's (metal-to-metal contacts).

Example 4.2 Resistance of a Metal Wire

Consider again the aluminum wire of Example 4.2, which is 10 cm long and 1 μm wide, and is routed on the first Aluminum layer. Assuming a sheet resistance for Al1 of 0.075 Ω/❑, we can compute the total resistance of the wire

$$R_{wire} = 0.075\ \Omega/\square \times (0.1 \times 10^6\ \mu m) / (1\ \mu m) = 7.5\ k\Omega$$

Implementing the wire in polysilicon with a sheet resistance of 175 Ω/❑ raises the overall resistance to 17.5 MΩ, which is clearly unacceptable. Silicided polysilicon with a sheet resistance of 4 Ω/❑ offers a better alternative, but still translates into a wire with a 400 kΩ resistance.

So far, we have considered the resistance of a semiconductor wire to be linear and constant. This is definitely the case for most semiconductor circuits. At very high frequencies however, an additional phenomenum — called the *skin effect* — comes into play such that the resistance becomes frequency-dependent. High-frequency currents tend to flow primarily on the surface of a conductor with the current density falling off exponentially

with depth into the conductor. The *skin depth* δ is defined as the depth where the current falls off to a value of e^{-1} of its nominal value, and is given by

$$\delta = \sqrt{\frac{\rho}{\pi f \mu}} \tag{4.6}$$

with f the frequency of the signal and μ the permeability of the surrounding dielectric (typically equal to the permeability of free space, or $\mu = 4\pi \times 10^{-7}$ H/m). For Aluminum at 1 GHz, the skin depth is equal to 2.6 μm. The obvious question is now if this is something we should be concerned about when designing state-of-the-art digital circuits?

The effect can be approximated by assuming that the current flows uniformly in an outer shell of the conductor with thickness δ, as is illustrated in Figure 4.9 for a rectangular wire. Assuming that the overall cross-section of the wire is now limited to approxi-

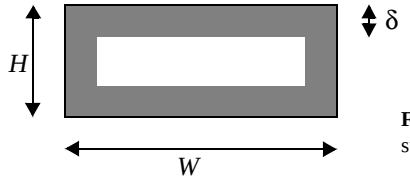


Figure 4.9 The skin-effect reduces the flow of the current to the surface of the wire.

mately $2(W+H)\delta$, we obtain the following expression for the resistance (per unit length) at high frequencies ($f > f_s$):

$$r(f) = \frac{\sqrt{\pi f \mu \rho}}{2(H + W)} \tag{4.7}$$

The increased resistance at higher frequencies may cause an extra attenuation — and hence distortion — of the signal being transmitted over the wire. To determine the on-set of the skin-effect, we can find the frequency f_s where the skin depth is equal to half the largest dimension (W or H) of the conductor. Below f_s the whole wire is conducting current, and the resistance is equal to (constant) low-frequency resistance of the wire. From Eq. (4.6), we find the value of f_s:

$$f_s = \frac{4\rho}{\pi \mu (\max(W, H))^2} \tag{4.8}$$

Example 4.3 Skin-effect and Aluminum wires

We determine the impact of the skin-effect on contemporary integrated circuits by analyzing an Aluminum wire with a resistivity of 2.7×10^{-8} Ω-m, embedded in a SiO_2 dielectric with a permeability of $4\pi \times 10^{-7}$ H/m. From Eq. (4.8), we find that the largest dimension of wire should be at least 5.2 μm for the effect to be noticable at 1 GHz. This is confirmed by the more accurate simulation results of Figure 4.10, which plots the increase in resistance due to skin effects for different width Aluminum conductors. A 30% increase in resistance

can be observed at 1 GHz for a 20 μm wire, while the increase for a 1 μm wire is less than 1%.

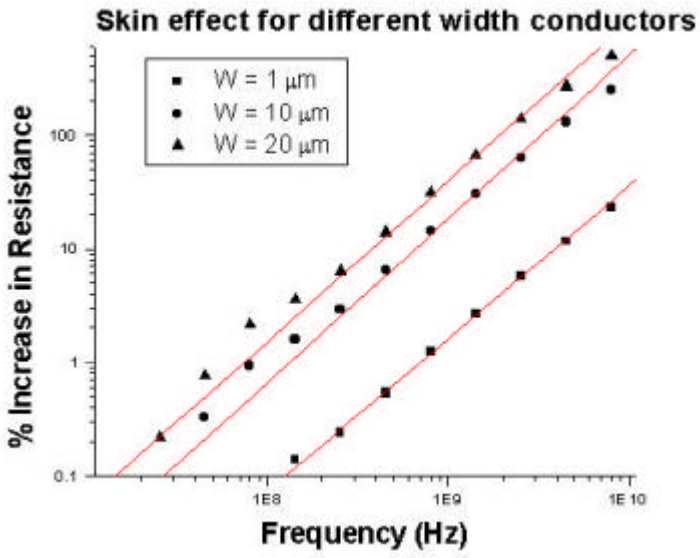


Figure 4.10 Skin-effect induced increase in resistance as a function of frequency and wire width. All simulations were performed for a wire thickness of 0.7 μm [Sylvester97].

In summary, the skin-effect is only an issue for wider wires. Since clocks tend to carry the highest-frequency signals on a chip and also are fairly wide to limit resistance, the skin effect is likely to have its first impact on these lines. This is a real concern for GHz-range design, as clocks determine the overall performance of the chip (cycle time, instructions per second, etc.). Another major design concern is that the adoption of better conductors such as Copper may move the on-set of skin-effects to lower frequencies.

4.3.3 Inductance

Integrated-circuit designers tend to dismiss inductance as something they heard about in their physics classes, but that has no impact on their field. This was definitely the case in the first decades of integrated digital circuit design. Yet with the adoption of low-resistive interconnect materials and the increase of switching frequencies to the super GHz range, inductance starts to play a role even on a chip. Consequences of on-chip inductance include ringing and overshoot effects, reflections of signals due to impedance mismatch, inductive coupling between lines, and switching noise due to Ldi/dt voltage drops.

The inductance of a section of a circuit can always be evaluated with the aid of its definition, which states that a changing current passing through an inductor generates a voltage drop DV

$$\Delta V = L\frac{di}{dt} \tag{4.9}$$

It is possible to compute the inductance a wire directly from its geometry and its environment. A simpler approach relies on the fact that the capacitance c and the inductance l (per unit length) of a wire are related by the following expression

$$cl = \varepsilon\mu \tag{4.10}$$

with ε and μ respectivily the permittivity and permeability of the surrounding dielectric. The caveat is that for this expression to be valid the conductor must be completely surrounded by a uniform dielectric medium. This is most often not the case. Yet even when the wire is embedded in different dielectric materials, its is possible to adopt "average" dielectric constants such that Eq. (4.10) still can be used to get an approximative value of the inductance.

Some other interesting relations, obtained from Maxwell's laws, can be pointed out. The constant product of permeability and permittivity also defines the speed ν at which an electromagnetic wave can propagate through the medium

$$\nu = \frac{1}{\sqrt{lc}} = \frac{1}{\sqrt{\varepsilon\mu}} = \frac{c_0}{\sqrt{\varepsilon_r\mu_r}} \tag{4.11}$$

c_0 equals the speed of light (30 cm/nsec) in a vacuum. The propagation speeds for a number of materials used in the fabrication of electronic circuits are tabulated in Table 4.6. The propagation speed for SiO_2 is two times slower than in a vacuum.

Table 4.6 Dielectric constants and wave-propagation speeds for various materials used in electronic circuits. The relative permeability μ_r of most dielectrics is approximately equal to 1.

Dielectric	ε_r	Propagation speed (cm/nsec)
Vacuum	1	30
SiO_2	3.9	15
PC board (epoxy glass)	5.0	13
Alumina (ceramic package)	9.5	10

Example 4.4 Inductance of a Semiconductor Wire

Consider an Al1 wire implemented in the 0.25 micron CMOS technology and routed on top of the field oxide. From Table 4.2, we can derive the capacitance of the wire per unit length:

$$c = (W\times 30 + 2\times 40)\ \text{aF/}\mu\text{m}$$

From Eq. (4.10), we can derive the inductance per unit length of the wire, assuming SiO_2 as the dielectric and assuming a uniform dielectric (make sure to use the correct units!)

$$l = (3.9 \times 8.854 \times 10^{-12}) \times (4\ \pi\ 10^{-7}) / C$$

For wire widths of 0.4 μm, 1μm and 10μm, this leads to the following numbers:

W = 0.4 μm: c = 92 aF/μm; l = 0.47 pH/μm
W = 1 μm: c = 110 aF/μm; l = 0.39 pH/μm
W = 10 μm: c = 380 aF/μm; l = 0.11 pH/μm

Assuming a sheet resistance of 0.075 Ω/❑, we can also determine the resistance of the wire,

$$r = 0.075/W\ \Omega/\mu m$$

It is interesting to observe that the inductive part of the wire impedance becomes equal in value to the resistive component at a frequency of 27.5 GHz (for a 1 μm wide wire), as can be obtained from solving the following expression:

$$\omega l = 2\pi f l = r$$

For extra wide wires, this frequency reduces to approximately 11 GHz. For wires with a smaller capacitance and resistance (such as the thicker wires located at the upper interconnect layers), this frequency can become as low as 500 MHz, especially when better interconnect materials such as Copper are being used. Yet, these numbers indicate that inductance only becomes an issue in integrated circuits for frequencies that are well above 1 GHz.

4.4 Electrical Wire Models

In previous sections, we have introduced the electrical properties of the interconnect wire — capacitance, resistance, and inductance — and presented some simple relations and techniques to derive their values from the interconnect geometries and topologies. These parasitic elements have an impact on the electrical behavior of the circuit and influence its delay, power dissipation, and reliability. To study these effects requires the introduction of electrical models that estimate and approximate the real behavior of the wire as a function of its parameters. These models vary from very simple to very complex depending upon the effects that are being studied and the required accuracy. In this section, we first derive models for manual analysis, while how to cope with interconnect wires in the SPICE circuit simulator is the topic follows next.

4.4.1 The Ideal Wire

In schematics, wires occur as simple lines with no attached parameters or parasatics. These wires have no impact on the electrical behavior of the circuit. A voltage change at one end of the wire propagates immediately to its other ends, even if those are some distance away. Hence, it may be assumed that the same voltage is present at every segment of the wire at the every point in time, and that the whole wire is an *equipotential region*. While this *ideal-wire model* is simplistic, it has its value, especially in the early phases of the design process when the designer wants to concentrate on the properties and the behavior of the transistors that are being connected. Also, when studying small circuit components such as gates, the wires tend to be very short and their parasitics ignorable. Taking these into account would just make the analysis unnecessarily complex. More often though, wire parasitics play a role and more complex models should be considered.

4.4.2 The Lumped Model

The circuit parasitics of a wire are distributed along its length and are not lumped into a single position. Yet, when only a single parasitic component is dominant, when the interaction between the components is small, or when looking at only one aspect of the circuit behavior, it is often useful to lump the different fractions into a single circuit element. The advantage of this approach is that the effects of the parasitic then can be described by an ordinary differential equation. As we will see later, the description of a distributed element requires partial differential equations.

As long as the resistive component of the wire is small and the switching frequencies are in the low to medium range, it is meaningful to consider only the capacitive component of the wire, and to lump the distributed capacitance into a single capacitor as shown in Figure 4.11. Observe that in this model the wire still represents an equipotential region, and that the wire itself does not introduce any delay. The only impact on performance is introduced by the loading effect of the capacitor on the driving gate. This capacitive lumped model is simple, yet effective, and is the model of choice for the analysis of most interconnect wires in digital integrated circuits.

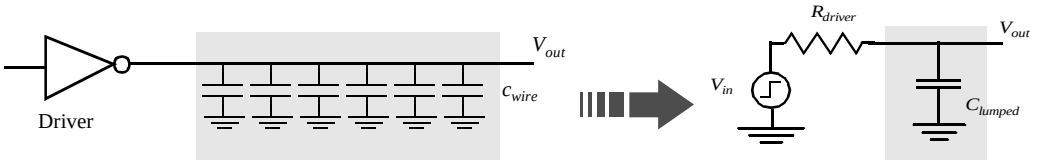


Figure 4.11 Distributed versus lumped capacitance model of wire. $C_{lumped} = L \times c_{wire}$, with L the length of the wire and cwire the capacitance per unit length. The driver is modeled as a voltage source and a source resistance R_{driver}.

Example 4.5 Lumped capacitance model of wire

For the circuit of Figure 4.11, assume that a driver with a source resistance of 10 kΩ is used to drive a 10 cm long, 1 μm wide Al1 wire. In Example 4.1, we have found that the total lumped capacitance for this wire equals 11 pf.

The operation of this simple RC network is described by the following ordinary differential equation:

$$C_{lumped}\frac{dV_{out}}{dt} + \frac{V_{out} - V_{in}}{R_{driver}} = 0$$

When applying a step input (with V_{in} going from 0 to V), the transient response of this circuit is known to be an exponential function, and is given by the following expression (where $\tau = R_{driver} \cdot C_{lumped}$, the time constant of the network):

$$V_{out}(t) = (1 - e^{-t/\tau})\, V$$

The time to reach the 50% point is easily computed as $t = \ln(2)\tau = 0.69\tau$. Similarly, it takes $t = \ln(9)\tau = 2.2\tau$ to get to the 90% point. It is worth memorizing these numbers, as they are extensively used in the rest of the text. Plugging in the numbers for this specific example yields

$$t_{50\%} = 0.69 \times 10\ \text{K}\Omega \times 11\ \text{pF} = 76\ \text{nsec}$$
$$t_{90\%} = 2.2 \times 10\ \text{K}\Omega \times 11\ \text{pF} = 242\ \text{nsec}$$

These numbers are not even acceptable for the lowest performance digital circuits. Techniques to deal with this bottleneck, such as reducing the source resistance of the driver, will be introduced in Chapter ZZZ.

While the lumped capacitor model is the most popular, sometimes it is also useful to present lumped models of a wire with respect to either resistance and inductance. This is often the case when studying the supply distribution network. Both the resistance and inductance of the supply wires can be interpreted as parasitic noise sources that introduce voltage drops and bounces on the supply rails.

4.4.3 The Lumped *RC* model

On-chip metal wires of over a few mm length have a significant resistance. The equipotential assumption, presented in the lumped-capacitor model, is no longer adequate, and a resistive-capacitive model has to be adopted.

A first approach lumps the total wire resistance of each wire segment into one single *R* and similarly combines the global capacitance into a single capacitor *C*. This simple model, called the *lumped RC model* is pessimistic and inaccurate for long interconnect wires, which are more adequately represented by a *distributed rc-model*. Yet, before analyzing the distributed model, its is worthwhile to spend some time on the analysis and the modeling of lumped *RC* networks for the following reasons:

- The distributed *rc*-model is complex and no closed form solutions exist. The behavior of the distributed *rc*-line can be adequately modeled by a simple *RC* network.
- A common practice in the study of the transient behavior of complex transistor-wire networks is to reduce the circuit to an *RC* network. Having a means to analyze such a network effectively and to predict its first-order response would add a great asset to the designers tool box.

In Example 4.5, we analyzed a single resistor-single capacitor network. The behavior of such a network is fully described by a single differential equation, and its transient waveform is a modeled by an exponential with a single time-constant (or network pole). Unfortunately, deriving the correct waveforms for a network with a larger number of capacitors and resistors rapidly becomes hopelessly complex: describing its behavior requires a set of ordinary differential equations, and the network now contains many time-constants (or poles and zeros). Short of running a full-fledged SPICE simulation, delay calculation methods such as the *Elmore delay formula* come to the rescue [Elmore48].

Consider the resistor-capacitor network of Figure 4.12. This circuit is called an *RC-tree* and has the following properties:

- the network has a single input node (called *s* in Figure 4.12)
- all the capacitors are between a node and the ground
- the network does not contain any resistive loops (which makes it a tree)

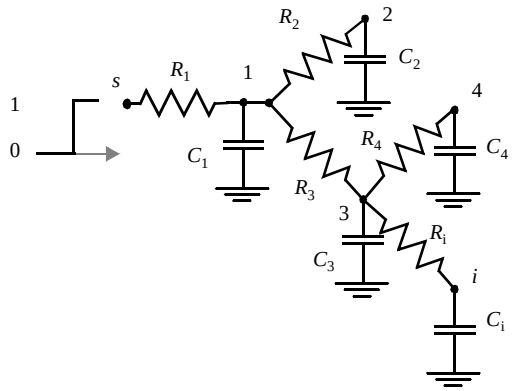


Figure 4.12 Tree-structured *RC* network.

An interesting result of this particilar circuit topology is that there exists a unique resistive path between the source node *s* and any node *i* of the network. The total resistance along this path is called the *path resistance* R_{ii}. For example, the path resistance between the source node *s* and node 4 in the example of Figure 4.12 equals

$$R_{44} = R_1 + R_3 + R_4$$

The definition of the path resistance can be extended to address the *shared path resistance* R_{ik}, which represents the resistance shared among the paths from the root node *s* to nodes *k* and *i*:

$$R_{ik} = \sum R_j \Rightarrow (R_j \in [path(s \rightarrow i) \cap path(s \rightarrow k)]) \tag{4.12}$$

For the circuit of Figure 4.12, $R_{i4} = R_1 + R_3$ while $R_{i2} = R_1$.

Assume now that each of the *N* nodes of the network is initially discharged to GND, and that a step input is applied at node *s* at time $t = 0$. The Elmore delay at node *i* is then given by the following expression:

$$\tau_{Di} = \sum_{k=1}^{N} C_k R_{ik} \tag{4.13}$$

The Elmore delay is equivalent to the first-order time constant of the network (or the first moment of the impulse response). The designer should be aware that this time-constant represents a simple approximation of the actual delay between source node and node *i*. Yet in most cases this approximation has proven to be quite reasonable and acceptable. It offers the designer a powerful mechanism for providing a quick estimate of the delay of a complex network.

Example 4.6 *RC* delay of a tree-structured network

Using Eq. (4.13), we can compute the Elmore delay for node *i* in the network of Figure 4.12.

$$\tau_{Di} = R_1C_1 + R_1C_2 + (R_1 + R_3)C_3 + (R_1 + R_3)C_4 + (R_1 + R_3 + R_i)C_i$$

As a special case of the *RC* tree network, let us consider the simple, non-branched *RC* chain (or ladder) shown in Figure 4.13. This network is worth analyzing because it is a structure that is often encountered in digital circuits, and also because it represents an approximative model of a resistive-capacitive wire. The Elmore delay of this chain network can be derived with the aid of Eq. (4.13):

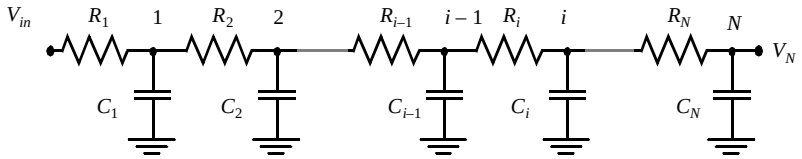


Figure 4.13 *RC* chain.

$$\tau_{DN} = \sum_{i=1}^{N} C_i \sum_{j=1}^{i} R_j = \sum_{i=1}^{N} C_i R_{ii} \tag{4.14}$$

or the shared-path resistance is replaced by simply the path resistance. As an example, consider node 2 in the *RC* chain of Figure 4.13. Its time-constant consists of two components contributed by nodes 1 and 2. The component of node 1 consists of C_1R_1 with R_1 the total resistance between the node and the source, while the contribution of node 2 equals $C_2(R_1 + R_2)$. The equivalent time constant at node *2* equals $C_1R_1 + C_2(R_1 + R_2)$. τ_i of node *i* can be derived in a similar way.

$$\tau_{Di} = C_1R_1 + C_2(R_1 + R_2) + \ldots + C_i(R_1 + R_2 + \ldots + R_i)$$

Example 4.7 Time-Constant of Resistive-Capacitive Wire

The model presented in Figure 4.13 can be used as an approximation of a resistive-capacitive wire. The wire with a total length of *L* is partitioned into *N* identical segments, each with a length of L/N. The resistance and capacitance of each segment are hence given by rL/N and cL/N, respectively. Using the Elmore formula, we can compute the dominant time-constant of the wire:

$$\tau_{DN} = \left(\frac{L}{N}\right)^2 (rc + 2rc + \ldots + Nrc) = (rcL^2)\frac{N(N+1)}{2N^2} = RC\frac{N+1}{2N} \tag{4.15}$$

with R (= rL) and C (= cL) the total lumped resistance and capacitance of the wire. For very large values of *N*, this model asymptotically approaches the distributed *rc* line. Eq. (4.15) then simplifies to the following expression:

$$\tau_{DN} = \frac{RC}{2} = \frac{rcL^2}{2} \tag{4.16}$$

Eq. (4.16) leads to two important conclusions:

- The delay of a wire is **a quadratic function of its length**! This means that doubling the length of the wire quadruples its delay.

- The delay of the distributed *rc*-line is **one half of the delay** that would have been predicted by the lumped *RC* model. The latter combines the total resistance and capacitance into single elements, and has a time-constant equal to *RC* (as is also obtained by setting $N = 1$ in Eq. (4.15)). This confirms the observation made earlier that the lumped model presents a pessimistic view on the delay of resistive wire.

WARNING: Be aware that an *RC*-chain is characterized by a number of time-constants. The Elmore expression determines the value of only the dominant one, and presents thus a first-order approximation.

The Elmore delay formula has proven to be extremely useful. Besides making it possible to analyze wires, the formula can also be used to approximate the propagation delay of complex transistor networks. In the switch model, transistors are replaced by their equivalent, linearized on-resistance. The evaluation of the propagation delay is then reduced to the analysis of the resulting *RC* network. More precise minimum and maximum bounds on the voltage waveforms in an *RC* tree have further been established [Rubinstein83]. These bounds have formed the base for most computer-aided timing analyzers at the switch and functional level [Horowitz83]. An interesting result [Ref] is that the exponential voltage waveform with the Elmore delay as time constant is always situated between these min and max bounds, which demonstrates the validity of the Elmore approximation.

4.4.4 The Distributed *rc* Line

In the previous paragraphs, we have shown that the lumped *RC* model is a pessimistic model for a resistive-capacitive wire, and that a distributed *rc* model (Figure 4.14a) is more appropriate. As before, L represents the total length of the wire, while r and c stand for the resistance and capacitance per unit length. A schematic representation of the distributed *rc* line is given in Figure 4.14b.

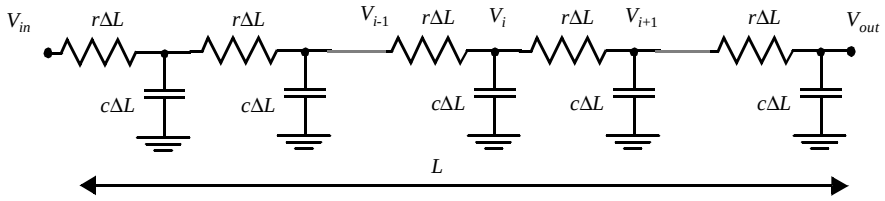
The voltage at node i of this network can be determined by solving the following set of partial differential equations:

$$c\Delta L\frac{\partial V_i}{\partial t} = \frac{(V_{i+1} - V_i) + (V_i - V_{i-1})}{r\Delta L} \tag{4.17}$$

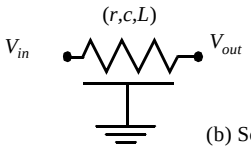
The correct behavior of the distributed *rc* line is then obtained by reducing ΔL asymptotically to 0. For $\Delta L \rightarrow 0$, Eq. (4.17) becomes the well-known *diffusion equation*:

$$rc\frac{\partial V}{\partial t} = \frac{\partial^2 V}{\partial x^2} \tag{4.18}$$

where V is the voltage at a particular point in the wire, and x is the distance between this point and the signal source. No closed-form solution exists for this equation, but approximative expressions such as the formula presented in Eq. (4.19) can be derived [Bakoglu90]. These equations are difficult to use for ordinary circuit analysis. It is known however that the distributed *rc* line can be approximated by a lumped *RC* ladder network,



(a) Distributed model



(b) Schematic symbol for distributed *RC* line

Figure 4.14 Distributed RC line wire-model and its schematic symbol.

which can be easily used in computer-aided analysis. Some of these models will be presented in a later section, discussing SPICE wire models.

$$\begin{aligned} V_{out}(t) &= 2erfc\left(\sqrt{\frac{RC}{4t}}\right) && t \ll RC \\ &= 1.0 - 1.366e^{-2.5359\frac{t}{RC}} + 0.366e^{-9.4641\frac{t}{RC}} && t \gg RC \end{aligned} \tag{4.19}$$

Figure 4.15 shows the response of a wire to a step input, plotting the waveforms at different points in the wire as a function of time. Observe how the step waveform "diffuses" from the start to the end of the wire, and the waveform rapidly degrades, resulting in a considerable delay for long wires. Driving these *rc* lines and minimizing the delay and

signal degradation is one of the trickiest problems in modern digital integrated circuit design. It hence will receive considerable attention in later chapters.

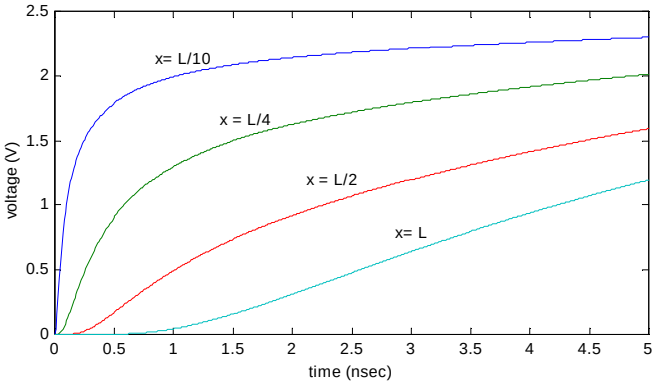


Figure 4.15 Simulated step response of resistive-capacitive wire as a function of time and place.

Some of the important reference points in the step response of the lumped and the distributed RC model of the wire are tabulated in Table 4.7. For instance, the propagation delay (defined at 50% of the final value) of the lumped network not surprisingly equals 0.69 *RC*. The distributed network, on the other hand, has a delay of only 0.38 *RC*, with *R* and *C* the total resistance and capacitance of the wire. This confirms the result of Eq. (4.16).

Table 4.7 Step response of lumped and distributed *RC* networks—points of Interest.

Voltage range	Lumped *RC* network	Distributed *RC* network
$0 \rightarrow 50\%$ (t_p)	0.69 *RC*	0.38 *RC*
$0 \rightarrow 63\%$ (τ)	*RC*	0.5 *RC*
$10\% \rightarrow 90\%$ (t_r)	2.2 *RC*	0.9 *RC*
$0\% \rightarrow 90\%$	2.3 *RC*	1.0 *RC*

Example 4.8 *RC* delay of Aluminum Wire

Let us consider again the 10 cm long, 1 µm wide Al1 wire of Example 4.1. In Example 4.4, we derived the following values for *r* and *c*:

$$c = 110 \text{ aF/µm}; \; r = 0.075 \; \Omega/\mu\text{m};$$

Using the entry of Table 4.7, we derive the propagation delay of the wire:

$$t_p = 0.38 \; RC = 0.38 \times (\, 0.075 \; \Omega/\mu\text{m}) \times (\, 110 \text{ aF/µm}) \times (10^5 \; \mu\text{m})^2 = 31.4 \text{ nsec}$$

We can also deduce the propagation delays of an identical wire implemented in polysilicon and Al5. The values of the capacitances are obtained from Table 4.2, while the resistances are assumed to be respectively 150 Ω/µm and 0.0375 Ω/µm for Poly and Al5:

Poly: $t_p = 0.38 \times (\ 150\ \Omega/\mu m) \times (\ 88 + 2 \times 54\ aF/\mu m) \times (10^5\ \mu m)^2 = 112\ \mu sec!$

Al5: $t_p = 0.38 \times (\ 0.0375\ \Omega/\mu m) \times (\ 5.2 + 2 \times 12\ aF/\mu m) \times (10^5\ \mu m)^2 = 4.2\ nsec$

Obviously, the choice of the interconnect material and layer has a dramatic impact on the delay of the wire.

An important question for a designer to answer when analyzing an interconnect network whether the effects of *RC* delays should be considered, or whether she can get away with a simpler lumped capacitive model. A simple rule of thumb proves to be very useful here.

Design Rules of Thumb

- ***rc* delays should only be considered when $t_{pRC} >> t_{pgate}$ of the driving gate.**

This translates into Eq. (4.20), which determines the critical length *L* of the interconnect wire where *RC* delays become dominant.

$$L_{crit} >> \sqrt{\frac{t_{pgate}}{0.38rc}} \tag{4.20}$$

The actual value of L_{crit} depends upon the sizing of the driving gate and the chosen interconnect material.

- ***rc* delays should only be considered when the rise (fall) time at the line input is smaller than *RC*, the rise (fall) time of the line.**

$$t_{rise} < RC \tag{4.21}$$

with R and C the total resistance and capacitance of the wire. When this condition is not met, the change in signal is slower than the propgation delay of the wire, and a lumped capacitive model suffices.

Example 4.9 *RC* versus Lumped *C*

The presented rule can be illustrated with the aid of the simple circuit shown in Figure 4.16. It is assumed here that the driving gate can be modeled as voltage source with a finite source resistance R_s. The total propagation delay of the network can be approximated by the following expression, obtained by applying the Elmore formula:[2]

$$\tau_D = R_s C_w + \frac{R_w C_w}{2} = R_s C_w + 0.5 r_w c_w L^2$$

and

[2] Hint: replace the wire by the lumped RC network of Figure 4.13 and apply the Elmore equation on the resulting network.

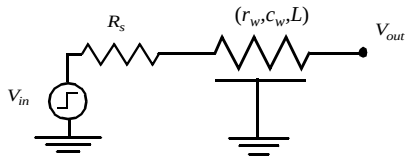


Figure 4.16 *rc*-line of length *L* driven by source with resistance equal to R_s.

$$t_p = 0.69R_sC_w + 0.38R_wC_w$$

with $R_w = rL$ and $C_w = cL$. The delay introduced by the wire resistance becomes dominant when $(R_wC_w)/2 \geq R_sC_w$, or $L \geq 2R_s/r$. Assume now a driver with a source resitance of 1 kΩ, driving an Al1 wire of 1 μm wide (r = 0.075 Ω/μm). This leads to a critical lenght of 2.67 cm.

4.4.5 The Transmission Line

When the switching speeds of the circuits become sufficiently fast, and the quality of the interconnect material become high enough so that the resistance of the wire is kept within bounds, the inductance of the wire starts to dominate the delay behavior, and transmission line effects must be considered. This is more precisely the case when the rise and fall times of the signal become comparable to the time of flight of the signal waveform across the line as determined by the speed of light. With the advent of Copper interconnect and the high switching speeds enabled by the deep-submicron technologies, transmission line effects are soon to be considered in the fastest CMOS designs.

In this section, we first analyze the transmission line model. Next, we apply it to the current semiconductor technology and determine when those effects should be actively considered in the design process.

Transmission Line Model

Similar to the resistance and capacitance of an interconnect line, the inductance is distributed over the wire. A distributed *rlc* model of a wire, known as the transmission line model, becomes the most accurate approximation of the actual behavior. The transmission line has the prime property that a signal propagates over the interconnection medium as a *wave*. This is in contrast to the distributed *rc* model, where the signal *diffuses* from the source to the destination governed by the diffusion equation, Eq. (4.18). In the wave mode, a signal propagates by alternatively transferring energy from the electric to the magnetic fields, or equivalently from the capacitive to the inductive modes.

Consider the point *x* along the transmission line of Figure 4.17 at time *t*. The following set of equations holds:

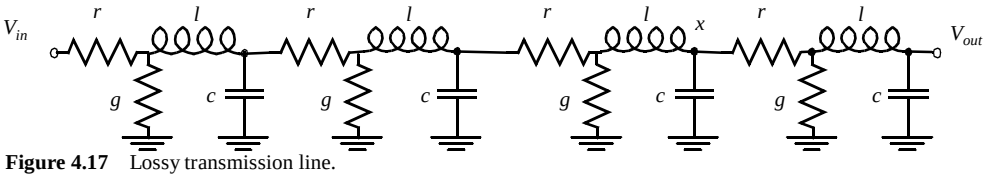


Figure 4.17 Lossy transmission line.

$$\frac{\partial v}{\partial x} = -ri - l\frac{\partial i}{\partial t}$$
$$\frac{\partial i}{\partial x} = -gv - c\frac{\partial v}{\partial t} \tag{4.22}$$

Assuming that the leakage conductance g equals 0, which is true for most insulating materials, and eliminating the current i yields the *wave propagation equation*, Eq. (4.23).

$$\frac{\partial^2 v}{\partial x^2} = rc\frac{\partial v}{\partial t} + lc\frac{\partial^2 v}{\partial t^2} \tag{4.23}$$

where r, c, and l are the resistance, capacitance, and inductance per unit length, respectively.

To understand the behavior of the transmission line, we will first assume that the resistance of the line is small. In this case, a simplified capacitive/inductive model, called the *lossless transmission line*, is appropriate. This model is applicable for wires at the printed-circuit board level. Due to the high conductivity of the Copper interconnect material used there, the resistance of the transmission line can be ignored. On the other hand, resistance plays an important role in integrated circuits, and a more complex model, called the *lossy transmission line* should be considered. The lossy model is only discussed briefly at the end.

The Lossless Transmission Line

For the lossless line, Eq. (4.23) simplifies to the *ideal wave* equation:

$$\frac{\partial^2 v}{\partial x^2} = lc\frac{\partial^2 v}{\partial t^2} = \frac{1}{\nu^2}\frac{\partial^2 v}{\partial t^2} \tag{4.24}$$

A step input applied to a lossless transmission line propagates along the line with a speed ν, given by Eq. (4.11) and repeated below.

$$\nu = \frac{1}{\sqrt{lc}} = \frac{1}{\sqrt{\varepsilon\mu}} = \frac{c_0}{\sqrt{\varepsilon_r\mu_r}} \tag{4.25}$$

Even though the values of both l and c depend on the geometric shape of the wire, their product is a constant and is only a function of the surrounding media. The propagation delay per unit wire length (t_p) of a transmission line is the inverse of the speed:

$$t_p = \sqrt{lc} \tag{4.26}$$

Let us now analyze how a wave propagates along a lossless transmission line. Suppose that a voltage step V has been applied at the input and has propagated to point x of the line (Figure 4.18). All currents are equal to 0 at the right side of x, while the voltage over the line equals V at the left side. An additional capacitance cdx must be charged for the wave to propagate over an additional distance dx. This requires the following current:

$$I = \frac{dQ}{dt} = c\frac{dx}{dt}V = c\nu V = \sqrt{\frac{c}{l}}V \tag{4.27}$$

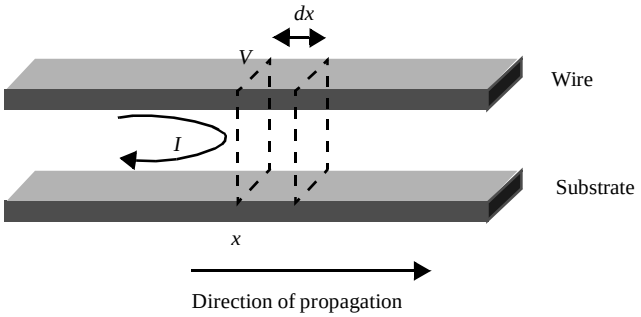


Figure 4.18 Propagation of voltage step along a lossless transmission line.

since the propagation speed of the signal dx/dt equals ν. This means that the signal sees the remainder of the line as areal impedance,

$$Z_0 = \frac{V}{I} = \sqrt{\frac{l}{c}} = \frac{\sqrt{\varepsilon\mu}}{c} = \frac{1}{c\nu}. \tag{4.28}$$

This impedance, called the *characteristic impedance* of the line, is a function of the dielectric medium and the geometry of the conducting wire and isolator (Eq. (4.28)), and is independent of the length of the wire and the frequency. That a line of arbitrary length has a constant, real impedance is a great feature as it simplifies the design of the driver circuitry. Typical values of the characteristic impedance of wires in semiconductor circuits range from 10 to 200 Ω.

Example 4.10 Propagation Speeds of Signal Waveforms

The information of Table 4.6 shows that it takes 1.5 nsec for a signal wave to propagate from source-to-destination on a 20 cm wire deposited on an epoxy printed-circuit board. If transmission line effects were an issue on silicon integrated circuits, it would take 0.67 nsec for the signal to reach the end of a 10 cm wire.

WARNING: The characteristic impedance of a wire is a function of the overall interconnect topology. The electro-magnetic fields in complex interconnect structures tend to be irregular, and are strongly influenced by issues such as the current return path. Providing a general answer to the latter problem has so far proven to be illusive, and no closed-formed

analytical solutions are typically available. Hence, accurate inductance and characteristic impedance extraction is still an active research topic. For some simplified structures, approximative expressions have been derived. For instance, the characteristic impedances of a triplate strip-line (a wire embedded in between two ground planes) and a semiconductor micro strip-line (wire above a semiconductor substrate) are approximated by Eq. (4.29) and Eq. (4.30), respectively.

$$Z_0(\text{triplate}) \approx 94\Omega \sqrt{\frac{\mu_r}{\varepsilon_r}} \ln\left(\frac{2t + W}{H + W}\right) \tag{4.29}$$

and

$$Z_0(\text{microstrip}) \approx 60\Omega \sqrt{\frac{\mu_r}{0.475\varepsilon_r + 0.67}} \ln\left(\frac{4t}{0.536W + 0.67H}\right) \tag{4.30}$$

Termination

The behavior of the transmission line is strongly influenced by the termination of the line. The termination determines how much of the wave is reflected upon arrival at the wire end. This is expressed by the *reflection coefficient* ρ that determines the relationship between the voltages and currents of the incident and reflected waveforms.

$$\rho = \frac{V_{refl}}{V_{inc}} = \frac{I_{refl}}{I_{inc}} = \frac{R - Z_0}{R + Z_o} \tag{4.31}$$

where R is the value of the termination resistance. The total voltages and currents at the termination end are the sum of incident and reflected waveforms.

$$\begin{aligned} V &= V_{inc}(1 + \rho) \\ I &= I_{inc}(1 - \rho) \end{aligned} \tag{4.32}$$

Three interesting cases can be distinguished, as illustrated in Figure 4.19. In case (a) the terminating resistance is equal to the characteristic impedance of the line. The termination appears as an infinite extension of the line, and no waveform is reflected. This is also demonstrated by the value of ρ, which equals 0. In case (b), the line termination is an open circuit ($R = \infty$), and $\rho = 1$. The total voltage waveform after reflection is twice the incident one as predicted by Eq. (4.32). Finally, in case (c) where the line termination is a short circuit, $R = 0$, and $\rho = -1$. The total voltage waveform after reflection equals zero.

The transient behavior of a complete transmission line can now be examined. It is influenced by the characteristic impedance of the line, the series impedance of the source Z_S, and the loading impedance Z_L at the destination end, as shown in Figure 4.20.

Consider first the case where the wire is open at the destination end, or $Z_L = \infty$, and $\rho_L = 1$. An incoming wave is completely reflected without phase reversal. Under the assumption that the source impedance is resistive, three possible scenarios are sketched in Figure 4.21: $R_S = 5\ Z_0$, $R_S = Z_0$, and $R_S = 1/5\ Z_0$.

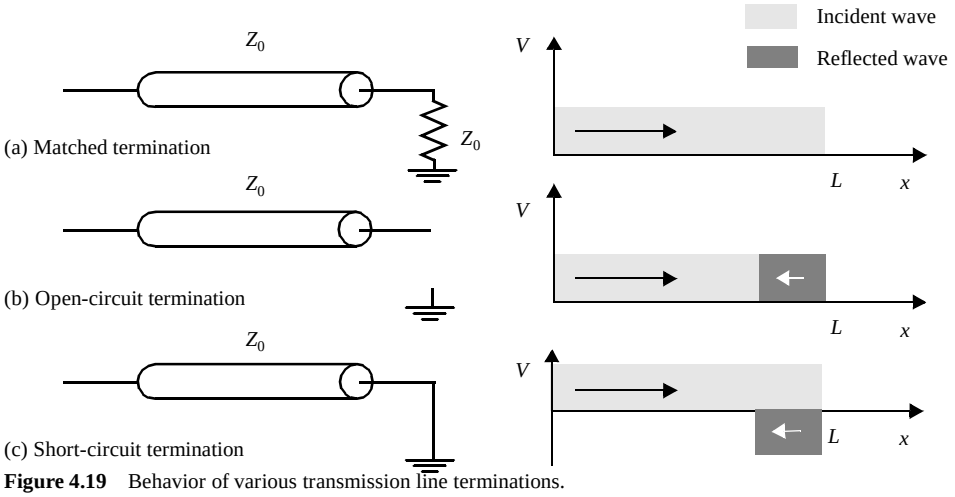


Figure 4.19 Behavior of various transmission line terminations.

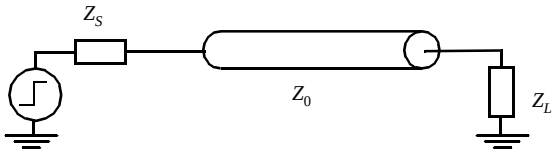


Figure 4.20 Transmission line with terminating impedances.

1. Large source resistance—$R_S = 5\ Z_0$ (Figure 4.21a)

Only a small fraction of the incoming signal V_{in} is injected into the transmission line. The amount injected is determined by the resistive divider formed by the source resistance and the characteristic impedance Z_0.

$$V_{source} = (Z_0 / (Z_0 + R_S))\ V_{in} = 1/6 \times 5\ \text{V} = 0.83\ \text{V} \tag{4.33}$$

This signal reaches the end of the line after L/v sec, where L stands for the length of the wire and is fully reflected, which effectively doubles the amplitude of the wave ($V_{dest} = 1.67$ V). The time it takes for the wave to propagate from one end of the wire to the other is called the *time-of-flight*, $t_{flight} = L/v$. Approximately the same happens when the wave reaches the source node again. The incident waveform is reflected with an amplitude determined by the source reflection coefficient, which equals 2/3 for this particular case.

$$\rho_S = \frac{5Z_0 - Z_0}{5Z_0 + Z_0} = \frac{2}{3} \tag{4.34}$$

The voltage amplitude at source and destination nodes gradually reaches its final value of V_{in}. The overall rise time is, however, many times L/v.

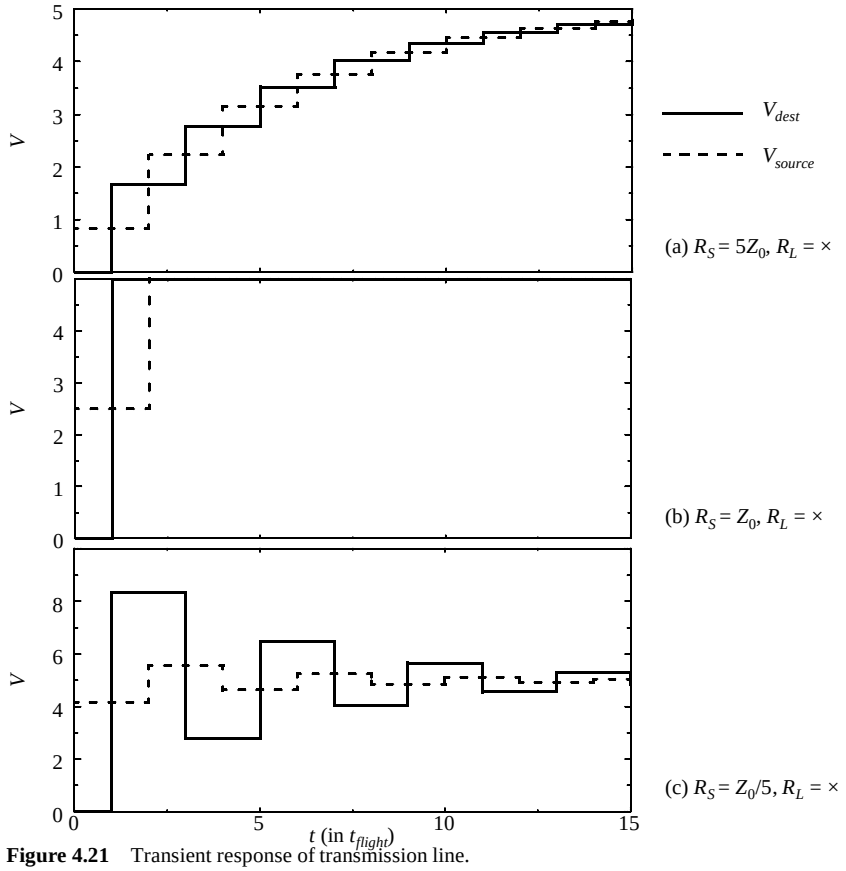


Figure 4.21 Transient response of transmission line.

When multiple reflections are present, as in the above case, keeping track of waves on the line and total voltage levels rapidly becomes cumbersome. Therefore a graphical construction called the *lattice diagram* is often used to keep track of the data (Figure 4.22). The diagram contains the values of the voltages at the source and destination ends, as well as the values of the incident and reflected wave forms. The line voltage at a termination point equals the sum of the previous voltage, the incident, and reflected waves.

2. Small source resistance—$R_S = Z_0/5$ (Figure 4.21c)

A large portion of the input is injected in the line. Its value is doubled at the destination end, which causes a severe overshoot. At the source end, the phase of the signal is reversed ($\rho_S = -2/3$). The signal bounces back and forth and exhibits severe ringing. It takes multiple L/v before it settles.

3. Matched source resistance—$R_S = Z_0$ (Figure 4.21b)

Half of the input signal is injected at the source. The reflection at the destination end doubles the signal, so that the final value is reached immediately. It is obvious that this is

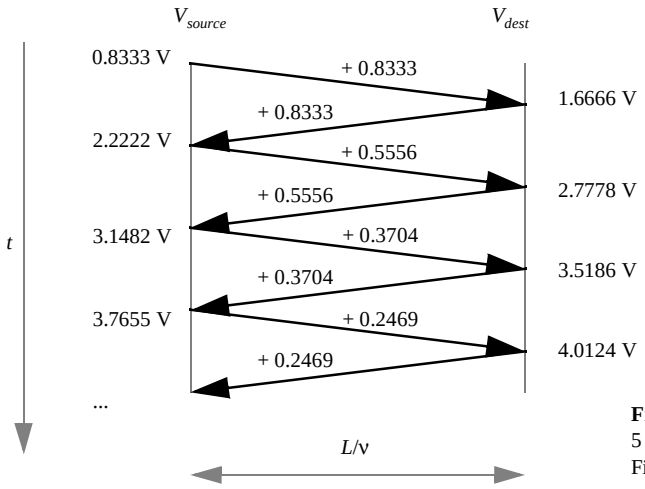


Figure 4.22 Lattice diagram for $R_S = 5\ Z_0$ and $R_L = \infty$. $V_{step} = 5$ V, (as in Figure 4.21a).

the most effective case. Matching the line impedance at the source end is called *series termination*.

Note that the above analysis is an ideal one, as it is assumed that the input signal has a zero rise time. In real conditions the signals are substantially smoother, as demonstrated in the simulated response of Figure 4.23 (for $R_S = Z_0/5$ and $t_r = t_{flight}$).

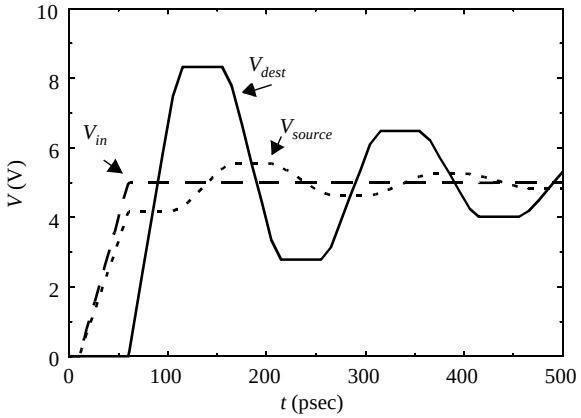


Figure 4.23 Simulated transient response of lossless transmission line for finite input rise times ($R_S = Z_0/5$, $t_r = t_{flight}$).

Problem 4.1 Transmission Line Response

Derive the lattice diagram of the above transmission line for $R_S = Z_0/5$, $R_L = \infty$, and $V_{step} = 5$ V. Also try the reverse picture—assume that the series resistance of the source equals zero, and consider different load impedances.

Similar considerations are valid when the termination is provided at the destination end, called *parallel termination*. Matching the load impedance to the characteristic impedance of the line once again results in the fastest response. This leads to the following conclusion.

To avoid potentially disastrous transmission line effects such as ringing or slow propagation delays, the transmission line should be terminated, either at the source (series termination), or at the destination (parallel termination) with a resistance equal to the characteristic impedance Z_0 of the transmission line.

Example 4.11 Capacitive Termination

Loads in MOS digital circuits tend to be of a capacitive nature. One might wonder how this influences the transmission line behavior and when the load capacitance should be taken into account.

The characteristic impedance of the transmission line determines the current that can be supplied to charge capacitive load C_L. From the load's point of the view, the line behaves as a resistance with value Z_0. The transient response at the capacitor node, therefore, displays a time constant Z_0C_L. This is illustrated in Figure 4.24, which shows the simulated transient response of a series-terminated transmission line with a characteristic impedance of 50 Ω loaded by a capacitance of 2 pF. The response shows how the output rises to its final value with a time-constant of 100 psec (= 50 Ω × 2 pF) after a delay equal to the time-of-flight of the line.

This asymptotic response causes some interesting artifacts. After 2 t_{flight}, an unexpected voltage dip occurs at the source node that can be explained as follows. Upon reaching the destination node, the incident wave is reflected. This reflected wave also approaches its final value asymptotically. Since V_{dest} equals 0 initially instead of the expected jump to 5 V, the reflection equals –2.5 V rather than the expected 2.5 V. This forces the transmission line temporarily to 0 V, as shown in the simulation. This effect gradually disappears as the output node converges to its final value.

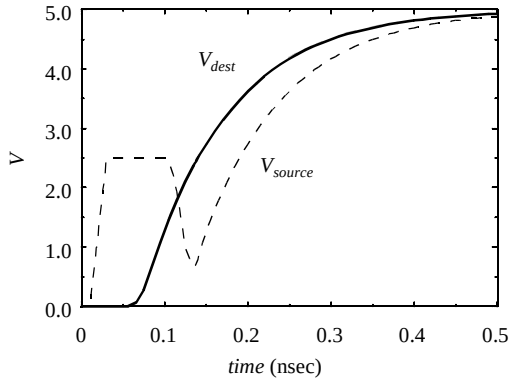


Figure 4.24 Capacitively terminated transmission line: R_S = 50 Ω, R_L = ∞, C_L = 2 pF, Z_0 = 50 Ω, t_{flight} = 50 psec.

The propagation delay of the line equals the sum of the time-of-flight of the line (= 50 psec) and the time it takes to charge the capacitance (= 0.69 Z_0 C_L = 69 psec). This is exactly what the simulation yields. In general, we can say that the capacitive load should only be considered in the analysis when its value is comparable to or larger than the total capacitance of the transmission line [Bakoglu90].

Lossy Transmission Line

While board and module wires are thick and wide enough to be treated as lossless transmission lines, the same is not entirely true for on-chip interconnect where the resistance of the wire is an important factor. The lossy transmission-line model should be applied instead. Going into detail about the behavior of a lossy line would lead us to far astray. We therefore only discuss the effects of resistive loss on the transmission line behavior in a qualitative fashion.

The response of a lossy *RLC line* to a unit step combines wave propagation with a diffusive component. This is demonstrated in Figure 4.25, which plots the response of the *RLC* transmission line as a function of distance from the source. The step input still propagates as a wave through the line. However, the amplitude of this traveling wave is attenuated along the line:

$$\frac{V_{step}(x)}{V_{step}(0)} = e^{-\frac{r}{2Z_0}x} \tag{4.35}$$

The arrival of the wave is followed by a diffusive relaxation to the steady-state value at point *x*. The farther it is from the source, the more the response resembles the behavior of a distributed *RC* line. In fact, the resistive effect becomes dominant, and the line behaves as a distributed *RC* line when R (= rL, the total resistance of the line) >> 2 Z_0. When $R = 5\ Z_0$, only 8% of the original step reaches the end of the line. At that point, the line is more appropriately modeled as a distributed *rc* line.

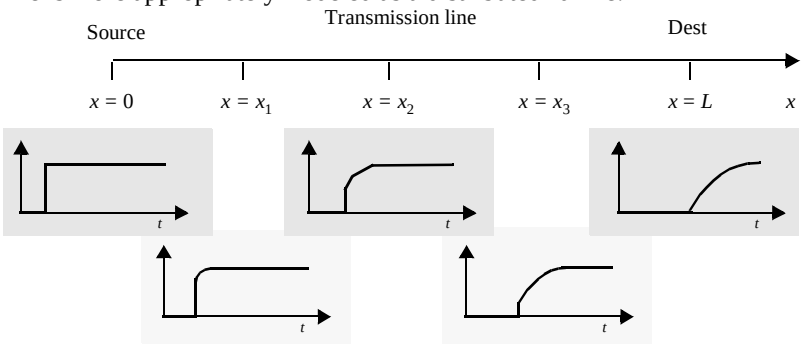


Figure 4.25 Step response of lossy transmission line.

Be aware that the actual wires on chips, boards, or substrates behave in a far more complex way than predicted by the above analysis. For instance, branches on wires, often called *transmission line taps,* cause extra reflections and can affect both signal shape and delay. Since the analysis of these effects is very involved, the only meaningful approach is to use computer analysis and simulation techniques. For a more extensive discussion of these effects, we would like to refer the reader to [Bakoglu90] and [Dally98].

Design Rules of Thumb

Once again, we have to ask ourselves the question when it is appropriate to consider transmission line effects. From the above discussion, we can derive two important constraints:

- **Transmission line effects should be considered when the rise or fall time of the input signal (t_r, t_f) is smaller than the time-of-flight of the transmission line (t_{flight}).**

This leads to the following rule of thumb, which determines when transmission line effects should be considered:

$$t_r(t_f) < 2.5t_{flight} = 2.5\frac{L}{n} \tag{4.36}$$

For on-chip wires with a maximum length of 1 cm, one should only worry about transmission line effects when t_r < 150 psec. At the board level, where wires can reach a length of up to 50 cm, we should account for the delay of the transmission line when t_r < 8 nsec. This condition is easily achieved with state-of-the-art processes and packaging technologies. Ignoring the inductive component of the propagation delay can easily result in overly optimistic delay predictions.

- **Transmission line effects should only be considered when the total resistance of the wire is limited:**

$$R < 5Z_0 \tag{4.37}$$

If this is not the case, the distributed RC model is more appropriate.
Both constraints can be summarized in the following set of bounds on the wire length:

$$\frac{t_r}{2.5}\frac{1}{\sqrt{lc}} < L < \frac{5}{r}\sqrt{\frac{l}{c}} \tag{4.38}$$

- **The transmission line is considered lossless when the total resistance is substantially smaller than the characteristic impedance, or**

$$R < \frac{Z_0}{2} \tag{4.39}$$

Example 4.12 When to Consider Transmission Line Effects

Consider again our Al1 wire. Using the data from Example 4.4 and Eq. (4.28), we can approximate the value of Z_0 for various wire widths:

W = 0.1 μm: c = 92 aF/μm; Z_0 = 74 Ω
W = 1.0 μm: c = 110 aF/μm; Z_0 = 60 Ω
W = 10 μm: c = 380 aF/μm; Z_0 = 17 Ω

Using tFor a wire with a width of 1μm, we can derive thech maximum length of the wire for which we should consider transmission line effects using Eq. (4.37):

$$L_{max} = \frac{5Z_0}{r} = \frac{5 \times 60\Omega}{0.075\Omega/\mu m} = 4000\mu m$$

From Eq. (4.36), we find a corresponding maximum rise (or fall) time of the input signal equal to

$$t_{rmax} = 2.5 \times (4000\ \mu m)/(15\ cm/nsec) = 67\ psec$$

This is hard to accomplish in current technologies. For these wires, a lumped capacitance model is more appropriate. Transmission line effects are more plausible in wider wires. For a 10 μm wide wire, we find a maximum length of 11.3 mm, which corresponds to a maximum rise time of 188 psec.

Assume now a Copper wire, implemented on level 5, with a characteristic impedance of 200 Ω and a resistance of 0.025 Ω/μm. The resulting maximum wire length equals 40 mm. Rise times smaller than 670 psec will cause transmission line effects to occur.

Be aware however that the values for Z_0, derived in this example, are only approximations. In actual designs, more complex expressions or empirical data should be used.

Example 4.13 Simulation of Transmission Line Effects

Show SPICE simulation

4.5 SPICE Wire Models

In previous sections, we have discussed the

4.5.1 Distributed *rc* Lines in SPICE

Because of the importance of the distributed *rc*-line in todays design, most circuit simulators have built-in distributed *rc*-models of high accuracy. For instance, the Berkeley SPICE3 simulator supports a uniform-distributed *rc*-line model (URC). This model approximates the *rc*-line as a network of lumped RC segments with internally generated nodes. Parameters include the length of the wire *L* and (optionally) the number of segments used in the model.

Example 4.14 SPICE3 URC Model

A typical example of a SPICE3 instantiation of a distributed rc-line is shown below. N1 and N2 represent the terminal nodes of the line, while N3 is the node the capacitances are connected to. RPERL and CPERL stand for the resistance and capacitance per meter.

```
U1 N1=1 N2=2 N3=0 URCMOD L=50m N=6
.MODEL URCMOD URC(RPERL=75K CPERL=100pF)
```

If your simulator does not support a distributed *rc*-model, or if the computational complexity of these models slows down your simulation too much, you can construct a simple yet accurate model yourself by approximating the distributed *rc* by a lumped *RC* network with a limited number of elements. Figure 4.26 shows some of these approximations ordered along increasing precision and complexity. The accuracy of the model is determined by the number of stages. For instance, the error of the π3 model is less than 3%, which is generally sufficient.

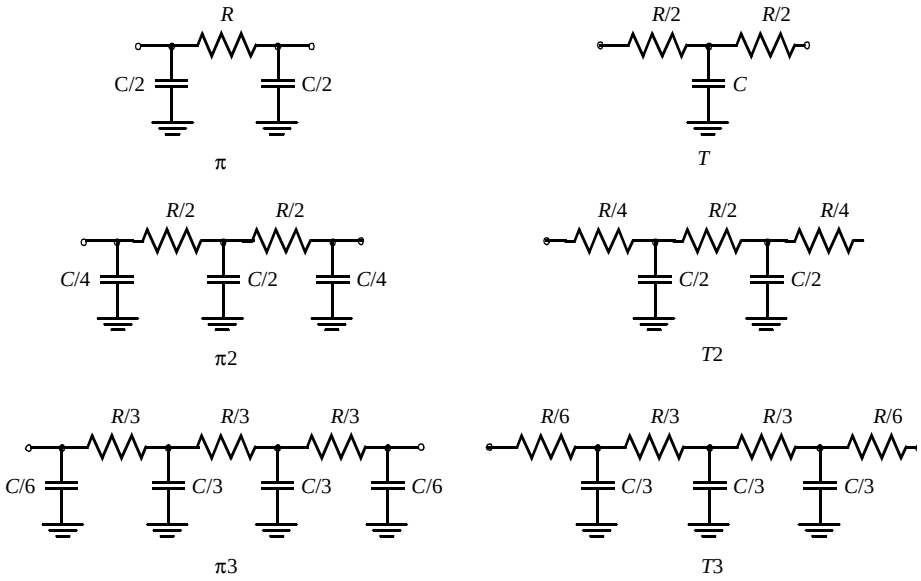


Figure 4.26 Simulation models for distributed *RC* line.

4.5.2 Transmission Line Models in SPICE

SPICE supports a lossless transmission line model. The line characteristics are defined by the characteristic impedance Z_0, while the length of the line can be defined in either of two forms. A first approach is to directly define the *transmission delay TD*, which is equivalent to the time-of-flight. Alternatively, a frequency *F* may be given together with *NL*, the dimensionless, normalized electrical length of the transmission line, which is measured with respect to the wavelength in the line at the frequency *F*. The following relation is valid.

$$NL = F \cdot TD \tag{4.40}$$

No lossy transmission line model is currently provided. When necessary, loss can be added by breaking up a long transmission line into shorter sections and adding a small series resistance in each section to model the transmission line loss. Be careful when using this approximation. First of all, the accuracy is still limited. Secondly, the simulation speed might be severely effected, since SPICE chooses a time step that is less than or equal to half of the value of *TD*. For small transmission lines, this time step might be much smaller than what is needed for transistor analysis.

4.6 Perspective: A Look into the Future

Similar to the approach we followed for the MOS transistor, it is worthwhile to explore how the wire parameters will evolve with further scaling of the technology. As transistor dimensions are reduced, the interconnect dimensions must also be reduced to take full advantage of the scaling process.

A straightforward approach is to scale all dimensions of the wire by the same factor *S* as the transistors (*ideal scaling*). This might not be possible for at least one dimension of the wire, being the length. It can be surmised that the length of *local interconnections* — wires that connect closely grouped transistors — scales in the same way as these transistors. On the other hand, *global interconnections*, that provide the connectivity between large modules and the input-output circuitry, display a different scaling behavior. Examples of such wires are clock signals, and data and instruction buses. Figure 4.27 contains a histogram showing the distribution of the wire lengths in an actual microprocessor design, containing approximately 90,000 gate) [Davis98]. While most of the wires tend to be only a couple of gate pitches long, a substantial number of them are much longer and can reach lengths up to 500 gate pitches.

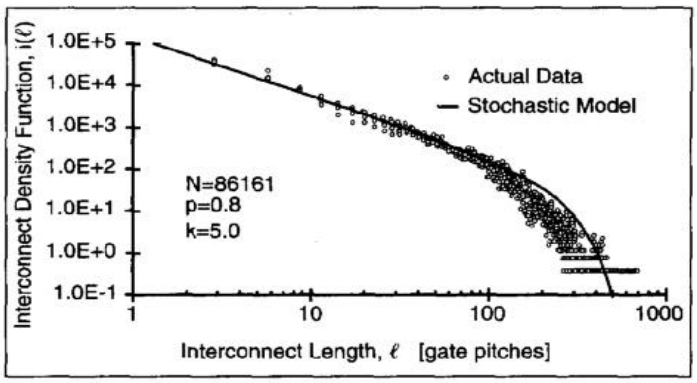


Figure 4.27 Distribution of wire lengths in an advanced microprocessor as a function of the gate pitch.

The average length of these long wires is proportional to the die size (or complexity) of the circuit. An interesting trend is that while transistor dimensions have continued to shrink over the last decades, the chip sizes have gradually increased. In fact, the size of the typical die (which is the square root of the die area) is increasing by 6% per year, doubling about every decade. Chips have scaled from 2 mm × 2 mm in the early 1960s to approximately 2 cm × 2 cm in 2000. They are projected to reach 4 cm on the side by 2010!

This argues that when studying the scaling behavior of the wire length, we have to differentiate between local and global wires. In our subsequent analysis, we will therefore consider three models: local wires ($S_L = S > 1$), constant length wires ($S_L = 1$), and global wires ($S_L = S_C < 1$).

Assume now that all other wire dimensions of the interconnect structure (W, H, t) scale with the technology factor S. This leads to the scaling behavior illustrated in Table 4.8. Be aware that this is only a first-order analysis, intended to look at overall trends. Effects such a fringing capacitance are ignored, and breakthroughs in semiconductor technology such as new interconnect and dielectric materials are also not considered.

Table 4.8 Ideal Scaling of Wire Properties

Parameter	Relation	Local Wire	Constant Lenght	Global Wire
W, H, t		*1/S*	*1/S*	*1/S*
L		*1/S*	1	$1/S_C$
C	*LW/t*	*1/S*	1	$1/S_C$
R	*L/WH*	*S*	S^2	S^2/S_C
CR	L^2/Ht	1	S^2	$S^2/S_C{}^2$

The eye-catching conclusion of this exercise is that scaling of the technology does not reduce wire delay (as personified by the *RC* time-constant). A constant delay is predicted for local wires, while the delay of the global wires goes up with 50% per year (for $S = 1.15$ and $S_C = 0.94$). This is in great contrast with the gate delay, which reduces from year to year. This explains why wire delays are starting to play a predominant role in todays digital integrated circuit design.

The ideal scaling approach clearly has problems, as it causes a rapid increase in wire resistance. This explains why other interconnect scaling techniques are attractive. One option is to scale the wire thickness at a different rate. The "constant resistance" model of Table 4.9 explores the impact of not scaling the wire thickness at all. While this approach seemingly has a positive impact on the performance, it causes the fringing and interwire capacitance components to come to the foreground. We therefore introduce an extra capacitance scaling factor ε_c (> 1), that captures the increasingly horizontal nature of the capacitance when wire widths and pitches are shrunk while the height is kept constant.

Table 4.9 "Constant Resistance" Scaling of Wire Properties

Parameter	Relation	Local Wire	Constant Lenght	Global Wire
W, t		1/*S*	1/*S*	1/*S*
H		1	1	1
L		1/*S*	1	$1/S_C$
C	$e_c LW/t$	e_c/S	e_c	e_c/S_C

Table 4.9 "Constant Resistance" Scaling of Wire Properties

Parameter	Relation	Local Wire	Constant Lenght	Global Wire
R	L/WH	1	S	S/S_C
CR	L^2/Ht	e_c/S	e_cS	e_cS/S_C^2

This scaling scenario offers a slightly more optimistic perspective, assuming of course that $\varepsilon_c < S$. Yet, delay is bound to increase substantially for intermediate and long wires, independent of the scaling scenario. To keep these delays from becoming excessive, interconnect technology has to be drastically improved. One option is to use better interconnect (Cu) and insulation materials (polymers and air). The other option is to differentiate between local and global wires. In the former, density and low-capacitance are crucial, while keeping the resistance under control is crucial in the latter. To address these conflicting demands, modern interconnect topologies combine a dense and thin wiring grid at the lower metal layers with fat, widely spaced wires at the higher levels, as is illustrated in Figure 4.28. Even with these advances, it is obvious that interconnect will play a dominant role in bothg high-performance and low-energy circuits for years to come.

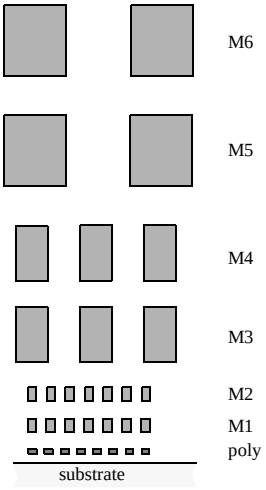


Figure 4.28 Interconnect hierarchy of 0.25 μm CMOS process, drawn to scale.

4.7 Summary

This chapter has presented a careful and in-depth analysis of the role and the behavior of the interconnect wire in modern semiconductor technology. The main goal is to identify the dominant parameters that set the values of the wire parasitics (being capacitance, resistance, and inductance), and to present adequate wire models that will aid us in the further analysis and optimization of complex digital circuits.

4.8 To Probe Further

Interconnect and its modeling is a hotly debated topic, that receives major attention in journals and conferences. A number of textbooks and reprint volumes have been published. [Bakoglu90], [Tewksbury94], and [Dally98] present an in-depth coverage of interconnect issues, and are a valuable resource for further browsing.

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4.9 Exercises and Design Problems