THEORETICAL ANALYSIS AND REDUCTION TECHNIQUES OF DC CAPACITOR RIPPLES AND REQUIREMENTS IN INVERTERS

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ABSTRACT

THEORETICAL ANALYSIS AND REDUCTION TECHNIQUES
OF DC CAPACITOR RIPPLES AND REQUIREMENTS IN INVERTERS

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DC link capacitor is an important component for many conventional topologies, such as three-phase voltage source inverter (VSI), H-bridge VSI and etc. However, it is usually very large, heavy and expensive. Therefore, minimization of the dc capacitor is an essential step towards developing and manufacturing compact low-cost inverter systems for high temperature operation, long life and high reliability. Traditionally, the dc capacitance has been determined according to empirical equations and computer simulations, which provides little insights into how to minimize the dc capacitor. In order to achieve an optimum minimization of the dc capacitor, an accurate theory to calculate the dc capacitor voltage ripple and current ripples must be developed first, then pulse-width modulation (PWM) and control techniques or topological improvements can be further developed to minimize both dc voltage and current ripples. This dissertation is mainly divided into two parts. First half is minimizing the capacitor ripple and requirements for three-phase VSI; while second half is for H-bridge VSI.

In the first half of the dissertation, it proposes an accurate theory of calculating the dc link capacitor voltage ripples and current ripples for inverters and PWM rectifiers. The results are analyzed and summarized into graphs according to the theory, which helps find the right capacitance value for a given voltage ripple tolerance and the rms ripple current that the capacitor has to absorb.

In hybrid electric vehicle (HEV) applications, the high voltage battery pack is connected to the dc link bus through a dc-dc converter. Based on the above-proposed theory, a PWM

modulation method for the dc-dc converter is developed to further reduce the dc capacitor current ripples and requirements. To verify the proposed theory and PWM method, a 150 kW inverter prototype has been built. The comparison between the calculation result and experimental result shows that they are in close agreement.

For the second half of the dissertation, contributions for H-bridge inverters are made for photovoltaic and FACTs systems.

As the demand of the renewable energy increases every year, the photovoltaic (PV) systems have been playing an important part in supplying energy for the global consumption. In order to connect PV modules to the grid without inserting any bulky low frequency step-up transformers, the cascaded H-bridge multilevel inverters are utilized to increase the output voltage level up to the grid voltage (e.g. 13.8 kV). The 2ω harmonic component on the dc link side of the H-bridge inverters has long been a thorny problem, which requires a huge dc link capacitor bank to absorb this 2ω low frequency current ripple in order to maintain the dc link voltage ripple under a tolerable value. This dissertation presents a simple 3^{rd} harmonic injection method for the cascaded H-bridge multilevel inverters for photovoltaic systems at unity power factor. This approach achieves a 40% to 50% reduction of the dc link capacitance, without adding any extra components or increasing the control complexity.

Same 2ω harmonic problem exists in FACTs devices, which is typically implemented by an H-bridge inverter. A new topology and control method are proposed to significantly reduce the dc capacitance to minimum by only adding a phase leg and an ac capacitor with the value of 1/10 of the original dc capacitance.

Dedicated to my Father and Mother:
Jiming Lu and Xuri Shen

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CHAPTER 1 DC Link Capacitors

DC link capacitors are used in intermediate circuit applications in power electronics e.g. power conversion technique, where different kinds of converters couples to one dc voltage level. Therefore, this kind of capacitors usually has to sustain high dc voltage which exists permanently and which is always accompanied by high frequency ripple voltages. The capacitors that can satisfy these requirements usually occupy a large space in the inverter, and they are also heavy and expensive. However, they commonly exist and play a very important role in most conventional topologies of power electronics, such as the three-phase voltage source inverter (VSI) and the single-phase VSI (or H-bridge VSI). These topologies are so matured in nowadays industry, and traditionally they cannot live without the dc link capacitors.

Therefore, minimization of the dc capacitor is an essential step towards developing and manufacturing compact low-cost inverter systems for high temperature operation, long life and high reliability.

Traditionally, the dc capacitance has been determined according to empirical equations and computer simulations, which provides little insights into how to minimize the dc capacitor. In order to achieve an optimum minimization of the dc capacitor, an accurate theory to calculate the dc capacitor voltage ripple and current ripples must be developed first, then pulse-width modulation (PWM) and control techniques or topological improvements can be further developed to minimize both dc voltage and current ripples.

This dissertation is mainly divided into two parts. First half is minimizing the capacitor ripple and requirements for three-phase VSI; while second half is for single-phase (H-bridge) VSI.

1.1 Types of DC Link Capacitors

Before going into details about how to minimize the dc link capacitors, let's take a look at those most common types of dc link capacitors.

In general, there are two types of capacitors are commonly used in the dc link. One is the electrolytic capacitor, and the other one is the film capacitor.

1.1.1 Electrolytic capacitor

Electrolytic capacitor for dc link usually looks similar to what are shown in Figure 1.1. It uses an electrolyte as one of its plates to achieve a larger capacitance per unit volume than other types. Due to this large capacitance, it makes it a very good candidate for low frequency filter and large energy storage. [1]

However, it also gets a lot of problems. It tends to have larger leakage current than other dry types of capacitors. In addition, the limitation on the operating temperatures keeps it away from high temperature applications. With the large parasitic resistance and inductance, it further limits its ripple current handle capability. Therefore, in some applications with high temperature and ripple currents, the electrolytic capacitors tend to have shorter life and less reliability.

(a)

(b)

Figure 1.1 Commercial electrolytic capacitors

Pictures are obtained from the below websites:

(a) http://theelectrostore.com/shopsite_sc/store/html/high-voltage-electrolytic-capacitors-400v-3900uf.html

(b) http://www.royalrrs.com/products/Capacitors/

1.1.2 Film capacitor

Film capacitors are made with an insulating plastic film as the dielectric, and combined with metallized aluminum or zinc as the electrodes. They are usually wound into cylindrical shape, with terminals attached on the sides, and then encapsulated. Some of them are look similar to what shown in Figure 1.2. [2, 3]

They are known of high current ripple handle ability, high operating temperature, very small equivalent series resistance and inductance. All these features make it a very good candidate for high switching frequency inverter/converters. However, the capacitance value tends to be smaller than the electrolytic capacitors. Additionally, the energy density is not as high as the electrolytic ones either.

(a)

(b)

Figure 1.2 Commercial film capacitors

Pictures are obtained from the below websites:

(a) https://encrypted-tbn3.gstatic.com/images?q=tbn:ANd9GcQs8-_8lP1VhCh90QQCjguK1HM-SqDLoc87_Hs_OZYvo4ZoWwaX

(b) http://www.sbelectronics.com/wp-content/uploads/2011/04/700D349_300_200.jpg

1.2 Comparisons

It is more straightforward to compare these two kinds of capacitors in a table shown in Table 1.1.

In conclusion, as the switching frequency goes higher, operating temperature goes higher, and the requirement of reliability goes up, it is more preferred to choose film capacitor rather than aluminum electrolytic capacitor.

Table 1.1 DC Link Capacitor Comparison between Film and Electrolytic [4]

Parameter	***Film***	***Aluminum Electrolytic***
Capacitance	Low	High
ESR	Low	High
Max operating temp	105 °C	85 °C
Max voltage	Larger than 1000 Vdc	600 Vdc
Ripple Current	High	Low
Life	Long	Short
Energy Density	Low	High
Failure mode	Fail open	rupture
Construction	Dry	Liquid electrolyte
Polarity	Non polar	Have polarity

1.3 Applications Using DC Link Capacitors and Outline of Dissertation

As mentioned previously, the dc link capacitors are needed in quite a lot of topologies, including those extremely matured ones, for example, the three-phase inverter and the single-phase inverter. These two topologies are going to be the focus of this dissertation.

1.3.1 Three-Phase Inverters

Figure 1.3 shows a typical three-phase inverter with a dc link capacitor shaded in the dashed box. This three-phase inverter has been widely used in the industry, for example, the hybrid electric vehicles (HEV), electric vehicles (EV) and so on.

In the first half of this dissertation, minimizing the dc link capacitance is focused on this three-phase inverter in HEV application, which is quite a hot topic in recent years.

Chapter 2 gives a general introduction and motivation of the first a few chapters (Chapter 3 to Chapter 7) on HEV applications, and introduces the limited work done in the past, which indicates more room for this dissertation to contribute.

Chapter 3 to Chapter 5 introduces the theoretical calculation of dc capacitance requirement and dc current ripple requirement for 3-phase inverter under SPWM, diode rectifier and 6-step operation method. This indicates the theoretical minimum value of dc capacitance. Chapter 6 shows the simulation, prototype and experimental results of a HEV system.

Chapter 7 proposes a new carrier modulation method to synchronize the dc-dc converter and SPWM inverter in the HEV systems to further minimize the dc link capacitor. It is cross checked with simulation and experimental results.

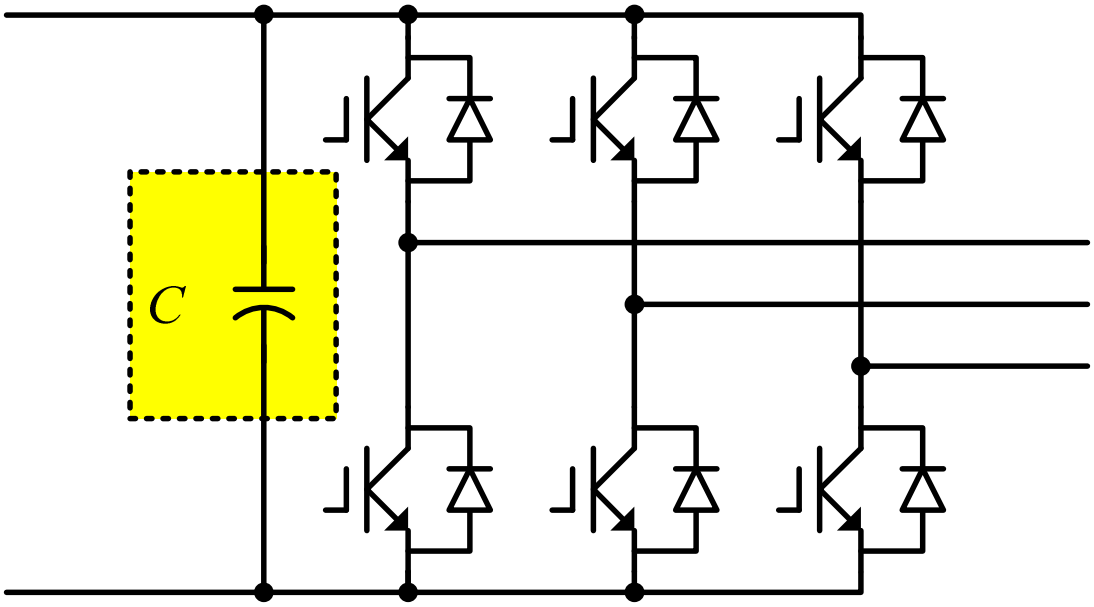


Figure 1.3 Typical three-phase inverter with dc link capacitor

1.3.2 Single-Phase Inverters

Figure 1.4 shows a typical single-phase (H-bridge) inverter with a dc link capacitor shaded in the dashed box. This single-phase inverter is also widely used in the industry for its matured technology and simple configuration and control.

There are quite a lot of applications. However, in this dissertation, the photovoltaic and the reactive power compensation is the focused application.

Chapter 8 proposes a 3rd harmonic injection for the photovoltaic system to reduce the dc link capacitor down to around 50%.

Chapter 9 proposes a new topology by adding an additional phase leg and a passive component to transfer the ripple energy to the auxiliary passive component, so as to reduce the dc link capacitor down to minimum.

And finally Chapter 10 is the contribution and future work.

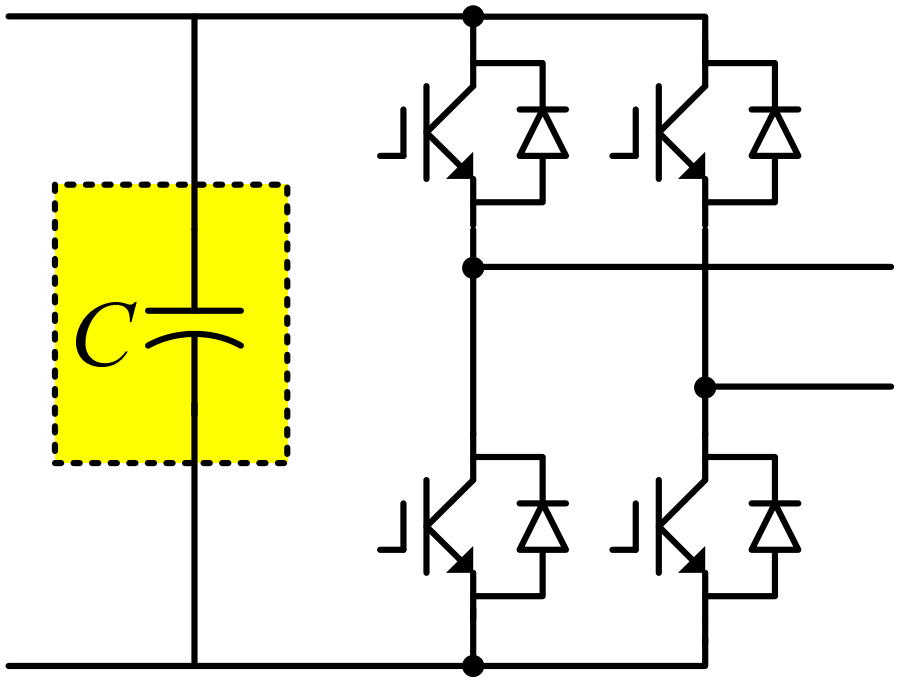


Figure 1.4 Typical single-phase inverter with dc link capacitor

CHAPTER 2 Introduction of HEV Applications and Their DC Capacitors

2.1 The Advantage of HEV in the Automotive Market

Emissions of CO_2 by human activities are currently amounting to about 27 billion tons per year [5]. The considerably high amount of CO_2 emission forces people to make every effort to minimize these emissions from the aspect of the human activities. Many excellent thoughts are considered, compared, analyzed, developed and finally built, tested and realized. One of these outstanding ideas, which protecting our mother earth from global warming and pollutions, is the development of hybrid electric vehicles (HEV), plug-in hybrid electric vehicles, and pure-electric vehicles. There are many worth reading websites and reviewed papers discussing the configurations of each kind and the comparison among them [6-8].

Nowadays, compared to the plug-in HEV and pure-electric vehicle, the HEV is the most popular and commercial type in the current automotive market. Similar to the ordinary vehicles, HEV possesses the power of fast acceleration and longer driving distance without the limitation of charging requirements.

The HEV system utilizes two different and independent energy sources, and hence, achieves a much higher fuel economy than the traditional vehicle with solely operated by the low-efficiency energy source—the internal combustion engine (ICE). Therefore, utilizing the HEV

can reduce the emissions of CO_2 and help clean the cities, at the same time save the limited energy resources for the world due to its higher efficiency (mile per gallon).

However, speaking to individuals, the cost of a HEV is still higher than the gas price that can be saved from it. Therefore, in order to impel more and more people to buy HEVs, the price needs to be further lowered down. That is why engineers have been doing researches on minimizing the cost, weight and size of the motors, generators, power electronics devices, and passive components in HEV systems during the past decades.

The work in this dissertation is mainly focusing on minimizing one of the biggest passive components in the HEV systems—the dc link capacitor, which leads to the ultimate goal of minimizing the cost, weight and size of the whole HEV systems.

2.2 Types of HEV Systems

Focus on HEVs, there are many different ways to classify HEV systems, and the general classification is to classify HEVs according to the way in which power is supplied to the drivetrain. Hence, there are three categories: series hybrid electric vehicles (SHEV), parallel hybrid electric vehicles (PHEV), and series-parallel hybrid electric vehicles (SPHEV). Generally speaking, the SHEV is used on heavy duty vehicles (buses, trucks etc.), while the PHEV is usually applied to light duty vehicles (family sedan etc.).

In order to illustrate the power electronics modules that located in the HEV, take the SHEV system as an example. The general power electronics function blocks in the commercial SHEV systems can be demonstrated similarly as Figure 2.1, which consists of an internal combustion engine (ICE), a generator/motor, a bidirectional pulse-width modulation (PWM) rectifier, a dc

link capacitor bank, a bidirectional inverter and a motor/generator. Additionally, instead of a high voltage battery, a low voltage battery with a smaller size is usually preferred and connected to the dc link through a dc-dc boost converter. For the sake of having the PWM rectifier, the inverter, and the dc-dc converter each at the same power rating, the system can have two smaller inverters controlling two traction motors respectively (shown in Figure 2.1) instead of only one inverter, whose power rating is the summation of the PWM rectifier's and the dc-dc converter's.

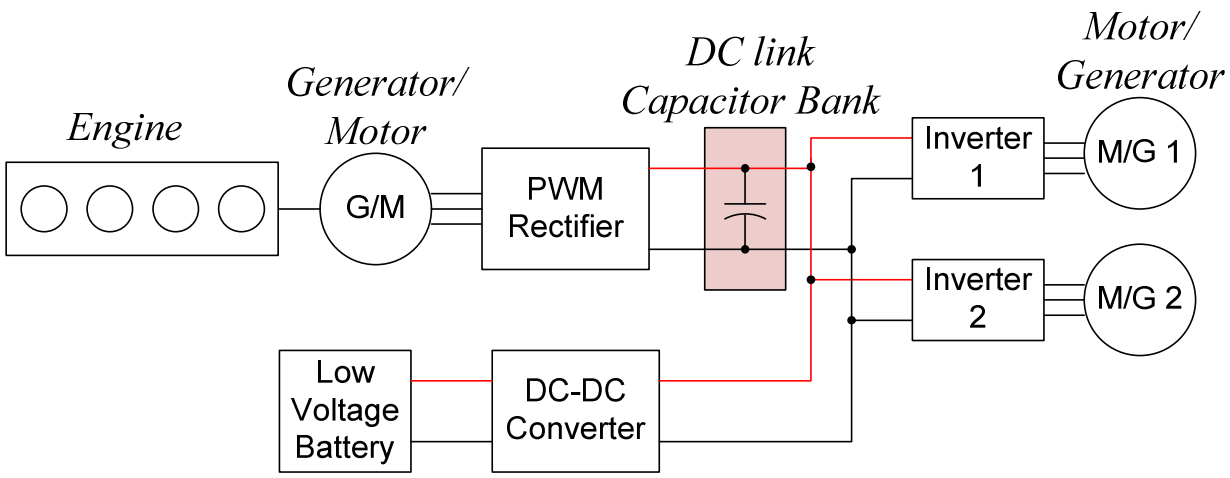


Figure 2.1 The power electronics function blocks of the series hybrid electric vehicle (SHEV) systems

2.3 Power Electronics Challenge in HEV systems

As shown in Figure 2.1, in a SHEV converter/inverter system, the dc link capacitor bank, shown in the shaded block, is usually bulky, heavy and expensive. The reason for this is that, this dc link capacitor bank needs to absorb all the current ripples generated by two inverters, the PWM rectifier, as well as the dc-dc converter. However, traditionally, this dc capacitance has been determined according to empirical equations and computer simulations, which provide little insight into how to minimize the dc link capacitance. Therefore, they are usually much bigger than needed, so that they occupy an unnecessarily large space. It is the biggest component in an

inverter box. As a result, minimization of the dc capacitance is an essential step towards developing and manufacturing compact, light, low-cost HEV converter/inverter systems for high temperature operation, long life and high reliability.

Therefore, in order to achieve an optimum minimization of the dc capacitor, an accurate theory to calculate the dc capacitor voltage and current ripple must be developed first, then PWM and control techniques can be further developed to minimize both dc voltage and current ripples.

2.4 Inverter Operation Modes in HEV

2.4.1 Sinusoidal Pulsewidth Modulation Mode

In the HEV converter/inverter systems, when the vehicle is at a relatively low speed, such as accelerating from a stop, battery is often chosen as the power supply, instead of the inefficient ICE. Plus, dc-dc converter is operated as a boost converter, to boost the low battery voltage to relatively high dc link voltage. Afterwards, the three-phase inverter used to drive the traction motor usually use sinusoidal pulse-width modulation (SPWM) mode. The SPWM mode can supply a smoothly increasing ac voltage to cooperate with the increasing speed, in order to ensure the maximum current and maximum torque. That comes from the *V/f* control. In this motoring situation, Figure 2.2 is the equivalent circuit.

Another important situation is when the generator/ICE started. In order to save the trouble of building another lower power rating starter and adding an additional 12-V battery, just utilizing the existed battery and the PWM rectifier instead could be a good choice. This requires the PWM rectifier works as an inverter at this time, which again Figure 2.2 is the equivalent circuit.

How about the regenerative modes? Regenerative mode happens at when the driver pushes

the brake pedal. At this time, the motor acts as a generator. The generated power is transferred through a three-phase PWM inverter (PWM rectifier mode in this case) and a dc-dc converter, and stored this power in the battery. By doing so, instead of wasting the energy to heat up the brakes or bleeding resistors, the energy is stored and can be reused later on. This results in energy saving, and high efficiency. Since the motor/generator is operating as a generator, the three-phase PWM inverter should operate as a PWM rectifier accordingly to convert the power from ac to dc. Although it sounds so different, the PWM rectifier is actually the same as the SPWM inverter. Therefore, in the regenerative mode, as the brake pedal is being pushed and the speed is decreasing, the PWM rectifier is operated by SPWM, which again Figure 2.2 is considered.

And of course, when the energy comes from ICE/generator side to the dc link side, the PWM rectifier is working as a PWM rectifier. Therefore, it is again Figure 2.2.

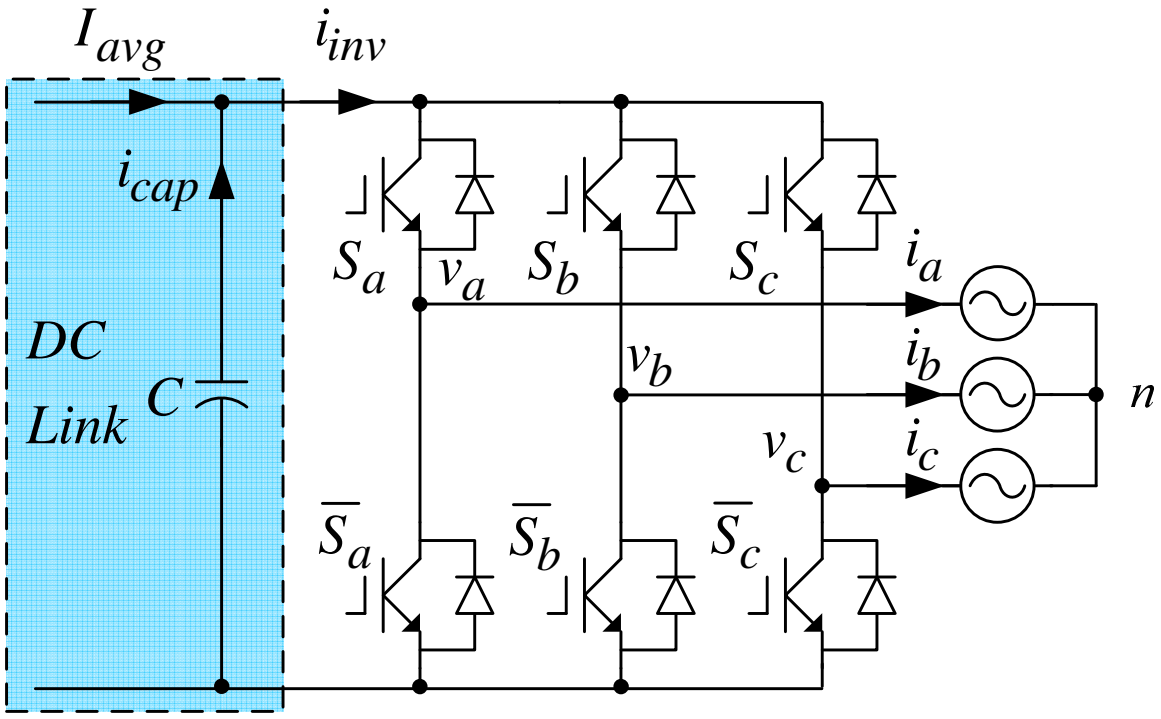


Figure 2.2 The schematic of a three-phase inverter/PWM rectifier using SPWM with three-phase current sources as load

2.4.2 Six-Step Mode

After the acceleration, the vehicle reaches at a much higher speed. This requires the inverter to output a higher voltage. In this case, six-step operation is often used, due to its higher dc voltage utilization. This is demonstrated in Figure 2.3. The only difference from the SPWM operation mode is that, for six-step operation, when the vehicle goes to higher speed, the back electromotive force (EMF) can no longer be ignored, that is what happened with those added voltage sources at the load side in Figure 2.3.

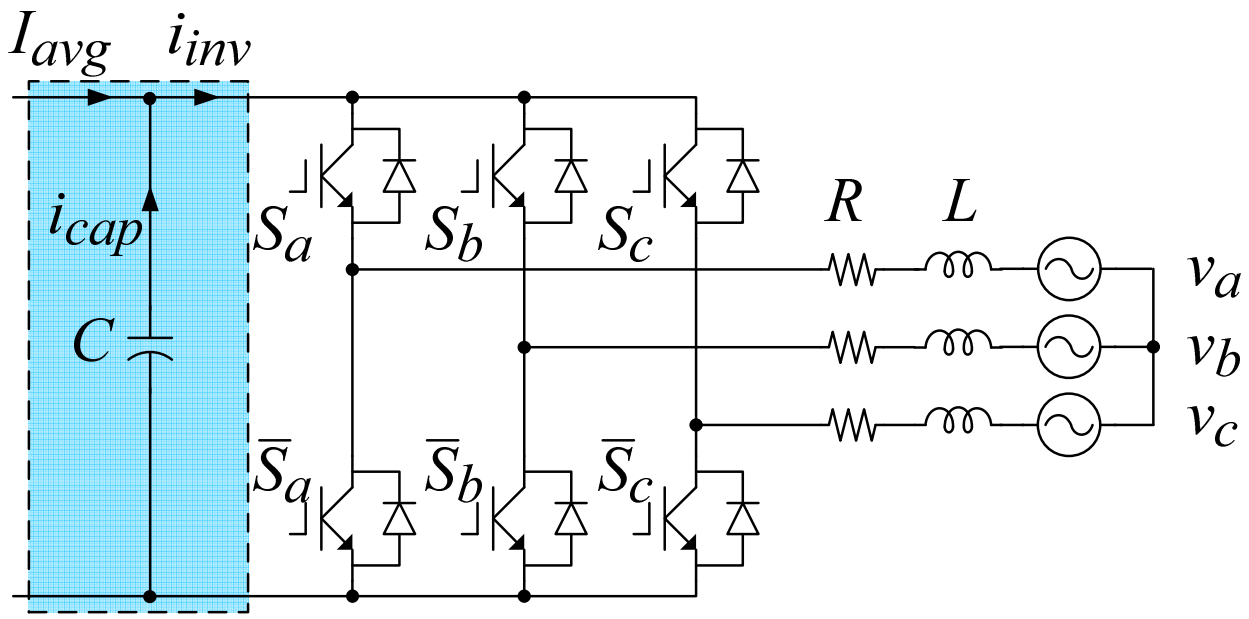


Figure 2.3 The simplified equivalent circuit of the inverter under six-step operation

2.4.3 Diode Rectifier Mode

The last mode is diode rectifier mode. For the PWM rectifier, if all the power switches switch off, and only the freewheeling diodes forced on and off the input voltages, the PWM rectifier becomes an uncontrolled diode rectifier, as shown in Figure 2.4.

If considered PHEV, there is no PWM rectifier connecting the generator/motor to the dc link. However, if considered SHEV, there is a PWM rectifier connecting the generator/motor to the dc link, which at most time rectifies the three-phase ac voltages generated by the generator/motor to dc voltage. As you may notice, this PWM rectifier can work as an uncontrolled diode rectifier, like Figure 2.4.

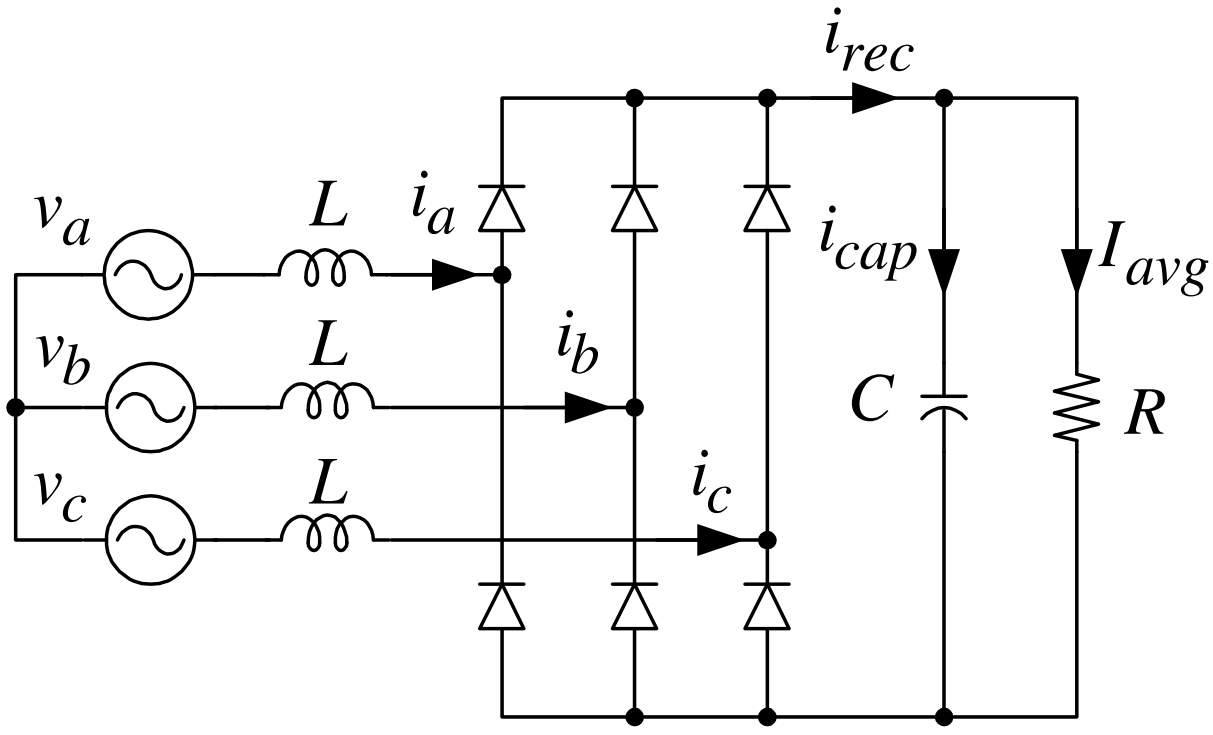


Figure 2.4 The schematic of a three-phase uncontrolled diode rectifier with line impedance on the ac side, and with dc link capacitor and resistive load on the dc side

2.4.4 Synchronization between DC-DC Converter and SPWM Inverter

One last converter that have not been mentioned above is the dc-dc converter that connects the battery—the energy storage system—to the dc link. Therefore, this dc-dc converter contributes a certain amount of current harmonics to the dc link capacitor as well, which results in voltage ripples on the dc link. Consequently, in order to minimize the dc capacitance of the HEV systems, this part should be considered as well, which shows in Figure 2.5.

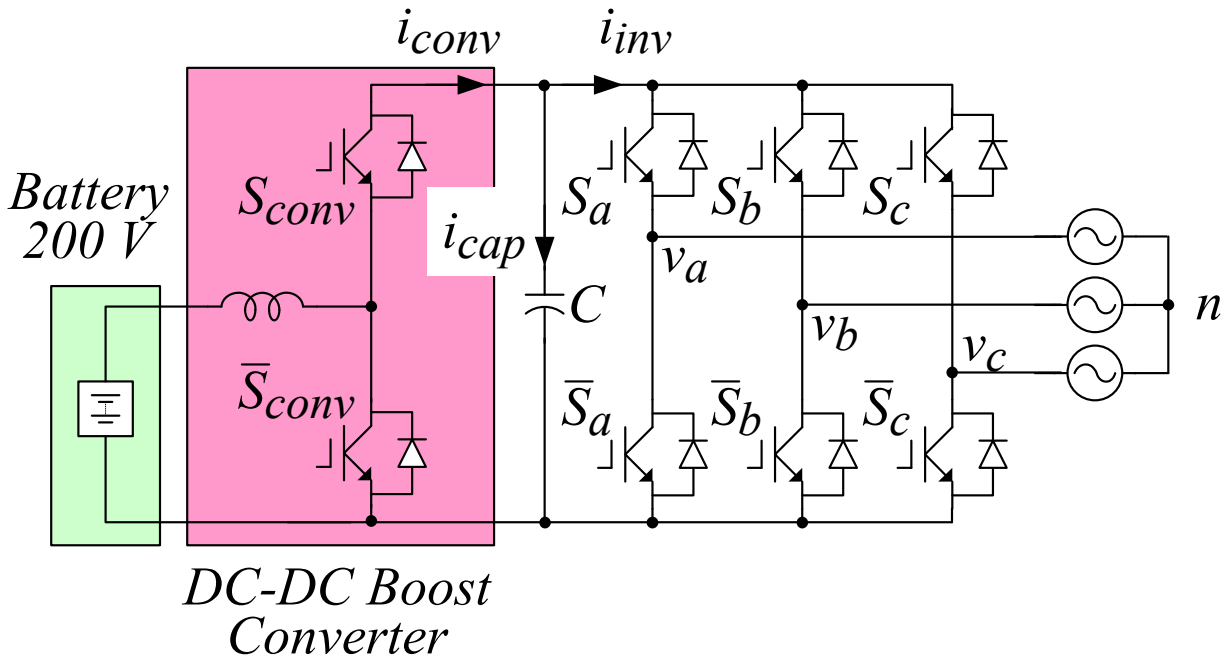


Figure 2.5 The schematic of a bidirectional dc-dc converter connected with a three-phase inverter with three-phase current sources as load

In conclusion, rectifiers and inverters, operated by SPWM and six-step mode, as well as the uncontrolled diode rectifier and dc-dc converter, are discussed in this thesis. Graphs, which show the right capacitance value for a given voltage ripple tolerance, are summarized at the end of each chapter.

2.5 Summary of Previous Work

2.5.1 Complicated AC-DC-AC PWM Converter Control Strategies

One of the typical AC-DC-AC PWM converters (sometimes called AC-AC converter) is shown in Figure 2.6. There are many papers discussing control strategies to reduce ripple current going through the dc link capacitor *C* by making the converter side dc link current the same as the inverter side dc link current, which theoretically needs no capacitance at all. For instance, direct capacitor current control [9], direct instantaneous input/output power balancing [10, 11], four-step commutation strategy [12], space vector modulation strategy [13], output current linearization feedback control (input/output current tracking) [14, 15], nonlinear control [16-18], and some other methods utilizing the current information. Also, there are a large number of papers discussing the matric converter or indirect matrix converter without dc link capacitor [19-21]. Similarly, they are all proposed with complicated close-loop control. However, there are few papers which discuss accurately obtaining the theoretical minimum capacitance for HEV systems by calculating the current ripple going through the dc link capacitor and voltage ripple across the dc link capacitor under open loop condition.

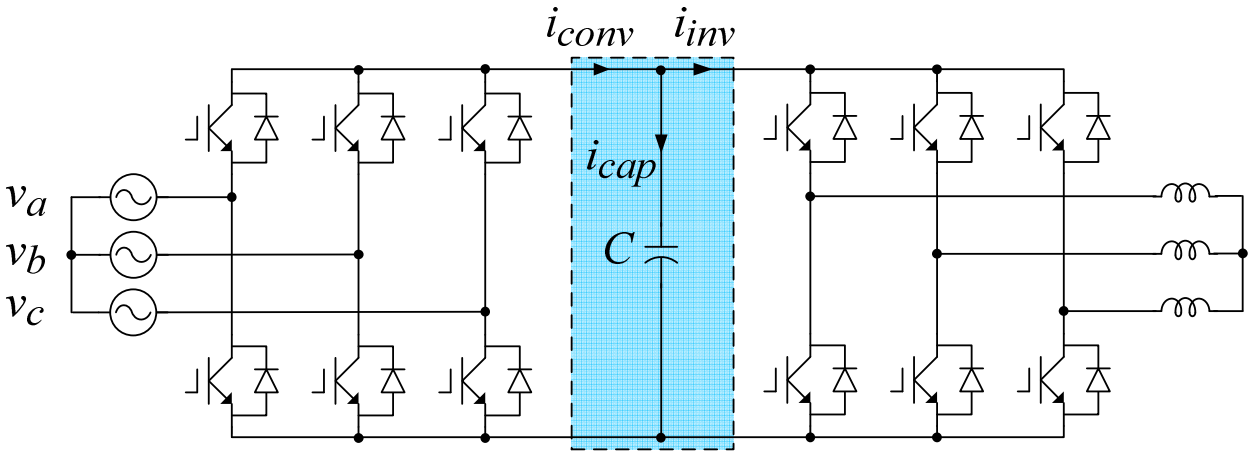


Figure 2.6 The schematic of a typical AC-DC-AC PWM converter system

2.5.2 Theoretical Analysis of Current Ripples and Harmonics of DC Capacitor

Some studies have been done on current ripple and harmonics of the dc link capacitor. For example, [22] is a very good paper about the rms current stress on the dc link capacitor for voltage source inverter (VSI) systems. In addition, [23, 24] are both on the topic of dc link current harmonics analysis. [25] is closer to the designer's viewpoint, but no closed-form equations of current ripple and capacitance value is derived. [26] did not give a theoretical calculation either. These papers provide a theoretical basis of the current ripple and harmonics. However, there are few papers talking about the voltage ripple and harmonics of the dc link capacitor. Also, there are few papers analyzed the current and voltage ripples through the Ampere-Second point of view, which is actually the source of the voltage ripple.

2.5.3 Simple Synchronization between DC-DC converter and SPWM Inverter to Minimize Capacitance

In the HEV converter/inverter system, inverters are always connected to dc-dc converters, for the sake of boosting the battery's low dc voltage to high dc voltage, and then converting into ac voltage to drive the traction motors, as shown in Figure 2.5. However, the dc link capacitor bank between the dc-dc converter and the inverter is usually bulky, heavy and expensive. Yet the bottleneck of the capacitor's size is determined by the current ripple requirement rather than the voltage ripple requirement. Hence, a better way to minimize the dc capacitance is narrowed down to minimize the current ripple through the capacitor by synchronizing the dc-dc converter and the SPWM inverter. The PWM and control techniques are fairly important. A good way will help minimizing the capacitance, whereas an unsuccessful one may need more capacitance than the normal operation.

Similar to the condition described in [9], in order to minimize the dc link capacitance between the dc-dc converter and SPWM inverter, making the converter side dc link current i_{conv} equals to the inverter side dc link current i_{inv} in a pulsewidth modulation (PWM) converter-inverter system is the final destination, so that ideally no current will flow through the dc link capacitor and no voltage fluctuation will be across the capacitor, meaning no capacitor needed at all. Till now, most papers that discussed the current ripple reduction and the dc link capacitance minimization are based on the AC-DC-AC PWM converter-inverter systems with relatively complicated close-loop control methods [9-11, 14, 27-29]. The best result that they can achieve is almost without any dc link capacitors. Besides, there are papers discussing innovating PWM strategies only on inverter side allowing reduction of the dc input current ripples [30-32]. Furthermore, for DC-DC-AC PWM converter [33]. However, very few papers have been written

focusing on the current ripple reduction by synchronizing between the DC-DC converter and the SPWM inverter, the so-called DC-DC-AC PWM converters, which is also commonly existed in the HEV systems. [34] was a good start for the synchronization by making the DC-DC converter's switching frequency twice as much as the inverter's switching frequency and optimizing the phase difference of the carrier waveforms between the inverter carrier and DC-DC carrier. This method does decrease the current ripple quite a lot. In spite of this, more improvement can be done.

2.6 Goal and Methodology

When designing a voltage source inverter, the dc link capacitor is an important parameter to the designer. It is always preferred to know the capacitance's per unit value if given a percentage of the tolerable dc link voltage ripple. As a result, once we get a curve showing the relationship between the per unit value of the dc link capacitor and the desired voltage ripple percentage of the dc link, as well as taking consideration of a certain value of power factor, we can easily find out the capacitance by only checking the curve and then multiplying the capacitance base value. This makes life much easier. In conclusion, our task is to find the curve mentioned above, which shows the relationship between the per unit value of the capacitance and the dc link voltage ripple percentage.

For the sake of calculating the capacitance, (2.1) is the basic equation that comes up to one's mind, which express the current going through a capacitor, i_{cap}, is equal to the capacitance, C, times the derivative of the voltage across this capacitor, v_{cap}.

$$i_{cap} = C\frac{dv_{cap}}{dt} \tag{2.1}$$

Extract the capacitance C out of (2.1), one can get (2.2).

$$C = \frac{i_{cap} \cdot dt}{dv_{cap}} \tag{2.2}$$

Let's take a closer look at (2.2), the numerator is $i_{cap} \cdot dt$, which is a current times a time interval. From now on, it will be called "Ampere-Second", short as $A \cdot sec$, in this thesis. Moreover, the denominator dv_{cap}, is actually the dc link voltage ripple, due to the assumption that this thesis is only dealing with dc link capacitance calculation.

For the sake of deriving the dc link capacitance, according to (2.2) obtaining an accurate expression, for the $i_{cap} \cdot dt$ —Ampere-Second ($A \cdot sec$)—of the ac ripple current i_{cap} that is flowing in and out of the dc link capacitor during one switching cycle, is the key point to get the required dc capacitance per unit (p.u.) value, of a given tolerable voltage ripple value, such as 10%.

Based on the previous discussion about the necessity and importance of finding the minimum dc capacitance for the HEV system, and the previous work that have done by others, here comes the outline of thesis.

Picking a dc link capacitor is decided by two constrains: one is the capacitance which is determined by the voltage ripple; the other one is the rms current ripple across the capacitor for the worst case, which will cause the capacitor internal temperature rise and has to be under a certain value to ensure the proper operation of the ordinary capacitors. Therefore, each chapter will be divided into basically two parts:

1. Calculation of the capacitance with a certain requirement of the voltage ripple endurance;

2. Calculation of the rms current ripple.

Voltage ripple is more directly related to the capacitance, as one can see from (2.3). Therefore, in order to get the minimum capacitance for the system, $i_{cap} \cdot dt$ (Ampere-Second) should be obtained first.

$$C = \frac{i_{cap} \cdot dt}{dv_{cap}} = \frac{i_{cap} \cdot dt}{\varepsilon V_{dc}} \tag{2.3}$$

These calculations have to be done for 3 different topologies that exists in the HEV systems: SPWM inverter (motoring low speed), 6-step inverter (motoring high speed), and diode rectifier (the PWM rectifier without controlling the switches).

In the following a few chapters, an accurate theory of calculating the voltage ripples and current ripples of the inverters and converters in HEV systems is presented, respectively. The topologies shown in Figure 2.2 (a) three-phase inverter/PWM rectifier, Figure 2.4 a three-phase uncontrolled diode rectifier, and Figure 2.5 a dc-dc converter, are mainly discussed in these chapters, which are the basic modules for a hybrid electric vehicle, both SHEV and PHEV. The voltage and current ripples of these cases are analyzed and summarized into graphs, which helps one to find the right capacitance value for a given voltage ripple tolerance and the rms ripple current that the capacitor has to absorb. Experiments are demonstrated with 510 μF of dc link capacitance for a 150 kVA inverter, and the results verify the derived expressions.

CHAPTER 3 DC Capacitance and Current Ripple Requirement of the Three-Phase SPWM Inverter/PWM Rectifier

Chapter 2 gives a general idea of why we need to minimize the dc link capacitor for HEV converter/inverter systems, and four topologies that are going to be discussed in this thesis. In this chapter, the objective is to find the requirement of the dc link capacitance and the current ripple for a three-phase SPWM inverter or a three-phase PWM rectifier. In fact, in terms of influence to the dc link capacitor voltage and current ripple, these two topologies are inherently the same. Therefore, only one needs to be analyzed, and the detailed analysis in this chapter is based on SPWM inverter [35].

In order to make the conclusions more general and convenient for other designers to apply to their own applications, the results of the dc link capacitance requirement are analyzed and summarized into graphs at the end of this chapter according to the proposed accurate theory. The conclusive graphs can help to find the right capacitance value for a given voltage ripple tolerance and the rms current ripple that the capacitor has to absorb for different power factors.

Finally, this chapter ends up with the experimental results from a 150 kVA inverter prototype, which proves the calculation result and experimental result are in close agreement.

First of all, let's start from the first topology in Figure 2.2—the three-phase SPWM inverter/rectifier. (For convenience, Figure 2.2 is redrawn here as Figure 3.1 on the next page.)

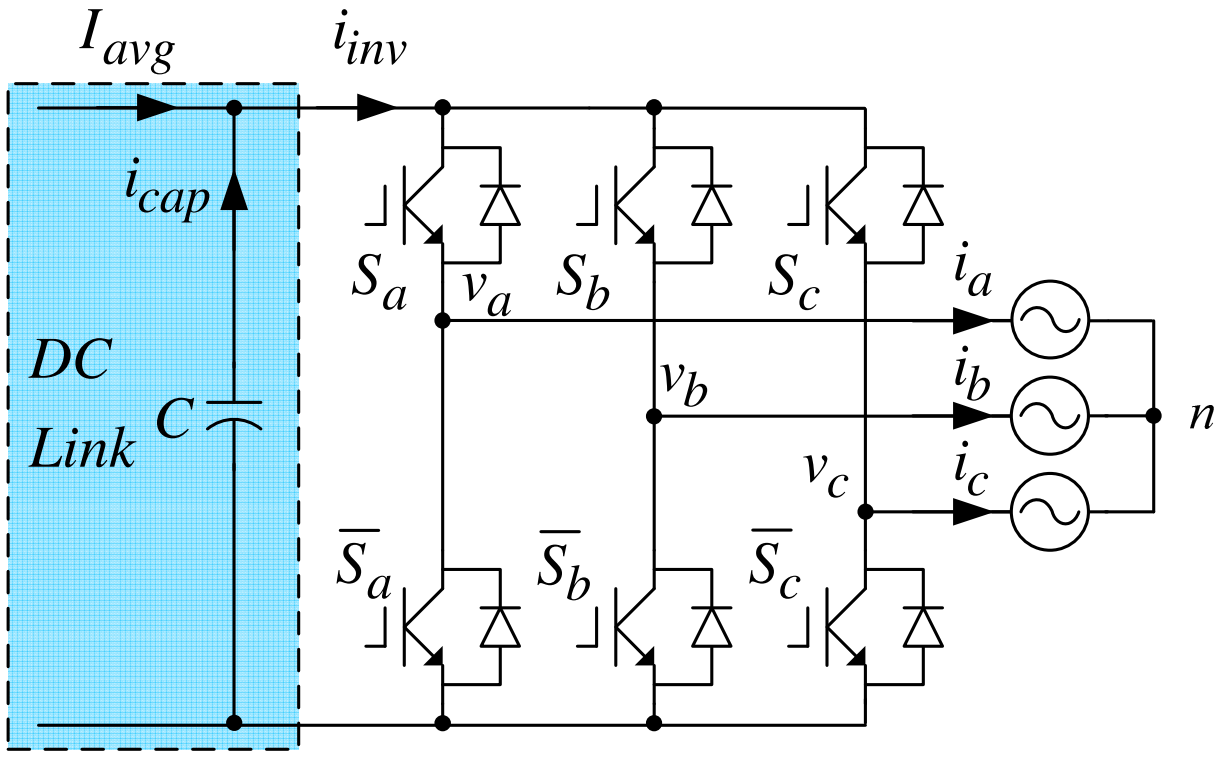


Figure 3.1 The schematic of a three-phase inverter/PWM rectifier using SPWM with three-phase current sources as load

3.1 Basic Idea of Calculating DC Link Capacitance

As mentioned in Chapter 2, for the sake of calculating the capacitance, (3.1) is the basic equation that comes up to one's mind, which express the current going through a capacitor, i_{cap}, is equal to the capacitance, *C*, times the derivative of the voltage across this capacitor, v_{cap}.

$$i_{cap} = C\frac{dv_{cap}}{dt} \tag{3.1}$$

Extract the capacitance *C* out of (3.1), one can get (3.2).

$$C = \frac{i_{cap} \cdot dt}{dv_{cap}} \tag{3.2}$$

In (3.2), the denominator, voltage ripple across the capacitor, dv_{cap}, is usually known for a design. In general, the smaller the capacitance is, the bigger the voltage ripple is. As a result, the bigger the voltage ripple on the dc link, the more harmonics goes to the ac side load. However, we want both small capacitor and low harmonics to the load. Obviously, there is a tradeoff between the two. This tradeoff is determined by the designer's target. Hence, this voltage ripple factor is considered a constant in the followed calculation.

Therefore, according to (3.2) and explanation in the above paragraph, the required dc capacitance *C* is proportional to the numerator, $i_{cap} \cdot dt$, which is called Ampere-Second ($A \cdot sec$) in the later paragraphs.

In conclusion, an accurate expression for the minimum required dc link capacitance can be obtained by finding an accurate $A \cdot sec$ expression of the ac ripple current i_{cap}, where i_{cap} represents the current going in and out of the dc link capacitor.

As explained above, the most challenging part of this calculation is to find an expression for $A \cdot sec$. This is achieved by integrating the positive/negative part of i_{cap} in one switching period. Obviously, if i_{cap} is integrated during one switching cycle, the result is zero because the dc link capacitor does not have a dc current offset, otherwise the dc link voltage will keep increasing and finally blow up the capacitor. That is why integrating the whole switching cycle does not help. Therefore, integrating either positive or negative part is the target.

3.2 Theoretical Basis

Figure 3.1 shows the schematic of a three-phase SPWM inverter/PWM rectifier with dc link capacitor and three-phase load/current source. Let's take a close look at this figure. First of all, it is desired to decompose the ideal inverter input current i_{inv} into two parts.

- A constant dc current I_{avg} is assumed to be supplied by a dc current source, which does not introduce any other current ripples. It can be imagined as a diode rectifier in series with a huge inductor. Although this does not really exist in the HEV system nowadays, the purpose of this assumption is eliminating all current ripples that coming from other sources, but only focusing on the current ripples that come from the SPWM inverter side, as shown in Figure 3.1.
- As one may already know, the other part of the ideal inverter input current i_{inv} is the ac ripple current i_{cap}, which flows in and out of the dc link capacitor bank, whose average is zero in every switching cycle and of course every fundamental cycle as well.

Therefore, I_{avg} is equal to the average of i_{inv}.

3.2.1 Switching Functions

First of all, assume the rms value of the inverter output line-to-line voltage is V_{ac}, the 3rd harmonic injection is $v_{3\omega}$ (the same to all three phases), the fundamental frequency in radian is

ω, the rms value of the inverter output line current is I_{ac}, the modulation index is *M*, and the power factor angle is ϕ.

The inverter three-phase output voltages v_{an}, v_{bn} and v_{cn} in Figure 3.1 can be expressed as shown in (3.3). Understand that the inverter three-phase output voltages are PWM waveforms. Equation (3.3) only shows their fundamental components. That is why they are sinusoidal expressions, without the summation of any higher order of sine terms.

$$\begin{aligned} v_{an} &= \frac{\sqrt{2}}{\sqrt{3}} V_{ac} \sin(\omega t) + v_{3\omega} \\ v_{bn} &= \frac{\sqrt{2}}{\sqrt{3}} V_{ac} \sin(\omega t - \frac{2}{3}\pi) + v_{3\omega} \\ v_{cn} &= \frac{\sqrt{2}}{\sqrt{3}} V_{ac} \sin(\omega t + \frac{2}{3}\pi) + v_{3\omega} \end{aligned} \tag{3.3}$$

Secondly, the inverter three-phase output currents i_a, i_b and i_c are all perfect sinusoidal currents. For one thing, it is relatively reasonable because the traction motors are usually equivalent to huge inductors, which are enough to smooth out most of the ripples. For another thing, similar as previous explanation, it is desired to eliminate all the other ripples influence, and only focus on the ripples that generated by the SPWM operation method.

Similarly, the inverter output three phase currents i_a, i_b and i_c can be expressed as shown in (3.4), where they are assumed to be perfect sinusoidal currents.

$$\begin{aligned} i_a &= \sqrt{2} I_{ac} \sin(\omega t - \phi) \\ i_b &= \sqrt{2} I_{ac} \sin(\omega t - \phi - \frac{2}{3}\pi) \\ i_c &= \sqrt{2} I_{ac} \sin(\omega t - \phi + \frac{2}{3}\pi) \end{aligned} \tag{3.4}$$

From Figure 3.2 and the proof in the Appendix, the switching functions of the three upper switches S_a, S_b and S_c are obtained in (3.5).

$$\begin{aligned} S_a &= \frac{1}{2} + \frac{1}{2} M \sin \omega t + \frac{v_{3\omega}}{V_{dc}} \\ S_b &= \frac{1}{2} + \frac{1}{2} M \sin(\omega t - \frac{2}{3}\pi) + \frac{v_{3\omega}}{V_{dc}} \\ S_c &= \frac{1}{2} + \frac{1}{2} M \sin(\omega t + \frac{2}{3}\pi) + \frac{v_{3\omega}}{V_{dc}} \end{aligned} \tag{3.5}$$

3.2.2 Relationship between *Vdc* and *Vac*

Please note that the dc link voltage has a relationship with the ac output line-to-line voltage as shown in (3.6), under both normal modulation and over modulation, which means $M \in [0, 1.15]$.

$$M \frac{V_{dc}}{2} = \frac{\sqrt{2}}{\sqrt{3}} V_{ac} \tag{3.6}$$

3.2.3 Average Current

The input real power of the inverter on the dc side can be expressed as (3.7).

$$P_{dc} = V_{dc} I_{avg} \tag{3.7}$$

The output real power of the inverter on the ac side can be expressed as (3.8).

$$P_{ac} = \sqrt{3} V_{ac} I_{ac} \cos \phi \tag{3.8}$$

The efficiency of the inverter is usually above 90%. This means the power loss is relatively small comparing to the total power. Therefore, if the power loss in the inverter is ignored, the input real power is equal to the output real power, as shown in (3.10).

$$V_{dc} I_{avg} = \sqrt{3} V_{ac} I_{ac} \cos\phi \tag{3.9}$$

Put I_{avg} on one side of the equation, and others on the other side. Equation (3.10) can be obtained.

$$I_{avg} = \sqrt{3} \frac{V_{ac}}{V_{dc}} I_{ac} \cos\phi \tag{3.10}$$

Hence, substituting (3.6) into (3.10), the average current (3.11) is obtained.

$$I_{avg} = \frac{3\sqrt{2}M}{4} I_{ac} \cos\phi \tag{3.11}$$

Similarly, the average current expression (3.11) can be achieved by substituting (3.4) and (3.5) into (3.12) as well, which means the switching functions shown in (3.5) are actually indicating the average duty cycle in each switching cycle.

$$I_{avg} = S_a i_a + S_b i_b + S_c i_c \tag{3.12}$$

3.3 Calculation of Required DC Link Capacitance

Figure 3.2 shows the PWM switching details during two switching cycles. Figure 3.2 (b) (c) (d) shows the switching functions of three phases determined by the traditional SPWM strategy, whose duty cycle in each switching period can be calculated from (3.5). In addition, Figure 3.2 (e) is the ideal inverter input current i_{inv}. As it is assumed the inverter is fed by a constant current source of I_{avg}, it can be understood that the current waveform that is flowing in and out of the dc link capacitor bank, i_{cap}, is the waveform in (e), but with I_{avg} as the x-axis instead of 0.

Instead of looking at the whole 360°, it is the same to analyze only 60°, for the reason that the waveforms are repeated in a low frequency at 6ω due to the three-phase system. Therefore, the following analysis will only focus on the range of 30° to 90° (take v_a as a reference), where $v_a > v_c > v_b$, drawed in pink (or shaded area) in Figure 3.3.

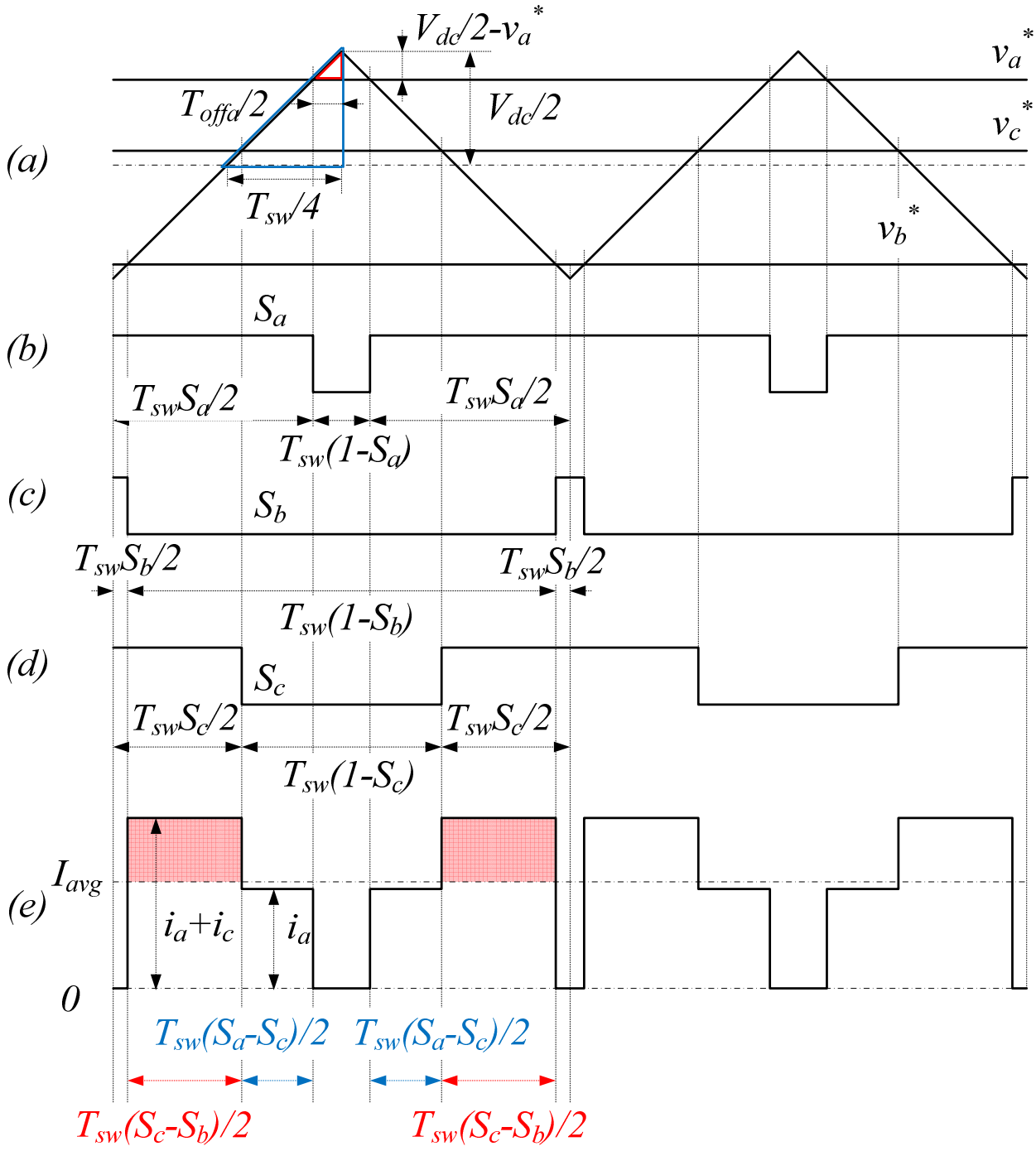


Figure 3.2 Detailed PWM waveforms in two switching periods
(a) sinusoidal reference and triangle carrier waveforms;
(b) switching function of phase A;
(c) switching function of phase B;
(d) switching function of phase C;
(e) ideal inverter input current i_{inv} with I_{avg} showing in the same graph.

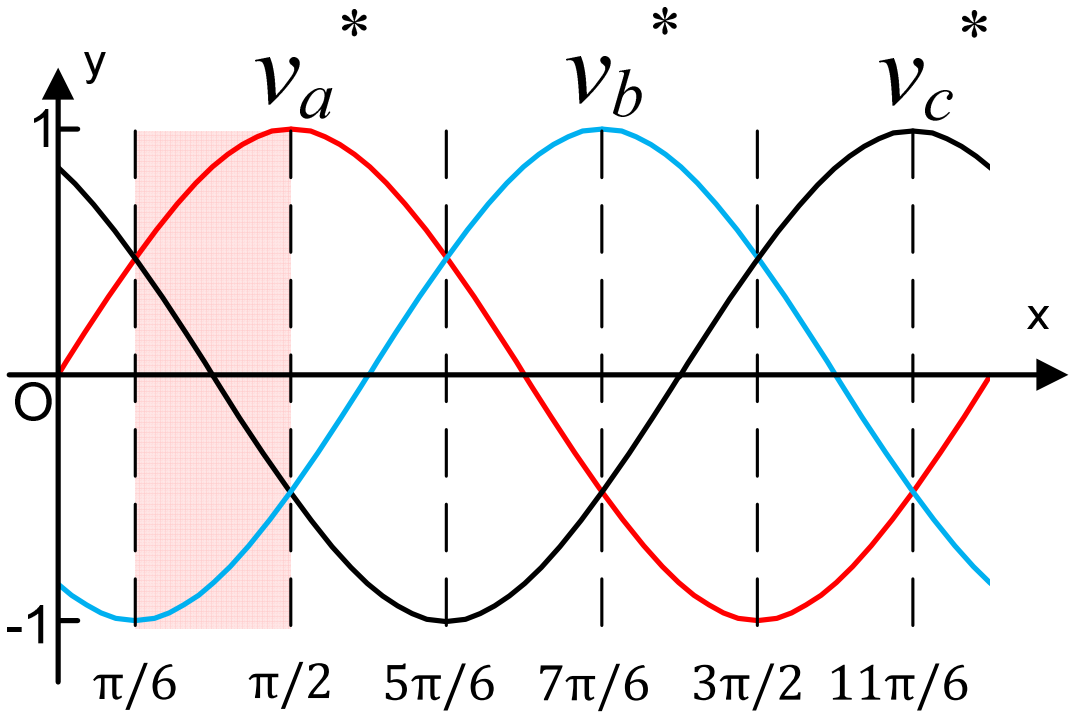


Figure 3.3 Six sectors for voltage references of phase A, B and C

From Figure 3.2(e), it is obvious to calculate $A \cdot sec$ by integrating the positive/negative half of i_{cap} during one switching period. If using the positive half, the expression for the area of the shaded blocks will be

$$A \cdot sec = T_{sw}(S_c - S_b)(i_a + i_c - I_{avg}) \tag{3.13}$$

By substituting (3.4), (3.5) and (3.11) into (3.13), we can get (3.14).

$$A \cdot sec = \frac{\sqrt{6}}{2} I_{ac} T_{sw} M \cos(\omega t)\left[\sin(\omega t - \phi + \frac{\pi}{3}) - \frac{3}{4} M \cos\phi\right] \tag{3.14}$$

As one can tell from (3.11), I_{avg} is related to power factor (pf) and modulation index (M). Therefore, if either of the two decreases, I_{avg} will decrease, which leads to the equation expressing the $A \cdot sec$ to be different, due to different blocks are involved into (3.13).

Here is the conclusion: during this 60°, $A \cdot sec$ is actually a piecewise function related to M, pf, rms line current, switching frequency and instantaneous time. For example, if it is assumed M=1 when pf=1, there are three expressions for $A \cdot sec$ listed in Table 3.1. The expression of $A \cdot sec$ is basically changing with the I_{avg} value level, depending on whether it is bigger or smaller than i_a or $i_a + i_c$. As mentioned before, pf can change the I_{avg} value, therefore the expression of Asec changes with pf. As pf decreases from unity to zero, the number of Asec expressions decreases from three to one as well, such as:

- pf=1, it has all three Asec expressions;
- pf=0.866, it has the first two Asec expressions;
- pf=0, it only has the first Asec expression;

Similarly, as M can modify the I_{avg} value as well, the expression of $A \cdot sec$ changes with M as expected. However, no matter what the condition is, the expression of $A \cdot sec$ will not come out from these three expressions.

Table 3.1 Expressions of $A \cdot sec$ ($v_a > v_c > v_b$)

Range	$A \cdot sec$	No.
$i_a < I_{avg} < i_a + i_c$	$T_{sw}(S_c - S_b)(i_a + i_c - I_{avg})$	Expression 1
$I_{avg} < i_a < i_a + i_c$ $I_{avg} < i_a + i_c < i_a$	$T_{sw}\left[(S_c - S_b)(i_a + i_c - I_{avg}) + (S_a - S_c)(i_a - I_{avg})\right]$ $= T_{sw}(1 - S_a + S_b) I_{avg}$	Expression 2
$i_a + i_c < I_{avg} < i_a$	$T_{sw}(S_a - S_c)(i_a - I_{avg})$	Expression 3

In conclusion, expression 1 will be effective for any pf and *M*. Expression 2 and expression 3 are only valid for pf=1 with any *M*. Table 3.2 shows the simplified expressions of $A \cdot sec$ by substituting (3.4) and (3.5) into Table 3.1.

Table 3.2 Simplified Expressions of $A \cdot sec$ ($v_a > v_c > v_b$)

Range	$A \cdot sec$	No.
$i_a < I_{avg} < i_a + i_c$	$\frac{\sqrt{6}}{2} I_{ac} T_{sw} MI \cos(\omega t) \left[\sin(\omega t - \phi + \frac{\pi}{3}) - \frac{3}{4} MI \cos\phi \right]$	Expression 1
$I_{avg} < i_a < i_a + i_c$ $I_{avg} < i_a + i_c < i_a$	$\frac{\sqrt{6}}{2} I_{ac} T_{sw} MI \cos\phi \left[\frac{\sqrt{3}}{2} - \frac{3}{4} MI \sin(\omega t + \frac{\pi}{6}) \right]$	Expression 2
$i_a + i_c < I_{avg} < i_a$	$\frac{\sqrt{6}}{2} I_{ac} T_{sw} MI \cos(\omega t + \frac{\pi}{3}) \left[\frac{3}{4} MI \cos\phi - \sin(\omega t - \phi) \right]$	Expression 3

3.3.1 Maximum $A \cdot sec$ during 60° with the Same Power Factor and Modulation Index

When pf=0, expression 1 becomes (3.15).

$$A \cdot sec = \frac{\sqrt{6}}{2} I_{ac} T_{sw} M \cos(\omega t) \sin(\omega t - \frac{\pi}{6}) \tag{3.15}$$

The maximum Asec during 60°, with the same pf and *M*, can be found by taking the partial derivative of (3.15) with respect to ωt.

Assume (3.16) to make things easier.

$$k = \sqrt{2} I_{ac} T_{sw} \tag{3.16}$$

The derivative can be expressed as (3.17).

$$\frac{d}{d\omega t} A \cdot sec = kM \cos(2\omega t - \frac{\pi}{6}) \tag{3.17}$$

Therefore, within the appropriate range of ωt, equation (3.18) can be derived. $m=1$ and $\omega t=\pi/3$ will give $A \cdot sec$ maximum value, where m is an integer in (3.18).

$$\omega t = m\frac{\pi}{2} - \frac{\pi}{6} = \frac{\pi}{3} \tag{3.18}$$

Put (3.18) back into (3.15),

$$A\sec = \frac{1}{4}\frac{\sqrt{3}}{2} kM \tag{3.19}$$

Equation (3.19) is drawn as the red line in Figure 3.5 by varying M from 0 to 1. If it is assumed that the base $A \cdot sec$ is (3.20), $A \cdot sec$ max can be derived in a per unit form as (3.21).

$$A \cdot sec_{base} = \sqrt{2} I_{ac} T_{sw} \tag{3.20}$$

$$A \cdot sec_{\max\ p.u.} = \frac{1}{4}\frac{\sqrt{3}}{2} M \tag{3.21}$$

Since Table 3.2 expression 2 is valid for pf=1, it is easier than Table 3.2 expression 1 to manipulate. In expression 2, please note that the term, that has ωt, has a negative sign in front, which will yield the minimum instead.

In this case, observation is necessary. For the expression 2, finding the minimum of sine will give a maximum value. $\omega t=\pi/6$ or $\pi/2$ will give the maximum Asec value.

The expression becomes (3.22).

$$A\sec_{\max} = \frac{\sqrt{6}}{2} I_{ac} T_{sw} M \cos\phi \left[\frac{\sqrt{3}}{2} - \frac{3}{4} M \sin(\frac{\pi}{3}) \right] \tag{3.22}$$

With (3.20), $A \cdot sec$ p.u. is obtained in (3.23).

$$A \cdot sec_{\max\ p.u.} = \frac{\sqrt{3}}{2} M \cos\phi \left[\frac{\sqrt{3}}{2} - \frac{3}{4} M \sin(\frac{\pi}{3}) \right] \tag{3.23}$$

In conclusion, the maximum Asec, standing for voltage ripple, can be expressed in (3.21) when pf=0 and in (3.23) when pf=1.

Similarly, the other power factors can be analyzed in the same way. However, it is a little bit harder to find the roots than the two shown here, since they will become a 4^{th} order polynomials.

Nevertheless, MATLAB can be used to achieve these solutions. Figure 3.4 shows the flowchart of calculating one point on Figure 3.5, such as on the pf=*u* line with M=*x*.

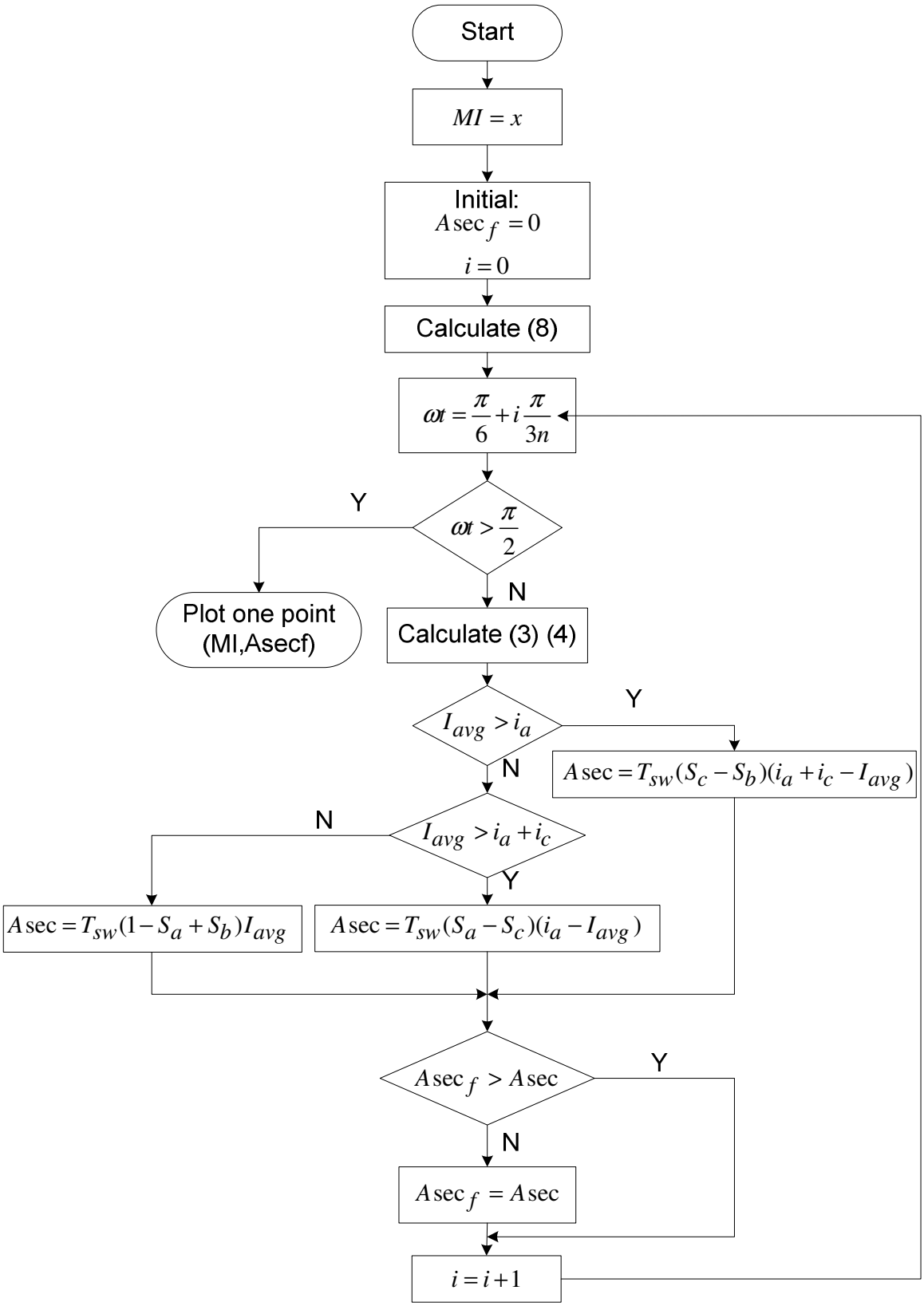


Figure 3.4 The flowchart of calculating the maximum Asec during 60° at a certain value of MI and pf

In the flowchart, n is the number of the switching cycles in 60° of the fundamental cycle, shown in (3.24).

$$n = \frac{f_{sw}}{f_{ref}} \tag{3.24}$$

f_{sw} is the switching frequency and f_{ref} is the fundamental frequency.

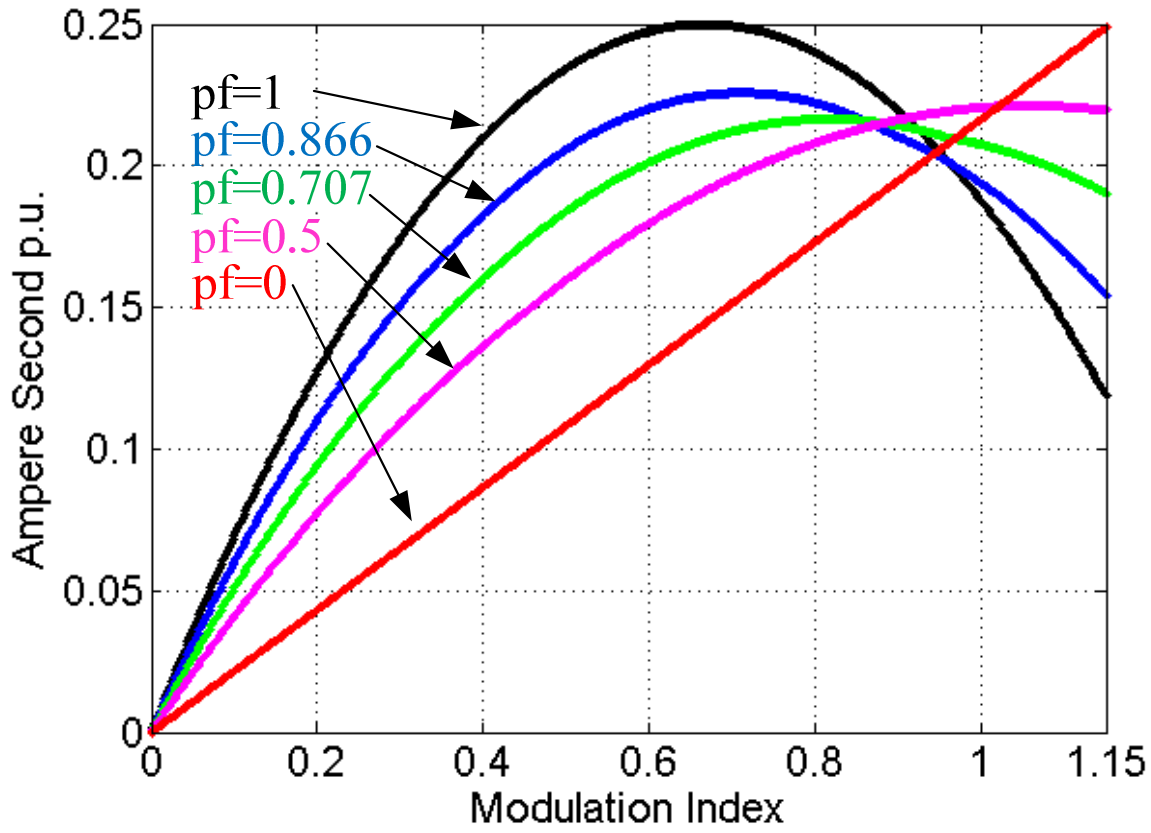


Figure 3.5 The relationship between Modulation Index (M) and Ampere Second ($A \cdot sec$)

Therefore, by varying M and pf, Figure 3.5 is obtained, which shows the relationship between the $A \cdot sec$ and modulation index by varying the pf from 0 to 1.

Please note that the three expressions shown in Table 3.1 possess a "$S_i - S_j$" term, so $v_{3\omega}$ in (3.5) disappears in the *A·sec* expression, meaning the voltage ripple will not be influenced by the 3rd harmonic injection. This happens to the current ripple as well, as one can see from section 2.4.

3.3.2 Maximum *A·sec* versus Power Factor

The maximum Asec at different power factor points must be determined, since it is necessary to consider the worst case when selecting capacitance values. For instance, this can be achieved by taking the partial derivative of (3.21) and (3.23) with respect to *M* for pf=0 and pf=1 respectively. Therefore, when pf=0 and *M*=1.15, *A·sec* reaches its maximum, while when pf=1, (3.25) is achieved.

$$\cos\phi - \frac{3}{2} M \cos\phi = 0 \tag{3.25}$$

If pf=$\cos\phi$=1, *M*=2/3 will give the maximum *A·sec*, which can be noticed in Figure 3.5 as well.

Finally, in order to get the per unit value of the desired capacitance, it is necessary to define the capacitance base formula. For the sake of eliminating the power rating of the inverter, C_{base} can be defined as (3.26).

$$C_{base} = \frac{\sqrt{3} I_{ac}}{2\pi f V_{ac}} \tag{3.26}$$

Considering V_{dc} is always constant, while V_{ac} is varied with frequency by changing the MI, C_{base} can be expressed using V_{dc} instead by substituting (3.6) into (3.26). Eq.(3.27) is obtained.

$$C_{base} = \frac{\sqrt{2} I_{ac}}{\pi f V_{dc} M} \tag{3.27}$$

In order to calculate (3.27), one has to find the maximum point for each pf on Figure 3.5 and record the specific M for that maximum point, as Table 3.3 shows.

Table 3.3 The M at the maximum *A·sec* for each pf

pf	**M**
1.000	0.667
0.866	0.744
0.707	0.816
0.500	1.150
0.000	1.150

Assume is Δv_{dc} the tolerable voltage ripple that the system requires, and ε is the voltage ripple percentage. The capacitance can be calculated through (3.28).

$$C = \frac{A\sec_{\max}}{\Delta v_{dc}} = \frac{A\sec_{\max}}{\varepsilon \cdot V_{dc}} \tag{3.28}$$

Therefore, the per unit value of the capacitance can be expressed as (3.29).

$$C_{p.u.} = \frac{f_{ref} A\sec_{\max}}{\sqrt{2} I_{ac}} \frac{\pi M}{\varepsilon} \tag{3.29}$$

Figure 3.6 shows the relationship between the per unit value of the desired capacitance $C_{p.u.}$ and a given DC link voltage ripple requirement ε.

Please note that Figure 3.6 is under the condition of switching at 5 kHz and having a fundamental frequency at 200 Hz because the experiment is under this condition and will be easier to compare later on.

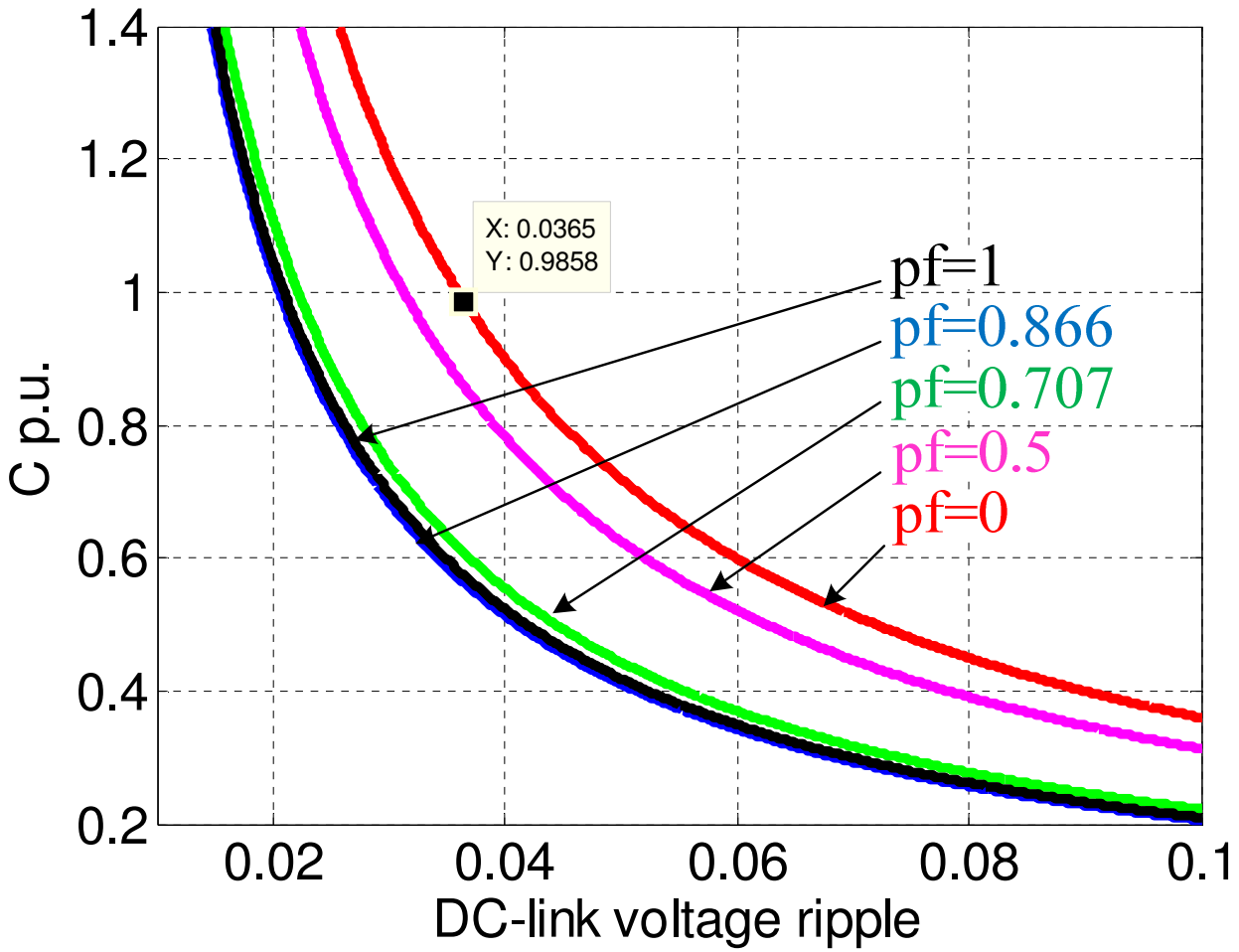


Figure 3.6 The relationship between per unit value of desired capacitance ($C_{p.u.}$) and DC link voltage ripple (ε)

3.4 Calculation of RMS Value of DC Current Ripple

Most dc ripple current has to be absorbed by the dc capacitor, which is also one of the most important factors for capacitor design and selection. For SPWM inverters, it is clear that calculating the rms current will be very similar to Asec. Eq.(3.30) can be obtained from Figure 3.2(e).

$$I_{rms}{}^2 = \frac{3}{\pi}\int_{\frac{\pi}{6}}^{\frac{\pi}{2}} \left\{ \begin{array}{l} (S_c - S_b)(i_a + i_c - I_{avg})^2 \\ +(S_a - S_c)(i_a - I_{avg})^2 \\ +(1 - S_a + S_b) I_{avg}{}^2 \end{array} \right\} d\omega t \tag{3.30}$$

By combining with (3.4), (3.5) and (3.11), eq. (3.31) is achieved.

$$I_{rms}{}^2 = \frac{3}{\pi}\left\{ \begin{array}{l} -\frac{\sqrt{3}}{12} M \cdot I_{ac}{}^2 \left[-4\cos(2\phi) + 3\sqrt{3}\pi M \cos^2\phi - \frac{27}{4}\cos^2\phi M^2 - 6 \right] \\ +\left(\frac{3\sqrt{2}}{4} I_{ac} \cos\phi M \right)^2 \left(\frac{\pi}{3} - \frac{\sqrt{3}}{2} M \right) \end{array} \right\} \tag{3.31}$$

It can be simplified to (3.32), which has been proved in [22] by Dr. Kolar. The agreement further proved both equations correctness.

$$I_{rms}{}^2 = 4 I_{ac}{}^2 M \left[\frac{\sqrt{3}}{4\pi} + \cos^2\phi \left(\frac{\sqrt{3}}{\pi} - \frac{9}{16} M \right) \right] \tag{3.32}$$

$v_{3\omega}$ does not appear in (3.31), which is the same as the three expressions in Table 3.2. This means the I_{rms} is not influenced by the 3rd harmonic injection, but varies with *MI* and power factor. Please note that during over modulation operation, the expression of I_{rms} remains the same, as *A·sec* does. The only difference is that the *MI* is extend from 1 to 1.15.

The p.u. value of I_{rms} versus MI is summarized in Figure 3.7 for SPWM, and for the sake of comparison, simulation results of several six-step operation points are also shown.

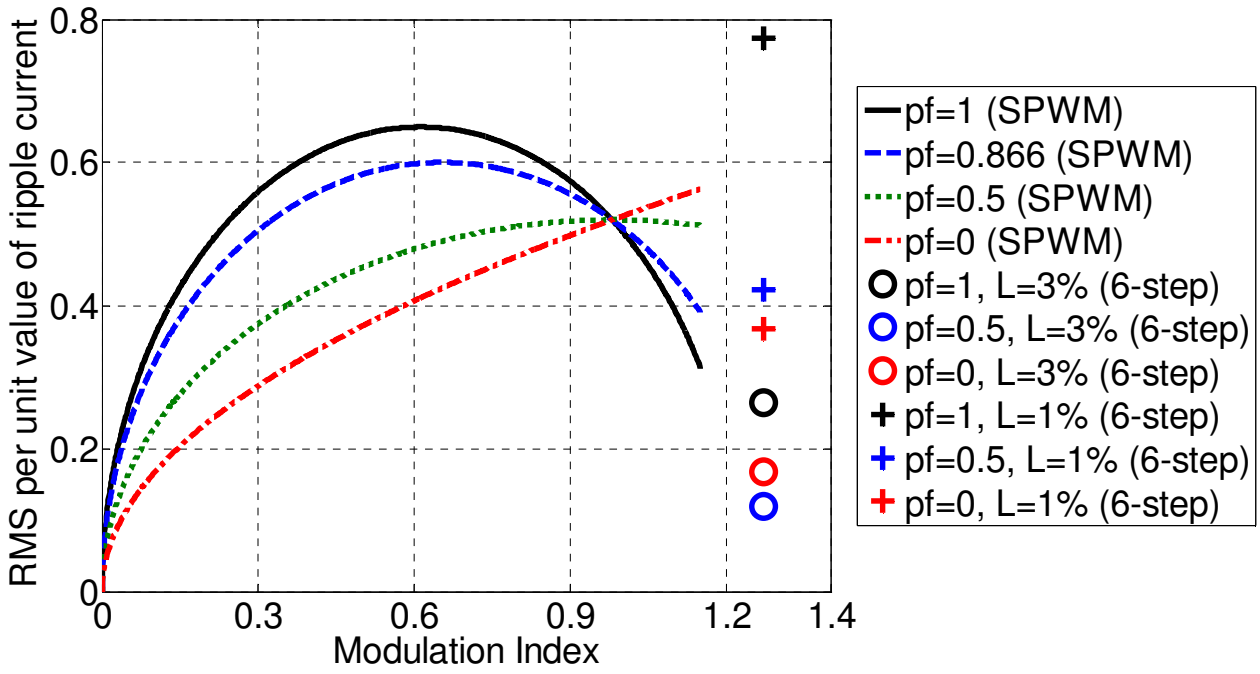


Figure 3.7 The relationship between the p.u. value of I_{rms} versus MI with different power factors for SPWM and 6-step operations

CHAPTER 4 DC Capacitance Requirement of the Three-Phase Diode Rectifier

The previous chapter is about the SPWM inverter/PWM rectifier. In this chapter, the dc capacitance and current ripple will be calculated for the traditional diode rectifier.

The three-phase diode rectifier is not specially built in a HEV system. However, every IGBT has a freewheeling diode paralleled with it. Therefore, when the traction motor is doing regenerative breaking, the energy from the motor will have to be sent back to the dc link side and intended to store in the battery or any other energy storage system connected on the other side of the dc-dc converter. When the firing angle is 0, that is to say, there is no control for the switches, but only the diodes, the converter is an uncontrolled diode rectifier as shown in Figure 2.4. Also, when the generator on the engine side is generating power, the PWM rectifier can work as a diode rectifier if there are no switching signals sent to the IGBTs.

In conclusion, in the HEV system, even if there is no diode rectifier purely consisted with diodes, the diode rectifier is still existed because of the freewheeling diode of the IGBT.

4.1 Introduction

Generally speaking, based on if there is current commutation when the phase current shifts, the diode rectifier can be divided into three cases:

a) Without line inductance;

b) With a small line inductance;

c) With a big line inductance.

How to determine this critical point between small and big inductance is the first question.

4.2 Calculation of the Critical Inductance

At this critical point, the output current i_d is between discontinuous current mode (DCM) and continuous current mode (CCM), where no phase current commutation happens. Therefore, there are always two diodes on at the same time, as shown in Figure 4.1. Therefore, (3.1) can be obtained from Figure 4.1.

$$v_{ab} - 2L\frac{di_{d2}}{dt} = V_{dc} \tag{4.1}$$

Assume α is the angle when the line current starts to rise from 0, as shown in Figure 4.3. Since current begins to flow only when the line-to-line voltage v_{ab} becomes equal to the dc link voltage, (3.2) is true.

$$\cos\alpha = \frac{V_{dc}}{\sqrt{2}V_{ac}} \tag{4.2}$$

Hence, by doing integration from 0 to *t* of (3.1), i_{d2} can be expressed as (3.3).

$$i_{d2} = \frac{1}{2L}\left\{\frac{\sqrt{2}V_{ac}}{\omega}\left[\sin(\omega t - \alpha) - \sin(-\alpha)\right] - V_{dc}t\right\} \tag{4.3}$$

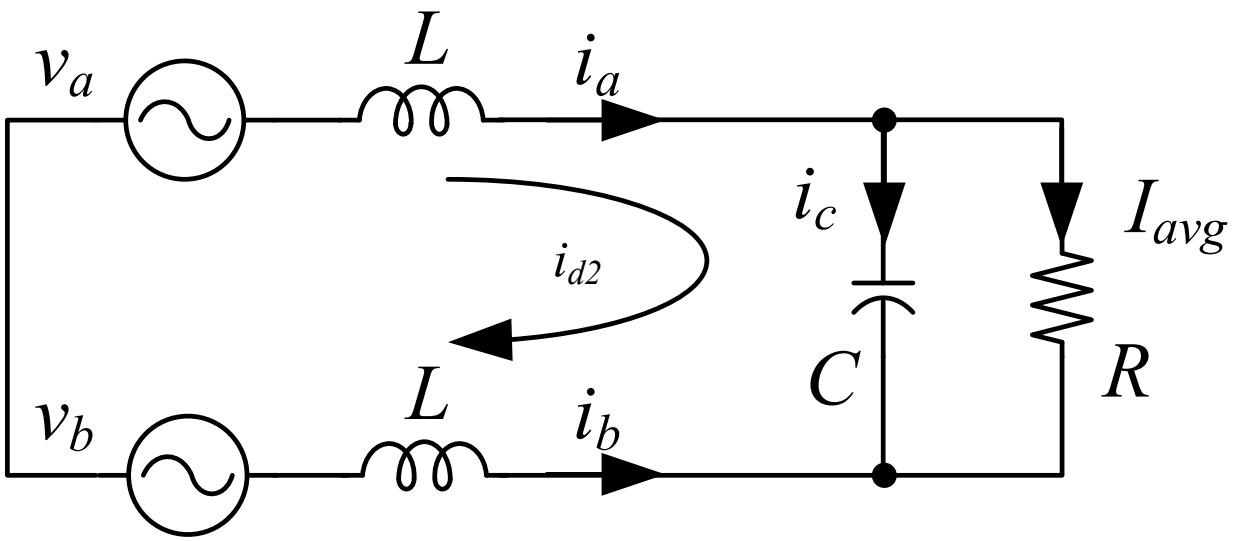


Figure 4.1 Simplified diode rectifier circuit with no line inductance or small line inductance

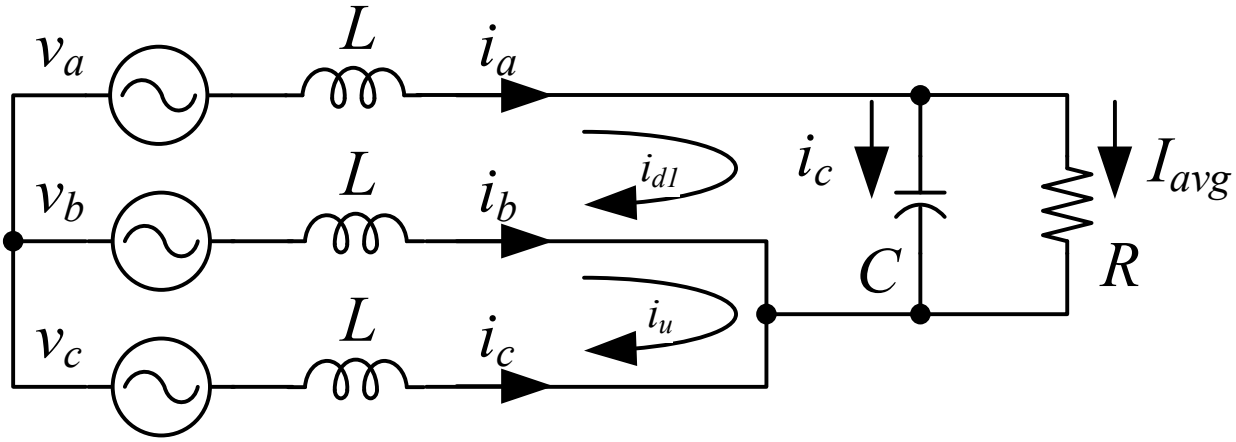


Figure 4.2 Simplified diode rectifier circuit with large line inductance

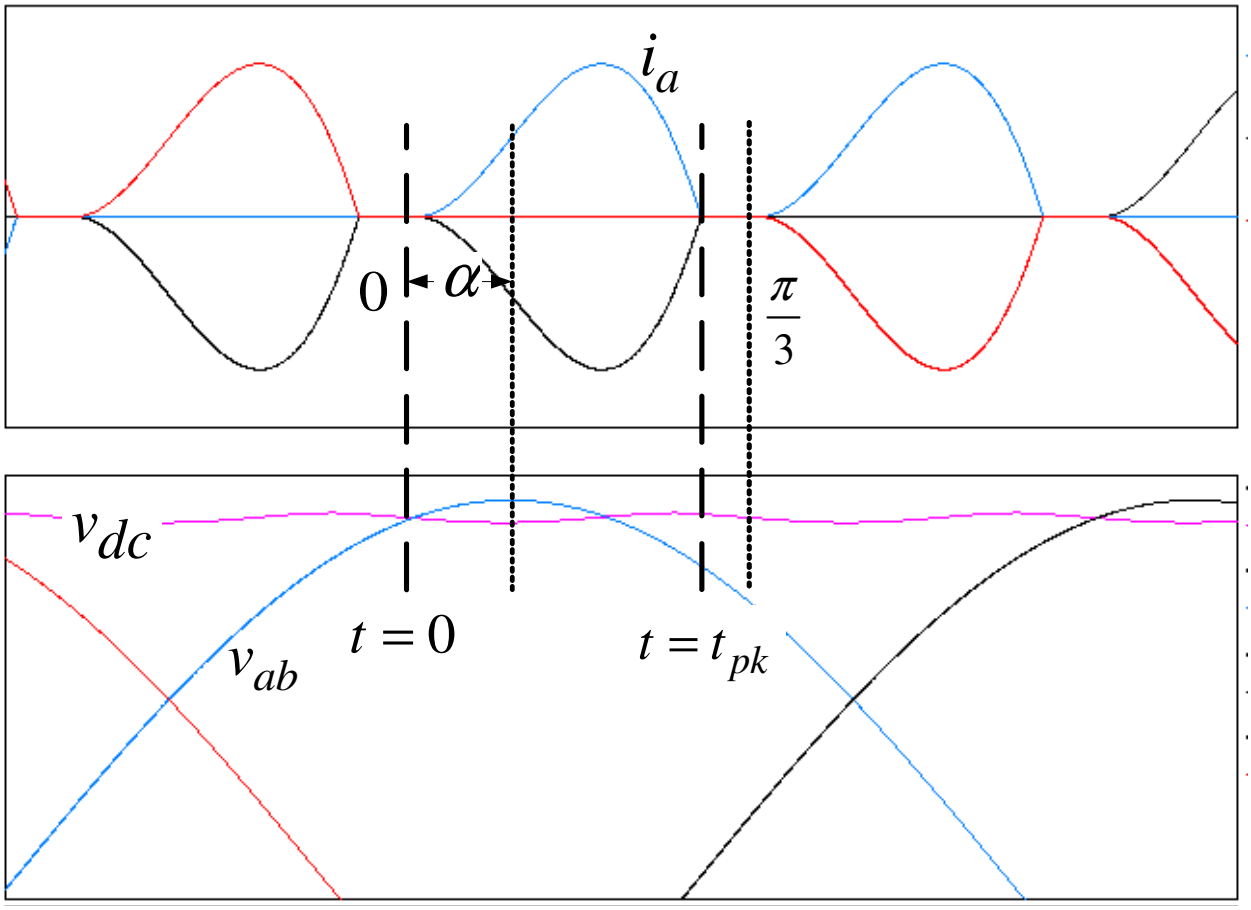


Figure 4.3 Critical inductance calculation of the diode rectifier (α definition) and Asec calculation of the diode rectifier with a small inductance

Since this case is the critical point of i_d, the initial condition is (3.4).

$$i_a = i_{d2}(0) = i_{d2}\left(\frac{T}{6}\right) = 0 \tag{4.4}$$

Assume the fundamental frequency is 60 Hz, so that $t=T/6=1/360$, and $\omega=2\pi 60$. Solving (3.2), (3.3) and (3.4) gives (3.5).

$$\alpha = 0.34767 = 19.92° \tag{4.5}$$

Assume the real power consumed by the load P remains the same. I_{avg} is the same as the

average value of i_a during 60°.

$$\frac{P}{V_{dc}} = I_{avg} = 360\int_0^{\frac{1}{360}} i_{d2}dt \tag{4.6}$$

Then, putting (3.2) and (3.3) into (3.6), the real value of the inductance is expressed as (3.7). By assuming the base value of the inductance is (3.8), the per unit value of critical inductance $L_{p.u.}$ is achieved to be 1.4639%.

$$L = \frac{\frac{360}{2}[-\frac{\sqrt{2}V_{ac}}{\omega^2}(\cos(\frac{\omega}{360}-\alpha)-\cos(-\alpha))-\frac{\sqrt{2}V_{ac}}{\omega}\frac{\sin(-\alpha)}{360}-V_{dc}\frac{(1/360)^2}{2}]}{\frac{P}{\sqrt{2}V_{ac}\cos\alpha}} \tag{4.7}$$

$$L_{base} = \frac{{V_{ac}}^2}{\omega P} \tag{4.8}$$

4.3 Calculation of Required DC Link Capacitance

4.3.1 With No Line Inductance

The voltage waveform of the diode rectifier when there is no line inductance is shown in Figure 4.4. The blue, green, magenta and red waveforms are v_{ab}, v_{bc}, v_{ca} and v_{dc} respectively. Assume the time interval is t_1 when the dc link capacitor is being charged through the diodes by the ac sources, and the time interval is t_2 when the capacitor is discharging to the load. During t_2, the dc link voltage is decreasing exponentially to be exact, like shown in (3.9).

$$V_{r(pp)} = \sqrt{2}V_{ac} - \sqrt{2}V_{ac}e^{-\frac{t}{RC}} \tag{4.9}$$

where R is the load resistance, C is the dc link capacitance and V_{ac} is the three-phase input line-to-line rms voltage. However, for the sake of convenience, the exponential function can be simplified to a linear function (3.10) without much error involved.

$$V_{r(pp)} = \frac{\sqrt{2}V_{ac}t_2}{RC} \tag{4.10}$$

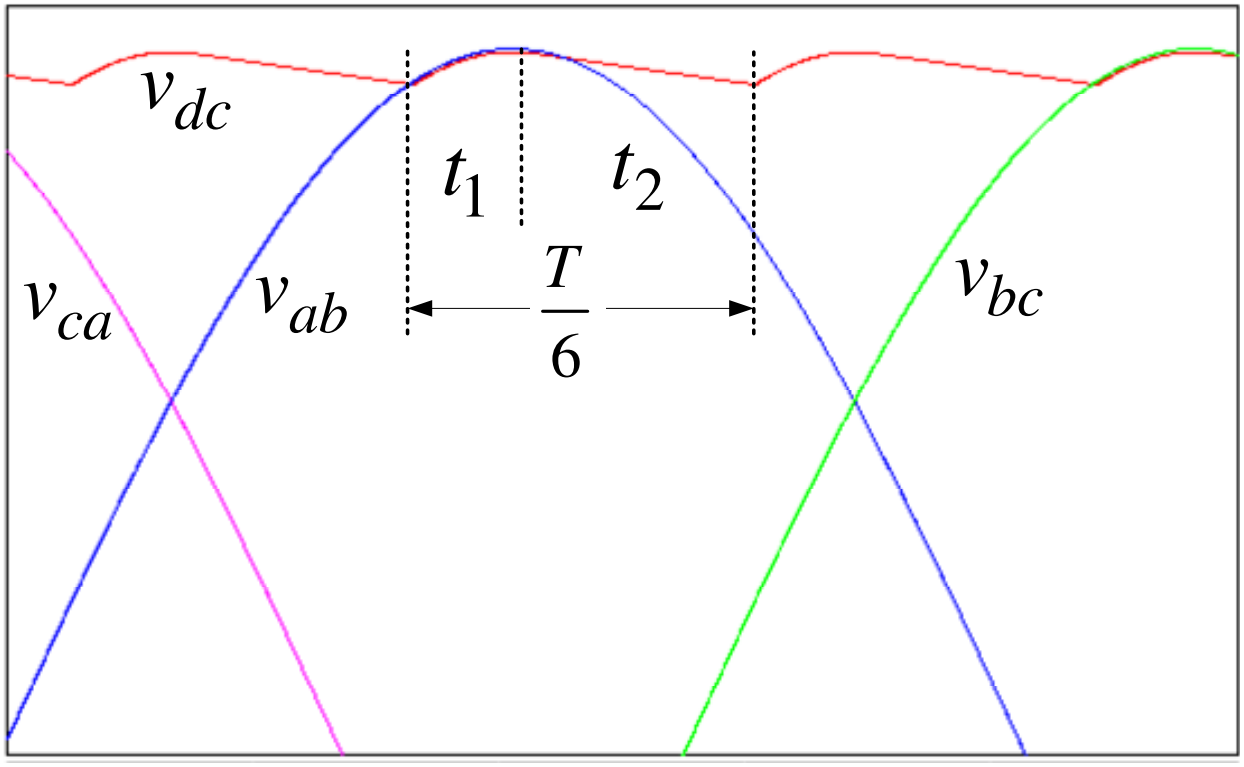


Figure 4.4 Asec calculation of the diode rectifier without line inductance

An approximated assumption is made here, in order to get the simple expression of the *A·sec*, which is $t_2 \approx$T/6. Therefore,

$$V_{r(pp)} = \frac{\sqrt{2}V_{ac}}{6fRC} \tag{4.11}$$

Hence, since a linearly decreasing voltage is assumed already, the average of the dc link voltage (4.12) is at the middle point of the peak to peak ripple voltage.

$$V_{dc} = \sqrt{2}V_{ac} - \frac{V_{r(pp)}}{2} \tag{4.12}$$

Again, assume the voltage ripple ε in (4.13) is the peak to peak ripple voltage divided by the average dc voltage.

$$\varepsilon = \frac{V_{r(pp)}}{V_{dc}} = \frac{2}{12fRC - 1} \tag{4.13}$$

One of the known conditions is (4.14).

$$R = \frac{{V_{dc}}^2}{P} \tag{4.14}$$

Consequently, substituting (4.13) into (4.14), will yield (4.15).

$$R = \frac{2{V_{ac}}^2\left(\frac{2}{2+\varepsilon}\right)^2}{P} \tag{4.15}$$

Substituting (4.15) into (4.13) will give the final capacitance expression as (4.16).

$$C = \frac{1}{96f}\frac{P}{{V_{ac}}^2}(2+\varepsilon)^2\left(\frac{2}{\varepsilon}+1\right) \tag{4.16}$$

The per unit value of the DC link capacitance (4.17) is only related the dc link voltage ripple factor ε, by assuming the base value in the form of (4.18).

$$C_{p.u.} = \frac{C}{C_{base}} = \frac{1}{96}(2+\varepsilon)^2\left(\frac{2}{\varepsilon}+1\right)2\pi \tag{4.17}$$

$$C_{base} = \frac{P}{2\pi f{V_{ac}}^2} \tag{4.18}$$

4.3.2 With 0%~1.46% Line Inductance

The primary method for this case is to first get the expression of the desired current i_c and secondly to integrate over a period to get *A·sec*. Matlab is used to get the initial value.

The equations for this case are almost the same as in the critical point calculation method. In Figure 4.3, α's assumption is the same as in the previous case. Therefore, (3.2) is again valid. The same (3.1) is obtained from the simplified circuit in Figure 4.1. The solution (3.3) of (3.1) is the phase current. When $t = t_{pk}$, $i_{d2} = 0$. (3.9) is obtained. The real power expression (3.6) is

valid as well.

$$\frac{\sqrt{2}V_{ac}}{2\omega L_s}[\sin(\omega t_{pk}-\alpha)-\sin(-\alpha)]-\frac{V_{dc}t_{pk}}{2L_s}=0 \tag{4.19}$$

Fortunately, only t_{pk} and α are unknowns in the system of equations (3.19) and (3.6), indicating that there exists a unique pair of solutions. Using Matlab, t_{pk} and α can be obtained.

Finally, integrating the positive half of i_c will give the expression of *Asec*. The upper and lower limit of the integration t_1 and t_2 are determined by (3.20) using Matlab. From all of these, (3.21) can be drawn in Figure 4.6 as the blue dashed line, of course by assuming the base value of the capacitance as (3.18).

$$i_c=\frac{\sqrt{2}V_{ac}}{2\omega L_s}[\sin(\omega t-\alpha)-\sin(-\alpha)]-\frac{V_{dc}t}{2L_s}-\frac{P}{V_{dc}}=0 \tag{4.20}$$

$$C=\frac{1}{\varepsilon}\int_{t_1}^{t_2}\left\{\frac{\sqrt{2}V_{ac}}{2\omega L_s}[\sin(\omega t-\alpha)-\sin(-\alpha)]-\frac{V_{dc}t}{2L_s}-\frac{P}{V_{dc}}\right\}dt \tag{4.21}$$

4.3.3 With Line Inductance Greater Than 1.46%

The primary method of this case is the same as the previous one with a small line inductance. However, this case includes two conditions: one is that three diodes are on at the same time as shown in Figure 4.2, and the other is that two diodes are on at the same time as shown in Figure 4.1, because of the phase current commutation.

For the first condition, derive (3.22) and (3.23) from the simplified diode rectifier circuit as shown in Figure 4.2.

$$v_{ab} = \sqrt{2}V_{ac}\cos(\omega t - \alpha) = 2L\frac{di_{d1}}{dt} - L\frac{di_u}{dt} + V_{dc} \tag{4.22}$$

$$v_{bc} = \sqrt{2}V_{ac}\cos(\omega t - \alpha - \frac{2\pi}{3}) = 2L\frac{di_u}{dt} - L\frac{di_{d1}}{dt} \tag{4.23}$$

By combining (3.22) and (3.23), i_{d1} and i_u are obtained.

$$\begin{aligned} i_{d1} = {} & \frac{2\sqrt{2}V_{ac}}{3\omega L}[\sin(\omega t - \alpha) - \sin(-\alpha)] - \frac{2V_{dc}t}{3L} \\ & + \frac{\sqrt{2}V_{ac}}{3\omega L}[\sin(\omega t - \alpha - \frac{2\pi}{3}) - \sin(-\alpha - \frac{2\pi}{3})] + i_{d1}(0) \end{aligned} \tag{4.24}$$

where $i_{d1}(0)$ is the initial condition.

$$\begin{aligned} i_u = {} & \frac{2\sqrt{2}V_{ac}}{3\omega L}[\sin(\omega t - \alpha - \frac{2\pi}{3}) - \sin(-\alpha - \frac{2\pi}{3})] \\ & + \frac{\sqrt{2}V_{ac}}{3\omega L}[\sin(\omega t - \alpha) - \sin(-\alpha)] - \frac{V_{dc}t}{3L} \end{aligned} \tag{4.25}$$

To calculate $i_{d1}(0)$, (3.26) is used, and (3.27) is achieved, where t_1 and the origin are demonstrated in Figure 4.5.

$$i_u(t_1) = i_{d1}(t_1) \tag{4.26}$$

$$i_{d1}(0) = \frac{\sqrt{2}V_{ac}}{3\omega L}(2\sqrt{3})\sin(\frac{\omega t_1}{2})\sin(\frac{\omega t_1}{2} - \alpha - \frac{\pi}{3}) + \frac{V_{dc}t_1}{3L} \tag{4.27}$$

For the second condition, (3.28) is derived from the simplified circuit, and please note that the time delay of π/3 is due to the reference voltage is v_{ab}.

$$v_{ac} = \sqrt{2}V_{ac}\cos(\omega t - \alpha - \frac{\pi}{3}) = 2L\frac{di_{d2}}{dt} + V_{dc} \tag{4.28}$$

where i_{d2} is shown in Figure 4.1.

Therefore, i_{d2} is obtained from (3.28).

$$i_{d2} = \frac{\sqrt{2}V_{ac}}{2\omega L}[\sin(\omega t - \alpha - \frac{\pi}{3}) - \sin(\omega t_1 - \alpha - \frac{\pi}{3})] - \frac{V_{dc}}{2L}(t - t_1) + i_{d2}(t_1) \tag{4.29}$$

where $i_{d2}(t_1)$ is the initial condition.

Since the condition is known:

$$i_{d2}(t_1) = i_u(t_1) \tag{4.30}$$

Substituting (3.30) into (3.25) yields (3.31).

$$\begin{aligned} i_{d2}(t_1) = {} & \frac{2\sqrt{2}V_{ac}}{3\omega L}[\sin(\omega t_1 - \alpha - \frac{2\pi}{3}) - \sin(-\alpha - \frac{2\pi}{3})] \\ & + \frac{\sqrt{2}V_{ac}}{3\omega L}[\sin(\omega t_1 - \alpha) - \sin(-\alpha)] - \frac{V_{dc}t_1}{3L} \end{aligned} \tag{4.31}$$

Finally, by utilizing (3.32) and (3.33), t_1 (the critical point from commutation to normal status) and V_{dc} can be achieved with Matlab. Using the same method as before, after getting the expression of *Asec*, the per unit value of capacitance can be obtained.

$$i_{d2}\left(\frac{1}{360}\right) = i_{d1}(0) \tag{4.32}$$

$$\frac{1}{1/360}\left(\int_0^{t1} i_{d1}dt + \int_{t1}^{\frac{1}{360}} i_{d2}dt\right) = \frac{P}{V_{dc}} \tag{4.33}$$

In conclusion, three curves, that show the relationship between the per unit capacitance value and the given tolerable voltage ripple percentage ε, for no line inductance, small inductance, and large inductance respectively, are drawn in the same graph in Figure 4.6, with comparison to the SPWM operation.

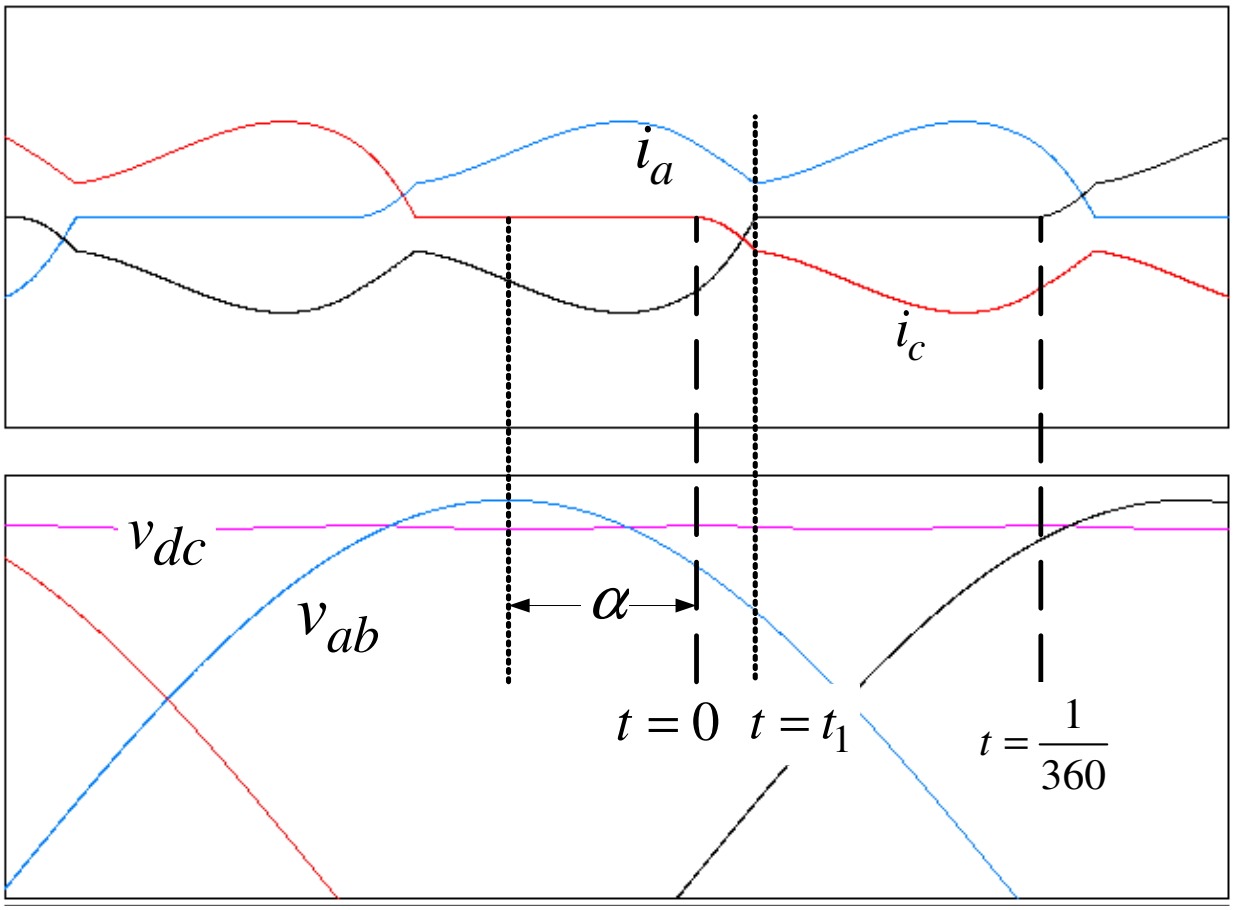


Figure 4.5 Asec calculation of the diode rectifier with a large inductance

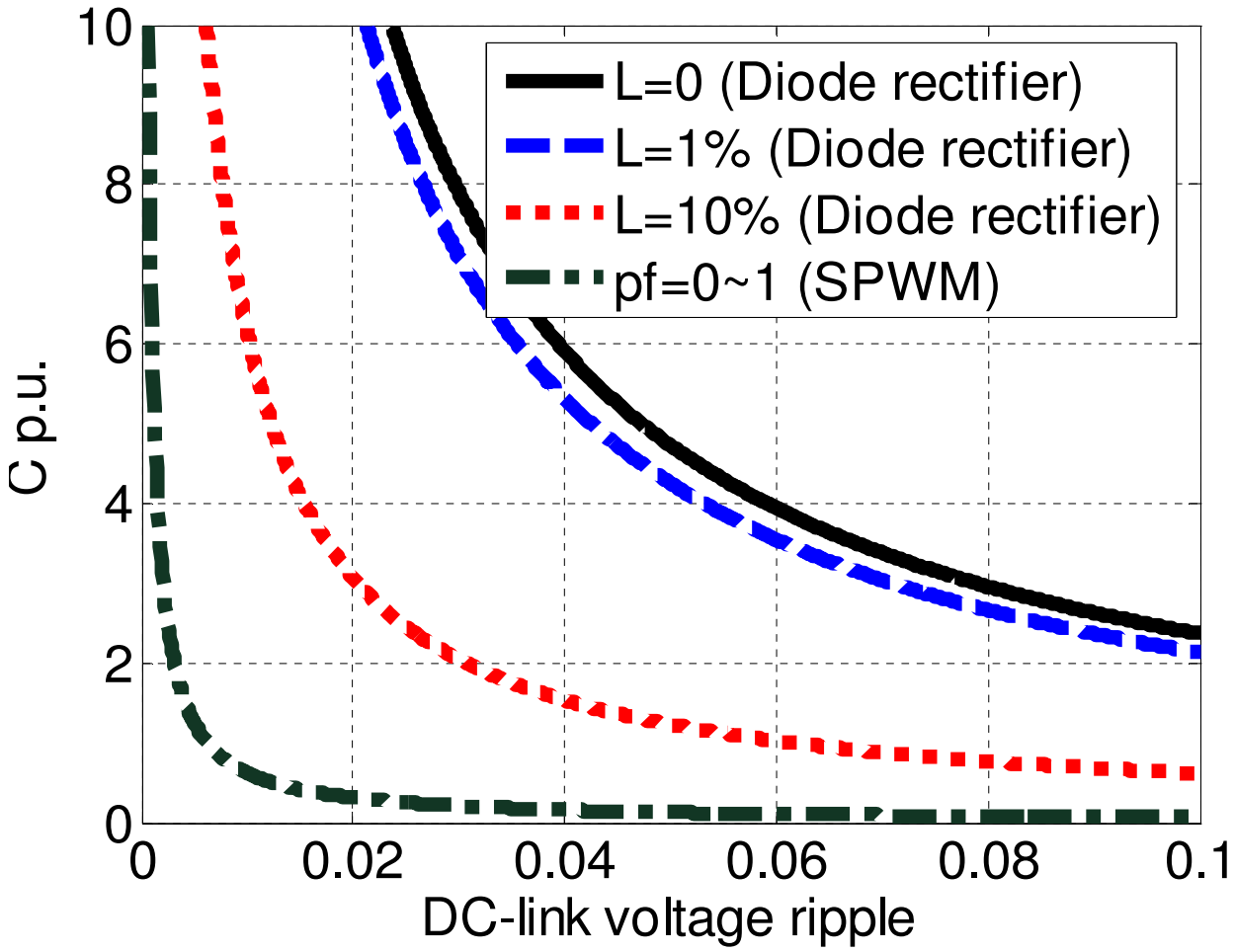


Figure 4.6 Cp.u. versus ε for rectifier operation compared with SPWM operation.

CHAPTER 5 DC Capacitance Requirement of the Six-Step Inverter

Six-step operation is used at a higher speed, when higher output voltage is required. It is because that six-step operation has higher dc utilization than the traditional SPWM operation.

5.1 Simplified Configuration and System Parameters

As the traction motors run to a higher speed, the back electromotive force (EMF) should be considered. In this case, the equivalent circuit of the inverter under six-step operation is shown in Figure 5.1. Assume that there are three more voltage sources v_a, v_b, and v_c, inserted in each phase leg at the load side, representing the three-phase back EMFs of the traction motors. Since the load is a traction motor, inductors and resistors should be added as well. In order to have unity power factor, the inserted voltage source will have a leading power factor, $v_a = V_i \sin(\omega t + \varphi)$ (V_i and φ are the amplitude and angle of the inserted voltage source—the back EMF, which are calculated by assuming a power factor and an inductance).

Assume the inductance L ranging from 0.3%, 1% and 3% of the per unit (p.u.) value, the resistance R is 1% p.u., the base system is as (5.1), the base speed of the traction motor is 1200 rpm, and the maximum speed is 5000 rpm. Therefore, the inductance of the system base would be as shown in Table 5.1.

$$\begin{cases} P = 150kW \\ V_{ll} = 480V \end{cases} \tag{5.1}$$

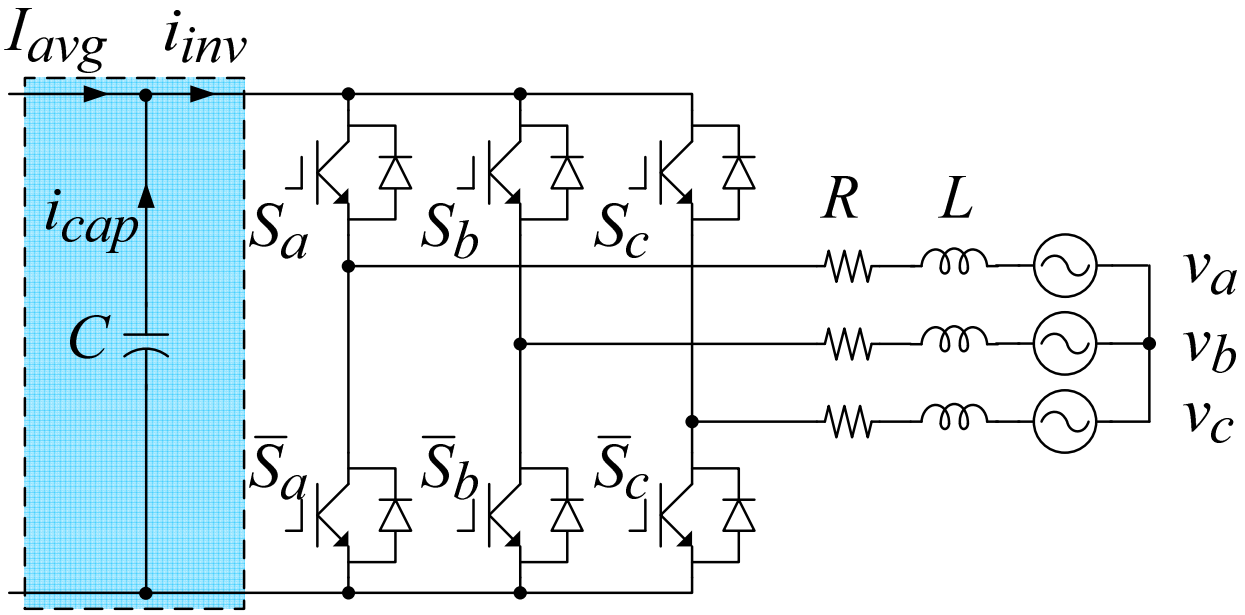


Figure 5.1 The simplified equivalent circuit of the inverter under six-step operation

Table 5.1 The list of Inductance and Resistance Changing Base

	Per unit (base speed)	L_{real}	$L_{new,base}$	**Per unit (max speed)**
L	0.3%	18.335 uH	1.466772 mH	1.25%
	1%	61.115 uH	1.466772 mH	4.17%
	3%	183.346 uH	1.466772 mH	12.5%
R	1%	0.01536 Ω		1%

By knowing the inductance and assuming a power factor, the amplitude and angle of the inserted voltage source, V_i and φ, are obtained in Table 5.2.

Table 5.2 The list of Inserted Voltage source Amplitude and Phase Angle Based on Different Power Factor and Load Impedance

p.f.	***L***					
	3%		**1%**		**0.3%**	
	$V_{i(peak)}$ / V	**φ/°**	$V_{i(peak)}$ / V	**φ/°**	$V_{i(peak)}$ / V	**φ/°**
1.0	391.08	7.19624	388.34	2.41002	388.03	0.72339
0.5	433.28	3.69049	404.27	1.63847	394.24	0.84928
0.0	440.93	0.50928	408.27	0.55002	396.84	0.56587

5.2 Calculation of Required DC Link Capacitance

From a simplified schematic of Figure 5.1, which is very similar to Figure 4.2, (4.2) is obtained.

$$\begin{cases} V_{dc} = Ri_a + L\dfrac{di_a}{dt} + v_a + R(-i_b) + L\dfrac{d(-i_b)}{dt} + (-v_b) \\ i_a + i_b + i_c = 0 \\ Ri_a + L\dfrac{di_a}{dt} + v_a = Ri_c + L\dfrac{di_c}{dt} + v_c \end{cases} \tag{5.2}$$

By combining them together, (4.3) is achieved.

$$\frac{di_a}{dt} + \frac{R}{L}i_a = \frac{V_{dc}}{3L} - \frac{v_a}{L} \tag{5.3}$$

Therefore, the solution of (5.3) should be in the general form of: $i_a = i_{a(p)} + i_{a(g)}$, where

$i_{a(p)}$ stands for the particular solution and $i_{a(g)}$ represent general solution. The particular solution $i_{a(p)}$ is (4.4).

$$i_{a(p)} = a + C\cos(\omega t - \varphi) + D\sin(\omega t - \varphi) \tag{5.4}$$

where $a = \frac{V_{dc}}{3R}, D = -\frac{V_i}{R^2 + \omega^2 L^2}, C = -\frac{D\omega L}{R}$.

and the general solution $i_{a(g)}$ is (4.5).

$$i_{a(g)} = k \cdot e^{-\frac{R}{L}t} \tag{5.5}$$

For i_a, the only unknown coefficient is *k*, the initial coefficient. To get this, Matlab can be utilized to calculate *k*, integrate i_a, and draw Figure 5.2 showing the relationship between the per unit value of the desired capacitance and a given dc link voltage ripple requirement.

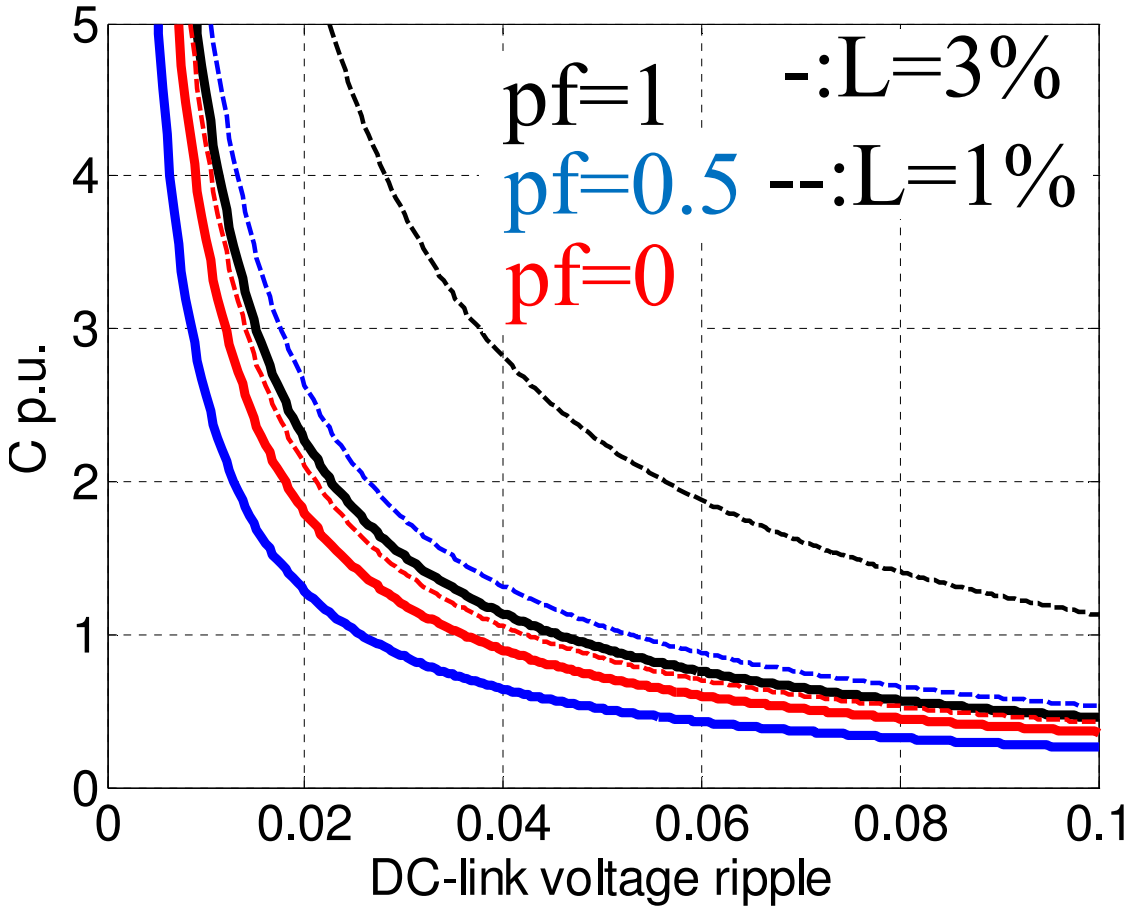


Figure 5.2 Cp.u. versus ΔV for 6-step

In conclusion, all figures above are aggregated and compared, in Figure 5.3 and Figure 5.4

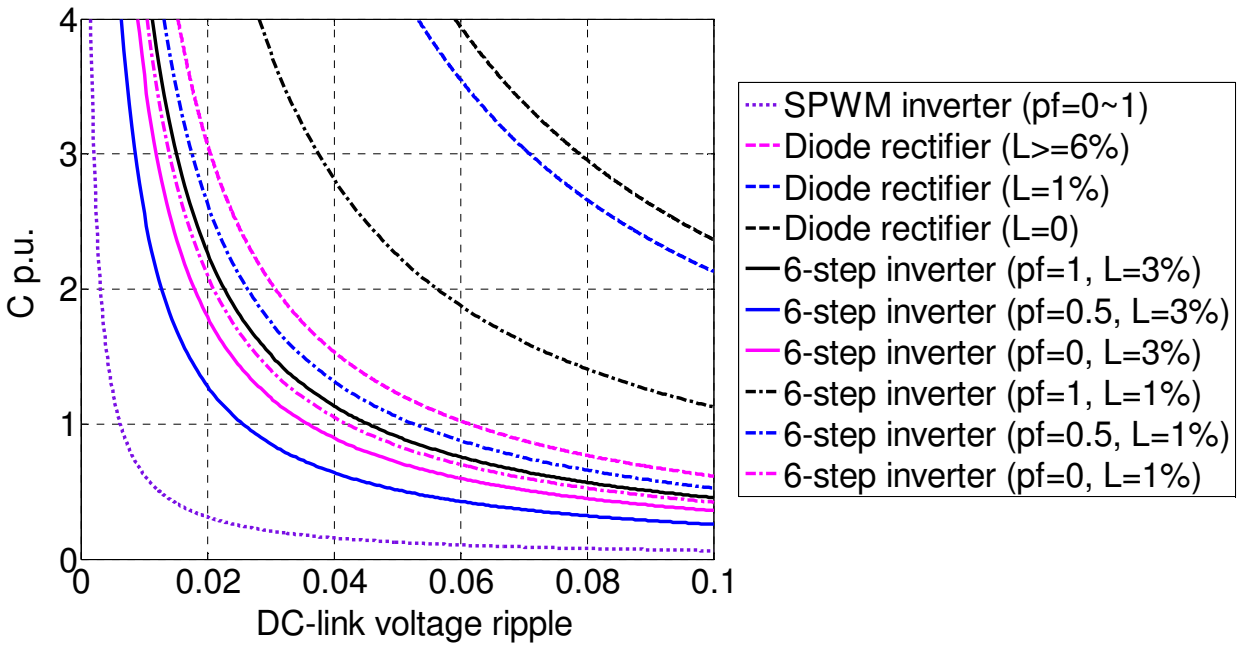


Figure 5.3 The aggregate of all figures above: Cp.u. versus ΔV for all operations

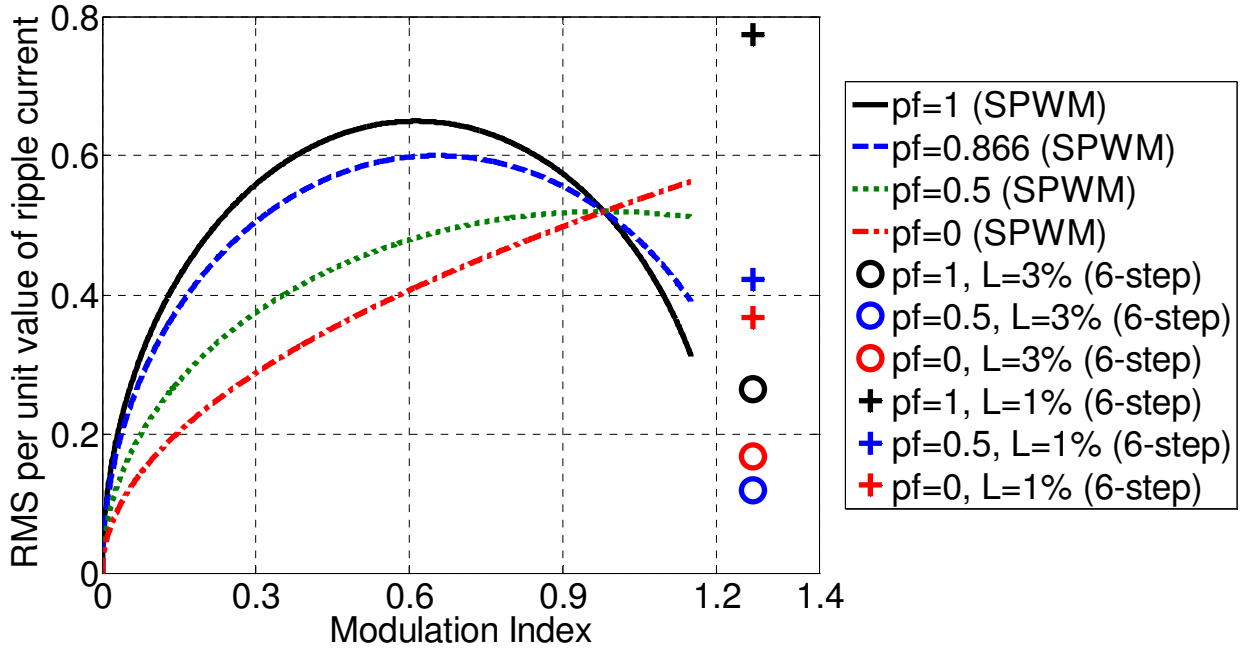


Figure 5.4 ΔI_{RMS} versus MI for SPWM and 6-step operation

CHAPTER 6 Prototype and Testing Results of SHEV Power Electronics Module

6.1 Prototype

The inverter module in Figure 6.1 was developed to achieve 100 kW continuous output power (150 kW peak power) for use in a series hybrid electric bus. The rated output line-to-line voltage is 480 V, and the rated line current is 180 A. Therefore, according to (3.29) and Table 3.3, C_{base} is 516.95 uF.

This paper shows calculations of the minimum capacitance that one system needs without any close-loop control strategy. Therefore, the experiments were done under open loop circumstances.

The experiment is done at the condition when the dc link voltages are 200 V, 300 V, 400 V, 500 V, 600V and 650 V, the switching frequency is 5 kHz, the fundamental frequency is 200 Hz, and the power factor is almost 0 with a purely inductive load—1 mH in each phase connected in wye. The inverter is operated under the SPWM normal modulation method. In this prototype, the parameters of the setup are listed in Table 6.1. In the system in Figure 6.1, the total dc link capacitance is 510 uF with six 85 uF 1000 V film capacitors in parallel.

The per unit value of dc capacitance can be obtained.

$$C_{p.u.} = \frac{510uF}{516.95uF} = 0.9866 \tag{6.1}$$

Table 6.1 The Configuration in the Prototype

Parameters	**Value**
Load inductor	*1 mH*
Power factor (pf)	*0*
DC link capacitance	*510 uF*
DC link voltage	*650 V*
AC current	*180 A*
Switching frequency	*5 kHz*
Fundamental frequency	*200 Hz*
Modulation index (MI)	*0.9*

From Figure 3.6, the nearest point of the per unit value of dc capacitance is 0.9858, whose y-coordinate indicates that the voltage ripples on the dc link would be 3.65%. This is verified by the following experiment results.

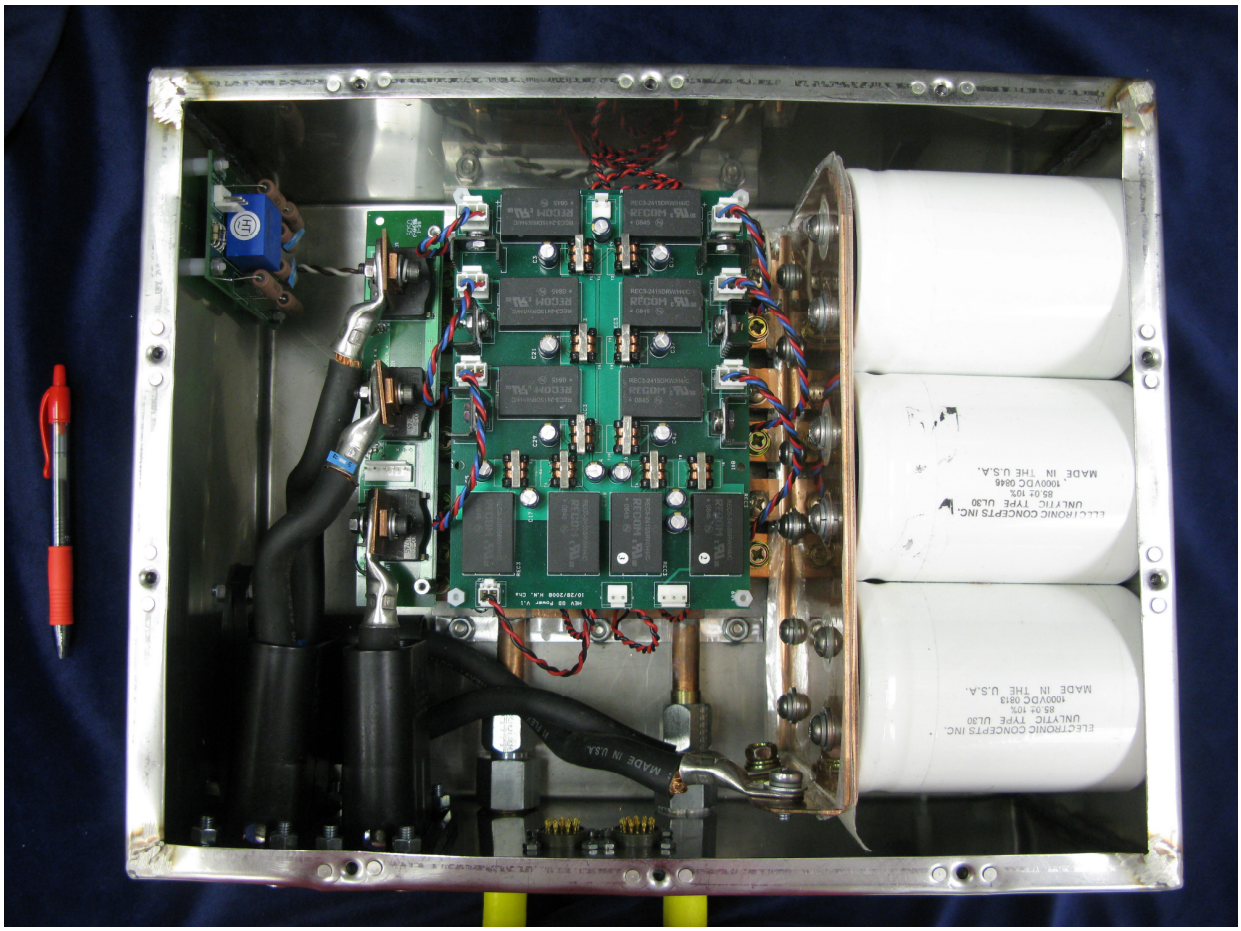


Figure 6.1 Inverter module assembly photos (including DC link capacitors, IGBT module, Gate Drive board and Gate drive power supply on top)

6.2 Test Results of Voltage Ripple

The experimental results are shown in Table 6.2.

Table 6.2 Expreimental Result of Voltage ripple

Vdc/V	**Iac/A**	**Vdc ripple/V**	**ε/%**
200	58	7.8	3.9
300	87	10.8	3.6
400	116	13.7	3.4
500	145	16.6	3.3
600	173	20.9	3.5
650	180	21.7	3.3

As mentioned before, the maximum voltage ripple on the dc link during one switching cycle should be around 3.6% of the dc voltage by the theoretical calcuation, which is in close agreement with the test result shown in Table 6.2. The purple, blue and yellow nearly sinusoidal waveforms in Figure 6.2, Figure 6.3, and Figure 6.4 are the load phase currents, and the green waveform is the dc link voltage ripple. The 6ω ripple component in the dc link voltage comes from the almost pure inductive load.

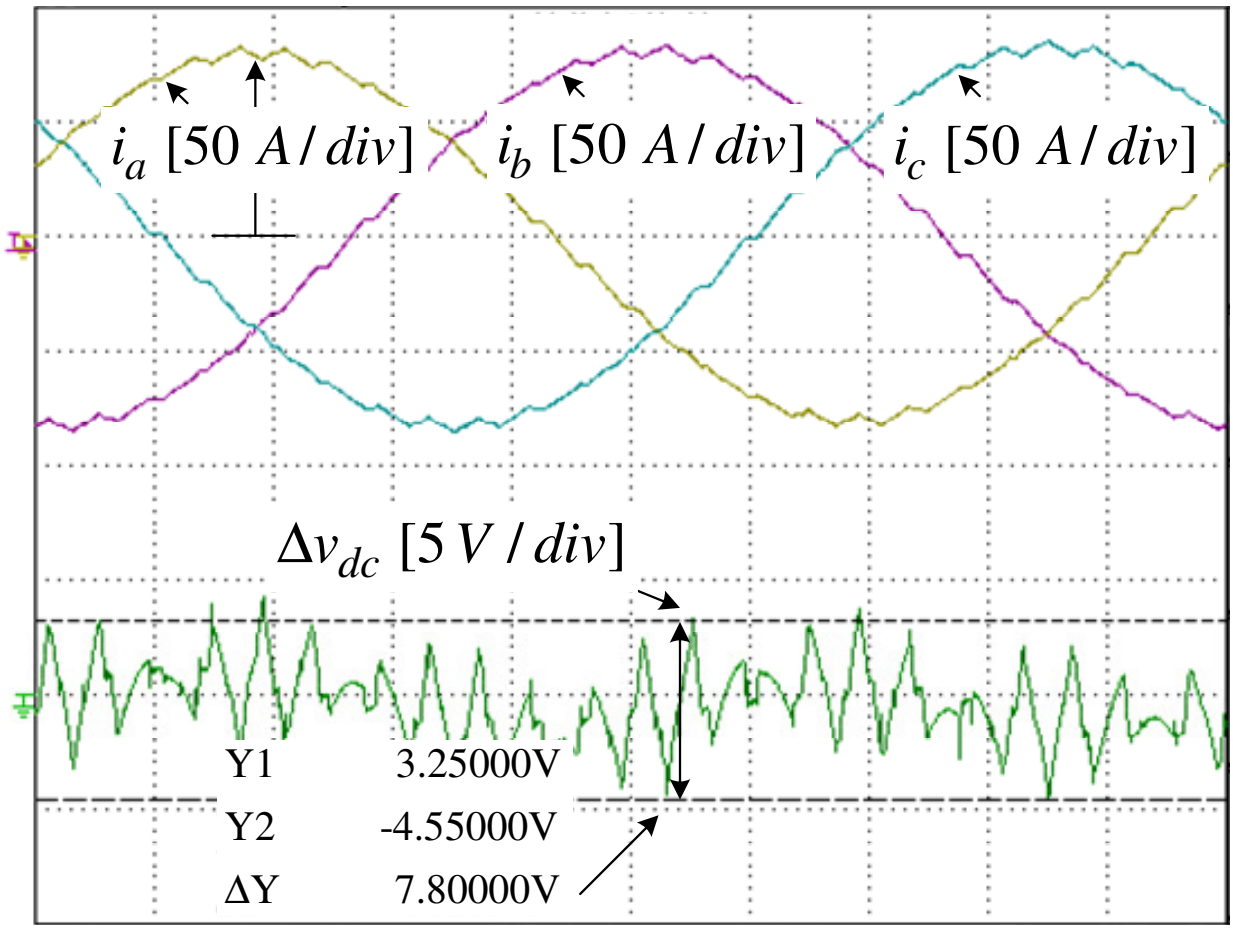


Figure 6.2 The experimental waveforms of three phase currents and DC link voltage ripple with DC link voltage at 200 V.

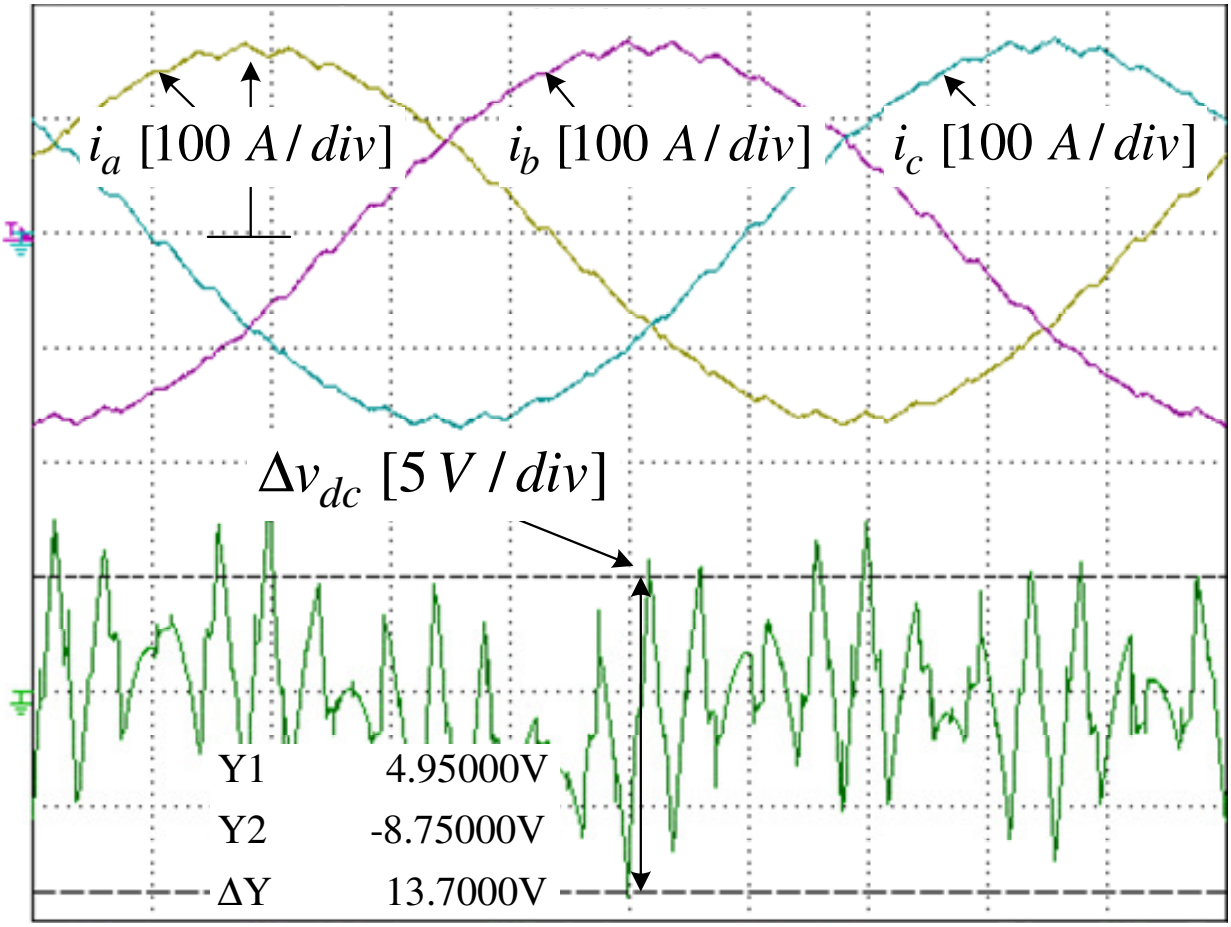


Figure 6.3 The experimental waveforms of three phase currents and DC link voltage ripple with DC link voltage at 400 V

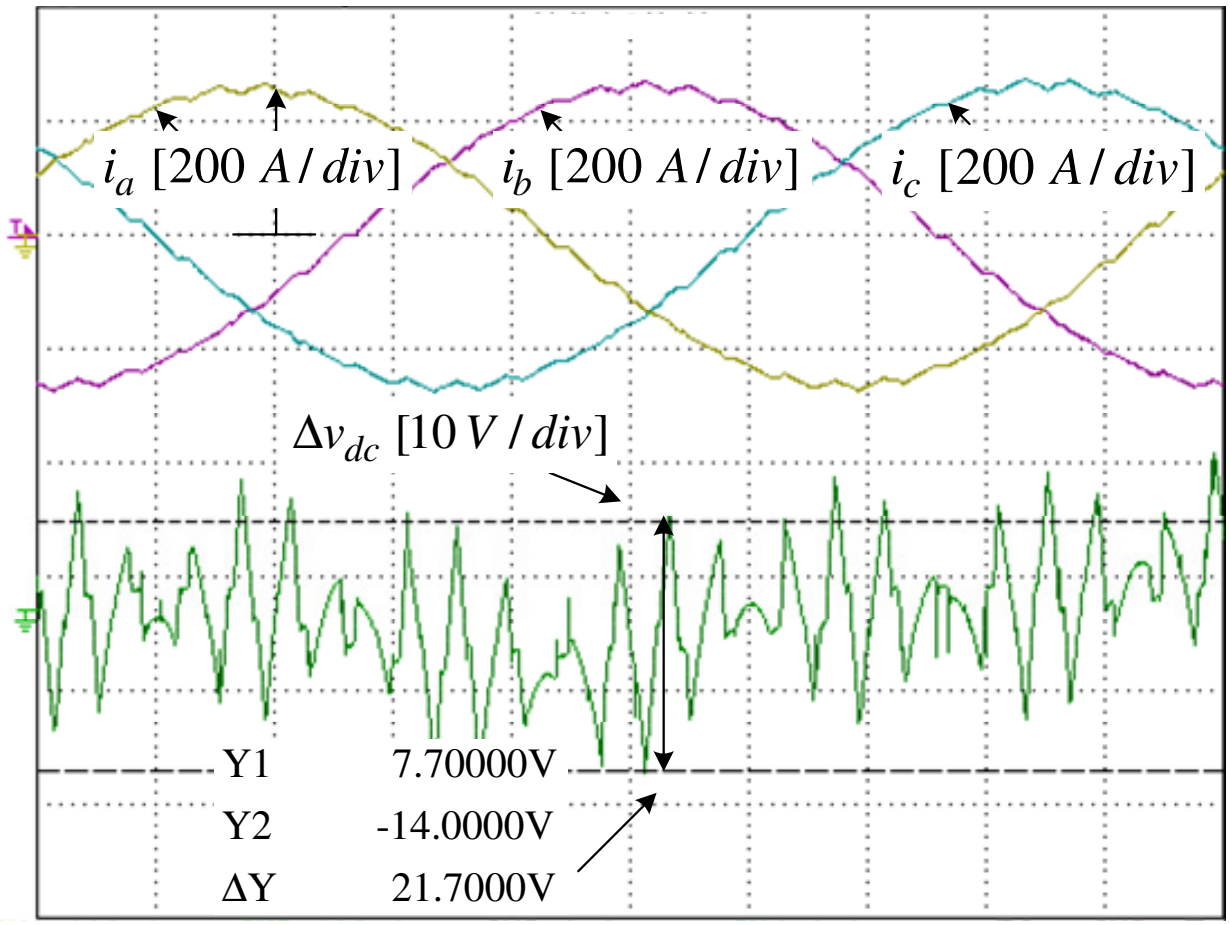


Figure 6.4 The experimental waveforms of three phase currents and DC link voltage ripple with DC link voltage at 650 V

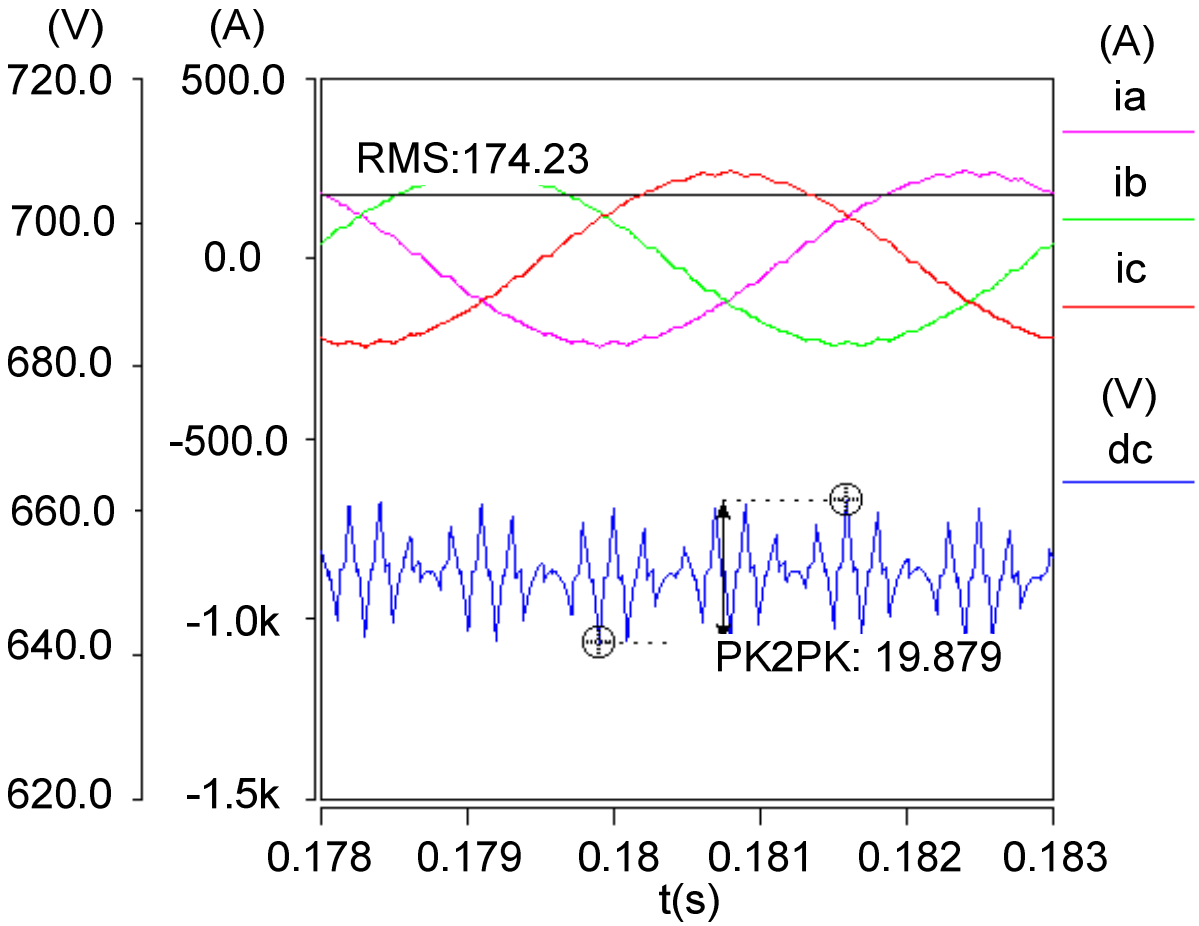


Figure 6.5 The simulation waveforms of three phase currents and DC link voltage ripple with DC link voltage at 650 V

6.3 Test Results of Current Ripple

From Figure 5.4, when pf=0 and MI=1, the rms current per unit value is 0.52; when MI=0.75, the p.u. is 0.46; when MI=0.5, the p.u. is 0.38; when MI=0.25, the p.u. is 0.27. The experimental results are shown in Table 6.3, which is in close agreement with the theoretical value.

$$i_d = S_a i_a + S_b i_b + S_c i_c \tag{6.2}$$

Table 6.3 Experimental Results of rms current of The Capacitor

Vdc/V	***MI=1***			***MI=0.75***		
	Iac/A	**Irms/A**	**ε**	**Iac/A**	**Irms/A**	**ε**
200	30.2	15.15	0.50	22.7	10.40	0.46
300	45.3	23.80	0.53	33.9	15.57	0.46
400	60.4	33.28	0.55	45.2	21.50	0.48
500	75.3	40.10	0.53	56.7	26.60	0.47
600	90.6	48.00	0.53	67.8	31.53	0.47
Vdc/V	***MI=0.5***			***MI=0.25***		
	Iac/A	**Irms/A**	**ε**	**Iac/A**	**Irms/A**	**ε**
200	15.1	5.73	0.38	7.22	1.93	0.27
300	22.5	8.83	0.39	10.9	3.02	0.28
400	30.0	11.4	0.38	14.3	3.88	0.27
500	37.6	15.0	0.40	18.1	4.80	0.27
600	44.9	17.7	0.39	21.6	5.65	0.26

The yellow and green waveforms in Figure 6.6 are V_{ce} waveforms of the lower switches of phase A and B. The red and orange sine waveforms are the phase currents of phase A and C. The middle PWM red waveform is the inverter input current and since pf=0, it is the capacitor current i_c as well due to I_{avg} =0. Since layout of the dc link is of the busbar design type, the capacitor current was measured by math function in oscilloscope by (6.2).

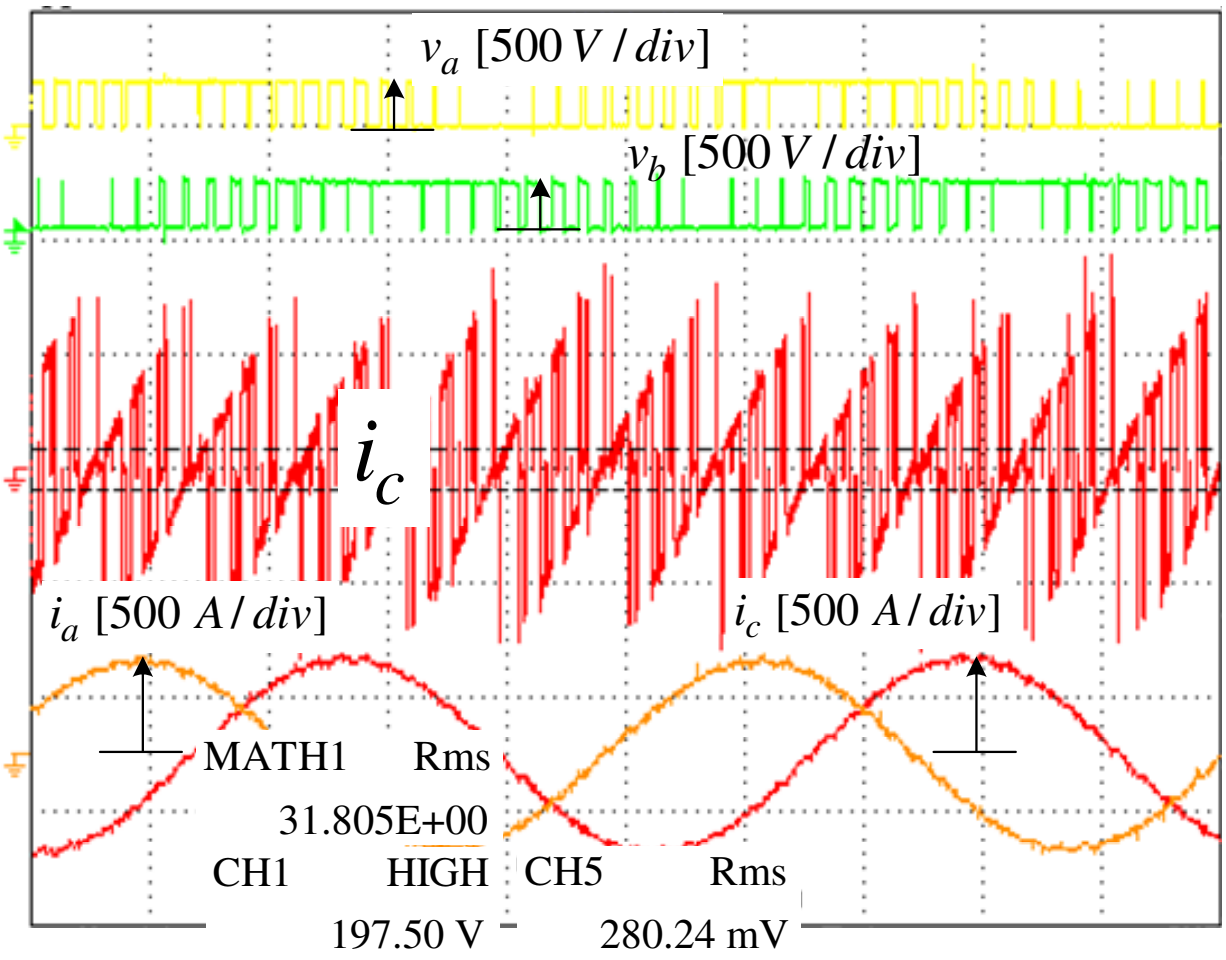


Figure 6.6 The experimental waveforms of the capacitor current with DC link voltage at 200 V, pf=0 and MI=0.9

Theoretical equations to express capacitance versus voltage ripple and rms ripple current versus modulation index have been developed for SPWM. These equations improve the design/calculation of the required dc capacitance and enhance insight into the limits and optimum operation of the HEV converter/inverter system as compared to the traditional empirical equations and simulations. The validity of the theory was verified by the experimental results of a three-phase SPWM inverter system.

CHAPTER 7 Minimizing the DC Capacitance between the DC-DC Converter and SPWM inverter—A Carrier Modulation Method

7.1 Introduction

In the HEV converter/inverter system, for the sake of boosting the battery's low dc voltage to high dc voltage, and then converting it into ac voltage to drive the traction motors, the inverters are always connected in series to the dc-dc converters, as shown in Figure 7.1. However, the dc link capacitor bank between the dc-dc converter and the inverter is usually bulky, heavy and expensive, due to the fact that it must absorb all the current ripples from every converter connected to it. Therefore, minimization of the dc capacitor is an essential step towards developing and manufacturing compact low-cost HEV converter/inverter systems for high temperature operation, long life and high reliability [36].

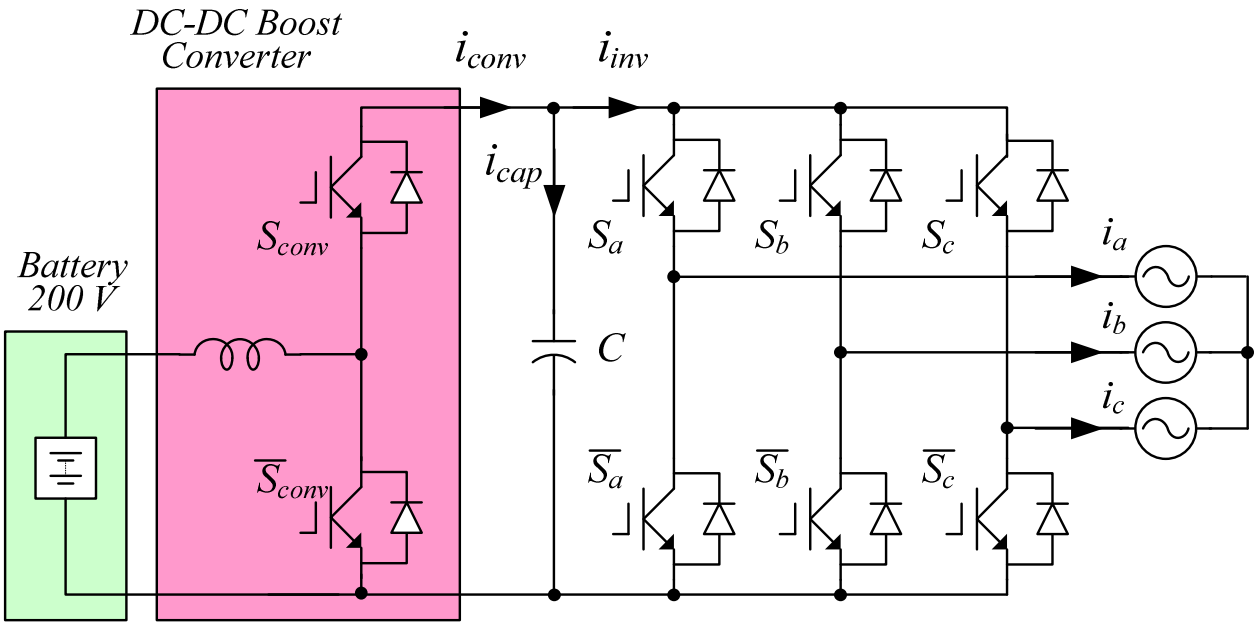


Figure 7.1 The schematic of the bidirectional DC-DC converter and the inverter

Yet the bottleneck of the capacitor's size is determined by the current ripple requirement rather than the voltage ripple requirement due to the existing capacitors-making technology. Similar to the condition described in [9], in order to minimize the dc link capacitance between the dc-dc converter and the SPWM inverter, making the converter side dc link current i_{conv} equal to the inverter side dc link current i_{inv} in a PWM converter-inverter system is the final destination. Ideally, no current will flow through the dc link capacitor and no voltage fluctuation will be across the capacitor, meaning no capacitor is needed at all. Till now, most papers that discussed the current ripple reduction and the dc link capacitance minimization are based on the AC-DC-AC PWM converter-inverter systems with relatively complicated close-loop control methods [9-11, 14, 24, 27-29]. The best result that they can achieve is almost without any dc link capacitors. Besides, there are papers discussing innovative PWM strategies only on the inverter side, allowing reduction of the dc input current ripples [30-32, 37], which is the same as reducing the capacitance. Still, there are a few papers related to DC-DC-AC PWM converters [33, 38]. [33]

used bang-bang control for the dc-dc converter to minimize the dc link capacitance, however it is a complicated close-loop control. Additionally, [38] developed a single-phase PWM method for the inverter to reduce 2/3 of the switching loss and achieve high efficiency; this kind of PWM method requires the system to have bigger ripple on the dc link so that only a tiny dc link capacitor is needed. These are either complicated close-loop control for the dc-dc converter, or the PWM strategy for the inverter. However, very few papers have been written focusing on the current ripple reduction by synchronizing between the dc-dc converter and the SPWM inverter. Shown in Figure 7.2 (c), the black solid line shows the converter output current when synchronized, while the blue dashed line shows the one that is unsynchronized. Therefore, in order to cancel the current ripple with the inverter input current shown in Figure 7.2 (a), the solid line one will definitely do a better job than the dashed line one. In conclusion, a synchronized PWM method will help minimize the capacitance, whereas an unsynchronized PWM may double the requirement of the capacitance. Hence, a better way to minimize the dc capacitance is to reduce the current ripple through the capacitor by synchronizing the dc-dc converter and the SPWM inverter. [34] made a good start for the synchronization by making the dc-dc converter's switching frequency twice as much as the inverter's switching frequency and optimizing the phase difference of the carrier waveforms between the inverter carrier and dc-dc carrier. This method does decrease the current ripple quite a lot, which is shown in Figure 7.2. In spite of this, more improvement can be made.

In this chapter, a simple carrier modulation method is proposed to reduce the current ripple going through the dc link capacitor. This paper proposes two different kinds of new carrier modulation methods for the dc-dc converter, and concludes to one that is easy to implement, in order to match with the inverter input current so as to minimize the current ripple that going

through the dc link capacitor. Comparing with the conventional triangle carrier, the proposed simple carrier modulation is able to help minimize the current ripple going through the dc link capacitor at unity power factor by a simple and easy implementation without complex close-loop control. The simulation and experimental results are provided to validate the effectiveness of the proposed method.

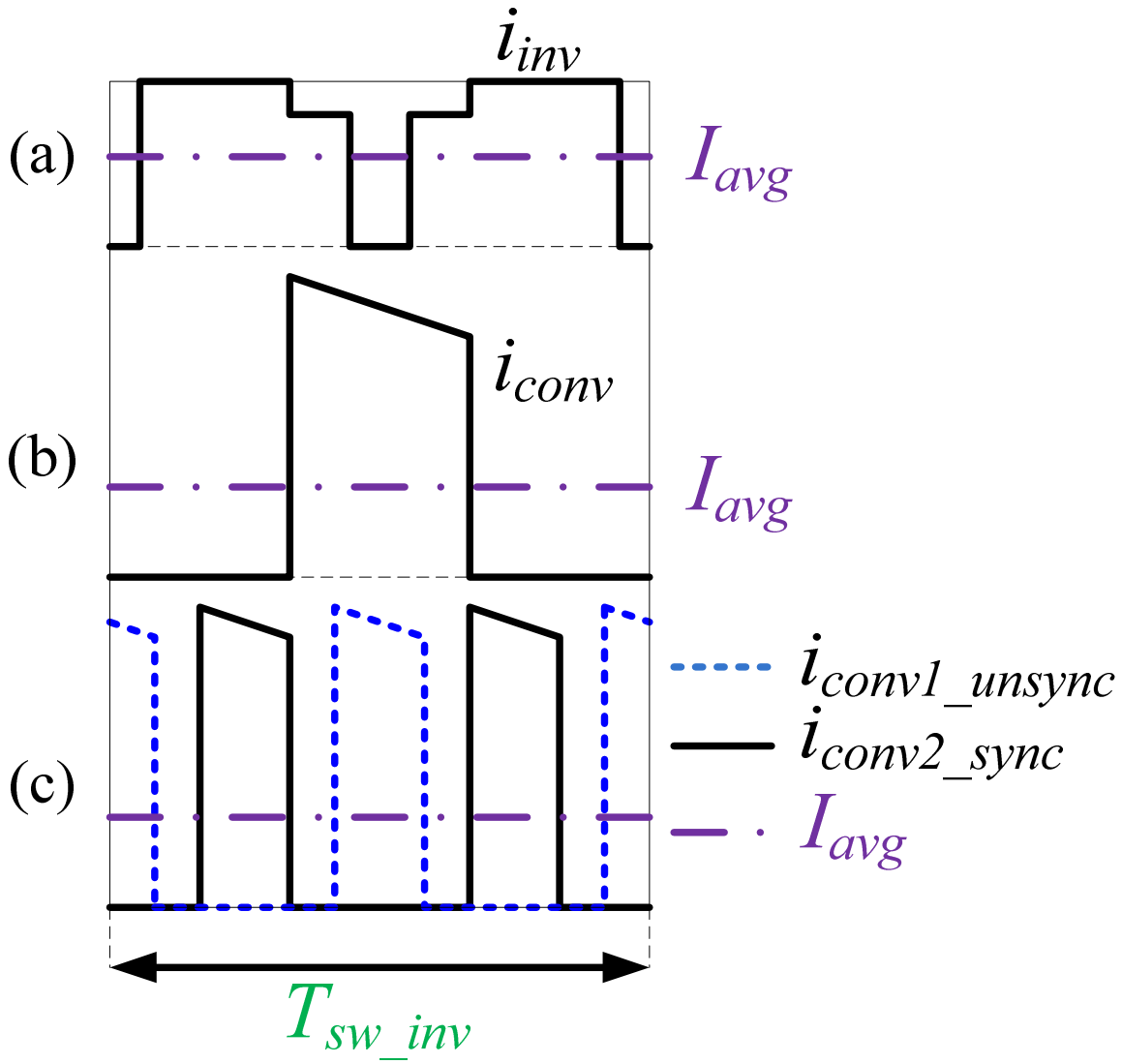


Figure 7.2 (a) One sample switching period of the inverter input current with average current drawn in the same figure; (b) The converter output current ($f_{conv} = f_{inv}$); (c) The converter output currents for unsynchronized case and synchronized case ($f_{conv} = 2 f_{inv}$).

7.2 The Conditions Under Consideration

7.2.1 Unity Modulation Index of the Inverter

Assume the dc-dc converter is working at boost mode; therefore the SPWM inverter operates at unity modulation index to maximize the output voltage. This assumption is made, because common sense states that lowering the voltage by decreasing the modulation index of the inverter is counter-productive, when dc-dc converter is doing boost. However, the method proposed in this paper is still applicable to modulation index other than unity, since different modulation index does not change the positions of the inverter current pulses.

7.2.2 Unity Power Factor of the Load

Depending on motor types and motor operation conditions, the motor power factor can range from 0.6 to unity. In this chapter, it is assumed that the load is at unity power factor, due to the reason that low power factor will result in low dc current, so that benefit of the proposed carrier modulation method will not be significant.

7.2.3 Constant Duty Cycle for the Boost Converter

The duty cycle of the dc-dc converter in every switching cycle is constant in steady state, and assume the dc-dc converter's duty cycle under 2/3, when doing boost. The reasons are as follows. First of all, the constant output voltage of the battery and the desired value of the dc link voltage determines the duty cycle of the dc-dc converter. Secondly, if one keeps the average duty cycle constant, but periodically changes it from cycle to cycle, the inductor current will end up with

much higher low frequency harmonic components, which is absolutely undesired. Therefore, it is better to keep the duty cycle constant in every switching cycle.

7.2.4 Sinusoidal Inverter Output Currents

Since the motors in HEV systems usually behave as huge inductors plus resistors, it is safe to assume that the output current is almost sinusoidal.

7.2.5 Analyze One of Six 60° Sectors

Instead of looking at the whole fundamental period of 360°, it is the same to analyze only 60°, for the reason that the waveforms are repeated at a frequency of 6ω due to the three phases. Therefore, the following analysis will only focus on the range of 30° to 90° (take v_a^* as a reference), where $v_a^* > v_c^* > v_b^*$, shown in pink shaded block in Figure 7.3.

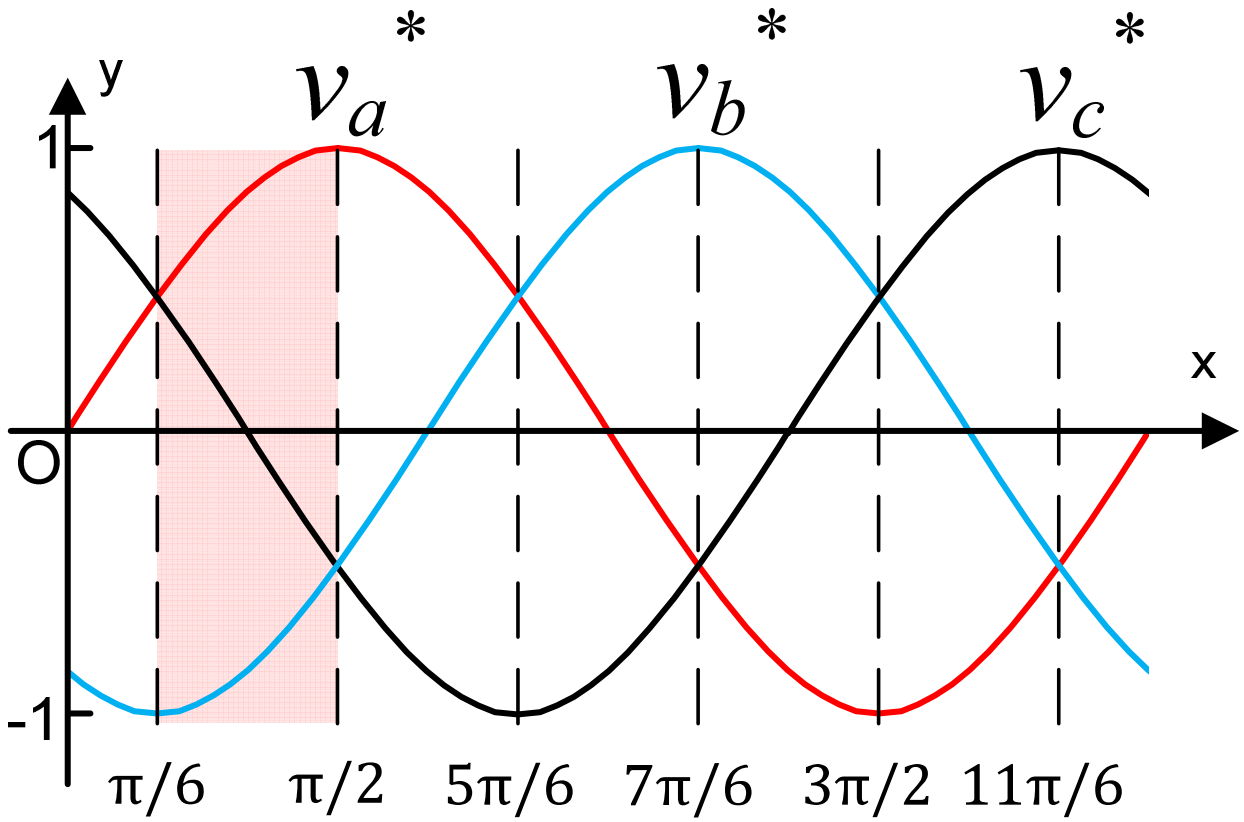


Figure 7.3 Three sinusoidal references v_a^*, v_b^*, and v_c^* of the SPWM inverter with one of the six sectors shown in pink shaded block, which will be discussed in this paper.

7.3 The Analysis of the Ideal SPWM Inverter Input Current Waveform

Figure 7.4 (a) shows the common sinusoidal PWM method for the inverter during the 60° sector ($v_a^* > v_c^* > v_b^*$) that specified in section II. Figure 7.4 (b) demonstrates the trend of the inverter input current's pulse positions within this sector. Each triangle indicates a switching cycle; therefore there are 6 switching cycles in Figure 7.4. From switching cycle No. 1 to No. 6, it can be seen that the two pulses in each switching cycle are shifting from the side to the middle.

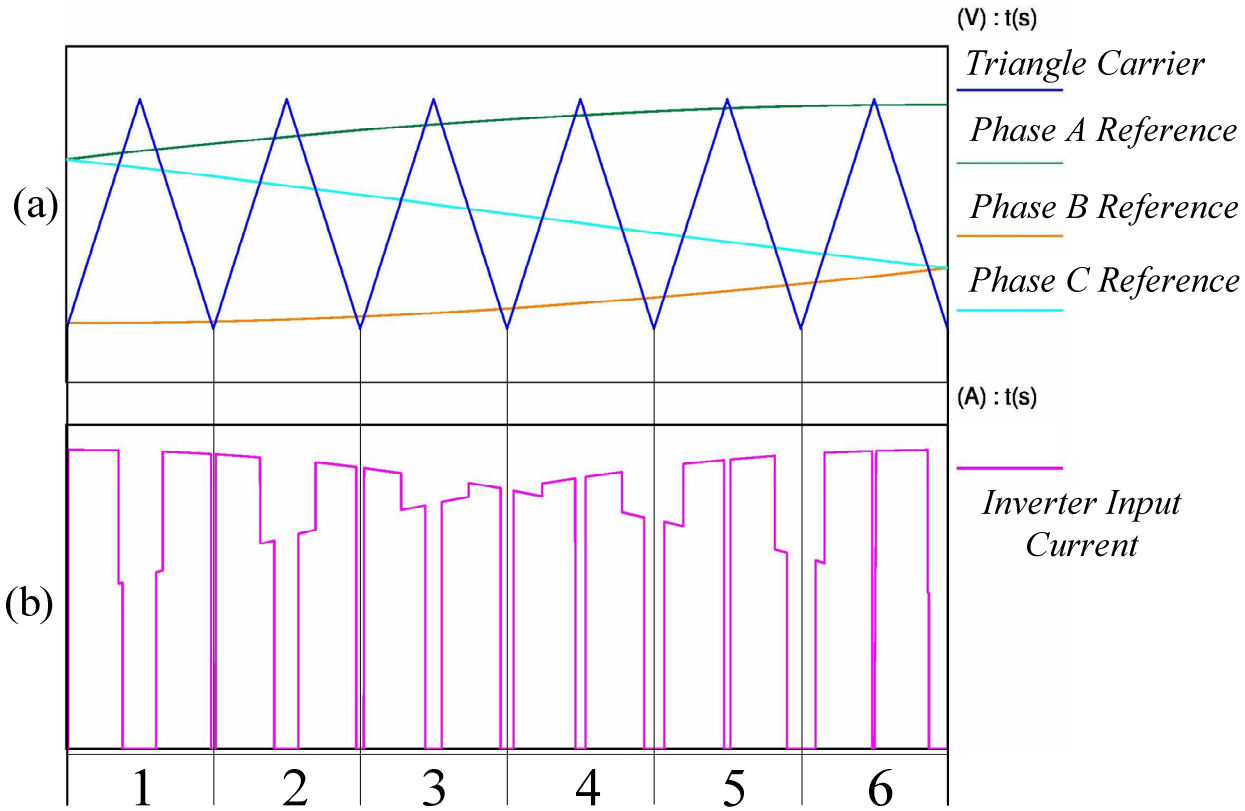


Figure 7.4 (a) Common sinusoidal PWM method for the inverter; (b) Simulation waveform of the inverter input current i_{inv}

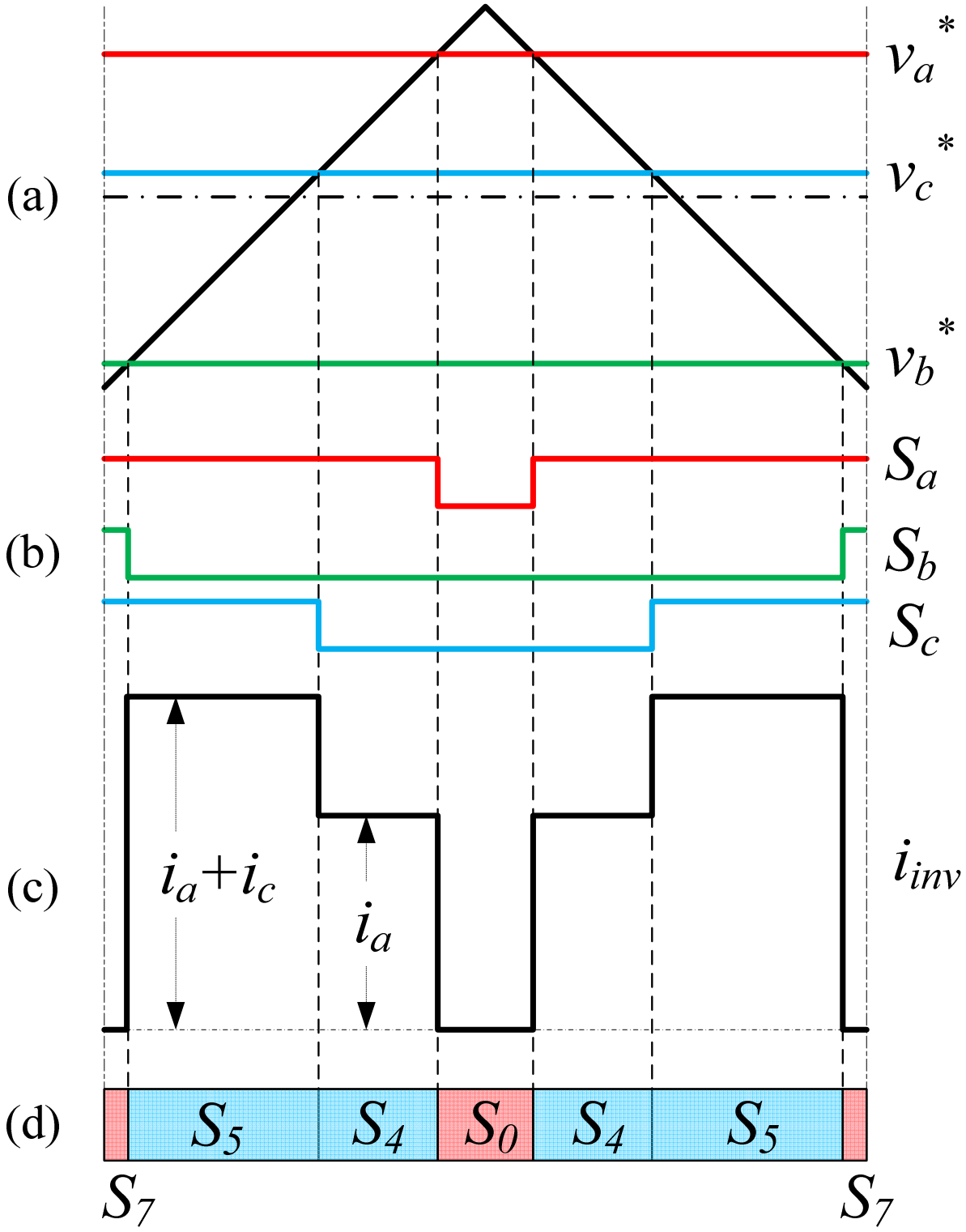


Figure 7.5 Detailed waveforms of SPWM in one switching period. (a) Sinusoidal reference and triangle carrier waveforms; (b) Switching functions S_a, S_b and S_c of phase A, B and C; (c) Ideal inverter input current i_{inv}; (d) Non-zero (active state) and zero (zero state) current portions in blocks.

Figure 7.5 shows the detailed SPWM inverter input current waveform in one switching period during this 60° sector of $v_a^* > v_c^* > v_b^*$. Therefore, v_a^* actually refers to the maximum phase voltage, v_c^* indicating the middle one and v_b^* represents the minimum phase voltage within this sector. It can be seen from Figure 7.5 (d) that the ideal SPWM inverter input current i_{inv} waveform is composed of two parts: the blue blocks indicating the non-zero current portion and the pink blocks stands for the zero current part. The analytical equations respect of the time for each portion can be obtained as shown in (7.1).

$$\begin{aligned} S_0 &= 1 - S_a \\ S_4 &= \frac{1}{2}(S_a - S_c) \\ S_5 &= \frac{1}{2}(S_c - S_b) \\ S_7 &= \frac{1}{2}S_b \end{aligned} \tag{7.1}$$

where S_a, S_b and S_c are the switching functions expressed as in (7.2) [39].

$$\begin{aligned} S_a &= \frac{1}{2} + \frac{1}{2}MI \cdot \sin \omega t \\ S_b &= \frac{1}{2} + \frac{1}{2}MI \cdot \sin(\omega t - \frac{2}{3}\pi) \\ S_c &= \frac{1}{2} + \frac{1}{2}MI \cdot \sin(\omega t + \frac{2}{3}\pi) \end{aligned} \tag{7.2}$$

MI stands for the modulation index and ωt represents the instantaneous time. From Figure 7.5 (c), it can be easily understood that the ideal SPWM inverter input side dc link current waveform i_{inv}, which is ideally expected to be cancelled as much as possible in order to minimize the dc capacitance, is composed of two almost symmetrical pulses. That is why the extended summary [34] made a big step towards minimizing the current ripple of the dc link capacitor by making the converter's switching frequency double that of the inverter switching frequency.

From (1), (2) and Figure 7.4, it is obvious that the zero current portions S_0 and S_7, as shown in the pink blocks in Figure 7.5 (d), are changing with ωt, while the duty cycle of the boost converter is fixed, determined by the battery's current voltage and the required dc link voltage. This conflict cannot be satisfied unless we shift the output converter current pulses left or right to fit the position of the inverter input current pulses. Figure 7.6 shows the trend of the S_0 and $2S_7$ v.s. the degrees. If $1-D$ is between 0.134 and 0.25, where D is the duty cycle of the dc-dc converter, the ripple cancellation will achieve a better result.

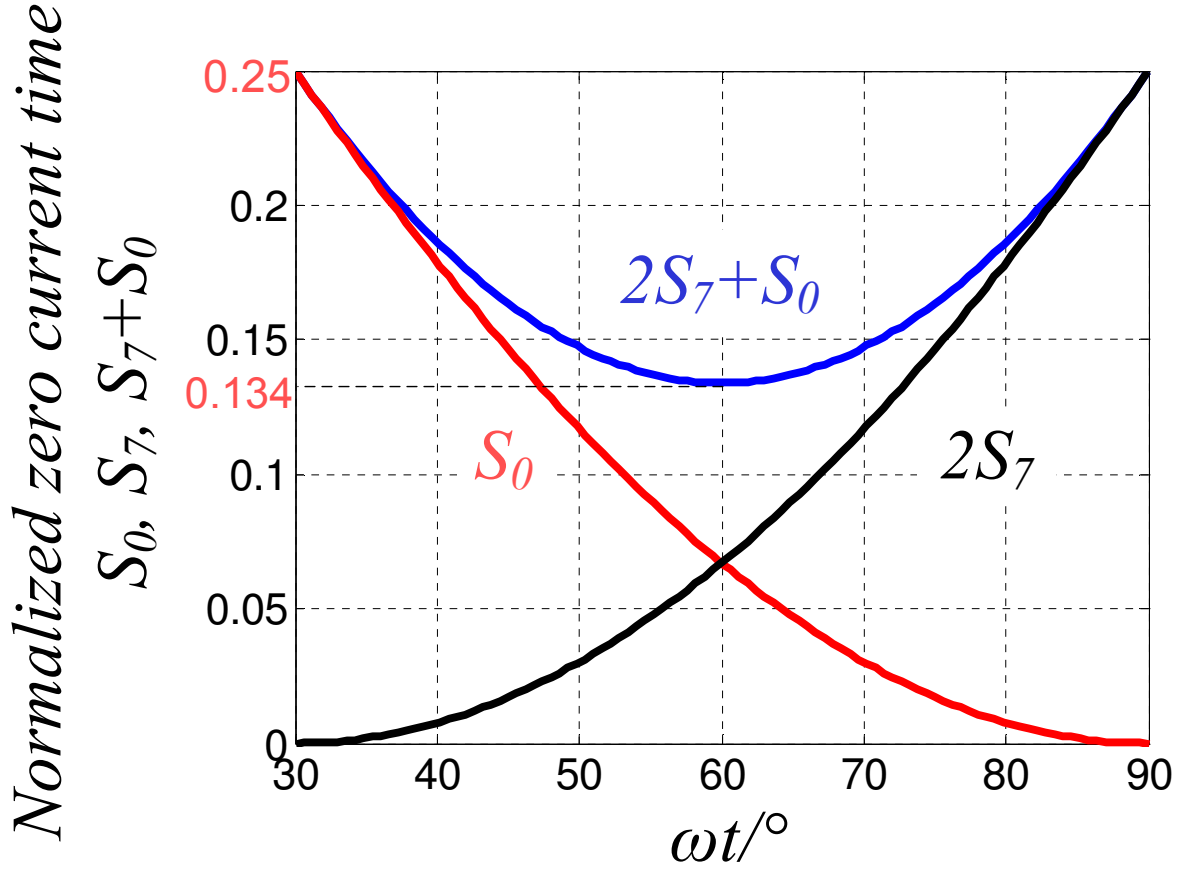


Figure 7.6 The trend of the S_0, $2S_7$, and S_0+2S_7 v.s. ωt

7.4 The Proposed Carrier Modulation Method for the Boost Converter

Considering pulse width modulation, there are usually two things that can be modified, the carrier and the reference. As discussed in section 6.2, the duty cycle of the boost converter is fixed. Hence, it is better to keep the reference as a straight horizontal line, and change the carrier to ensure the fixed duty cycle in each cycle, but at the same time shift the output current pulses of the dc-dc converter left or right to match with the inverter's input current.

In order to match the dc-dc converter output current pulses in Figure 7.2 (c), with the above described inverter input current pulses, there are several ways to generate this modulated carrier. Two of them are listed below as *A* and *B*. Please note that they are different, so that the resulted rms values of the dc link capacitor ripple current are different as well. However, since *A*—the linear method—involves in fewer harmonics, it has lower rms current ripples than the others.

7.4.1 Sine Carrier Modulation Method

If we just consider the middle point X of the left one pulse of the two shown as in Figure 7.7, the function of this shifting actually can be expressed as the length in (7.3).

$$\Delta T = \left(S_7 + \frac{S_5 + S_4}{2} \right) T_{sw} \tag{7.3}$$

where T_{sw} is the inverter switching period and ΔT is defined to be the time length from the starting point of the switching cycle to the above mentioned middle point X. Substitute (7.1) and (7.2) into (7.3) will achieve (7.4).

$$\Delta T = \frac{1}{4}(S_a + S_b)T_{sw} = \frac{T_{sw}}{4}\left[1 + \frac{1}{2}MI\sin\left(\omega t + \frac{\pi}{3}\right)\right] \tag{7.4}$$

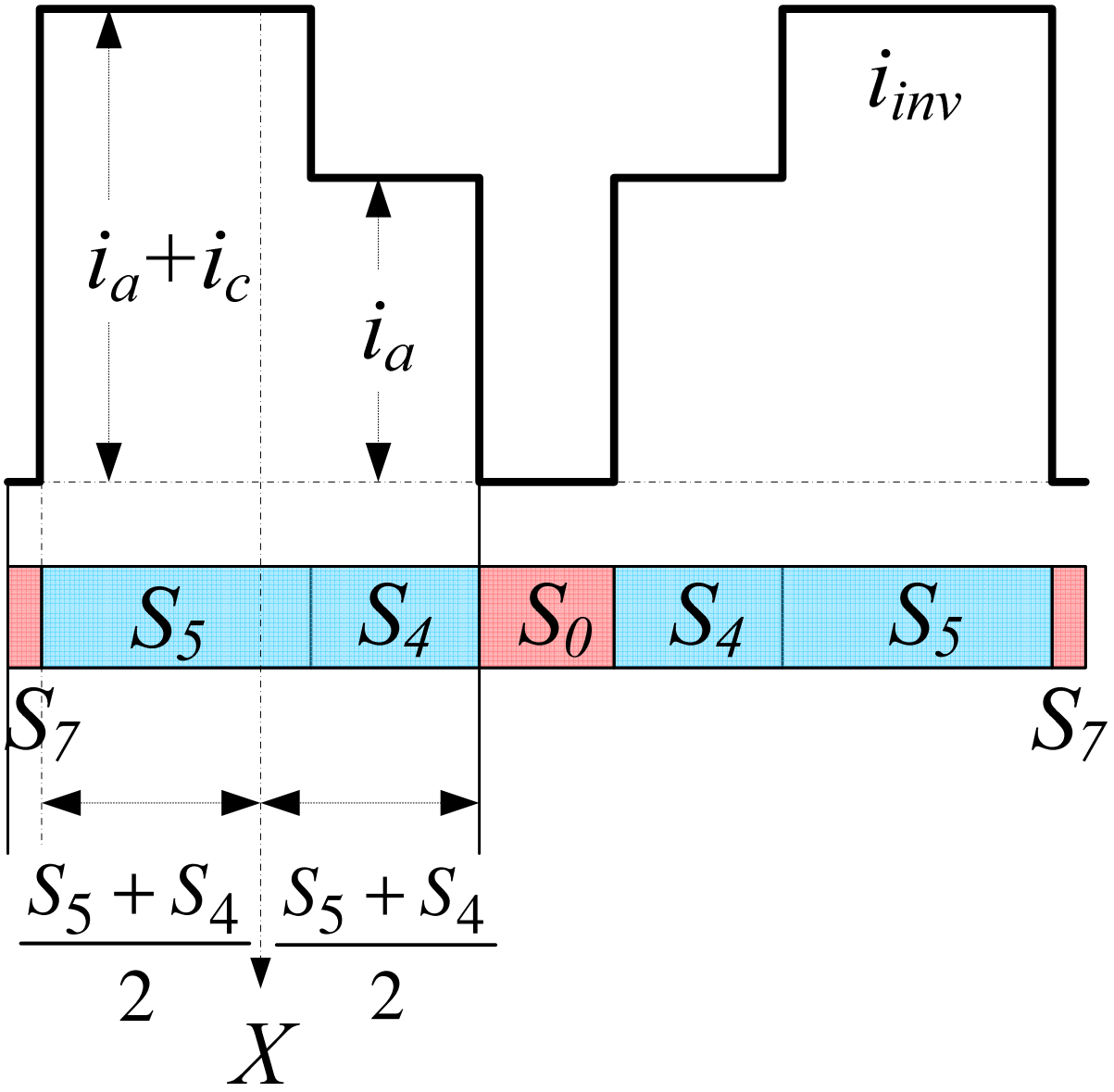


Figure 7.7 Sine carrier modulation method

7.4.2 Linear Carrier Modulation Method

A balanced system indicates that $S_a + S_b + S_c = 0$, therefore, $S_a + S_b = -S_c$. It can be noticed that ΔT in (7.4) is proportional to S_c, where again S_a is the maximum phase voltage, S_b is the minimum phase voltage, and S_c is the middle phase voltage.

As we all know, sine function is approaching linear around zero crossing point. Review Figure 7.3 or Figure 7.4 (a), the middle phase voltage can actually be simplified to a straight line crossing zero. This is the B method—linear carrier modulation method. The mathematical expression is written in (7.5).

$$\Delta T = \frac{T_{sw}}{2}\left(\frac{f_{sw}}{6f_0} - n\right), \quad n = 1, 2, \ldots, \frac{f_{sw}}{6f_0} \tag{7.5}$$

where ΔT is the same meaning as previous one, f_0 is the fundamental frequency, and n is the index number of each switching cycle.

It is quite simple and easy to realize both of them. Taking the sine carrier modulation method as an example, ΔT in (7.4) is actually a part of the sine function for each sector, but is very close to the ΔT in (7.5)—a triangle function. Based on the triangle theory and assuming the amplitude of the triangle carrier is 1, (7.6) and (7.7) are easy to get from observing Figure 7.8, where D is the boost converter's duty cycle. Please note that (7.4) has a minimum and maximum value of [1/4, 3/4], when ωt is between 30° and 90°, which means D in (7.6) and (7.7) can only be between [1/2, 1] to make sure V_x and V_y are between 0 and 1. With the assumption that the boost converter's duty cycle is usually under 2/3, in this case D is limited in the range of [1/2, 2/3]. Finally, the way to get S_{conv} is simply $S_x \oplus S_y$ as shown in Figure 7.8 .

$$\left.\begin{aligned} T_x &= \Delta T - \frac{1-D}{2}\frac{T_{sw}}{2} \\ \frac{T_x}{T_{sw}/2} &= \frac{V_x}{1} \end{aligned}\right\} \Rightarrow V_x = \frac{2\Delta T}{T_{sw}} - \frac{1-D}{2} \tag{7.6}$$

$$\left.\begin{aligned} T_y &= \Delta T + \frac{1-D}{2}\frac{T_{sw}}{2} \\ \frac{T_y}{T_{sw}/2} &= \frac{V_y}{1} \end{aligned}\right\} \Rightarrow V_y = \frac{2\Delta T}{T_{sw}} + \frac{1-D}{2} \tag{7.7}$$

The way to generate the sine carrier modulation is quite similar to [40].

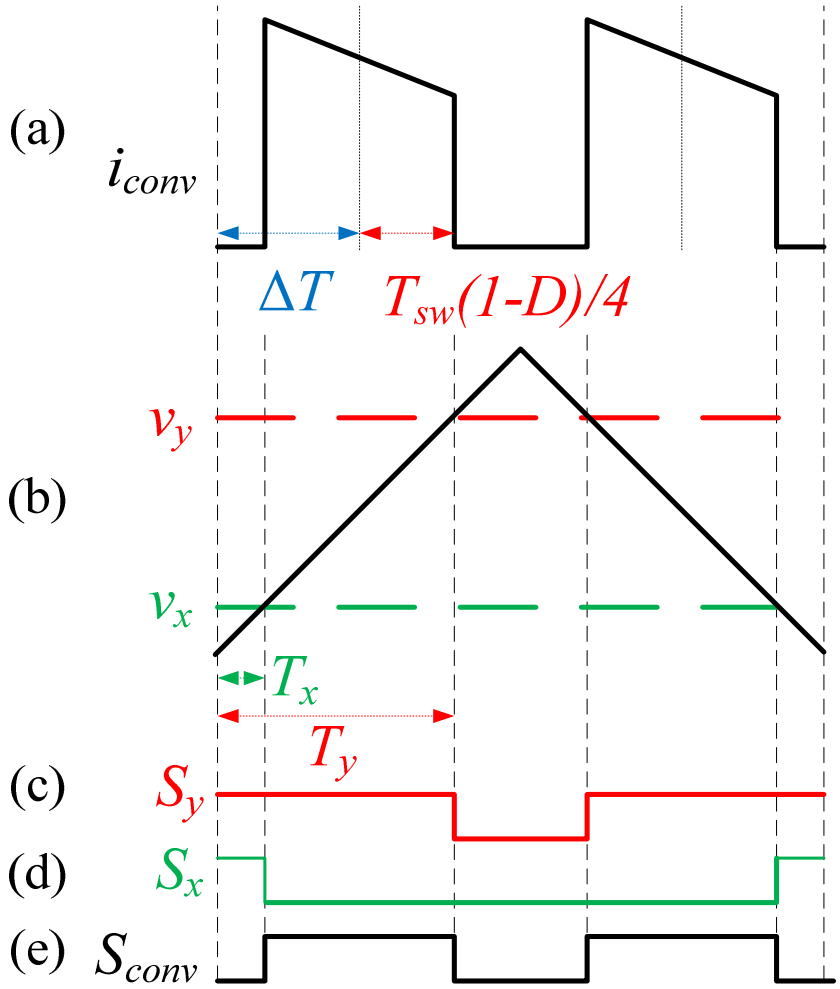


Figure 7.8 (a) The desired converter output current of the dc-dc converter; (b) Two references compared with the triangle carrier for the dc-dc converter; (c) Generated switching function of v_y; (d) Generated switching function of v_x; (e) Generate S_{conv} using $S_x \oplus S_y$

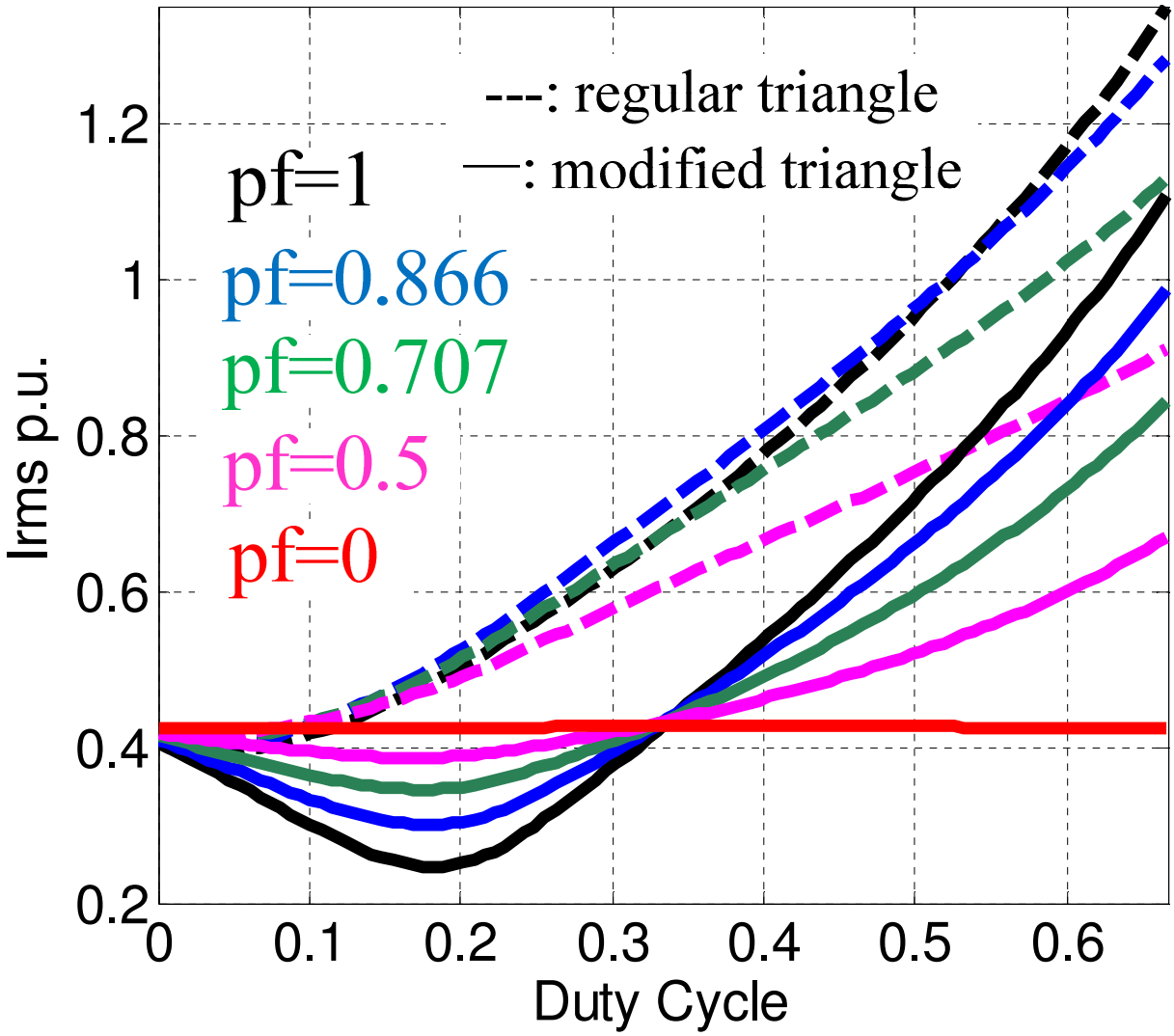


Figure 7.9 The comparison of I_{RMS} between the regular PWM strategy and modified linear carrier modulation method

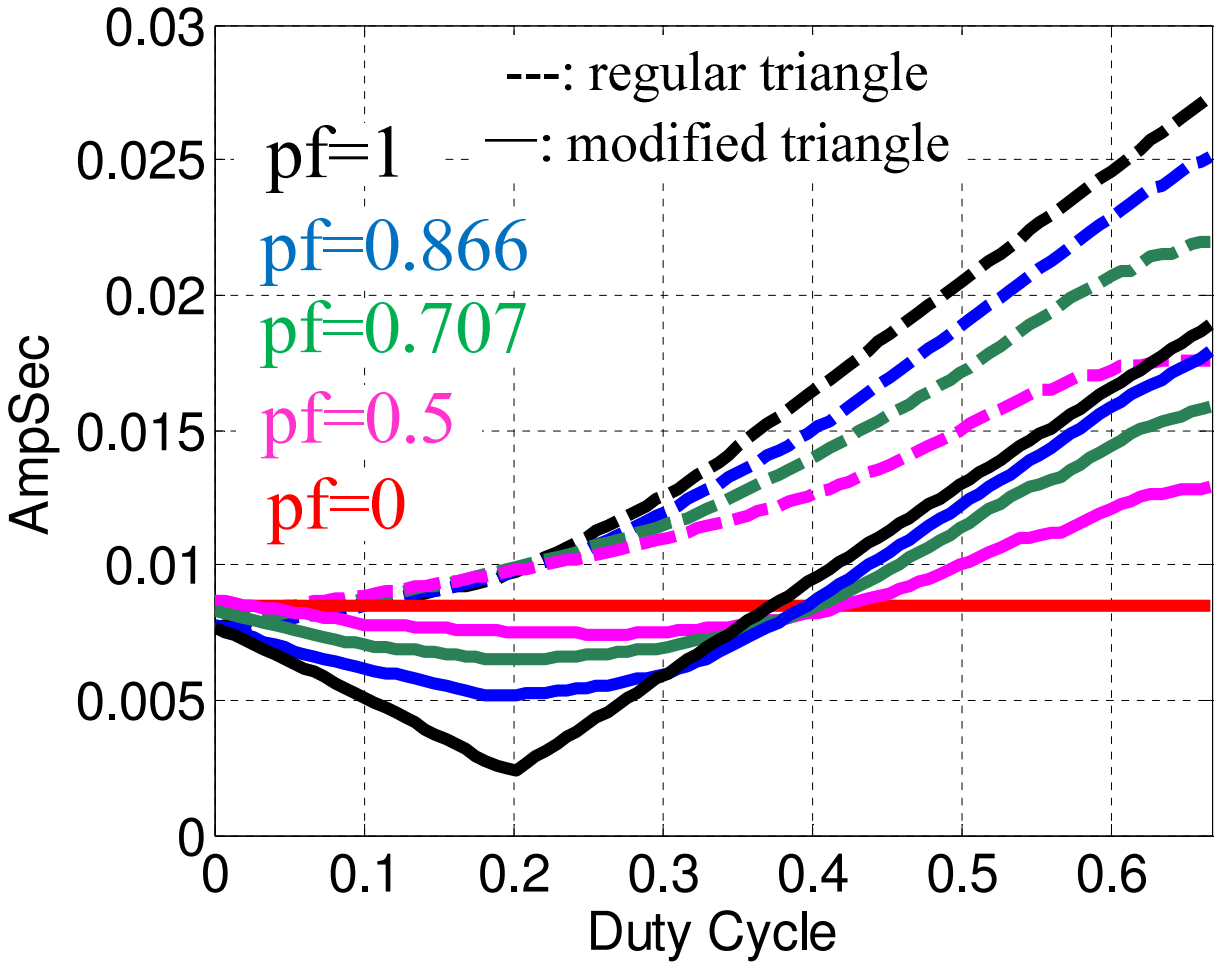


Figure 7.10 The comparison of *A·sec* between the regular PWM strategy and modified linear carrier modulation method

7.5 Theoretical Analysis of DC Link Current Ripple for Sine Carrier Modulation Method

More theoretical analysis is highly desired to prove the effectiveness for many other different conditions.

This section presents the theoretical analysis and experimental verification of the dc link capacitor current ripple reduction using this proposed carrier modulation method, in the HEV dc-dc converter and inverter systems. Detailed analysis and equations are shown for both the dc-dc converter output current waveforms and the SPWM inverter input current waveforms. By subtracting one from the other, the dc link capacitor current waveform is obtained. Thereafter, MATLAB is used to calculate the rms value of this dc link capacitor current waveform. The conclusions are summarized into graphs to show the variation of the rms current ripple changing with the dc-dc converter duty cycle for different load power factors.

In this section, the final goal is to get the expression of the dc link current ripple (i_{cap}) for both the traditional method and carrier modulation method. In order to achieve this goal, it is necessary to get the expressions of the dc-dc converter output current i_{conv} and the SPWM inverter input current i_{inv} respectively. Please note that the carrier modulation method referred in this section is the sine carrier modulation method as explained in the last section.

In Figure 7.4 (a), each triangle indicates a switching cycle. Obviously, there are 6 switching cycles in Figure 7.4. From switching cycle No. 1 to No. 6, it can be seen that the two inverter input current pulses in each switching cycle are shifting from the sides to the middle. Therefore,

in order to cancel out the inverter input current pulses, the desired converter output current should have the similar pattern as shown in Figure 7.4.

7.5.1 Basic Equations

Figure 7.11 shows the details of the realization approach for the carrier modulation method. In order to get the desired dc-dc converter output current shown in Figure 7.11 (a), the switches control signal is generated by two references comparing with the traditional triangle carrier, shown in Figure 7.11 (b), instead of generating a modulated triangle carrier, which requires a lot from a DSP. The final switch control signal is shown in Figure 7.11 (e).

Obviously, there are five time intervals shown in Figure 7.11 (e): T1, T2, T3, T4, and T5. Because of the symmetry and assume the carrier's frequency is much higher than the reference's fundamental frequency, it can be concluded that T1=T5, and T2=T4. Therefore, we can get T1, T2, and T3 as shown in (7.8), (7.9) and (7.10) respectively.

$$T_1 = T_x = \Delta T - \frac{1-D}{4} T_{sw} \tag{7.8}$$

$$T_2 = \frac{1-D}{2} T_{sw} \tag{7.9}$$

$$T_3 = T_{sw} - 2\Delta T - \frac{1-D}{2} T_{sw} \tag{7.10}$$

where $\Delta T = \left(S_7 + \frac{S_5 + S_4}{2} \right) T_{sw}$. Please note that the sine modulation method tries to align the middle of the inverter input current pulses with the middle of the converter output pulses.

Figure 7.5 (c) shows the detailed SPWM inverter input current in one switching period which is in the 60° sector of $v_a > v_c > v_b$. Therefore, v_a refers to the maximum phase voltage, v_c

indicates the medium one and v_b represents the minimum phase voltage. The analytical equations respect of the time for each portion can be obtained as (7.11).

$$\begin{aligned} T_{S_0} &= \frac{1}{2} T_{sw} S_b \\ T_{S_5} &= \frac{1}{2} T_{sw} (S_c - S_b) \\ T_{S_4} &= \frac{1}{2} T_{sw} (S_a - S_c) \\ T_{S_7} &= T_{sw} (1 - S_a) \end{aligned} \tag{7.11}$$

where T_{sw} is the switching period of the inverter, and S_a, S_b and S_c are switching functions expressed as in (7.2).

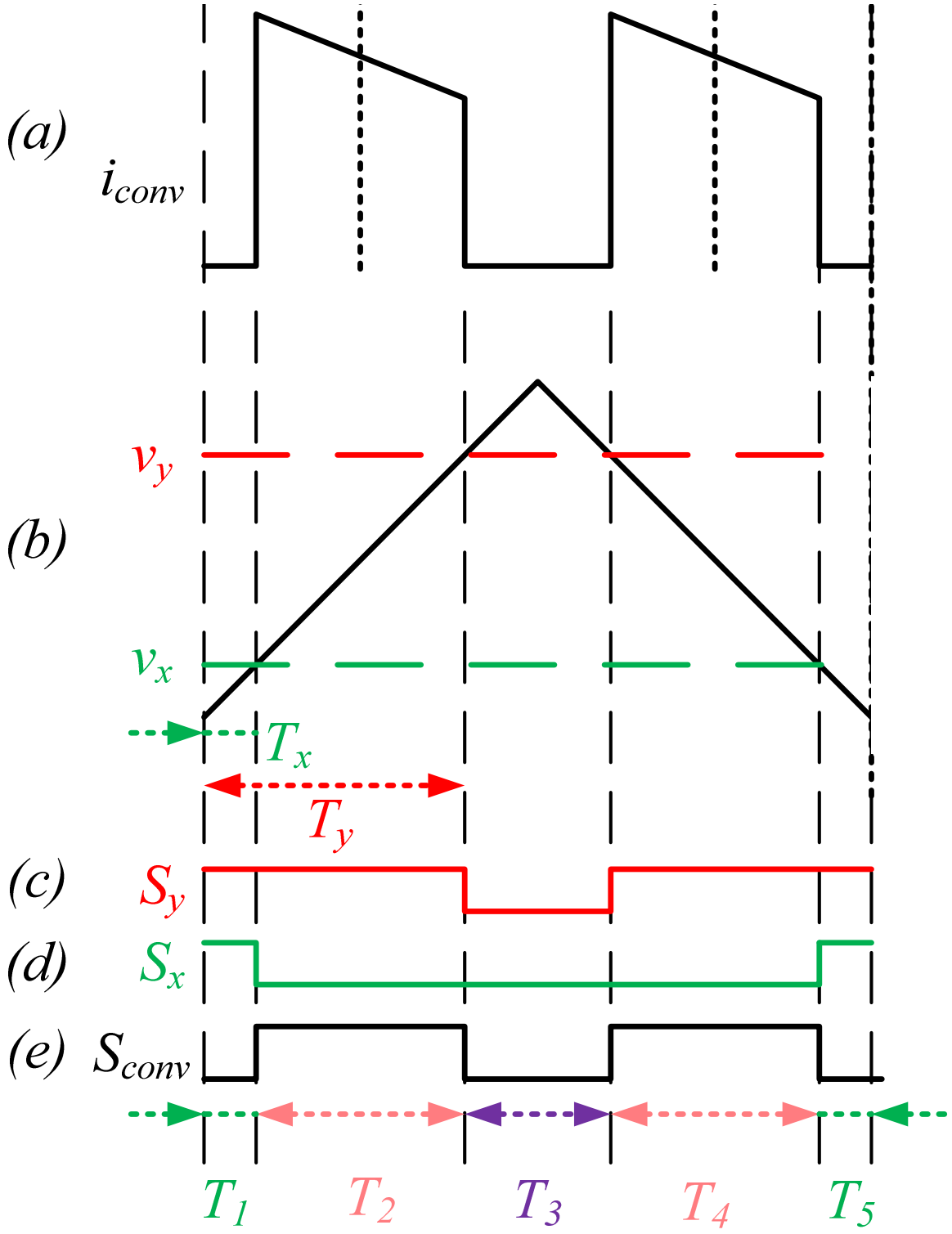


Figure 7.11 (a) The desired dc-dc converter output; (b) The realization approach of the carrier modulation method: two references, instead of only one, compared with the traditional triangle carrier; (c) Generated switching function of v_y from (b);(d) Generated switching function of v_x from (b); (e) Generate S_{conv} by $S_x \oplus S_y$.

7.5.2 Current Ripple Analysis

First of all, obtain the dc-dc converter output current expression, which is a piecewise function as you can see from Figure 7.11 (a). Known that the average of the inductor current I_{avg} is related with the average of the dc-dc converter output current I_{avg_conv} by the duty cycle *D*, as shown in (7.12).

$$I_{avg} = \frac{I_{avg\_conv}}{1-D} \tag{7.12}$$

Due to the conservation of energy, the average of the dc-dc converter output current I_{avg_conv} is equal to the inverter input current I_{avg_inv}, whose expression is shown in (7.13).

$$I_{avg\_inv} = \frac{3\sqrt{2}MI}{4} I_{ac} \cos\phi \tag{7.13}$$

Hence, the inductor average current can be expressed as shown in.

$$I_{avg} = \frac{3\sqrt{2}MI}{4(1-D)} I_{ac} \cos\phi \tag{7.14}$$

Understand that, for every steady-state switching cycle, the inductor current starts with this I_{avg}, and ends with this I_{avg} as well. Therefore, the inductor current expression for the five time intervals are shown below from a to e.

i. During time interval T1

The inductor current has a positive slope, because that the switch is turned on, and the converter input voltage is charging the inductor. The inductor current can be express as shown in (7.15).

$$i_{L\_T1} = I_{avg} + \frac{V_{in}}{L} t \tag{7.15}$$

where $t = [0, T_1]$.

ii. During time interval T2

$$i_{L\_T2} = \left(I_{avg} + \frac{V_{in}}{L} T_1 \right) - \frac{DV_{in}}{(1-D)L} (t - T_1) \tag{7.16}$$

where $t = [T_1, T_1 + T_2]$.

iii. During time interval T3

$$i_{L\_T3} = \left(I_{avg} + \frac{V_{in}}{L} T_1 - \frac{DV_{in}}{2L} T_{sw} \right) + \frac{V_{in}}{L} (t - T_1 - T_2) \tag{7.17}$$

where $t = [T_2, T_3]$.

iv. During time interval T4

$$i_{L\_T4} = \left(I_{avg} + \frac{V_{in}}{L} T_1 - \frac{DV_{in}}{2L} T_{sw} + \frac{V_{in}}{L} T_3 \right) - \frac{DV_{in}}{(1-D)L} (t - T_1 - T_2 - T_3) \tag{7.18}$$

where $t = [T_3, T_4]$.

v. During time interval T5

$$i_{L\_T5} = \left(I_{avg} + \frac{V_{in}}{L} T_1 - \frac{DV_{in}}{2L} T_{sw} + \frac{V_{in}}{L} T_3 - \frac{DV_{in}}{2L} T_{sw} \right) + \frac{V_{in}}{L} (t - T_1 - T_2 - T_3 - T_4) \tag{7.19}$$

where $t = [T_4, T_5]$

7.5.3 Calculation Results

Figure 7.12 shows calculation result (the solid line) and simulation result (six red dots, simulation data are in Table 7.2) of the current ripple per unit value vs. duty cycle under test condition but varies the duty ratio. Figure 7.13 shows the comparison of the capacitor current ripple per unit value between the regular PWM strategy (dash line) and modified carrier modulation method (solid line) (black: p.f.=1, blue: 0.866; green: 0.707; magenta: 0.5; red: p.f.=0.)

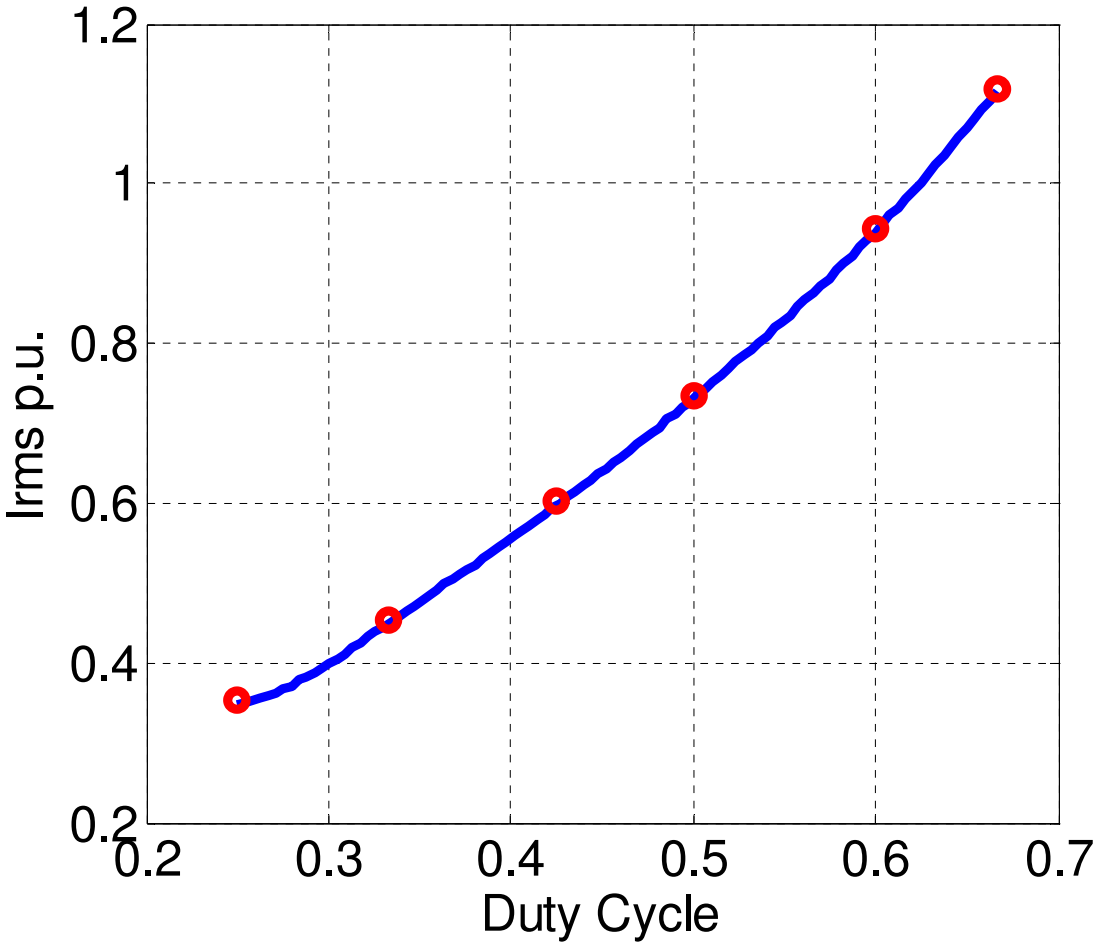


Figure 7.12 Calculation result and simulation result of the capacitor current ripple per unit value v.s. duty cycle under test condition

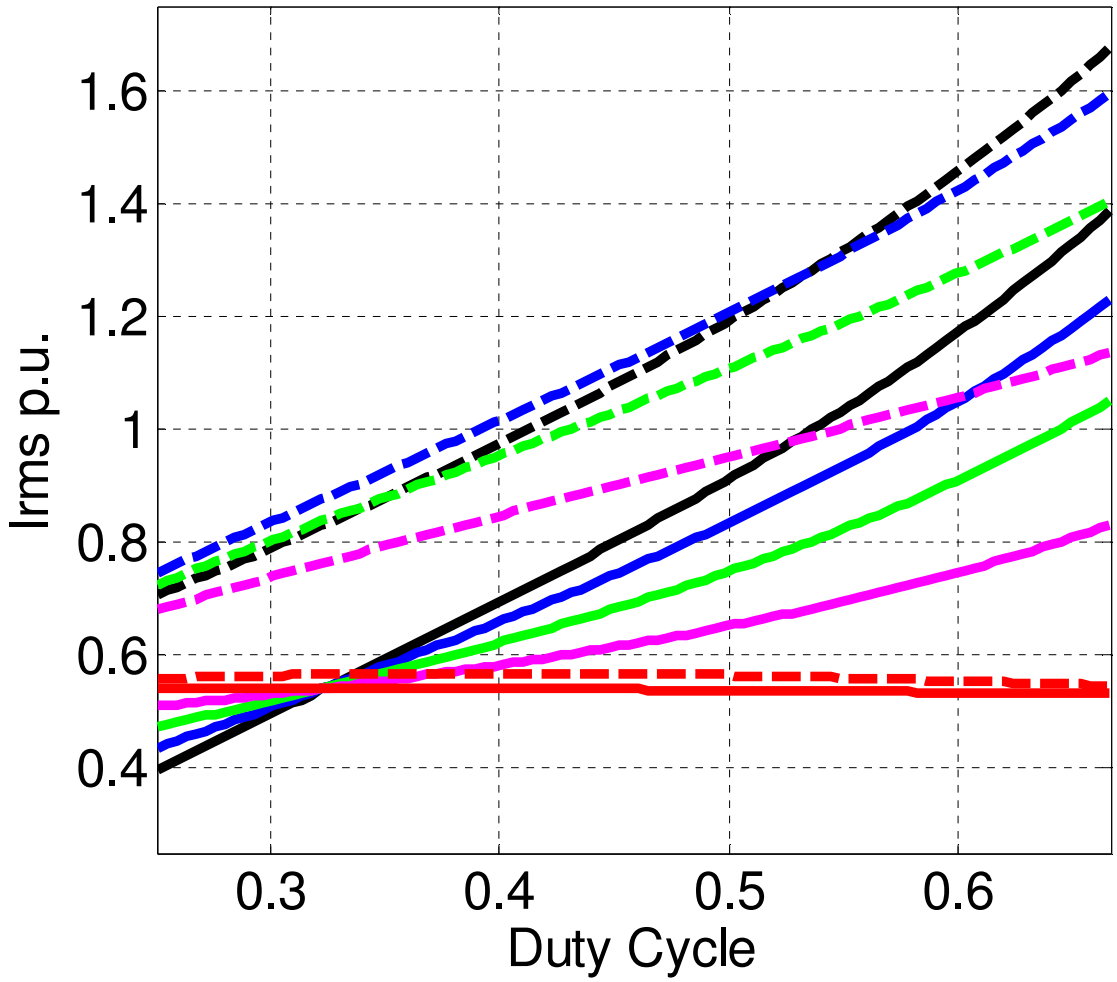


Figure 7.13 The comparison of the capacitor current ripple per unit value between the regular PWM strategy (dash line) and modified carrier modulation method (solid line)

Table 7.1 Circuit Parameters and Experimental Conditions

DC-DC converter input voltage	V_{in}	200 V
DC-DC converter duty cycle	D	1/3
DC link voltage	V_{dc}	300 V
DC-DC converter inductance	L	180 uH
DC link capacitor	C	510 uF
Inverter switching frequency	f_{sw}	10.8 kHz
Equivalent converter switching frequency	f_{sw_conv}	21.6 kHz
Fundamental frequency	f	60 Hz
Load power factor	$cos\varphi$	0.884
Load	Z	2.5 Ω + 3.5 mH
Modulation index	MI	0.92

Table 7.2 Simulation Data

D	**Vin (V)**	**Icap_rms (A)**	**Iac (A)**	**p.u.=Irms/Iac**
0.25	225	12.1273079	34.40646281	0.352471801
0.333	***200***	***15.63728678***	***34.3981922***	***0.45459618***
0.425	172.5	20.67948663	34.38478368	0.601413893
0.5	150	25.21480867	34.36809767	0.733669024
0.6	120	32.3776283	34.32988761	0.943132371
0.667	100	38.33122442	34.28333922	1.118071498

7.6 Experimental Results

The experiment was conducted under the following conditions: the dc-dc input voltage is 200 V generated by a three-phase diode rectifier with a large electrolytic capacitor bank, dc-dc converter duty cycle is 1/3, the dc link voltage is 300 V, the inverter switching frequency is 10.8 kHz, the equivalent dc-dc converter switching frequency is 21.6 kHz, the fundamental frequency is 60 Hz, and the p.f. is around 0.884 with a 3.5 mH inductor and a 2.5 Ω resistor in series connected in wye. The inverter is operated under the SPWM normal modulation method with a modulation index of 0.92.

One thing has to be mentioned here: since the inverter's dc link capacitor banks are connected to the IGBT pack through busbars, which preventing direct measurement of the inverter input current, the same thing on the converter side. Therefore, the inverter current is obtained by (7.20) based on measurement of the output currents and switching signals from the DSP, while the converter output current is obtained by (7.21).

$$i_{inv} = S_a i_a + S_b i_b - S_c (i_a + i_b) \tag{7.20}$$

$$i_{conv} = S_{conv} i_L \tag{7.21}$$

This requires at least 2 current sensors and 3 voltage sensors for the inverter input current measurement and 1 current sensor and 1 voltage sensor for the converter output current measurement. The available oscilloscopes have 4 analog channels with enough digital inputs, however, the math function (7.22) cannot apply to the already calculated i_{inv} and i_{conv}. Therefore, the experimental results that have more than 3 waveforms on the same graph are done by saving "waveform"—data file *.wvf*—on the oscilloscope and redrawn on the computer by *WVF Viewer* software from Yokogawa.

$$i_{cap} = i_{conv} - i_{inv} \tag{7.22}$$

Table 7.3 shows the saber simulation of the four different modulation methods. First one is the original method with the same switching frequency for both the converter and inverter. Second is that the converter switching frequency is twice as much as the inverter switching frequency. Third method is, based on second one, shift the converter output current pulses using linear carrier modulation method proposed in this paper. The last one is the sine carrier modulation method. It can be seen that the linear carrier modulation method achieves the best result, and around 17%~20% reduction of the current ripple based on the second method is made.

Table 7.3 Saber Simulation Result of The rms Value of The DC Link Capacitor's Ripple Current

Condition	I_{cap_rms}
$f_{conv} = f_{inv}$	*26.531 A*
$f_{conv} = 2f_{inv}$	*19.271 A*
$f_{conv} = 2f_{inv}$ with linear carrier modulation	*15.656 A*
$f_{conv} = 2f_{inv}$ with sine carrier modulation	*15.704 A*

Figure 7.14 Shows the experimental results of the rms ripple current of the dc link capacitor is 15.651 A at 300 V dc link voltage, and it is highly agreed with the SABER simulation in table I row 3. Figure 7.15 shows the synchronized the inverter phase A reference signal (yellow) with the converter V_x and V_y low frequency triangle reference signal (V_x is green and V_y is Purple). The ripples on these signals are due to the reason that they are got from the PWM signals after a low pass RC filter. Figure 7.16 shows the S_x , S_y and S_{conv} for the proposed linear carrier

modulation method. It can be seen that the switching signal of S_{conv}, achieved by $S_x \oplus S_y$, is shifting its pulses in one inverter switching cycle left and right. Figure 7.17 shows how the converter output current is gotten from (7.21). Digital and analog signals are separated by the oscilloscope automatically. Figure 7.18 and Figure 7.19 show the how the inverter input current is gotten from (7.20). Figure 7.20 and Figure 7.21 show the capacitor current got from (7.22) with the converter output current and the inverter input current, for comparison. Finally, Figure 7.22 gives the SABER simulation for a comparison with Figure 7.21. The simulation result and the experimental result are very similar, and the only difference is the experimental result has a 6ω component involved in the converter output current due to the diode rectifier at the input side.

Group1 Trigger Time: 10/07/22 22:14:43 Number of Data: 10020

	I_inv	I_conv	I_cap
Max	43.85254E+00 A	55.56641E+00 A	79.47754E+00 A
Min	-32.22656E+00 A	0.000000E+00 A	-43.73535E+00 A
High	43.37704E+00 A	54.41340E+00 A	53.88007E+00 A
Low	-7.061005E-03 A	0.000000E+00 A	-7.233532E+00 A
P-P	76.07910E+00 A	55.56641E+00 A	123.2129E+00 A
Ampl	43.38411E+00 A	54.41340E+00 A	61.11360E+00 A
Avg	26.06004E+00 A	26.11510E+00 A	54.39223E-03 A
Rms	31.00015E+00 A	32.65733E+00 A	15.65157E+00 A
Middle	5.812988E+00 A	27.78320E+00 A	17.87109E+00 A
StdDev	16.789	19.608	15.651
Oshoot	1.10 %	2.12 %	41.89 %
Ushoot	74.27 %	0.00 %	59.73 %
Rise	0.0000 s	0.0000 s	24.999us
Fall	0.0000 s	24.999us	19.999us
Freq	11.111kHz	28.571kHz	10.526kHz
Period	90.000us	35.000us	95.000us
+Duty	77.78 %	85.71 %	5.26 %
-Duty	22.22 %	14.29 %	94.74 %
+Width	70.000us	29.999us	4.9999us
-Width	19.999us	4.9999us	90.000us

Figure 7.14 The experimental result of the rms ripple current is 15.651 A at 300 V dc link voltage (Analyzed from the saved data by WVF Viewer from Yokogawa)

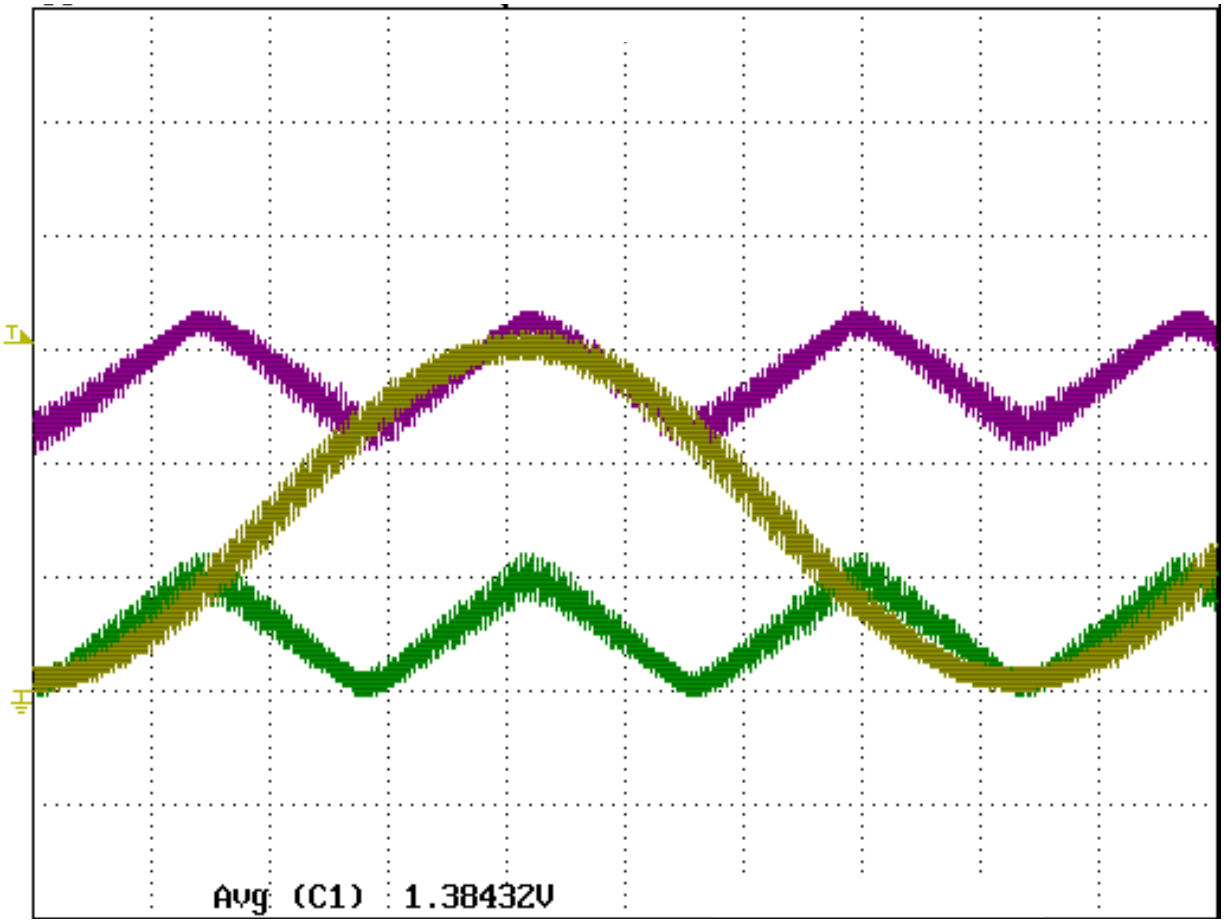


Figure 7.15 Synchronized the inverter phase A reference signal (yellow) with the converter V_x and V_y low frequency triangle reference signal (V_x is green and V_y is Purple)

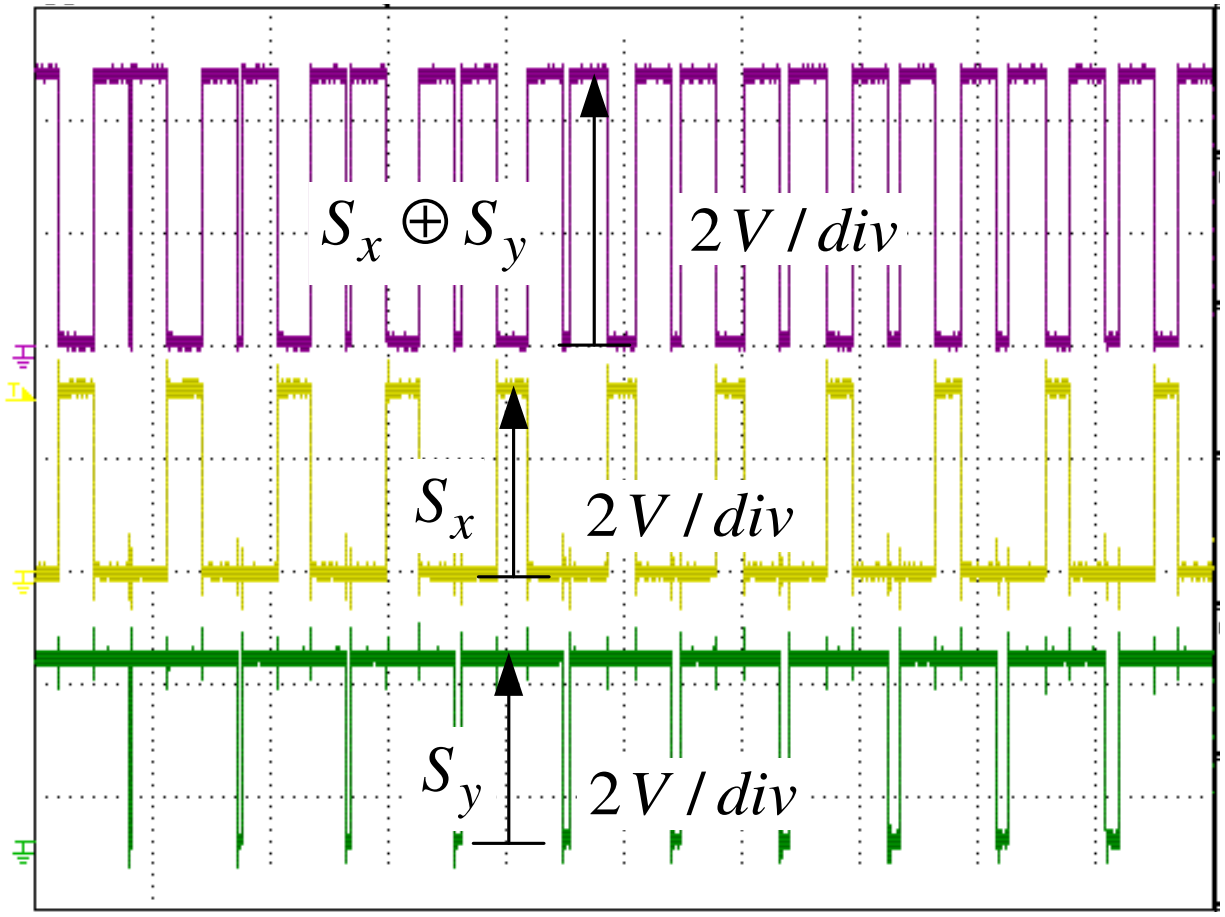


Figure 7.16 The experimental result of the proposed carrier modulation signal for dc-dc boost converter

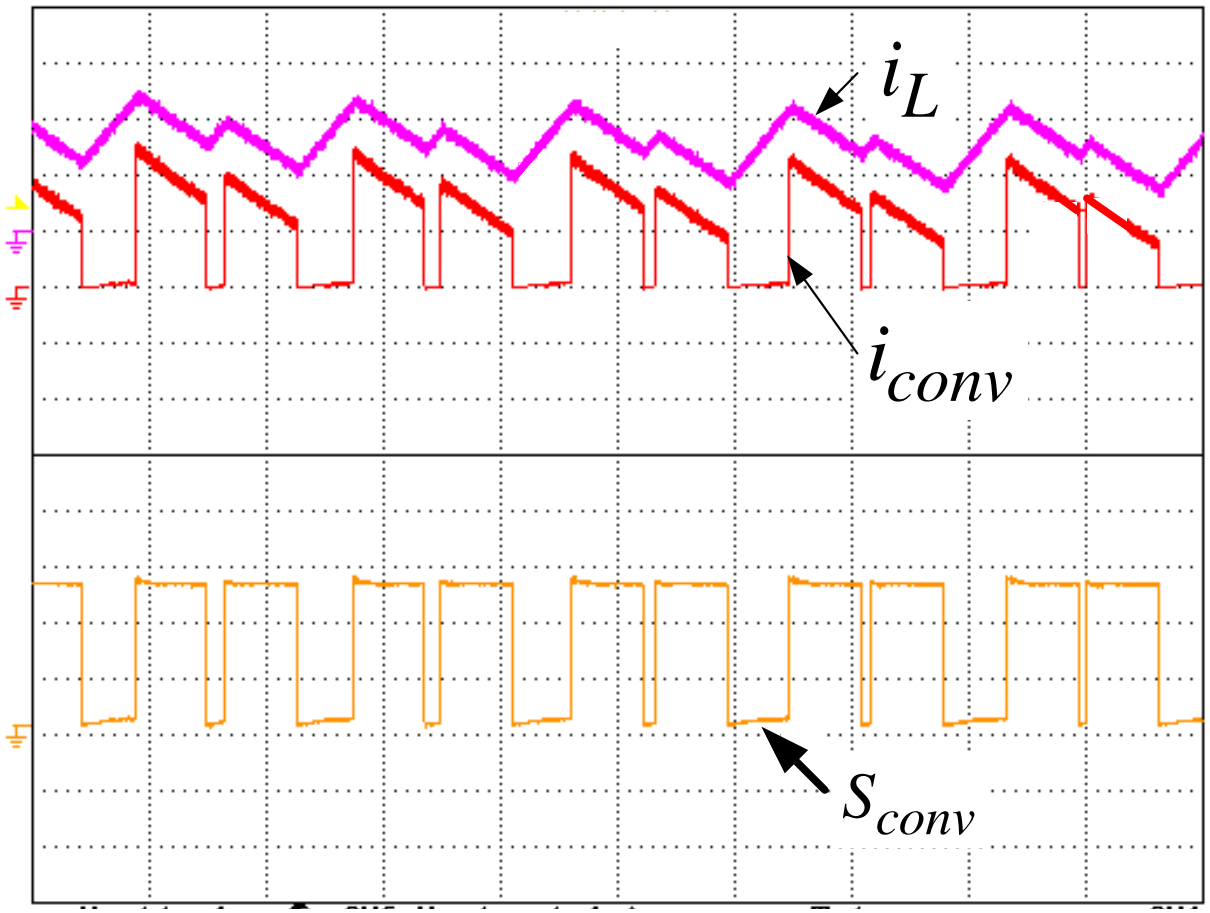


Figure 7.17 The experimental results of the inductor current, the converter output current and the switching signal of the dc-dc boost converter

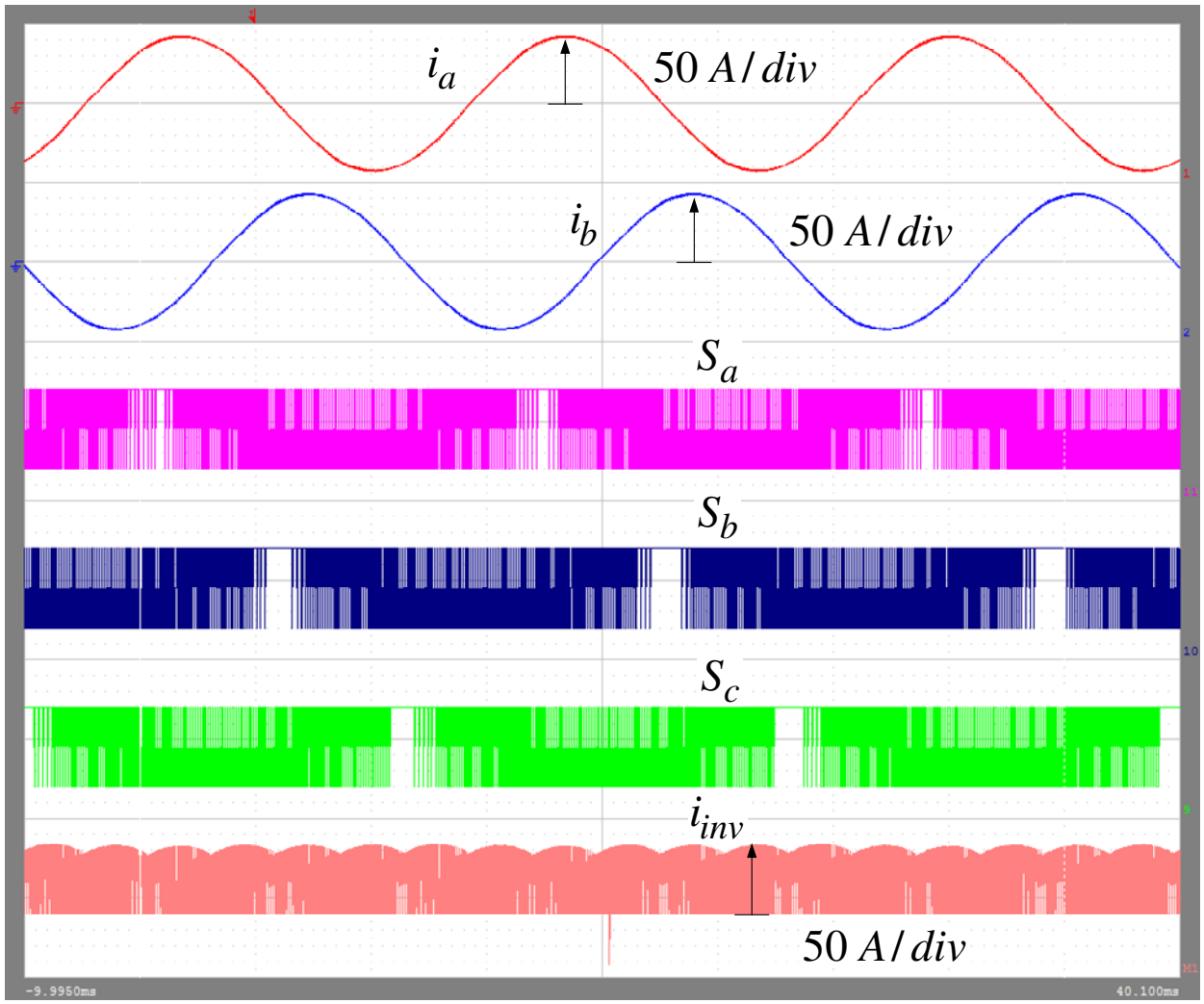


Figure 7.18 The experimental results of the inverter output currents, the switching functions, and the input current of the SPWM inverter (Redraw the waveforms from the saved data by WVF Viewer from Yokogawa)

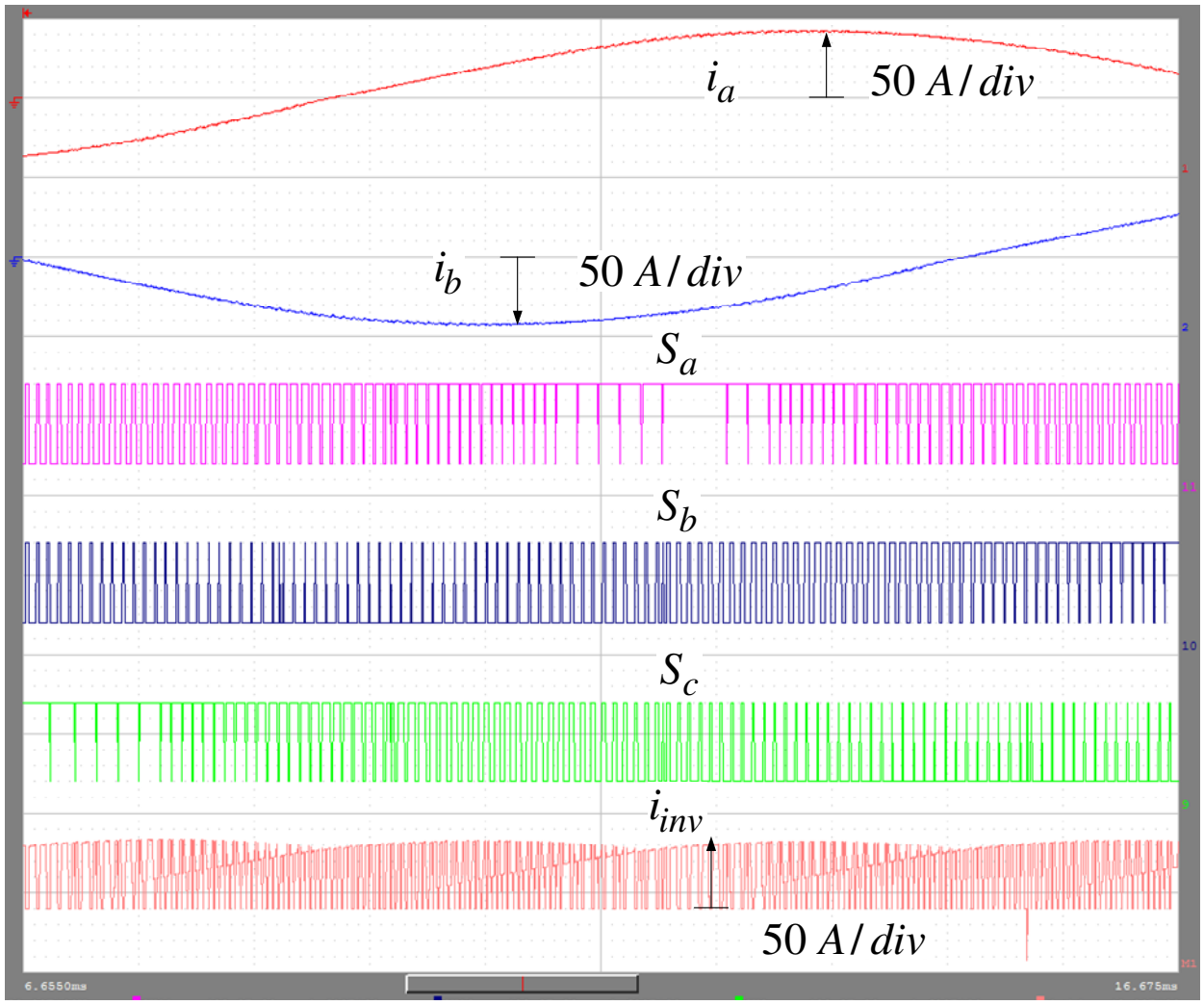


Figure 7.19 Zoom in view of Figure 7.18

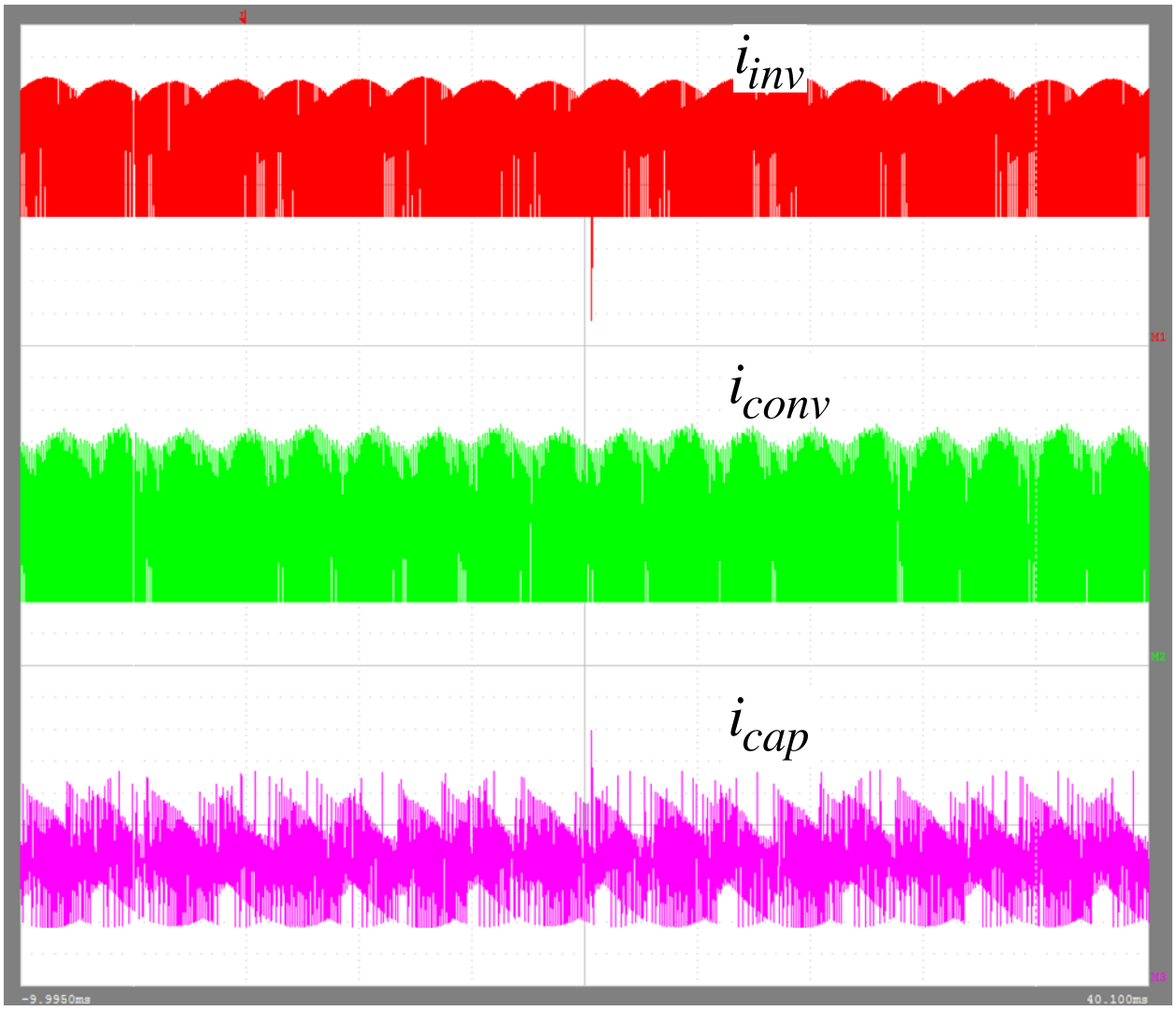


Figure 7.20 Experimental results of the inverter input current, the converter output current, and the DC link capacitor current (Redraw the waveforms from the saved data by WVF Viewer from Yokogawa)

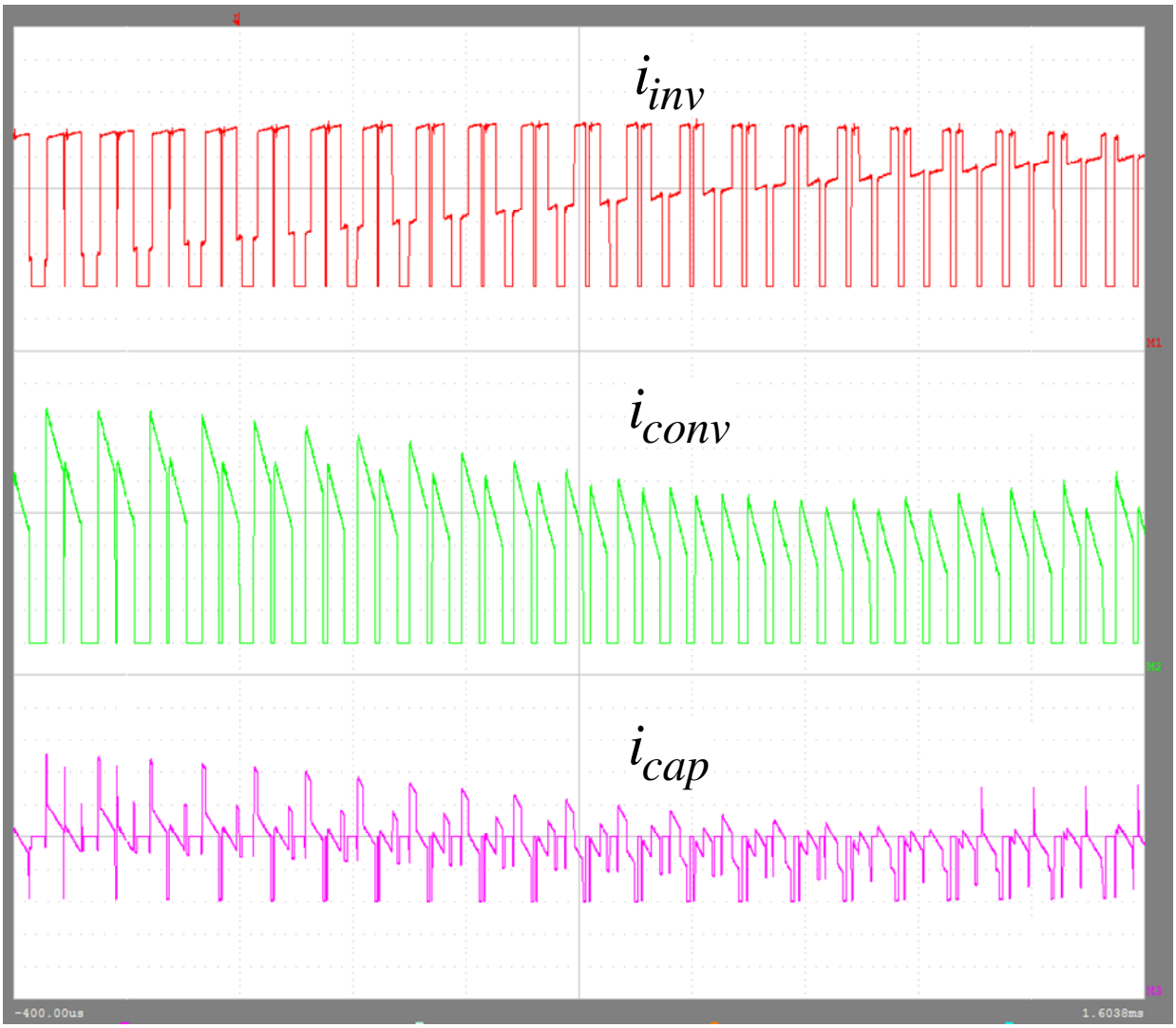


Figure 7.21 Zoom in of Figure 7.20.

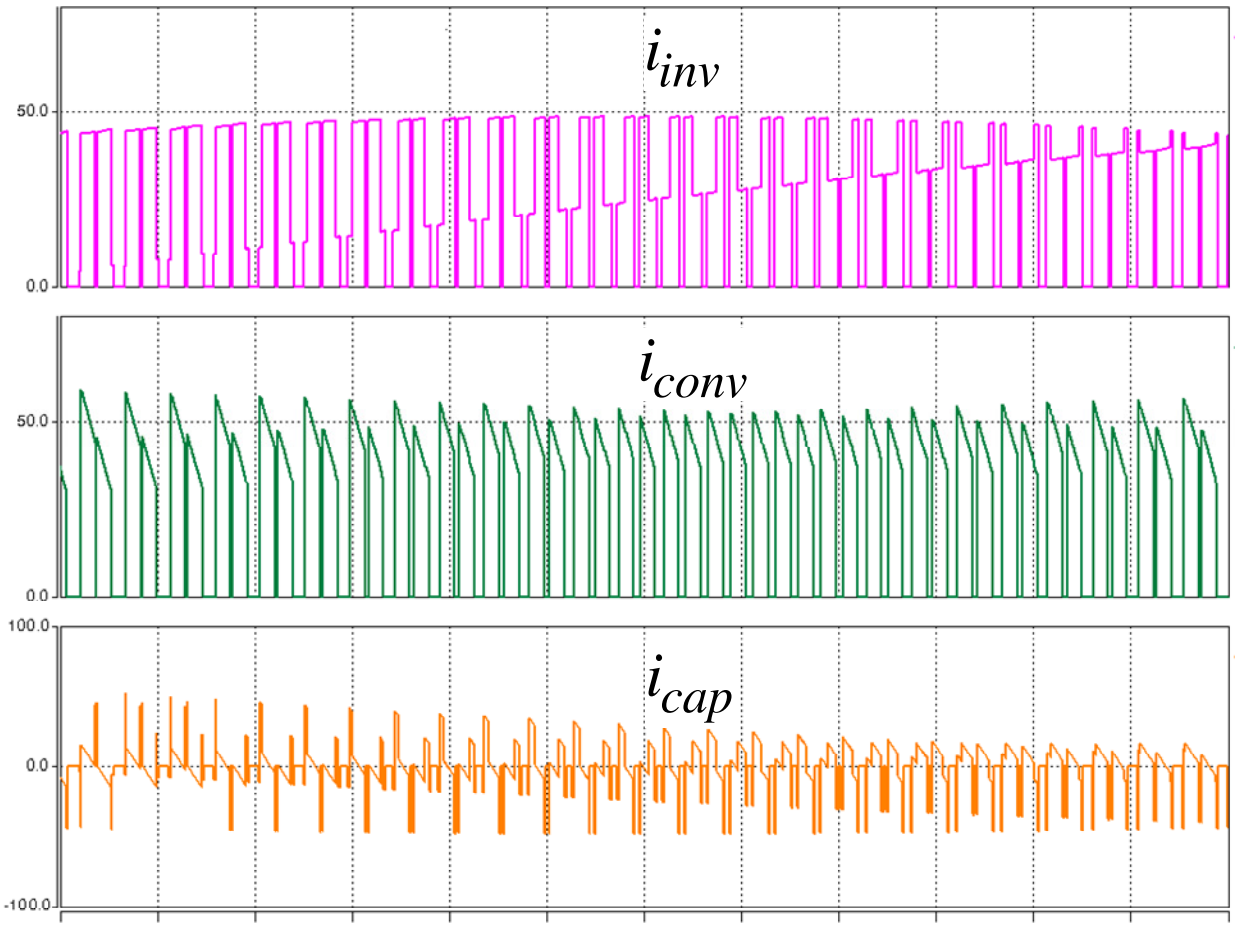


Figure 7.22 The SABER simulation results of the dc link capacitor current (comparison for Figure 7.21)

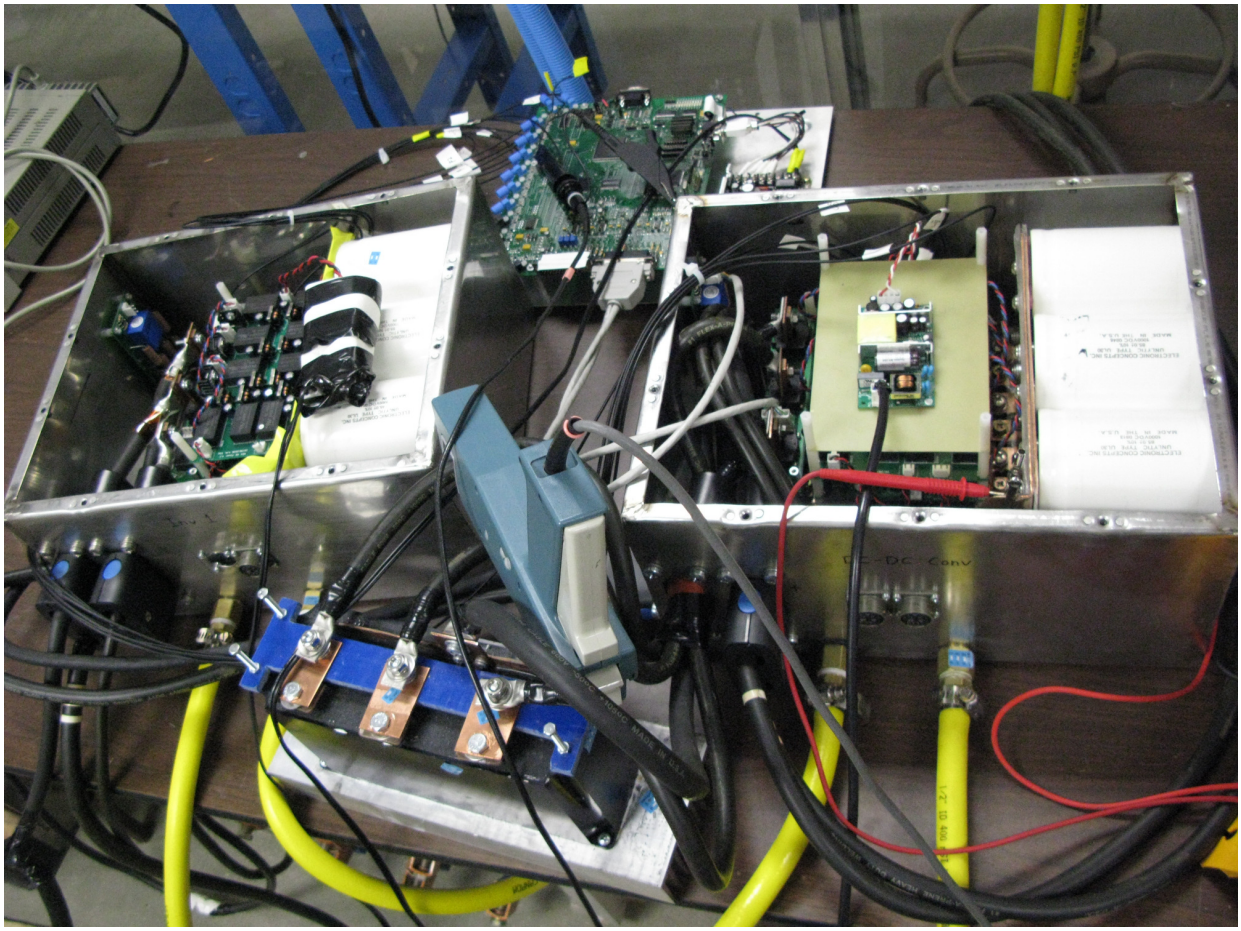


Figure 7.23 Prototype setup

7.7 Conclusion

Around 17%~20% reduction of the current ripple based on the already reduced current ripple in [34] is realized by using the proposed carrier modulation method, which leads to the minimization of the dc capacitance. Due to the reduced current ripple, the voltage ripple of the dc link is reduced as well. The proposed method has the merits of simple and easy realization. There is no requirement of any fast feedback and complicated close-loop control blocks, but gives significant dc link ripple reduction and dc link capacitance minimization.

CHAPTER 8 Minimizing DC Capacitance Requirement of Cascaded H-Bridge Multilevel Inverters for Photovoltaic Systems by 3rd Harmonic Injection

8.1 Introduction

As the demand of the renewable energy increases every year, the photovoltaic (PV) systems have been playing an important part in supplying energy for the global consumption. In order to connect those PV modules to supply power to the grid without inserting any bulky low frequency step-up transformers, the cascaded H-bridge multilevel inverters are utilized to increase the output voltage up to the grid voltage, which is tens of kilovolts. Therefore, no bulky low frequency transformer is needed.

The cascaded H-bridge multilevel inverters have been introduced for more than 20 years, and are widely used in the high voltage and high power applications. Various studies have been done for this special category, such as topology research and development [41-51], power flow management [52], and performance-improving control methods [53-66]. However, none of them has ever focused on the reduction of the dc link capacitor—one of the biggest components in the whole system. The reason for this inevitable huge dc link capacitor is that it has to absorb a low

frequency current ripple that is twice as much as the fundamental frequency (noted as 2ω), in order to maintain the dc link voltage ripple under a certain value. Due to this huge low frequency current ripple, the dc link capacitor bank is accordingly bulky, heavy and expensive. Hence, minimizing this dc link capacitor becomes an essential step towards developing and manufacturing compact, light and low cost cascaded H-bridge multilevel inverters with long life and high reliability.

This chapter proposes a 3rd harmonic injection method that achieves a 40% to 50% reduction of the dc link capacitance, meaning a great reduction to the capacitor size, weight and cost. This 3rd harmonic injection will not cause any problem for the 3-phase cascaded H-bridge multilevel inverter, because the 3rd harmonic currents cannot flow. On the other hand, by injecting this 3rd harmonic, it is able to generate a negative 2ω component, which is able to cancel fully or part of the 2ω component that generated by the traditional SPWM method. The percentage of the capacitance reduction depends on the fundamental modulation index. Theoretical analysis and simulation results are demonstrated to prove the effectiveness of the proposed method.

8.2 Theoretical Analysis of the DC Capacitance Reduction

8.2.1 System Configuration

Figure 8.1 shows the schematic of the cascaded H-bridge multilevel inverter with separate photovoltaic sources, which needs a huge dc link capacitor banks for each module. This dc link capacitor is supposed to absorb the current ripple from both the photovoltaic source side and the H-bridge inverter side.

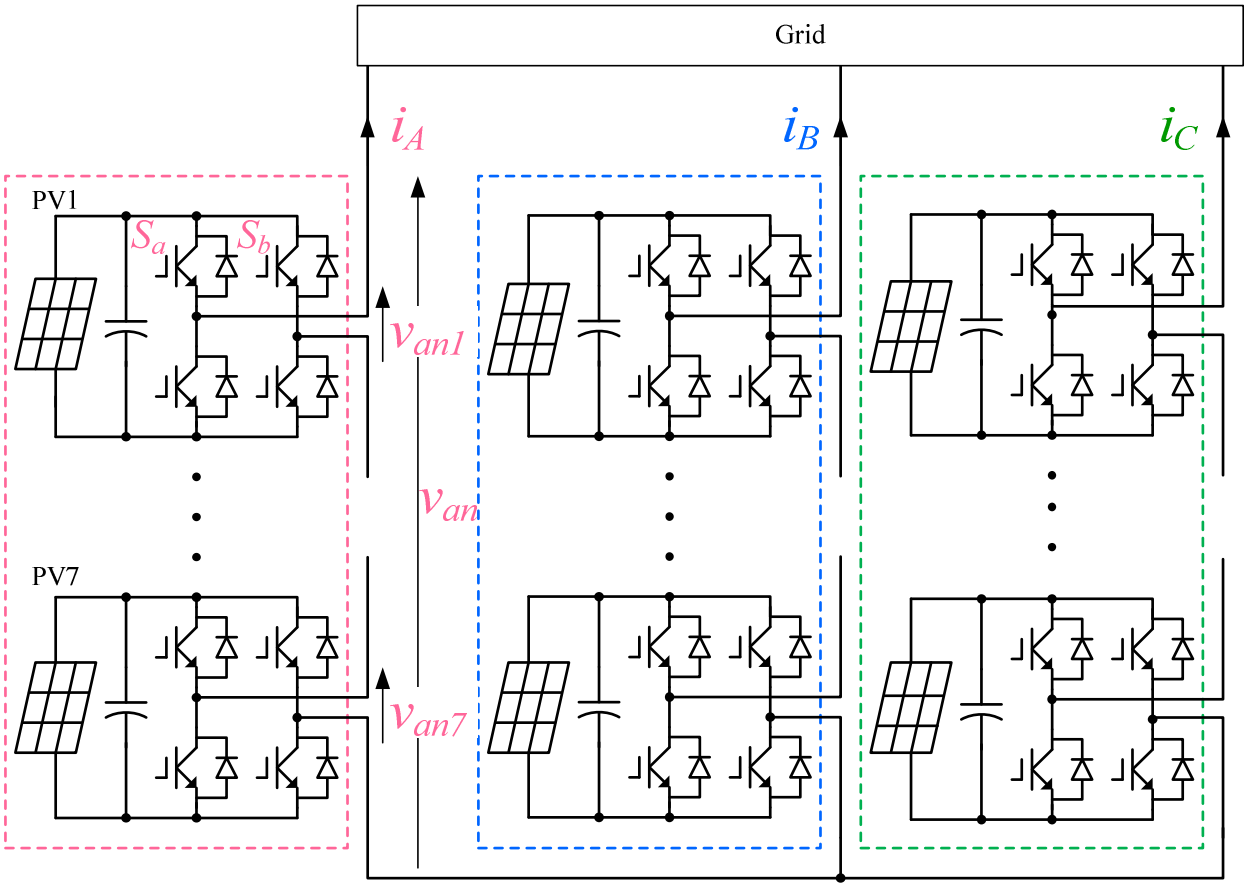


Figure 8.1 The system schematic of the 2.1 MVA three-phase cascaded H-bridge multilevel inverter with separate photovoltaic sources.

Considering photovoltaic sources usually have a quite smooth output current, the majority of the current ripples for the dc link capacitor to absorb come from the inverter side. This current ripple i_d can be expressed as:

$$i_d = (S_a - S_b) i_A \tag{8.1}$$

where S_a and S_b are the switching functions of the top switches for each phase leg within one module operated by the traditional SPWM method, and i_A is the line current of phase A, as shown in Figure 8.2.

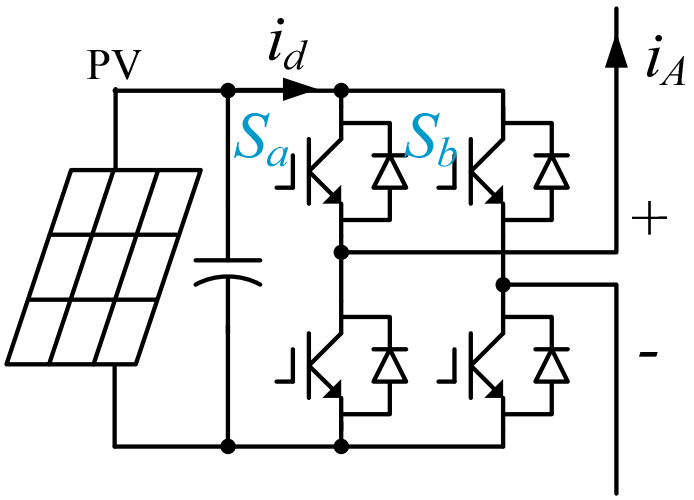


Figure 8.2 The schematic of one H-bridge module with notations

Due to the cascaded multilevel structure, the output voltage with many voltage levels has fewer harmonics, which leads to an almost sinusoidal output current without any filtering. Therefore, it is reasonable to assume i_A to be sine shaped, with a power factor angle of φ as shown in (8.2).

$$i_A = \sqrt{2} I_A \sin(\omega_0 t + \varphi) \tag{8.2}$$

8.2.2 DC link current ripple without 3rd harmonic injection

According to [67, 68], without 3rd harmonic injection, the switching functions S_{a0} and S_{b0} of phase A and phase B can be written as below.

For phase A,

$$S_{a0} = \frac{1}{2} + \frac{1}{2} M_0 \sin(\omega_0 t) \tag{8.3}$$

and for phase B,

$$S_{b0} = \frac{1}{2} + \frac{1}{2} M_0 \sin\left(\omega_0 t - \pi\right) \tag{8.4}$$

Substitute (8.2), (8.3) and (8.4) into (8.1), it is able to obtain (8.5).

$$\begin{aligned} i_d &= \sqrt{2} I_A \sin\left(\omega_0 t + \varphi\right)\left[M_0 \cos\left(\omega_0 t - \frac{\pi}{2} \right)\right] \\ &= \sqrt{2} I_A \frac{M_0}{2}\left[\sin\left(2\omega_0 t + \varphi - \frac{\pi}{2} \right) + \sin\left(\varphi + \frac{\pi}{2} \right)\right] \end{aligned} \tag{8.5}$$

Obviously, without injecting the 3rd harmonic component, i_d contains a 2ω component with an amplitude of $\sqrt{2} M_0 I_A / 2$, as the first term shows in (8.5).

8.2.3 DC link current ripple with 3rd harmonic injection

If the 3rd harmonic component is injected into the system with amplitude of M_3, the switching functions for the two phase-legs are changed into (8.6)

$$S_{a3} = \frac{1}{2} + \frac{1}{2} M_3 \sin\left(3\omega_0 t\right) \tag{8.6}$$

And (8.7)

$$S_{b3} = \frac{1}{2} + \frac{1}{2} M_3 \sin\left(3\omega_0 t - \pi\right) \tag{8.7}$$

respectively.

Therefore, the H-bridge dc side input current i_d can be expressed as

$$i_d = \left(S_{a0} + S_{a3} - S_{b0} - S_{b3}\right) i_A \tag{8.8}$$

which can be calculated by substitute (8.2), (8.3), (8.4), (8.6) and (8.7) into (8.8).

$$
\begin{aligned}
i_d &= \left[M_0 \cos\left(\omega_0 t - \frac{\pi}{2} \right) + M_3 \cos\left(3\omega_0 t - \frac{\pi}{2} \right) \right] \times \sqrt{2} I_A \sin\left(\omega_0 t + \varphi \right) \\
&= \sqrt{2} I_A \left\{ \begin{array}{l} \frac{1}{2} M_0 \sin\left(2\omega_0 t - \frac{\pi}{2} + \varphi \right) + \frac{1}{2} M_0 \sin\left(\frac{\pi}{2} + \varphi \right) \\ + \frac{1}{2} M_3 \sin\left(4\omega_0 t - \frac{\pi}{2} + \varphi \right) - \frac{1}{2} M_3 \sin\left(2\omega_0 t - \frac{\pi}{2} - \varphi \right) \end{array} \right\}
\end{aligned} \tag{8.9}
$$

The first term showing in (8.9) indicates that the 2ω component can be completely cancelled out, as long as the 3rd harmonic injection's magnitude M_3 is made to be the same as the fundamental's magnitude M_0. Plus, the phase angle of the output current has to be in phase with the voltage, meaning unity power factor. Assume the 2ω component is completely cancelled, the amplitude of the 4ω component is going to be $\sqrt{2} M_3 I_A / 2$.

However, there is a maximum modulation index for the inserted 3rd harmonics, since the sum f of the fundamental and the 3rd harmonic has to be within the range of [-1, +1].

$$
f = M_0 \sin \omega_0 t + M_3 \sin 3\omega_0 t \tag{8.10}
$$

Hence, two unknowns, ωt and M_0 (or M_3), can be calculated, based on two independent equations shown below in (8.11).

$$
\left\{ \begin{array}{l} \frac{df}{dt} = \frac{d}{dt} \left(M_0 \sin \omega_0 t + M_3 \sin 3\omega_0 t \right) = 0 \\ M_0 = M_3 \end{array} \right. \tag{8.11}
$$

The solutions are as follows.

$$
\left\{ \begin{array}{l} \cos \omega_0 t = \sqrt{\frac{2}{3}} \\ \sin \omega_0 t = \sqrt{\frac{1}{3}} \\ M_0 = M_3 = \frac{3\sqrt{3}}{8} \end{array} \right. \tag{8.12}
$$

Eq. (8.12) means that in order to completely cancel out the 2ω harmonic component in i_d, the maximum fundamental modulation index can go up to $3\sqrt{3}/8$, which is about 0.6495, by injecting the same amplitude of the 3rd harmonic component. At the same time, the total waveform after combining the 1st and 3rd component reaches 1 at $\omega_0 t = arc\cos\sqrt{2/3}$. and the lowest harmonic component in the dc current ripple increases from 2ω to 4ω. This frequency increase is the key factor of reducing the dc capacitor size.

8.2.4 Current ripple and voltage ripple reduction

According to the expression of the required capacitance shown in (8.13).

$$C = \frac{i_d \Delta t}{\Delta v} \tag{8.13}$$

When M_0=M_3=0.6495, the reduction of the dc capacitance reaches maximum, and can be calculated based on the relationship shown in (8.14), comparing to without the 3rd harmonic injection:

$$\begin{cases} \dfrac{i_d'}{i_d} = \dfrac{\frac{1}{2}M_3}{\frac{1}{2}M_0} = \dfrac{\frac{3\sqrt{3}}{8}}{1} \\ \dfrac{\Delta t'}{\Delta t} = \dfrac{1}{2} \end{cases} \tag{8.14}$$

Assume keeping the voltage ripple as before, the requirement of the dc capacitance can be 1/2 of the original requirement, which is a 50% reduction. As the fundamental modulation index goes up, higher than 0.6495, the magnitude of the 3rd harmonic injection is reduced accordingly to ensure the combined waveform is no greater than 1. When the modulation index reaches 0.9,

the dc link capacitor still can achieve a 42% reduction by injecting a magnitude of 0.486 of the 3rd harmonic to the fundamental.

The maximum 3rd harmonic injection is shown in Figure 8.3 for fundamental modulation index ranging from 0 to 1.15.

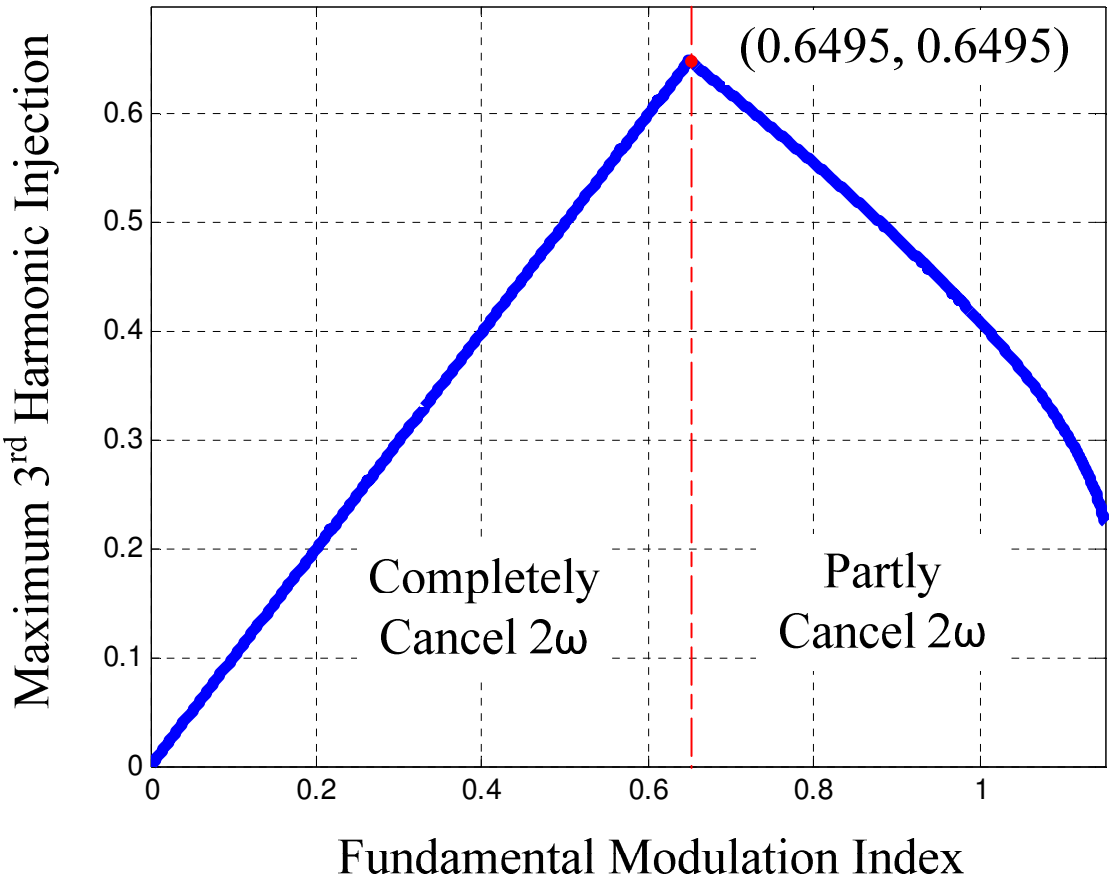


Figure 8.3 The maximum magnitude of the 3rd harmonic injection that can be selected under a certain fundamental modulation index.

8.3 Simulation Results

The simulated cascaded H-bridge multilevel inverter for PV system is rated as follows.

This is a three-phase system with 7 cascaded H-bridge modules in each phase leg, totally 21 modules. Each module is rated at $P = 100\,kW$. Therefore, the whole system is rated at 2.1 MVA. The line-to-line voltage is $V_{ll} = 13.8\,kV$.

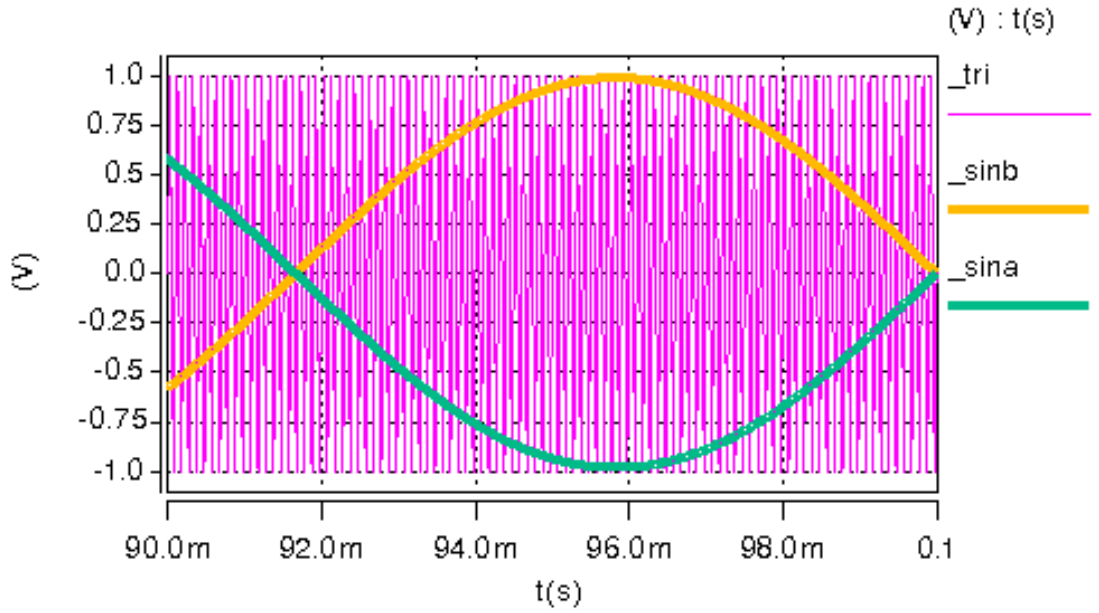
Based on the given power and voltage, it can be derived that the base value of the capacitance *C*, as shown in.

$$C = \frac{1}{\omega Z} = 205\,\mu F \tag{8.15}$$

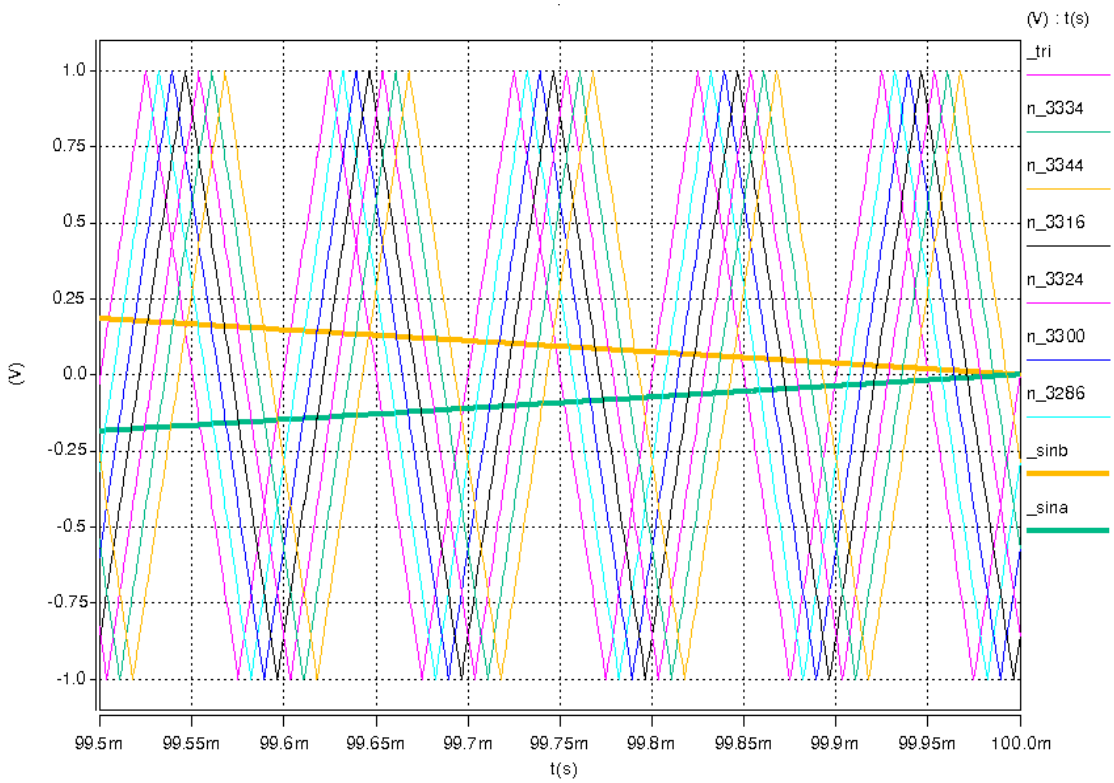
Generally speaking, there are three modulation methods to simulate this cascaded multilevel inverter: programmed modulation, carrier based PWM and space vector PWM. Although they are not mathematically equal and with different implementation method, the main idea is the same—to generate a sine-shaped output voltage. If one wants to insert a 3rd harmonic into the originally perfect sinusoidal voltage, for carrier-based PWM, it is obvious that the goal can be achieved by simply adding a 3rd harmonic sine wave to the fundamental sine reference. For space vector PWM, it originally contains a 3rd harmonic component, which means modify this 3rd harmonic is possible. For programmed modulation, simply change the 3rd harmonic component equation from 0 to the desired amplitude, and one will get those off-line switching angles.

Therefore, the conclusion is that the proposed 3rd harmonic injection method can achieve similar results, no matter which modulation methods one is working with.

Hence, the phase-shifted carrier-based PWM method is chosen in this experiment. Figure 8.4 shows the phase-shifted carrier-based PWM method: (a) two fundamental references with a triangle carrier; (b) zoom-in view of (a), showing the seven phase-shifted triangle carriers for the seven modules in one phase leg.



(a)



(b)

Figure 8.4 The phase-shifted carrier-based PWM method: (a) two fundamental references with a triangle carrier; (b) zoom-in view of (a), showing the seven phase-shifted triangle carrier for the seven modules in one phase leg.

Figure 8.5 and Figure 8.6 shows the SABER simulation's circuit and PWM generating part respectively.

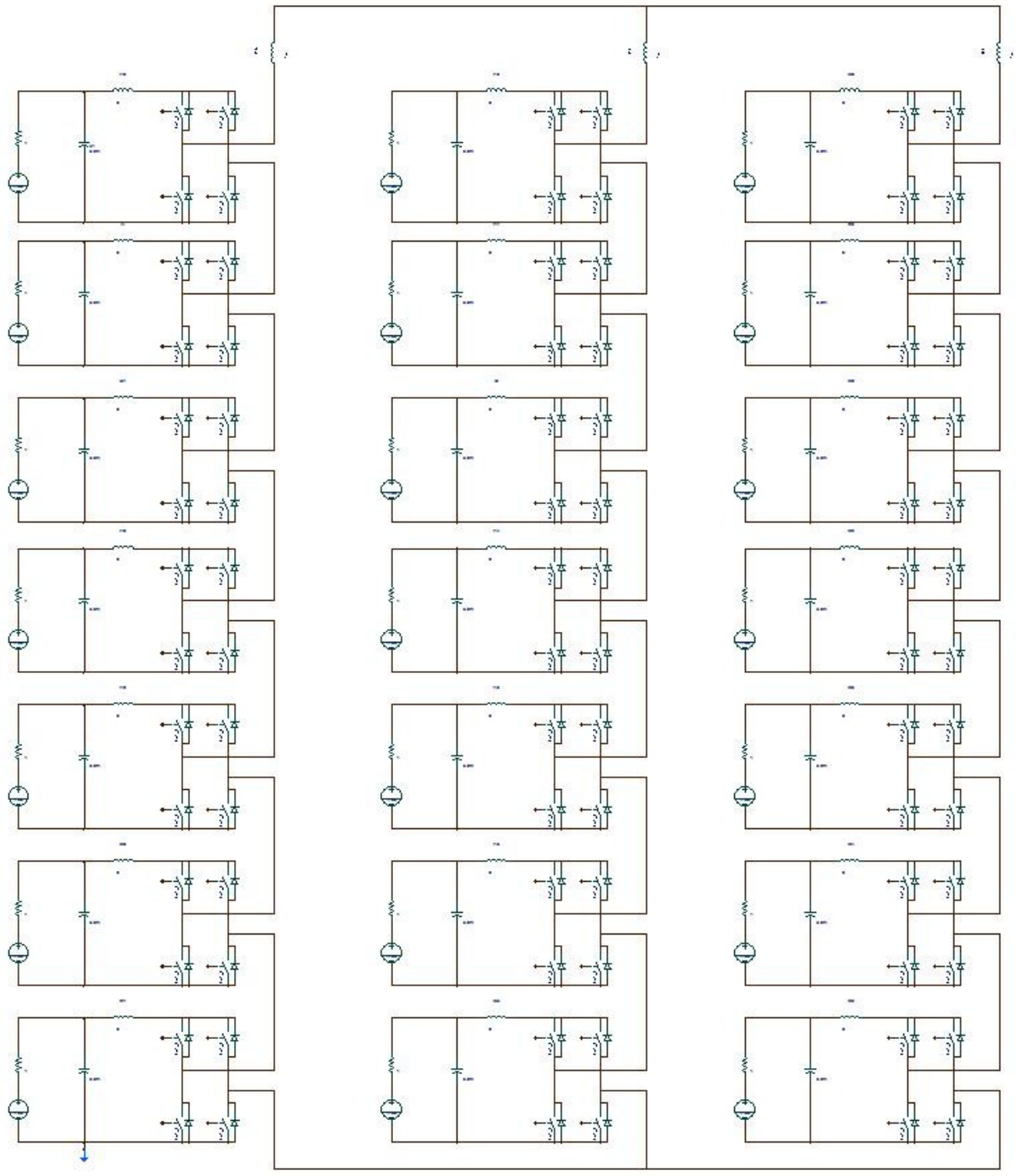


Figure 8.5 SABER Simulation – circuit part

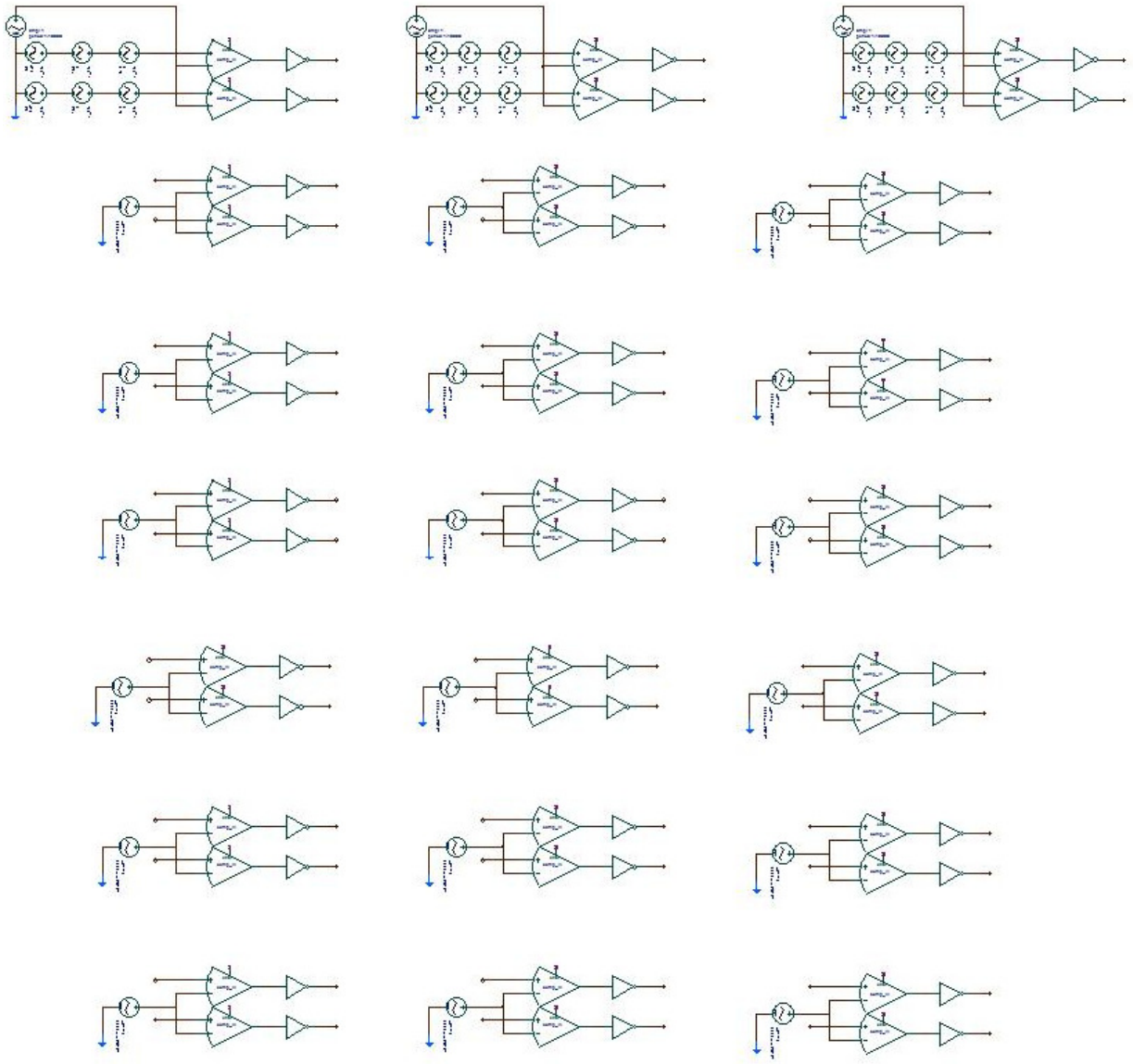


Figure 8.6 SABER Simulation – PWM generating part

As known from Figure 8.3, if the fundamental modulation index is high, there is only limited quantity of 3rd harmonics can be injected. For example, M_0=0.9, maximum M_3 can only be 0.4865.

On the other hand, if the fundamental modulation index is less than 0.6459, it can be completely cancelled out by inserting the same amplitude of the 3rd harmonic component. For example, M_0=0.6459, maximum M_3 can also be 0.6459.

Figure 8.7 shows the simulation results when traditional pulsewidth modulation method is used, and the fundamental modulation index is 0.9, which is at the higher end. The top 3 waveforms show the line-to-line voltage, measured to be at 12.7 kV. The 2nd 3 waveforms are the capacitor currents in the top modules of each phase. Numerical simulation shows the rms value of this ripple current that the dc link capacitor has to absorb is 47.2 A. The 3rd 3 waveforms demonstrate the phase voltage of the multilevel inverter, and the rms value is measured to be 7.3 kV. And the 4th 3 waveforms show the 3 phase inverter output current. The last waveform shows the dc link voltage for the top module in Phase A, which indicates the voltage ripple peak-to-peak versus the dc link average voltage is around 2%.

$$\frac{V_{ripple(pp)}}{V_{dc(avg)}} = \frac{34.329\,V}{1648.2\,V} = 2.0\% \tag{8.16}$$

This percentage is consistent for other modules as well.

From this simulation result, it is concluded that to maintain the dc link voltage ripple under 2% at this situation, the dc link capacitor for each H-bridge module has to be at least 3.8 mF. Accordingly, in per unit value, this capacitance is

$$\frac{3.8\,mF}{205\,\mu F} = 18.5\ p.u. \tag{8.17}$$

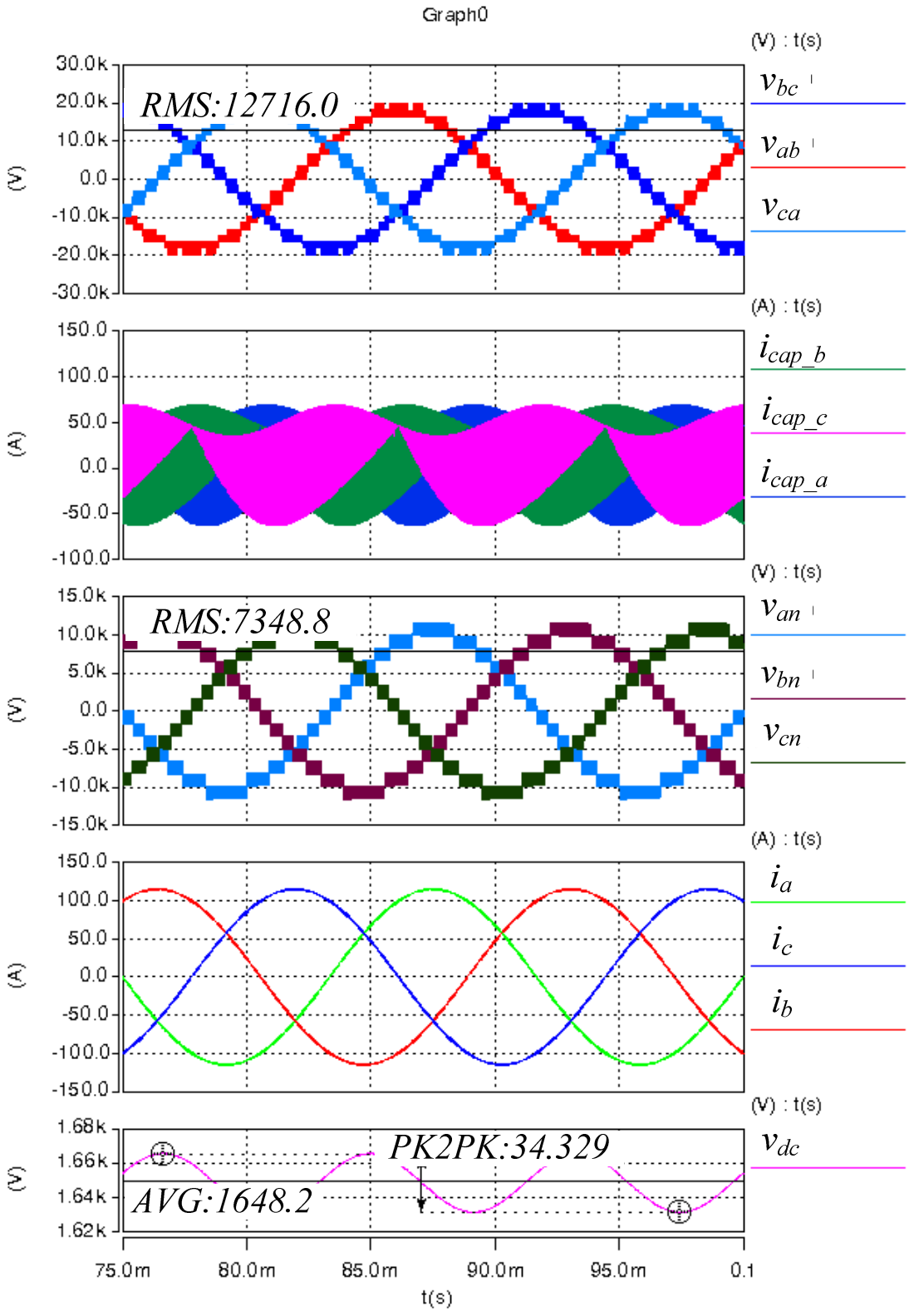


Figure 8.7 Simulation results of the traditional pulsewidth modulation method without 3rd harmonic injection: M0=0.9, f0=60 Hz, Cdc=3.8 mF.

Figure 8.8 shows the simulation results of the proposed 3rd harmonic injection method with the same dc capacitor of 3.8 mF. Waveforms are the similar as Figure 8.7, except in the 3rd waveforms, 3rd harmonic injection can be noticed easily. Without changing the line-to-line voltage, the dc voltage ripple is reduced to

$$\frac{V_{ripple(pp)}}{V_{dc(avg)}} = \frac{21.696\,V}{1648.2\,V} = 1.3\% \tag{8.18}$$

Therefore, by using a smaller dc capacitance, one can still achieve the 2% voltage ripple requirement. Figure 8.9 shows the simulation results of the proposed 3rd harmonic injection method with a smaller dc capacitor.

In this simulation, the dc link capacitance is reduced to 2.2 mF, and still keeping a 2% voltage ripple. The per unit value is

$$\frac{2.2\ mF}{205\ \mu F} = 10.7\ \ p.u. \tag{8.19}$$

This is a 42% reduction, compared to the traditional PWM method.

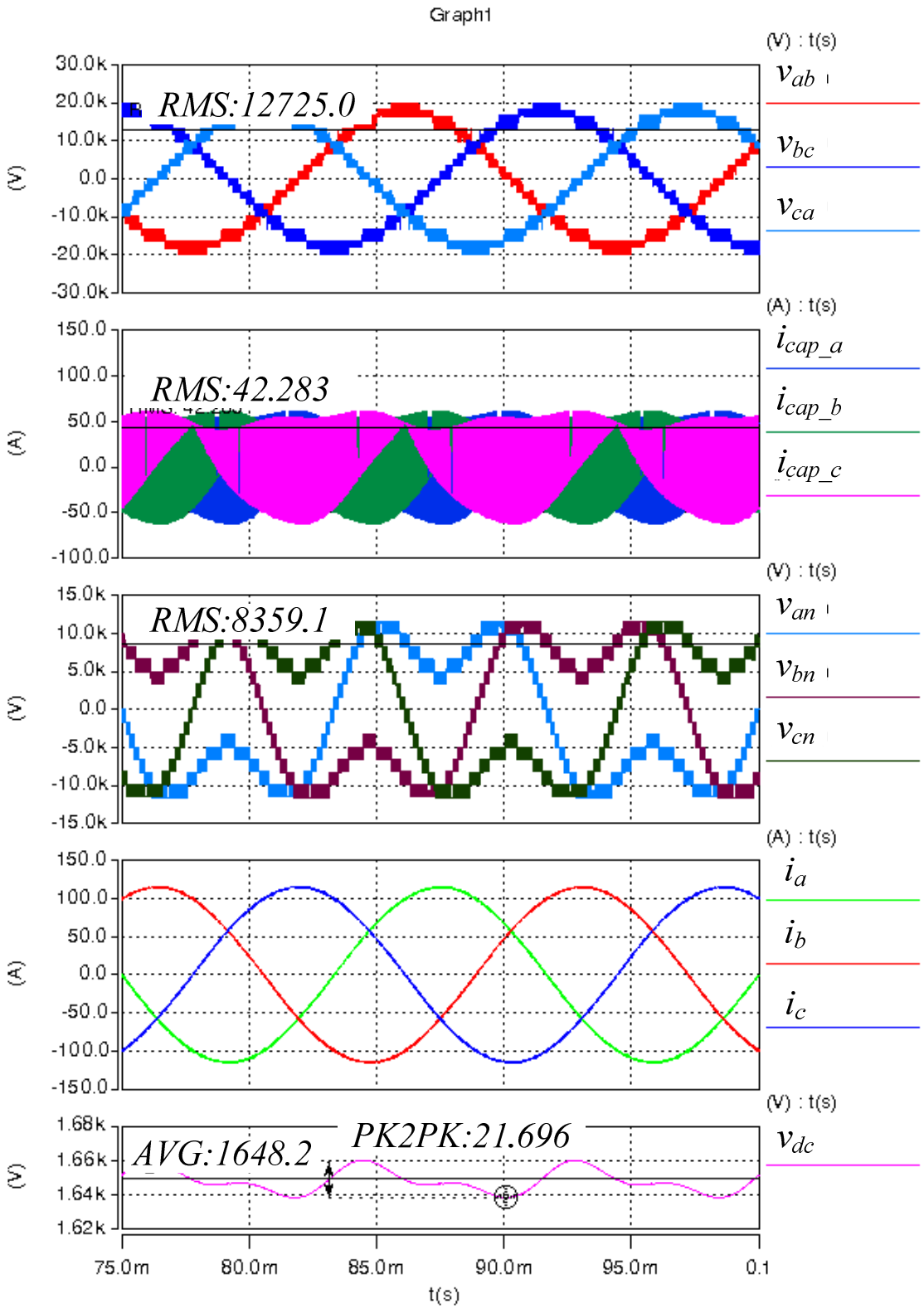


Figure 8.8 Simulation results of the proposed 3rd harmonic injection pulsewidth modulation method: M0=0.9, f0=60 Hz, M3=0.4865, f3=180 Hz, Cdc=3.8 mF.

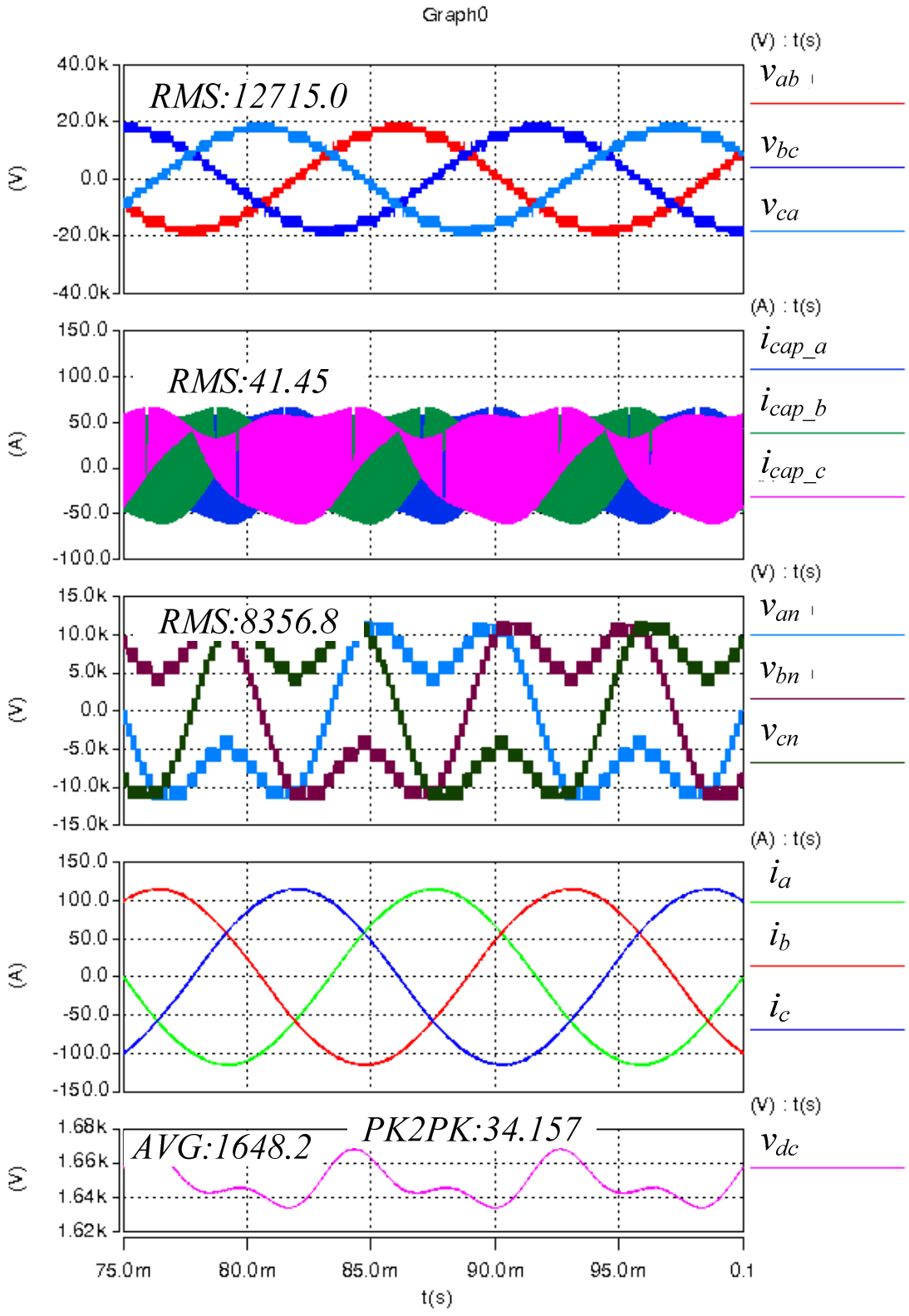


Figure 8.9 Simulation results of the proposed 3rd harmonic injection pulsewidth modulation method: M0=0.9, f0=60 Hz, M3=0.4865, f3=180 Hz, Cdc=2.2 mF.

Again, the above case is at the higher end of the fundamental modulation index, which has limited reduction on the 2ω ripple. Whereas at the lower end, when the fundamental modulation index is smaller than 0.6459, the reduction can be even more. Figure 8.10 and Figure 8.11 is a good example for this situation.

Figure 8.10 shows an example of M0=0.6459, where Cdc is 1.6 mF to achieve a 2% voltage ripple at the dc link side. And Figure 8.11 shows an example of M0=0.6459 with an additional 3^{rd} harmonic injection of the same amplitude 0.6459. In this case, Cdc is reduced to 800 uF, and still achieving a 2% voltage ripple. The total dc capacitance reduction is reached to 50%, and this is completely contributed by the frequency increases from 2ω to 4ω.

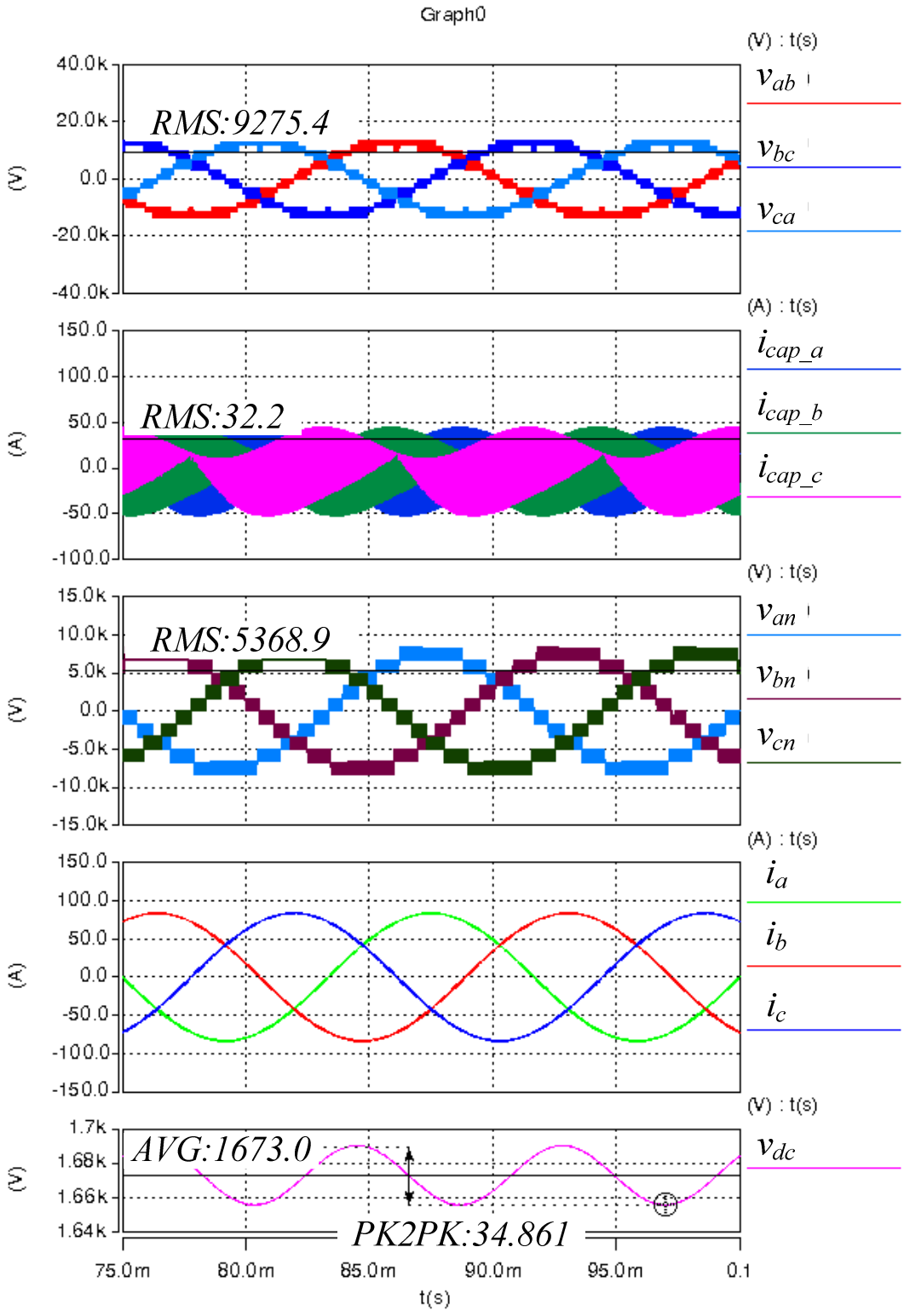


Figure 8.10 Simulation results of the traditional pulsewidth modulation method without 3rd harmonic injection: M0=0.6459, f0=60 Hz, Cdc=1.6 mF.

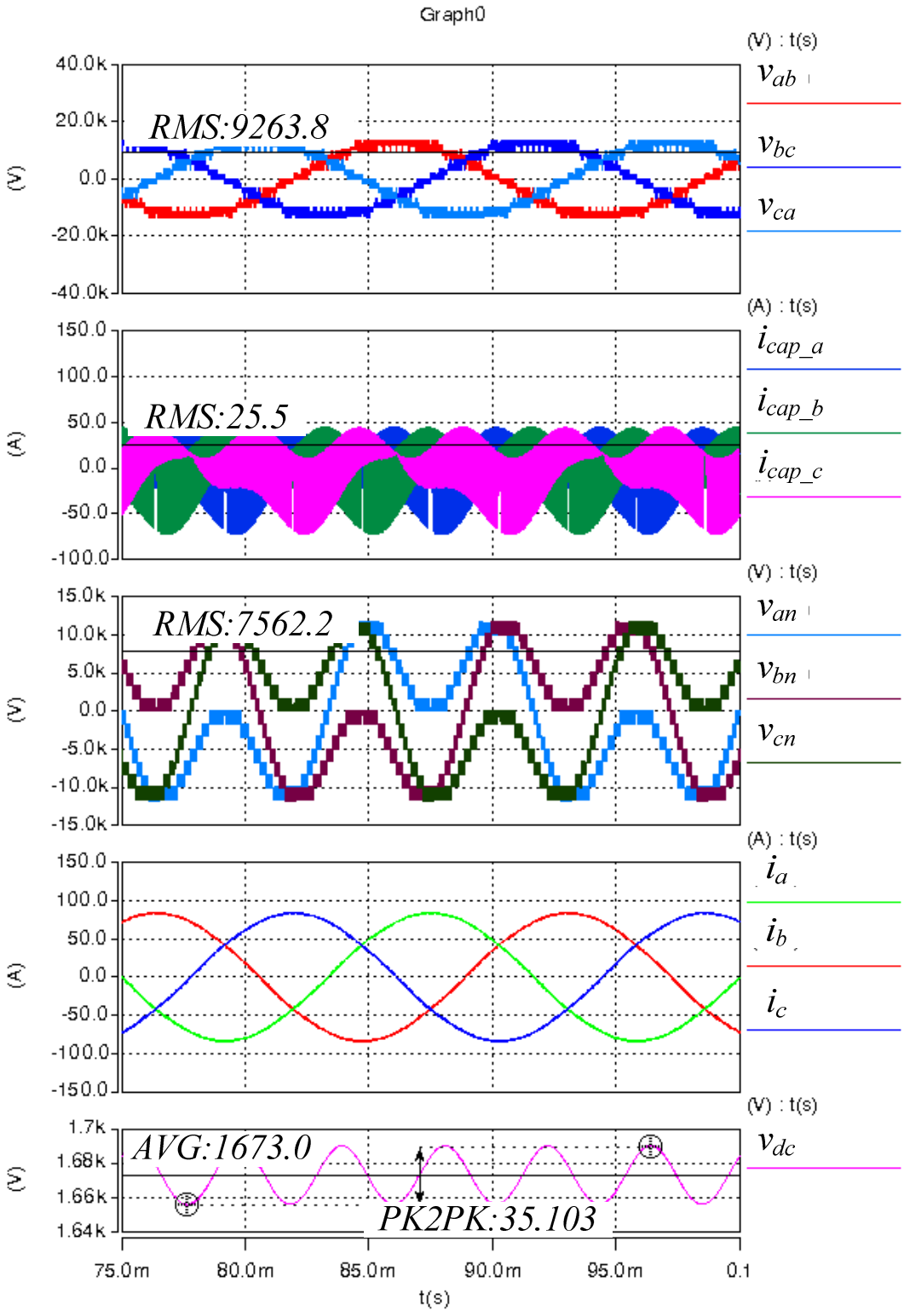


Figure 8.11 Simulation results of the proposed 3rd harmonic injection pulsewidth modulation method: M0=0.6459, f0=60 Hz, M3=0.6459, f3=180 Hz, Cdc=800 uF.

8.4 Conclusions

This chapter presents a simple 3rd harmonic injection method for the cascaded H-bridge multilevel inverters for photovoltaic systems. Without adding any extra components or increasing too much of the control complexity, this approach achieves a 40% to 50% reduction of the dc link capacitor. Theoretical analysis and simulation results are demonstrated to prove the effectiveness.

CHAPTER 9 Solid State Variable Inductor-Capacitor for Reactive Power Compensation with Minimum DC Capacitance

Last chapter talks about that the H-bridge inverter has an inherent problem of the 2ω ripple that requires a huge dc capacitor on the dc link side to absorb this low frequency ripple and smooth out the dc bus voltage. By 3rd harmonic injection, which is simply playing with the PWM strategy with minimum effort, the dc capacitance can be reduced to half. However, the method is based on the pre-requirement of unity output power factor. Otherwise, the 2ω component cannot be cancelled because of mis-phase. In this chapter, the application that will be focused on is the reactive power compensation, whose output factor is zero. Therefore, 3rd harmonic injection will not be able to work in this situation. This dc capacitance reduction is realized by a proposed modified H-bridge topology with suitable closed-loop control.

9.1 Introduction

As the power demands go up, the power system becomes more complicated. Traditionally, the real and reactive power flow through a transmission line in the power grid is determined by its line impedance, voltage magnitudes, and voltage angle differences of the two ends [69]. Sometimes, without adequate control, excessive reactive power flow and unwanted loss can happen, which result in thermal and stability issues [70]. To solve these problems and increase

the transmittable power in the grid, reactive power compensation is used. The basic idea of the reactive power compensation is to insert ideal variable inductors or capacitors that can absorb or supply reactive power to the grid.

Figure 9.1 shows an ideal variable capacitor. At the rated line voltage V_S, as the current changes from *0* to the rated current I_C, the variable capacitance changes from *0* to C_{ac} as well. In this case, the ac capacitor needed for this circuit is 1 per unit (pu). However, in the real life, a large value variable inductor or capacitor can hardly be found, especially for utility grid applications. Therefore, flexible AC transmission system (FACTS) has been introduced since 1990 to implement a real-world variable inductor or capacitor based on semiconductors. Some FACTS such as thyristor switched reactor (TSR) and thyristor switched capacitor (TSC) are simply inductors and capacitors that can vary in a stepwise manner with utilizing thyristors, while some other FACTS devices such as static synchronous compensator (STATCOM) and unified power flow controller (UPFC) could realize continuous variation based on converter topologies with PWM schemes. For example, a variable inductor or capacitor can be implemented by an H-bridge as shown in Figure 9.2. The principle of this H-bridge working as a variable capacitor is controlling the phase angle of ac current I_C to lead the phase angle of ac voltage V_S by 90°, and controlling the amplitude of I_C to achieve the desired equivalent capacitance C_{ac}. The principle of this H-bridge acting as a variable inductor is controlling the

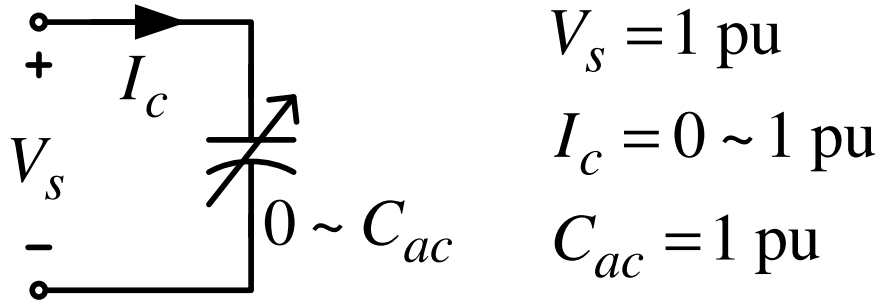


Figure 9.1 An ideal variable capacitor

phase angle of ac current I_C to lag the phase angle of ac voltage V_S by 90°, and controlling the amplitude of I_C to achieve the desired equivalent capacitance C_{ac}. However, this traditional H-bridge implementation has a well-known problem of a large dc link capacitor C_{dc}, due to the low frequency harmonic (2ω ripple) inherent with the H-bridge topology [71]. This dc capacitor is 10 times (assuming the dc voltage ripple peak-to-peak is 5%) as big as the ac capacitance shown in Figure 9.1 in order to maintain the dc voltage ripple low. In addition, increasing the switching frequency is not an option here. Although increasing the switching frequency can reduce the inductance, unfortunately it does not reduce this dc capacitance.

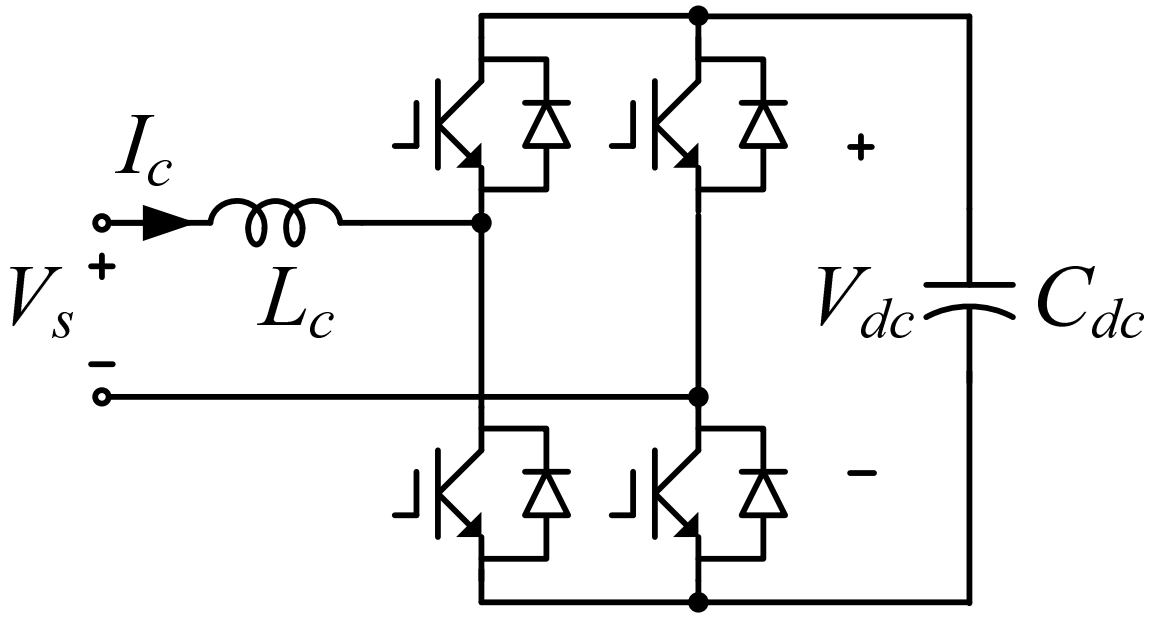
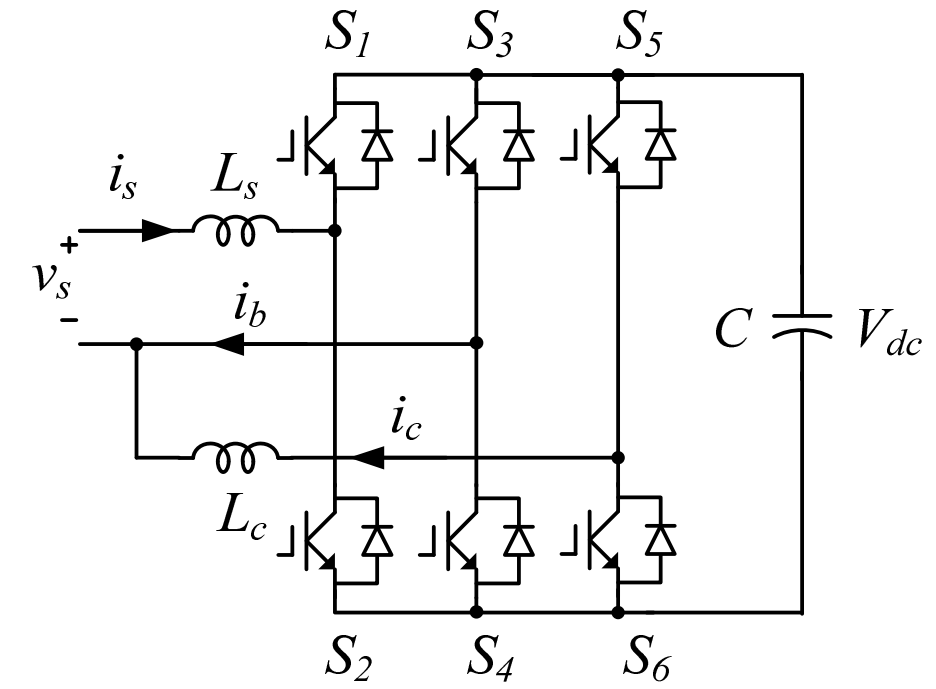


Figure 9.2 A variable capacitor implemented by an H-bridge inverter

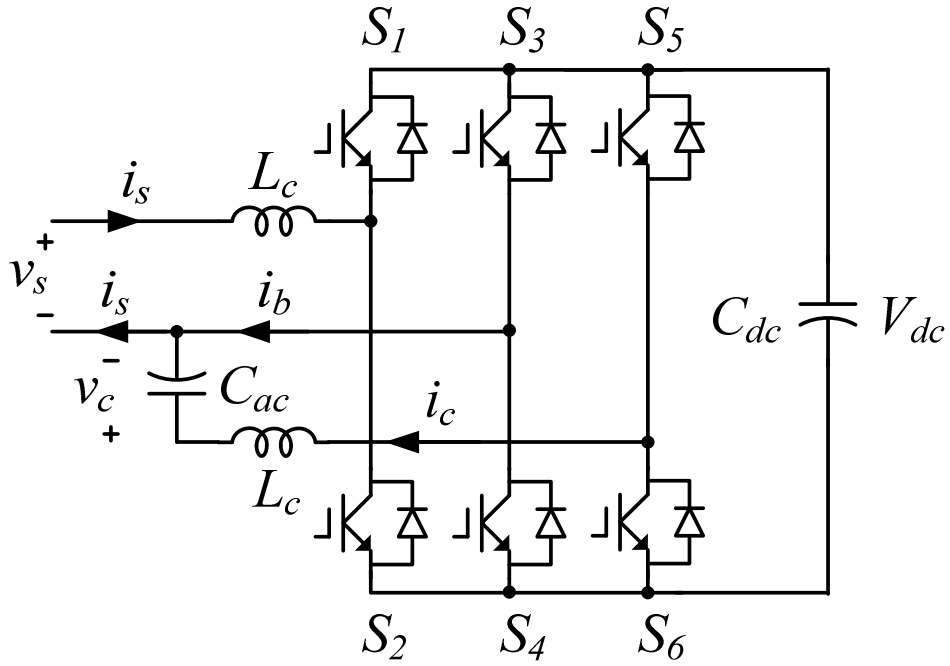
Therefore, this chapter proposes a solid state variable inductor-capacitor (SSVLC), as shown in Figure 9.3. Figure 9.3 (a) shows the proposed solid state variable inductor (SSVL) and Figure 9.3 (b) shows the proposed solid state variable capacitor (SSVC). The proposed SSVLC can

reduce the dc link capacitance to minimum by adding a phase leg to the H-bridge and a small auxiliary ac capacitor/inductor. The main idea is to completely transfer the 2ω low frequency ripple from the dc link capacitor to this auxiliary ac component through the added phase leg. The advantages of this topology are many. First of all, the dc link capacitor can reduce to minimum, subject to only switching frequency ripples. This improvement eliminates the electrolytic capacitor, and enables the use of film capacitor. Film capacitors are typically come with smaller capacitance but larger rms current ripple handling capability, and this kind of capacitors has self-healing capability and small ESR. Therefore they are usually considered to have longer lifetime and higher reliability [72, 73]. On the other hand, the auxiliary ac capacitor is reduced to only 1/10 of the original dc capacitance. Therefore, the combined volume of the dc capacitor and the auxiliary ac capacitor is still smaller than the original huge dc capacitor.

In this chapter, theoretical analysis of the SSVC is provided. Regarding to SSVL, similar derivation method can be applied. Simulation and experimental results are shown to prove the effectiveness of the proposed SSVC with minimum dc capacitance.



(a)



(b)

Figure 9.3 The proposed solid state variable inductor-capacitor:

(a) solid state variable inductor (SSVL); (b) solid state variable capacitor (SSVC).

9.2 Past Works

The purpose of this section is to identify all the topologies that been proposed in the past with their theoretical dc and ac capacitance requirements.

A. Traditional H-Bridge Inverter

The simplest way to implement a variable inductor-capacitor is to use a traditional H-bridge inverter. As mentioned earlier, this topology suffers a huge dc link capacitor C_{dc}, due to the fact that it has to absorb the 2ω ripple. In addition, electrolytic capacitor is commonly preferred for this circuit because of its high power density, which can reduce the size of the converter, but at the same time makes this converter less lifetime and less reliability.

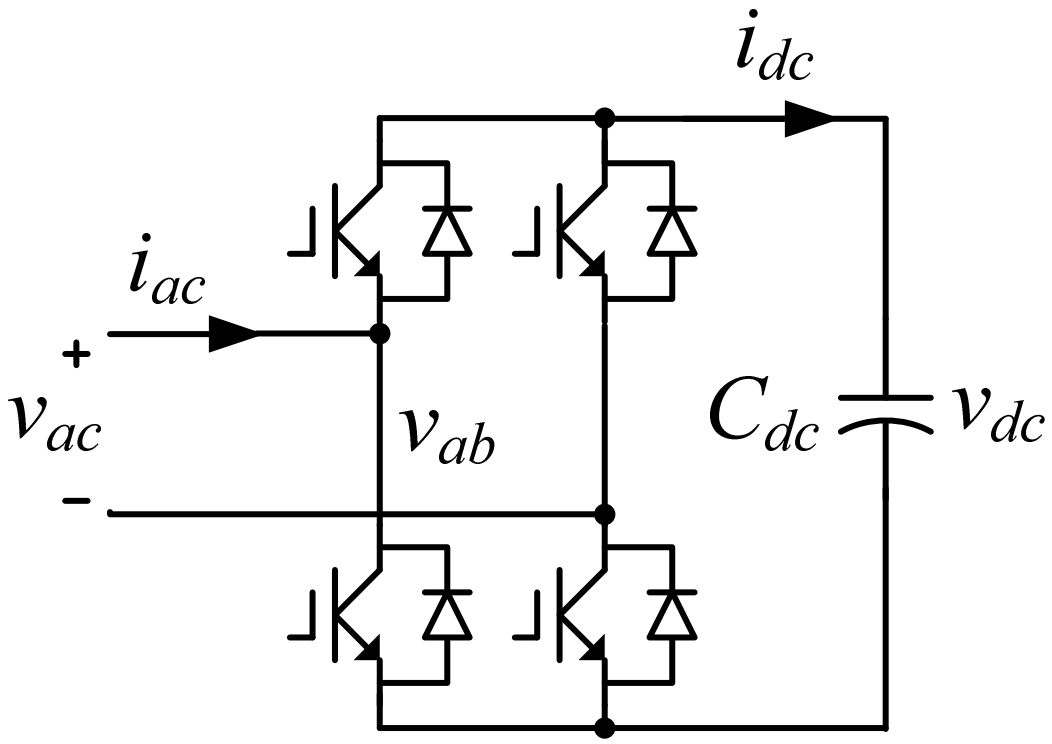


Figure 9.4 Traditional H-bridge inverter

The dc current ripple i_{dc} for this traditional H-bridge inverter can be calculated as shown in (9.1),

$$i_{dc} = \left(S_a - S_b\right) i_{ac} \tag{9.1}$$

where i_{ac} is the ac side current, and S_a and S_b are the switching functions of phase leg *a* and *b* as shown in (9.2).

$$\begin{aligned} S_a &= \frac{1}{2} MI \sin \omega t \\ S_b &= \frac{1}{2} MI \sin\left(\omega t - \pi\right) \\ i_{ac} &= \sqrt{2} I_{ac} \sin\left(\omega t + \varphi\right) \end{aligned} \tag{9.2}$$

φ is the phase angle between ac side voltage and current, v_{ac} and i_{ac}. If φ=90°, it means i_{ac} is leading v_{ac} 90°. If φ=-90°, it means i_{ac} is lagging v_{ac} 90°.

Substitute (9.2) into (9.1), one can achieve (9.3).

$$i_{dc} = \frac{\sqrt{2}}{2} I_{ac} MI \left[\sin\left(2\omega t - \frac{\pi}{2} + \varphi \right) + \sin\left(\frac{\pi}{2} + \varphi \right) \right] \tag{9.3}$$

It is not hard to notice that the first term in (9.3) represents the ripple current part, while the second term in (9.3) represents the dc current portion. As this H-bridge inverter is focused on the application of reactive power compensation, it does not have a dc current. That is to say, for the reactive power compensation, it is equivalent to substitute φ=±90° into (9.3), and the second term goes to zero, meaning no dc current. In conclusion, the capacitor ripple current is the first term in (9.3) and is rewritten below in (9.4).

$$i_{cap} = \frac{\sqrt{2}}{2} I_{ac} MI \sin\left(2\omega t - \frac{\pi}{2} + \varphi \right) \tag{9.4}$$

By integrating the capacitor ripple current i_{cap}, it gives the voltage ripple across the dc capacitor as shown in (9.5).

$$v_C = \frac{1}{C}\int i_{cap}dt = \frac{1}{C}\frac{\sqrt{2}}{2} I_{ac} MI\left(-\frac{1}{2\omega}\right)\cos\left(2\omega t - \frac{\pi}{2} + \varphi\right) \tag{9.5}$$

whose peak-to-peak voltage is shown in (9.6).

$$v_{Cpp} = \frac{1}{C}\frac{\sqrt{2}}{2\omega} I_{ac} MI \tag{9.6}$$

By moving the capacitance *C* to the left side of the equation, one can obtain the capacitance as shown in (9.7).

$$C = \frac{\sqrt{2}}{2\omega v_{Cpp}} I_{ac} MI \tag{9.7}$$

From (9.7), the variables are explained here. ω is the ac side fundamental frequency, and in this grid application case, it will be either 50 Hz or 60 Hz. v_{Cpp} is the capacitor's peak-to-peak voltage ripple in volts. I_{ac} is the rms value of the ac side current, and *MI* is the modulation index of the H-bridge inverter.

It looks like the capacitance can be varied with the modulation index of the inverter, however, this is not the case in reality, since one will not change the actual capacitor for each operating points. Once the capacitor is installed, it will be there for all operating conditions within the specification. This is equivalent to say the dc capacitor is chosen based on the worse case shown in the specification. Therefore, the dc capacitance should be determined at the largest modulation index, *MI*=1, and (9.7) is simplified to be (9.8). Ref [74] also has detailed derivations on this capacitor requirement in section III and the expression is concluded in its own paper equation (9).

$$C = \frac{\sqrt{2} I_{ac}}{2\omega v_{Cpp}} \tag{9.8}$$

Same thing for the ac side current, the dc capacitance is determined by the maximum ac side current's amplitude, therefore the unit value. It is simple for the fundamental frequency and voltage ripple, since they are both constant for a certain design. So far, the capacitance requirement of the traditional H-bridge inverter has been obtained as shown in (9.8). In fact, only the constant $\sqrt{2}/2$ is what one really wants to keep in mind for further comparison.

In the next a couple of pages, a few different topologies will be discussed, analyzed and theoretically calculated to compare the dc capacitance value to (9.8). Therefore, per unit system is a good way to help comparing and determining the best choice among all. In order to get the per unit value of the capacitance, the base value of this case should be calculated first, as shown in (9.9).

$$C_{base} = \frac{1}{\omega Z_{base}} = \frac{I_{ac}}{\omega V_{ac}} \tag{9.9}$$

Therefore, it is straightforward to get the per unit value of the dc capacitance of this traditional H-bridge inverter as shown in (9.10).

$$C_{p.u.} = \frac{C}{C_{base}} = \frac{\frac{\sqrt{2} I_{ac}}{2\omega v_{Cpp}}}{\frac{I_{ac}}{\omega V_{ac}}} = \frac{\sqrt{2} V_{ac}}{2 v_{Cpp}} = \frac{V_{dc}}{2 v_{Cpp}} \tag{9.10}$$

Obviously, from (9.10), in order to calculate the per unit value of the dc capacitance, assumption on the peak-to-peak voltage ripple is needed, and it is usually determined by the specification of the circuit. Let's assume it to be 5% for calculation and comparison purpose, which is most likely the case in the reality as well. Therefore, the per unit value of the dc link

capacitor for the traditional H-bridge inverter is about 10 as shown in (9.11). 10 pu is a very large number for electrolytic capacitors, and the root cause of this huge capacitor is the 2ω ripple that the capacitor has to absorb.

$$C_{p.u.} = \frac{C}{C_{base}} = \frac{V_{dc}}{2v_{Cpp}} = 10 \tag{9.11}$$

B. Traditional H-Bridge Inverter with a Bidirectional Buck/Boost Converter

One proposed topology to minimize this dc link capacitor is shown in Figure 9.5 [75]. This topology utilizes a bidirectional buck/boost converter as an auxiliary ripple energy storage circuit, and achieves a 50% reduction of the whole system size. This is a very good topology in terms of his specific application. However because the auxiliary capacitor C_s has a dc offset, resulting in its ripple power handling capability not maximized, this method still hasn't reached the maximum reduction in the reactive power compensation application.

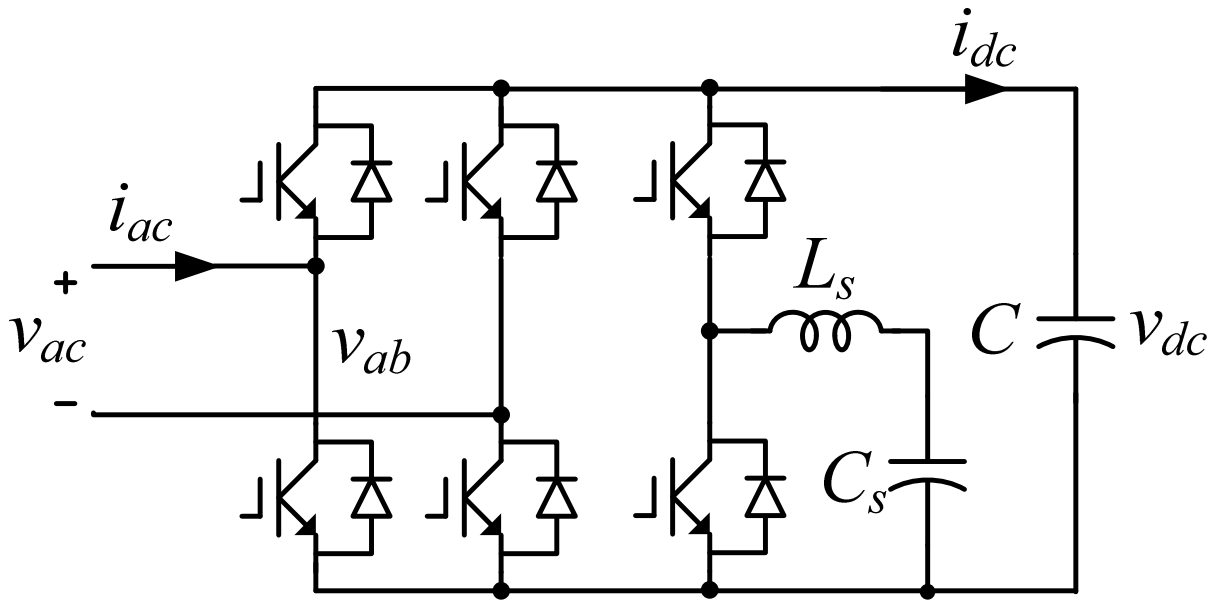


Figure 9.5 Traditional H-bridge topology with a bidirectional buck/boost converter

In order to compare with the proposed SSVLC, it is desired to calculate the auxiliary capacitance here. Firstly, the input power P_{in} on the ac side is calculated as shown in (9.12).

$$P_{in} = v_{ac} i_{ac} \tag{9.12}$$

where

$$v_{ac} = \sqrt{2} V_{ac} \sin(\omega t) \tag{9.13}$$

Substitute (9.13) and (9.2) into (9.12), P_{in} can be simplified to (9.14).

$$P_{in} = V_{ac} I_{ac} \cos\varphi - V_{ac} I_{ac} \cos(2\omega t + \varphi) \tag{9.14}$$

Again, due to different application from [75], the SSVLC is focused on reactive power only. Therefore, $\varphi = \pm 90°$, and the first term in (9.14) goes to zero, leaving only the second term as shown in (9.15).

$$P_{ripple} = -V_{ac} I_{ac} \cos(2\omega t + \varphi) \tag{9.15}$$

Similarly, the ripple energy stores on the auxiliary capacitor can be expressed as (9.16).

$$\frac{1}{2} C_s V_{c\_peak}{}^2 = E_{ripple\_peak} = \frac{P_{ripple\_peak}}{\omega} \tag{9.16}$$

Therefore, the auxiliary capacitance C_s can be calculated as shown in (9.17).

$$C_s = \frac{2 P_{ripple\_peak}}{\omega V_{c\_peak}{}^2} \tag{9.17}$$

where

$$\begin{aligned} P_{ripple\_peak} &= V_{ac} I_{ac} \\ V_{c\_peak} &= \frac{1}{2} V_{dc} \end{aligned} \tag{9.18}$$

Substitute (9.18) into (9.17), (9.19) is achieved.

$$C_s = \frac{8V_{ac}I_{ac}}{\omega {V_{dc}}^2} \tag{9.19}$$

Therefore, the per unit value of the dc link capacitor for the traditional H-bridge inverter with a bidirectional buck-boost converter is about 4, as shown in (9.20).

$$C_{p.u.} = \frac{C}{C_{base}} = \frac{\frac{8V_{ac}I_{ac}}{\omega {V_{dc}}^2}}{\frac{I_{ac}}{\omega V_{ac}}} = \frac{8{V_{ac}}^2}{{V_{dc}}^2} = 4 \tag{9.20}$$

Please note that, ideally, the auxiliary circuit can completely transfer the 2ω ripple energy from the dc link capacitor to the auxiliary capacitor. That is to say, the dc link capacitance can be ignored (very small) for ideal case, and that's why only the auxiliary capacitance is calculated here in order to compare with the traditional H-bridge inverter's main dc link capacitance.

C. Traditional H-Bridge Inverter with Another Bidirectional Buck/Boost Converter

This topology [76] is similar to the previous one [75], in the sense that both of them are adding a complete buck/boost converter to the dc bus, performing as an active filter. Similarly, the auxiliary capacitor has a dc offset. Therefore, the utilization of its energy storage is not fully. In addition, due to the different configuration comparing with the previous topology, this topology's auxiliary capacitor has a voltage that is higher than the dc bus voltage, while the previous one has a voltage that is smaller than the dc bus voltage. The high capacitor voltage forms a killing factor for grid applications, since the grid voltage has already been really high. It will be really challenging if the capacitor voltage is twice as much as the grid voltage. In spite of these disadvantages under our special application, this is still a valid topology. Therefore,

theoretical calculation for dc capacitance is carried out to compare with the traditional H-bridge inverter case.

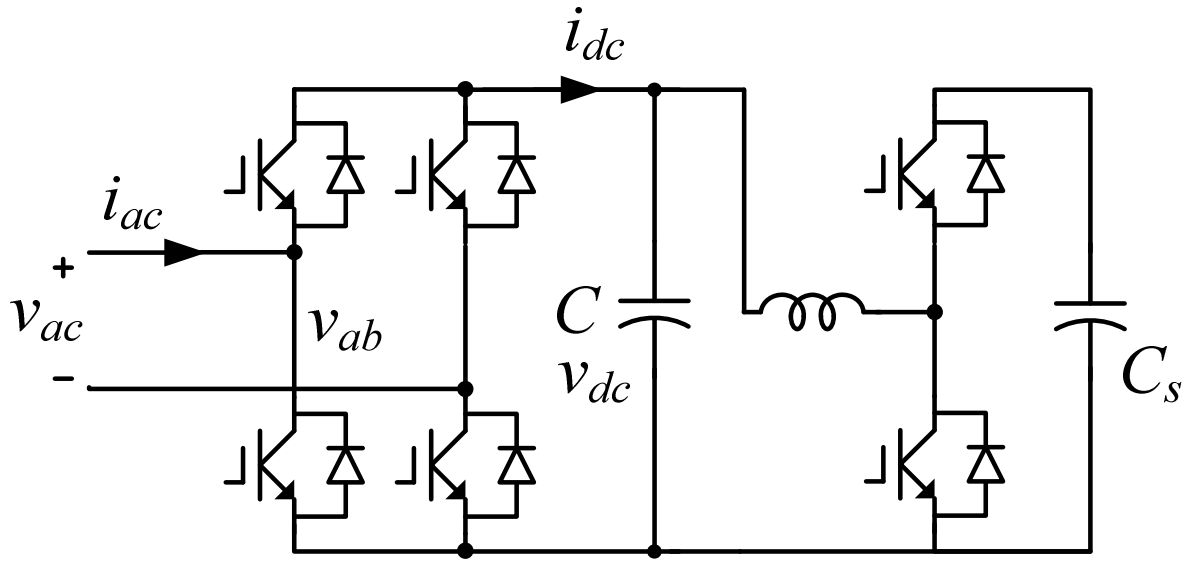


Figure 9.6 Traditional H-bridge topology with another bidirectional buck-boost converter

According to the paper, in order to completely eliminate the 2ω ripple in C, C_s is calculated as shown in (9.21).

$$C_s = \frac{2E_{ripple}}{\left(V_H^2 - V_L^2\right)} \tag{9.21}$$

where V_H and V_L are the upper and lower limit of the C_s voltage ripple respectively, and E_{ripple} is ripple energy of the 2ω harmonics.

Different from the previous topology, as pointed out earlier, V_H and V_L here are both higher than the dc bus voltage. According to (9.21), the larger the difference between V_H and V_L, the smaller the C_s is. Therefore, let's see how much different can these two values be: the lowest value that V_L can go is the dc bus voltage, while theoretically there is no maxim for the highest

value that V_H can achieve. However, in reality, V_H cannot be as high as possible. One reason lies in that the boost converter cannot boost up to more than 4 or 5 times due to the parasitic resistance, such as internal resistance of the power inductor. Another reason is that, with the increase of the V_H, the voltage rating of both the auxiliary capacitor and the auxiliary IGBTs need to be increased accordingly. Based on the two reasons explained above, although (9.21) is adequate for calculating the capacitance, it is hard to decide a reasonable V_H and V_L to compare with those previous topologies.

In order to put a number here, it is assumed that V_H is 1.5 times of the dc bus voltage, while V_L is the dc bus voltage. Therefore, it can achieve(9.22).

$$C_{p.u.} = \frac{C}{C_{base}} = \frac{\frac{2V_{ac}I_{ac}}{\omega 1.25V_{dc}^2}}{\frac{I_{ac}}{\omega V_{ac}}} = 1.6\frac{{V_{ac}}^2}{{V_{dc}}^2} = 3.2 \tag{9.22}$$

D. Traditional H-Bridge Inverter with another Auxiliary H-Bridge Inverter on the ac side

An example of this topology is similar to [77] as shown in Figure 9.7.

According to [77], the auxiliary capacitance *Cs* can be calculated using the equation (23) in the paper. It is rewritten as below in (9.23).

$$C_s = \frac{V_{ac} I_{ac}}{\omega(V_{Cs\_pk}{}^2 - V_{dc}{}^2)} \tag{9.23}$$

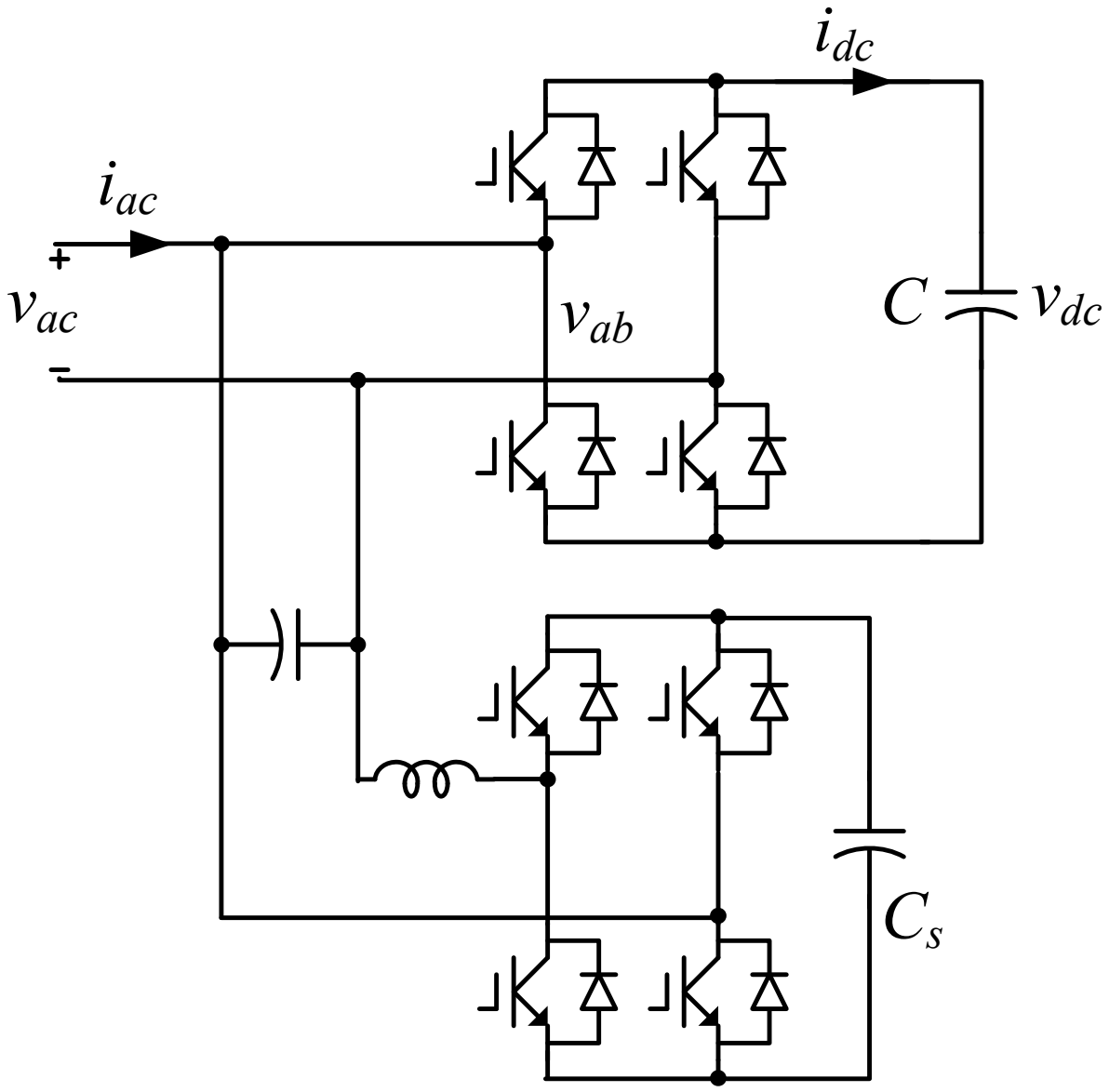


Figure 9.7 Traditional H-bridge topology with another H-bridge inverter on the ac side

where V_{ac} and I_{ac} are the rms values of the ac side voltage and current (the so-called reactive and harmonic component of the load current is in fact all the ac side current here for the reactive power compensation application), and V_{Cs_pk} and V_{dc} are the peak voltage and average voltage of the auxiliary capacitor respectively.

It can be easily noticed that the auxiliary capacitor is essentially still a dc capacitor, which needs to maintain a smooth dc bus voltage for the normal operation of the auxiliary inverter. Since the ac side 2ω power ripple flows to the auxiliary inverter instead of the main inverter, the main dc capacitor can be kept small. Instead, the auxiliary capacitor is huge, and has to take all the reactive ripples. Essentially, it uses a big auxiliary dc capacitor to substitute the big main dc capacitor. Theoretically, there is no change in the total dc capacitor size [71]. This can be double checked from (9.23), because the peak and the average is always kept small for the safe operation of the auxiliary inverter, for example 5%. Therefore, the denominator is very small, leading to a relatively big capacitance.

$$C_{p.u.} = \frac{C_s}{C_{base}} = \frac{\dfrac{V_{ac} I_{ac}}{\omega(V_{Cs\_pk}{}^2 - V_{dc}{}^2)}}{\dfrac{I_{ac}}{\omega V_{ac}}} = \frac{V_{ac}{}^2}{0.05 V_{dc}{}^2} = 40 \tag{9.24}$$

E. Traditional H-Bridge Inverter with another Auxiliary H-Bridge Inverter on the dc side

Instead of putting the H-bridge on the ac side as the reference [77] shows, it is also possible to put this H-bridge a couple of ways on the dc side as well as shown in Figure 9.8. For example, [78, 79] show the H-bridge can be added on the dc side, acting as a series voltage compensator. Similarly to the [77], both of them do not work, since the whole system is used for the reactive power compensation, and additional H-bridge inverter is going to be big.

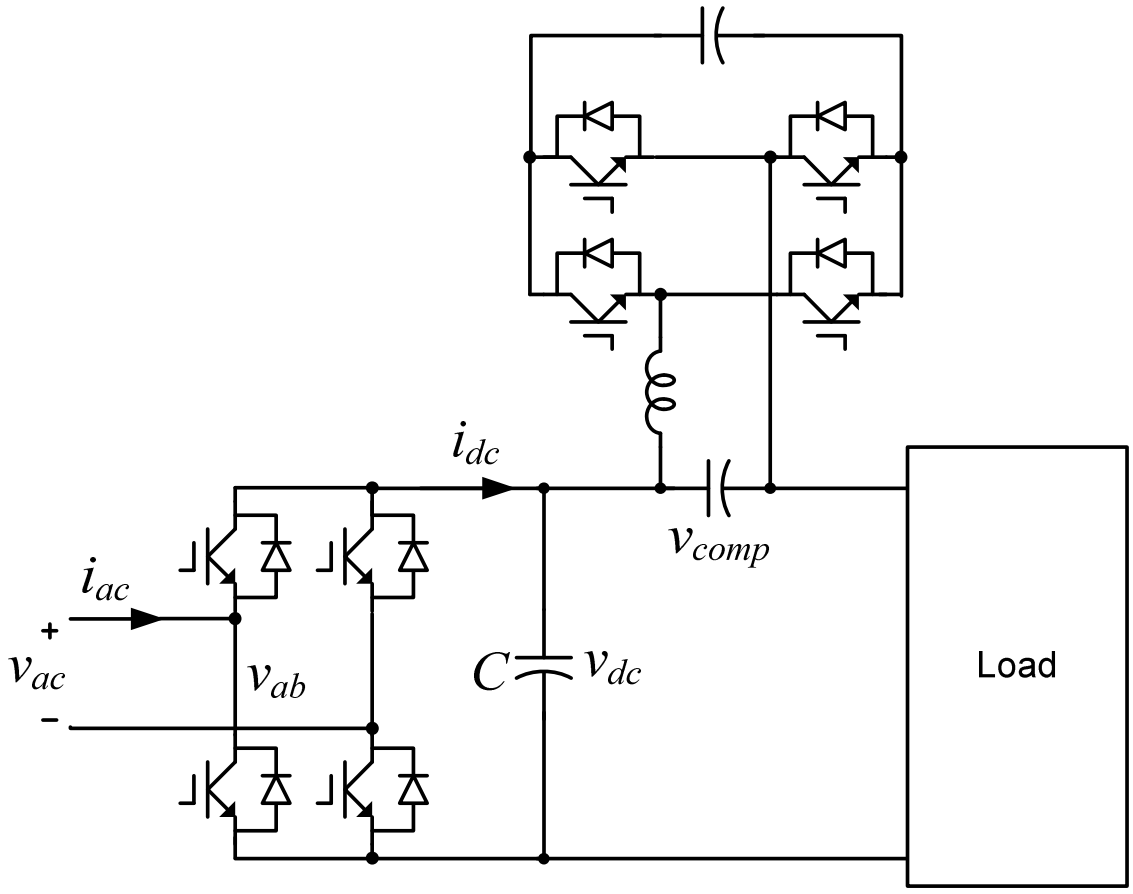


Figure 9.8 Traditional H-bridge topology with another H-bridge inverter in series on the dc side

Another way to add the H-bridge inverter on the dc side is to add in parallel with the main inverter, such as shown below in Figure 9.9. This is a good starting point; however, there is some redundancy in this circuit by using 2 phase legs to compensate the 2ω ripple.

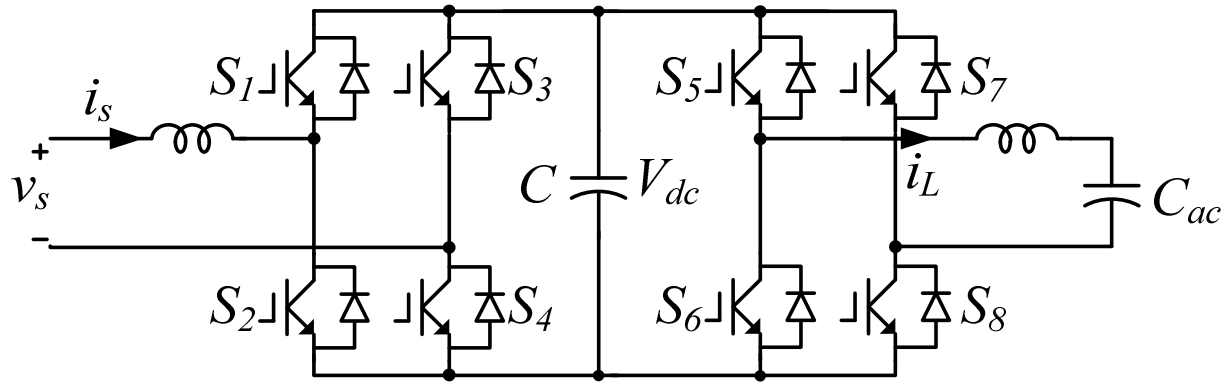
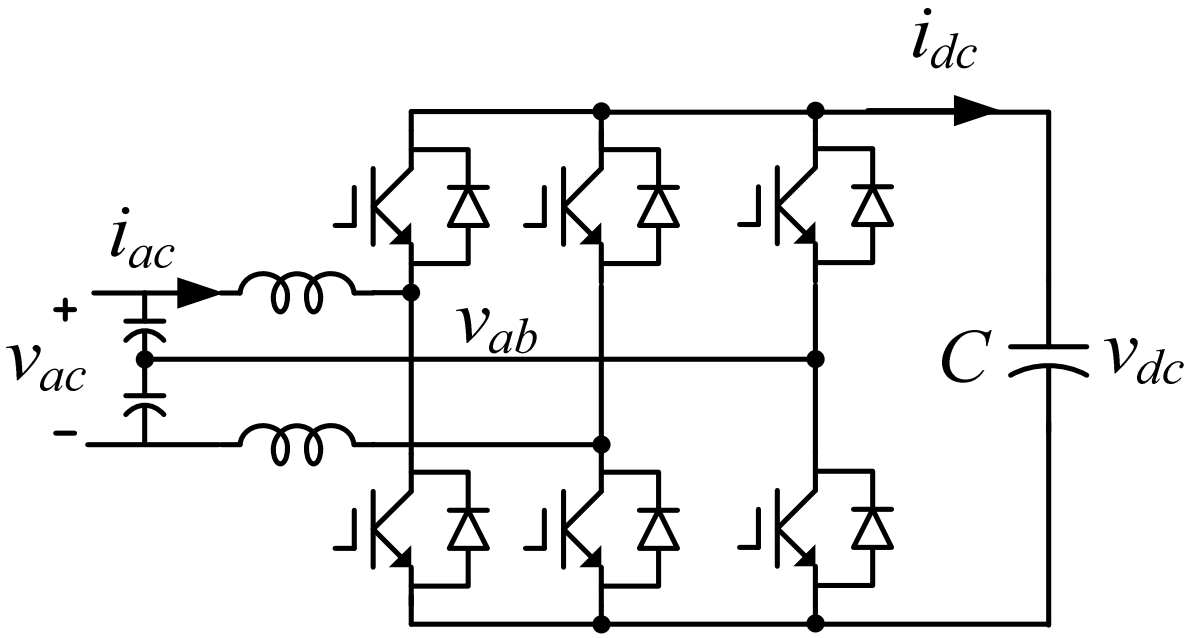


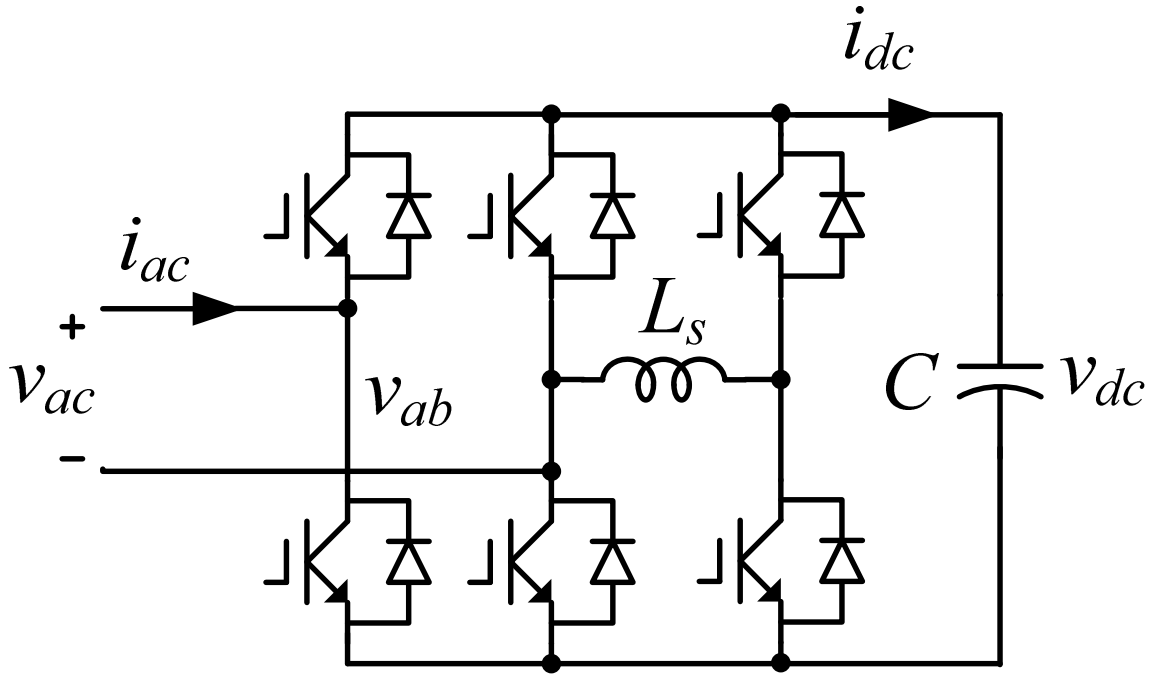
Figure 9.9 Traditional H-bridge topology with another H-bridge inverter in parallel on the dc side

F. *Traditional H-Bridge Inverter with one additional phase added*

Figure 9.10 shows the active filter way of reducing the dc capacitance. The topology is adding only one phase leg to transfer the 2ω ripple to the added passive energy storage component (the inductor or the capacitor). Accordingly, specific control strategy is needed to realize the functionality. However, the author of this paper utilizes this nice topology for power factor correction in [80], whereas this topology could perform the best if used in the reactive power compensation with appropriate control strategy.



(a)



(b)

Figure 9.10 Traditional H-bridge topology with an active filter:
(a) use a capacitor as the auxiliary energy storage;
(b) use an inductor as the auxiliary energy storage.

9.3 The Proposed Solid State Variable Inductor–Capacitor (SSVLC)

In the previous section, a few past works have been discussed and analyzed. From the original H-bridge inverter, who needs a 10 pu dc capacitor, to the H-bridge with a bidirectional buck-boost converter, who needs a 4 pu dc capacitor, more improvements can be achieved.

Most of the previous methods are the same characteristic in terms of treating the auxiliary capacitor as a dc capacitor, since the voltages on these auxiliary capacitors are all having a dc offset with an ac ripple. By modifying the circuit topology to those shown in Figure 9.4 to Figure 9.8, the C_{ac} becomes a pure ac capacitor, making it handle more ripple power, as shown in Figure 9.9 and Figure 9.10.

Now, let's take SSVC as an example of calculating the auxiliary capacitance C_{ac}. Again, power balance is used. Assuming that input voltage v_s and input current i_s are shown as (9.25).

$$\begin{aligned} v_s &= \sqrt{2}V_s \sin \omega t \\ i_s &= \sqrt{2}I_s \sin\left(\omega t + \varphi\right) \end{aligned} \tag{9.25}$$

Since (9.25) represents an ideal capacitor, φ should equals to $90°$, meaning the current is leading the voltage. Hence, (9.25) is simplified to be (9.26).

$$\begin{aligned} v_s &= \sqrt{2}V_s \sin \omega t \\ i_s &= \sqrt{2}I_s \sin\left(\omega t + \frac{\pi}{2}\right) \end{aligned} \tag{9.26}$$

Therefore, the input ripple power can be calculated as (9.27).

$$p_{ripple} = v_s i_s = -V_s I_s \cos\left(2\omega t + \varphi\right) = -V_s I_s \sin\left(2\omega t + \varphi + \frac{\pi}{2}\right) \tag{9.27}$$

The auxiliary capacitor's voltage v_c and current i_c are shown as in (9.28).

$$\begin{cases} i_c = \sqrt{2} I_c \sin(\omega t + \theta) \\ v_c = \dfrac{\sqrt{2} I_c}{\omega C_{ac}} \left[-\cos(\omega t + \theta) \right] \end{cases} \tag{9.28}$$

Therefore, the ripple power stores in the auxiliary capacitor can be expressed as in (9.29).

$$p_c = v_c i_c = -\frac{2 {I_c}^2}{C_{ac}\omega} \sin(\omega t + \theta)\cos(\omega t + \theta) = -\frac{{I_c}^2}{C_{ac}\omega} \sin(2\omega t + 2\theta) \tag{9.29}$$

Again, the whole purpose of adding this auxiliary capacitor is letting it store the entire 2ω ripple power that generated by the input source, so that the dc link capacitor does not have to handle this 2ω ripple power and keeps its own capacitance minimum.

Therefore, by making

$$p_{ripple} = p_c \tag{9.30}$$

one can find the relationship between the amplitudes and phase angles as shown in (9.31).

$$\begin{aligned} -V_s I_s &= -\frac{{I_c}^2}{C_{ac}\omega} \\ \varphi + \frac{\pi}{2} &= 2\theta \end{aligned} \tag{9.31}$$

There are two pairs of solutions shown in (9.32) that can satisfy (9.31):

$$\begin{aligned} &\text{SSVC:} \quad \varphi = \frac{\pi}{2} \;\Rightarrow\; \theta = \frac{\pi}{2} \\ &\text{SSVL:} \quad \varphi = -\frac{\pi}{2} \;\Rightarrow\; \theta = 0 \end{aligned} \tag{9.32}$$

The auxiliary inductor or capacitor's ripple power is concluded in Table 9.1

Table 9.1 Expressions for ripple power on auxiliary inductor and capacitor for SSVL and SSVC

	SSVC	**SSVL**
Input voltage and current	$v_s = \sqrt{2}V_s \sin \omega t$ $i_s = \sqrt{2}I_s \sin\left(\omega t + \frac{\pi}{2}\right)$	$v_s = \sqrt{2}V_s \sin \omega t$ $i_s = \sqrt{2}I_s \sin\left(\omega t - \frac{\pi}{2}\right)$
Auxiliary C/L's voltage and current	$i_c = \sqrt{2}I_c \sin\left(\omega t + \frac{\pi}{2}\right)$ $v_c = \frac{\sqrt{2}I_c}{\omega C_{ac}} \sin \omega t$	$i_l = \sqrt{2}I_l \sin \omega t$ $v_l = \omega L_{ac}\sqrt{2}I_l \cos \omega t$
Ripple energy generated by input source	$p_{ripple} = v_s i_s = V_s I_s \sin 2\omega t$	$p_{ripple} = v_s i_s = -V_s I_s \sin 2\omega t$
Ripple energy stored in auxiliary C/L	$p_c = v_c i_c = \frac{{I_c}^2}{\omega C_{ac}} \sin 2\omega t$	$p_l = v_l i_l = \omega L_{ac} {I_l}^2 \sin 2\omega t$

According to Table 9.1 and (9.31), C pu can be calculated pretty straightforwardly.

$$C_{p.u.} = \frac{C_{ac}}{C_{base}} = \frac{\frac{{I_c}^2}{V_s I_s \omega}}{\frac{I_s}{\omega V_s}} = \frac{{I_c}^2}{{I_s}^2} \tag{9.33}$$

Equation (9.33) means that in order to completely transfer the 2ω ripple that generated by the input source, for SSVC, the auxiliary capacitance has to satisfy (9.33).

Figure 9.11 shows the phase diagram of the source and auxiliary inductor/capacitor's voltage and current relationships. Again, taking the SSVC as an example, the phase b current shown in Figure 9.3 is equal to the arithmetic difference between i_s and i_c, since both vectors are in phase.

Therefore, if i_s and i_c have the same amplitude, the phase b current can reduce down to 0. At this situation, according to (9.33), the auxiliary capacitance is chosen to be 1 pu.

(a) (b)

Figure 9.11 Phasor diagram of (a) SSVL and (b) SSVC.

9.4 Experimental Results

A 1 kVar solid state variable capacitor prototype is built for validation purpose with 100 V dc voltage.

Figure 9.12 shows the ac source voltage and current with the dc voltage ripple, if the auxiliary phase leg, capacitor and smoothing inductor are not connected at all. The dc capacitance in this case was 820 uF, with a voltage ripple of 13%. In order to maintain a 5% voltage ripple requirement, the dc capacitance is needed to be 3 mF.

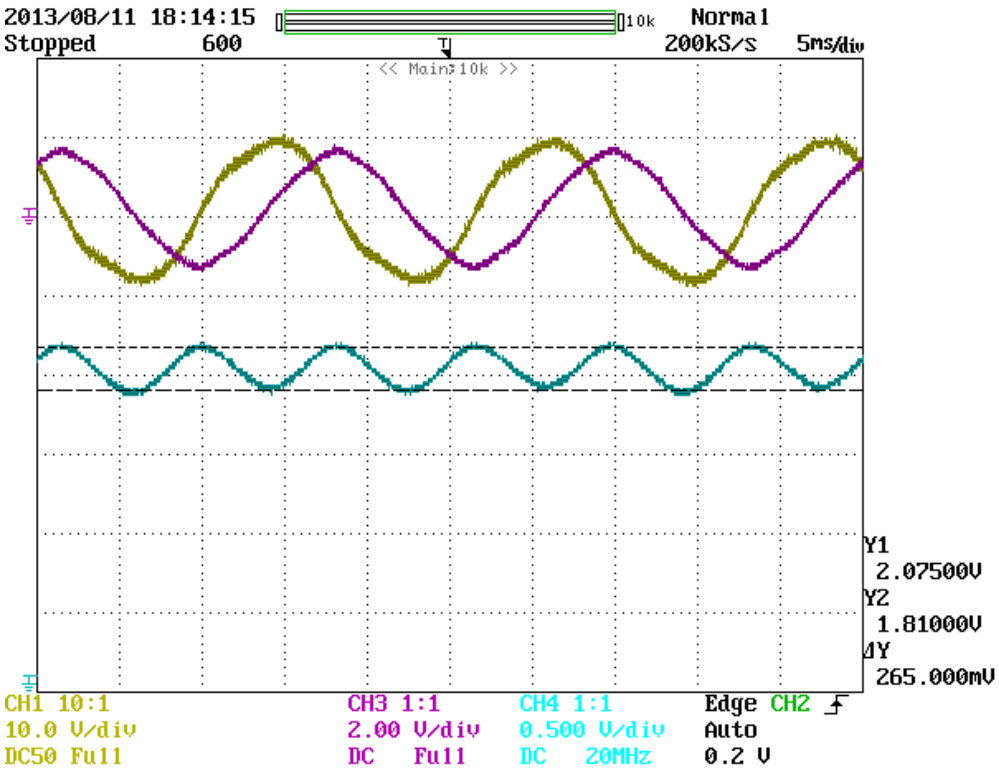


Figure 9.12 Traditional H-bridge inverter with 820 uF dc capacitor

Figure 9.13 and Figure 9.14 shows the experimental result of the proposed SSVC with the same condition as Figure 9.12, but with reduced dc link capacitor of 150 uF. However, this can hold the dc link voltage ripple under 5%.

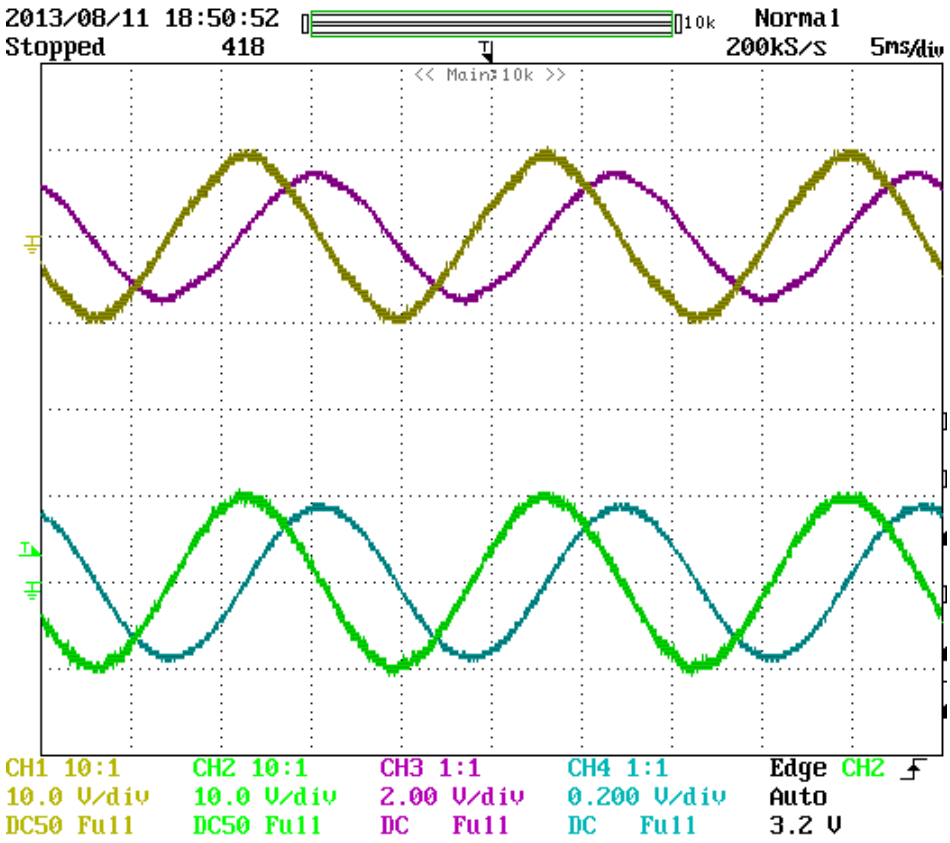


Figure 9.13 The proposed SSVC with 150 uF dc capacitor and 300 uF ac auxiliary capacitor.

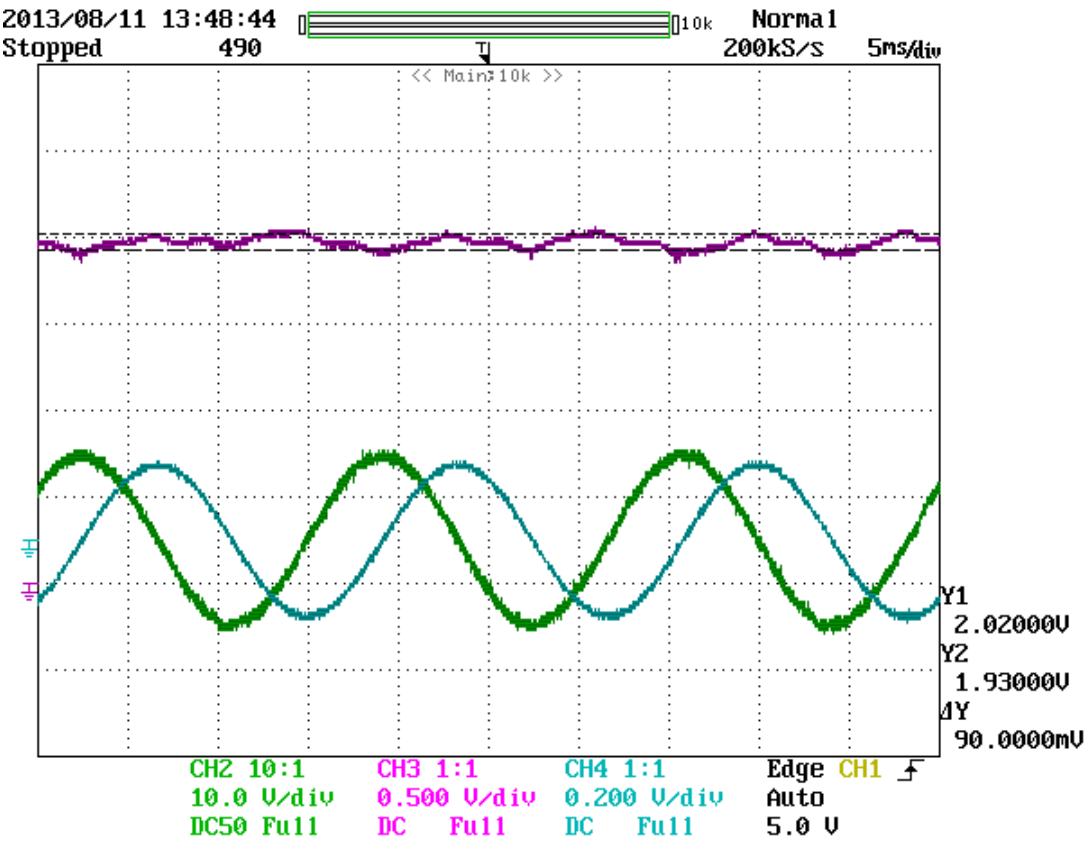


Figure 9.14 The proposed SSVC with 150 uF dc capacitor and 300 uF ac auxiliary capacitor.

9.5 Conclusions

A new solid state variable capacitor (SSVC) with minimum dc capacitance is proposed. The proposed SSVC consists of an H-bridge and an additional phase leg connected to an ac capacitor with fixed capacitance, *Cac* and can reduce the dc capacitance to the minimum just for absorbing switching ripples. The fixed ac capacitor controlled by the additional phase leg absorbs the 2ω component and theoretically can eliminate 2ω ripples in the dc capacitor completely. Therefore, no electrolytic capacitors would be needed. Simulation and experimental results are shown to prove the effectiveness of the proposed SSVC with minimum dc capacitance.

CHAPTER 10 Contribution and Future Work

10.1 Contributions

The contributions presented in this dissertation are listed in short conclusions below:

- Theoretical equations to express capacitance versus voltage ripple and rms ripple current versus modulation index have been developed for SPWM, 6-step operation, as well as for diode rectifier, which provides better design/calculation of the required dc capacitance and better insights into the limits and optimum operation of the converter/inverter system, than the traditional empirical equations and simulations.
- From the theory developed above, a carrier modulation method for the dc-dc converter, which synchronizes the dc-dc converter with the SPWM inverter in the HEV system, is further proposed. This is also able to minimize the dc capacitance and dc current ripples through the improved PWM methods.
- The 3-phase cascaded multilevel H-bridge inverters for photovoltaic application are usually suffers a big dc capacitor due to the 2ω ripples. A 3rd harmonic injection method is proposed to reduce this dc capacitor to 50% or less depending on the modulation index used. The 3rd harmonic components do not affect the output voltage due to the 3-phase configuration, and it is quite easy to implement by simply insert an additional harmonics in the PWM references, where no complicated closed-loop control is required.

- A new solid state variable capacitor (SSVC) with minimum dc capacitance is proposed. The proposed SSVC consists of an H-bridge and an additional phase leg connected to an ac capacitor with fixed capacitance, *Cac* and can reduce the dc capacitance to the minimum just for absorbing switching ripples. The fixed ac capacitor controlled by the additional phase leg absorbs the 2ω component and theoretically can eliminate 2ω ripples in the dc capacitor completely. Therefore, no electrolytic capacitors would be needed.

10.2Future Work

- Although this dissertation has basically covered all the topologies and operation methods that exists in the HEV system nowadays, all the analysis are assumed to be ideal, for example, the motor currents. However, in the real system, the situation would not be even closed to ideal at all times. Any oscillation or saturation happened would push the circuit condition into a non-ideal case, which needs to be researched more in details.
- The proposed theory and PWM methods are all based on open loop control, which is the very first step of minimizing the dc link capacitance. The next step would be, on this basis by knowing the minimum value under open loop, further minimizing the dc capacitance would be realized by utilizing close-loop control.
- 3rd harmonic injection method for the multilevel H-bridge inverter needs experimental confirmation to approve the effectiveness. Additionally, this method is limited to unity power factor applications, such as the photovoltaic application proposed in the dissertation. However, many other applications with non-unity power

factor still suffer from the big dc capacitor. Topology modification may be a good way to go to reduce the capacitance in non-unity power factor cases.

- SSVLC definitely needs more work, both in theoretical and experimental ways. Utilizing wide-band gap devices to further increase the switching frequency and shrink the auxiliary inductor size is one direction, and my labmates are working on this right now.

APPENDIX

APPENDIX

Proof of Switching Functions:

Fig. 3(a) shows the three sinusoidal references and the triangle carrier waveform for two switching periods. Assume the switching period is T_{sw}, the turn off time during a switching cycle of the phase A upper switch is T_{offa}, and the DC link voltage is V_{dc}.

As one may notice, the blue right angle triangle is similar to the red right angle triangle. Therefore, a relationship (A. 1) is obtained.

$$\frac{\frac{V_{dc}}{2} - v_{an}}{\frac{T_{offa}}{2}} = \frac{\frac{V_{dc}}{2}}{\frac{T_{sw}}{4}} \tag{A. 2}$$

By substituting (2.1) and (2.4), (A. 3) is achieved.

$$T_{offa} = T_{sw}\left(\frac{1}{2} - \frac{1}{2}MI \cdot \sin\omega t - \frac{v_{3\omega}}{V_{dc}}\right) \tag{A. 4}$$

Therefore, the expression of S_a is obvious:

$$S_a = (1 - \frac{T_{offa}}{T_{sw}}) \tag{A. 5}$$

Substituting (A. 6) into (A. 7) will give the expression of switching functions as (2.3).

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