

# Thermal Packaging Challenges for Next-Generation Power Electronics

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New Orleans

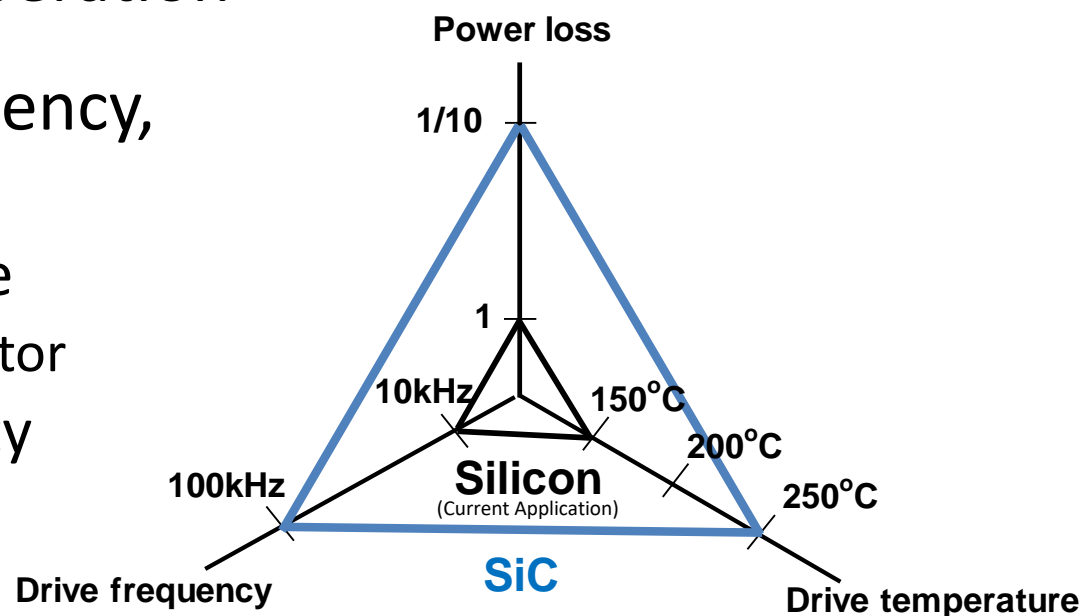
March 15-19, 2020

# Overview

- Characteristics of Wide Band-Gap Devices
- Requirements of Next-Generation Packaging
- Packaging Trends for Power Electronics
- Relevant Future Technologies
  - Near-Junction Cooling
  - Thermal Ground Planes
  - Transient Liquid Phase Bonding
  - Self-Healing Die Attach
- Conclusions

# Characteristics of Wide Band-Gap Devices

- Increased device breakdown electric field
- High temperature operation
- High switching frequency, low switching loss
  - Reduced passive size
    - E.g. inductor, capacitor
  - Higher power density



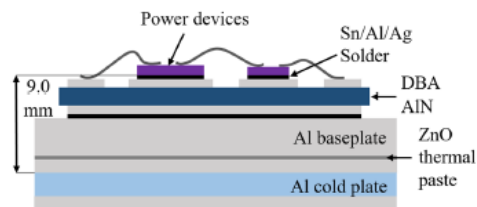
\* Ref.: Ogawa, et al., 2016

# Requirements of Next-Generation Packaging

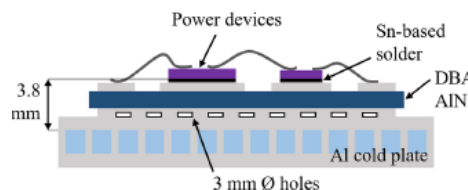
- Packaging strategies that support higher maximum junction temperature: 150 °C → 250 °C
  - E.g. new material systems must be developed for bonding, substrate, encapsulation
- Thermal management techniques that enable higher power density (orders-of-magnitude)
  - E.g. new approaches needed beyond conventional remote cooling techniques
- Careful consideration of package for low parasitic inductance and electromagnetic interference (EMI)

# Packaging Trends for Power Electronics

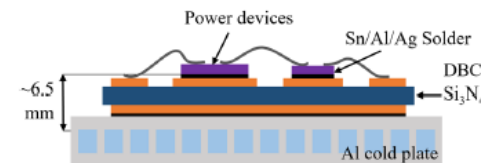
- Historical approaches in automotive:



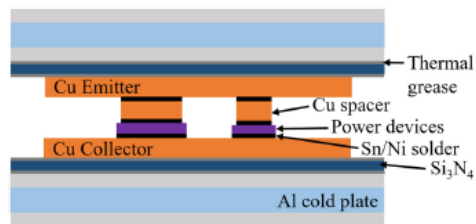
Toyota Prius 2004



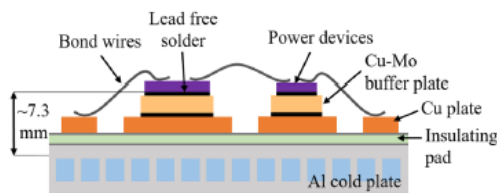
Toyota Prius 2010



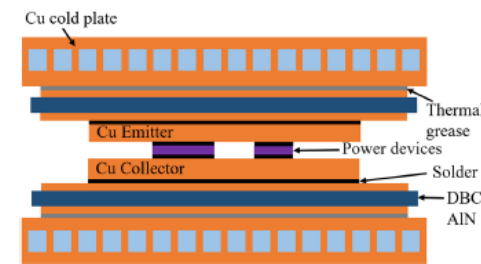
Honda Accord 2014



Lexus LS 600h 2008



Nissan Leaf 2012



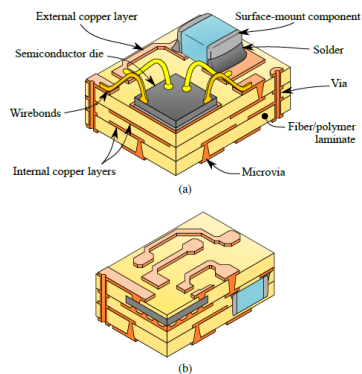
Chevrolet Volt 2016

\* Ref.: Broughton, et al., 2018

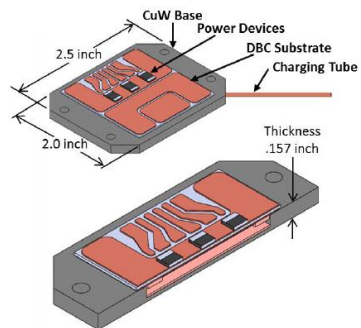
Multiple layers and single-phase remote cooling dominate applications, but limit packaging breakthrough

# Packaging Trends for Power Electronics

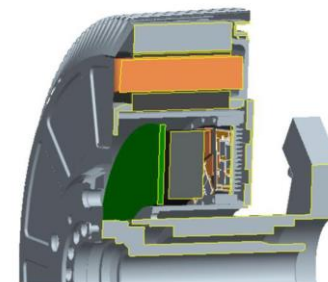
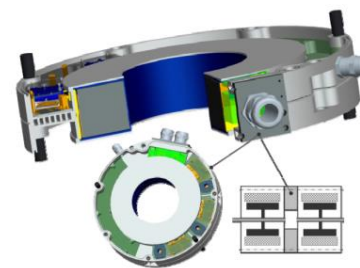
- Efforts towards higher levels of integration:



\* Ref.: Buttay, et al., 2018

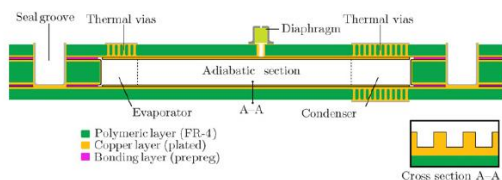


\* Ref.: Hose, et al., 2017

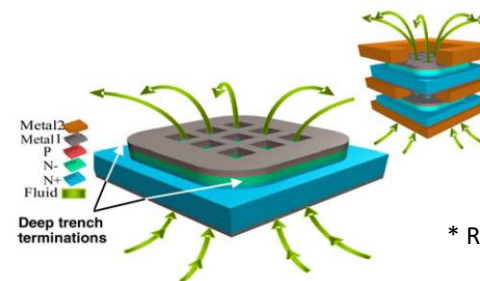


\* Ref.: Marz, et al., 2010

## New Form Factors & Motor Integration



\* Ref.: Wits, et al., 2010



\* Ref.: Vladimirova, et al., 2013

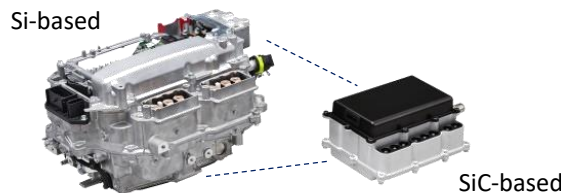
Substrate (e.g. PCB, DBC) Embedding

Device Embedded Cooling

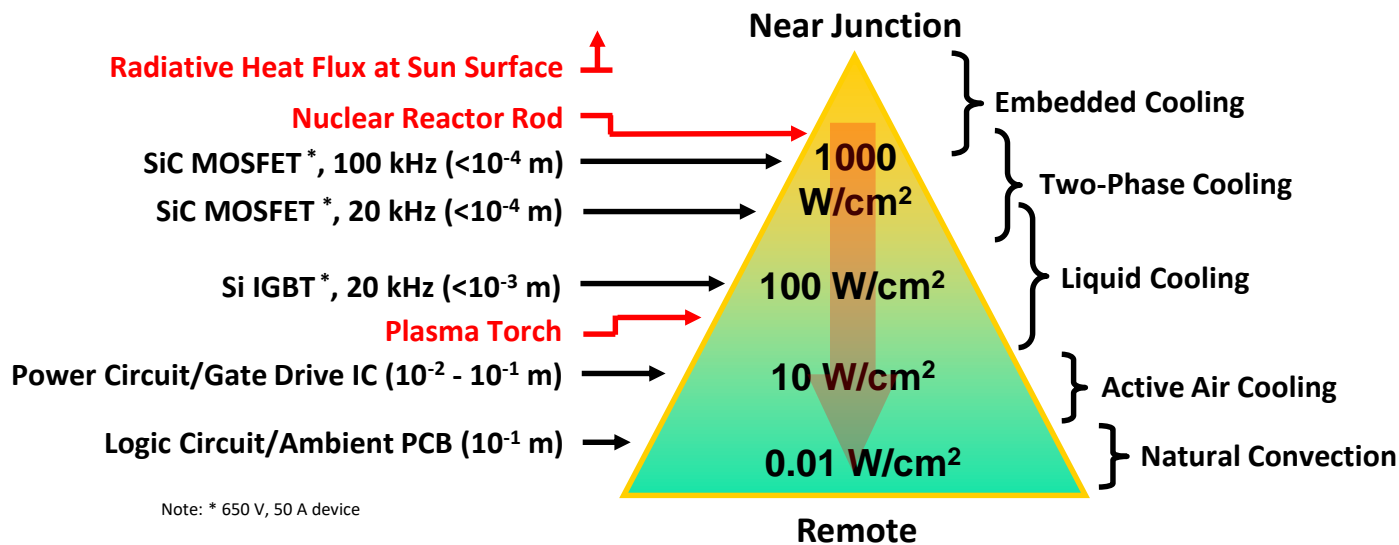
High power density → embedding + integration → novel packaging and different process workflows

# Packaging Trends for Power Electronics

- Future transition to wide band-gap (WBG) devices; e.g., SiC or GaN
  - Device breakdown voltage  $\uparrow$
  - Temperature tolerance  $\uparrow$
  - Switching speed  $\uparrow$ , passive size  $\downarrow$ , power control unit (PCU) size  $\downarrow$



- Trend in device heat flux and cooling technology



Power density drives (conductive path) packaging approach and (convective path) cooling technology

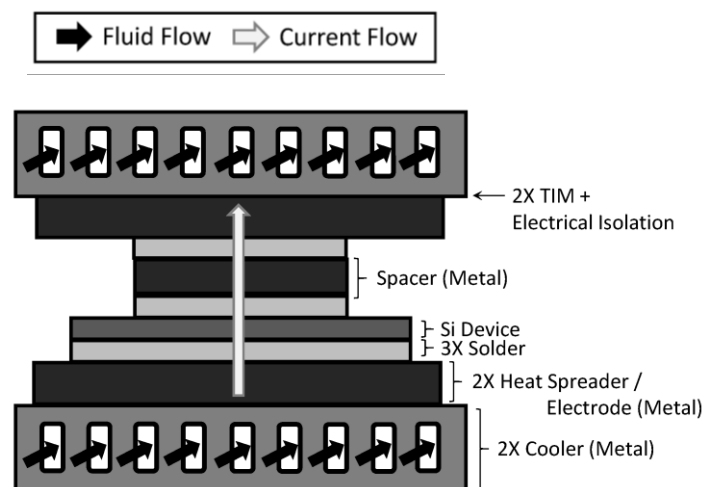
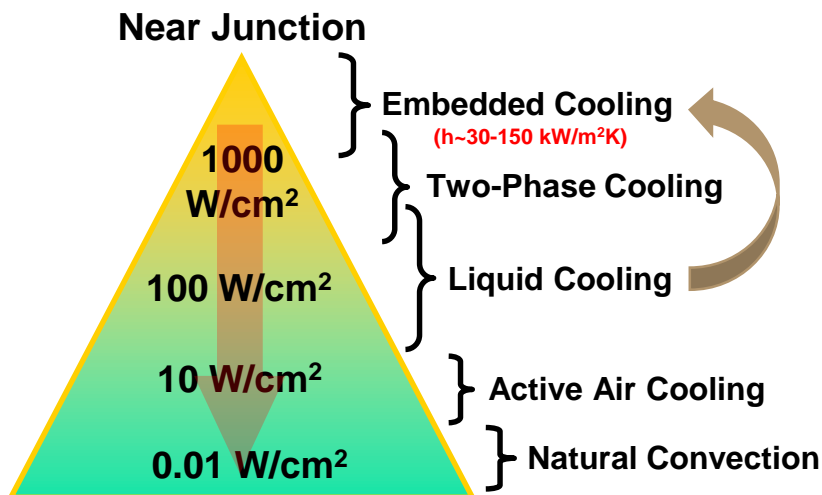
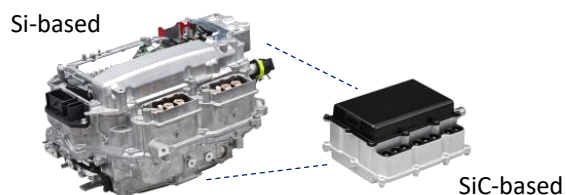
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# Near-Junction Cooling – Motivation

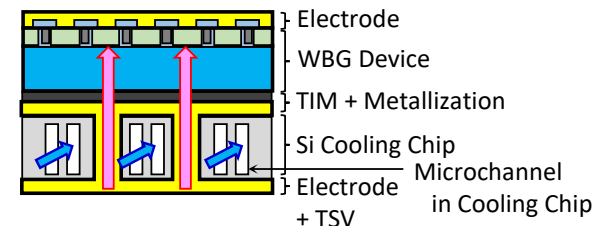
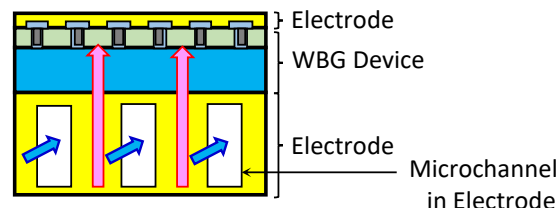
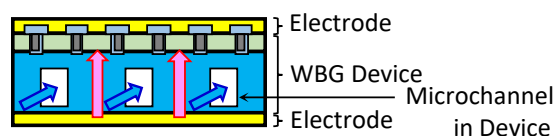
- Order-of-magnitude downsizing requires new packaging concepts
  - Package conductive thermal resistance → driving factor



Conventional Power Card Structure

# Near-Junction Cooling – Concepts

- Three concepts for vertical current WBG devices

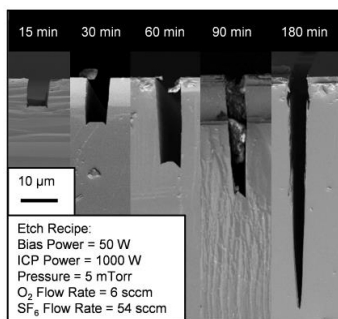


➡ Fluid Flow   
 ➡ Current Flow

**Concept A**  
( $\mu$ Channels Fabricated in Device)

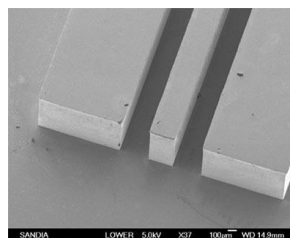
**Concept B**  
( $\mu$ Channels Fabricated in Electrode)

**Concept C**  
( $\mu$ Channels Fabricated in Cooling Chip)



**SiC Etching SoA**

Ref.: Dowling, et al., 2017.  
 DOI: 10.1109/JMEMS.2016.2621131



**LIGA Microfabrication**  
(lithography, electroplating and molding)

Ref.: Michael.Forman - Own work, CC BY 3.0,  
<https://commons.wikimedia.org/w/index.php?curid=7155729>

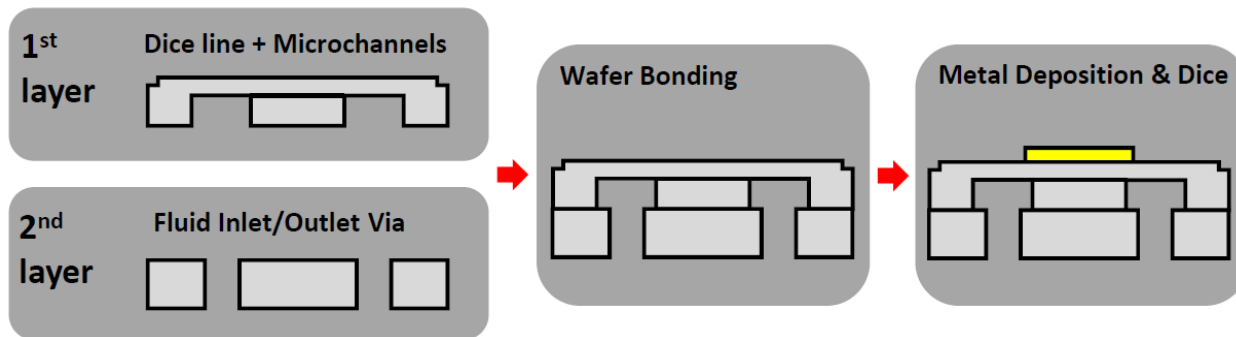
## Qualitative Comparison of Concepts

	Concept A	Concept B	Concept C
Thermal Performance	○	○	△
Electrical performance	△	○	○
Fabrication feasibility	△	×	○

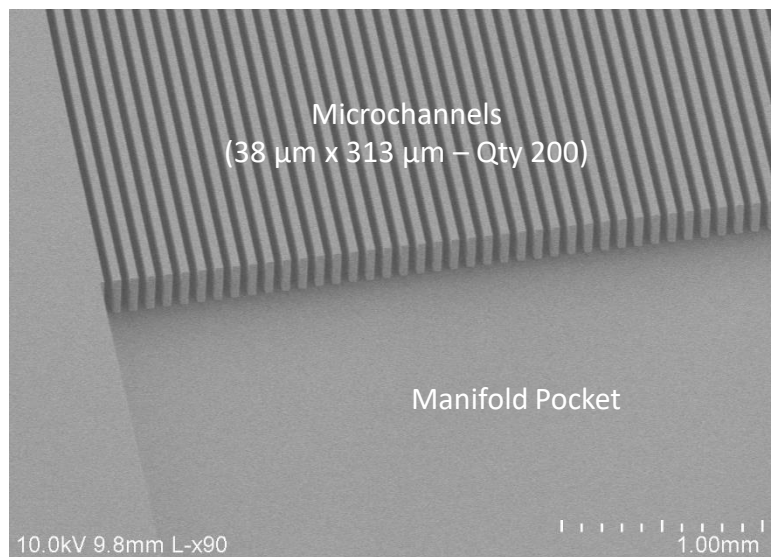
Leverage established MEMS microfabrication processes in silicon to explore Concept C cooling chip

# Near-Junction Cooling – 1<sup>st</sup> Prototype Fab

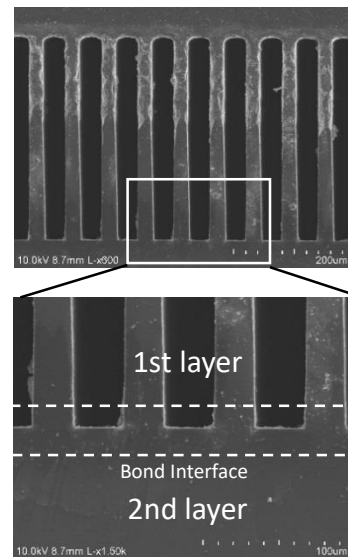
- Straight microchannel prototype fabrication using Bosch process



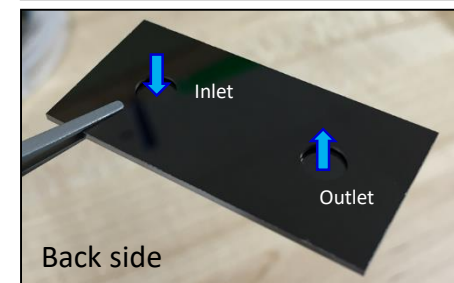
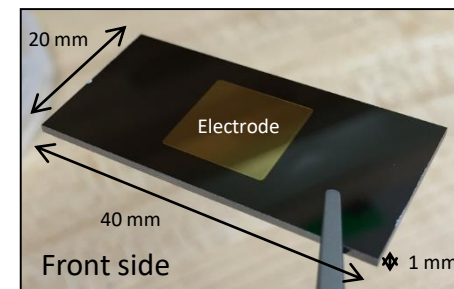
LNF User Facility



SEM Image of 1<sup>st</sup> Layer

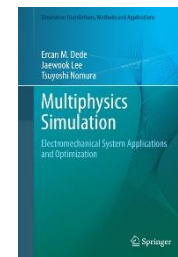


SEM Image of Bonded Assembly Cross-Section



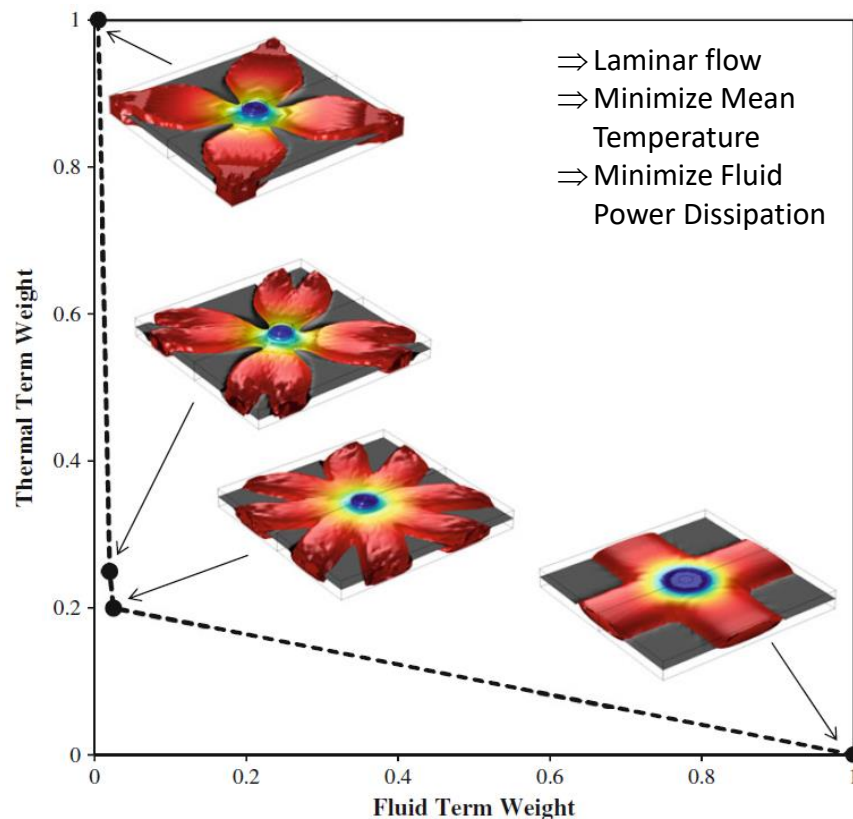
Si Cooling Chip Prototype

# Near-Junction Cooling – 2<sup>nd</sup> Prototype Design

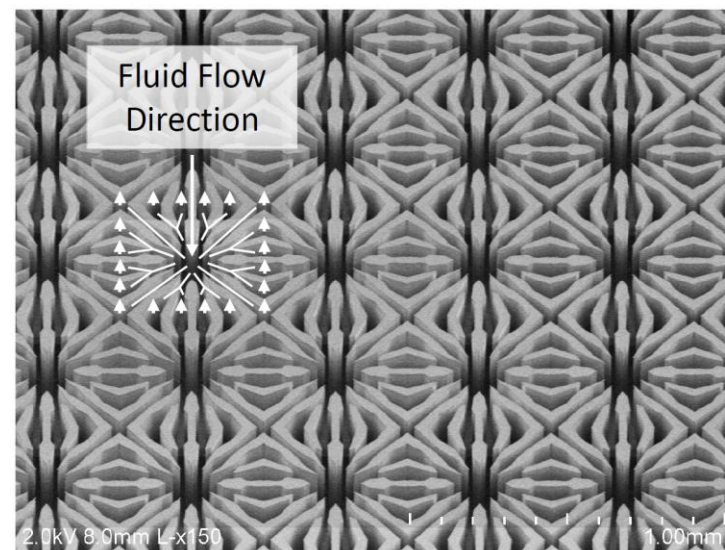
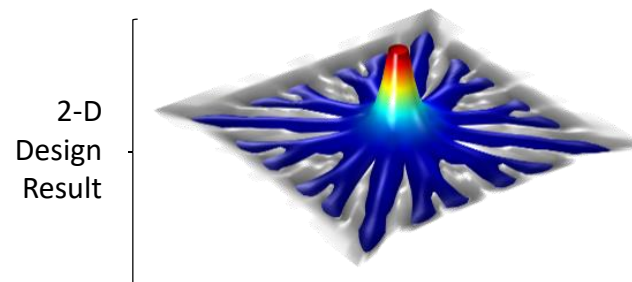


\*Ref.: Dede, et al. (2014) Springer

- Microchannel unit cell design optimized for conjugate heat transfer

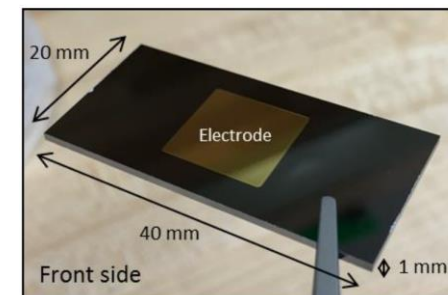
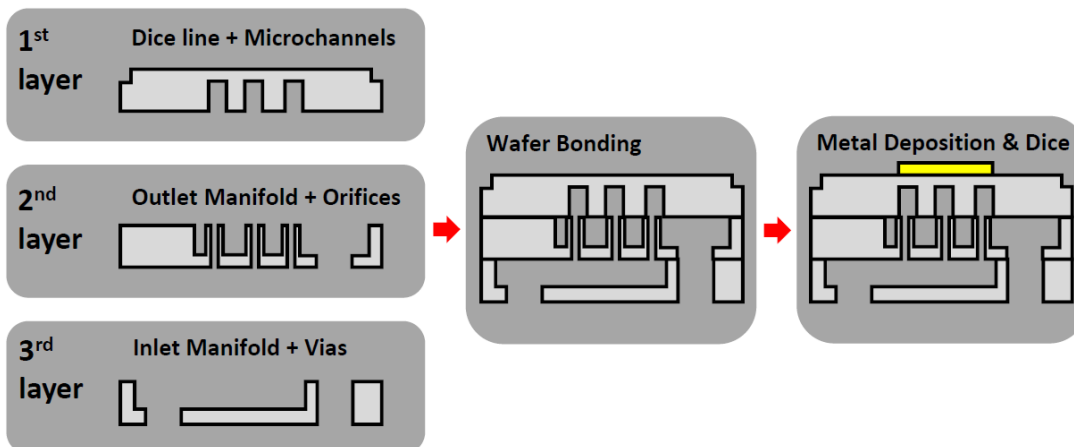


Pareto Front of Multi-Objective Design Optimization in 3-D for Thermal-Fluid Problem

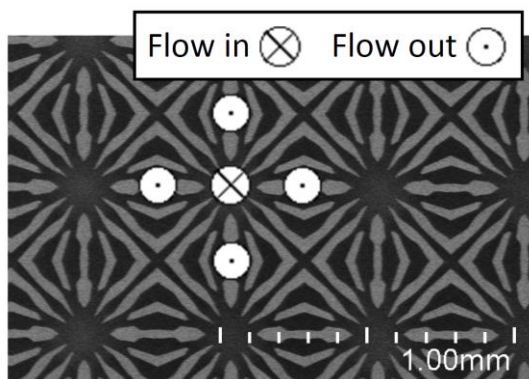


SEM Image of 1<sup>st</sup> Layer Microchannel Structure (Zoomed Isometric View)

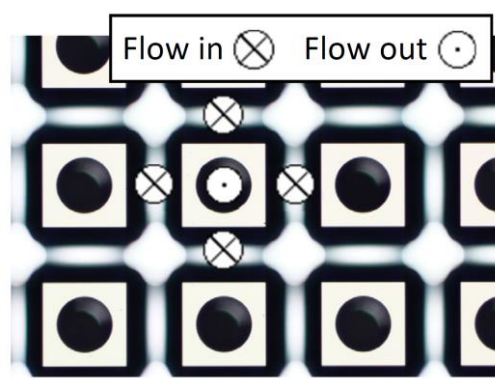
# Near-Junction Cooling – 2<sup>nd</sup> Prototype Fab



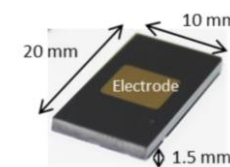
Straight Microchannel Design



1<sup>st</sup> Layer



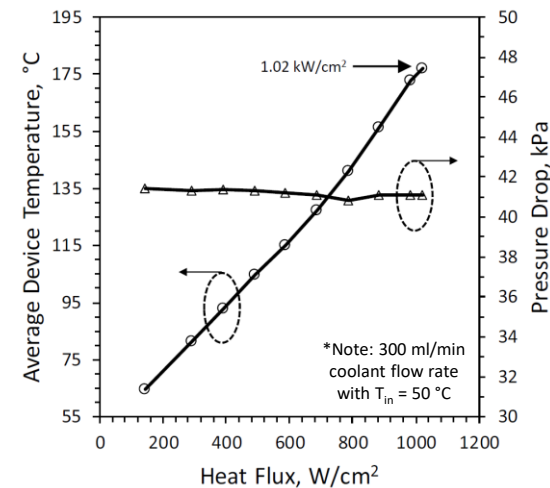
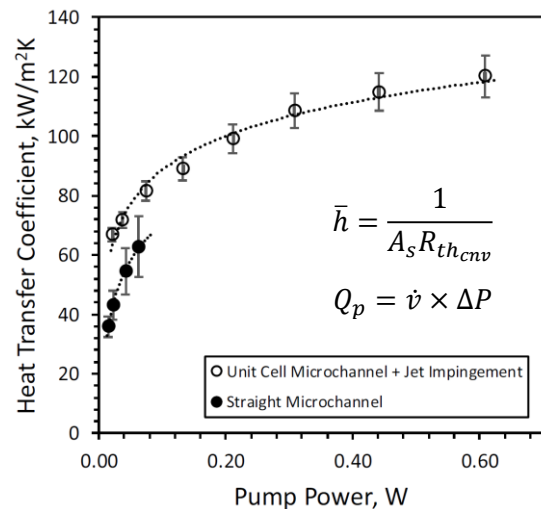
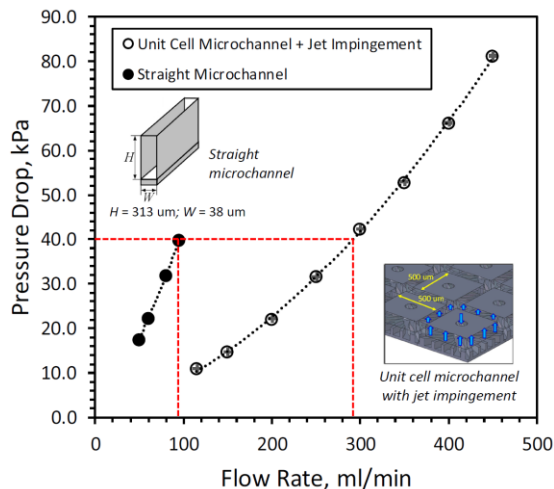
2<sup>nd</sup> Layer



Optimized Unit Cell Design

2<sup>nd</sup> prototype cooling chip design is one-quarter footprint size of straight microchannel cooling chip

# Near-Junction Cooling – Experimental Results



Si TO-247 devices + liquid cold plate

**Conventional**

- 10 x 10 x 5 cm = 500 cc
- Toroidal inductor
- High thermal resistance
- Efficiency = 93% (est.)

~5X Smaller, More Efficient

**Chip-scale cooling**

- 8 x 6.5 x 2 cm = 104 cc
- Planar inductor
- Low thermal resistance
- Efficiency = 97% (est.)

SiC bare dies + chip-scale coolers

Toward Order-of-Magnitude Size Reduction

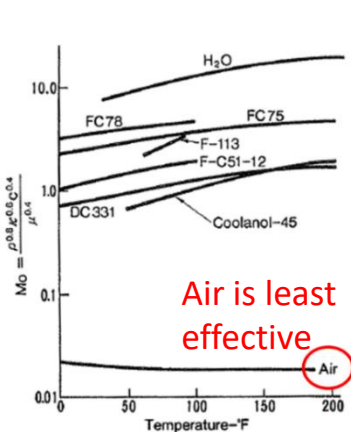
For same  $\Delta P$  , UC microchannel design supports 3X higher flow rate  $\rightarrow$  larger heat transfer coefficient

# Overview

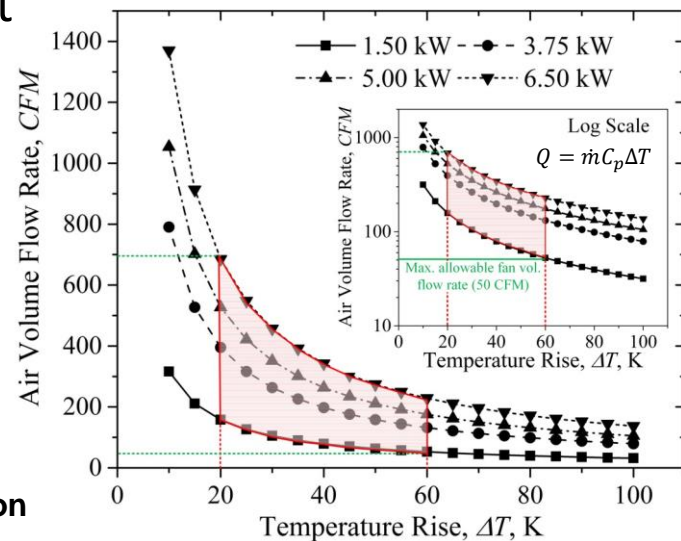
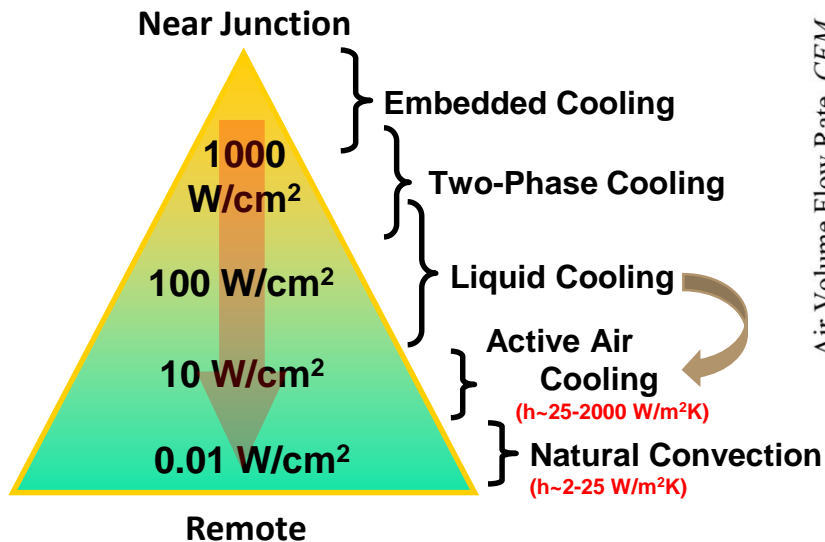
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# Air Cooling – Technology Breakdown

- Ultimate simplicity, but inherently poor coolant

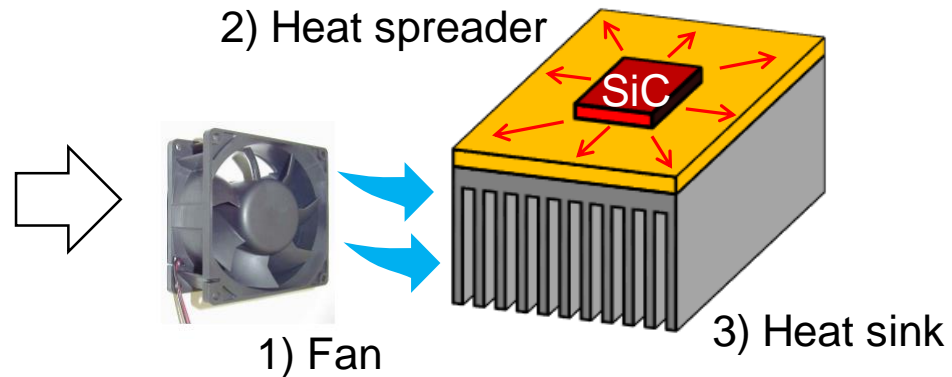


\* Ref.: Kim, et al., 1996



- Key technologies for air cooling system

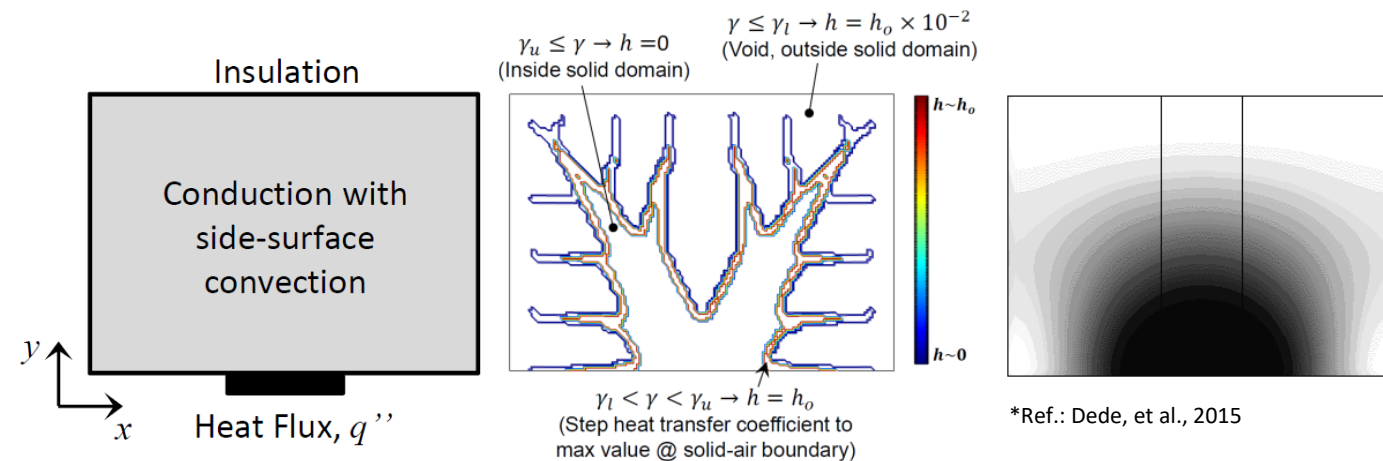
- 1) Efficient air movement
- 2) High performance heat sink
- 3) Extreme heat spreading



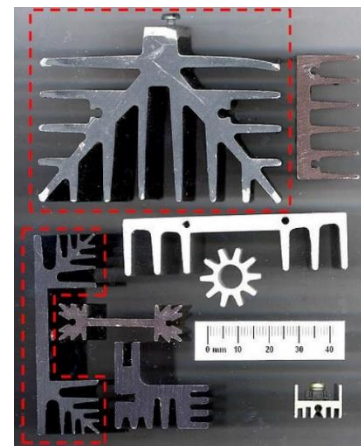


# Air Cooling – High Performance Heat Sink

- Optimization of basic 2-D finned element

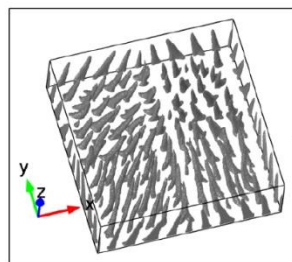


\*Ref.: Dede, et al., 2015

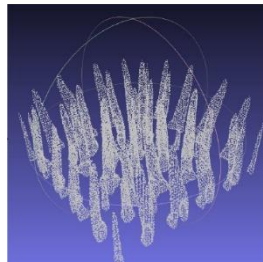


\*Ref.: [https://en.wikipedia.org/wiki/Fin\\_\(extended\\_surface\)](https://en.wikipedia.org/wiki/Fin_(extended_surface))

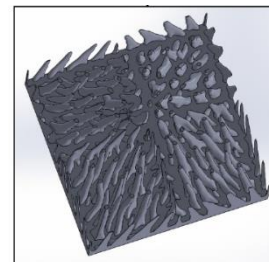
- Application to 3-D heat sink design



3D Optimization Result



Quarter-Symmetry Point Cloud Data



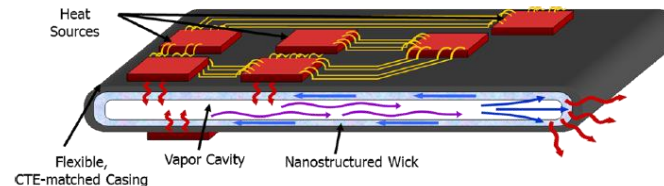
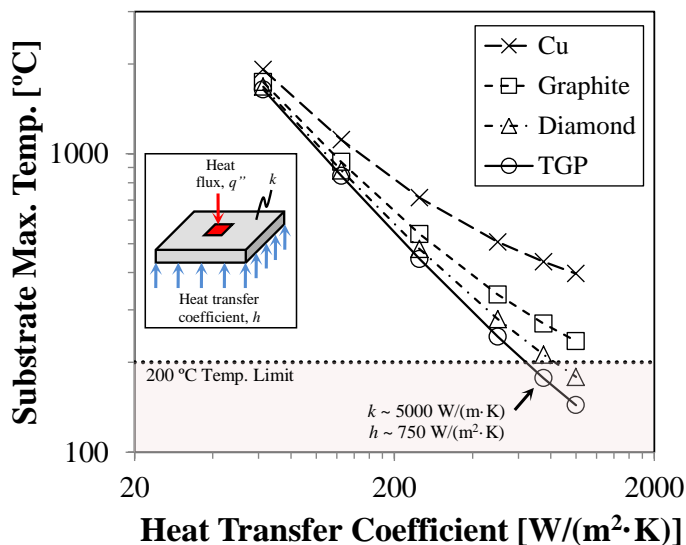
Solid Model CAD Geometry



AlSi12 Rapid Prototype

# Air Cooling – Extreme Heat Spreading

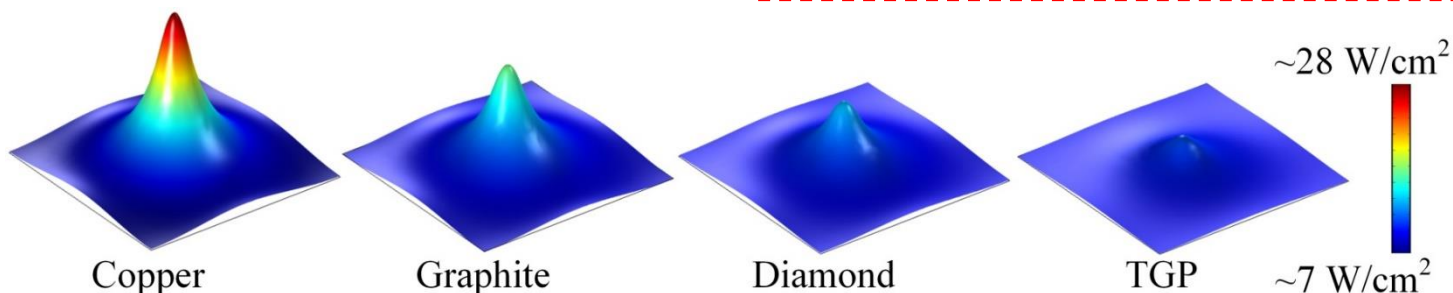
- Efficient heat spreading required to utilize aggressive air cooling



\*Ref.: Bar-Cohen, et al., 2015

## Thermal Ground Plane (TGP) Concept

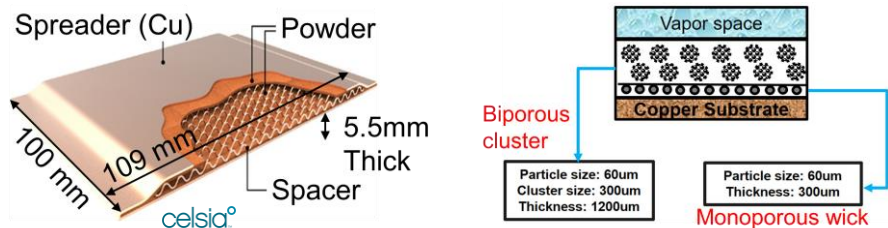
Evaporator Porous Structure	Maximum Heat Flux [W/cm <sup>2</sup> ]	Superheat [K]	Heated Area [mm <sup>2</sup> ]
Electrodeposited Cu [16]	>1200	~10	0.6
Cu $\mu$ -posts + nano-CuO coating [18]	~800	~35	4
Biporous silicon $\mu$ -posts [19]	~730	~13	~6
Sintered Cu [20]	~590	~23	25
Biporous sintered Cu [21]	~990	~147	32
Sintered Cu + feed arteries [17]	~580	~72	100
<b>Technology Gap</b>	<b>&gt; 1000</b>	<b>&lt; 35</b>	<b>&gt; 100</b>



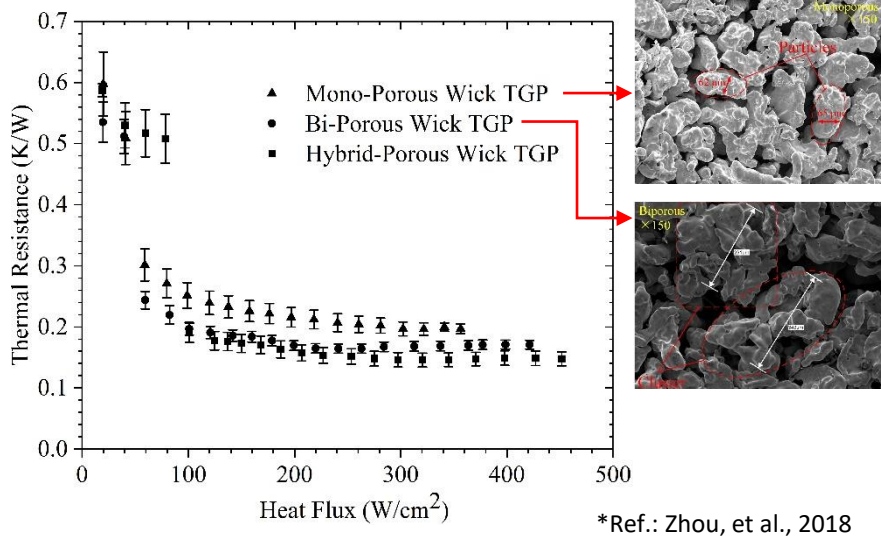
\*Ref.: Dede, et al., 2016

# Air Cooling – Extreme Heat Spreading

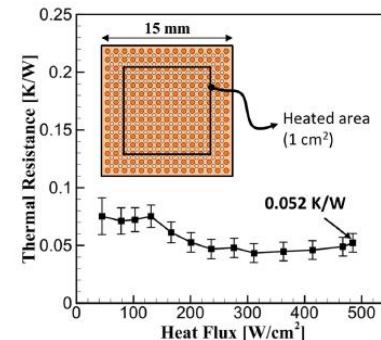
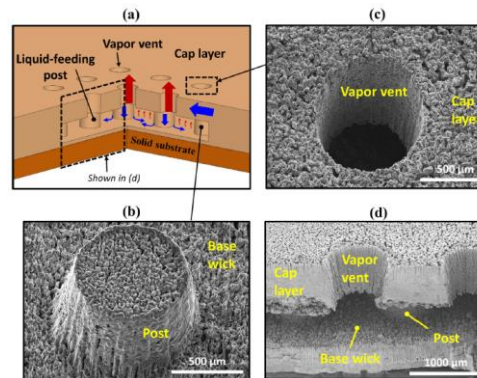
- Novel wick structures to enable high heat fluxes



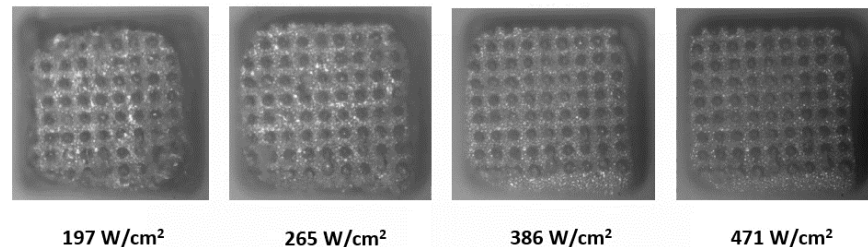
Vapor Chamber & Wick Design



TGP Heat Flux vs. Thermal Resistance



\*Ref.: Sudhakar, et al., 2019



\*Ref.: Sudhakar, et al., In press

At high heat flux, liquid menisci recede to separate liquid feed and vapor vent mechanism

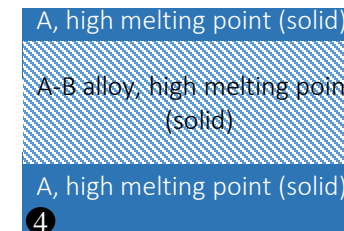
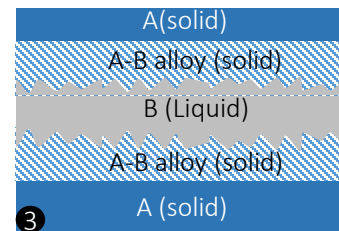
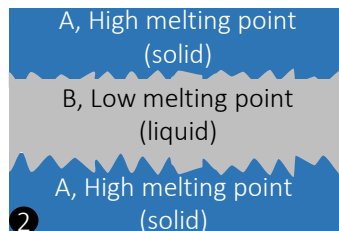
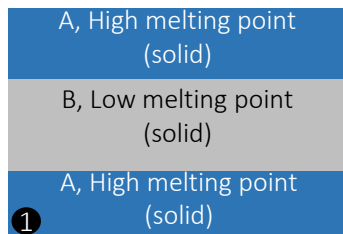
Wick Heat Flux vs. Thermal Resistance

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# Transient Liquid Phase Bonding Overview

- Technology benefits

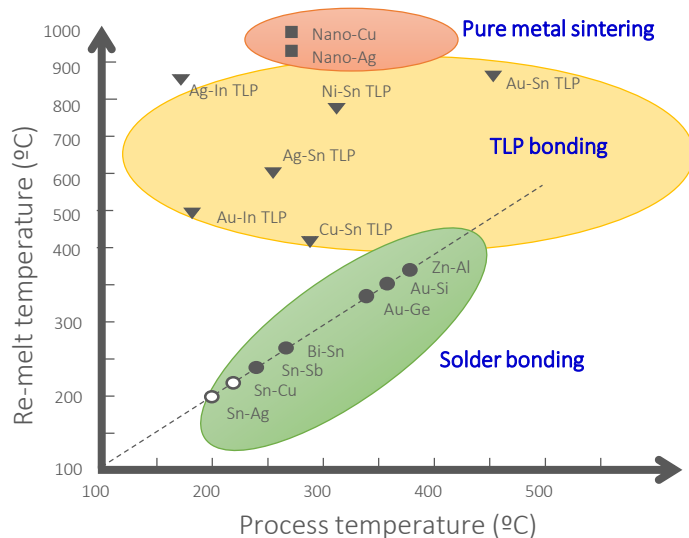


Assembly

Diffusion

Isothermal solidification

Homogenization

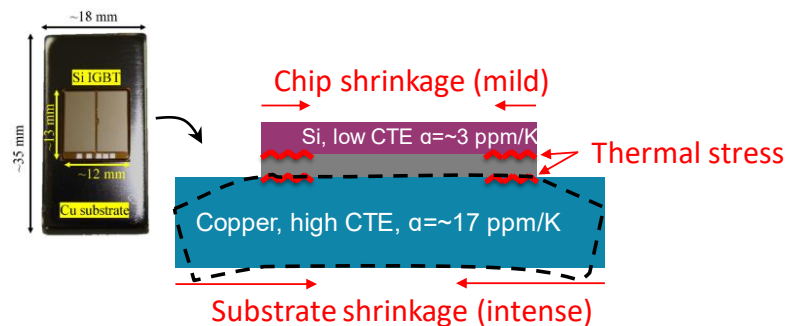


Candidates	Re-melting temp.	Process temp.	Fabrication difficulty	Material cost
Pure metal sintering	○	○	×	×
Solder bonding	▲	▲	○	○
TLP bonding	○	○	▲	○

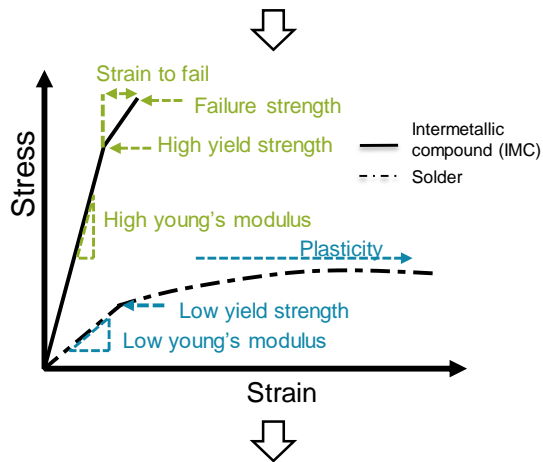
○ Good    ▲ Moderate    × Bad

\*Ref.: Noguchi et al., 2016

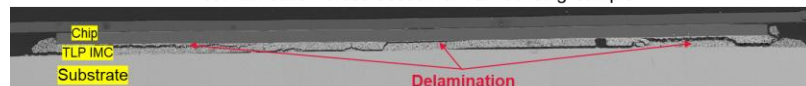
# Die Attach Challenges & Higher Compliance Concept



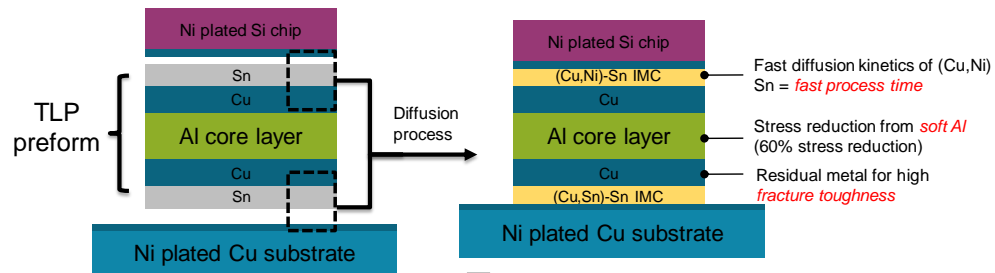
Copper Substrate Die-Attachment



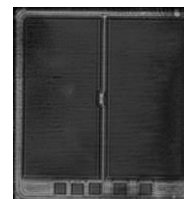
Post fabrication cross-section of TLP bonding sample



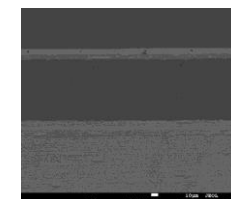
TLP IMCs brittle & susceptible to cracking



C-SAM

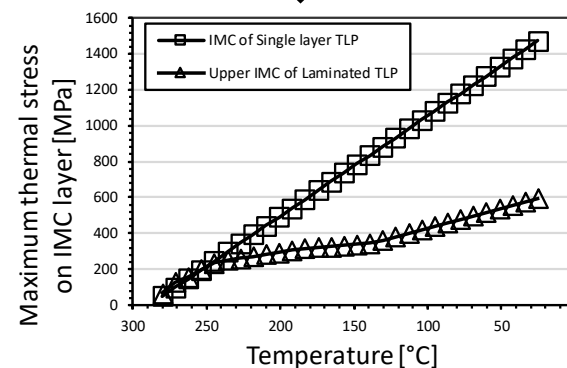


Cross-section SEM



- Ni plated Si chip
- Upper IMC
- Upper Cu
- Al core layer
- Lower Cu
- Lower IMC
- Ni plated Cu substrate

\*Ref.: Liu et al., 2019

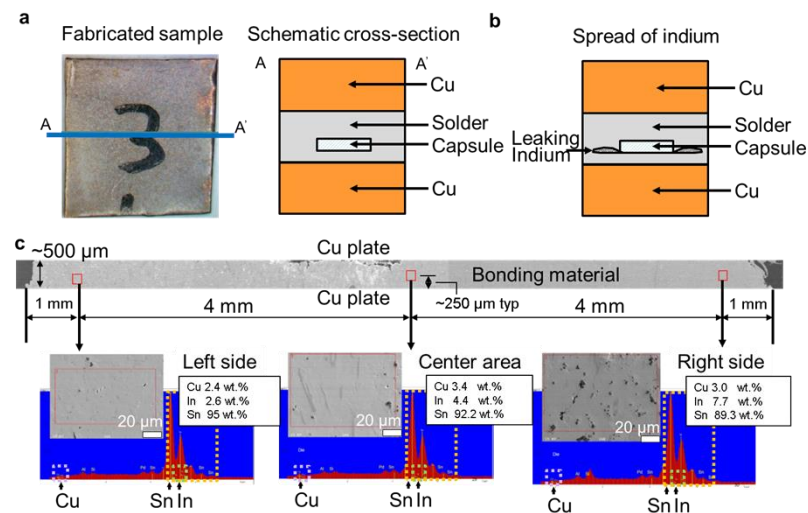
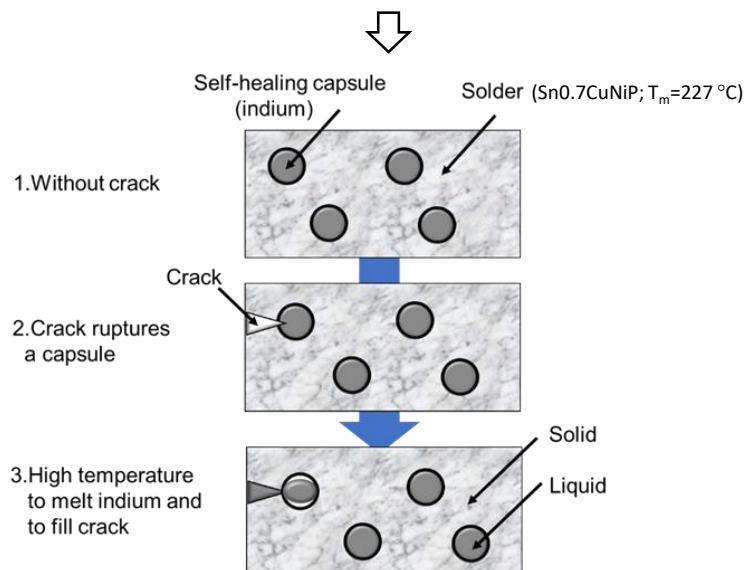
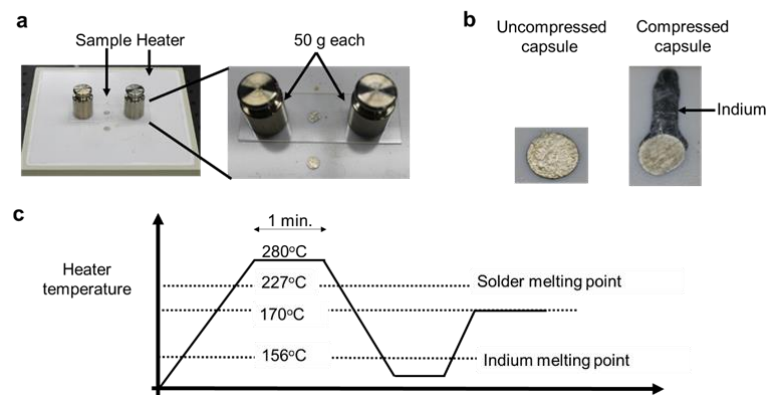
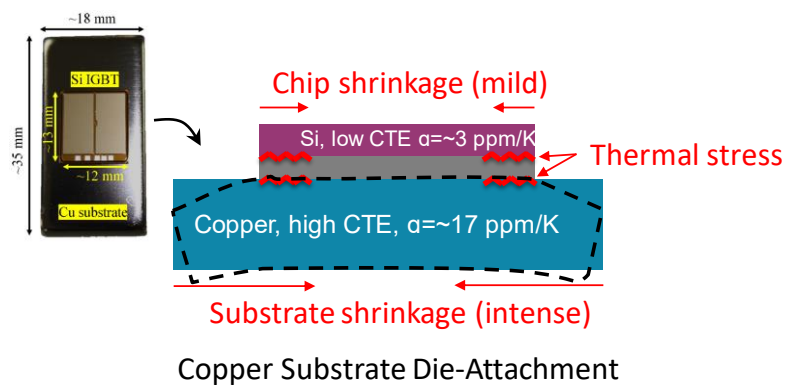


Introduce compliance via laminated preform w/Al core

# Overview

- Characteristics of Wide Band-Gap Devices
- Requirements of Next-Generation Packaging
- Packaging Trends for Power Electronics
- **Relevant Future Technologies**
  - Near-Junction Cooling
  - Thermal Ground Planes
  - Transient Liquid Phase Bonding
  - **Self-Healing Die Attach**
- Conclusions

# Self-Healing Die Attach Concept



Atomic layer deposition (ALD) fabrication of In-Pt core-shell capsule for material system proof-of-concept



# Overview

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# Conclusions

- Higher power density requires consideration of embedding and integration
  - Remote cooling fundamentally limits order-of-magnitude size reduction
  - New packaging strategies and process workflows required
- Near-junction cooling explored as ultra-compact packaging paradigm
  - Straight channel and arrayed hierarchical unit cell flow structures explored
  - Unit cell design exhibits reduced pressure drop and higher heat transfer rates
  - Packaging explored as next step → heterogeneous integration
- Air cooling is robust and simple but requires effective heat spreading for high power density application
  - Heat sink optimization coupled with thermal ground plane technologies may be a solution
- High temperature operation bonding materials are critical
  - Transient liquid phase bonding with increased compliance has potential
  - Self-healing die attach may be disruptive technology to increase package reliability

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