SW Test Workshop
Semiconductor Wafer Test Workshop

Thermal Testing of Singulated Devices Get Us Closer to Known-Good Die/Stack

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Overview

1. Background
2. Die Level Testing
3. Challenges
4. Dual Fluid Thermal Control System
5. Thermal Evaluation
6. Summary

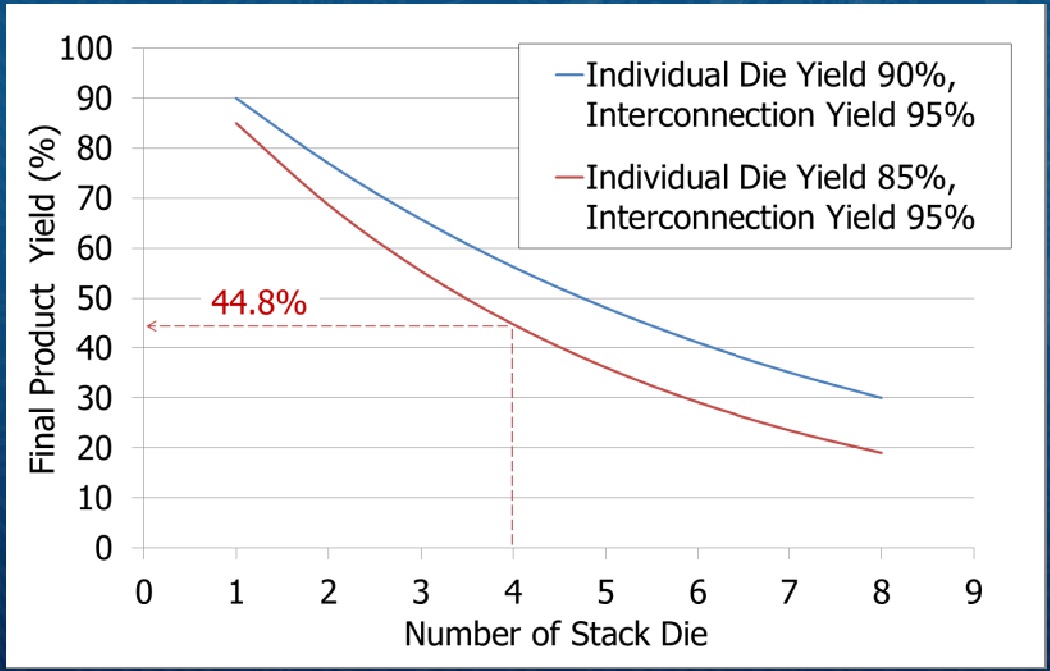
Background

Technology Node Transitions are Slowing

The semiconductor industry moves quickly toward more and more 2.5D and 3D integration.

KGD and KGSD are Critical for 2.5D/3D Integration

Without it final product yield.



$$Final\ Product\ Yield \leq \prod_{d=1}^{n} Yd \times \prod_{i=1}^{n-1} Yi$$

Yd : *Individual Die Yield*
Yi : *Intercconection Yield*
n : *Number of Stack Die*

Test Conference (ITC), 2014 IEEE International
Direct probing on large-array fine-pitch micro-bumps of a wide-I/O logic-memory interface
EJ. Marinissen, B. De Wachter, K. Smith, J. Kiesewetter, M. Taouil, S. Hamdioui

Typical Test Process

Frontend Process → Probe Test → Grinding → Bumping → Dicing

Not enough thermal test of thin wafer in wafer-Level
- Wafer support has high thermal resistance

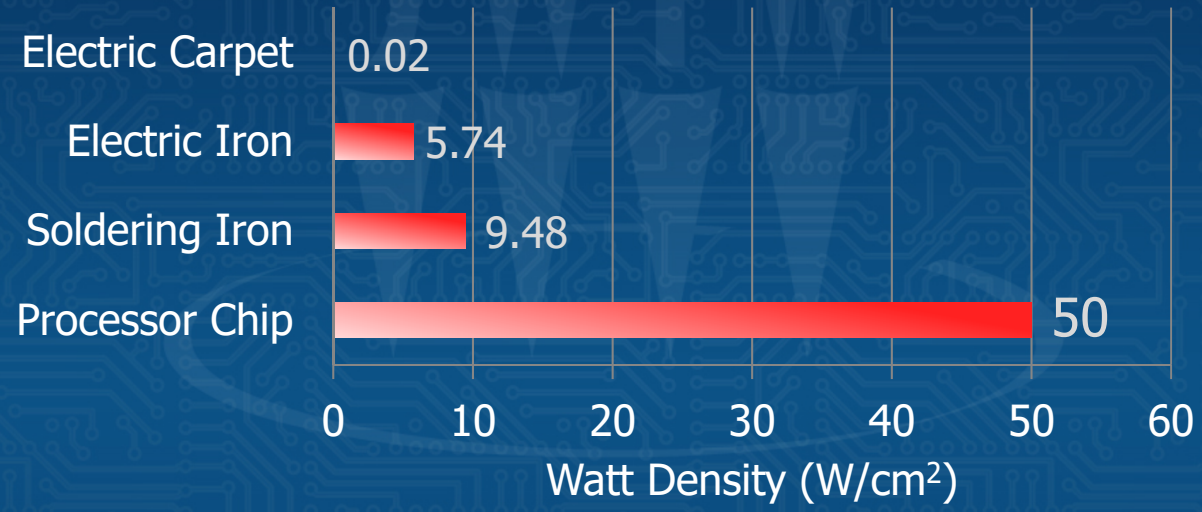
Die Level Test

Target : PKG test on die

Die Bonding → PKG Burn-in → PKG Test → Shipping

Challenges

- **Thermal Control System for High Watt Density**
  - Low thermal resistance is needed to minimize temperature rise in die-level testing

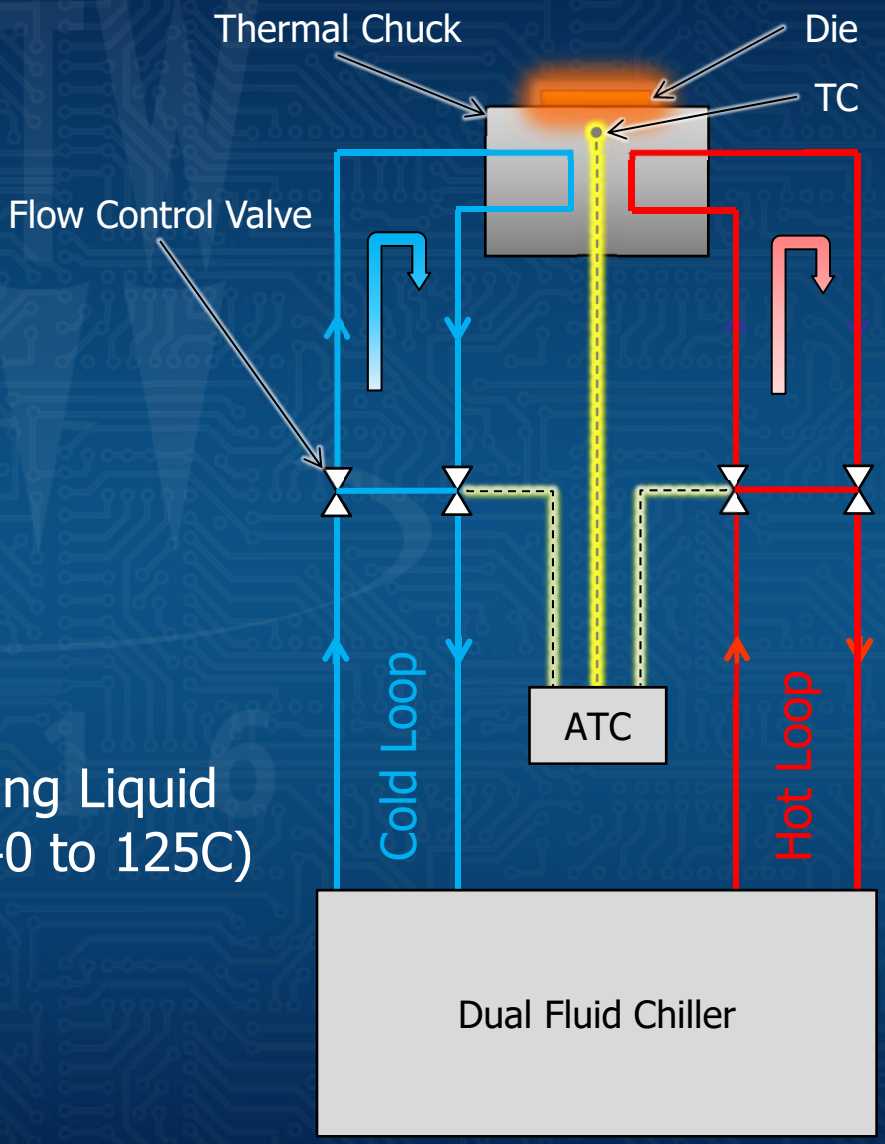


- **Rapid Setting Temperature Change**
  - High response thermal control for high power die
  - Reducing die-level test time
- **Thermal Model for New Thermal Control System**
  - Predict thermal performance for variety die conditions

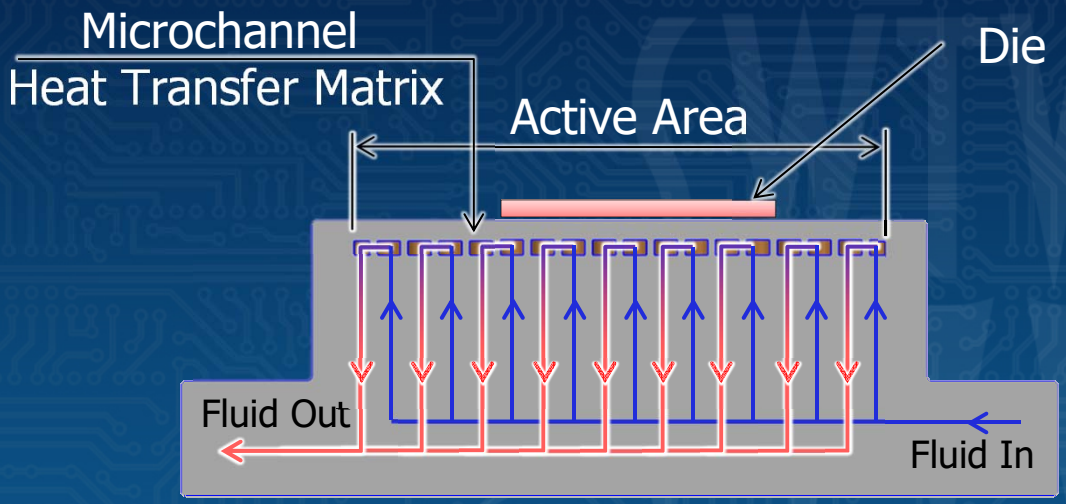
Dual Fluid Thermal Control System

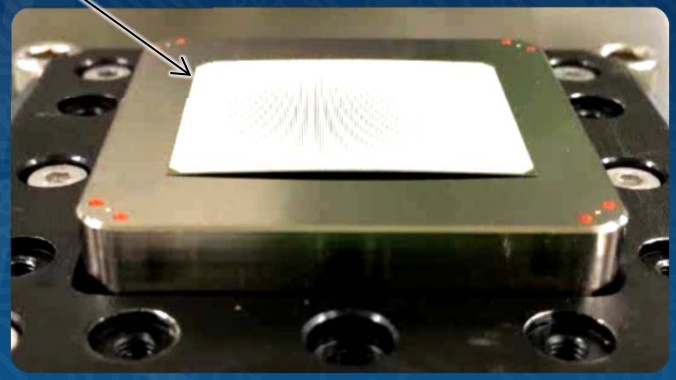
Feature

- Low Thermal Resistance Chuck
  - Liquid Cooling Chuck
  - Microchannel Heat Transfer
  - Low Temperature Gradient
- Rapid Temperature Change
  - Active Thermal Control
  - Switching Hot and Cold Cooling Liquid
  - Wide Temperature Range (-40 to 125C)



Dual Fluid Thermal Chuck





- Low Thermal Resistance
  - Microchannel Heat Transfer Matrix
- Low Temperature Gradient
  - Fresh Coolant is supplied to the entire of surface equally
- Vacuum Chuck
  - Available die size is from 3x3mm to 33x33mm
  - Capable of chucking a warped thin die

HA1000 Die-Level Test System

Die-Level Test Solution

- Thick and Thin Die Handling
  - Die size : 3x3 to 33x33mm
  - Thickness : Minimum 75um
- Fine Pitch Probing
  - Vision Alignment
  - Micro-Bump, Cu Pillar, TSV
- High and Low Temp.
  - Dual Fluid Thermal Control
  - Temp. Range : -40 to 125C
  - Cooling Capacity : 300 Watt

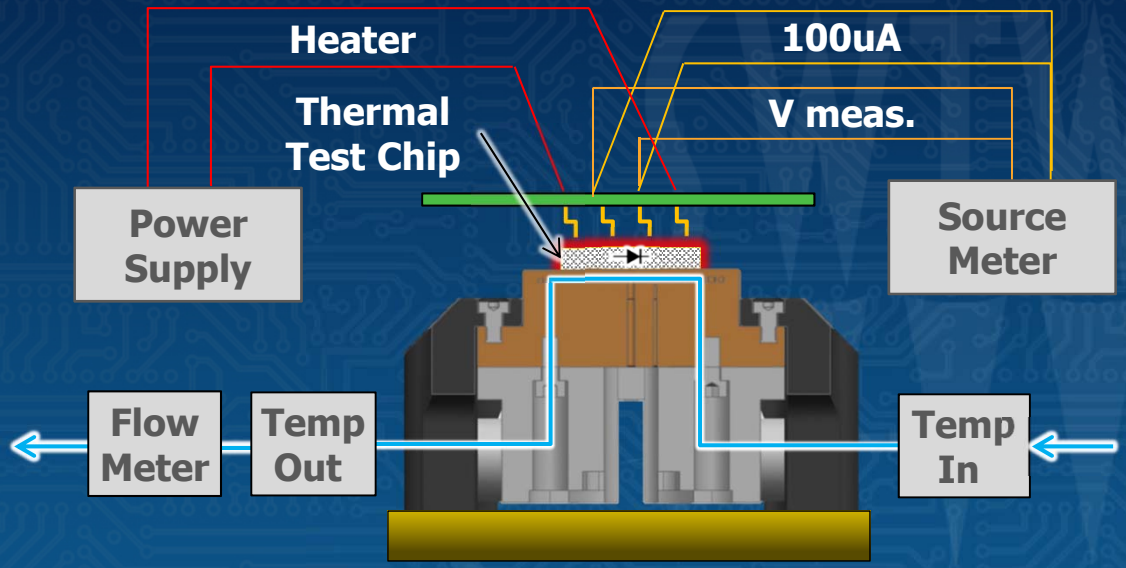
Thermal Evaluation Objectives

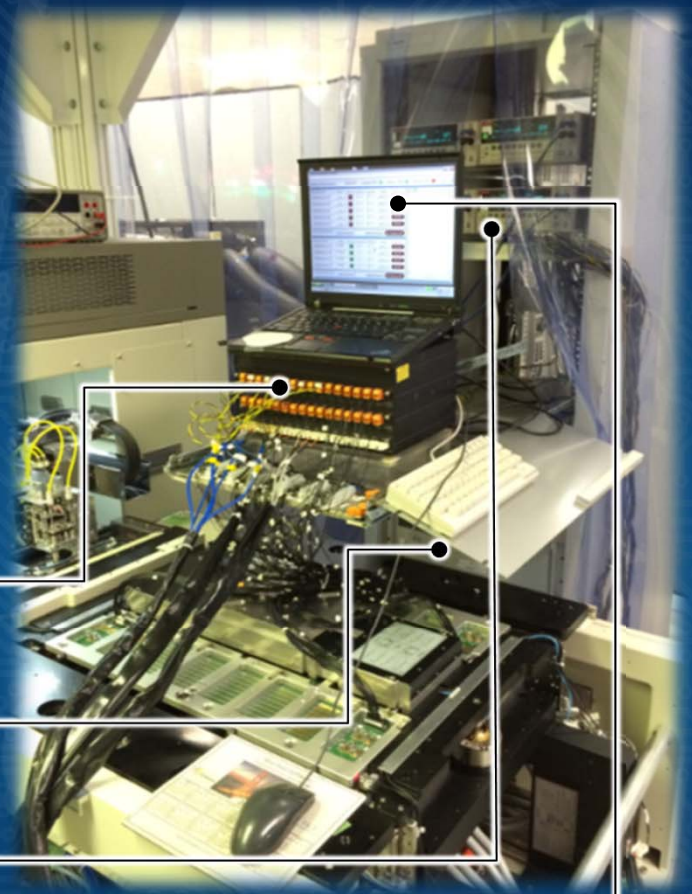
1. Characterize performance of thermal chuck
2. Make thermal model for simulate other conditions
3. Explore possibility of new use models

Characterization of Thermal Chuck

- Evaluation items
  - Steady State Thermal Resistance
  - Temperature Gradient
  - Cooling Capacity
  - Effective Chip Area
  - Single Insertion Multiple Temperature Test

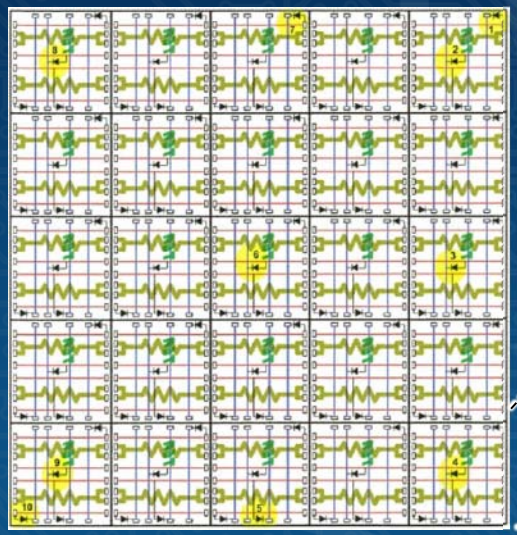
Thermal Evaluation Environment

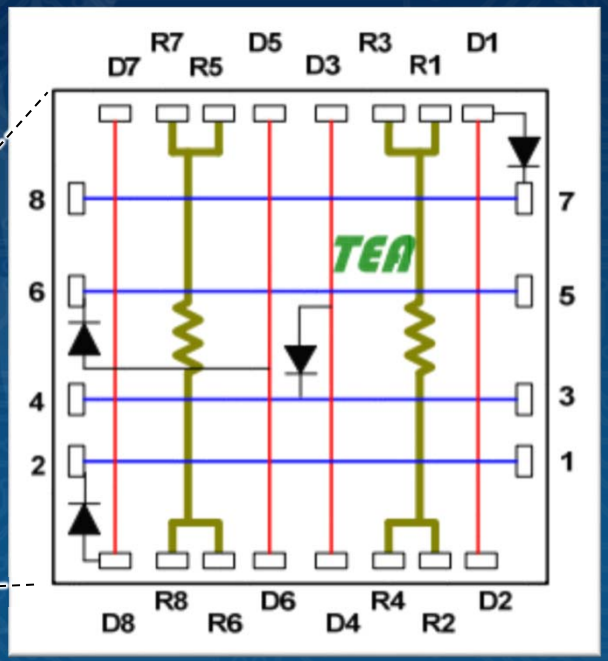




- IOTech Data Acquisition System
  - 48 channels
- Agilent 6651A Power Supplies
  - To power chip heaters
- Keithley 2400 Current Sources
  - To power diodes
  - Monitored by a current meter
- Laptop
  - Application to control power supplies and current sources via GPIB

Thermal Test Chip





5X5 Cell

Unit Cell

- Test chips are made up of a matrix of 2.54 mm square cells
- Each cell contains 4 diodes and 2 heaters
  - Maximum heat dissipation 12W/cell

Evaluation Conditions

Item	Condition
Test Chip Size	1x1, 4x4, 5x5, 10x10 cell (Unit Cell Size 2.54 x 2.54mm)
Max Power	< 380W (Current limit of Probe)
Set Temperature	25C
Fluid	HFE-7500
Flow Rate	1.0lpm
Probe Card	Cobra Probe
Probing Force	25lbs and 70lbs (11.3kgf, 31.8kgf) (Calculation Value from Servo Motor Amp.)

Evaluation Procedure

1. Determine max power for 30C rise

2. Temp vs power, steady state response at max power step
   - Temperature gradient power on and off

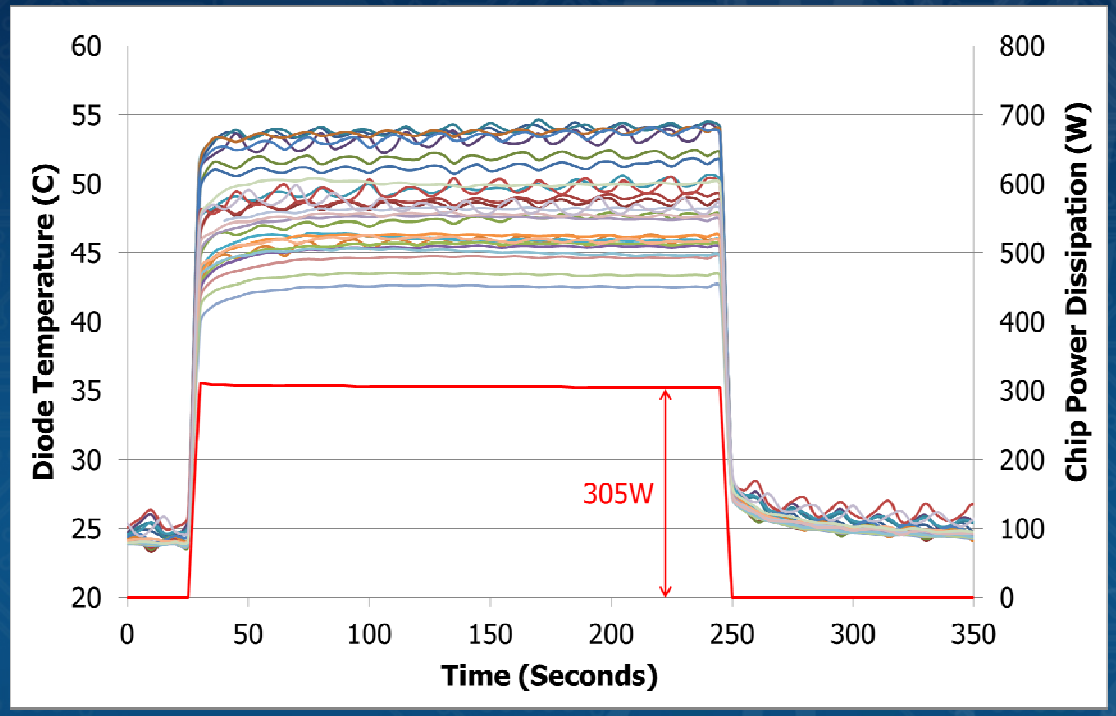
3. Repeat multiple powers
   - 25%, 50% and 75% max power

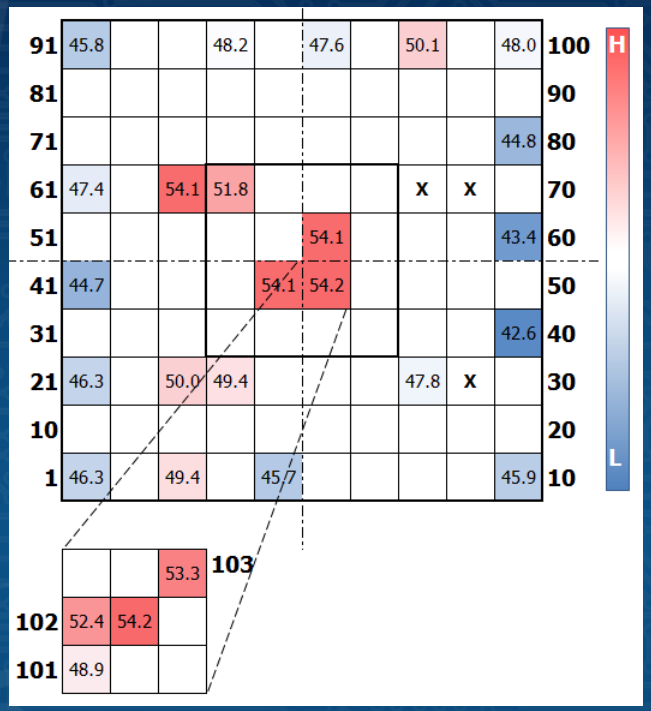
4. Use steady state temp from each power step to plot temp vs power
   - Confirm linearity of temp vs power
   - Slope is steady state thermal resistance

5. Repeat for other chip size, adjusted power, same equipment conditions
   - 25%, 50%, 75%, 100% power

6. Assess impact of effective chip area, using 10x10 cell chip
   - Repeat steady state tests to create temp vs power curve
   - Power only 1x1, 5x5, 5x7 and full 10x10 cell area

Max Power for 30C Rise
(Individual 10x10 Chip)



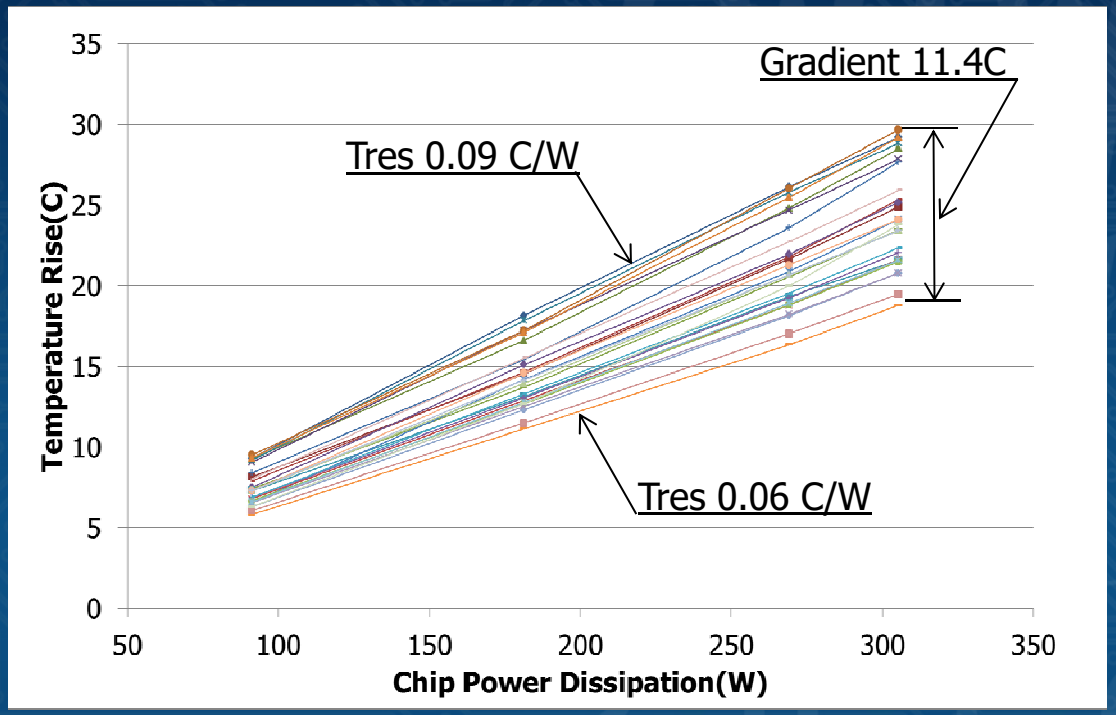


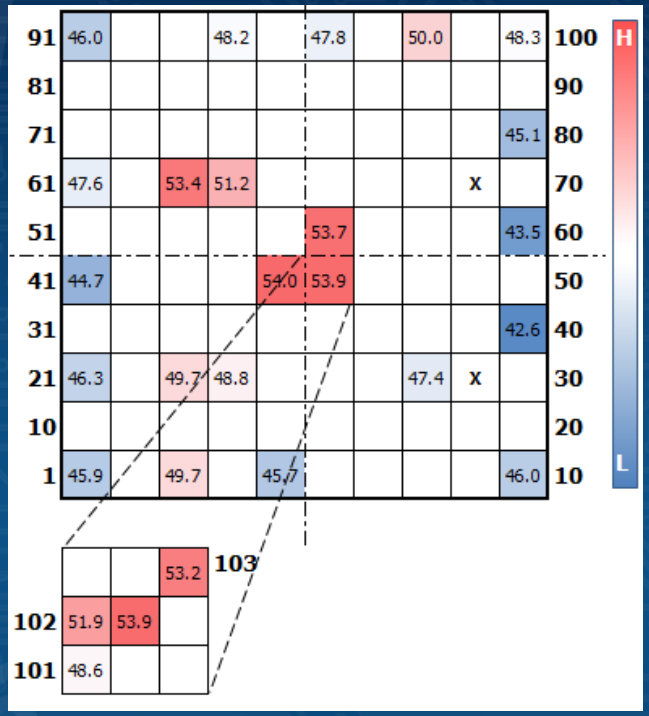
Chuck has cooling capacity of 305W for 30C rise.

- Condition

Die Size : 25.4 x 25.4mm (10X10 Cell)
Fluid Temp, FR : 25C, 1.0lpm
Probe Force : 70lbs(=31.8kgf)

Thermal Resistance and Linearity Check
(Individual 10x10 Chip)



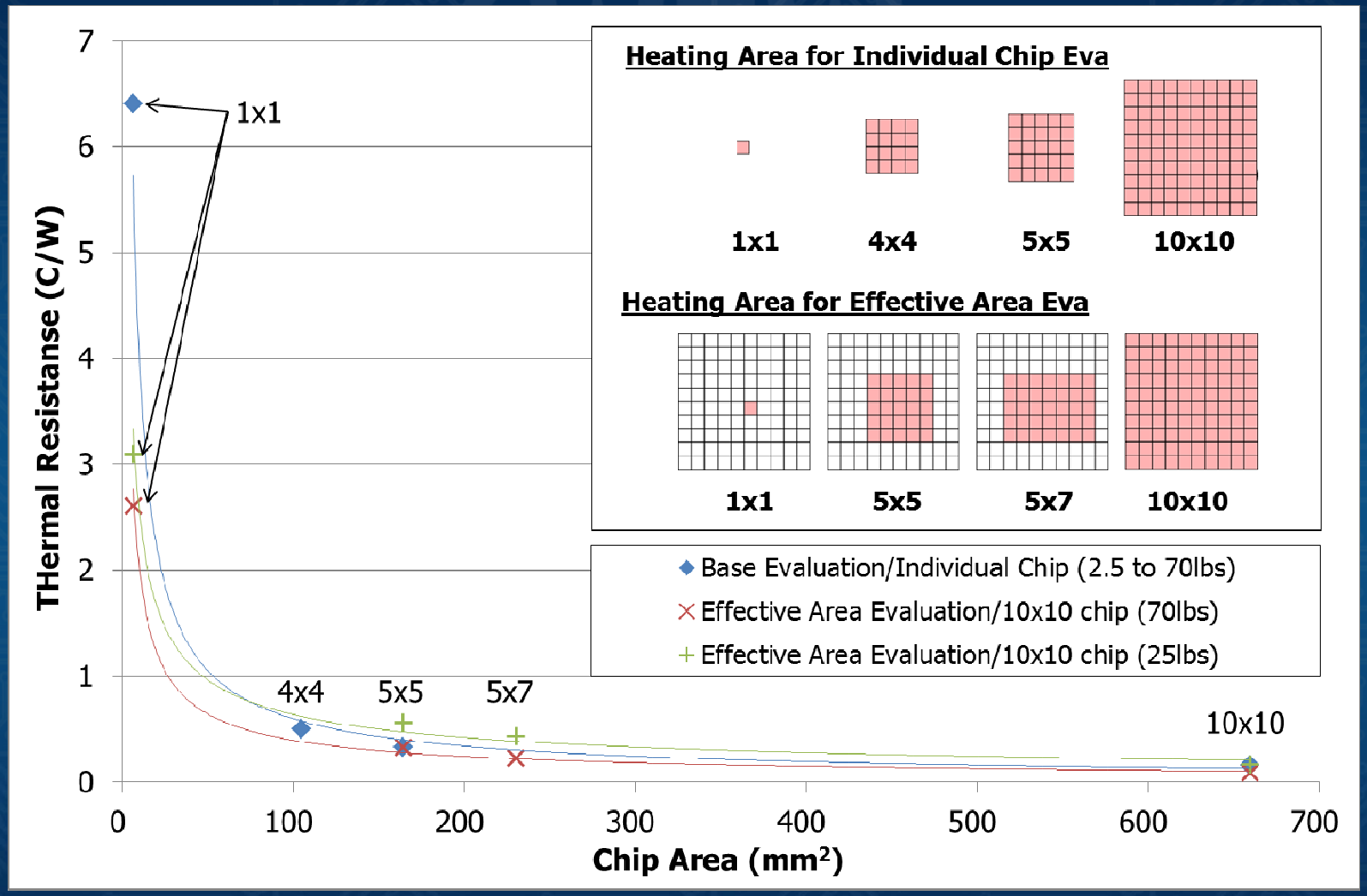


Chuck has a good linearity and Tres is less than 0.09C/W.

- Condition

Die Size : 25.4 x 25.4mm (10X10 Cell)
Fluid Temp, FR : 25C, 1.0lpm
Probe Force : 70lbs(=31.8kgf)

Thermal Resistance of Chip Center
(Individual Chip vs Effective Area)



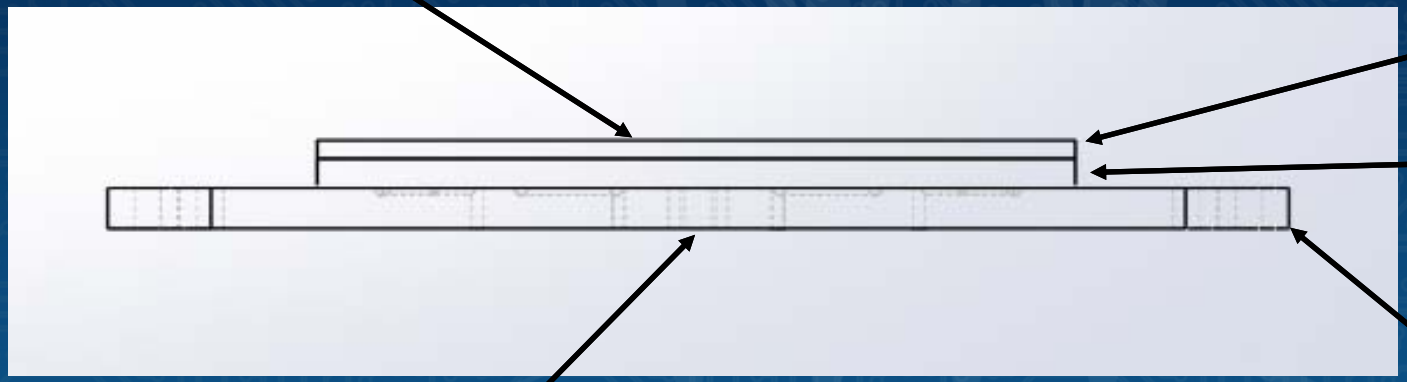
Tres value is depends on the chip area and the contact force.

Thermal Model Details

- **Solidworks CAD model**
- **Comsol Multiphysics finite element analysis**
- **Took advantage of symmetry to cut model in half**
- **10x10 cell chip (25.68 x25.68 mm)**
  - Silicon
  - 200W heat load on die surface
- **Thermal interface layer**
  - Air
  - Increased layer thickness for model simplification, and increased thermal conductivity by the same factor to compensate. This was the starting point.
  - Adjusted thermal conductivity for model correlation – contact is more a weighted average of direct contact and air gap (iterative)
- **Chuck**
  - Copper
  - Heat transfer coefficient on backside to simulate chuck performance (iterative)

Thermal Head

200W heat load

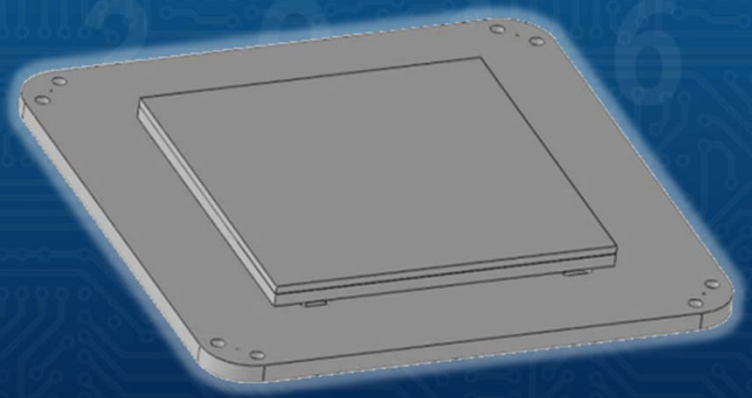


Chip

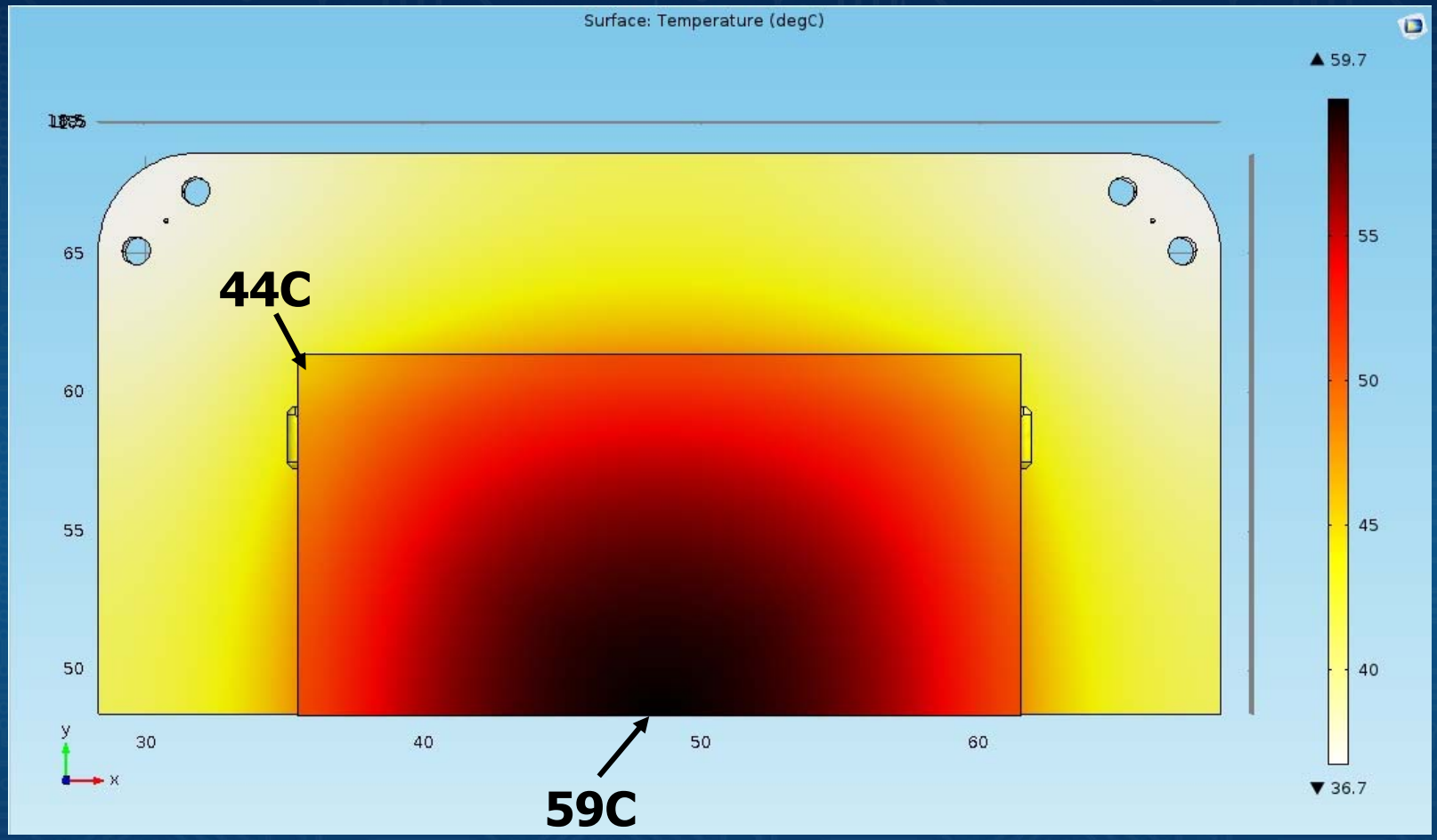
Thermal interface (scaled)

Convective heat coefficient to simulate thermal head performance

Thickness of thermal head from surface to fluid channel

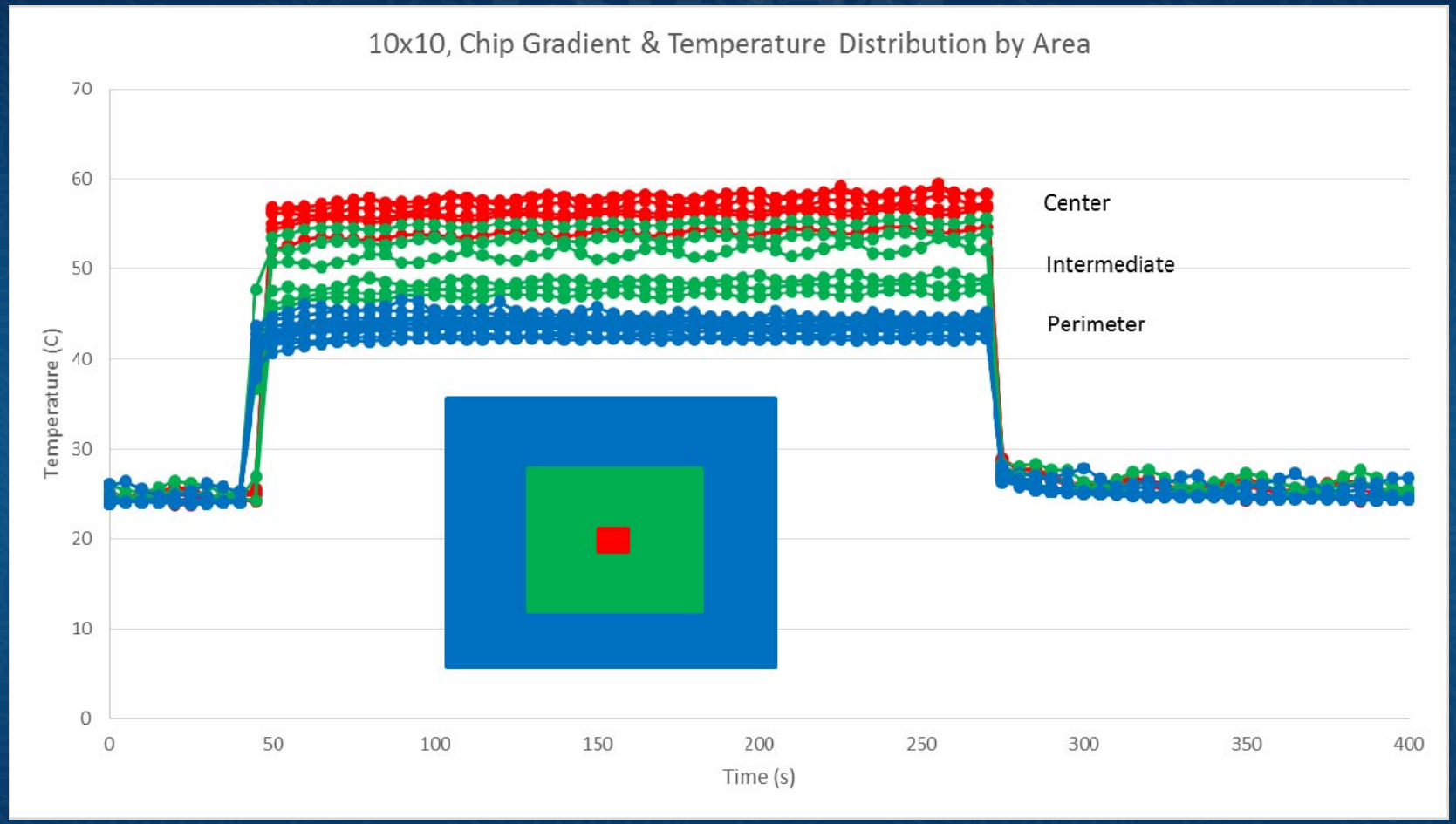


Model Results



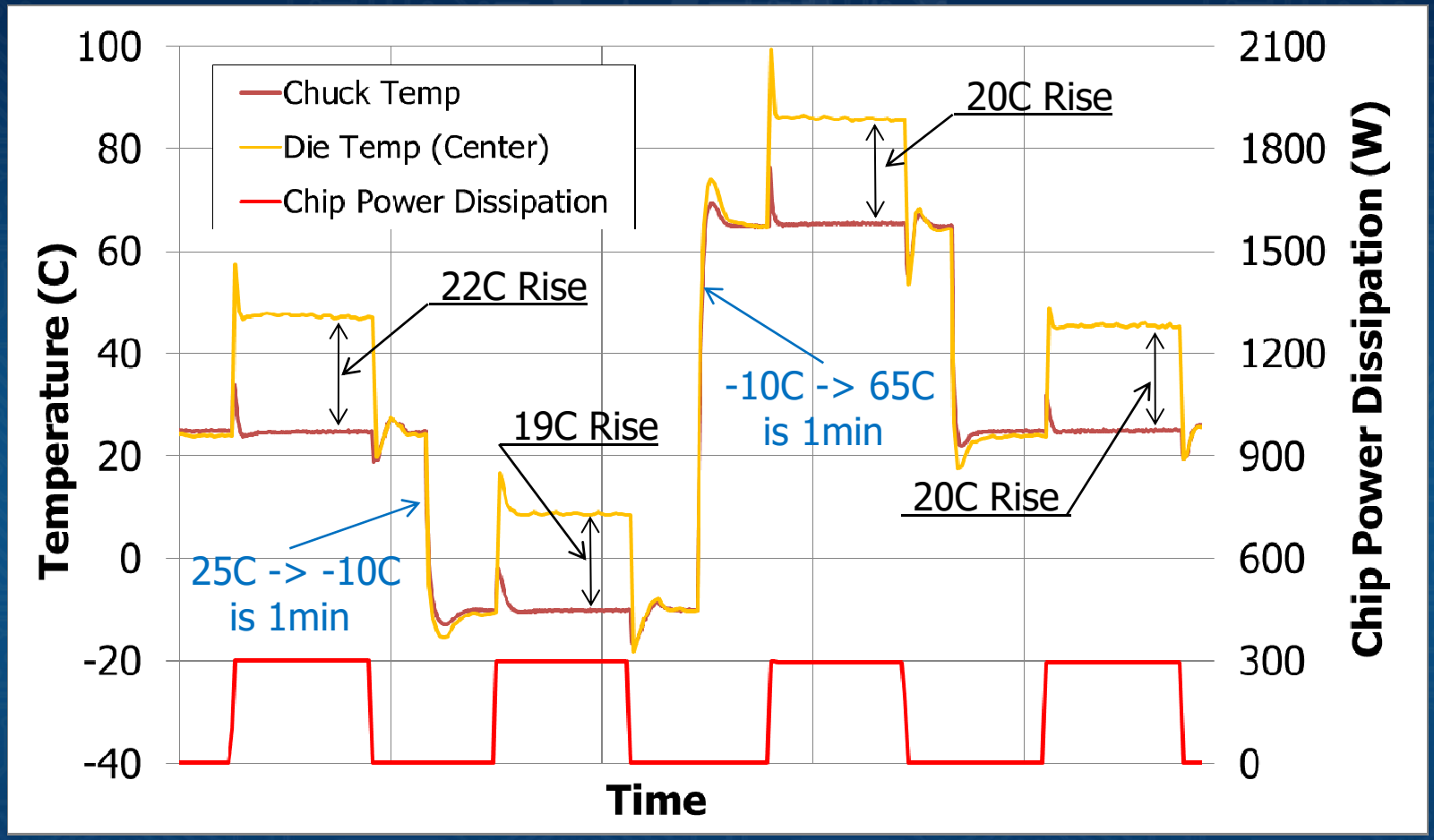
- A properly validated model can be used to predict performance for other device conditions (ie. power maps)

Model Correlation with Measured Data



- 10x10 cell chip, 200W power step at 25lbs force
- Corner-to-center gradient from 42–59 C

Single Insertion Multi-Temp Test
(25C -> -10C -> 65C ->25C)



- Temperature Change Time at 25C -> -10C & -10C -> 65C is 1min.
- Same temperature rise suggests that chuck was able to keep good thermal contact condition at each set temperature.

Summary

1. **Low thermal resistance for a dry condition**
   - 0.09C/W for 2.5cm x 2.5cm
2. **Achieved excellent cooling capacity**
   - 50W/cm^2 for 30C Rise
   - 300W for 30C Rise
3. **Confirmed Single Insertion Multiple Temperature Test**
   - Rapid Temp. Change 25C->-10C & -10C->65C is 1min
   - Possible to Reduce Waiting Time for Changing Temperature
4. **Thermal model can be used to predict performance for other device conditions.**

Dual fluid cooling system can provide a significant value for die-level thermal testing