Final Program and Abstracts

Topical Workshop on Heterostructure Microelectronics for Information Systems Applications (TWHM-ISA '98)

August 30-September 2, 1998

Shonan Village Center
Hayama-machi,
Kanagawa, Japan

Sponsors:
- AFOSR/AOARD
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In Cooperation with:
- The Japan Society of Applied Physics
- The Institute of Electronics, Information and Communication Engineers

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REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. AGENCY USE ONLY *(Leave blank)*	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	15 March 99	Final/ 01 May 98 through 30 Oct.98

4. TITLE AND SUBTITLE
Workshop for Heterostructure Microelectronics Information Systems Applications (TWHM-ISA '98)

5. FUNDING NUMBERS
N00014-98-1-0582

6. AUTHOR(S)
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7. PERFORMING ORGANIZATION NAMES(S) AND ADDRESS(ES)
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8. PERFORMING ORGANIZATION REPORT NUMBER
Regents of The University of Michigan
Tax# 386-00-6309

9. SPONSORING / MONITORING AGENCY NAMES(S) AND ADDRESS(ES)
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10. SPONSORING / MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES

a. DISTRIBUTION / AVAILABILITY STATEMENT
APPROVED FOR PUBLIC RELEASE

12. DISTRIBUTION CODE
DOD

13. ABSTRACT *(Maximum 200 words)*

The 3rd Topical Workshop on Heterstructure Microelectronics for Information Systems Applications (TWHM-ISA '98), held in in Hayama-machi, Japan. A special emphasis was placed on the applications in information systems for this workshop. The Workshop sessions contain a variety of contributions on devices, materials, circuits and systems. The technologies employed are based on heterostructure bipolar transistors, heterostructure field effect transistors and resonant tunneling diodes, and make use of a variety of heterostructure material systems including III-Vs (e.g. GaAs, InP and related compounds), group IV semiconductors (e.g. SiGe), and wide bandgap semiconductors (e.g. III-V Nitrides and SiC). Special emphasis was also placed on the effective insertion of these devices and circuits into systems such as mobile, fiber optic, space communications, as well as signal and data processing.

14. SUBJECT TERMS	15. NUMBER OF PAGES
Heterostructure devices, III-V and SiGe components, Systems for Communication and Information	113
	16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT

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Preface

Welcome to the 1998 Topical Workshop on Heterostructure Microelectronics for Information Systems Applications (TWHM-ISA '98). Since 1994, when this Workshop began in Susono, it was followed by another successful meeting in Sapporo two years later and has become a well respected and recognized event for bringing up the latest achievements of Heterostructure Microelectronics as viewed by industry and university experts in the field. This year TWHM is being held in Hayama-machi on the beautiful Miura Peninsula and a new tone has been added to it by placing special emphasis on heterostructure microelectronics applications on information systems. This change is reflected by the addition of ISA to the Workshop name, and was prompted by the evolution of heterostructure microelectronics witnessed over the previous events and the fact that the heterostructure issues we address are no longer a future dream, but actual applications.

The sessions contain a variety of contributions on devices, materials, circuits and systems. The technologies employed are based on heterostructure bipolar transistors, heterostructure field effect transistors and resonant tunneling diodes, and make use of a variety of heterostructure material systems including III-Vs (e.g. GaAs, InP and related compounds), group IV semiconductors (e.g. SiGe), and wide bandgap semiconductors (e.g. III-V Nitrides and SiC). Special emphasis is also placed on the effective insertion of these devices and circuits into systems such as mobile, fiber optic, space communications, as well as signal and data processing.

We would like to take this opportunity to thank the workshop committee members of TWHM-ISA '98 for soliciting papers and arranging the excellent program. The financial and organizing support made by the Asian Office of Aerospace Research and Development (AOARD), and the Office of Naval Research (ONR) are also greatly appreciated. Technical sponsorship by the IEEE Electron Device Society, the Japan Society of Applied Physics, and the Institute of Electronics, Information and Communication Engineers has also been instrumental in the organization of this Workshop.

On behalf of the Organizing Committee and the Technical Program Committee, we welcome you to the 1998 Topical Workshop on Heterostructure Microelectronics for Information Systems Applications. We hope you will enjoy the presentations and encourage you to share your experience with others in order to ensure a very productive Workshop and contribute to the successful expansion of the field of Heterostructure Microelectronics.

Dimitris Pavlidis
Workshop Co-Chair

Tadao Ishibashi
Workshop Co-Chair

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Collected Abstracts

Compound Semiconductor Devices for Future Data Transmission Systems

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Applications of compound semiconductor devices are very diversified and fragmented, ranging from low volume, high priced parts for military and space systems to volume RF devices for commercial and consumer electronic applications, where priceing pressure are intense. The largest volume markets are communications, such as mobile communications, satellite receivers, and fiber-optic communications. As operating frequencies move up in future systems, this will give new markets to compound semiconductor devices. We examine the key technology driving the use of compound semiconductor devices in future systems.

RF applications in mobile communication handsets are expected to provide the largest volume application for compound semiconductor devices, but are fiercely contested. Si and compound semiconductor devices are battling to secure a place. The key trends favoring the use of compound semiconductor devices are the move to the digital systems which places greater demands on power consumption, requiring high efficiency and linear devices, to higher frequencies (1.8 - 1.9 GHz) and to lower operating voltage (2 - 3 V). Processes such as Bi-CMOS and SiGe present a serious threat in the longer term, although both are likely to be more expensive than GaAs. But the issues which remain as obstacles for compound semiconductor devices include cost, integration levels and a negative voltage supply. The main advantage of Si is its well proven maturity and the size of the industry. Si offers large and low cost substrate. The use of compound semiconductor devices prohibits the implementation of entire system on a one chip. On the contrary, Si has the potential to completely integrate RF sub-systems and VLSI base-band functions on a single chip. At present, it is harder for GaAs to compete on the receiver, where low cost and high integration level Si is available. The power amplifier is a key standard product for compound semiconductor devices, but they also face strong competition from Si-MOSFETs which can operate under a single positive voltage supply, and this is highly preferable. Several compound semiconductor devices, such as HBT, can operate under a single positive voltage supply. Heterostructure-FETs(HFETs) are another contender. We developed new enhancement mode HFETs(Vth>0.3 V) to realize the operation under a single positive voltage supply. We have demonstrated the performance capability of this enhancement mode MMIC for the high power requirement of the GSM band[1], which is by far the most mature of all

digital cellular systems. This approach can be extended to higher frequencies and lower voltages where compound semiconductor performance can be fully utilized. It is a reliable, low system cost solutions for future mobile communication handsets applications.

A range of technologies designed to help control road traffic, increase safety, reduce pollution and contribute to road-maintenance costs are under way in North-America, Europe and Japan. Many of these systems will require the use of high performance microwave, millimeter-wave components. The longer term impact of these development is expected to be of significance in terms of demand for compound semiconductor (GaAs and possibly InP) devices. However, there are many cost and technology trade-off for these systems, especially for collision warning systems at 76 GHz, which is the frequency allocated in the world-wide for this application. Automotive supply companies are developing low-cost collision warning technologies for the passenger car market. It is expected that the systems will be available by the end of the decade. This also will provide the large volume application for compound semiconductor devices. Flip-chip bonding is one of the attractive technologies for reducing fabrication and assembly costs and for improving the performance of MMICs in W-band applications. In addition, coplanar wave guide transmission line technology should be used to develop low cost flip-chip MMICs since there is no wafer thinning process, no via etch and no backside processing of the wafer. We designed and fabricated W-band flip-chip MMICs with coplanar wave-guide transmission lines using 0.15 μm InGaP/InGaAs HEMT technology. [2)]

Satellite communication systems include GPS, VSAT, DBS-TV, and satellite-based PCS. Several major consortia are developing PCS based on low earth orbit. All these PCS systems require compound semiconductor devices. A key technology for this sector is p-HEMTs. The high transconductance and current of these devices result in improved gain and power add efficiency at Ku-band. While the potential demand on compound semiconductor devices arising from these systems is very large, issues remain to be solved before the programs start, especially raising finance and reducing the price of RF components. As mentioned above, flip-chip bonding is the attractive technologies for satisfying the low cost and high volume requirements of the user terminals.

To realize these future systems, high performance compound semiconductor devices should be available at low prices, in high volumes.

(References)

1)W. Abey et al, IEEE MTT-S Digest, pp1315, 1997.

2)T. Hirose et al, to be presented in IEEE MTT-S, 1998.

1988 Topical Workshop on Heterostructure Microelectronics for Information Systems Applications, Kanagawa, Japan, Aug. 30- Sept. 2, 1998

Correlation Between Gate Lag, Power Drift, and Power Slump of Digitally Modulated RF Power PHEMTs for Wireless Communication Applications

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A new degradation mode of PHEMTs under RF overdrive is reported in terms of recoverable drift in the output power. This power drift and the previously reported irreversible power slump appear to be different manifestations of the same charge accumulation phenomena in the silicon-nitride surface passivation layer. In power drift it is manifested as a reduction of transient drain current, whereas in power slump it is manifested as a reduction of steady-state drain current. Thus, power drift can be a precursor for power slump, while the worsening of a PHEMT's gate-lag characteristics can be used as an indicator of its power drift tendency. A pulsed *I-V* gate-lag test is therefore proposed for in-process wafer screening. Ultimately, all these surface-related problems can be minimized by improving the surface passivation and by reducing the channel-to-surface sensitivity.

Power-added efficiency is critical to RF power amplifiers used in battery-operated wireless handset. High efficiency in power amplification is typically achieved by maximizing the drain-source voltage swing under Class AB or B operation. High drain-gate voltages therefore occur when the gate-source voltage is swung below pinch off. This results in large electric fields at the drain edge of the gate which can cause enhanced carrier conduction, hot-carrier injection, and hydrogen dissociation/diffusion in the surface passivation layer of a PHEMT which is typically made of hydrogenated amorphous silicon nitride. These high-field phenomena can occur simultaneously and can all increase the amount of fixed charge in the passivation hence changing the surface potential of the semiconductor. This situation is exasperated in time-division multiple-access (TDMA) systems such as global system for mobile communications (GSM) for which the power amplifier is repeatedly swung between deep pinch off (to prevent RF leakage) and deep compression (to achieve high power-added efficiency). Long talk time and dense spectrum usage therefore come at the price of reduced reliability.

Passivation charge can have a number of effects on device characteristics. In power slump the large amount of charge in the passivation results in a wide depletion region in the semiconductor which increases the drain access resistance and decreases the drain-gate capacitance as well as the maximum drain current. In addition, an increase in the drain-gate breakdown voltage can be found before the decrease in drain current. This is because the passivation charge can relax the electric field near the drain edge of the gate just as the charge occupying the semiconductor/passivation interface states does. However, in the case involving the passivation charge, not only can the electric field be relaxed, but also the occupation of interface states can be affected. The latter may be detrimental for surface-sensitive devices such as PHEMTs.

To illustrate such an effect, pulsed *I-V* stress tests were performed by pulsing a PHEMT gate from on to off repeatedly. The PHEMT was normally kept on by maintaining its gate-source voltage at 0.5 V. Once every second the gate-source voltage was pulsed down to -4 V (well below the threshold voltage of -1 V) for 10 ms. This pulse at -4 V simulates the stress under RF overdrive. The long holding period at 0.5 V allows transient and steady-state drain currents to be continuously monitored during the stress test.

Drain currents measured at 1 μs and steady state after each pulse are shown in Fig. 1, 2 and 3 for different PHEMTs. The difference between the drain currents measured at 1 μs and steady state represents the magnitude of gate lag. For a PHEMT that is known to be stable against power drift, although the 1 μs current is always different from the steady-state current, neither current varies with the

number of pulses (Fig. 1). For a PHEMT that is known to suffer from power drift, the 1 μs current decreases with increasing pulse number while the steady-state current remains the same (Fig. 2). Thus power drift appears to be correlated with the worsening of gate lag but not gate lag per se.

Detailed measurements indicate that, while the amount of gate lag increases with stress, the time constant of gate lag remains the same implying that no new type of interface states are formed. Further, the rate of drift increases with increasing off time and decreasing off voltage, similar to the trends observed in power slump. Fig. 3 shows the case in which the off time is increased significantly from 10 to 500 ms. It can be seen that, while the 1 μs current drifts essentially instantly and even recovers a little eventually, its steady-state current starts to slump slightly. This suggests that power slump may in fact be an advanced stage of power drift.

With other types of measurements such as pulsed RF large-signal waveform, deep-level transient spectroscopy, metal-insulator-metal leakage, light and temperature effects, etc. we have concluded that, power drift, power slump, and the worsening of gate lag (not gate lag per se) are all caused by the reverse gate-drain voltage stress under RF overdrive. The proposed mechanism is that, under a reverse gate-drain voltage stress, negative charge starts to accumulate in the silicon-nitride passivation layer between the gate and drain. This can occur through tunnel injection into the nitride from the drain edge of the gate. The initial impact of the nitride charge is to relax the average electric field, reduce hole generation, and increase breakdown voltage while the PHEMT is off. Reduced hole generation leads to reduced hole capture at the passivation/semiconductor interface. This allows the interface states to be more negatively charged while the PHEMT is off hence more gate lag and power drift when PHEMT is swung back on. With increasing stress, eventually there will be enough nitride charge to directly impact the steady-state drain current therefore power slumps. Finally, the injected charge in the nitride can release the hydrogen that passivates the dangling silicon bonds and, once hydrogen outdiffuses, damage will be irreversible.

ACKNOWLEDGMENT

This work was supported in part by the U.S. Air Force Research Laboratory, Sensors Directorate, Aerospace Components and Subsystems Technology Division, under Contract No. F33615-95-C-1755.

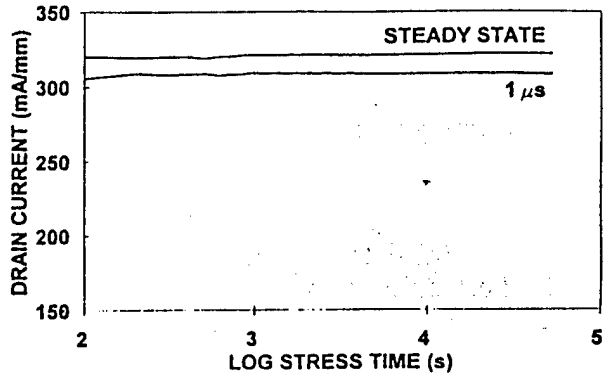

Fig. 1 With a stable PHEMT kept on most of the time but once every second pulsed off for 10 ms, transient drain current was then measured at 1 μs and 64 ms (steady state) after pulsed on. Notice that although the 1 μs current is always different from the steady-state current, neither current varies with the number of pulses. *Vgs(on)* = 0.5 V. *Vgs(off)* = -4 V. *Vdd* = 5 V. *Zl* = 15 Ω mm.

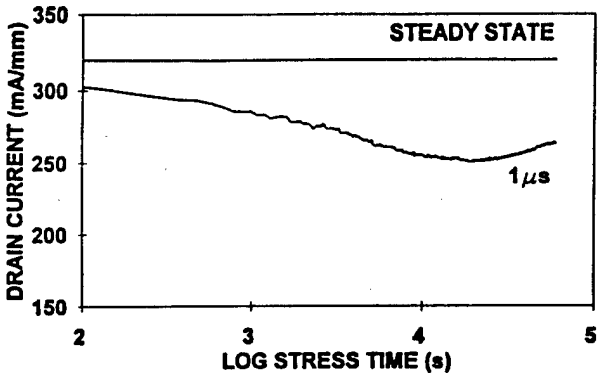

Fig. 2 Same as Fig. 1 except that a PHEMT that is known to suffer from power drift is tested. Notice that the 1 μs current decreases with increasing pulse number while the steady-state current remains the same, suggesting that power drift is correlated with the worsening of gate lag but not gate lag per se.

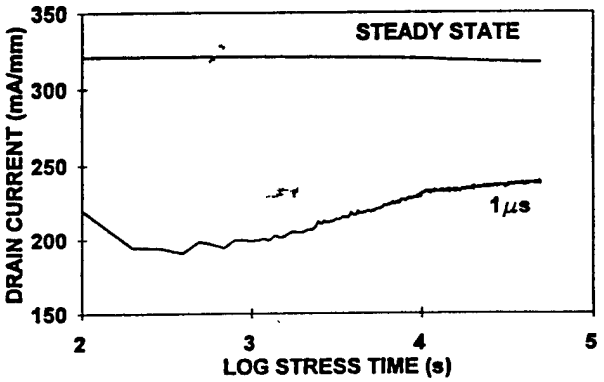

Fig. 3 Same as Fig. 2 except the off time is increased from 10 to 500 ms. In this case, the 1 μs current drifts essentially instantly and even recovers a little eventually, but the steady-state current starts to slump slightly. This suggests that power slump may in fact be an advanced stage of power drift.

Novel HEMT Processing Technologies and Their Circuit Applications

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InP-based high electron mobility transistors (HEMTs) have demonstrated the highest unity current-gain cutoff frequency (f_t) [1] the highest maximum frequency of oscillation (f_{max}) [2], and the lowest minimum noise figure (F_{min}) [3] of any transistor to date. Additionally, a D-band MMIC low noise amplifier (LNA) exhibiting 12 dB of gain at an operating frequency of 155 GHz has been fabricated [4], which is the highest operating amplifier ever demonstrated. With the increasing size and complexity of circuits, however, power consumption also becomes a concern to the circuit designer. In order to achieve both low power and high speed circuit operation, a viable process for the monolithic integration of enhancement- and depletion-mode high-electron mobility transistors (E- and D-HEMTs) in the lattice-matched InP material system must be developed. With both types of devices available, a Direct-Coupled FET Logic (DCFL) technology can be employed for circuit design yielding circuits which dissipate substantially less power than those using only D-HEMTs. Recently, we have developed and validated a process for the monolithic integration of E- and D-HEMTs on lattice-matched InP [5,6]. Using this process, a 23-stage ring oscillator employing a DCFL technology was fabricated using a gate length of 0.5 μm for both driver and load devices. The ring oscillator exhibited room temperature operation for supply voltages as low as 0.24 V and propagation delay times of about 20 ps/stage. A room temperature power-delay-product (PDP) of 0.322 fJ/stage was also measured which, to the best of the authors' knowledge, is the lowest in the InP material system. Also, for the first time in the InP material system, a DCFL divide-by-four prescaler was fabricated and demonstrated functionality up to 6 GHz, with a power dissipation of only 5.37 mW/stage. We will compare our realization of prescalers in the DCFL and the Source-Coupled FET Logic (SCFL) technologies. Additionally, a review of various E-HEMT fabrication techniques will be presented.

[1] L. Nguyen et al., "50-nm Self-aligned-gate pseudomorphic AlInAs/GaInAs high electron mobility transistors," *IEEE Trans. Electron Devices*, 1992, **39**, pp. 2007-2014.

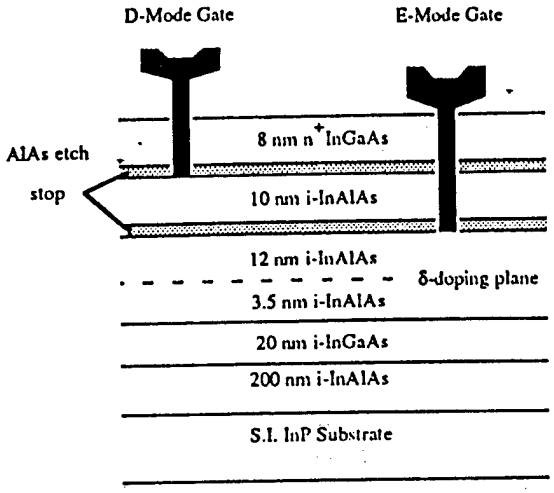
[2] P. Smith et al., "W-Band high efficiency InP-based power HEMT with 600 GHz f_{max}," *IEEE Microwave and Guided Lett.*, 1995, **5**, pp. 230-232.

[3] P. Smith, et al., "Microwave InAlAs/InGaAs/InP HEMTs: status and applications," in *Proc. 2nd Int. Conf. InP and Related Materials*, 1990, pp. 39-43.

[4] R. Lai et al, "D-Band MMIC LNAs with 12 dB gain at 155 GHz fabricated on a high yield InP HEMT MMIC production process," in *Proc. 9th Int. Conf. InP and Related Materials*, 1997, pp. 241-244.

[5] A. Mahajan et al., "Monolithic integration of InAlAs/InGaAs/InP Enhancement- and depletion-mode high electron mobility transistors," in *IEDM '96 Proceedings*, 1996, pp. 51-53.

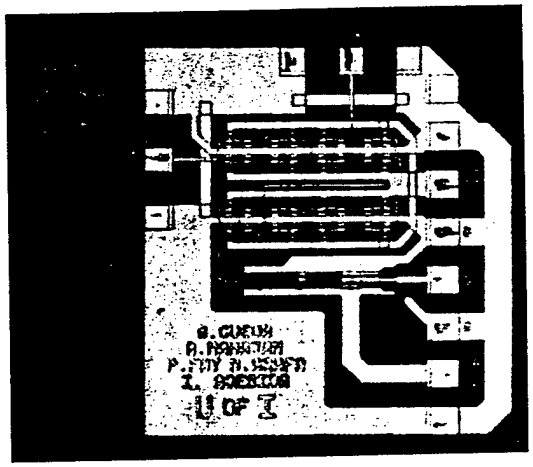
[6] A. Mahajan et al., "Fabrication and characterization of ring oscillator using integrated enhancement- and depletion-mode high electron mobility transistors," *IEEE Electron Device Lett.*, **18**, 1997, pp. 391-393.



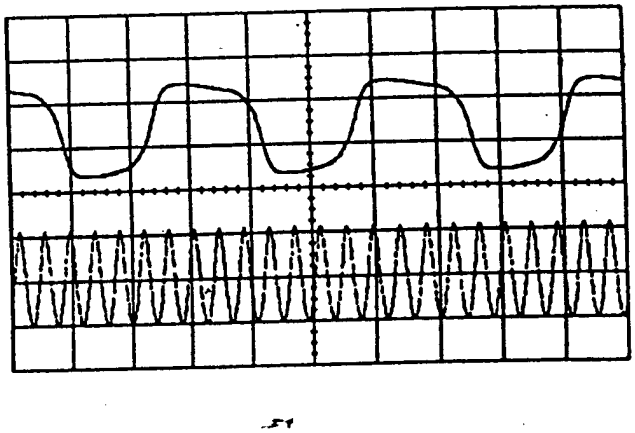
E/D layer structure. The D-mode gate metalization is Ti/Au while the E-mode gate metalization is Pt/Ti/Pt/Au.

	E-HEMT	D-HEMT
# measured devices	80	80
V_T (mV)	187	-443
σV_T (mV)	7	12
g_{mext} (mS/mm)	625	462
I_D (mA/mm)	149	159
g_o (mS/mm)	18	25
g_{mext}/g_o	35	18
f_T (GHz)	95	102

Summary of device results for 0.3 μm HEMTs.



SEM micrograph of DCFL divide-by-four prescaler.



Input (bottom trace, frequency-doubled due to instrument limitations) and output (top trace) for divide-by-four prescaler operating at 6 GHz.

Suppression of G_{DS} Frequency Dispersions in Heterojunction FETs with a Partially Depleted p-Type Buffer Layer

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INTRODUCTION

Heterojunction FETs have excellent high-speed performance, but frequency dispersion or drain-lag have been serious problems for their digital circuit applications. They cause so-called "mark-ratio effect," which degrades the phase margins at high bit-rate operations. Since, unlike power FETs, source and drain n^+-regions are placed as close as possible to gate electrode, the main origin of the frequency dispersion can be attributed to the deep traps at substrate/epitaxial layer interface or in the substrate [1]. The purpose of this work is to find a heterojunction FET structure that can suppress the substrate trap effects.

Frequency dispersion occurs due to the delayed responses of the traps to the drain voltage. In ion-implanted MESFETs, buried p-region is introduced to suppress short-channel effects, but it also suppresses the frequency dispersion [2]. A possible explanation for this effect is that a conductive p-region shields the trap effects. In this case, however, the electric potential of the p-region should be fixed, otherwise a large dispersion will appear due to the fluctuation of the p-layer potential [3]. So the problem is how to stabilize the electric potential of the p-layer which is electrically floating in conventional heterojunction FETs.

THEORY

The electric potential of the p-region at low frequencies is determined by the resistances of the two pn-junctions at the source and drain. The potential will be settled at the source voltage due to the lower resistance of the forward biased pn-junction at the source. At high frequencies, however, the potential will be fluctuated with drain voltage by capacitive coupling. The potential fluctuation δV_P for the p-region by drain voltage will be written as,

$$\delta V_P = \frac{C_{DP}}{C_{SP}+C_{DP}} \delta V_D \qquad (1)$$

where, C_{SP} and C_{DP} are the p-region capacitance to the source and drain electrodes, respectively (Fig.1). Due to the symmetrical structure of the FET, they are nearly the same when the p-region is not depleted. However, if the holes in the p-region deplete by the drain bias, C_{DP} drastically decreases while C_{SP} remains the same. Then, δV_P becomes nearly zero resulting in no fluctuation of the p-region voltage. Thus, the p-region voltage is stabilized from DC to high frequencies at the value of source voltage when the p-region under the drain is depleted.

EXPERIMENTS

MBE epitaxial wafers are prepared; one with conventional non-doped(i-type) buffer layer and the other with a newly designed p-type buffer layer(Fig.1). The FET fabrication process includes selective wet etching, lift-off metalizations and boron implantation for isolation. The gate length and width are 0.7 μm and 2x50 μm, respectively. DC characteristics show a better saturation characteristics for the FET with p-buffer, but also show severe kink effect at high drain bias (Fig.2). Both effects may be caused by the shallow p-layer. G_m was about 350mS/mm, f_T and f_{max} were 17.2GHz and 39GHz for FET with i-buffer, respectively, and 15.8GHz and 36GHz for FET with p-buffer, respectively, both at V_g=0V and V_d=1.5V.

Frequency dispersions normally appear at around 1KHz for FET on MBE epi-wafers due to the oxygen contamination at the growth interface. So, we compared 1Hz G_{DS} and 100KHz G_{DS}, varying

V_D. As shown in Fig.3, the difference between the two G_{DS}'s is large up to 0.9V, but then dramatically decreases. This voltage is close to the designed voltage at which holes under the drain will deplete. Above 2V, 1Hz G_{DS}increases. This is due to kink effect, in which generated holes elevate the p-region voltage. The FET with i-buffer shows large and constant dispersions for entire drain voltages. The drain voltage range of no dispersion for the present device is limited, but it can be extended by proper designing of the p-region and precise controlling of epitaxial layers.

CONCLUSION

Drain conductance frequency dispersion in heterojunction FET is suppressed by a partially depleted p-layer. This structure requires only new epitaxial layer configuration. No process step and mask pattern modification are needed. This structure basically does not degrade high-frequency performance due to low drain capacitance. The partially depleted buried p-layer will enable for heterojunction FETs to be used in digital and wide-band applications.

REFERENCES

[1] K. Kasahara, et.al., Solid-State Electronics vol.38, p.1221(1995)
[2] P. Canfield and D. Allstot, IEEE J. Solid-State Circuit, vol.25, p.1544(1990)
[3] K. Kunihiro, M. Nogome and Y. Ohno, Proc. 1996 IEEE GaAs IC Symposium, p.179(1996)

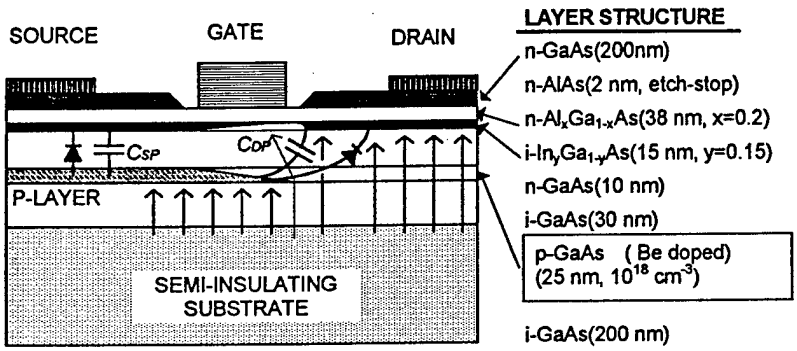

Fig.1 Schematic explanation of the p-layer voltage fluctuation mechanism. Epitaxial layers structure used in the experiment is also shown.

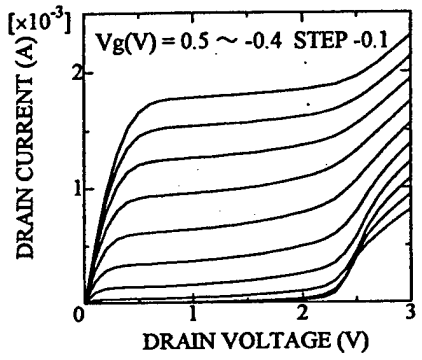

Fig. 2 I_D-V_D characteristics of the FET with p-buffer.

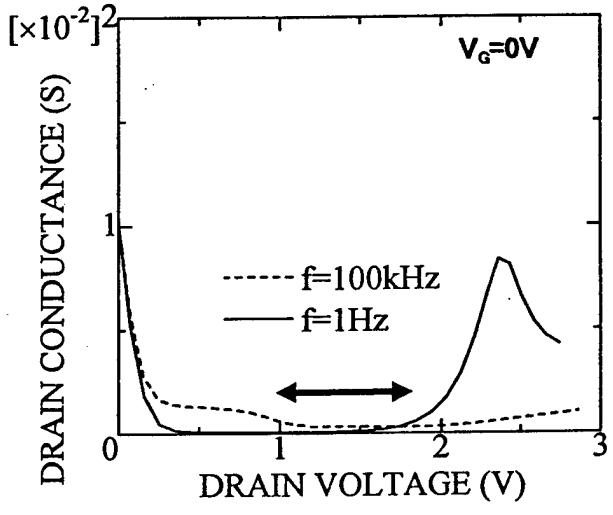

Fig. 3 Comparison of G_{DS}'s at 1Hz and 100KHz for the FET with p-buffer. The arrow indicates the dispersion suppressed region.

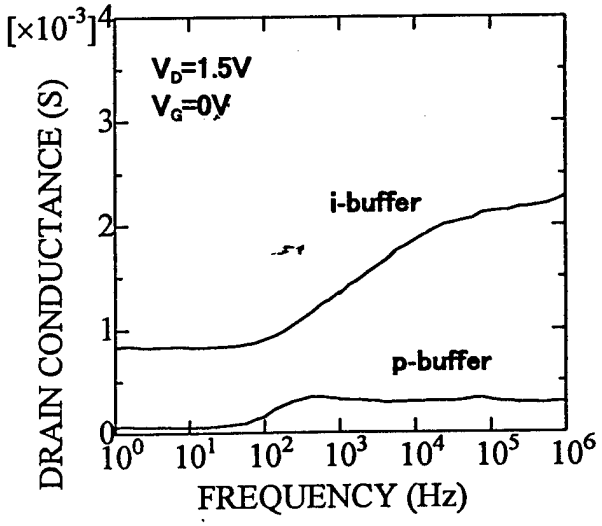

Fig. 4 Comparison of G_{DS}'s for FETs with and without p-buffer. V_G=0V and V_D=1.5V.

A New Method for Evaluation of Surface Recombination in Heterojunction Bipolar Transistors by Magnetotransport

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We present a novel method for evaluating the surface recombination in the base of heterojunction bipolar transistors (HBTs) employing magnetotransport of electrons. Magnetic field vertical to the base / emitter junction was found to suppress the lateral diffusion of electrons toward the base electrodes in the extrinsic base region, which in turn decreased the surface recombination. The surface recombination velocity was obtained by measuring the current gain in the magnetic field with the aid of 2-dimensional simulation. We estimated the surface recombination velocity as 7×10^6 cm/s for AlGaAs / GaAs HBT with an emitter area of $3\times3\mu m^2$ which was in good agreement with reported data.[1] This is the first report that the surface recombination velocity was obtained experimentally for a small HBT without any reference samples.

The behavior of electrons in the base region in a magnetic field was studied theoretically and was described in the 2-dimentional diffusion equation as;

$$\frac{\partial^2 n}{\partial \tilde{x}^2}+\frac{\partial^2 n}{\partial z^2}-\frac{n}{D\tau}=0 \text{ , where } \tilde{x}=\sqrt{1+(\mu B)^2}\,x \text{ .} \qquad (1)$$

Here B is magnetic field and D, τ, n, and μ are diffusion constant(at $B=0$), relaxation time, density, and mobility of electron, respectively. The emitter / base junction is in the xy plane and B is along the z direction (Fig. 1). The equation (1) was treated in the same manner as $B=0$ with reduced scaling toward the x direction. The surface recombination velocity *sa* was taken in the calculation through boundary conditions.[2] Figure 2 shows calculated current gain *hfe*, surface recombination current *Isa*, and bulk recombination current *Ibulk* as a function of μB. The current gain increased as μB increased due to the decrease of surface recombination current. On the contrary, bulk recombination current was not affected by μB. These results were explained by the modification of the electron path which was vertical to the magnetic field. The present method was applied to an HBT with an emitter area of $3\times3\mu m^2$. The schematic cross section is shown in fig. 1. The base layer was GaAs doped with carbon (5×10^{19} cm^{-3}) and 50 nm in thickness. The extrinsic base surface was covered with polyimide. Figure 3 shows calculated and measured magnetic field dependence of *hfe*. Using the parameters *sa* = 7×10^6 cm/s, $D=65$ cm^2/s, and $\tau=40$ ps, the calculation was in good agreement with measured data. These results were also in good agreement with recent data.[3]

Notice that GaAs based HBTs have attracted considerable attention for high speed devices, however they have been suffered from high surface recombination velocity in the base. The degradation of current gain is apparent for HBTs with a small emitter area. The evaluation of the surface recombination has been carried out only with reference samples or specially designated structures which were deferent from the HBT structure for IC applications, so far. Furthermore, the surface recombination is thought to play an important role in the degradation of HBTs after a bias stress test where the same degree of degradation for individual samples is not expected. Therefore, the present method is not only useful for study in the transport of the minority carrier but will be a powerful tool for developing the HBTs with higher performance and reliability for information systems applications.

1) H. Ito and T. Ishibashi, Jpn. J. of Appl. Phys. 33, 88 (1994)
2) W. U. Liu et al., Solid States Electronics 34, 1119 (1991)
3) C. M. Colomb et al., J of Appl. Phys. 73, 7471 (1993)

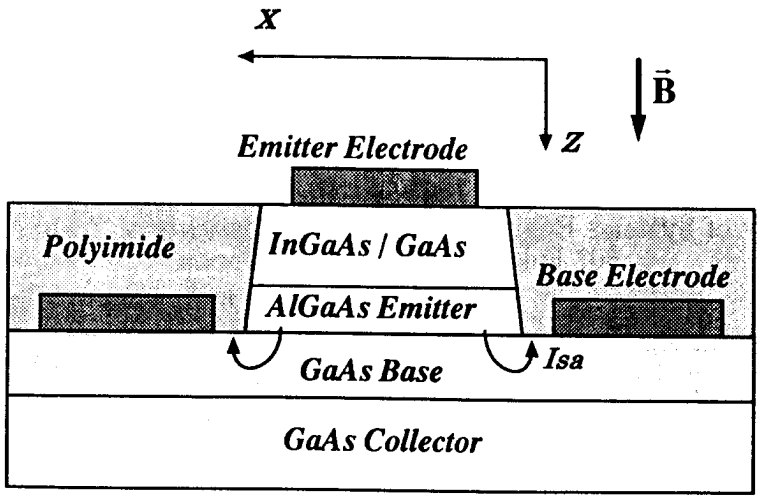

Fig.1 Schematic cross section of HBT

The magnetic field is parallel to the z axis. The surface recombination current flows from the intrinsic base region (under the emitter region) to the extrinsic base surfaces. The magnetic field suppresses the diffusion of electrons to the extrinsic base region.

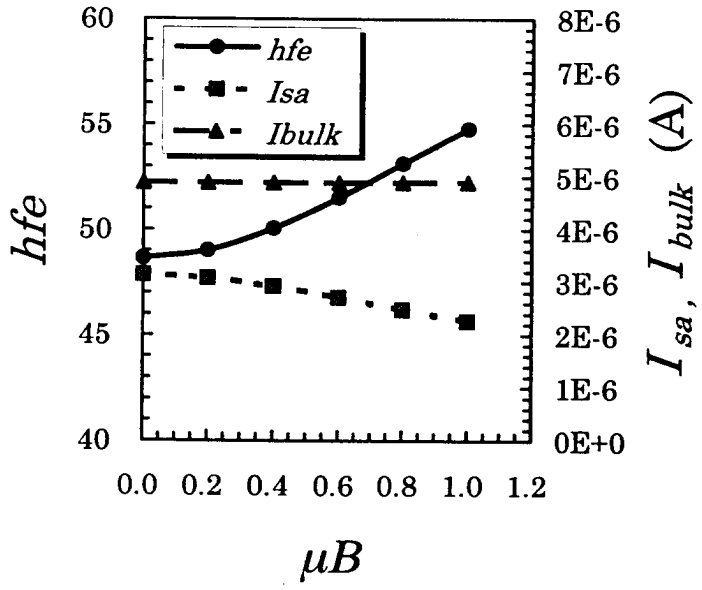

Figure 2 Current gain and recombination currents vs. magnetic field.

Notations hfe, Isa and Ibulk represent current gain, surface recombination current and bulk recombination current, respectively. The surface recombination was decreased by the magnetic field, however, the bulk recombination was not affected.

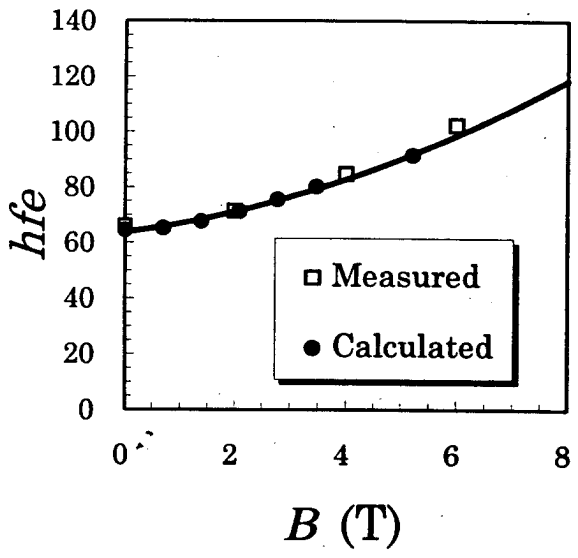

Figure 3 Current gain vs. magnetic field.

Open square and solid line with closed circle represent measured data and calculation, respectively. The measured data were obtained with Ic = 1mA and Vce = 2 V at 262K. The surface recombination velocity, diffusion constant, relaxation time were estimated as $7x10^6$ cm/s, $65cm^2/s$, and 40ps, respectively.

Effects of Surface States on Cutoff Frequency Characteristics of AlGaAs/GaAs HBTs

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AlGaAs/GaAs heterojunction bipolar transistors (HBTs) have received great interest for application to high-speed and high-frequency devices. It is recognized that in GaAs-based devices such as GaAs MESFETs, existance of surface states strongly affects the device characteristics. It is also well known that in the AlGaAs/GaAs HBTs, the surface states act as recombinatin centers and hence the base current increases, resulting in the degradation of current gain [1],[2]. However, there is no work reported on how the surface states affect the high-frequency performance of the HBTs. So, in this work, we have simulated the cutoff frequency (f_T) characteristics of AlGaAs/GaAs HBTs considering surface-state effects, and found that the heavy degradation of f_T could occur due to surface states in the external base region.

Fig.1 shows device structures simulated here. (a) is a normal emitter-up HBT, and (b) is an ideal collector-up HBT where the external emitter is assumed perfectly insulating. In the emitter-up and collector-up HBTs, the surface states are considered on the emitter and base surfaces, and on the base and collector surfaces, respectively, as shown in the figure. As for the surface-state model, we adopt the Spicer's unified defect model [3]. We assume that the surface states consist of a pair of deep donor and deep acceptor, and the following case based on experiments is considered: $E_{SD} = 0.925$ eV and $E_{SA} = 0.8$ eV [3], where E_{SD} is energy difference between the bottom of conduction band and the deep donor's energy level, and E_{SA} is energy difference between the deep acceptor's energy level and the top of valence band. The surface states are assumed to distribute uniformly within 5 Å from the surface and their density N_S is typically set to 10^{13} cm^{-2}. Basic equations are Poisson's equation including ionized deep-level terms, continuity equations for electrons and holes, and current equations for electrons and holes. We have calculated the cutoff frequency f_T and the delay times (τ_E, τ_B, τ_C) in the respective regions. f_T and the base delay time τ_B are given by $f_T = (1/2\pi) \cdot (\partial I_C/\partial Q_n)_{V_{CE}}$ and $\tau_B = (\partial Q_{nB}/\partial I_C)_{V_{CE}}$, where Q_n and Q_{nB} are electron charges in the whole device and in the base layer, respectively. The ionized deep-level densities are held fixed during the small-signal swing to obtain the high-frequency performance.

Fig.2 shows calculated f_T - I_C characteristics of the emitter-up HBT as a parameter of the surface-state density N_S. It is seen that when N_S is higher, f_T becomes lower. This is because, as shown in Fig.3, the base delay time τ_B becomes longer (, although τ_E and τ_C are almost unchanged). Fig.4 shows comparison of conduction-band energy diagrams with and without surface states. With surface states, the energy at the base surface is lowered because the Fermi level is pinned around the midgap. So, electrons tend to fall into this surface-state region, and accumulate there (as shown in Fig.5) when the deep levels do not respond to the voltage swing. Therefore, τ_B given by $(\partial Q_{nB}/\partial I_C)_{V_{CE}}$ becomes very long, and hence f_T degrades much in this case.

Next, we discuss the collector-up HBT. Fig.6 shows maximum value of cutoff frequency f_{Tmax} (in the f_T - I_C characteristics) as a parameter of the difference x between emitter width and collector width (cf. Fig.1(b)). When x is positive, that is, the collector width is narrower than the emitter width, f_T degrades much even without surface states because of the carrier-blocking effect [4]. With surface states, f_T takes a rather low value even if x becomes slightly negative. This is because with surface states, as shown in Fig.7, the energy at the base surface is lowered, and hence electrons spreading toward the external base accumulate in this region (Fig.8), as in the case of emitter-up HBT. Therefore, τ_B given by $(\partial Q_{nB}/\partial I_C)_{V_{CE}}$ becomes long as shown in Fig.9, and hence f_T degrades. This degradation can be improved by setting x more negative, that is, by making the collector width much wider than the emitter width.

In conclusion, we have shown theoretically that the existance of surface states on the external base region in AlGaAs/GaAs HBTs should lead to the degradation of f_T, because electrons tend to fall into this region and hence the effective base delay time becomes very long.

[1] Y. S. Hiraoka and J. Yoshida, *IEEE Trans. Electron Devices*, vol.35, pp.857-862, 1988.
[2] P. M. Asbeck *et al.*, *Proc. IEEE*, vol.81, pp.1709-1726, 1993.
[3] W. E. Spicer *et al.*, *J. Vac. Sci. Technol.*, vol.16, pp.1422-1433, 1979.
[4] K. Horio and A. Nakatani, *IEEE Trans. Electron Devices*, vol.42, pp.1897-1902, 1995.

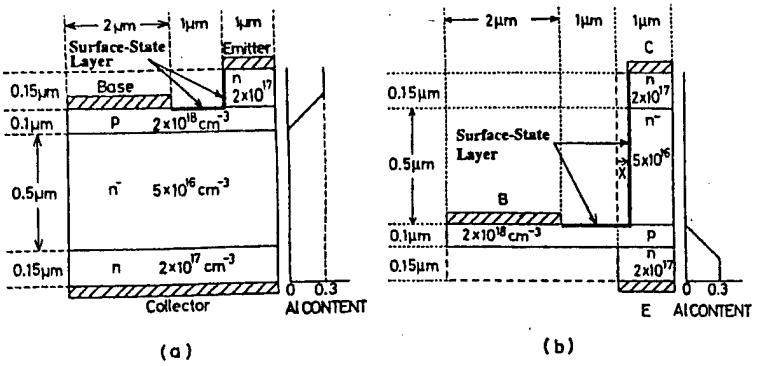

Fig.1 AlGaAs/GaAs HBT structures analyzed in this study. (a) normal emitter-up HBT, (b) collector-up HBT.

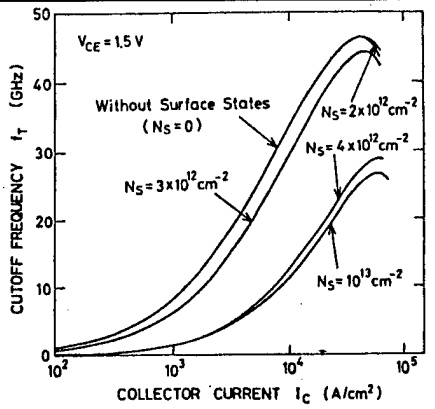

Fig.2 Calculated f_T - I_C characteristics of AlGaAs/GaAs emitter-up HBT as a parameter of surface-state density N_S. $V_{CE} = 1.5$ V.

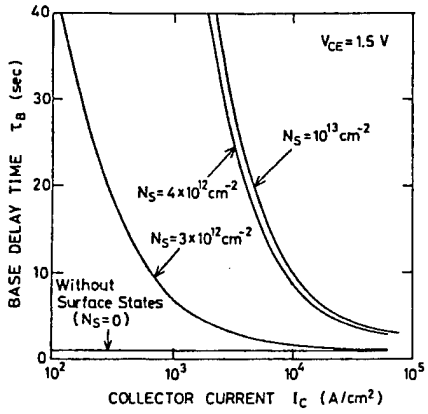

Fig.3 Calculated base delay time τ_B versus I_C curves, corresponding to Fig.2.

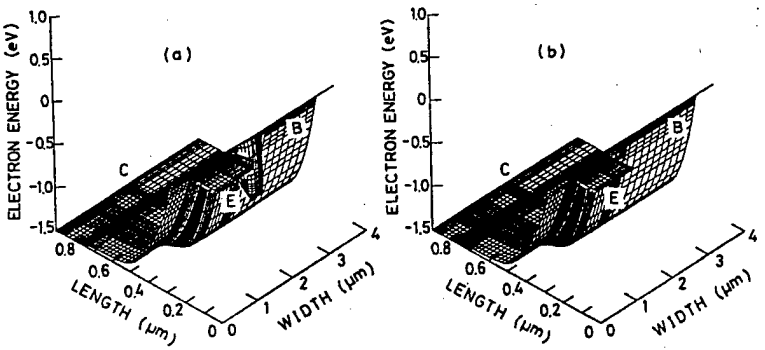

Fig.4 Comparison of conduction-band energy diagrams with and without surface states. $I_C = 5 \times 10^4$ A/cm^2. (a) with surface states ($N_S = 10^{13}$ cm^{-2}), (b) without surface states.

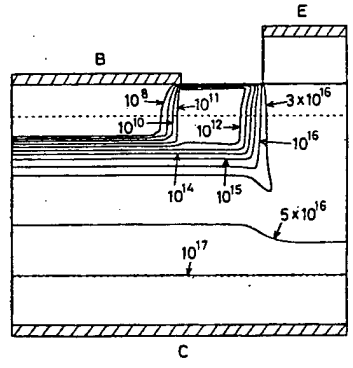

Fig.5 Electron density profiles for the case with surface states ($N_S = 10^{13}$ cm^{-2}) when the deep levels do not respond to voltage swing. $I_C = 5 \times 10^4$ A/cm^2.

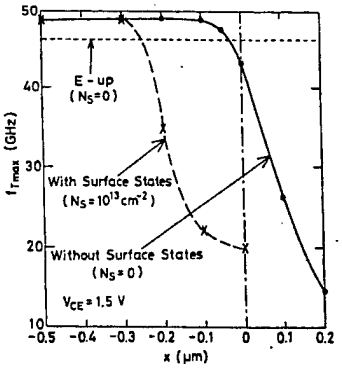

Fig.6 Maximum value of cutoff frequency f_{Tmax} (in f_T - I_C curves) versus emitter-collector width difference x for collector-up AlGaAs/GaAs HBT.

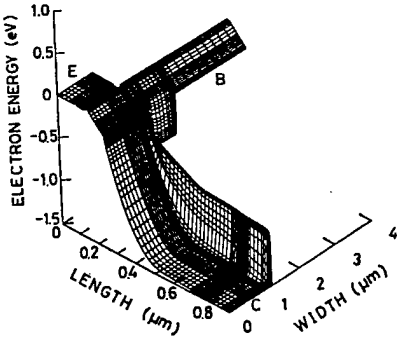

Fig.7 Conduction-band energy diagram for the case with surface states ($N_S = 10^{13}$ cm^{-2}). $x = -0.2$ μm. $I_C = 5 \times 10^4$ A/cm^2.

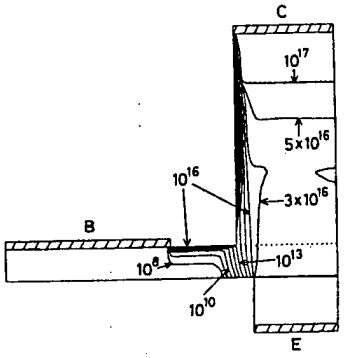

Fig.8 Electron density profiles for the case with surface states ($N_S = 10^{13}$ cm^{-2}) when the deep levels do not respond to voltage swing. $x = -0.2$ μm. $I_C = 5 \times 10^4$ A/cm^2.

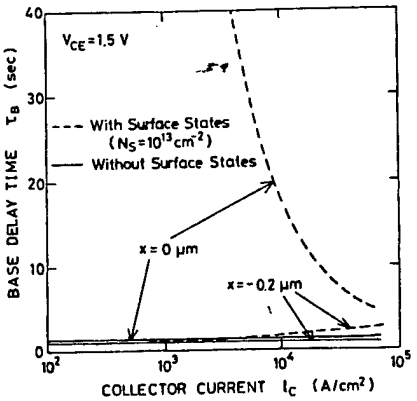

Fig.9 Comparison of τ_B - I_C curves of collector-up HBTs with and without surface states.

Resonant-Tunneling Analog/Mixed-Signal Circuit Technology

(Invited)

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The performance of present generation high-speed integrated circuits (ICs) is limited by the finite gain-bandwidth product of the transistor technology. The world's highest speed transistors are based on InP substrates with a cut-off frequency of 340 GHz. The highest speed semiconductor switching device is the resonant tunneling diode (RTD) and it's best performance is also achieved on InP. A large scale integration (LSI) technology has now been demonstrated that combines these record-high-speed devices in a monolithic IC format for ultrahigh speed analog/mixed signal circuits. World's first demonstrations of this technology include: 4-bit, 3 GHz analog-to-digital converter, 3 GHz (50 dB spur free dynamic range) clocked quantizer, 3 GHz sample & hold (55 dB linearity), clock circuits, shift registers, and ultralow power SRAM (50 nW/bit). This technology should be capable of producing analog-to-digital converters with resolutions of 8-bits at 10 GSps, 6-bits at 25 GSps, and even 4-bits at 100 GHz. Other circuits of interest include mux/demux, true time delay, direct digital synthesizers, and fiber receiver functions with 10-100 GHz data rates.

Indium phosphide substrates are not the only substrates of interest for RTDs. Resonant tunneling diode circuits in combination with CMOS transistors are also being developed. Such a technology offers 23x lower power for Si embedded-DRAM, as well as gigahertz shift registers and clocks. Progress in silicon heterostructures toward realization of an IC-compatible silicon RTD will be discussed.

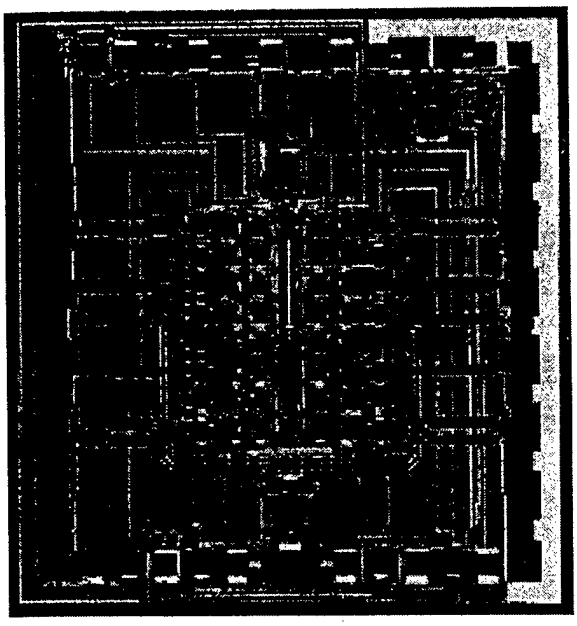

Figure 1. Photomicrograph of the resonant tunneling diode/ heterojunction field effect transistor analog-to-digital converter, measuring 1.9x2.1 mm^2. The ADC die has 450 components, including 64 RTDs, 225 HFETs, Schottky diodes, resistors, and capacitors.

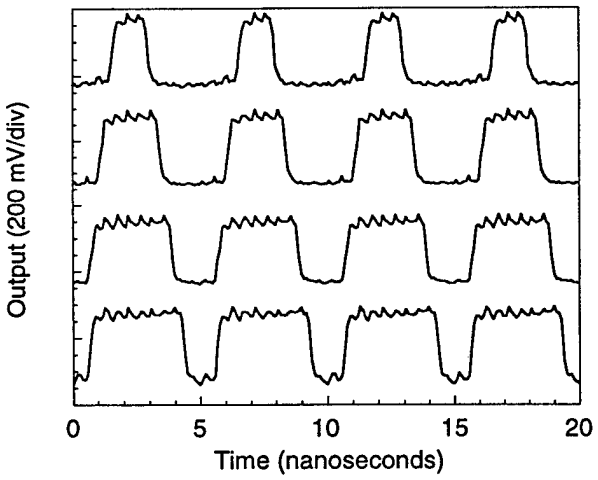

Figure 2. Beat frequency test for 4 outputs of the ADC showing clean operation for input signals above Nyquist. The clock frequency is 2.2 GSps and the input frequency is 2 GHz. The output is at the beat frequency of 200 MHz.

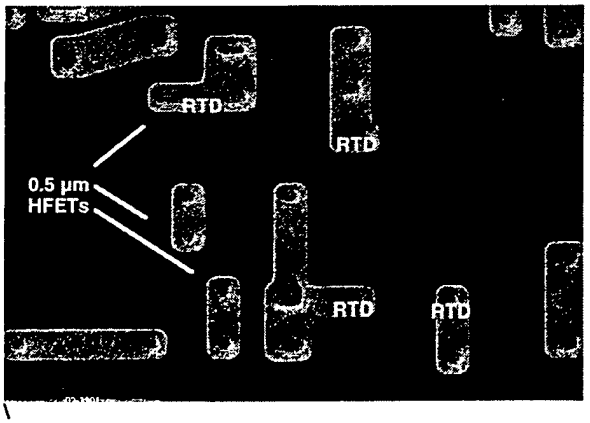

Figure 3. Scanning electron micrograph of a completed resonant tunneling quantizer showing the co-location of RTDs on HFET source and drain contact regions.

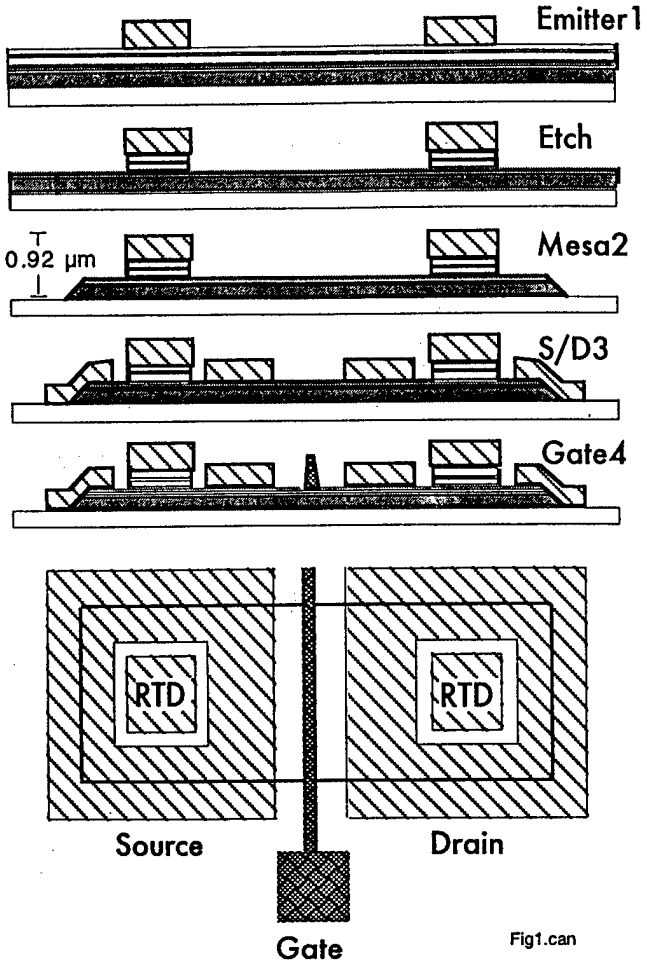

Figure 4. Schematic diagram of the first four mask levels (labeled 1 to 4) of the IC process. The vertical dimension is drawn to scale. In the lower drawing is shown a top view of the transistor with a resonant tunneling diode (RTD) on both the source and the drain; this is an option in the layout.

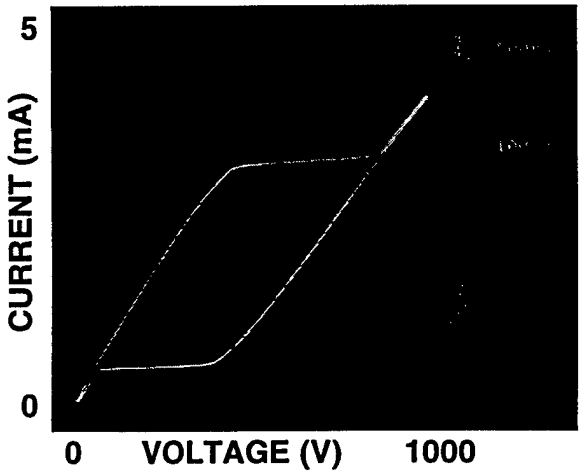

Figure 5. Five hundred resonant tunneling diodes in series showing only a few percent variation of peak and valley currents over the entire device array.

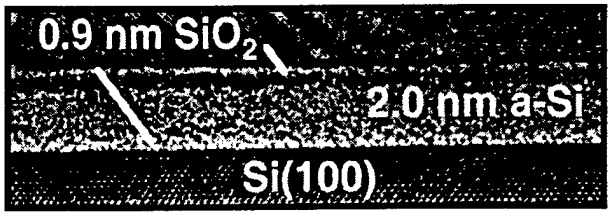

Figure 6. $SiO_2/Si/SiO_2$ resonant tunneling diode.

Influence of RTD Device Physics on Circuit Performance

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Resonant tunneling diodes (RTDs) have achieved a level of maturity such that prototype integrated circuits at tens of gigahertz frequencies have been demonstrated. Detailed computer intensive quantum tunneling calculations have been useful for understanding the basic mechanisms involved in determining the device behavior. However, we have found that a semi-empirical approach is also quite useful in understanding the variation of current versus voltage, *I(V)*, behavior, and also provides a link to computer aided design circuit simulation tools such as SPICE.[1] An important application of this approach is to tailor the RTD *I(V)* curve for the particular use made of it within a given circuit. Different circuits require that different aspects of the RTD *I(V)* curve be optimized. These aspects usually include the current and voltages of the RTD peak and valley, as well as the form of the curve beyond the valley. However, an example will be given where the relative slope ratio on either side of the peak may also be critical.

We have used our semi-empirical framework to design RTD structures to optimize the *I(V)* and also to evaluate the relative advantages of different heterostructure material systems. The two most important systems are the InGaAs/InAlAs pair lattice matched to InP, possibly including an additional pure InAs central layer, and the InAs/AlSb/GaSb Type II resonant interband tunnel diode (RITD). The advantage of the latter system is significantly lower peak voltages, while maintaining high current densities.

To analyze and compare these two material systems in detail we have extended the simplest, and original, RTD model, the Tsu-Esaki model. The main goal was to include the effects of differing effective masses in the emitter and well.[2] This is essential for two reasons. First, the Tsu-Esaki model as is produces an unrealistically abrupt negative resistance. We show that the differing masses provide the simplest broadening mechanism contributing to the magnitude of the negative resistance and can also demonstrate the combined effects of varying the masses, temperature, Fermi level, and resonance energy. Second, RITDs have masses which differ in sign in the emitter and well, and the existing Tsu-Esaki model cannot be applied at all to this important case. The resulting formula for the current density for the case when the emitter mass is less than the well mass is

$$J = \frac{em_W kT}{2\pi^2 \hbar^3} \int_0^\infty dU t(U) \ln\left[\frac{1+e^{(E_F-U)/kT}}{1+e^{(E_F-U-eV)/kT}} \frac{1+e^{(E_F-\alpha U-eV)/kT}}{1+e^{(E_F-\alpha U)/kT}}\right]$$

where $\alpha = m_W/(m_W - m_E)$. The modifications are the replacement of the emitter mass, m_E, by the quantum well mass, m_W, and the additional factor in the logarithm, which comes from new limits on the range of the in-plane momentum. We also use a simple $k \cdot p$ model to demonstrate that having masses that differ is the usual case, even when the same semiconductor is chosen for the emitter and well. This also extends the previously derived analytical SPICE-compatible *I(V)* formula.

We use this formalism to evaluate the variation of current peak magnitude and voltage versus structural parameters. For example, Fig. 1 compares the peak region of the *I(V)* curves for several values of the quantum well effective mass (in units of the free electron mass, m_e). The negative resistance region is most abrupt when the emitter mass is the same as the quantum well

mass. Larger quantum well masses decrease the peak voltage while smaller masses maintain the peak voltage but spread out the negative resistance region. The negative, -0.04, mass is relevant to the RITD case, in which the tunneling is through quantum well hole states. The peak voltage is reduced significantly, demonstrating its superiority for low voltage applications.

We also show that care must be taken in comparing measured *I(V)* data to theoretical predictions. We demonstrate that the well known negative resistance circuit oscillations can distort the *I(V)* even beyond the negative resistance region in two ways. First, depending on the parasitic impedances, the measured *I(V)* can become quite sharp at the *I(V)* peak, even if the intrinsic *I(V)* is rounded. Second, the well known circuit oscillations within the negative resistance region are shown to depend on circuit transients as well as the measurement circuit. Figure 2 shows an example of the calculated *I(V)* curves where the measured result depends on the circuit history.

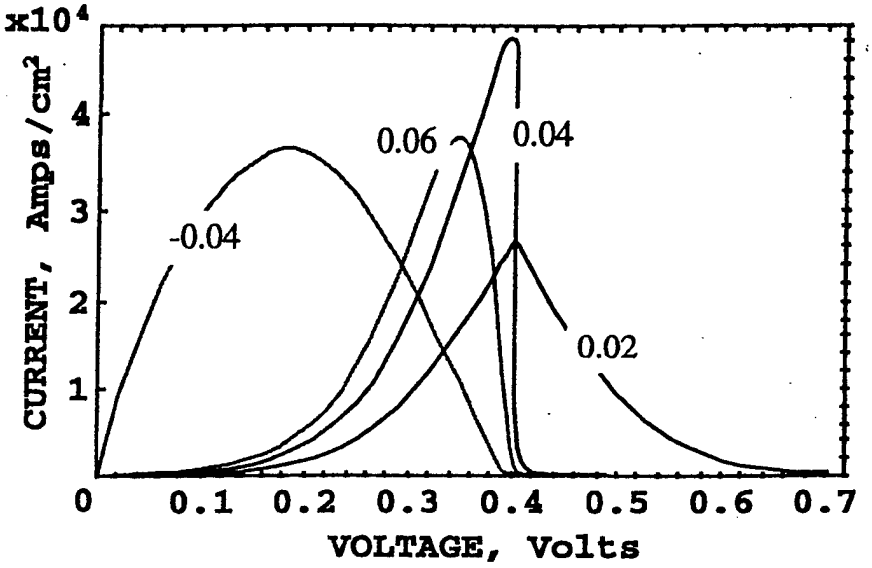

Figure 1. Calculated RTD *I(V)* characteristics in the peak current region for RTDs with emitter effective mass of 0.04 m_e and quantum well effective masses as labelled.

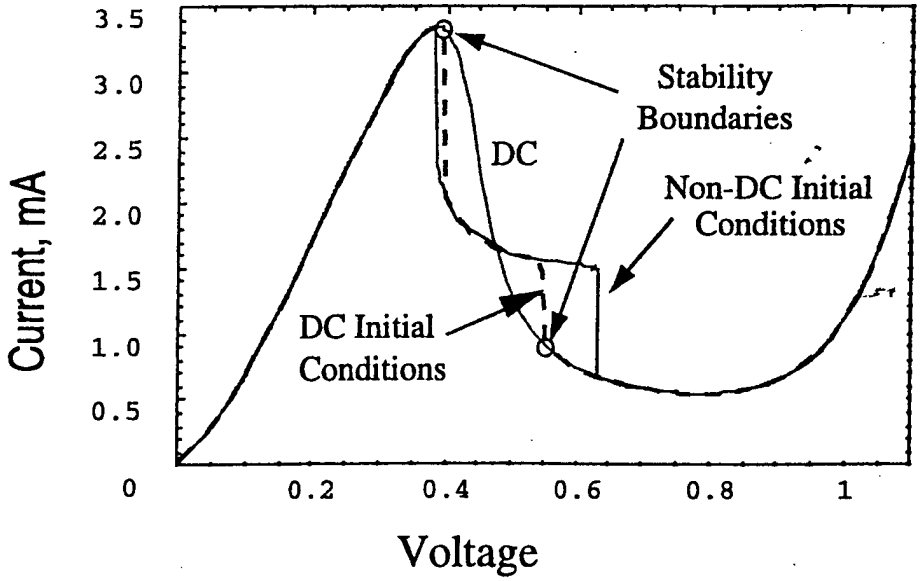

Figure 2. Calculated RTD *I(V)* characteristics showing the intrinsic (DC) characteristic, and two time averaged results depending on two different initial conditions.

[1] J. N. Schulman, H. J. De Los Santos, and D. H. Chow, Elect. Dev. Lett. 17, 220 (1996).
[2] J. N. Schulman, Appl. Phys. Lett. 72, #22, June 1, 1998.

SiGe HBTs for Mobile Communication

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Introduction

Silicon Germanium heterobipolar transistors (SiGe HBTs) offers the opportunity to fabricate high performance ICs for mobile communcation systems in the 0.9 - 5.8 GHz range. The greatest benefit of SiGe one can earn in analoge and mixed signal circuits as e.g. low noise amplifiers (LNAs), power amplifiers (PA), mixers, voltage controlled oscillators (VCOs) and phased locked loops (PLLs).
The advantages of SiGe over pure silicon for these applications are mainly the extremely high cutoff frequencies with record values from research HBTs of f_T = 130 GHz [1] and f_{max} = 160 GHz [2], and a ECL gate delay down to 9.3ps [3]. The good high frequency noise performance with rf noise figures of 0.9dB at 10GHz [4] emphasizes the potential of SiGe-HBTs in mobile communication systems. However, an important argument for using HBTs for wireless applications is the high power added efficiencies at low DC- voltages. This is an advantage not only over silicon but also over GaAs-MESFETs, due to the higher linearity and gain for operation voltages below 3.6V.

Technology

TEMIC offers a production technology, called SiGe1, including npn HBTs with and without selectively implanted collector on the same wafer [5]. The SiGe HBTs reveal transit frequencies of 30 GHz with BV_{CEO}=6V and 50GHz with BV_{CEO}=3V, respectively. In addition, spiral inductors, nitride capacitors, three types of poly resistors, a LPNP, rf- and dc-ESD protection and varactor diodes are incorporated in the present technology.
In contrast to other companies, as e.g. IBM, Siemens or Philips, which prefer a triangular Ge profile with only up to 15% Ge in the medium doped base, TEMIC´s SiGe1 technology has a nearly box shaped Ge profile with above 20% Ge in the base. The highly Boron doped SiGe base, $4x10^{19}$ cm^{-3}, grown by a single wafer CVD machine, has a real advantage over the drift HBTs due to the approximately 10 times smaller base sheet resistance, revealing values of 1.5kΩ/ . Hence, it is possible to use wide emitter stripes, up to 2 µm, for power HBTs without any degradation of the rf performance. SiGe1 consists of a special self-aligned emitter module using poly-Si as contact material and two metallazation levels. The technology is planar and comparable in terms of masks and costs to a standard double poly Si BJT process. SiGe1 is well suited for LSI, as nicely demonstrated in Fig.1, which shows a wafer mapping of 10k transistor arrays over a typical 6 inch wafer.

Circuits

On research level a couple of circuits were investigated in the last few years, e.g. a digital to analog converter (DAC) from IBM in 1993 [6], an optical transmitter circuit from NEC in 1994 [7], VCOs at 26GHz and 40 GHz from Daimler-Benz in 1995 [8], and a frequency divider by Hitachi in 1998 [9]. However, at the moment the bigest market share for SiGe is be seen in wireless communication systems in the 1 - 6 GHz range. Hence, mixers, GSM power modules, dual band frontends for GSM and PCS1800 and DECT frontends are in the focus. DECT frontends including LNAs with 1.5dB noise figure and 20dB gain combined with a 28dBm power amplifier with 47% PAE over the whole packaged device are production ready. LNAs with noise figures of 1.7 dB at 5.8GHz were recently fabricated using SiGe1. As example for the high quality of SiGe-HBTs Fig.2 shows the gain, rf output power and the PAE value of a DECT power transistor from load pull measurements.
In addition a couple of SiGe-IC measurements will be presented at the conference.

[1] K. Oda, E. Ohue, M. Tanabe et al. IEDM Tech. Dig. (1997), pp. 791-794
[2] A. Schüppen, U. Erben, A. Gruhle et al. IEDM Tech. Dig. (1995), pp. 743-746
[3] K. Wahio, E. Ohue, K. Oda et al. IEDM Tech. Dig. (1997), pp. 795-798
[4] H. Schumacher, U. Erben, A. Gruhle, IEEE MTT-S Dig. (1994), pp. 1167-1170
[5] A. Schüppen, H. Dietrich, S. Gerlach et al. IEEE BCTM (1996), pp. 130-133
[6] D.L. Harame, J.M.C. Stork, B.S. Meyerson et al., IEDM Tech. Dig. (1993), pp. 71-74
[7] T. Hashimoto, H. Tezuka, F. Sato et al., BCTM (1994), pp. 163-170
[8] A. Gruhle, A. Schüppen, U. König et al., IEDM Tech. Dig., pp. 725-728
[9] ISSCC (1998), pp.

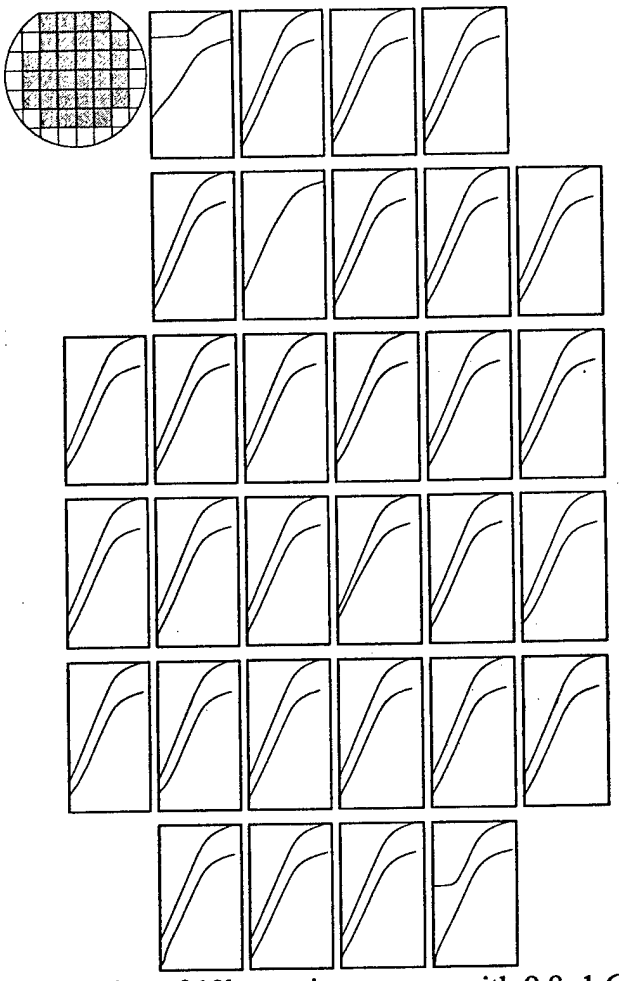

Fig.1: Gummelplot wafer mapping of 10k transistor arrays with 0.8x1.6µm^2 SiGe-HBTs
y-axis: 1pA-100mA, x-axis: 0.2-1V

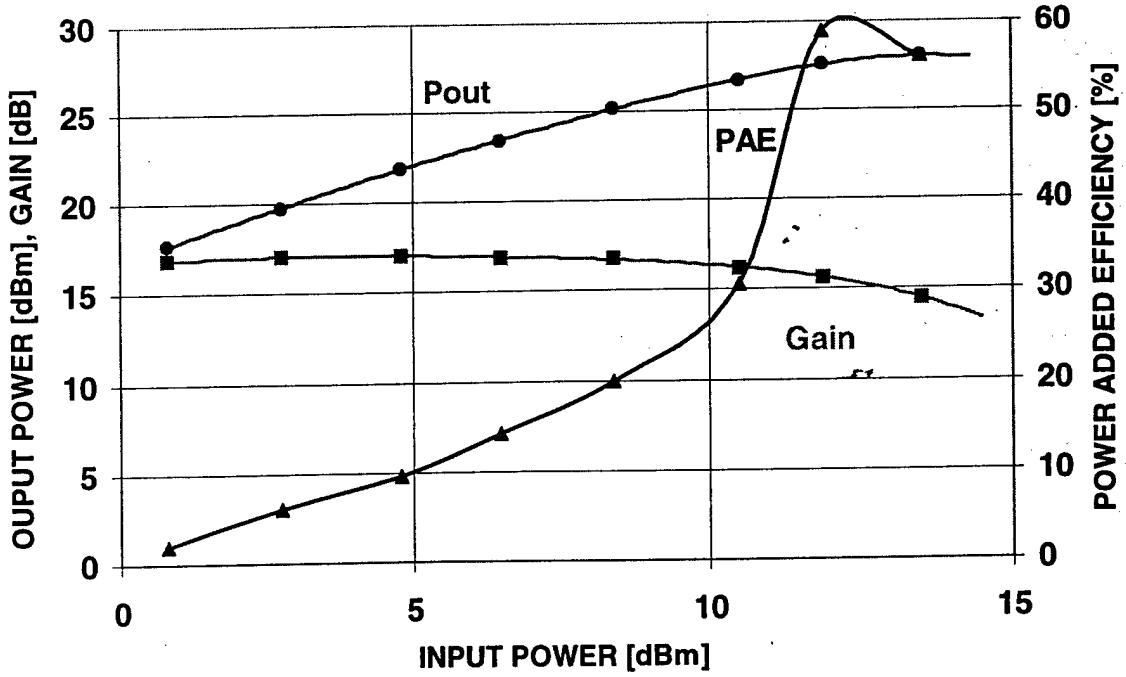

Fig. 2: Load pull measurement at 1.9 GHz of a SiGe Power HBT with 60 x 2 x 30µm^2 emitter area. DC opertion point is V_{CE} = 3.6V, I_C = 270mA, class AB

n- and p-Type SiGe HFETs and Circuits

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The SiGe/Si heterosystem and its compatibility to the dominating Si-technology opens perspectives for a new generation of high volume microelectronic components. After the successful implementation of SiGe HBT into production a breakthrough is now expected for SiGe hetero fieldeffect transistors (SiGe HFETs). Not only that the speed of n-type HFETs is already above standard n-Si-MOSFETs (inspite of a non selfaligned layout) rather the speed of p-type HFETs is even twice that of p-Si-MOSFETs. First circuit demonstrators are available too.

n-HFETs

The transconductances of n-HFETs with a Si-channel embedded into SiGe layers (up to 45% Ge) reaches around 300 mS/mm for depletion and up to 500 mS/mm for enhancement operation at RT. Respective currents have been up to 320 mA/mm or 200 mA/mm. Cut-off frequencies f_{max} up to 92 GHz and f_T up to 46 GHz have been extrapolated from the gains of 0.15 to 0.2 µm HFETs (Fig. 1) at a gate bias from 0 to -2V and supply voltages close to 1 or 2 V (Fig.2).

p-HFETs

The transconductances of p-HFETs (Schottky- or MOS-gated) with a SiGe- (30% Ge) or a Ge-channel show the gate length dependence plotted in Fig. 3. Intrinsic transconductances are up to 100 mS/mm higher. High currents up to 700 mA/mm have been measured for MOS-gated HFETs. For 0.25 µm p-HFETs we obtained f_{max} up to 66 GHz and f_T up to 35 GHz at a gate bias of 0.4 to 0.6 V (Fig. 4, 5).

HFET circuits

First demonstrator circuits are using n-type SiGe HFETs. A digital chip contains ring oscillators (23 and 43 steps), inverters, level shifters and test circuits. An analog chip focussed on transimpedance amplifiers with various input and output stages and up to 8 transistors per output stage. In this very preliminary phase we chose a flexible design in order to accept both depletion and enhancement HFETs as well as technology related scatter in parasitic elements. The chip technology is based on e-beam gates from 0.8 to 0.15 µm and on two interconnect levels. Large signal measurements of the inverter with an input signal of 600 ps rise time at a supply voltage of V_{dd} = 2V show a gate delay of 70 ps for the 300 nm gate length. The maximum output voltage swing is 430 mV. Measurements with an input signal of 150 ps rise time show a gate delay of 22 to 25 ps for the 150 nm gate length inverter circuit (Fig. 6). The gate delay was determined from the delay between the 50% input and output signal value, taking into account the different RC-delays of the measurement equipment. Amplifiers passivated with a CVD oxide show a high transimpedance of 56 dBΩ with a -3 dBΩ frequency of 1.8 GHz (Fig. 7). Circuits with sputter oxide passivation yield a higher transimpedance of up to 72 dBΩ with 1 GHz bandwidth.

SiGe enables equal performance of n- and p-HFETs. Regarding the above results for discrete HFETs we are close to this target. A superior generation of CMOS circuits can be envisaged (SiGe HCMOS). Simulations predict gate delays down to 1 ps in unloaded and around 3 ps in loaded operation (Fig. 8), furthermore a power-delay product below 1 fJ.

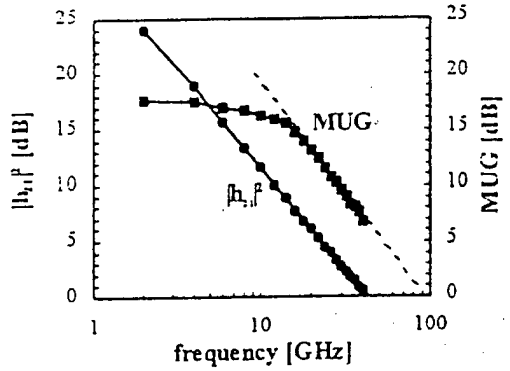

Fig. 1: Gains of n-HFETs to extrapolate f_T and f_{max}

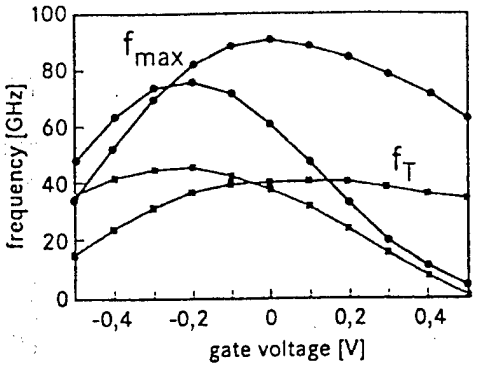

Fig. 2: Gate bias dependence of frequencies for n-HFETs

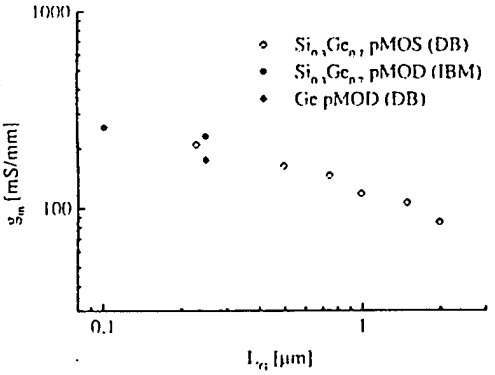

Fig. 3: Gate length dependence of the transconductance for p-HFETs

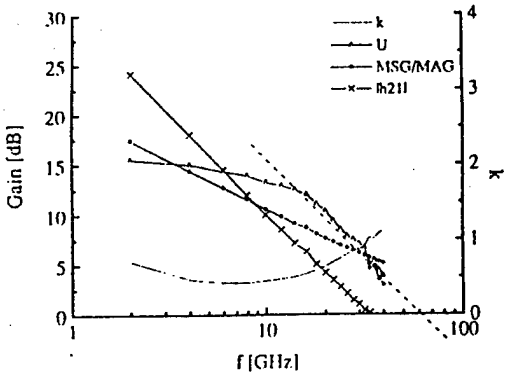

Fig. 4: Gains of p-HFETs to extrapolate f_T and f_{max}

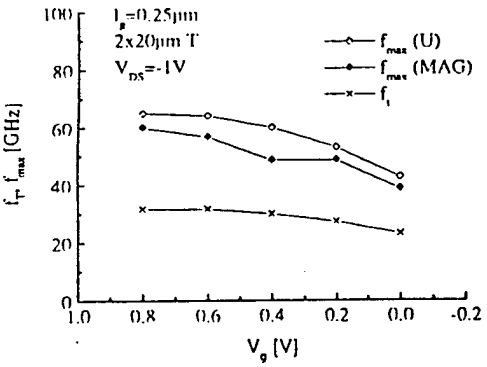

Fig. 5: Frequencies of p-HFETs in dependence of gate bias

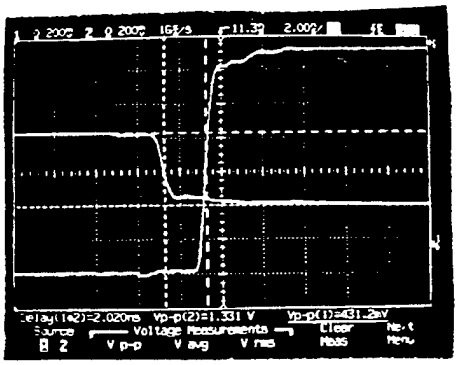

Fig. 6: Gate delay and output voltage swing of a n-HFET inverter

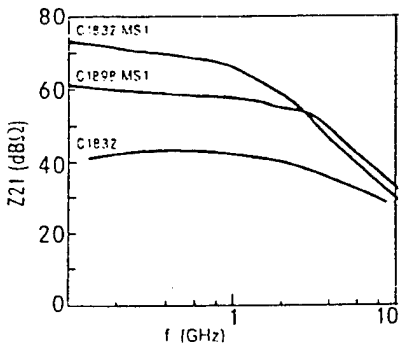

Fig. 7: Transimpedances of some SiGe HFET amplifiers

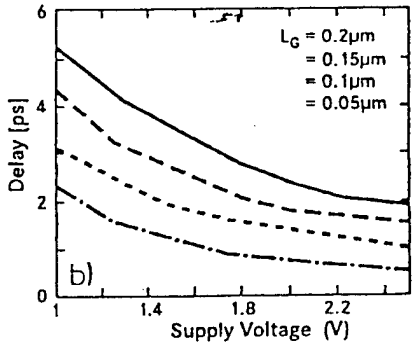

Fig. 8: Speed potential of a novel SiGe HCMOS generation made of n- and p-HFETs

Process design for SiGe-HBTs prepared using cold-wall UHV/CVD

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We have studied the process and intrinsic base design of SiGe heterojunction bipolar transistors (HBTs) prepared using a cold-wall ultra-high vacuum (UHV)/CVD technique. During heat treatment after the SiGe base formation, boron diffusing out of the p^+-SiGe to the n-Si collector forms a parasitic energy barrier [1], [2] that prevents minority carrier current flow. To avoid generating this barrier, we carefully design the process conditions. Two effective techniques are lowering the processing temperature and optimizing the base profile.

The experimental self-aligned SiGe-HBT we used is shown in Fig. 1. Its base layer is formed using selective epitaxial growth (SEG) technology [3]. The SEG layer is a triple layer [4]. The first layer grown on the Si collector is an undoped $Si_{0.9}Ge_{0.1}$ spacer layer with constant Ge concentration; it acts as a spacer blocking the boron out-diffusion, located between the Si collector and the p^+ base. This initially undoped layer is doped with phosphorus (about 1×10^{17} cm^{-3}) by using ion implantation immediately before emitter polysilicon deposition. The middle layer is a p^+-graded SiGe layer; it serves as the intrinsic base. The upper layer is a pure Si layer; it is doped with n-type impurity during the emitter drive-in process. To study the effect of the process and intrinsic base design on the SiGe-HBT characteristics, we examined three points: the effect of the CVD temperature (>800℃, <700℃), the effect of the emitter-doping impurities, and the effect of the spacer thickness. The process flow used is illustrated in Fig. 2. We measured the cut-off frequency f_T vs. collector current I_C characteristics of a Si bipolar junction transistor (BJT) and a SiGe HBT (30-nm undoped SiGe layer) fabricated using high temperature oxide (HTO) film and in-situ As-doped polysilicon. They have the same as-grown boron-doping profile in the SEG layer. As shown in Fig. 3, the measured f_T for the Si BJT was 28 GHz, but for the SiGe HBT, it was as low as 12 GHz. This difference can not be explained by the base width, because the reported boron-diffusion coefficient for SiGe is about one order of magnitude smaller than that for Si. The potential barrier blocks the electron flow from the emitter through the base to the collector. The temperature dependence of current gain h_{FE} for the SiGe-HBT and the Si-BJT is shown in Fig. 4. The current gain of the SiGe-HBT decreased with the temperature, in spite of the nearly temperature-independent characteristics of the Si-BJT. This indicates the presence of a parasitic energy barrier. To reduce the processing temperature, we used low temperature oxide (LTO) film and in-situ phosphorus-doped polysilicon for the emitter electrode instead of the HTO film and As-doped polysilicon. The h_{FE} vs. $1/T$ characteristics of SiGe-HBTs with a 15- or 30-nm undoped-SiGe layer are show in Fig. 5. With the 15-nm-thick SiGe spacer, h_{FE} was nearly independent of temperature, like for the Si-BJT. In contrast, with the 30-nm-thick spacer, it increased with a decreasing temperature. Figure 6 shows the f_T vs. I_C characteristics of the SiGe-HBTs shown in Fig. 5. A maximum cut-off frequency of 63 GHz was obtained for the SiGe-HBT with the 30-nm undoped SiGe spacer.

In summary, we have studied the process design of SiGe-HBTs. Compared with the 28-GHz f_T of the Si-BJT, the f_T of the SiGe HBT with a parasitic energy barrier was 12 GHz in spite of the same as-grown boron doping profile. Reducing the processing temperature changed the temperature dependence of the current gain; that is, h_{FE} increased with a decreasing temperature. A maximum cut-off frequency of 63 GHz was obtained.

References

[1] E. J. Prinz et al., in *IEDM Tech. Dig.*, p. 639, 1989.
[2] J. W. Slotboom et al., *IEEE Electron Device Lett.*, vol. 12, p. 486, 1991.
[3] F. Sato et al., *IEEE Trans. Electron Devices*, vol. 41, p. 1373, 1994.
[4] F. Sato et al., *IEEE Trans. Electron Devices*, vol. 42, p. 483, 1995.

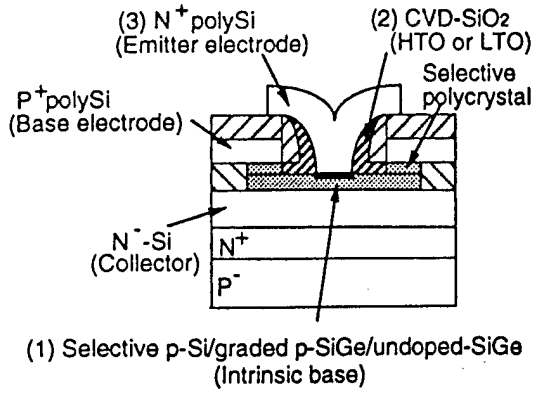

Figure 1: Schematic cross section of SiGe-HBT. Selective epitaxial base is triple layers, p-Si/p-graded SiGe/undoped-SiGe.

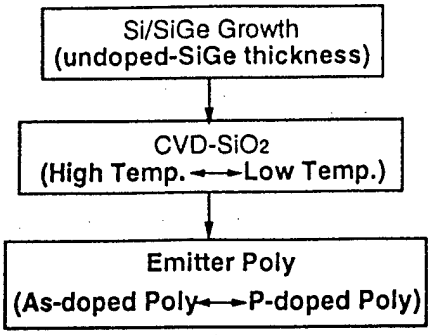

Figure 2: Main process flow after Si/SiGe growth. Three points were studied: (1) undoped SiGe layer thickness, (2) CVD-SiO2 deposited at high (>800℃) or low (<700℃) temperature, and (3) emitter polysilicon dopant (arsenic or phosphorus).

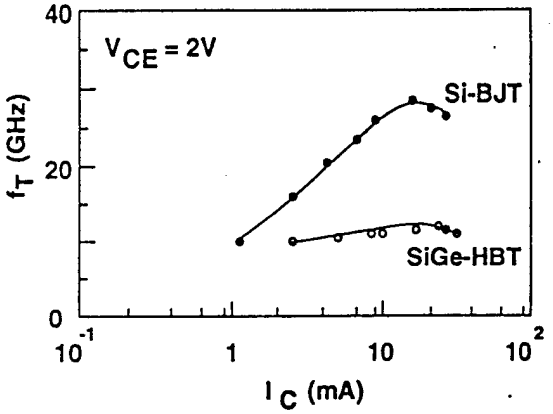

Figure 3: f_T vs. I_C characteristics of SiGe HBT (30-nm undoped-SiGe layer) and Si BJT using HTO film and in-situ arsenic-doped emitter polysilicon. They have the same boron-doping profile in SEG layer.

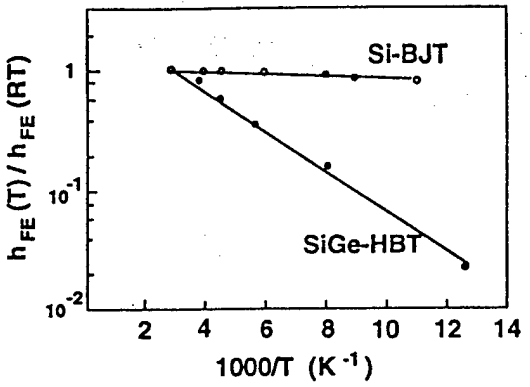

Figure 4: Current gain vs. reciprocal temperature characteristics of SiGe HBT and Si-BJT shown in Fig. 3. Temperature dependence of current gain of SiGe-HBT suggests that it has parasitic energy barrier.

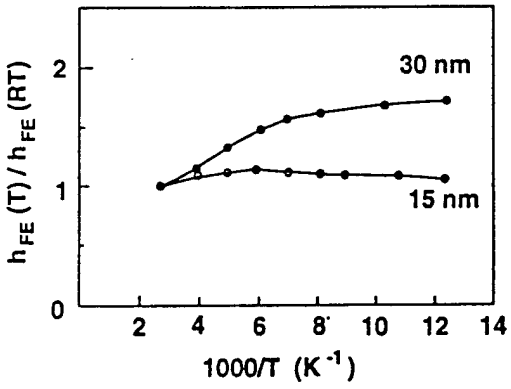

Figure 5: Current gain vs. reciprocal temperature characteristics of SiGe-HBTs with 15 or 30 nm undoped-SiGe layer using LTO film and in-situ phosphorus-doped emitter polysilicon.

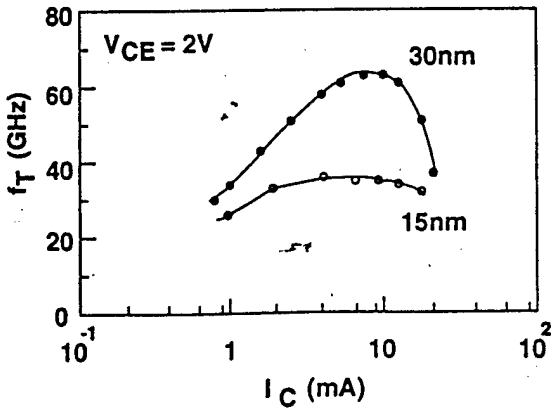

Figure 6: f_T vs. I_C characteristics of SiGe-HBTs shown in Fig. 5.

GaInAs/AlAs/InP resonant tunneling diodes by MOVPE

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GaInAs/AlAs/InP resonant tunneling diodes(RTDs) were fabricated by metal organic vapor phase epitaxy (MOVPE). Observed peak to valley(P/V) current ratios of fabricated RTDs were 5.7 at 77K and 3.3 at 300K. To our knowledge, this is the first report of GaInAs/AlAs/InP RTDs by MOVPE.

Recently, integrated circuit by a combination with RTDs and other electron devices, such as HEMT, exhibited high-speed capability in logic circuits[1]. As material, GaInAs/AlAs heterostructure on InP substrate was used for RTDs because InP-based electron devices shows the highest speed as electron devices[2] while AlAs barriers on InP provides high P/V current ratio at room temperature[3]. To grow RTDs, molecular beam epitaxy(MBE) was used from the nature of abrupt heterointerface. However, MOVPE has superior characteristics in InP related material and successive growth by MBE and MOVPE was carried out for HEMT/RTDs circuits[1]. On the other hand, we studied InP-based RTDs by MOVPE and reported good P/V ratio[4]. In this report, GaInAs/AlAs/InP resonant tunneling diodes(RTD) grown by MOVPE are presented.

The apparatus for MOVPE has a horizontal reactor with low pressure of 76 Torr. The source materials used in the MOVPE were trimethylindium, triethylgallium and trimethylaluminum(TMA) as III group gas, arsine for group V and disilane for n-type dopant. The growth temperature was 600℃. The growth rate and the V/III ratio of GaInAs were 1.7μm/h and 70, respectively. The partial pressure of As was 0.76 Torr. The RTD structures is shown in Fig.1. The barrier thickness of AlAs was designed as 3nm. The contact layer was 30nm-thick n^+-GaInAs layer with doping of $1x10^{18}cm^{-3}$ and emitter and collector were 360nm-thick n-GaInAs with doping concentration of $3x10^{17}cm^{-3}$. As the spacer layers, 5nm-thick undoped GaInAs layers were inserted between barriers and n-GaInAs.

After the growth, diodes were fabricated by the following process. Cr/Au dots with area of $100x100\mu m^2$ were evaporated with the metal mask on the wafer. Dots were separated into mesas by Br-methanol etching down to the RTD structure. After etching, Cr/Au was evaporated on the reverse side of the wafer. I-V characteristics were measured at 77K and room temperature. Observed characteristics are

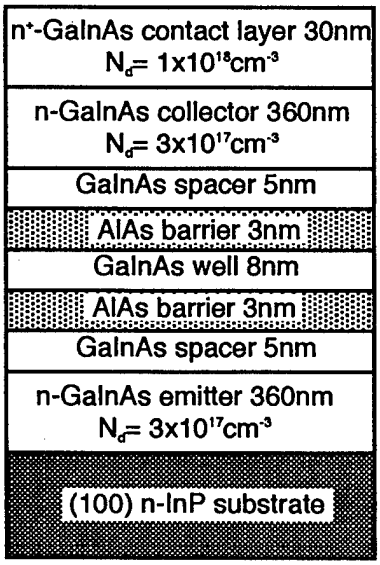

Fig.1 Grown structure for GaInAs/AlAs RTDs

shown in Fig.2. Highest P/V current ratios at 77K were 2.9 in the forward bias conditions and 5.7 in the reverse bias conditions. At 300K, highest P/V current ratios reduced to 2.0 in the forward bias conditions and 3.3 in the reverse bias conditions. To our knowledge, this is the first observation of negative differential resistance(NDR) of GaInAs/AlAs/InP RTDs grown by MOVPE. Highest peak current density was 0.55 A/cm^2

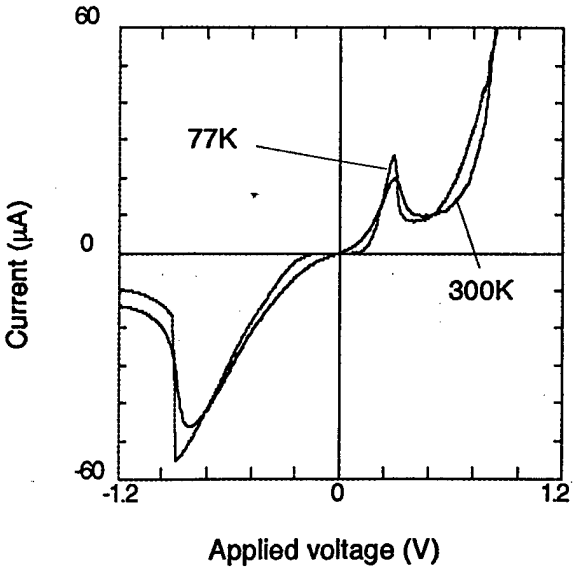

Fig.2 Measured I-V characteristics of GaInAs/AlAs RTD at 77K and 300K

Observed current density was extremely lower than reported values[2]. We estimate the growth rate of AlAs from reported vapor pressure of TMA, pressure of bubbler, flow rate and growth rate of InP. However, when we grew RTDs with 4.5nm-thick AlAs as designed thickness, no NDR was observed. If actual thickness was 4.5nm, we could expect NDR because 4.5nm is lower than critical thickness and NDR by MBE was reported[5]. Thus more introduction of TMA from estimated value or dynamic change of growth rate at heterointerface[6] would be reasons of lower current density. Low P/V current ratio may be explained by low current density because leakage current at surface can be a reason.

We used different apparatus from former InP RTDs because of Al source. Thus GaInAs/InP RTDs were fabricated as reference. The structure was same as for the the GaInAs/AlAs RTD shown in Fig.1, except that the barriers were 8nm-thick InP. Observed highest P/V ratio was 1.9 and this value was lower than our previous value. Thus poor abruptness at heterointerface grown by new apparatus might be the reason of low P/V ratio in GaInAs/AlAs RTDs.

We appreciate Profs. S.Arai, M.Asada and M.Watanabe and Dr. M.Suhara for fruitful discussion and Messrs T.Kojima, and T.Arai for experimental support. This work was supported by a Scientific Grant-In Aid from the Ministry of Education, Science, Sports and Culture and by the "Research for the Future" Program #JSPS-RFTF96P00101 of the Japan Society for the Promotion of Science(JSPS).

1. K.J.Chen, K.Maezawa, M.Yamamoto, IEEE Electron Device Lett., **17**, (1996) 127.
2. e.g., T.Enoki, H.Yokoyama, Y.Umeda and T.Otsuji, Int. Conf. on Solid State Devices and Materials, D10-1, 1987.
3. T.Inata, S.Muto, Y.Nakata, S.Sasa, T.Fujii, and S.Hiyamizu, Jpn.J.Appl.Phys., **26**, (1987) L1332.
4. T.Sekiguchi, Y.Miyamoto and K.Furuya, J.Crystal Growth **124**, (1992) 807
5. J.P.Mattia, E.R.Brown, A.R.Calawa and M.J.Manfra, Appl.Phys.Lett., **63**, (1993) 521.
6. L.Samuelson, M-E. Pistol, W.Seifert, J.O.Frobnell and L.Ledebo, Inst.Phys.Conf.Ser., **106**, (1990) 897.

Advanced Heterostructure Transistor Technologies for Wireless Communications

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Abstract

Wireless Communications in recent years have experienced continuous and phenomenal growth, especially in the below 3 GHz applications. Recently FCC auctioned off the LMDS frequency band (millimeter wave) for point-to-point applications, which should be a boost to the millimeter wave market. The equipment manufacturers are constantly looking for better parts and lower price; and the market changed from the past 10 years when buyers looked for "qualified parts" to now when buyers look for "better-valued parts." This presents a market need for the Heterostructure Transistor Technologies.

Below 3GHz applications include cellular, PCS, GPS, ISM applications (WLAN, WLL, etc at both 900 and 2400MHz bands) and LEO satellite communications (e.g. Iridium and Globalstar). The cellular/PCS market covers many different systems, for example: GSM, CDMA, TDMA, DECT, PDC, PHS, and W-CDMA. From the RF design consideration, these systems have different RF power requirement, different signal modulation approach and different frequency bands; therefore different technical demands on the RF architecture and components. In ISM band, there is an even broader range of technical variety than the cellular/PCS market.

One key technical demand on the RF components below 3GHz is the linearity. This is because the cellular/PCS environment is "interference dominated", which is very different from "noise dominated" scenario in the satellite communication. Many Cellular/PCS users are sending out and receiving RF signals simultaneously; through the non-linearity of the receiver, an interference can be generated by signals in other channel. On the other hand, the noise performance is not as critical since the background noise on the horizon is much higher than the noise from the sky.

Silicon bipolar transistor and GaAs FET are the two workhorse technologies for the low frequency wireless market till now. In the millimeter wave band, two-terminal devices (Schottky diode and Gunn device) are still popular in production. Recently, GaAs PHEMT, GaAs HBT, SiGe HBT are all gaining acceptance into the wireless market. The advantages of these heterostructure transistors will be discussed according to the application requirements in the following paragraphs.

Silicon bipolar transistor is widely used in small signal circuits, such as modulator, variable gain amplifier, low noise amplifier, down-convert mixer. GaAs FET is used in the power amplifier, as well as in the LNA/mixer. The advantages of Si bipolar transistor are its high transconductance in the high-frequency analog circuit and its requirement of only single polarity power supply. GaAs FET, with a high breakdown

voltage and high frequency performance through most bias condition, is very attractive in the power amplifier for its efficiency and gain. However GaAs FET requires a negative gate bias, and a P-channel transistor for power down; these two add to the cost and PCB area.

- SiGe HBT
  SiGe HBT has a performance improvement over the Si Bipolar Transistor. However it still has a low breakdown voltage making it an unfavorable choice for power application. It can be a good candidate for high-speed digital LSI circuitry with its large wafer size and traditional interconnection on Si wafer. The technology is not yet mature with commercial product.

- GaAs HBT
  GaAs HBT in general have about twice the f_{max} of the best Si bipolar transistor. Together with the semi-insulating substrate advantage, GaAs HBT can more than double the frequency response of an analog circuit. Its breakdown voltage is high (>10V BV_{ceo} is easily achievable), allowing RF power application. Compared with GaAs FET power amplifier, GAAS HBT amplifier does not require the negative gate bias, or the p-channel power down transistor. Although GaAs HBT technology cannot make good RF switch, overall GaAs HBT is the most attractive one for the below 3GHz application.
  Although GaAs HBT research has shown result in the Ka band, it is still uncertain whether HBT can have a production edge over GaAs PHEMT in such case.

- GaAs PHEMT
  The first large-scale application of PHEMT is the low noise transistor of DBS. For the below 3GHz application, the noise advantage is not so prominent in the "interference dominant" environment. In power application, it suffers from the same disadvantage as GaAs FET.
  In millimeter-wave application, such as LMDS, GaAs PHEMT offers obvious advantage over other technologies. It has good gain, good noise, and power performance. With the MMIC approach it also offers good performance/cost tradeoff.

Heterostructure transistors based on InP substrate is not as mature as the above three technologies. The performance advantage in circuitry is not obvious either. The major attraction is the OEIC integrated with InP-based laser/detector.

Summary:

Heterostructure transistors are receiving wide acceptance into the wireless application. However the number of suppliers is still limited and each supplier has its own "recipe" and strategy. Since the users are looking for "solution and value" and is not committed to any technology, the supplier's business execution and implementation is most critical for the success of the technology.

A Novel GaAs Flip-Chip Power FET with High Gain and Efficiency

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Abstract

This paper describes leading edge technology of GaAs power FET that can achieve high gain, efficiency and high thermal stability.

GaAs power FETs have been widely used as key devices for mobile communication systems. In those systems, both low voltage and high efficiency operations are major concern for the power FETs because these performances give long battery life and small volume in the handy phone set. In order to achieve higher gain and efficiency, we developed the spike gate MODFET [1], [2] assembled by flip-chip technology.

Figure 1 shows the cross-sectional view of the spike-gate power FET. Sub-quarter micron footprints of the spike-gate were defined by using the phase shift lithography. Since the effective gate length is determined by the bottom of the gate metal, the highest transconductance and the lowest on-resistance are obtained. The comparison of DC characteristics with and without spike-gate is summarized in Table 1. The attained on-resistance of 1.5 Ω-mm of the device with the spike-gate is less than a half of the FET without spike. The fringe of the spike-gate plays a role of relieving the electric field between the gate and drain. There observed little increase of the resultant drain conductance compared with the FET without spike.

Flip-chip technology has the advantage of high gain in the high frequency characteristics. Since the FET operates free from the parasitic inductances caused by bonding wires, the nagative feedback can be eliminated. The schematic cross-sectional view of the fabricated flip-chip power FET is shown in Fig. 2. The gold-electro-plating was used as the thermal bump on the FET active area. The device was mounted on aluminum nitride (AlN) substrate. Figure 3 shows the resultant relationship between the duration of DC power and the increase of the device temperature. The obtained thermal resistance of the flip-chip power FET is 12 ℃/W which is even lower than that of conventional wire-bonded one.

The gate orientation was chosen to <010> in order to compensate the temperature drift of the FET performances such as drain current, threshold voltage and gate-source capacitance [4]. These performances are strongly dependent on the mechanical stress caused by the difference of thermal expansion coefficient which generates piezoelectric charge in the channel.

Power performance of the fabricated power FET was measured using the automated tuner system. The resultant output power is shown in Fig. 4 as a function of the input power. The power-added efficiency of 70 % can be obtained even when the supply voltage is reduced down to 1.5 V. This high performance with low supply voltage is owing to the unique spike-gate structure. By eliminating parasitic wire inductance, the linear gain of the FET is improved 2 dB resulting in increasing PAE (power-added efficiency) of 5 % compared to that of conventional wire-bonded ones. The comparison of the RF performances between these devices are summarized in Table 2.

[1] T. Tanaka et al., IEEE Trans on Electron Devices, Vol. 44, No. 3, pp. 354-359, 1997
[2]H. Furukawa et al., Solid-State Electronics Vol. 41, No. 10, pp. 1599-1640, 1997
[3] T. Tanaka et al., 1997 IEEE IEDM Technical Digest, 557-560, 1997

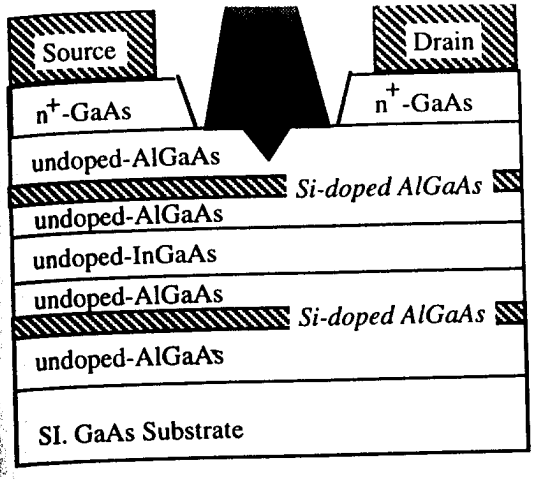


Fig. 1 Structure of spike-gate Power MODFET.

Table 1 Comparison of spike-gate Power MODFET with conventional 0.5um MODFET.

Parameter	Spike gate MODFET	0.5um MODFET
Ron (Ω-mm)	1.5	2.8
gmmax (mS/mm)	280	220
gd (mS/mm)	5.7	5.6
BVgd (V)	13	13
Idmax (mA/mm)	650	450

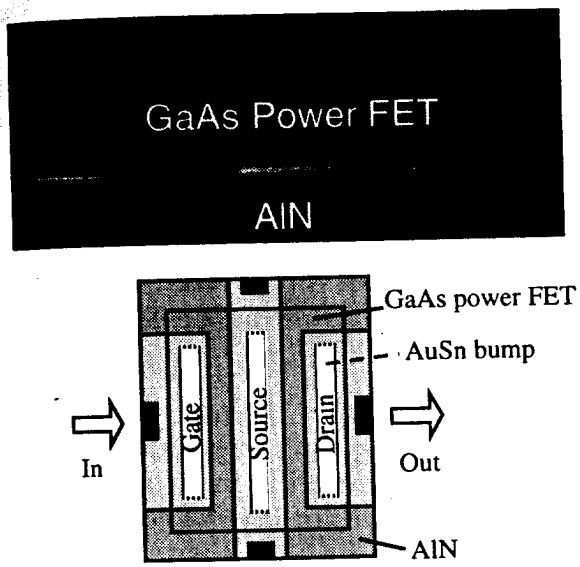


Fig. 2 Cross-sectional SEM of flip-chip spike-gate Power MODFET.

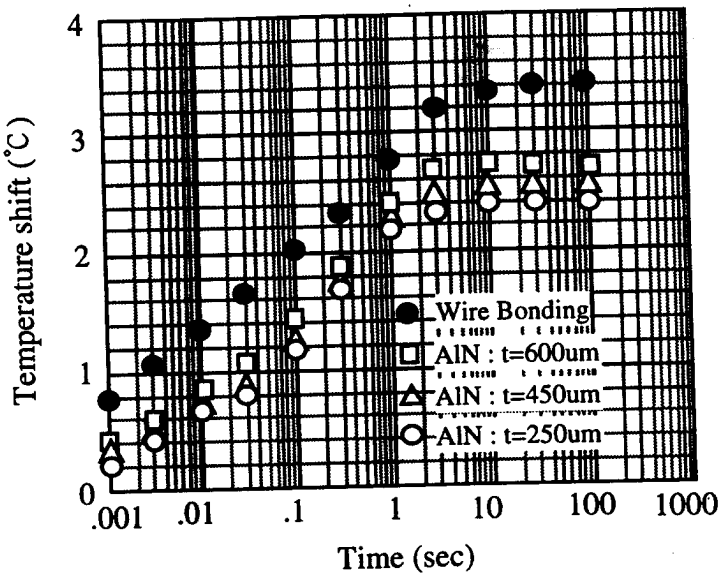
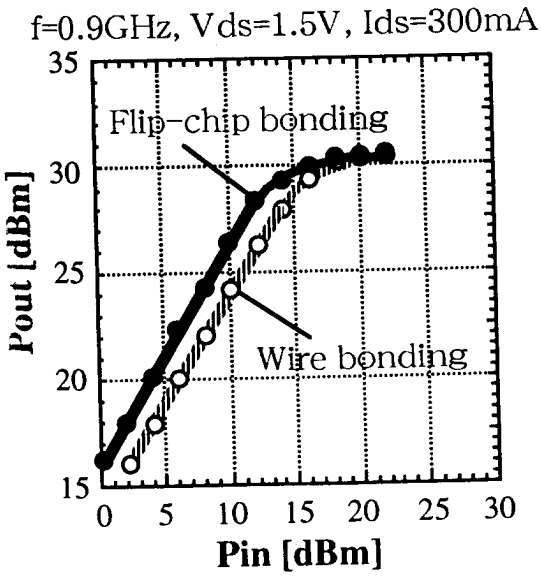


Fig. 3 The relationship between the supplied time of the DC power and the increase of the device temperature. Supplied peak DC power is 0.2W.



g. 4 Pin-Pout characteristics for flip-chip and wire nding spike-gate power MODFET.

Table 2 Summary of the RF performances compared flip-chip bonding Power MODFET with wire bonding one.

Parameter	Flip-chip bonding	Wire bonding
Rth (°C/W)	12	17
Gain (dB)	16	14
PAE (%)	71	65
Psat (dBm)	30	30
P1dB (dBm)	28.8	28.5
S12 (dB)	-40	-40

A Low Power Dissipation 0.4~7 GHz Transimpedance Amplifier IC for SCM Optical Communication System

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A low power dissipation and ultra broadband transimpedance amplifier IC has been developed for sub-carrier multiplexing (SCM) optical communication system represented by multichannel video signal transmission. High transimpedance gain of 52 dBΩ and low group delay deviation less than 30 ps has been obtained for 0.4 to 7 GHz. Low equivalent input noise current of 12 pA/$\sqrt{}$Hz has been also obtained. By using integrated STO ($SrTiO_3$) capacitors for DC blocking, power dissipation of 300 mW is realized, which is less than 1/2 compared with conventional transimpedance amplifier.

For optical transimpedance amplifier, broad band-width and low noise performance are required with low power dissipation. The SCM optical communication system requires flat gain and low group delay deviation to achieve extreme low distortion characteristics. Then, we adopted a 0.25 μm pseudomorphic double heterojunction modulation doped FET (MODFET) in order to minimize total input capacitance. A novel STO capacitor process technology is also incorporated.

Figure 1 shows the cross-sectional structure of 0.25 μm MODFET [1]. The active part consists of an undoped InGaAs channel layer sandwiched between an upper n-AlGaAs layer and a lower n-AlGaAs layer. An i-AlGaAs layer is inserted as a schottky barrier between n-GaAs and n-AlGaAs layer to improve breakdown voltage. The threshold voltage (Vth) is selected at -0.6 V. The obtained maximum transconductance (gmmax) is 450 mS/mm. The current gain cutoff frequency (ft) and maximum frequency of oscillation (fmax) are 42 GHz and 110 GHz, respectively.

Figure 2 shows the schematic cross-section of the IC. We have developed STO ($SrTiO_3$) capacitor on the GaAs epitaxial substrate by using low-temperature RF sputtering method [2]. We have successfully integrated large value capacitors (~200 pF) on the IC without degrading the elaborate epitaxial layers by depositing STO film at the temperature of 200 °C. Figure 3 shows the microphotograph of the fabricated transimpedance amplifier IC.

The feedback resistance Rf is determined to 270 Ω in order to obtain required band-width up to 6 GHz. The output impedance is designed to be matched with 50 Ω to prevent the reflection at the output port. Figure 4 shows the circuit diagram of the transimpedance amplifier IC. To realize wide-temperature-range operation, level shifting diodes are eliminated from the conventional circuit replaced by STO capacitors for DC blocking. As a result, this IC operates at single low supply voltage of +5 V without minus supply voltage (except gate bias voltage), and less than 1/2 power dissipation is realized compared with conventional IC with level shifting diodes. Figure 5 shows the transimpedance gain of the IC measured with an avalanche photo diode (APD). The high transimpedance of 52 dBΩ and the -3 dB band-width of 7 GHz have been obtained. Figure 6 shows the group delay of the transimpedance amplifier IC. The low group delay deviation less than 30 ps has been obtained.

[1] H. Masato et al., "AlGaAs/GaAs/InGaAs Double-Doped Quantum-Well HEMTs for Low Distortion Amplifier", SSDM Digest pp.715-717, 1993.
[2] M. Nishitsuji et al., "ADVANCED GaAs-MMIC PROCESS TECHNOLOGY USING HIGH-DIELECTRIC CONSTANT THIN FILM CAPACITORS BY LOW-TEMPERATURE RF SPUTTERING METHOD", IEEE GaAs IC Symposium pp.329-332, 1993.

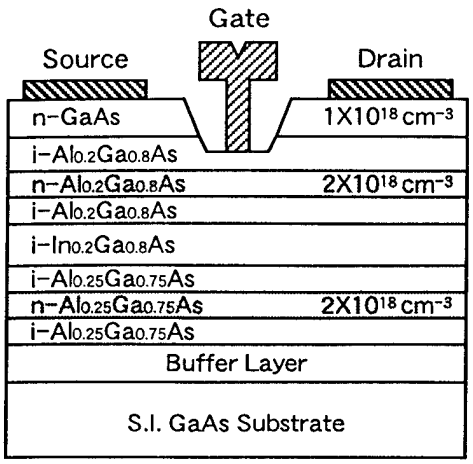

Fig.1. Cross-sectional structure of the 0.25 μm MODFET.

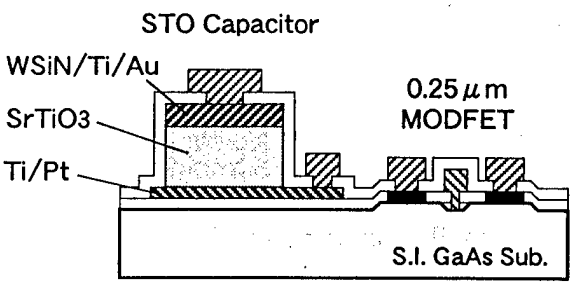

Fig.2. Schematic cross-section of the IC with integrated STO ($SrTiO_3$) Capacitor.

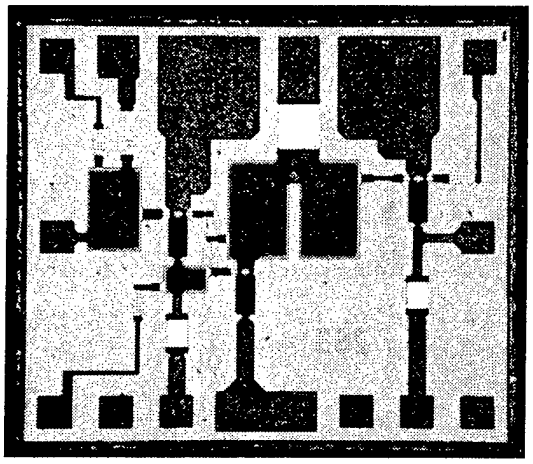

Fig.3. Microphotograph of the fabricated IC. Chip size is 1.29 mm × 1.14 mm.

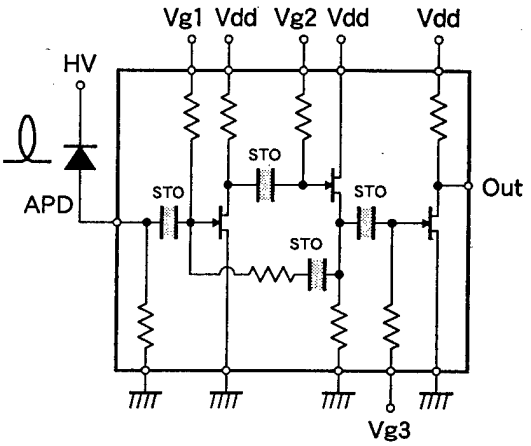

Fig.4. Circuit diagram of the transimpedance amplifier IC.

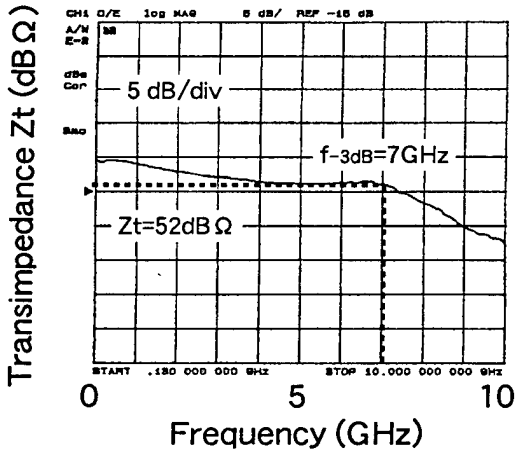

Fig.5. Transimpedance Zt of the IC.

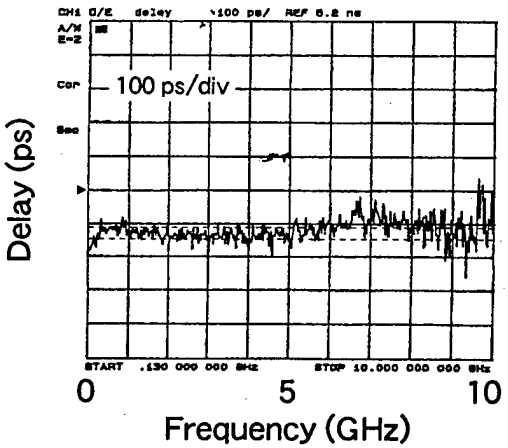

Fig.6. Group delay of the IC.

44% Efficiency Power Heterojunction FET Operated at 3.5V for 1.95GHz Wide-Band CDMA Cellular Phones

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This paper describes 1.95GHz power performance of a double-doped AlGaAs/InGaAs/AlGaAs heterojunction FET(HJFET) operated at 3.5V drain bias voltage for Wide-band CDMA(W-CDMA) cellular phone systems. Since the W-CDMA systems require strict distortion criteria[1] as compared to the IS-95 systems, a lower distortion power transistor with a high power added efficiency(PAE) is demanded. In addition, a low on-resistance(R_{on}) is a key issue for low voltage operation[2]. We have reported a double-doped HJFET which shows R_{on} of 2.1Ω·mm with 50% PAE at the IS-95 criteria[3]. In this work, further reduction of R_{on} has been accomplished with a novel power HJFET structure, and this results in a high PAE at the W-CDMA criteria.

We investigated two novel designs for the HJFET. The first is a narrow recessed structure. In the investigation, total recess width(L_w) from 1.0 to 2.3μm were evaluated with a 0.7μm long gate. We found that 1.0μm shrinkage of L_w reduced R_{on} by 0.3Ω·mm. An HJFET with a gate-to-drain spacing(L_{gdr}) of 0.4μm achieved a gate-to-drain voltage(BV_{gd}) of more than 13.5V, which was sufficiently high for Li-ion battery operation. Thus the optimized recess structure was determined to be L_w of 1.5μm with L_{gdr} of 0.4μm. The second is a multilayer cap consisting of highly Si-doped GaAs, undoped GaAs and highly Si-doped AlGaAs layers. With this layer structure, 0.1Ω·mm reduction of R_{on} was achieved. This is due to reduction of the contact resistance between the cap and the channel layers. As a result, the developed HJFET shows a low R_{on} of 1.4Ω·mm. This R_{on} is 0.7Ω·mm lower than the previously reported HJFET[3]. The maximum drain current of the HJFET estimated at a gate-to-source voltage(V_{gs}) of 1.5V was 580mA/mm. The maximum transconductance of 400mS/mm was achieved at around V_{gs}=0V. The threshold voltage was -0.6V.

1.95GHz power performance of a 25.6mm gate width HJFET was evaluated with QPSK signal of 4.096MHz channel width. Through load-pull measurements, the optimum load impedance(Z_L) for maximum PAE while maintaining an adjacent channel leakage power ratio(ACPR) of less than -43dBc and an output power(P_{out}) of 28dBm was found to be 4.0-j12.2Ω. At a drain bias voltage(V_{ds}) of 3.5V and a quiescent drain current(I_q) of 80mA, the HJFET exhibited P_{out} of 600mW(28.0dBm) with PAE of 44.2% and an associated gain(G_a) of 9.7dB with ACPR of -43dBc. This PAE is the best value among power transistors for the W-CDMA systems. The power performance was also evaluated as a function of V_{ds} ranging from 1.0 to 5.7V. At more than 2.5V V_{ds}, a high PAE of more than 40% was achieved. Even operated at a reduced V_{ds} of 1.2V, PAE of 29.2% was obtained.

These results indicate that the developed HJFET has great potential for W-CDMA cellular phone systems, which can be operated with one Li-ion battery cell.

[1] NTT Mobile Communication Network, Inc., NTT DoCoMo Brochure "W-CDMA", Nov. 1997.
[2] N. Iwata, *et al.*, 1996 GaAs IC Symp. Dig., pp. 119-122.
[3] K. Yamaguchi, *et al.*, 1997 APMC Proc., 1997, pp.1105-1108.

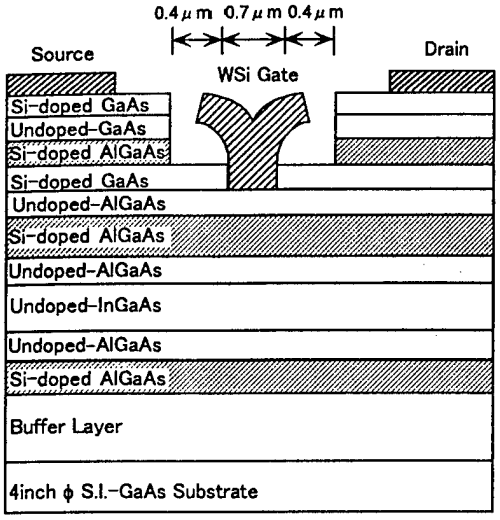

Fig.1 Cross section of the HJFET.

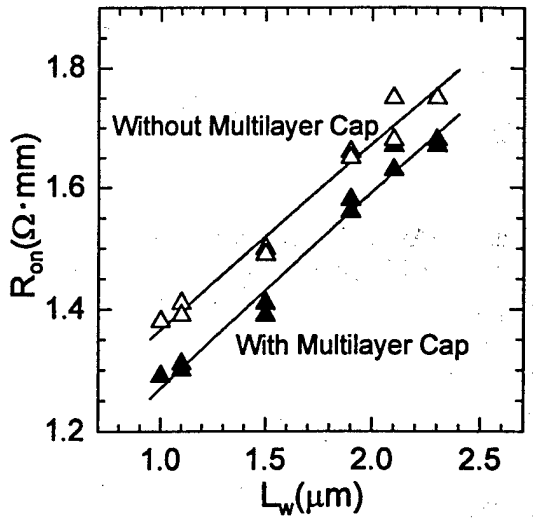

Fig.2 R_{on} vs. L_w for the fabricated HJFET.

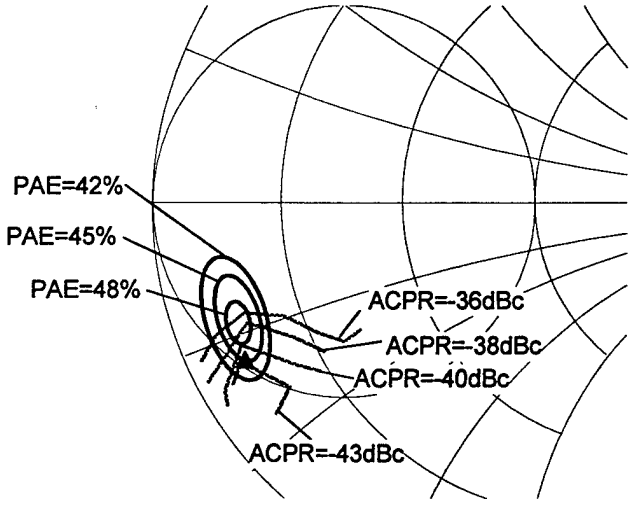

Fig.3 PAE and ACPR vs. Z_L at P_{out} =28dBm.

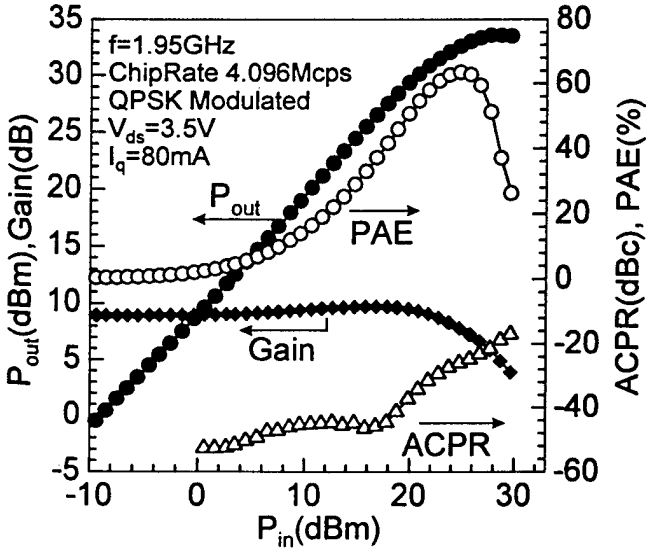

Fig.4 P_{out}, PAE, gain and ACPR vs. P_{in}.

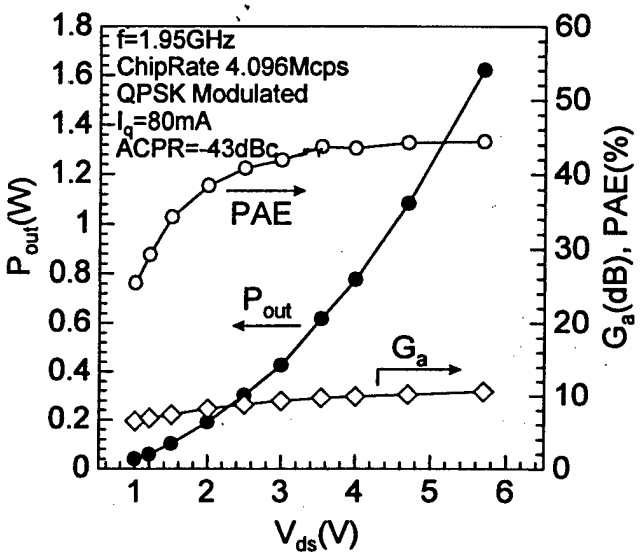

Fig.5 P_{out}, PAE and G_a vs. V_{ds} at ACPR=-43dBc.

Reliability Investigation of Heavily C-doped InGaP/GaAs HBTs Operated under a Very High Current-density Condition

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InGaP/GaAs heterojunction bipolar transistors (HBTs) have attracted considerable attention as devices for high-speed optical communication because of their superior reliability characteristics compared to AlGaAs/GaAs HBTs [1]. To fully utilize their excellent microwave performance, they should be operated with an emitter current density J_E at which the cutoff frequency and maximum oscillation frequency peak ($J_E \sim 2 \times 10^5$ A/cm^2 [2]). However, the J_E during bias testing in ref. [1] was one-third of this value (6×10^4 A/cm^2). To investigate degradation characteristics at $J_E = 2 \times 10^5$ A/cm^2, we have carried out bias testing of InGaP/GaAs HBTs at a base-emitter junction temperature T_j ranging from 230°C to 310°C. Although the base layer of the HBTs was heavily doped with C to 1×10^{20} cm^{-3}, a fairly long lifetime of 1.7×10^4 h at T_j = 125°C was extrapolated with an activation energy E_a of 1.1 eV. To our knowledge, this is the first reliability investigation of HBTs with a C concentration exceeding 5×10^{19} cm^{-3} operated with a J_E exceeding 6×10^4 A/cm^2.

A schematic illustration of the fabricated HBT is shown in Fig. 1. The epitaxial layers were grown by gas-source molecular beam epitaxy [2]. Triple emitter cap layers were used to reduce emitter resistance R_E: a 50-nm-thick InGaAs layer doped to 4×10^{19} cm^{-3}, a 50-nm-thick GaAs layer doped to 5×10^{18} cm^{-3}, and a 50-nm-thick InGaP layer doped to 8×10^{18} cm^{-3}. The InGaP emitter layer below the InGaP cap layer was also 50 nm thick and was doped to 1×10^{18} cm^{-3}. The GaAs base layer was 30 nm thick. The collector layer was 200-nm-thick undoped GaAs. A thick GaAs subcollector (800 nm, 5×10^{18} cm^{-3}) was used to reduce collector resistance. A non-self-aligned process was used to form the emitter (WSi), base (Au/Pt/Ti/Mo/Ti/Pt), and collector electrodes (Au/Ni/W/AuGe). The InGaP cap and emitter layers were left on the 1-μm-long extrinsic base as a surface passivation layer. We carried out bias testing of the HBTs, which had an emitter area S_E of 2×5 μm, at a substrate temperature T_s of 170°C, using a J_E of 2×10^5 A/cm^2 and a base-collector bias V_{BC} ranging from 0 to 2 V. The T_j was determined from the dependence of h_{FE} on the power consumption and T_s [3].

Figure 2 shows Gummel plots of the HBTs before and after a 30-h-long bias stress at V_{BC} of 0 V. We observed a forward V_{BE} shift of 4.8 mV for the collector current, which was probably due to debonding of H from neutral C-H pairs in the base, which is thought to occur during bias testing [4]. We also observed increases in R_E and I_B. The R_E, determined from the emitter current I_E vs. V_{BE} linear plots, was 12.7 Ω before the stress and 17.1 Ω after the stress. This R_E increase should be attributed to increased contact resistivity of the WSi on the InGaAs cap layer. The ideality factor for I_B after the stress was 1.8 when $V_{BE} \leqq 1.3$ V, which indicates that the increase in I_B is dominated by a generation-recombination process. This I_B increase degraded h_{FE} (Fig. 3). We defined the lifetime of the HBTs as the time taken for the peak h_{FE} (i.e., h_{FE} at $J_E = 5 \times 10^4$ A/cm^2) to decrease by 20%. The dependence of the lifetime on T_j is shown in Fig. 4. A fairly long lifetime of 1.7×10^4 h at T_j of 125°C was extrapolated with an E_a of 1.1 eV. We expect that an In doping technique [5] will further improve this lifetime.

In summary, we have found that InGaP/GaAs HBTs whose base layers were doped to 1×10^{20} cm^{-3} remain very stable even when they are operated with a J_E of 2×10^5 A/cm^2.

References
1) T. Takahashi et al., in *Tech. Dig. IEEE IEDM*, 1994, p. 194.
2) T. Oka et al., in *Abst. Topical Workshop on Heterostructure Microelectronics*, 1996, p. 76.
3) J. R. Waldrop et al., *IEEE Trans. Electron Devices*, vol. 39, p. 1248, 1992.
4) F. Ren et al., *Solid-State Electron.*, vol. 38, p. 1137, 1995.
5) H. Sugahara et al., in *Proc. GaAs IC Symp.*, 1993, p. 115.

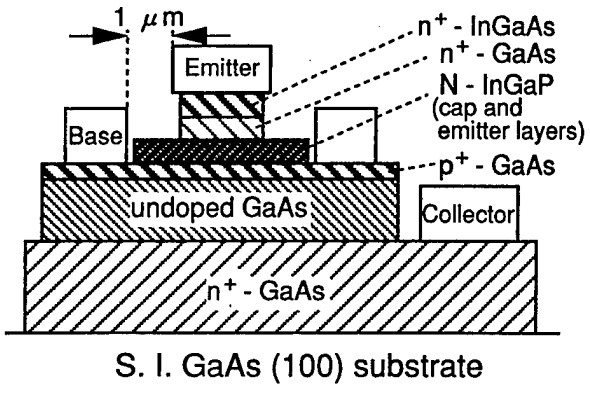

Fig. 1. Schematic illustration of a tested HBT. The spacing between the emitter and the base electrodes was 1 μm.

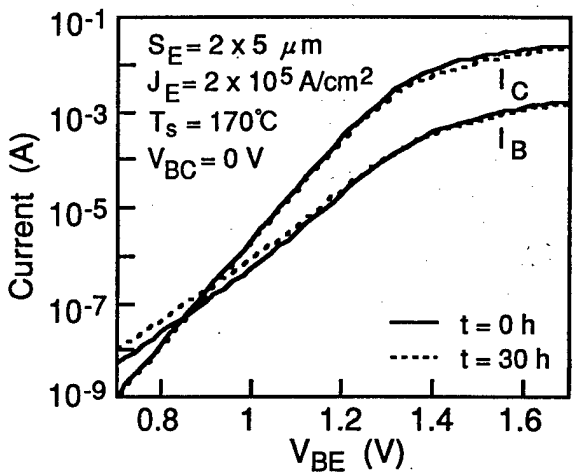

Fig. 2. Gummel plots of InGaP/GaAs HBTs before (solid lines) and after the 30-h-long bias testing (dotted lines).

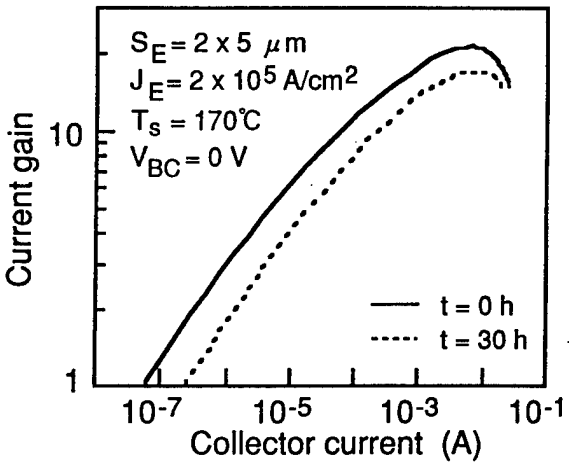

Fig. 3. Dependence of current gain on collector current of InGaP/GaAs HBTs before (solid lines) and after the 30-h-long bias testing (dotted lines).

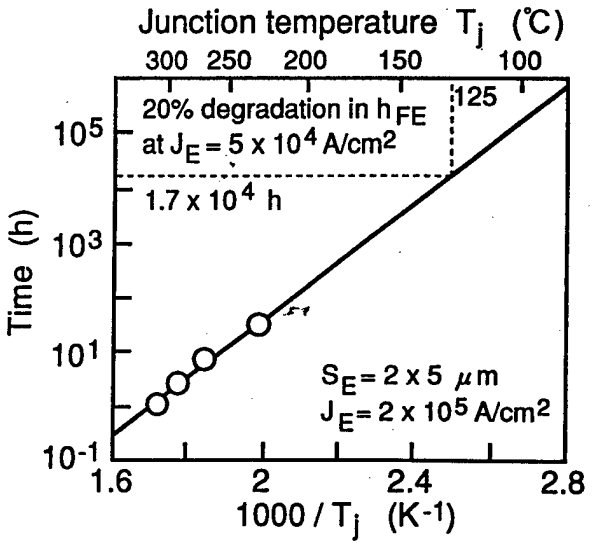

Fig. 4. Time vs. 1000 / junction temperature for 20% degradation in current gain at an emitter current density of 5 x 10^4 A/cm^2.

Comparison of Conventional and Thermally-Stable Cascode (TSC) AlGaAs/GaAs HBTs for Microwave Power Applications

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Thermal effects in AlGaAs/GaAs HBTs are an important issue for power applications. To control these effects, various approaches have been used in the past including ballast resistors and thermal-shunt structures [1]-[3]. More recently, a new Thermally-Stable Cascode HBT (TSC-HBT) design was developed, which not only provides an effective solution to the thermal runaway issue, but also can improve the robustness of high power HBTs under overstressed DC or RF bias conditions [4]. In this study, we compared the DC, small-signal, and large-signal performance characteristics of conventional common-emitter (CE) to TSC-HBT to provide a direct assessment of this new design approach.

In a TSC-HBT the part of the device (common-base stage) that provides power (and therefore gets hot) is physically separated from the part that regulates the current (common-emitter stage). Because the electrothermal feedback is effectively eliminated in this configuration, the collector current remains uniformly distributed across all parts of the CB stage. The net result is that a uniform temperature distribution is achieved at all DC and RF drive conditions without thermal instability. As the results in this paper will show, this increased thermal stability is possible without compromising the microwave performance of power HBT cells.

All devices studied here were fabricated using MOCVD-grown wafers with a self-aligned emitter-base process. A constant emitter geometry 2.5×20 μm^2 was used in all designs. The conventional CE HBT had four emitter fingers separated by 30μm. Identical cell layout approach was used in TSC-HBTs for both CE and CB stages. A virtually complete thermal isolation was provided between CE and CB stages by separating these cells by at least 100 μm. Thermal shunt structures were used for the CE stage to minimize temperature variation between emitter fingers and therefore to maintain a uniform collector current generation. The collector of each CE subcell was directly connected to the corresponding emitter of the CB subcell. No thermal shunt structures were used for the CB stage cell.

The negative slope of the collector current in the forward I_c-V_{ce} characteristics (*Figure 1*) of conventional devices indicate the strong influence of junction temperature on current gain. A similar effect was not observed with TSC-HBTs because the rise in temperature is confined mostly to the CB cell, whose current is controlled by CE cell located at a cooler temperature zone. A large-signal microwave device model including *self-heating* effects was employed to investigate the thermal characteristics for both devices. The *base-emitter* junction temperature increase was simulated and the results are shown in *Figure 2*. The TSC-HBT CE stage junction temperature was found to increase by ~ 20 C° at V_{ce} = 10V, while the temperature increase was ~ 60 C° for the conventional HBT at V_{ce} = 5V. These results prove the advantage of the TSC-HBT design to suppress electrothermal effects by maintaining a lower junction temperature increase at the CE .

The small-signal *S-parameters* of the conventional and TSC-HBT devices were measured and the results are shown in *figure 3*. The maximum available gain for TSC-HBT devices is ~13 dB higher than for conventional HBTs at lower frequencies. Above 10 GHz, the G_{max} dropped at different slopes (– 20dB/dec and – 40dB/dec for CE and TSC-HBT, respectively). The extrapolated results suggest similar f_{max} value of 92 GHz for both devices. On the other hand, $|h_{21}|^2$ is higher for TSC-HBTs in the measured frequency range (0.5- 25.5 GHz) leading to higher f_t .

On-wafer power characterization was performed at 8 GHz using a *load-pull* measurement system with electromechanical tuners. The devices were biased under the same conditions as above. The input and output impedance were optimized for maximum gain at P_{in} = 0 dBm. Under this input power level, the optimized gain was 18.47 dB and 25.4 dB for conventional and TSC-HBT devices respectively. In addition,

the corresponding P_{out} was 18.11dBm and 22.98 dBm; *PAE* was 25.4%, 53.4% for each device. The power handling capabilities were investigated by measuring 1dB gain compression characteristics of each device type. The measured power and gain characteristics are shown in *Figure 4* for the TSC-HBTs. As can be seen, this device can reach a gain of 32.9dB while producing P_{out} = 21.2 dBm. This result compares very favorably with conventional CE devices, which produced a maximum -1 dB gain of 18.5 dB and P_{out} = 18.5dBm. It is clear that the TSC-HBT devices perform considerably better than the conventional devices.

In summary, we have compared the DC, small-signal and large-signal power characteristics of conventional and TSC-HBTs and found that the TSC_HBT device provides a higher power handling capability than the conventional HBTs. The CB-stage in the TSC-HBTs not only leads to lower temperature increase but also provides additional power amplification stage. The net result is that TSC-HBTs are eminently more suitable for high frequency power applications than conventional CE HBTs.

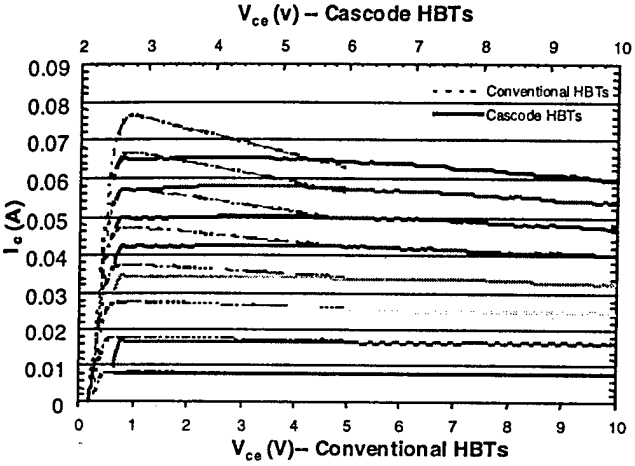

Figure 1. *Forward I_c/V_{ce} characteristics for conventional and cascode HBTs. I_b = 0.3, 0.6,.., 2.4 mA, V_{ce} = 0 – 5 V for conventional HBT and 2.5 – 10 V for cascode HBTs.*

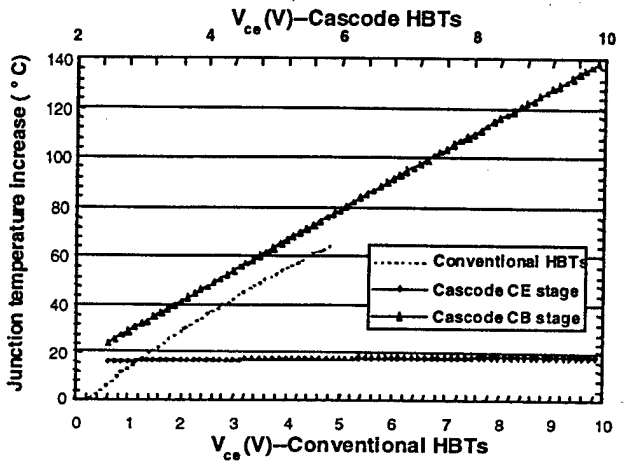

Figure 2. *Simulated junction temperature increase for conventional, cascode CE stage and CB stage HBTs. I_b = 2.4 mA, Vce = 0 – 5 V for conventional HBTs and 2.5 – 10 V for cascode HBTs.*

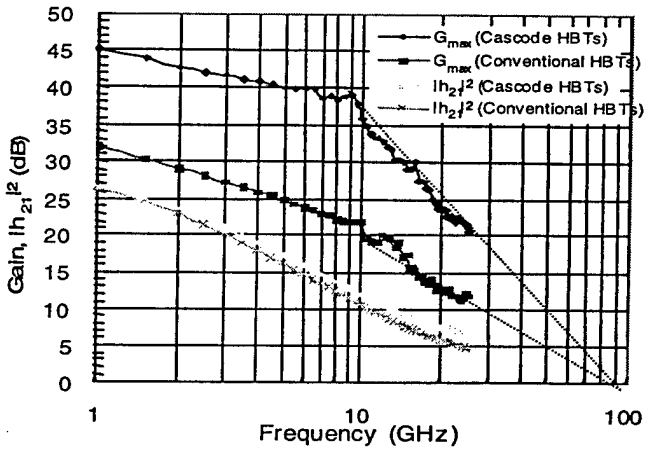

Figure 3. *G_{max} and $|h_{21}|^2$ for conventional and cascode HBTs. I_b = 2.4 mA, I_c = 65.06 mA, V_{ce} = 4V for conventional HBTs, I_b = 2.1 mA, V_{b2} = 2.5, Ic = 57.44 mA, V_{ce} = 7V for cascode HBTs.*

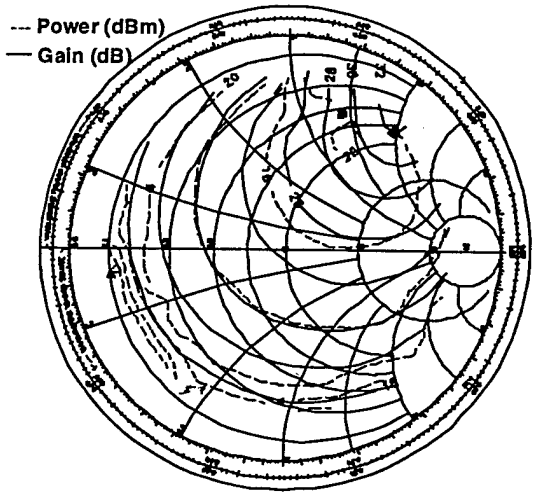

Figure 4. *One dB gain compressed on-wafer load pull measurement for cascode HBTs. Maximum Gain = 32.9 dB and P_{out} = 21.2 dBm.*

Acknowledgement: This work is supported by DARPA MAFET Thrust 2 Program, Contract No: N00014-95-C-6026.

[References]

[1] G. Gao, et al, *IEEE Trans. Electron Devices, Vol. 38, 1991, pp. 185-196.*
[2] W. Liu, et al, *IEEE Trans. Electron Devices, Vol. 41, 1994, pp. 1698-1707.*
[3] B. Bayraktaroglu et al, *IEEE Trans. Electron Devices Letter, Vol. 14, 1993, pp. 493- 495.*
[4] M. Salib and B. Bayraktaroglu, *IEEE MTT-S Int. Microwave Symp. Dig. 1997, pp. 897-899.*

InGaP HBT Technology for RF and Microwave Instrumentation

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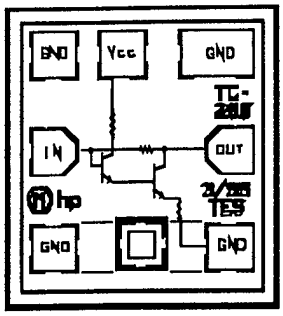
Heterojunction Bipolar Transistors have emerged as a competitive technology for wireless and communication markets. At Hewlett-Packard a major application for HBT technology is in RF and microwave instrumentation. For this application, HBTs offer an attractive complement to the existing 0.25 μm PHEMT technology. The higher power and gain density provided by HBTs leads to significantly smaller chip sizes and potentially lower cost per function. HBTs can achieve comparable F_t's to 0.25 μm PHEMTs with much larger (~ 1 μm CD's) and improved uniformity and control, enabling higher levels of integration and more functionality on a chip. In addition, the inherently lower 1/f noise is promising for low phase noise oscillators. Key instrumentation requirements include high linearity, broadband gain, low phase noise, moderate levels of integration for digital modulation and a high degree of reliability. HP's Microwave Technology Center (MWTC) has developed an InGaP emitter, HBT technology to address the instrumentation market.

The HBT process is based on MOCVD epitaxial wafers manufactured by Kopin Corp. Key features of the epitaxial structure include a 4000 Å collector drift, an 800 Å, C doped base, an InGaP emitter and a highly doped InGaAs contact layer. The process utilizes G-line stepper lithography that readily defines the minimum geometries, 2 x 2 μm emitters and 1 x 1 μm vias. Chlorine based RIE is used to define the emitter, emitter ledge, base, trench and collector contact areas. Non-alloyed TiPtAu contacts are used for the emitter and base while an alloyed Au/Ge/Ni contact is used for the collector. He implantation isolates passive and active devices. Device passivation is realized with PECVD Si_3N_4. Planarization and an intermetal dielectric layer are achieved with a 1 μm thick layer of Dupont's PI2555 polyimide. The HBTs are integrated with the standard MWTC passive component platform which includes 22 ohm per square thin film resistors, MIM capacitors with 1500 Å PECVD Si_3N_4, 2 μm thick TiPtAu interconnect metal and dry etched backside vias in 100 μm thick substrates. Because of the high performance requirements of the instrumentation applications the HBTs are operated at a relatively high current density of $6x10^4 A/cm^2$. Nominal values of key process monitors include: F_t = 62 GHz, F_{max} =67 GHz, β = 132 and BV_{ceo} = 8.4 V.

Several products have been developed to address the instrumentation market. A typical example is a broadband Darlington Feedback Amplifier that provides 9.5 dB gain from DC to 20 GHz, figure 1. This product is designed as a cascadable gain block which uses feedback to minimize sensitivity to process variations. It features 50 ohm input and output match, a 0.41 x 0.46 mm^2 chip size and 214 mW DC power dissipation. A simplified schematic/layout and a typical S_{21} versus frequency characteristic are diagrammed in figure 1. A second product example is a DC to 15 GHz Divide-by-8 Prescaler. On-chip pre and post-amplifiers have been incorporated in the design to improve input sensitivity and output signal swing. The chip layout and input sensitivity window are shown in figure 2. The chip operates over most of the frequency range with input powers between –20 and +20 dBm. The input sensitivity decreases to –10 to +5 dBm at 15 GHz. Relatively low phase noise, -153 dBc/Hz at 100kHz offset, is also achieved. The chip size is 1.33 x 0.44 mm^2.

Maintaining a high level of reliability is essential for components addressing instrumentation markets. To characterize the reliability of the InGaP emitter HBT process, several hundred Darlington amplifiers have been subjected to high temperature operating life (HTOL) stress tests for periods in excess of 3000 hours. In all cases, collector currents were held at the maximum use condition of $J_c = 6x10^4$ A/cm^2. Junction temperatures were varied between 303 and 363 °C. Typical values of mean time to failure (MTTF) extrapolated to T_j = 150 °C are 500,000 hours with activation energies, E_a, between 0.68 and 0.96 eV and sigmas of 0.6, see figure 3. The InGaP emitter results are significantly better than the results obtained with AlGaAs emitter devices made in the same process, MTTF(@ T_j=150 °C) = 50,000 hours, E_a = 0.5 eV. In both cases, the failure mode is sudden and dramatic increase in base current. In contrast to previous investigations [1,2] the results reported here indicate that activation energies can be similar for both AlGaAs and InGaP emitter materials. The similar activation energies suggest that the same failure mechanism dominates in both cases. As has been reported in the literature [1,3] the failure mode is consistent with a rapid increase in emitter-base recombination current potentially initiated by recombination enhanced defect formation.

[1] T. Takahashi et al., IEDM Tech. Digest, 1994, p. 191.
[2] C. Beaulieu et al., 1996 GaAs REL Workshop Proceedings, p. 11.
[3] T. Henderson et al., GaAs MANTECH, 1997, p 38.



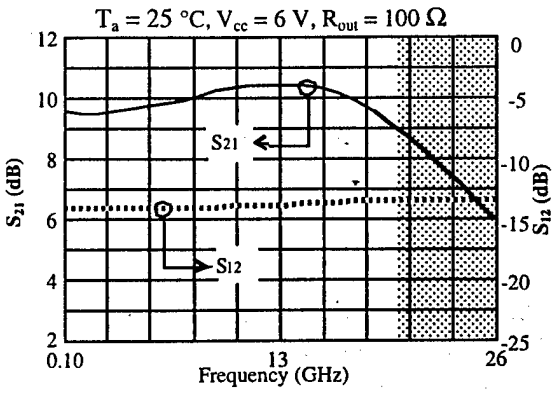
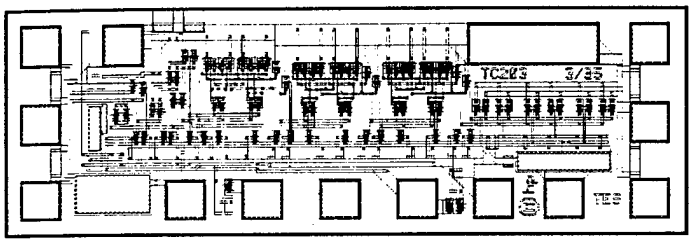


Figure 1. Darlington Feedback Amplifier, simplified schematic/layout and gain versus frequency.



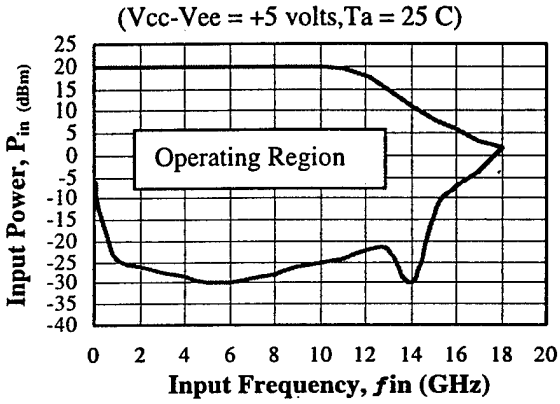


Figure 2. DC to 15 GHz Divide-by-8 Prescaler, chip-layout and input sensitivity curve.

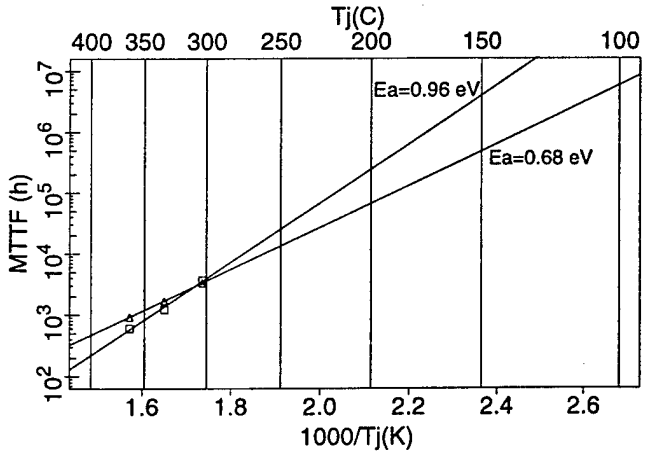


Figure 3. HTOL Arrehnius plot for InGaP emitter Darlington Amplifiers, $J_c = 6x10^4$ A/cm^2.

Passivation of InP-based HBTs

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In compound semiconductor HBTs the base-emitter surface is crucially important for good device performance. The difficulties arise because of the surface states and associated recombination centers that degrade the performance. The clearest evidence is in the dc Gummel plots. The ideality factors (n) for the base current are closer to 2 than the ideal case of n=1 when the surface recombination is large. This leads to crossing of the collector and base currents at low bias and bias (voltage or current) dependence of the dc gain. Most notorious in this respect are many examples in the literature for AlGaAs/GaAs HBTs. InP-based HBTs are cited to be better than GaAs-based devices because InGaAs has a lower surface recombination velocity than GaAs. Nevertheless poor Gummel plots can occur in InP-based HBTs, even for large-area devices - this when the rate of surface recombination is increased by putting an oxide on the InGaAs. We have studied various approaches to reducing the surface recombination on InP/InGaAs HBTs. We have found a surface treatment that works even under PECVD SiO_2 - a UV-ozone treatment that produces a sacrificial oxide that is then removed by HF. We have also found improvements with a thin InP ledge that avoids the InGaAs being exposed at all.

The HBTs were triple-mesa devices fabricated using wet-chemical etching using epitaxial layer structures described in Table 1. The major difference in the second layer design is that the InP emitter is 30 nm thick. In Fig. 1 we show the different cross-sectional structures of the devices studied, starting with the normal structure (N) with an exposed InGaAs base to devices with the thin InP emitter left intact and the contact to the base either through the InP itself, or through a via hole in the InP layer. The latter 2 structures are referred to as self-passivated and ledge-passivated devices respectively.

In Fig. 2 we show that passivation by sulfur or by UV-ozone improves the dc performance of an unpassivated device by reducing the base current at low bias. However these effects can degrade with time. Thus, while the chemical treatment of the interface is a viable strategy for improving the dc performance, the use of a ledge (part of the wide bandgap material composing the emitter stack) avoids the need to treat the exposed base surface. The difficulty is to ensure that the thin layer is fully depleted and does not provide a leakage path to the emitter. In Fig. 3 we show clearly how the thin InP emitter ledge is effective in reducing the current dependence of the gain. The ledge passivated device is an attractive solution for the passivation problem.

High frequency devices have to be covered with a dielectric such as SiO_2. An uncoated, unpassivated device can have its dc gain performance severely degraded by the deposition of a PECVD SiO_2 coating layer (Fig. 4). Although the originally exposed surface is protected by the SiO_2 , recombination at the interface increases the base current and decreases the gain, even for a large-area device. By treating the surface either with wet- and dry-etching prior to oxide deposition this degradation can be alleviated. We show this in Fig. 5 where the UV-ozone + HF treatment is shown to improve the dc gain of a high frequency device with a 5 x 10 μm^2 emitter. A further challenge is to apply the ledge- or self-passivation approach to high frequency devices, and to optimize the thickness of the InP emitter that is used for the ledge.

Layer	Material	Thickness (nm)	Doping (cm^{-3})
Cap	InGaAs	100	Si: $2x10^{19}$
	InP (InGaAs)	60 (70)	Si: $2x10^{19}$
Emitter	InP	90 (30)	Si: $3x10^{17}$
Set-back	InGaAs	10	-
Base	InGaAs	50	Be: $2x10^{19}$
Spacer	InGaAs	50	Si: $5x10^{15}$
p-Spacer Dipole	InGaAs	10	Be: $1x10^{18}$
n-Collector Dipole	InP	10	Si: $1x10^{18}$
Collector	InP	290	Si: $5x10^{15}$
Collector Contact	InGaAs	450	Si: $5x10^{18}$
Substrate	InP		Fe

Table 1. Epitaxial layer structures. Values in brackets are the differences for the second layer design. The wafers were grown by GS-MBE by Tutcore Ltd., Finland.

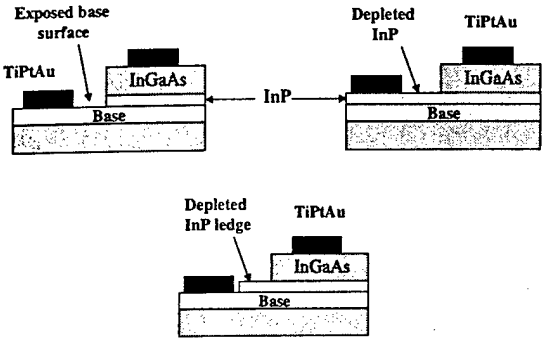

Fig. 1. Schematic cross section of the devices, showing different emitter-base mesa structures. The normal structure (N) has an exposed InGaAs base - other structures either have the base contact through a depleted InP layer (self passivated - SP) or onto the base though a via hole in the InP layer (ledge passivated - LP).

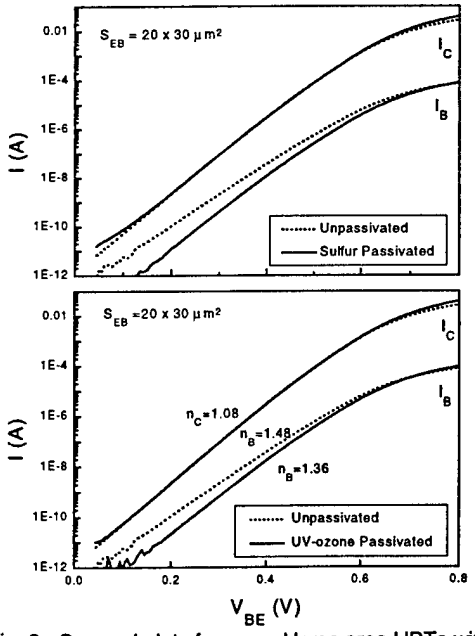

Fig. 2. Gummel plots for normal large area HBTs with and without the surface treatments indicated. There was no oxide coating on these devices.

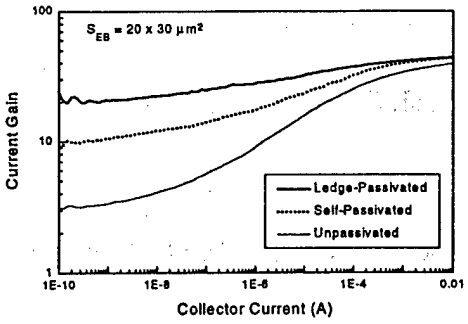

Fig. 3. DC current gain for large area HBTs with the self- or ledge-passivated structures (see Fig. 1). The second wafer design was used for these devices. There was no oxide coating.

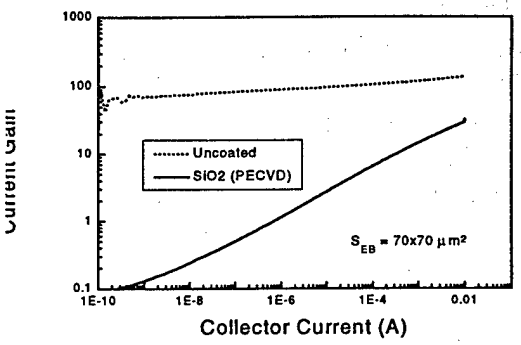

Fig. 4. DC current gain for a large area devices with or without a PECVD oxide coating layer. No passivation treatment was done before the oxide deposition.

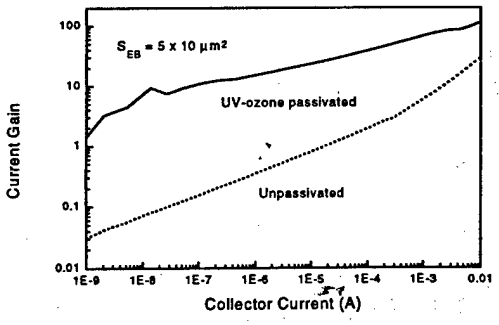

Fig. 5. DC current gain for small-area high frequency devices. Both devices were PECVD-oxide coated, the device with the higher gain had the UV-ozone + HF surface treatment prior to oxide deposition. The layer structure had the 150 nm thick InP emitter, as in Figs. 2 and 4.

GaN-based Electronic Devices.

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ABSTRACT

The electron peak velocity in GaN is triple of that for Si, its electron mobility is about twice as large as for Si, and its thermal conductivity is comparable to that of Si (see Fig.1). With an increase in the doping density, the electron mobility decreases more slowly than, for example, for GaAs. This allows us to obtain record values of the mobility-sheet carrier density products. The AlGaN/GaN material system is capable of supporting the sheet carrier densities of the two-dimensional electron gas up to $1.5x10^{13}$ cm-3 (up to $5x10^{13}$ cm^{-2} in doped channel structures), which is 5 to 20 times larger than in the AlGaAs/GaAs materials system [1]. GaN epitaxial layers can be grown on SiC, which allows us to combine superior transport properties of GaN with an exceptional thermal conductivity of SiC [1]. Very large piezoelectric constants of AlN and GaN can be used in piezoelectric [2] and pyroelectric [3] sensors and could be taken advantage of in designing conventional electronic devices for enhancing the sheet carrier concentration and reducing leakage current [4]. A recent analysis of hot electrons in GaN quantum wells [5] seems to imply that the breakdown field in such wells will be determined by the AlGaN cladding layers and not by the quantum well material. All this gives hope that electronic devices based on GaN will reach the same prominence as GaN-based blue and white light emitters. In this paper, we review recent progress on GaN electronic devices, including GaN-based Schottky diodes, *p-n* junctions, piezoelectric and pyroelectric sensors, detectors of microwave radiation [6], and field effect transistors with emphasis on the special device designs that can utilize superior physical properties of the GaN-based material system. An example of such a device is a Doped Channel Heterostructure Field Effect Transistor grown on SiC (Fig. 2).

References.

1. R. Gaska, J. W. Yang, A. Osinsky, M. A. Khan, M. S. Shur, IEDM-97 Technical Digest, pp. 565-568, December, 1997; R. Gaska, M. S. Shur, J. W. Yang, A. Osinsky, A. O. Orlov, G. L. Snider, in Proceedings of the International Conference on SiC and Related Compounds, vol. 2, p. 1445, Sweden (1998); R. Gaska, Q. Chen, J. Yang, A. Osinsky, M. Asif Khan, and Michael S. Shur, High Temperature Performance of AlGaN/GaN HFETs on SiC Substrates, IEEE Electron Device Letters, vol. 18, No. 10, pp.492-494, October 1997

2. A. Bykhovski, B. Gelmont, M. S. Shur, and A. Khan, J. Appl. Phys., vol. 77(4), 1616 (1995); R. Gaska, J. Yang, A. D. Bykhovski, Michael S. Shur, V. V. Kaminski, and S. M. Soloviov, Piezoresistive Effect in GaN-AlN-GaN Structures, Appl. Phys. Lett., vol. 71 (26), pp. 3817-3819 29 Dec. (1997)

3. A. D. Bykhovski, V. V. Kaminski, M. S. Shur, Q. C. Chen, M. A. Khan, Applied Physics Letters, 69(21), p. 3254-3256 (1996);
4. R. Gaska, J. W. Yang, A. Osinsky, A. D. Bykhovski, and Michael S. Shur, Appl. Phys. Lett., Applied Physics Letters **71**(25), 3673 (1997)
5. M. Dyakonov and M. S. Shur, unpublished
6. J. Q. Lu, M. S. Shur, R. Weikle, and M. I. Dyakonov, and M. A. Khan, in Proceedings of Sixteenth Biennial Conference on Advanced Concepts in High Speed Semiconductor Devices and Circuits, Ithaca, New York, Aug. 4-6 (1997), pp. 211-217

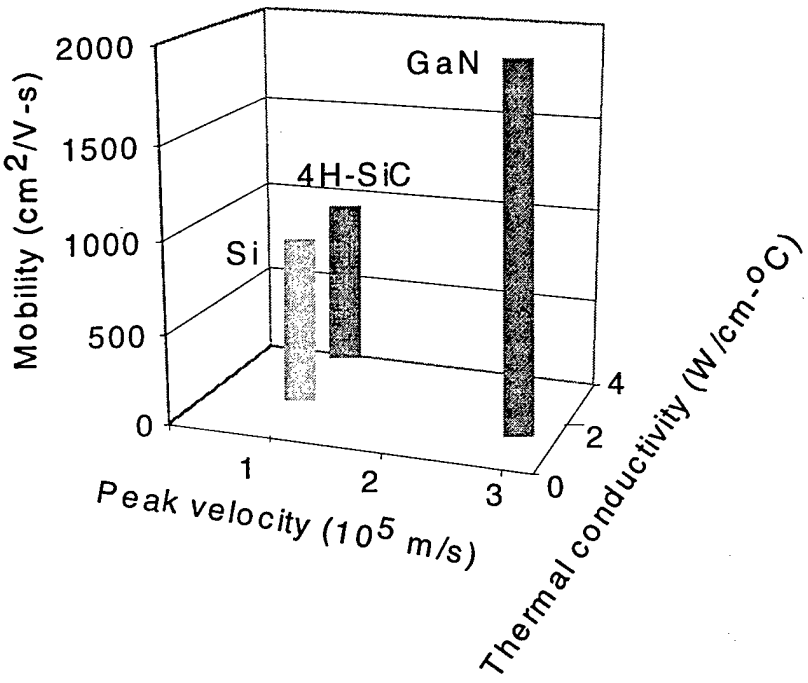

Fig. 1. Materials properties of Si, SiC, and GaN.

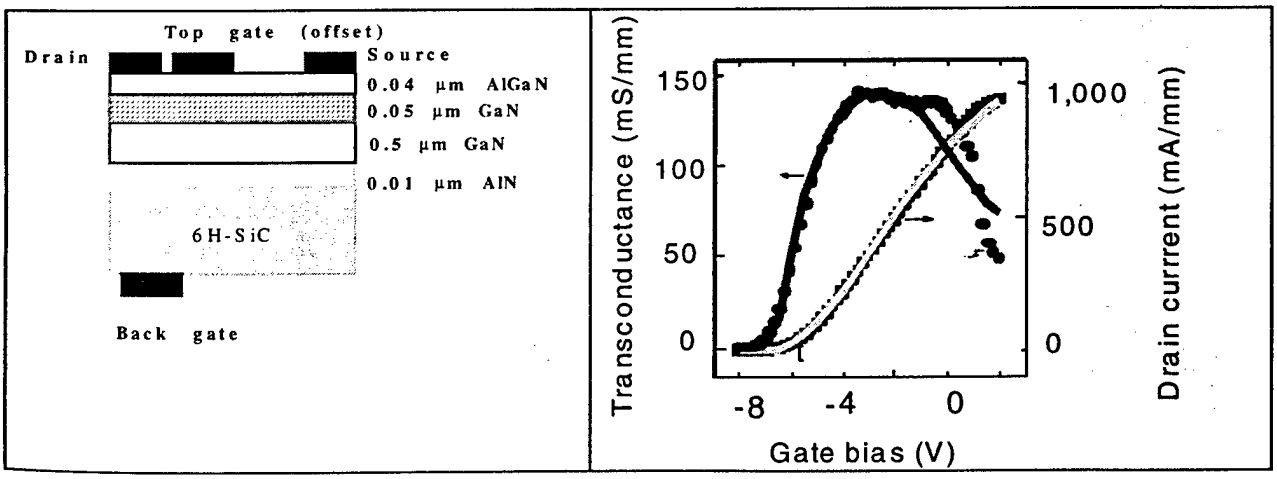

Fig. 2. Schematic structure and characteristics of AlGaN/GaN HFETs on SiC. [1]

TWHM, Japan, August 1998

Lateral Epitaxial Overgrowth (LEO) for Low Defect Density GaN on Sapphire

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The structural,optical and device (LEDs, and HEMTs) properties of GaN stripes prepared by lateral epitaxial overgrowth (LEO) are investigated using a combination of atomic force microscopy (AFM), transmission electron microscopy (TEM), high-resolution x-ray diffraction (HRXRD), time resolved photoluminescence spectroscopy (TRPL), and cathodoluminescence (CL). A large reduction in the leakage current (<1E-12A) is measured for both LEDs and HEMTs fabricated on LEO GaN is discovered. The LEO GaN was grown by low pressure MOCVD on 2 μm thick GaN/Al2O3 substrates covered with a SiO2 layer in which openings were etched. We observe that the stripe orientation, growth parameters (temperature, input V/III ratio), and pattern geometry all determine which facets are exposed during the LEO growth. The density of threading dislocations is reduced from 109-1010 cm-2 in bulk GaN to <105 cm-2 in the LEO GaN, as measured by AFM and TEM as shown in Figure 1 and 2..

The starting material consisted of 2 μm thick GaN grown by MOCVD on 2-inch diameter sapphire wafers using a standard two-step process [14]. Samples were coated with 200 nmthick SiO2 using PECVD and 5-10 μm wide stripes were patterned using standard UV photolithography and wet chemical etching. Following the results of Kapolnek et al. [5], thestripes were oriented in the <100> direction in order to yield a large lateral growth rate. The stripe spacing was varied to give 'fill factors' (ratio of open width to pattern period) of 0.1 to 0.5. The LEO GaN was grown at 1080°C using hydrogen as the carrier gas. The sample was heated to the growth temperature under NH3. The total pressure was set to 76 Torr andthe TMGa flow was 105 μmoles/min. Samples were characterized by scanning electron microscopy (SEM) using a JEOL 6300F field emission microscope operating at 5 KeV withoutany conductive coating applied to the sample surface. Surface topography was measured in tapping mode using a Digital Instruments Nanoscope III atomic force microscope (AFM).

We would like to acknowledge the program support of ONR (Colin Wood, Max Yoder) and AFOSR(Jerry Witt).

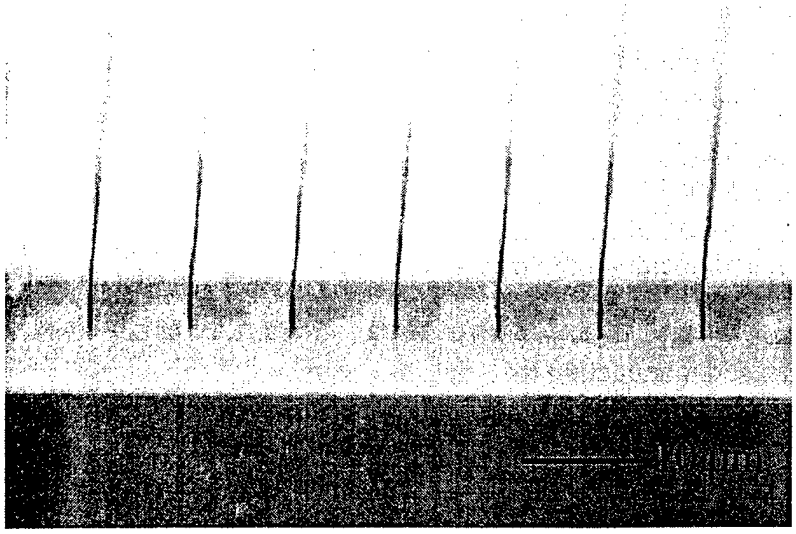

Fig 1.Lateral Epitaxially Overgrowth of GaN

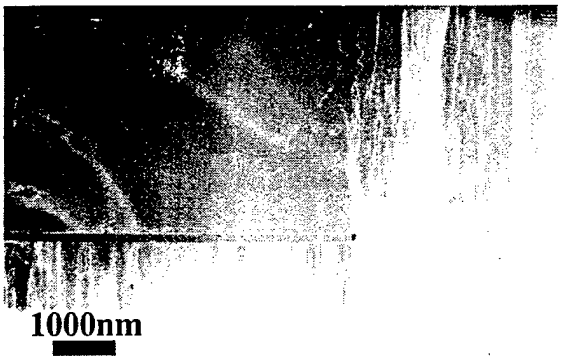

Fig 2 Cross-sectional TEM of LEO GaN diplaying large reduction of threading dislocation in lateral overgrown GaN region.

SiC and GaN Wide Bandgap Semiconductor Materials and Devices

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Wide bandgap semiconducting materials are promising candidates for high-power, high-temperature, microwave and optoelectronic devices because of their superior thermal and electrical properties in comparison to conventional semiconductors(Table I)[1]. SiC, for example, has an order of magnitude greater thermal conductivity and breakdown field strength, and a higher saturated electron drift velocity than GaAs. In the case of GaN, the direct bandgap makes highly efficient blue light emitting diodes(LEDs) and laser diodes possible. The lack of high-quality, large-area, and lattice matched substrates(in the case of GaN), combined with the difficulties in processing these materials due to their chemical, mechanical, and thermal stability, have hampered the development of wide-bandgap devices. In the case of 4H-SiC, up to two-inch diameter, device-quality, substrates are now commercially available. Although work has been done in molecular beam epitaxy [2,3] as well as in ion implantation [4] for device active layer formation, the most successful methods for SiC and GaN device active layer fabrication have been vapor phase techniques. SiC epitaxial layer background doping densities less than $1x10^{14}$ cm^{-2} and n and p-type intentional doping from $1x10^{15}$ cm^{-2} to over $1x10^{19}$ cm^{-2} have been reported [5]. In the case of GaN, the use of AlN buffer layers, SiC substrates, and lateral overgrowth [6] have dramatically reduced the ~10^{10} cm^{-2} dislocation density initially observed in layers grown on sapphire substrates.

Table I: Electronic and physical properties of Si, GaAs, 4H-SiC, and GaN

Property	Si	GaAs	4H-SiC	GaN
bandgap(eV)	1.12	1.43	3.25	3.4
breakdown field(MV/cm)	0.25	0.3	~3	~3
saturated electron velocity(10^7 cm/s)	1	2.0 (peak) 1.2 (sat)	2.0	2.5 (peak) 1.5 (sat)
electron mobility @ $N_d \sim 10^{16}$ cm^{-3} (cm^2/Vs)	1200	6500	800	900
thermal conductivity (W/cm K)	1.5	0.5	4.9	1.3 (on sapphire)
dielectric constant	11.8	12.8	9.7	9
Normalized Johnson figure of merit	1	7	360	560

As a result of these developments in wide bandgap materials and processes, SiC Metal Semiconductor Field Effect Transistors (MESFETs) with cut-off frequencies of 42 GHz and power densities as high as 3.3 W/mm at 10 GHz have been demonstrated (see figure 1)[7]. The power density is more than six times higher than that typically obtained with current GaAs MESFETs. SiC Static Induction Transistors (SITs) with 4 GHz cut-off frequencies have been developed from VHF through S-Band, exhibiting over four times the power density of silicon power transistors at

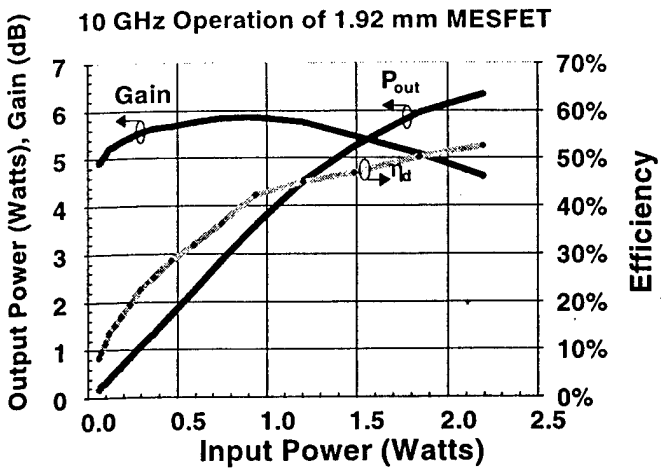

Figure 1. 4H-SiC, 0.5 μm gate-length MESFET with 6.2 W output power at X-Band.

S-band [8]. GaN/AlGaN Modulation Doped Field Effect Transistors (MODFETs) have demonstrated cut-off frequencies in excess of 97 GHz promising millimeter wave applications [9]. The recent demonstration of room-temperature, CW operation of blue laser diodes [10], only two years after the first demonstration of laser action in this materials system, is representative of the extremely rapid pace of development in the area of wide bandgap semiconductors. These and other wide bandgap materials, processing, and device developments will be presented.

Acknowledgements

This work was supported in part by the Department of the Air Force under contract F33615-92-C-5912 and F33615-95-C-5427 (Tom Kensky contact monitor).

References

1. H. Morkoç, S. Strite, G. B. Gao, M. E. Lin, B. Sverdlov, and M. Burns, J. Appl. Phys., 76, 1363 (1994).
2. T. Yoshinobu, M. Nakayama, H. Shiomi, T. Fuyuki and H. Matsunami, J. Crystal Growth, 99, 520 (1990).
3. L. B. Rowland, R. S. Kern, S. Tanaka and R. F. Davis, J. Mater. Res. 8, 2753 (1993).
4. M. Ghezzo, D. M. Brown, E. D. Downey, J. Kretchmer, W. Hennessy, D. L. Polla, and H. Bakhru, IEEE Electron Device Lett., 10, 639 (1992).
5. A. A. Burk, Jr. And L. B. Rowland, phys. stat. sol. (b) 202, 263 (1997).
6. Ok-Hyun Nam, M. D. Bremser, Tsvetanka S. Zheleva, and R. F. Davis, Appl. Phys. Lett. 71 (18), 2638 (1997).
7. S. Sriram, G. Augustine, A. A. Burk, Jr., R. C. Glass, H. M. Hobgood, P. A. Orphanos, L. B. Rowland, R. R. Siergiej, T. J. Smith, C. D. Brandt, M. C. Driver, and R. H. Hopkins, IEEE Electron Device Lett., EDL-17, 369 (1996).
8. R. R. Siergiej, S. Sriram, R. C. Clarke, A. K. Agarwal, C. D. Brandt, A. A. Burk, Jr., T. J. Smith, A Morse, and P. A. Orphanos, Tech. Digest Int. Conf. SiC and Rel. Mat'95, (Kyoto Japan 1995), p. 321.
9. M. A. Khan, Q. Chen, M. S. Shur, B.T. Dermott, J. A. Higgins, J. Burm, W. J. Schaff, and L. F. Eastman, IEEE Electron Device Lett., EDL-17, 584 (1996).
10. S.Nakamura, M.Senoh, S.Nagahama, N.Iwasa, T.Yamada, T.Matsushita, H.Kiyoko, Y.Sugimoto, T.Kozaki, H.Umemoto, M.Sano, and K.Chocho, Appl. Phys. Lett., 72(2), 211(1998).

Diamond field effect transistors using hydrogen-terminated surfaces

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Although only p-type is available for device application in diamond, mobility and saturated carrier velocity of holes are comparable to those of electrons in Si. Compared with other semiconductors, the figures of merit of diamond in the field of integrated circuits, high power, and high frequency devices are extremely high because of its high thermal conductivity, breakdown voltage, and low dielectric constant. In order to utilize these merits, low density of surface states, ohmic contacts, and shallow acceptor levels are inevitable. These requirements have been achieved on surface p-type conductive layers of hydrogen-terminated (H-terminated) diamond surfaces without additional dopants [1].

Using the surface conductive layer as p-type surface channel, both metal-semiconductor (MES) and metal-oxide-semiconductor (MOS) field effect transistors (FETs) have been realized (Fig. 1). The transconductances of these devices with gate length of several μm exceeds 10 mS/mm (Fig. 2) [2]. These values are comparable to those of silicon (Si) n-channel MOSFETs in the same gate length and are more than 10 times higher than those of other types of diamond FETs using boron-doped p-type channel with oxygen-terminated surfaces, where ohmic contacts are very difficult to obtain and Fermi level pinning states are also found. On H-terminated surfaces, however, Schottky barrier heights depends on metal electronegativity indicating the low density of pinning states [1]. Both enhancement (E) and depletion (D) mode MESFETs have been obtained using different kind of gate metals. E/D type inverters, NAND (Fig. 3), and NOR circuits have been realized [1,2]. The breakdown voltage of the MESFETs in a planar structure is about 200 V resulting in the power handling capability of 2 W/mm [3]. MOSFETs using the H-terminated surface channel operate up to 300°C in air without device passivation [4]. The same type of FETs on heteroepitaxial diamond surface exhibits almost the same performance as those on homoepitaxial surfaces [5]. Even on the polycrystalline surfaces, maximum transconductance of more than 1 mS/mm in several μm gate can be obtained exhibiting the feasibility of polycrystalline diamond wafers for sensors using FETs.

From the device simulation, the experimental device operation can be reproduced in shallow in-depth distribution of acceptors such as less than 1 nm in diffusion length or even monolayer surface acceptor. It indicates that the

surface acceptors due to H-termination might be responsible for the p-type conduction of H-terminated surfaces. Using the device parameters obtained from the experimental FET operation, the transconductance of 1 μm gate MESFET with small source-gate distance exhibits 150 mS/mm which exceeds those of Si n-MOSFETs in the same device scale. From the device scaling rule, the obtained shallow junction depth is small enough to operate much smaller FETs with less than 50 nm in gate length.

[1] H. Kawarada, Surf. Sci. Rep. 26, 207 (1996).
[2] A. Hokazono and H.Kawarada, Jpn. J. Appl. Phys. A 36, 7133 (1997).
[3] P. Gluche, A. Aleksov, A. Vescan, W. Ebert, and E. Kohn, IEEE Electron Dev. Lett. EDL-**18**, 547 (1997).
[4] H. Kawarada, Oyo Buturi, 67, 128 (1998) (in Japanese).
[5] H. Kawarada, C.Wild, N. Herres, P. Koidl, Y. Mizuochi, A. Hokazono and H. Nagasawa, Appl. Phys. Lett. 72 (1998) (April 13 issue).

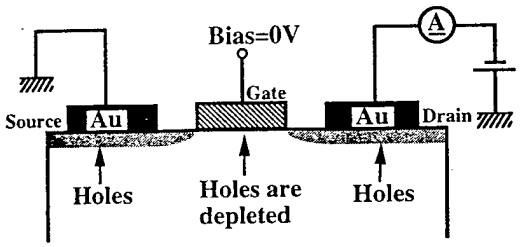


Fig. 1. Schematic cross section of enhancement mode MESFET using H-terminated diamond surface. The gate metal has low electronegativity.

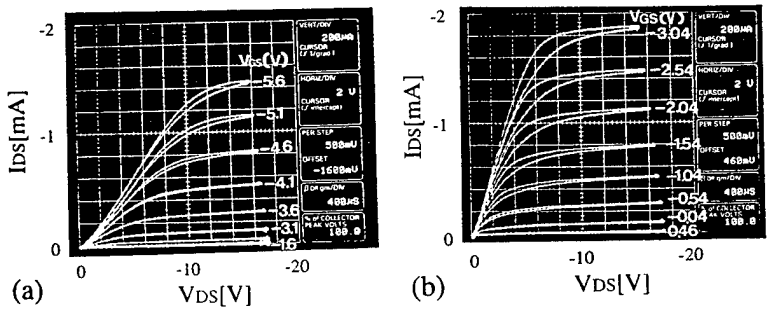
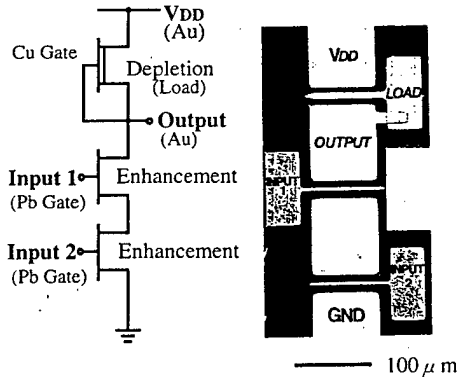


Fig. 2. I_{DS}-V_{DS} characteristics of diamond MESFETs of (a) enhancement and (b) depletion modes with Al and Cr gates, respectively.



(a) circuit schematic of NAND (b) NAND circuit

Fig. 3. Circuit schematic and optical micrograph of diamond E/D-type NAND circuit.

GaN Microwave HEMTs

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(The work was supported by US Army-SMDC/BMDO, ONR and Hughes Electronics.)

Progress in GaN based high-electron-mobility-transistors (HEMTs) has been enormous. Both $Al_{0.17}Ga_{0.83}N$/GaN HEMTs[1] and $Al_{0.14}Ga_{0.86}N$/GaN DC-HFETs[2] showed a power density of 1.7 W/mm at X band. This was boosted to 2.6 W/mm at 10 GHz with 0.7-μm gate devices, and to > 3 W/mm at 18 GHz with 0.25-μm gate devices, by employing high Al-content AlGaN layers[3,4]. However, these devices still showed fairly low power-added-efficiencies (PAE's) of 15 % ~ 28 %. This is identified as a result of the trapping effect directly related to the material quality, as also pointed out by Binari et al[5]. Also, for practical applications, large gate-periphery devices are yet to be developed, where thermal management posts a challenge for devices grown on sapphire substrates due to the poor thermal conductivity of sapphire. In this presentation, we report both improved device efficiencies through emphasis on material quality and high power operation of large-gate-periphery devices with thermal management by flip-chip bonding.

The devices under study were grown on C-plane sapphire substrates, starting with 2-μm insulating GaN followed by 200 Å modulation doped $Al_{0.5}Ga_{0.5}N$ barrier layer. The growth was by metal-organic-chemical-vapor-deposition (MOCVD) and the system parameters were optimized for low defect densities.

0.25-μm gate devices were fabricated by electron beam lithography. Although their DC characteristics were similar to previous non-optimized ones, these devices exhibited substantial increase in PAE due to the improved large-signal gain. Figure 1 shows the CW power performance at 8 GHz for an $Al_{0.5}Ga_{0.5}N$/GaN HEMT with gate dimensions of 0.25 μm x 150 μm. The peak PAE is 46 % with a power density of 2.8 W/mm. The saturated power density is 3.2 W/mm with a slightly lower PAE of 44 %. This combination of efficiency and power density is state-of-the-art for any high band-gap FET. It is noted that although optimized with recent technology, the GaN crystal under study is far from perfect. Performance will continue to improve with further advances in material quality.

Large gate-periphery devices were also fabricated and were flip-chip bonded on AlN substrates for effective heat sinking. These devices have a gate-length of 1 μm and exhibited substantial power gain at 4 GHz as seen in figure 2 and 3. The 1-mm-wide devices showed a small-signal gain of 12.5 dB, peak PAE 37.3 % and saturated output power of 33.26 dBm, or 2.1 W. The 2-mm-wide devices produced a higher output power of 35.0 dBm, or 3.2 W, with a peak PAE of 30 %.

In summary, reduction in defect density of GaN-based HEMTs has led to increased PAE's of 44 ~ 46 % with power densities of 2.8 ~ 3.2 W/mm at 8 GHz. Thermal management by flip-chip bounding on AlN carrier has resulted in GaN-HEMTs-on-sapphire with 3.2 W output power.

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[1] Y.-F. Wu, B.P. Keller, S. Keller, N.X. Nguyen, M. Le, C. Nguyen, T.J. Jenkins, L.T. Kehias, S.P. Denbarrs and U.K. Mishra, "Short-channel AlGaN/GaN MODFET's with 50-GHz f_t and 1.7-W/mm output power at 10 GHz", *IEEE Electron Device Lett.*, vol. 18, pp. 438-440, Sept. 1997.

[2] Q. Chen, J.W. Yang, R. Gaska, M. A. Khan, M.S. Shur, G.J. Sullivan, A.L. Sailor, J.A. Higgings, A.T. Ping and Adesida, "High-Power microwave 0.25-μm gate doped-channel GaN/AlGaN heterostructure field effect transistor", *IEEE Electron Device Lett.*, vol. 19, pp. 44-46, February, 1998.

[3] Y.-F. Wu, B.P. Keller, P. Fini, S. Keller, T.J. Jenkins, L.T. Kehias, S.P. Denbarrs and U.K. Mishra, "High Al-content AlGaN/GaN MODFETs for ultra-high performance", *IEEE Electron Device Lett.*, vol. 19, pp. 50-53, Feb., 1998.

[4] Y.-F. Wu, B.P. Keller, P. Fini, J. Pusl, M. Le, N.X. Nguyen, C. Nguyen, D. Widman, S. Keller, S.P. Denbaars, and U.K. Mishra, "Short-Channel $Al_{0.5}Ga_{0.5}N$/GaN MODFETs with power density > 3 W/mm at 18 GHz", *Electronics Letters, no. 20, vol. 33, pp. 1742-1743, Sept. 25, 1997.*

[5] S.C Binari, H.B. Dierich, W. Kruppa, G. Kelner, N.S. Saks, A. Edwards, J.M. Redwing, A.E. Wicknden, D.D. Koleske, "GaN-based Electronic Device for High-power, High-Speed, and High-Temperature Applications", *the Second International Conference on Nitride Semiconductors*, Oct. 27-31, Tokushima, Japan.

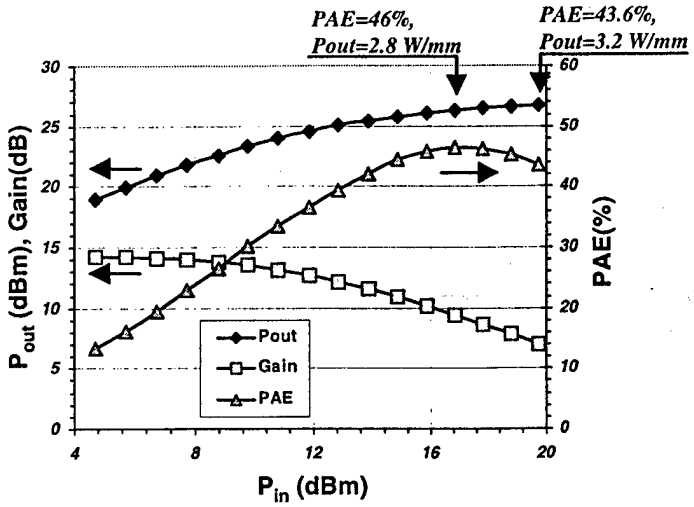

Fig. 1. Power performance of a 150-μm-wide AlGaN/GaN HEMT (L_g=0.25μm, f=8GHz)

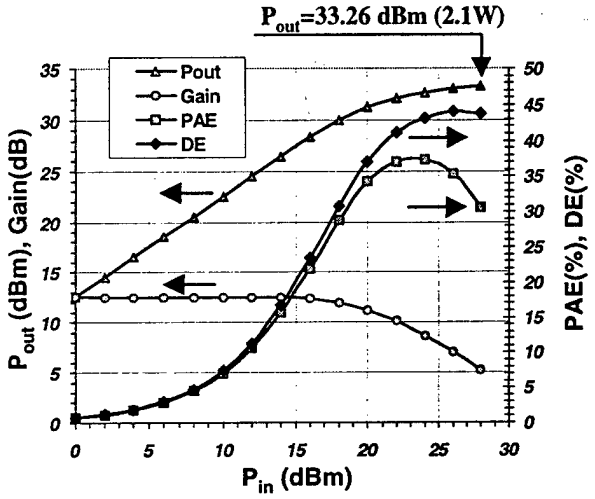

Fig. 2 Power performance of a 1mm-wide AlGaN/GaN HEMT (L_g=1μm, f=4GHz)

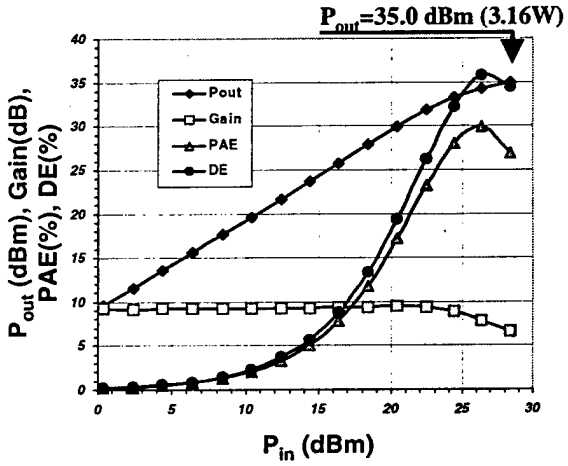

Fig.3 Power performance of a 2mm-wide AlGaN/GaN HEMT (L_g=1μm, f=4GHz)

GaN MODFET Microwave Power Technology for Future Generation Radar & Communications Systems

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The recent rapid progress in GaN MODFET technology provides clear convincing evidence that it has the potential to revolutionize the field of microwave power electronics. As a result, this swiftly evolving technology will likely have a dramatic impact on a wide range of systems such as future generation radar and satellite communications systems. In order to better understand the role that GaN MODFET technology will play in such systems, a comparison of the performance state-of-the-art of a range of microwave power technologies will be reviewed. The relative advantages and limitations of each technology will be discussed in relation to system needs.

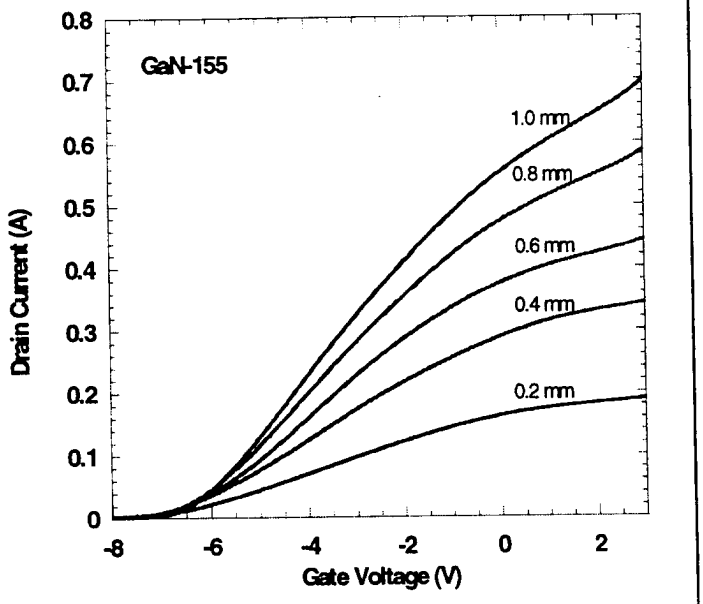

Figure 1. Transfer characteristics of GaN MODFETs with gate peripheries ranging from 0.2 mm to 1 mm at V_{DS} = 10V.

In particular, GaN MODFET microwave power technology has two fundamental advantages over the GaAs PHEMT technology, which is currently being used in many such systems. First, GaN MODFETs exhibit microwave power densities that are higher by a factor of 5X or larger. As a result, GaN MODFETs are capable of producing several times the microwave output power for a given device size (i.e., gate periphery) or High Power Amplifier (HPA) circuit footprint. The dramatically higher power density also allows one to trade-off device power and device size, resulting in higher GaN MODFET yield, and thus lower cost, as well as improved device impedance matching. A second, and just as important, advantage of GaN MODFET technology is the capability of these devices to operate effectively and reliably at higher temperatures. This is a direct result of intrinsic GaN materials properties (e.g., large bandgap), plus the higher materials growth and processing temperatures used for these devices.

Recent advances in HRL's development of MBE-grown GaN MODFET power technology will be reviewed. MBE-grown 0.25 μm gate GaN MODFETs have been shown to exhibit less than 5% variation in maximum drain current density (I_{dmax}) from the center to the edge of a 2 inch sapphire substrate wafer. This represents a major improvement in the uniformity of GaN devices compared with that from MOCVD-grown devices. MBE GaN MODFETs with gate peripheries from 0.2 mm of up to 1 mm have been fabricated and have undergone DC and RF characterization. Thick air bridge heat-spreader technology was utilized in the fabrication of these larger gate periphery devices. Figure 1 shows that the drain current scales well with increasing gate periphery.

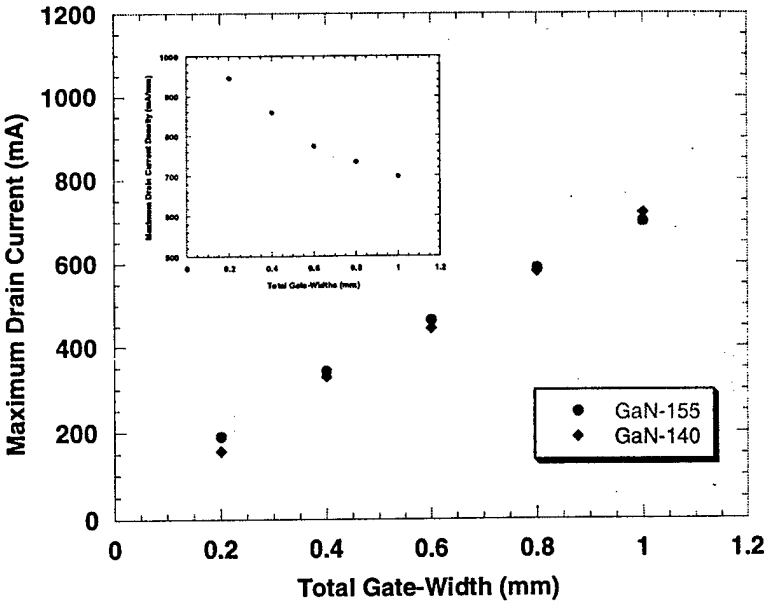

Figure 2. Dependence of GaN MODFET maximum drain current and current density (See Inset) on gate periphery at V_{DS} = 10 V for two different wafers.

As can be seen in Figure 2, the maximum drain current in these GaN MODFET devices scales almost linearly with gate periphery up to a maximum drain current of 750 mA for 1 mm of gate periphery GaN device. There is, however, some roll-off in the maximum drain current density (I_{dmax}) with increasing gate periphery as shown in the inset in Figure 2 which may be associated with thermal effects. S-parameter measurements of the RF performance of these GaN devices were also carried out as a function of gate periphery are shown in Figure 3. The short circuit current gain (f_T) of these GaN devices remained approximately constant, varying between 23 GHz to 26 GHz as the gate periphery increased from 0.2 mm up to 1 mm. The extrapolated maximum oscillation frequency (f_{max}), on the other hand, decreased significantly with increasing gate periphery. This latter effect may be associated with increasing parasitic source inductance for the wider GaN MODFETs.

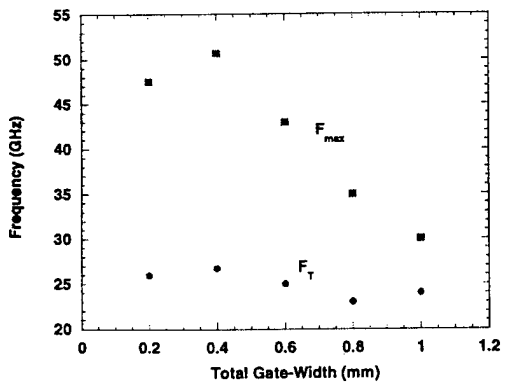

Figure 3. Cut-off frequencies extrapolated from S-parameter measurements for devices of varying gate peripheries.

This work has been supported in part by Dr. Elliot Brown & Dr. Gerald Witt under the MAFET-Thrust III program.

Progress Towards Ultra-Wideband AlGaN/GaN MMICs

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The potential of the wide bandgap, Nitride-based, semiconductors (GaN, AlN, and AlGaN) for the realization of high power, high frequency transistors has been well documented (1-3). This potential is due to the advantageous materials properties summarized in Table I along with the existence of the AlGaN/GaN heterostructure (4,5). The later allows modulation doping to form a high mobility two dimensional electron gas (2DEG) and, more importantly, the formation of piezoelectronically induced sheet carriers. The piezoelectric effect is at least three times stronger in these materials than in GaAs (see values for e_{31} and e_{33} in Table I) and contributes to the realization of high sheet electron densities (up to $5x10^{13}$ cm^{-2} is predicted for an AlN/GaN interface) in AlGaN/GaN HEMTs (6,7). These material properties enable the impressive DC and microwave device results achieved for AlGaN/GaN power field effect transistors summarized in Table II.

Table I: Summary of key material parameters for AlGaAs/GaAs, 4H SiC, and AlGaN/GaN (after Refs 3-5)

Metric	AlGaAs/GaAs	4H SiC	AlGaN/GaN
Maximum sheet electron density (cm^{-2})	$2\text{-}3x10^{12}$	na	$1\text{-}5x10^{13}$
Breakdown field (V/cm) ($x10^5$)	4	20	33
2 Dimensional Electron Mobility (cm^2/V s)	8500	na	2000
Saturated electron velocity ($x10^7$ cm/s)	1.0	2.0	2.2
Thermal conductivity (W/cm K)	0.53	4.9	1.3
Piezoelectric coefficient (C/m^2) e_{31}	0.093		-0.36
e_{33}	-0.185	0.2	1.0

Table II: Summary of key device parameters for AlGaAs/GaAs, 4H SiC, and AlGaN/GaN power field effect transistors.

Metric	AlGaAs/GaAs	4H SiC	AlGaN/GaN
Typical gate/drain breakdown (V)	~20	>100	>100
I_{DSS} (mA/mm)†	500	400	> 1000
Gate turn-on voltage at mA/mm (V)	~1	> 1	> 1
F_t (GHz)†	~150	10	30

F_{max} (GHz)†	> 150	20	100
Power density at 10 GHz (W/mm)	1.2	2.5(demonstrated) 4.0 (predicted)	2.8 (demonstrated) 8-12 (predicted)
Total power at 10 GHz (W)	1	10	4

† results for a gate length of ~0.25 μm

The material and device parameters discussed above enable new approaches to wide bandwidth power amplifiers. First, since the characteristic impedance of the AlGaN/GaN transistors is roughly three times that of a similar size AlGaAs/GaAs device, impedance matching and power combining is simpler. Second, the factor of three increase in thermal conductivity and the factor of eight increase in dielectric breakdown strength for AlGaN/GaN compared to AlGaAs/GaAs enables high-efficiency, class B, push/pull amplifier architectures. Class B high power amplifier designs are not practical with AlGaAs/GaAs transistors since the thermal and dielectric limits are comparable. Third, the higher power density capability of AlGaN/GaN allows narrower transistor fingers (smaller W_g) for the same power level thereby reducing C_{GS} since C_{GS} is proportional to W_g. Reducing C_{GS} allows larger bandwidth since

$$f_{high} = \frac{1}{2\pi Z_o C_{GS}} \qquad (1)$$

where Z_o is the characteristic load impedance.

The improved transistor performance described above will significantly improve the bandwidth of amplifiers incorporating them, however, to realize still larger bandwidths, new circuit approaches are also required. While traditional matching networks are effective at single frequencies, distributed approaches or traveling wave designs will be needed to achieve multi-octave bandwidths. Furthermore, the application of analog circuit design approaches to microwave circuits will enable conversion of f_t-limited lumped element circuits to f_{max}-limited distributed designs. Details of potential circuit approaches will be given at the workshop.

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References

1. B. J. Baliga, IEEE Electron Device Lett., **10**, 455 (1989).
2. T. P. Chow and R. Tyagi, IEEE Trans. Elec. Dev. **41**, 1481 (1994).
3. R. J. Trew, M. W. Shin, and V. Gatto, Solid State Electronics, **41**, 1561 (1997).
4. M. N. Yoder, IEEE Trans. Elec. Dev, **43**, 1633 (1996).
5. T. P. Chow, N. Ramungul, and M. Ghezzo, Materials Research Society, symposium E, Fall 1997, Boston MA (in press).
6. A. D. Bykhovski, B. L. Gelmont, and M. S. Shur, J. Appl. Phys., **81**, 6332 (1997).
7. P. M. Asbeck, E. T. Yu, S. S. Lau, G. J. Sullivan, J. Van Hove, and J. Redwing, Electronic Letts., **33**, 1230 (1997).

Optimization of Schottky Gate Formation Process for n-Channel GaN MESFETs

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The GaN-based material system is of great interest, not only for recently reported high-efficiency blue/green LEDs and LDs, but also for realization of devices for high temperature electronics and high power microwave electronics [1]. Development of a stable Schottky gate contact with high Schottky barrier height (SBH) and low leakage current is crucial for realization of the GaN-based electronic devices such as MESFETs, HFETs, HEMT, etc. However, little is known about electronic properties of metal/GaN systems.

In this paper, an attempt was made to optimize the formation process of Schottky gates for n-channel GaN MESFETs. The electronic properties of Schottky contacts to n-GaN prepared by vacuum deposition and electrochemical deposition were systematically investigated by I-V, C-V and XPS methods.

Figure 1 (a) shows the MESFET structure under consideration. **Figure 1 (b)** shows the sample structure for Schottky contact characterization. Si-doped GaN layers ($n=5x10^{16}$-$1x10^{17}$ cm^{-3}) grown on sapphire substrates by MBE were used. A series of high and low workfunction metals (Pt, Au, Ag and Sn) was deposited onto n-GaN surfaces by a conventional vacuum deposition process and a novel *in-situ* electrochemical deposition process [2,3]. Just prior to vacuum deposition, surfaces were treated in either HF- or NH_4OH-based solutions. The electrochemical process consisted of the controlled anodic etching of the GaN surface followed by *in-situ* metal deposition in the same electrolyte, resulting in formation of oxide- and stress-free Schottky interfaces [2,3].

Figures 2-4 show the typical I-V characteristics of the Schottky contacts to n-GaN formed by a conventional vacuum deposition process after various surface treatments. For the diodes treated only in organic solvent, high n-values and poor linearity of I-V curve were obtained. XPS results clearly showed that large amounts of oxide components remained on this surface, indicating the presence of an interfacial oxide layer. Significant decrease of oxide components was observed after surface treatments in $HF:HCl:H_2O=1:5:5$ solution for 1min and in NH_4OH solution for 15min. However, I-V characteristics of the Schottky diodes fabricated after these treatments are very different as shown in **Figs.3 and 4**. Almost all of the diodes exhibited ohmic-like characteristics after treatment in HF/HCl solution, while relatively lower n-values and good linearity of I-V curve were realized on the diodes treated in NH_4OH solution.

The XPS integrated intensity ratios of Ga3*d* to N1*s* obtained from the as-treated surfaces and the Ag/GaN and Au/GaN interfaces are summarized in **Fig.5**. For the samples treated in the NH_4OH solution, the intensity ratio is almost the same before and after metal deposition. On the other hand, the intensity ratio was drastically changed after metal deposition in HF/HCl treated diodes, clearly indicating that an interfacial reaction took place during metal deposition. This appears to be responsible for the ohmic-like I-V characteristics.

Figure 6 shows the I-V characteristics of the Sn- and Pt-Schottky contacts formed by the *in-situ* electrochemical process. Strongly metal-workfunction dependent I-V behavior was clearly observed. This seems to be due to the extremely low processing energy (several 100meV) which realizes stress- and disorder-free Schottky interface [2,3] on GaN.

Thus, the electronic properties of GaN Schottky contacts strongly depend on the interface formation process. The electrochemical deposition of Pt and the vacuum deposition of Au with NH_4OH-based treatment processes seem to be promising for formation of high-SBH Schottky gates for GaN MESFETs which are currently under fabrication and characterization.

[1] B.J. Trew, M.W. Shin and V. Gatto: TWHM'96, Solid-State Electron. **41**, 1561(1997).
[2] H. Hasegawa et al: J. Vac. Sci. Technol. **15**, 1227(1997).
[3] H. Hasegawa: TWHM'96, Solid-State Electron. **41**, 1441(1997).

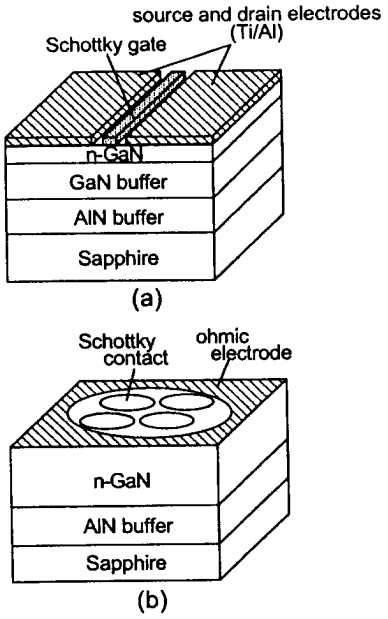

Fig.1 Schematic illustrations of (a) a GaN MESFET structue and (b) GaN Schottky diodes.

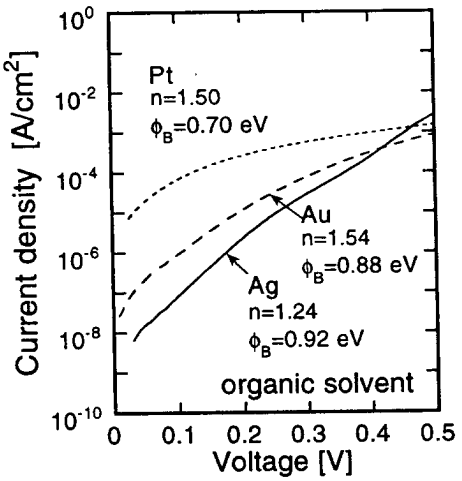

Fig.2 I-V characteristics of n-GaN Schottky contacts formed by vacuum deposition with organic solvent treatment.

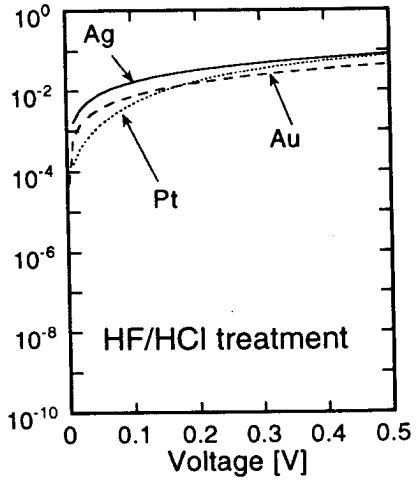

Fig.3 I-V characteristics of n-GaN Schottky contacts formed by vacuum deposition

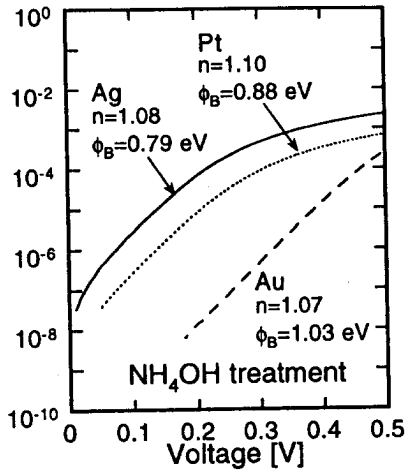

Fig.4 I-V characteristics of n-GaN Schottky contacts formed by vacuum deposition with NH_4OH treatment.

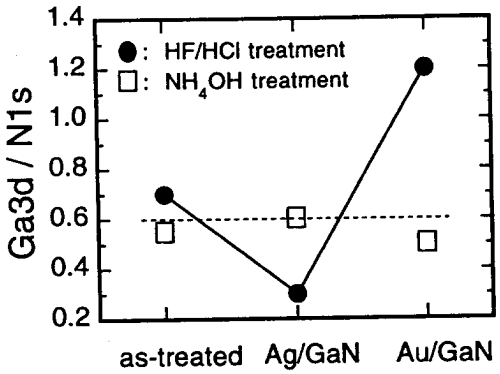

Fig.5 Change in integrated XPS intensity ratio of Ga3d to N1s before and after metal depostion.

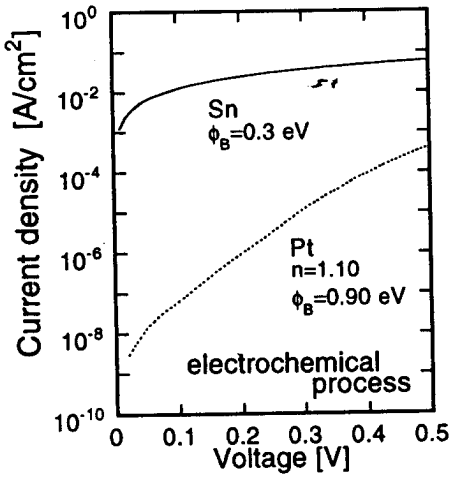

Fig.6 I-V characteristics of n-GaN Schottky contacts formed by the in-situ electrocehmical deposition.

Novel Bipolar Technologies and Their Circuit Applications

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Applications for heterojunction bipolar transistors (HBT) include microwave analog-digital conversion, microwave direct digital frequency synthesis, and high-capacity fiber-optic transmission. High circuit bandwidths are desirable; in $\Delta-\Sigma$ analog-digital converters and oversampled digital-analog converters, increased clock frequencies lead to increased signal/noise ratios, hence an HBT logic family capable of 100 + GHz clock rates would permit significant advances in the performance of signal conversion ICs. Future optical transmission systems will require multiplexers, PLL's, and decision circuits with ~100 GHz clock rates.

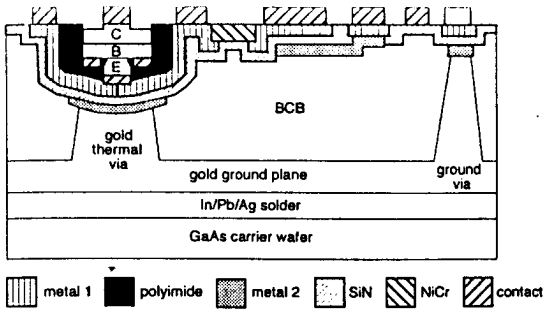
To permit clock rates exceeding 100 GHz, the transistor current gain (f_τ) and power gain (f_{max}) cutoff frequencies must be several hundred GHz. The interconnects must have small inductance and capacitance per unit length, and the wire lengths, hence transistor spacings must be small. Given that fast HBTs operate at ~10^5 A/cm^2 current density, efficient heat sinking is then essential.

Using a substrate transfer process, HBTs can be fabricated with narrow emitter and collector stripes aligned on opposing sides of the base epitaxial layer. The base-collector time constant ($R_{bb}C_{cb}$) becomes proportional to the process minimum feature size, and f_{max} increases rapidly with scaling. The substrate transfer process provides microstrip interconnects on a low-ε (2.7) Benzocyclobutene substrate, and a ground plane for low wiring ground-return inductance. Heat-sinking is provided by electroplated gold thermal vias.

Devices with submicron emitter and collector dimensions have obtained f_{max} as high as 500 GHz. Devices with ~0.6 μm emitter widths, 0.8 μm collector widths, and strong base bandgap grading exhibit 215 GHz f_τ and > 400 GHz f_{max}. Scaling to ~0.1 μm should result in f_{max} approaching 1 THz. ICs demonstrated in the technology include 48 GHz static frequency dividers, DC-50 GHz feedback amplifiers, 5-80 GHz distributed amplifiers, and DC-50 GHz differential AGC / limiting amplifiers.

UCSB work supported by the ONR under grants N00014-95-1-0688 and N00014-98-1-0068, and by the AFOSR under grant F4962096-1-0019. JPL work peformed at the Center for Space Microelectronics Technology, JPL, Caltech, and sponsored by the NASA office of Space Science

[1] Q. Lee, et. al, IEEE Electron Device Letters, Vol. 19, No. 3, March 1998
[2] B. Agarwal et. al, IEEE MTT-S symposium, June, Baltimore.
[3] R. Pullela et. al. , IEEE InP Conference, Tsukuba, Japan, May 1998



. 1: Transferred-Substrate HBT technology

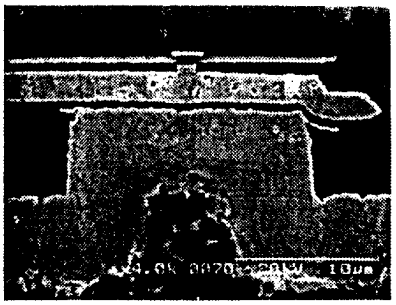
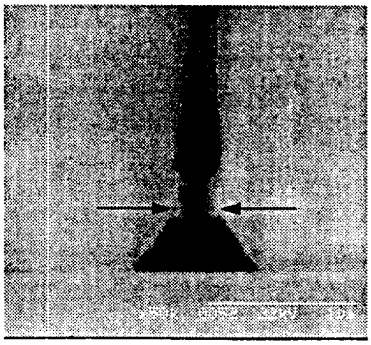


Fig. 2: Cross-section of transferred-substrate HBT



g. 3: 0.15 μm emitter-base junction. (structure cleaved cross-sections, omits base Ohmic ntacts & collector)

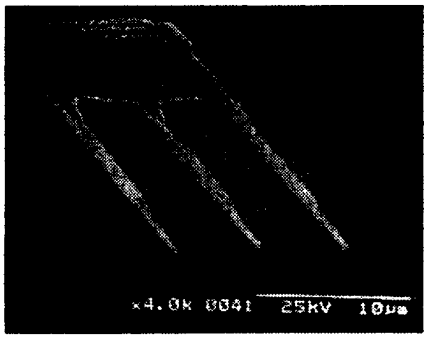
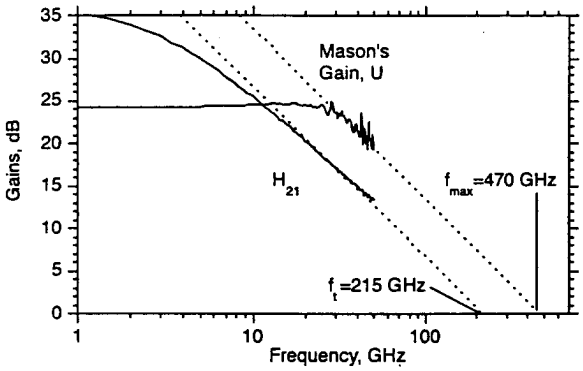


Fig. 4: Collector view of triple-finger HBT with 0.4 μm x 29 μm collector stripes and 0.2 μm x 25 μm emitter stripes.



g. 5: DC-50 GHz gains of device with 0.6 μm 25 μm emitter, 1.8 μm x 29 μm collector and T base bandgap grading

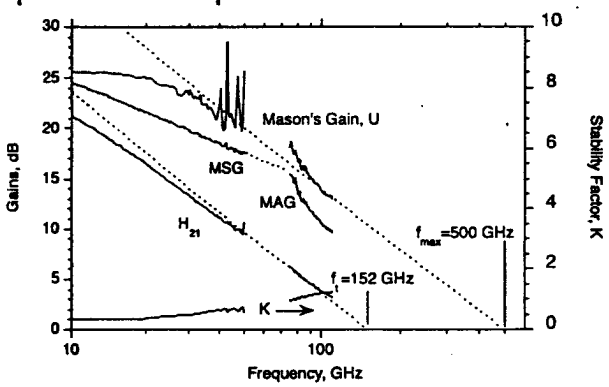
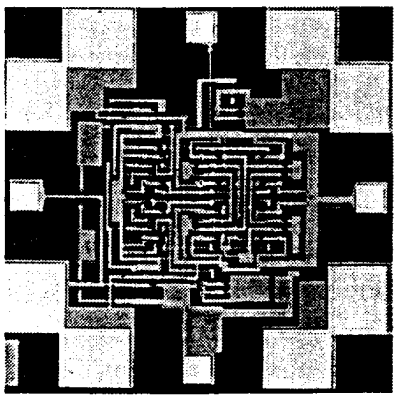
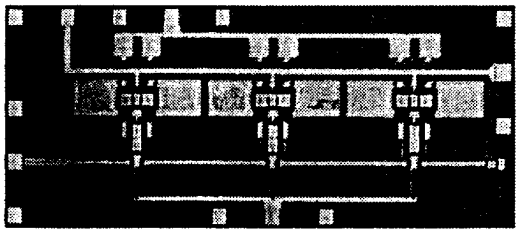
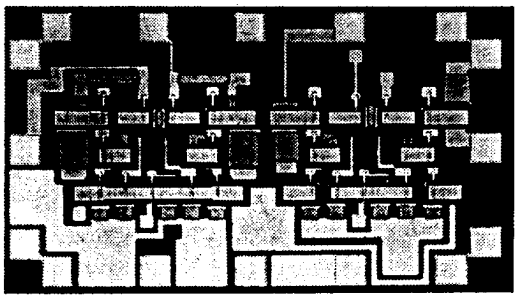


Fig. 6: W-band gains of device with 0.4 μm x 25 μm emitter and 1.0 μm x 29 μm collector







g. 7: Transferred-substrate HBT ICs: 48 GHz L static frequency divider (left), 5-80 GHz tributed amplifier (top right) and DC-50 GHz ferential AGC/limiting amplifier (bottom right).

SiGe Heterostructure CMOS Circuits and Applications

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Abstract

The Si-SiGe heterostructure system is attracting considerable interest because of its ability to enhance the performance of the three principal Si integrated circuit (IC) technologies - bipolar, BiCMOS and CMOS. When incorporated in the device active region, the parameters which can be significantly influenced are device speed, power dissipation, supply voltage and noise performance. Other applications of SiGe in MOS devices which are currently under consideration include the suppression of parasitic bipolar action in short channel MOS using "reverse" heterojunctions and the use of poly-crystalline SiGe in place of poly-Si as a gate material to improve threshold voltage control and subthreshold leakage.

With SiGe heterojunction bipolar devices now established in viable IC technologies (including integration with conventional CMOS), particularly in wireless systems operating up to 1.9 GHz, this paper concentrates on the key issue - appraising the potential for Si-SiGe to impact at the active channel level on the dominant microelectronics IC technology, CMOS. What are the real benefits, windows of opportunity and product markets for SiGe heterojunction CMOS (HCMOS)?

The intense industrially-led activity on deep submicron CMOS (channel lengths (L) $\leq$ 0.1μm) is demonstrating a real potential for CMOS to reach well into the GHz regime and for use in RF front and back ends, but the process demands are formidable. Although the intricacies of carrier transport across channels containing high lateral and vertical fields have yet to be fully unravelled, prototype device results and simulation work throughout the deep submicron regime - and even down at the 50 nm gate-length level - reveal two pervading factors - *the p-channel MOSFET remains the significantly inferior device* in terms of current drive and performance at high frequency and the *low field carrier mobility* remains a crucial transport parameter influencing device performance. These observations define and motivate two areas of activity by the SiGe fraternity, firstly to symmetrise p- and n-channel performance in CMOS and secondly to push n- and p-channel device performance well beyond current levels enabling industrially-relevant (i.e. factor of 2) improvements in general CMOS speed and allowing Si technology to comfortably access existing and future wireless markets.

This paper will address the key issue of how Si-$Si_{1-x}Ge_x$ heterostructures can be used to achieve the required improvements in hole and electron transport. Even now, hole transport at the Si-SiO_2 interface remains something of an enigma, but the modifications to the band structure and scattering processes facilitated by modifying the vertical device architecture with relatively low concentrations ($\leq$ 50%) of Ge and the associated compressive strain should allow hole transport to match that of electrons. Such enhancement should be achievable through the addition of one very thin SiGe layer, which if produced by epitaxy, would otherwise leave the device structurally sound.

The more ambitious goal of driving up n-channel performance requires tensile-strained Si. Matching p-channel performance might then be obtained in the Si-channel or in a strained channel of high Ge content (not excluding pure Ge). Here, a relaxed strain-tuning SiGe "virtual substrate" needs to be formed on the Si substrate prior to the formation of the active channels. For such a procedure even to be considered by MOS fabrication engineers the virtual substrate naturally should have no detrimental influences on device performance or reliability, be able to withstand subsequent processing and be economic to produce. Mobilities up to x5 those seen at the bulk-Si/SiO_2 interface have already been demonstrated.

The majority of SiGe FET device activity has to date been on modulation doped Schottky barrier-gated structures (MODFETs)- and may be regarded as a precursor to HMOS device work. N-channels in tensile strained Si layers - requiring a virtual substrate with a terminating composition of x = 0.3-0.4 have shown the most dramatic enhancements at 300K for dc and microwave frequencies. Mobilities approaching 3000 $cm^2\ V^{-1}s^{-1}$ for electron sheet densities of 3 x 10^{12} cm^{-2}, g_m values up to 500 $mSmm^{-1}$ and f_T and f_{max} values of 60 GHz and 100 GHz (L = 0.15μm), respectively, have been obtained - indicative of at least a factor of 2 improvement in performance compared to the Si control devices. Comparable virtual substrated p-channel devices also have given similarly impressive results with mobilities up to 1050 $cm^2\ V^{-1}s^{-1}$ at carrier sheet densities of 3 x 10^{12} cm^{-2} for an x = 0.8 channel on an x = 0.3 virtual substrate, with g_m = 258 $mSmm^{-1}$, f_T = 70 GHz and f_{max} = 55 GHz for a similar structure having a gate length of 0.1μm. Pure Ge channels on virtual substrates gave particularly high hole mobility values (1800 $cm^2\ V^{-1}s^{-1}$) with further improvements expected. Depletion and enhancement mode MODFETs can be made and digital and analogue MODFET circuits are being investigated. Only limited work on virtual substrated MOS devices has been reported but there is now substantial activity in this area and data are eagerly awaited.

Much more work has been carried out on fully pseudomorphic Si/SiGe/Si MOS p-channel devices, aimed at symmeterising p- and n-channel performance with minimal disruption to conventional processing. MOS SiGe p-channel devices in the range x = 0.2-0.5 have been produced but somewhat surprisingly researchers have struggled to achieve the required performance enhancements. Very recently however, significant strides have been made.

Some critical issues remain. These concern a knowledge of the precise enhancement levels obtainable in deep sub-micron technologies, the maintenance of acceptable operational characteristics with Ge incorporated, the design and processing route for circuits involving virtual substrates, the manufacturability and reliability of ICs containing regions with high Ge concentrations and associated strain and the economics of SiGe processing.

This talk will include the latest data on mobility and device and circuit performance relating to HCMOS, described how near the SiGe research community is to producing answers to the pertinent questions and concerns regarding SiGe HCMOS and will consider when will be the likely date of judgement.

Power Amplification using NPN and PNP InP HBTs and Application to Push-Pull Circuits

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Wireless communication systems require power amplifiers with high linearity, high power-adde efficiency (PAE), and high power-handling capability. HBTs offer this capability, and AlGaAs/GaA devices have already been introduced in wireless systems. Another promising device approach is InP-base HBTs, which have demonstrated very good high-frequency performance and have been implemented i various integrated circuits for electronic and optoelectronic applications. Their power capability i promising, with power levels up to 1.4 mW/μm^2 reported by the authors using NPN single HBT designs Further enhancement is possible by means of double heterojunction designs, and a power density o 3.6 mW/μm^2 with PAE of 54% at 9 GHz has been reported with the latter approach from Hughes Researc Labs. InP/InGaAs HBTs are consequently of interest for power amplification.

InP-based HBTs offer several advantages over GaAs-based HBTs in satisfying the requirements o wireless communications. In general, the improved frequency performance of InP-based HBTs produce higher gain at high frequencies. The lower contact and sheet resistances of the emitter cap and subcollecto layers, along with the smaller offset voltage (0.2 V vs. 0.4 V), reduces the saturation voltage of InP-base HBTs and allows the use of low-voltage batteries. Since InP has ten times smaller surface recombinatio velocity than GaAs, the current gain is more uniform with bias, which should produce better amplifie linearity. Less surface recombination also increases the gain of large power HBTs with many emitter finger (large total periphery), and it also allows for very small HBTs for digital applications. Finally, the highe thermal conductance of the InP substrate (0.7 W/cm-K, versus 0.5 for GaAs) allows for more powe dissipation in any given HBT design. InP-based single HBTs do suffer from low breakdown voltages typically around 2 to 7 V. This limitation can be overcome in double HBTs with InP collectors. A additional benefit of double HBTs is that the offset voltage is reduced to almost 0 V.

This paper addresses another method to improve power performance by developing a PNP HB technology and combining the PNP HBTs with NPN HBTs in a push-pull amplifier scheme that allow improvement in linearity characteristics. Complementary push-pull amplifiers have several advantages ove single-transistor power amplifiers, and they are much simpler to design than NPN-only push-pull amplifiers Since the output voltage swing is generated across two transistors in the push-pull amplifier, approximatel twice the output voltage is possible. In addition, push-pull amplifiers can produce linear output in Class A or Class B, which can have efficiencies as high as 78%. To achieve the same linearity, single transisto amplifiers must use Class A, with efficiency limited to 50%. InP-based HBTs offer an additional advanta for push-pull operation: the turn-on voltage V_{BE} is approximately 0.75 V, versus 1.4 V for GaAs-base HBTs. In Class B amplifiers, the smaller turn-on voltage reduces the crossover distortion. In Class A amplifiers, the smaller turn-on voltage reduces the power consumed in the level-shifting diodes.

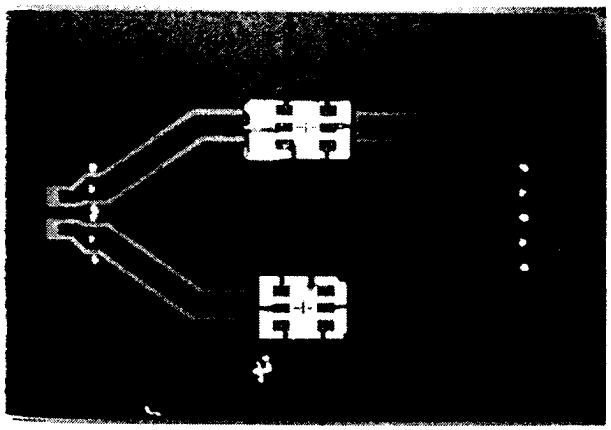
Unlike NPN HBTs, PNP HBTs have attracted much less attention, and little is known about thei characteristics, especially under large-signal conditions. The PNP HBTs studied here had a uniformly dope 500-Å base doped at 5×10^{18} cm^{-3}. A self-aligned technology was used for fabrication and Ti/Pt/Au wa employed for base metalization. Devices with 5×10-μm^2 emitter fingers showed ideality factors n_B and n equal to 1.60 and 1.00, respectively. Their maximum gain at J_C = 34 kA/cm^2 and V_{CE} = 4.0 V was greate than 30 while their breakdown was 5.6 V. A study of the high frequency characteristics of the device demonstrated f_T and f_{max} of 11 GHz and 31 GHz, respectively. This exceeds the best-reported f_{max} of 22 GH for InAlAs/InGaAs PNP HBTs. The devices were characterized using load pull techniques at 10 GHz an

demonstrated a small-signal gain of 10 dB, peak power-added-efficiency of 24%, and maximum output power density of 0.49 mW/μm^2. These characteristics are very similar to NPN InP-based HBTs fabricated with the same technology, which had slightly higher gain (+1dB) and efficiency (+5%) but produced less power than the PNP HBTs (-3dBm). Further studies indicated that output power scaled linearly with the number of emitter fingers up to 10 fingers, which was the largest HBT measured. The microwave gain was constant up to 4 emitter fingers, and the gain degraded by 3 dB when the number of emitter fingers was increased to 10. Finally, common-base HBTs provided 3 to 6 dB more gain than similarly biased common-emitter HBTs, which resulted in 5% higher efficiency.

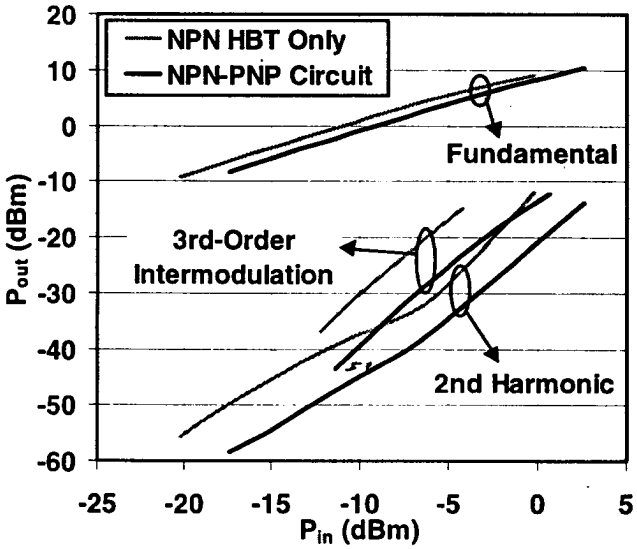
A push-pull amplifier was studied using the fabricated NPN and PNP HBTs. While for single HBTs Class B operation shows better efficiency but worse linearity, push-pull amplifiers can combine these two features and maintain therefore high linearity and efficiency under Class B conditions. A coplanar circuit was developed to permit feeding of NPN and PNP common-emitter HBTs from a common input signal terminal. The devices were thinned to 200 μm and mounted on 10-mil alumina substrates. Electromechanical tuners were used to increase the PNP gain and match it to that of NPN devices. Testing of the circuit showed best IM3 (by ~7 dBc) and smaller second harmonic content (by ~9 dBc) compared with NPN HBTs. In addition, the circuit produced 1.32 dB more output power than the NPN HBT alone at 1 dB of gain compression.

Overall, we present here the characteristics of PNP InP-based HBTs and first results on the implementation of complementary HBT circuits. Circuits of this type could lead to improved wireless communication systems. Other applications of the proposed scheme include high bit-rate communication with lower error rates.

Work supported by ARO-MURI (DAAH04-96-1-0001)



NPN/PNP push-pull common-emitter amplifier. The NPN and PNP HBTs were individually fabricated.



Power characterization of NPN/PNP push-pull common-emitter amplifier at 8 GHz. The 2nd harmonic and 3rd-order intermodulation (500 kHz separation) are improved when compared to a single NPN HBT amplifier.

SIMULATION OF THE MICROWAVE PERFORMANCE OF SiGe HBTS AND ITS AMPLIFIERS

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summary In this paper, we based on the physical model give the small signal equivalent circuits and the element value, through the following analyses: (1) The carrier transfer time from the emitter to collector include:□a□the carrier capacitance charge time from emitter to baseτe□(b) the emitter junction at forward bias, a few hole diffusion into emitter region, its store timeτef□□c□base transfer timeτb□□d□the collector deplete layer transfer timeτd□□e□the collector capacitance store charge timeτc,. when the base width is lower to several hundreds angstrom, and the base transfer timeτ_b decreced sharply, the emitter delay time and the collector delay time became more important for the cut off frequency f_T of SiGe HBTs; (2) the emitter series resistance is consist of three parts□□a□the meal contact resistance R_{Econ}□□b□the heavy doping region resistance R_{Eh}□□c□the low doping region resistance R_{El}. .The influence of the low doping density emitter layer to the emitter delay time is more important. it will increase the emitter series resistance and the emitter delay time. (3) For the emitter junction biased by forwards voltage, the emitter capacitance is composed of three parts: (a)the barrier capacitance C_{TE} in the EB junction space charge region(SCR), (b)the diffuse capacitance C_{DE} in several diffuse length out of the SCR□(c)at forward bias, as free carrier injection in the emitter-base SCR, increase the capacitance C_F. For the collector base junction capacitance, at normal operation, the collector base junction is reverse biased, it is composed of barrier capacitance mainly. as well as the capacitance due to the change of the fixed charges in the heterojuntion, the carrier injection in the emitter-base space charge region will result an additional capacitance for an heterojunction operating at forward bias, it will affect the cut off frequency f_T and the maximum oscillation frequency f_{max}. Based on this, We give the equal circuits of the SiGe HBTs (FIG. 2, 3), and analyze, simulate and optimize the device design, and the microwave parameters of the SiGe HBTs (FIG. 4), The samples of SiGe HBT of cut off frequency f_T=10GHz have been fabricated, in tripe mesa structure, emitter areas Ae=3×18 μm^2. the base areas Ab=23×24μm^2. The results of the tests are in agreement with our simulation. Use this type SiGe HBTs, we design and optimize the SiGe HBTs microwave amplifers (FIG.5). the linear power gain Gp=8dB, in the bandwidth range of f=0.1GHz to f=3.0GHz, in 50Ω input ant output system.

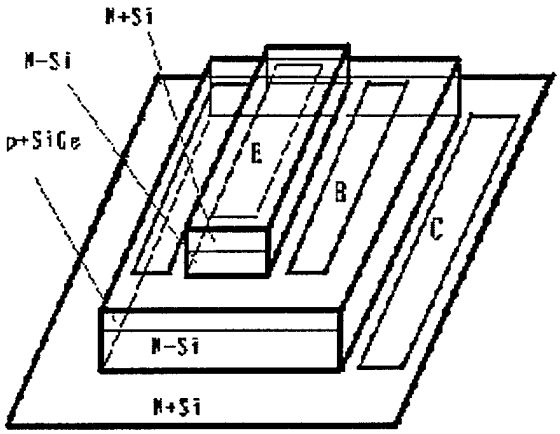


Fig. (2) SiGeHBTs Structure

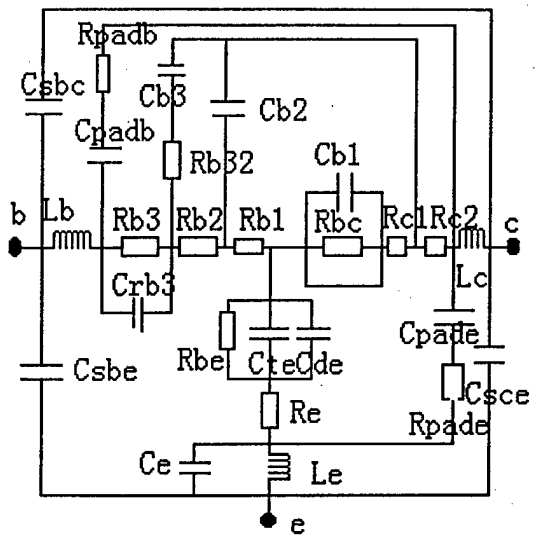
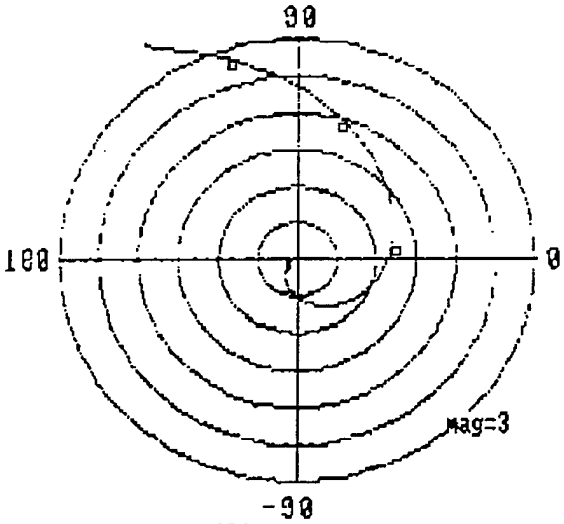
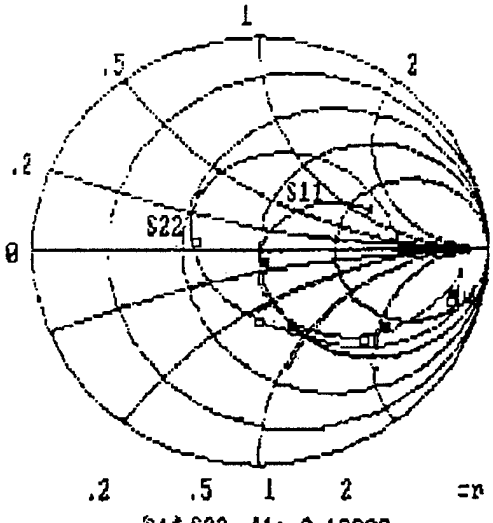


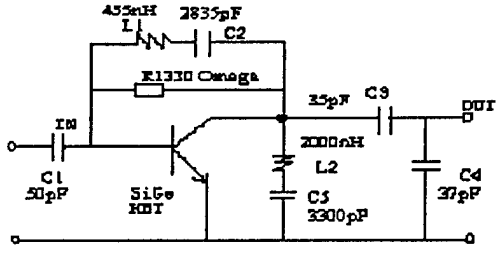
Fig.(3) SiGeHBTs Equal Circuits





Bias level: Vce=3V,Ic=15mA

□ Symble: Measurement data (frequency 0.10-6.10 GHz)



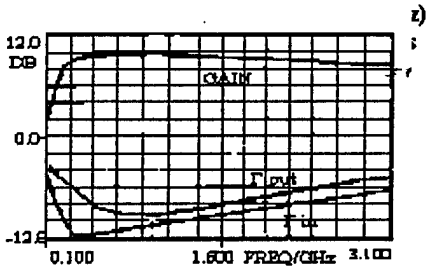


Fig.(5) SiGeHBTs Amplifier Circuits and SiGeHBTs Amplifier Gain--Frequency

77K Analog Monolithic HEMT Amplifier for High-Speed Josephson-Semiconductor Interface Circuit

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Josephson junction devices offer such attractive features as a fast switching speed and extremely low-power dissipation. A hybrid system combining Josephson and semiconductor devices is a realistic approach to constructing a practical Josephson system. A hybrid system would combine the high-speed processing of Josephson circuits and the large-scale processing capability of semiconductor circuits to be exploited concurrently. However, the Josephson output voltage is only 2.8 mV, while room-temperature semiconductor operation requires an operational voltage of at least several hundreds of millivolts and up to 1 volt. Therefore, the output voltage from the Josephson device must be increased by more than two orders of magnitude. To date, several Josephson-semiconductor interface circuits have been proposed and developed for various applications [1,2]. The purpose [3,4] of this work was to develop high-performance output interface circuits that can transfer the voltage signal from Josephson circuits to semiconductor circuits, speeds exceeding current GHz clocks.

It is difficult to amplify a voltage signal with only a Josephson device or a semiconductor transistor running at several gigahertz. Consequently, we proposed the output interface circuit illustrated in Figure 1. The circuit combines 4.2K Josephson high-voltage drivers[5] with a 77K analog HEMT monolithic amplifier. A Josephson driver with 10 stacks boosts the signal voltage from 2.8 to 28 mV, and the HEMT amplifier converts the voltage from 28 mV to almost 1 V, which is sufficient for driving room temperature semiconductor devices. HEMT device technology was employed for its superior high-speed performance, and the 77K operational temperature was selected both to suppress power-consumption in a liquid-helium refrigerator and in anticipation of future 77K superconductive electronics.

To construct 77K analog HEMT amplifiers, we employed the basic wide-band circuit configuration. It includes a differential amplifier with complementary input ports and 50 Ω termination resistors as a first stage, 4-stage high-gain source-grounded amplifiers, and output buffer. A differential amplifier with complementary inputs was employed to cancel changes in the output signal voltage caused by ground-level voltage fluctuations in Josephson circuits.

We fabricated a monolithic amplifier chip using the 0.5 μm-gate InGaP/InGaAs HEMT technology we developed. Sputtered WSiN thin film was used for the resistors. The resulting HEMT has a typical transconductance of 530 mS/mm and a current-gain cutoff frequency of 43 GHz at 77K.

RF performance was measured with a cryogenic on-wafer probing system and an automatic network analyzer. The amplifier gain was measured as a function of frequency from 0.2 to 20.2 GHz at 77K. The low-frequency gain was 23 dB, and the frequency at -3 dB was 8 GHz. This is sufficient for the clock frequency of several gigahertz used in Josephson digital circuits. The output waveform response for high-frequency operation was also tested. A complementary 30 mV_{pp}, 3 Gbit/s RZ signal pattern, which simulates the output of a 10-stack Josephson high-voltage driver, was added to two input ports. As shown in Figure 2, the output amplitude is 0.7 V_{pp} making it possible to drive room-temperature GaAs DCFL gates and/or future scaled CMOS gates.

The operation of the overall interface circuit was examined by joining the 77K HEMT amplifier to liquid-helium cooled Josephson high-voltage drivers. Complementary input signals from a room-temperature pattern generator were sent to two Josephson chips. The output signal of the gates were sent to two input terminals of the HEMT amplifier held at

77K via biaxial cables at room temperature. The repetition frequency is 300 MHz, which is limited by crosstalk at the signal lines by a chip holder in liquid He. Figure 3 shows the output waveform, which has an amplitude of 0.7 V_{pp}. Since circuit simulations have confirmed that Josephson high-voltage drivers can operate at several gigaherz, we can state that our interface circuit can transfer a high-speed voltage signal from Josephson circuits to a room temperature apparatus at a 0.7 V_{pp} amplitude.

We developed high-speed interface circuits composed of 4.2K Josephson high-voltage drivers and a 77K analog HEMT amplifier. We employed a basic wide-band circuit configuration for the 77K analog HEMT amplifier, which consists of a complementary input differential amplifier and high-gain single-ended amplifiers. We successfully demonstrated that this circuit can transfer the voltage signal from a Josephson driver to a room-temperature device at 0.7 V_{pp} of amplitude.

This work was performed under the management of FED as a part of the MITI R&D program (Josephson Device Hybrid System Technologies Project) supported by NEDO.

References

[1] V. Ghoshal, et al., IEEE Trans. Appl. Supercond. vol. 5, pp. 2640-2643, 1995.
[2] V. Ghoshal, Extended Abstracts of Intern. Symp. on the Basis of Future Electronics Technology (FUET'96), pp. 121-128, 1996.
[3] K. Hikosaka, et al., Extended Abstracts of 15th Symposium on Future Electron Devices (FED-149), pp. 171-176, 1996.
[4] K. Hikosaka, et al., Extended Abstracts of the 5th International Workshop on High-Temperature Superconducting Electron Devices (HTSED '97), pp. 55-56, 1997.
[5] H. Suzuki et al., Technical Digest of International Electron Devices Meeting , pp. 290, 1988.

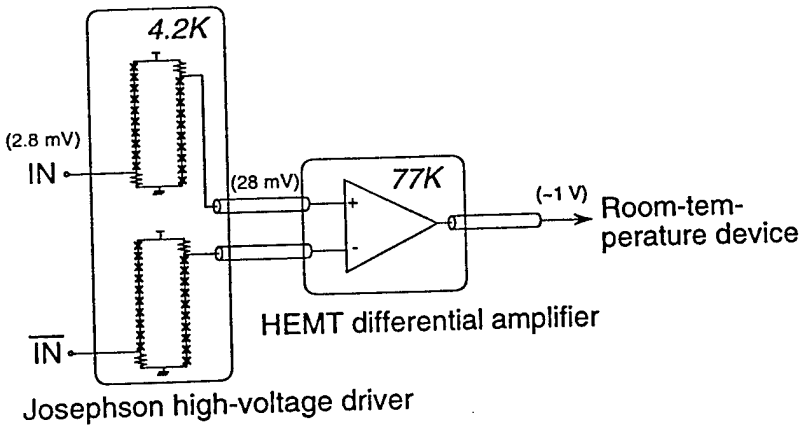

Figure 1 Diagram of our proposed Josephson-Semiconductor output interface circuit.

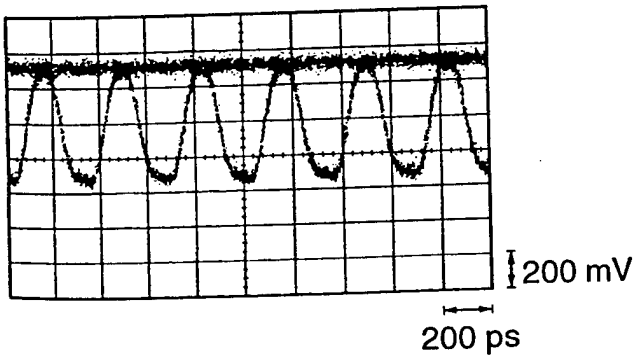

Figure 2 Output waveform of HEMT amplifier with 3 Gbit/s, 30 mV_{pp} inputs.

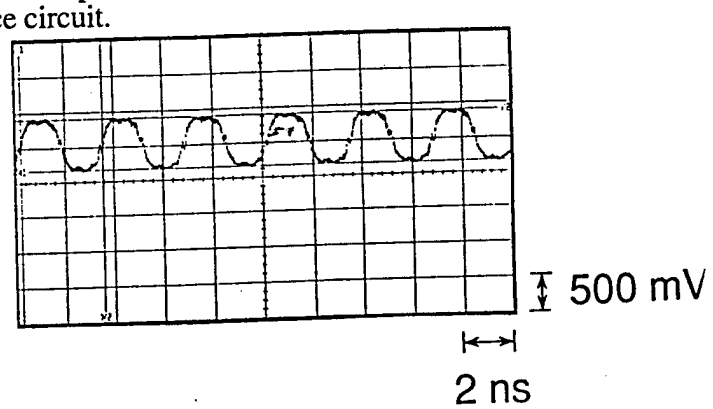

Figure 3 Output waveform of overall interface circuit.

By suppression of electro chemical etching in deionized water

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In the fabrication process of HEMT, the recessed depth and shape is critical to its device performa However it was found that the gate recess region was anomalously etched during the deionized water rinse pro due to the electro-chemical etching effect [1-3]. This paper describes the mechanism of the electro-chemical etc which seriously affects the device performance.

Figure 1 shows the cross-section of the 0.1μm-gate pseudomorphic InGaAs/AlGaAs HEMT used in this st All the layers were grown by MBE. At first, the oxygen ion implantation for the device isolation was perfor and the Au-based ohmic electrodes were formed. Next, the silicon nitride film of 0.1μm-thick was deposite PCVD and the 0.1μm resist spacing for the gate pattern was formed using electron beam lithography. Then silicon nitride was etched by RIE and the resist pattern for the top portion of the T-shaped gate was formed usin line lithography. After the recess etching using H_3PO_4-based etchant, Al/Ti gate electrode was evaporated lifted off. During the process, the deionized water rinse, in which the gate recess region was directly expose the deionized water, was performed twice. The first deionized water rinse was performed after the resist rem followed by RIE of silicon nitride film and the second was performed in the Al/Ti gate lift-off process. property of the deionized water was the resistivity of 18MΩcm and the dissolved oxygen concentrat incorporated from air, of 8ppm. Figure 2(a) shows the profile of the gate recess region after the first deioni water rinse measured by AFM. As shown in figure 2(a), the boundary between the channel region and the isol region was anomalously etched and a non-flat profile was obtained. This anomalous etching can be understoo the electro-chemical etching effect of deionized water where the ohmic electrode works as the cathode and GaA the gate recess region as the anode. The mechanism of the electro-chemical etching effect is graphically show figure 3. Due to the cathode reaction on the ohmic electrode, OH^- ions are generated from the reaction between deionized water (H_2O) and the dissolved oxygen (O_2). At the same time with the cathode reaction, the an reaction on GaAs surface, oxidation and etching, occurs. Because hole in GaAs enhance the anode reaction, isolated region, which behaves like p-type, is deeply etched. The etching current as shown in figure 3 decrease the distance from the ohmic electrode becomes large because of the high resistivity of the isolated Ga Therefore the etching occurs especially near the boundary between the channel region and the isolated reg resulting in the non-flat profile. Such an electro-chemical etching effect also occurs during the second deioni water rinse process. Figure 4(a) shows the cross-sectional TEM image of the recessed region around the A gate after the lift-off process. From this figure, it was found that GaAs of the recessed region beside the Al/Ti g was anomalously etched. This anomalous etching can be also understood as the electro-chemical etching ef between the Al/Ti gate and GaAs. Based on the model as shown in figure 3, in order to suppress the elect chemical etching effect, it is effective to reduce the dissolved oxygen in deionized water which causes OH^- ion. confirm the effect of dissolved oxygen in deionized water on the electro-chemical etching effect, the deionized wa with reduced dissolved oxygen was used for the water rinse process. The rinse was performed in N_2 ambiance prevent incorporation of oxygen from air. Figure 5 shows the dependence of the etching depth at the bound between the channel region and the isolated region on the concentration of the dissolved oxygen. This fig shows that the etching depth decreases as the concentration of the dissolved oxygen decreases. Figure 2(b) sho the profile of the gate recess region in case of 2ppb for the dissolved oxygen. The electro-chemical etching w successfully suppressed and a flat profile was obtained. The anomalous etching beside the Al/Ti gate can be a suppressed by the deionized water with dissolved oxygen of 2ppb as shown in figure4(b).

Using the deionized water with reduced dissolved oxygen, the 0.1μm-gate pseudomorphic HEMT w fabricated. Figure 6 shows the current gain cut-off frequencies (f_T) extracted from S-parameter measuremer By reducing the dissolved oxygen in deionized water, f_T was improved up to 104GHz. It should be noted that key of the process is the amount of the dissolved oxygen in deionized water for the rinse process.

1) Y. Nitta, T. Ohshima, R. Shigemasa, S. Nishi and T. Kimura : Tech. Dig. IEDM, 47(1996)
2) T. Ohshima, R. Shigemasa, Y. Nitta, M. Tsunotani and T. Kimura : Record of the 16th Electronic Materi Symposium, 241(1997)
3) M. Hagio : J. Electrochem. Soc., 140, 2402 (1993)

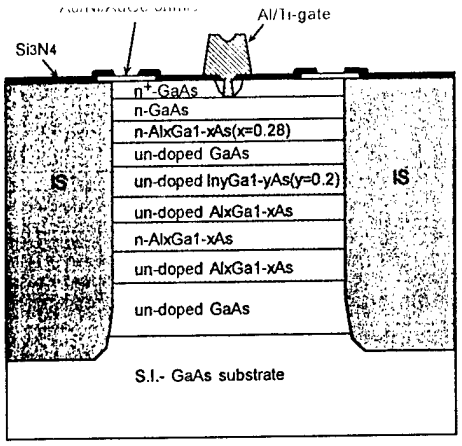

Fig.1 Cross-section of pseudomorphic HEMT

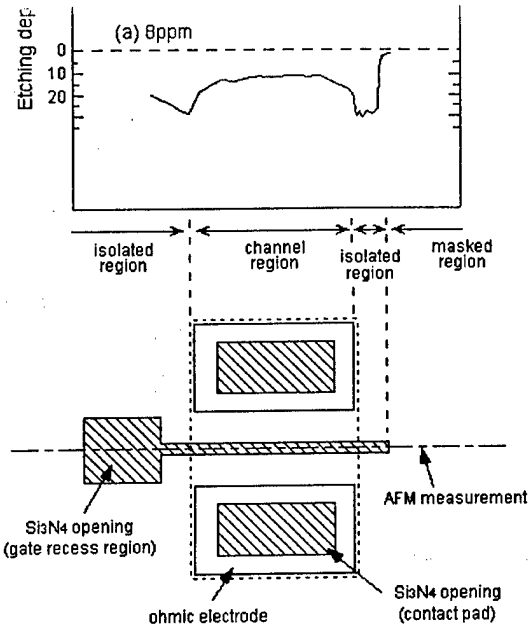

Fig. 2 Profiles of gate recess region after the deionized water rinse with dissolved oxygen of (a)8ppm and (b)2ppb

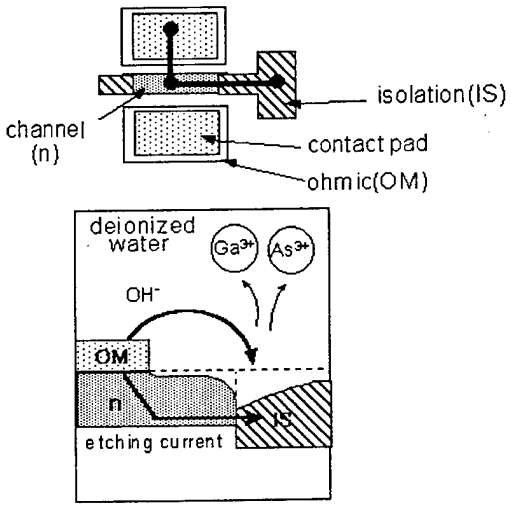

Fig. 3 Model for electro-chemical etching

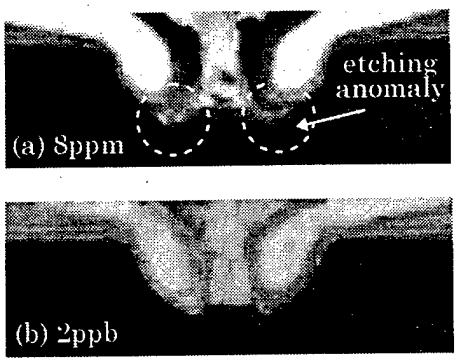

Fig. 4 TEM images of recessed region around the Al/Ti gate after the deionized water rinse with dissolved oxygen of (a)8ppm and (b)2ppb

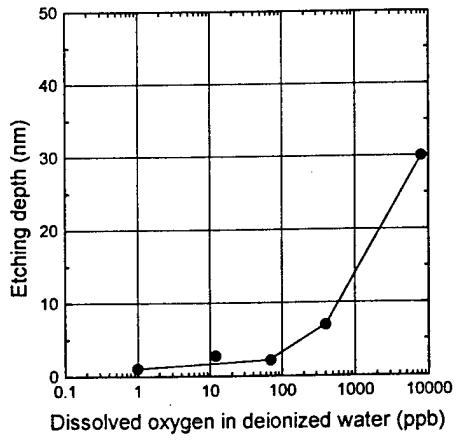

Fig. 5 Dependence of concentration of dissolved oxygen on the etching depth.

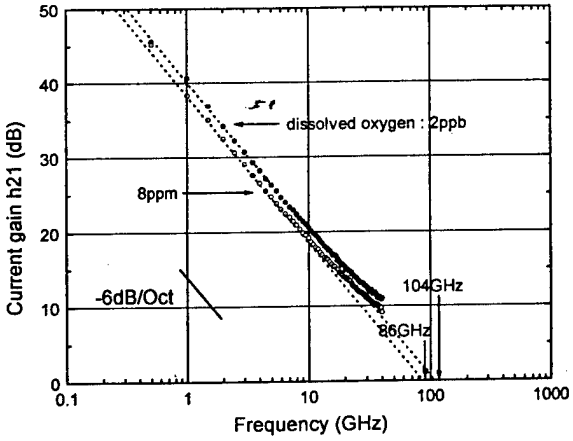

Fig. 6 Frequency characteristics for the HEMTs rinsed in deionized water with dissolved oxygen of 8ppm and 2ppb.

for InAlAs/InGaAs MODFETs with Short Gate-lengths

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Proper width of side recess etching is very important to the performance of the modulation-doped field-effe transistor (MODFET)[1]. Since the gate grooves are usually symmetric, a trade-off regarding the width of sic etching has to be made in accordance with the specific requirements of a device. Asymmetrically recesse gates, whose side etching is small on the source side and simultaneously large on the drain side, make it poss ble for us to take full advantage of the superior transport properties of InAlAs/InGaAs heterostructures and r sulting excellent high frequency performance of MODFETs. The standard fabrication approach is to for asymmetrical resist profiles. This can be achieved either by a so-called "double-recess" process[2] or by electro beam lithography based on a four-layer stack of resist.[3] The former methodology needs two step lithograph on the other hand, the multilayer-resist technology requires the control of various process parameters, whic makes the fabrication process complicated and subject to failure. Our new approach, however, is based c asymmetrical etching that is induced by electrochemical effects in the course of gate-recess etching.

Figure 1 shows the cross section of a device ready for gate-recess etching. The citric-acid-based etchant giv an etching rate of 0.2 nm/s for both InAlAs and InGaAs in the absence of electrodes. However, this etching ra will be significantly modified by the presence of electrodes, as an electrochemical potential will be establishe between the electrodes and the semiconductors in the gate region. Fig. 2(a) shows that the groove for the N sample extends at greatly enhanced rates of 10 and 4 nm/s vertically and laterally. The higher electrode pote tial of Pt surface metal, on the other hand, will lead to excessive oxidation and a consequent slowing down c semiconductor etching (e.g. 0.07 nm/s in n^+-InAlAs) in the gate opening as shown in Fig. 2(b). Therefore, wit the respective deposition of Pt and Ni on the source and drain electrodes, asymmetric gate grooves can be fab ricated by the subsequent wet-chemical etching. Note that the structures we used were grown by metalorgani chemical vapor deposition (MOCVD), which include an InP etching stopper.

Figure 3 shows the micrograph of scanning electron microscope (SEM) of an asymmetric groove for a 0.1-μm gate opening. The width of side etching is defined as the width of the groove where the largest side etchin occurs, i.e. in n^+-InGaAs. The widths of side etching are 30 ($=L_s$) and 50 nm ($=L_d$) on the source and drain side accordingly, producing an asymmetry ratio, defined as L_d/L_s, of around 1.7; further work is in need to increas the asymmetric ratio. The first MODFETs have been fabricated with the above-described technology.

The *I-V* characteristics of MODFETs with this asymmetric gate groove are shown in Fig. 4(a) in compariso with those with the normal symmetric gate grooves as shown in Fig. 4(b). Because the side etching in both type of wafers are not large, no obvious difference in parasitic resistance can be found. Both devices have a maxi mum transconductance of around 1 S/mm at V_{ds}=1 V. The remarkable feature in Fig. 4 is the higher output con ductance for asymmetric MODFETs, which can be explained by the smaller effective gate lengths resultin from the "step" in the groove bottom as shown in Fig. 3. The reduced effective gate lengths for asymmetri MODFETs can be further evidenced by their larger threshold-voltage shift compared with those with the iden tical nominal gate lengths but symmetric gate grooves as presented in Fig. 5. Figure 6 shows the on-wafer s parameter characterization, which indicates a 10% increase in the current gain cut-off frequency (f_T) for device with gate lengths ranging from 0.07 to 0.1 μm. The maximum oscillation frequency (f_{max}) of asymmetric MOD FETs also show a higher value. For the nominal 0.07-μm devices, this figure of merit is 270 and 240 GHz fo the asymmetric and symmetric grooves. This should be attributed to the higher f_T and the lower feedback ca pacitance due to the wider L_d of the device with asymmetric gate groove.

1.Y. Kwon et al., *Proc. of 13th Conf. Advanced Concepts in High Speed Devices & Circuits*, pp. 141-150, 1991.
2.R. Grundbacher et al., *IEEE Trans. Electron Devices*, vol. 44, pp. 2136-2142, 1997.
3.C. Gaquiere et al., *IEEE Trans. Electron Devices*, vol. 42, pp. 209-214, 1995.

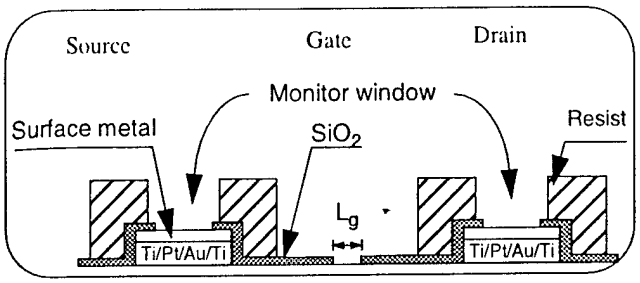

Fig.1: Schematic of wet-chemical gate recess etching for MODFET fabrication. The surface metal on ohmic electrodes can be either Ni or Pt.

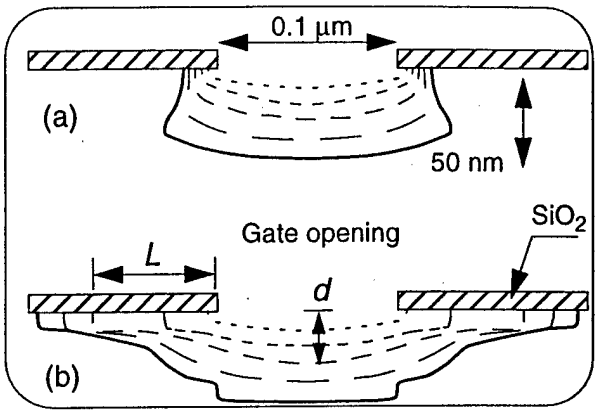

Fig. 2: SEM-observed evolution of groove profiles of 0.1-μm gate for (a) the Ni and (b) the Pt samples during recess. The etching times in (a) are 5, 10, 15, 20, and 25 s, and in (b) 5, 80, 140, 150, and 160 s. d and L are respectively the depth of vertical etching and the width of side etching.

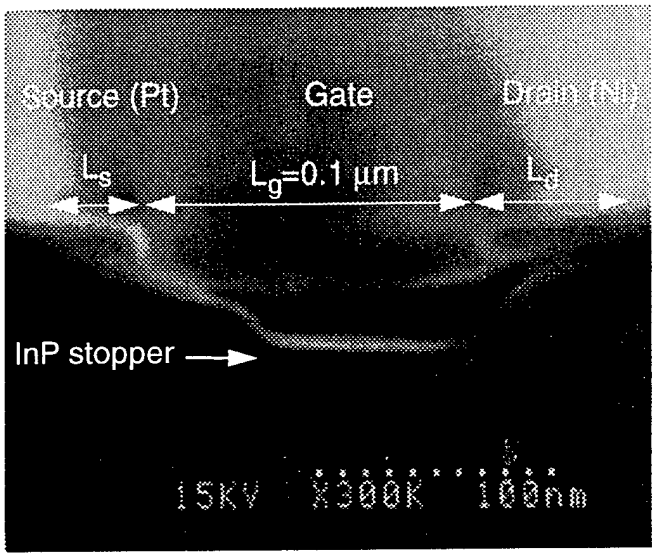

Fig. 3: SEM micrographs of asymmetrically recessed gate grooves for a 0.1-μm MODFET that was fabricated using the procedures depicted in Fig. 4. In the figure, L_s and L_d denote the side etching on the source side and the drain side, respectively. The flat groove bottom is from InP etch stopper.

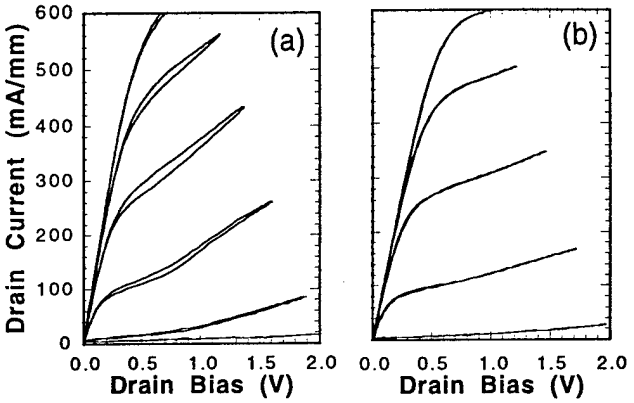

Fig. 4: I-V characteristics for 0.1-μm MODFETs (a) with the asymmetric gate groove profile shown by the solid curve in Fig. 3, and (b) with the conventional symmetric gate groove profile. Top curves: V_{ds}=0.4 V, ΔV_{gs}=-0.2 V.

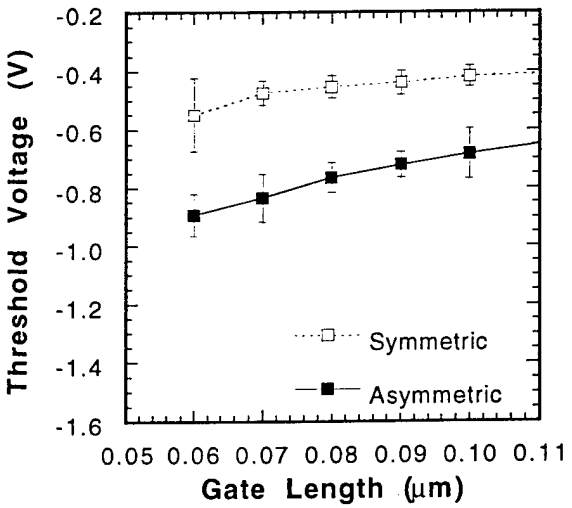

Fig. 5: Threshold voltage shift (measured at V_{ds} = 1 V) with respect to gate length for MODFETs with asymmetric and conventional symmetric gate-groove profiles.

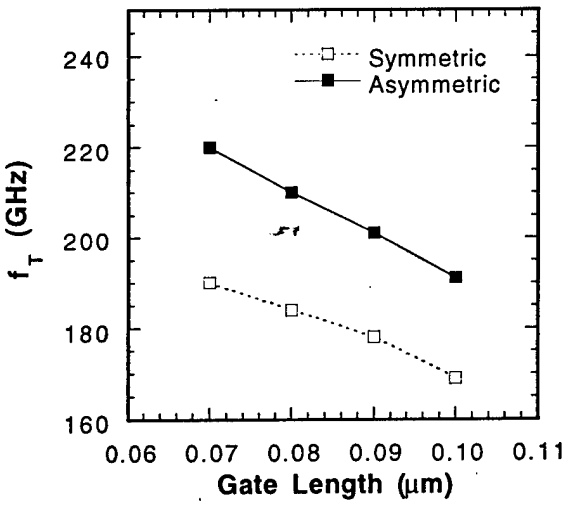

Fig. 6: Current gain cut-off frequency (measured at V_{ds} = 1 V) with respect to gate length for MODFETs with asymmetric and conventional symmetric gate-groove profiles.

HFET transfered onto GaAs substrate

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One proposed concept of monolithic integration of optoelectronic and electronic components without any degradation of the optimized optoelectronic device-properties is the growth of HFETs at very low temperatures (LTG) at comparable temperatures as those of thin film transistors. The P_{In} anti-side defect with first excited state located $120\,meV$ above the conduction band edge [1] leads to auto-doped n-type layers and makes LTG-InP a promising candidate for active layers. The concentration of this P_{In} anti-site defects is connected with the growth temperature and V/III flux ratio. Therefore, a strong influence of growth temperature on sheet carrier concentration and saturation current is found.

First devices fully grown on InP substrates at $300°C$ and below were presented earlier [2,3]. We demonstrated the feasibility of fully low temperature grown and processed devices on InP substrates. Despite the fact that in first order approximation the doping concentration equals the defect concentration, RF measurement results even revealed similar potential for high speed applications as compared to conventionally grown InP. For a $l_g = 0.4\,\mu m$ gate length device maximum current cut-off frequency of $f_t = 18$ GHz and maximum oscillation frequency $f_{max} = 40$ GHz were presented (Fig. 4) [3]. To merge, for example, previous grown VCSEL structures on GaAs substrates with active devices, LTG GaAs layers applicable for FET structures will be needed. However, LTG GaAs layers are known to be insulating and in contrast especially used for buffer layers or gate dielectric [4]. Therefore, an attempt was made to transfer the concept of the LTG InP layers onto other substrates besides InP and even GaAs.

In this investigation we will demonstrate the first LTG InP-channel HFET devices grown at $300°C$ on GaAs substrates. Hall effect measurements, of the first experiment, revealed a sheet charge density of $1 \cdot 10^{13}\,cm^2$ and corresponding mobility of $1000\,cm^2/Vs$ comparable to conventionally grown InP layers on InP substrates to high for FET channel to be pinched off. LTG-AlInAs was used as gate contact layer [2]. The thickness of the thin layers still remains below the critical thickness for relaxation and therefore the layers are highly strained and under compressive stress. A new technological redesign has lead to the DC output characteristics of LTG-InP FETs shown in Figure 3 with the gatewidth of $W_g = 50\,\mu m$ and $l_g = 1.5\,\mu m$. The channel current reaches a maximum open channel current density of $2.8\,mA/mm$ which is still low. Due to difficulties with the Schottky, layer pinch off is only partially possible. As in the case of InP the Schottky layer characteristics seem most critical. In comparison to the first HFET structure on GaAs (Fig.1 & 2), DC output characteristics and RF results of optimized HFET device structure grown on InP substrate are shown in Figure 3 & 4 [3]. It

further to make them comparable to the InP counterparts.

In conclusion, this proof of concept is the starting-point for further improvements. Furthermore, the fundamental possibility of transfering the growth of LTG-InP channel HFETs to GaAs substrates was shown leading to promising expectations for growth on other non-InP substrates.

References

[1] W. Chen et al., *J. Appl. Phys.*, **76,** (1994), pp. 600-602.

[2] B. Henle and E. Kohn, *IPRM 97*, Hyannis, Ma, USA, 11-15 May 1997, proc. 165-168

[3] L.H. Lee, M. Kunze, B. Henle and E. Kohn, *accepted for IPRM 98*, Tsukuba, Japan, May 1998

[4] C.-L. Chen et al., *IEEE Electron Dev. Lett.*, **12,** (1991), pp. 306-308.

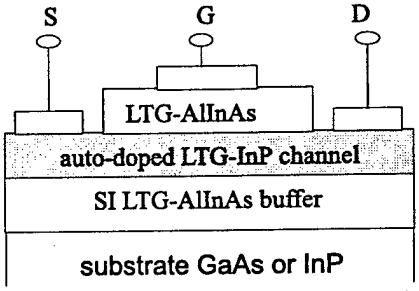

Fig.1: Schematic device structure of LTG-InP FET on GaAs or InP substrate

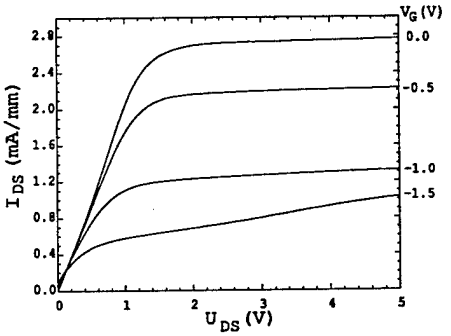

Fig.2: First output characteristics of LTG-InP FET grown on GaAs substrate at $300°C$ ($W_g = 50\,\mu m$ and $l_g = 1.5\,\mu m$

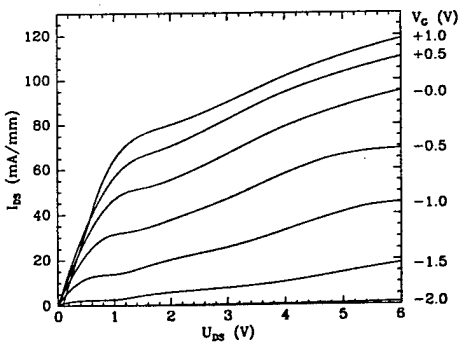

Fig.3: Output characteristics of optimized LTG-InP FET grown on InP substrate at $280°C$ ($W_g = 50\,\mu m$ and $l_g = 1.5\,\mu m$

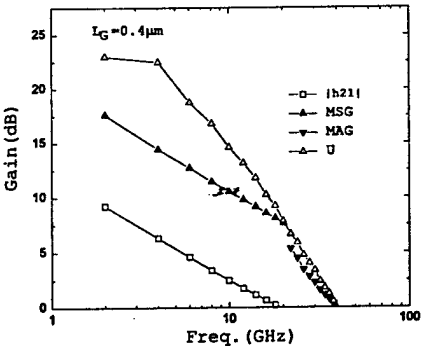

Fig.4: Gain plot of LTG InP HFET on InP substrate ($l_g = 0.4\,\mu m$, $T_{growth} = 280°C$)

Growth of Device Quality InGaP/GaAs Heterostructure by GSMBE using TBP

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Recently, $In_{0.48}Ga_{0.52}P$/GaAs HBTs and HEMTs have been attracting significant attentions due to their advantages over conventional AlGaAs/GaAs-based devices. Particularly, a larger ΔE_V, a lower surface recombination velocity, lower defect densities and higher reliability of the InGaP/GaAs system than the AlGaAs/GaAs system as well as absence of DX centers are attractive for HBT applications, leading to high and temperature insensitive current gain, low noise performance and high reliability of InGaP/GaAs HBTs.[1]

As compared with standard MOVPE and GSMBE approaches using highly toxic phosphine to grow InGaP, GSMBE using tertiarybutylphosphine (TBP), which combines advantages of MBE with low toxic nature of TBP, seems to be attractive for high volume production of heterostructure wafers. However, crystal qualities of InGaP layers grown by GSMBE using TBP reported so far have been inferior to those by the standard methods and no systematic optimization of the growth has been made for achieving high quality InGaP/GaAs heterostructures by this method.[2-4]

The purpose of this paper is to systematically investigate the GSMBE growth of InGaP layer on GaAs using TBP and to optimize the growth conditions for achieving device quality InGaP/GaAs heterostructure. Undoped InGaP layers were grown on GaAs buffer layers by GSMBE using metallic In, Ga, As and 100% TBP as source materials. RHEED, AFM, SEM, XRD, PL and Hall measurements were performed for characterization. Main results are listed below:

(1) The initial surface reconstruction of GaAs was found to be vitally important for successful growth. **Figure 1(a)** compares RHEED behavior taken during InGaP growth on As-rich c(4x4) GaAs and As-stabilized (2x4) GaAs surfaces. As shown in **Fig.1(a)**, only the growth on (2x4) surface led to observation of strong and persistent RHEED oscillations, indicating realization of stable layer-by-layer growth of InGaP. Observed number of RHEED oscillation cycles, N, during the growth of InGaP on (2x4) GaAs was found to be strongly dependent on growth temperatures, T_s, as shown in **Fig.1(b)**. N took maximum around T_s=490°C, indicating that highly stable layer-by-layer growth of InGaP was realized under this condition.

(2) Such an optimum growth condition led to growth of InGaP layers with excellent optical qualities as shown in **Fig.2**. The narrowest PL FWHM value of 15.5meV obtained at T_s=490°C is comparable with the best data reported for InGaP layers grown by the standard methods.

(3) **Figure 3** shows AFM images of InGaP surfaces grown at the optimum growth temperature of 490°C and that at 510°C together with histograms of their height distributions. It is found from **Fig.3(a)** that remarkably smooth surface morphology of InGaP was obtained at 490°C. The RMS value of 1.0nm is comparable with that of GaAs grown by conventional MBE, indicating that high quality heterointerface can be formed under such an optimum condition. On the other hand, growth at unoptimum temperatures resulted in rough surfaces such as shown in **Fig.3(b)**.

(4) The InGaP layers grown by the present GSMBE using TBP under the optimum condition were found to posses excellent electrical properties. High electron mobilities larger than 2,500 cm^2/Vs as well as low residual n-type carrier concentrations around $1x10^{15}cm^{-3}$ were achieved as shown in **Fig.4**, which are comparable to the best data obtained for InGaP layer grown by MOVPE and GSMBE using phosphine. Such a good electrical property as well as the smooth surface achieved in the present InGaP layers are obviously promising for applications to HBTs and HEMTs.

[2] E.A.Beam III et al.: J. Crystal Growth **110** (1992) 456.
[3] J.M.Kuo et al.: J. Vac. Sci. Technol. **B10** (1992) 959.
[4] Y. Ohba et al.: J. Crystal Growth **77** (1986) 374.
[5] C.Besikci et al.: IEEE Trans. Electron Devices **41**(1994) 1066.

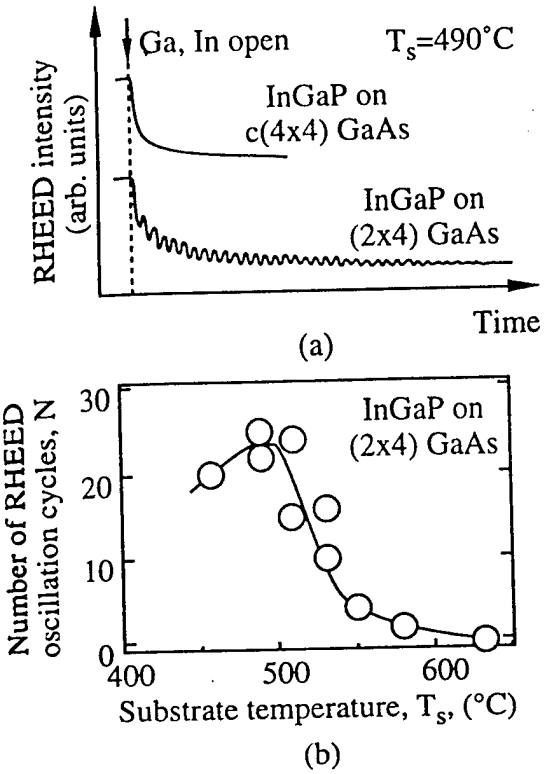

Fig.1 Dependences of RHEED behavior observed during InGaP growth on (a) initial GaAs surface reconstructions and (b) substrate temperatures.

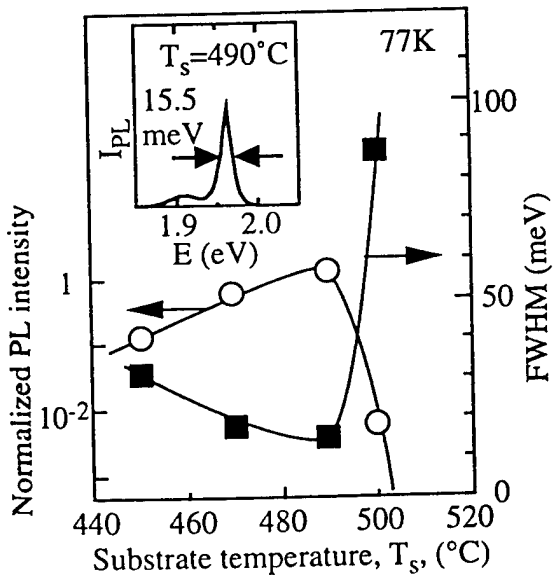

Fig.2 Growth temperature dependence of PL inteinsities and PL FWHM values of the InGaP layers.

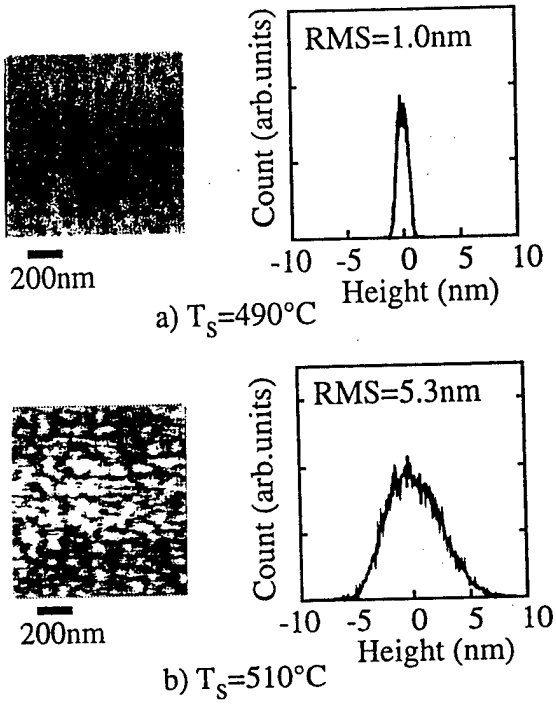

Fig. 3 AFM images and histograms of their height distributions of InGaP surfaces grown at (a)T_S=490°C and (b)510°C.

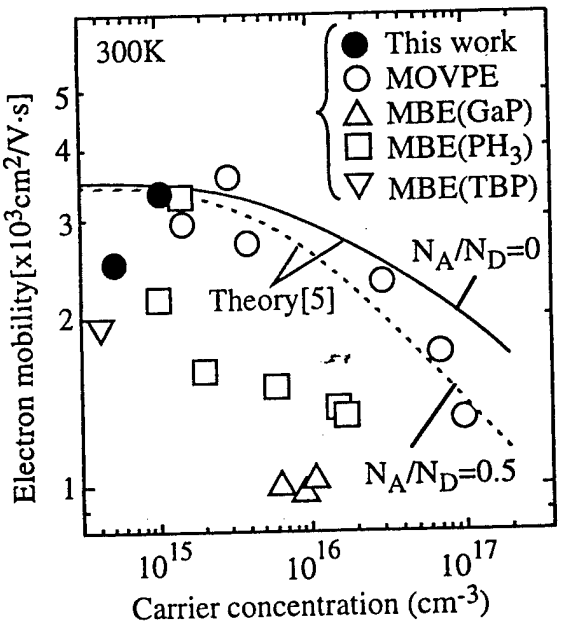

Fig. 4 Relationship between electron Hall mobilities and carrier concentrations for InGaP layer grown by various methods.

Grown GaAs Layer by Kelvin Probe Force Microscopy

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Kelvin probe force microscopy (KFM) has proven to be an atttractive method t measure the potential profile of the GaAs devices [1,2,3]. In this work, we have applied th KFM technology to the GaAs MESFETs passivated with low-temperature (LT) grown GaA layer, which was designed to realize high breakdown voltage [4]. High-field regions at th drain-side edge of the gate was not so clear compared to that of the MESFET without the L GaAs cap layer. This suggests that the LT GaAs is effective in reducing the electric field a the drain-side edge of the gate resulting in a high breakdown voltage.

Figure 1 shows a schematic diagram of the KFM measurement system. The measuremen system has two feedback loops. Z feedback loop is used for the control of the z-axis positio of the sample, and the other is used for the surface potential measurements. The operatio principle of the KFM is based on the measurement of electrostatic force which arises whe potential difference exists between the cantilever tip and the sample surface. When the DC bias voltage V_{off} is adjusted so that amplitude of the electrostatic force becomes zero, th sample surface potential, V_s, can be given as $-V_{off}$. The measurements were carried out in a air ambient at room temperature.

Figure 2 shows a schematic cross-sectional view of the measured GaAs MESFETs All layers were grown by MBE. The LT GaAs grown at 200 C is used as a low-conductiv bypass with linear I-V characteristics [4]. The AlAs layers were grown to prevent th in-diffusion of excess As from the LT layer. The source-drain breakdown voltage was 30 V at V_{GS} = 0 V for the MESFET with 5.5 μm drain-source spacing and 1.2 μm gate length Figure 3 shows the I-V characteristics of the measured MESFETs with LT GaAscap layer Measured devices were prepared by cleavage, which did not cause any damage on the I-V characteristics of the devices.

Figure 4 shows the contour lines of the measured potential profile of the MESFET a (a) a linear region (V_{GS} = 0 Vand V_{DS}= 2.5 V) and (b) a saturation region (V_{GS} = - 3 Vanc V_{DS}= 2.5 V) of the I-V characteristics. In the linear region, a relatively uniform electric fielc is obtained as shown in Fig. 4(a). In the saturation region, the shape of the contour lines changed. However, the high-field region at the drain-side edge of the gate is not so clear a shown in Fig. 4(b) compared to those of GaAs HEMTs which was reported previously [2] The MESFET without the LT GaAs cap layer was measured as a reference. In this case, the high-field region at the gate edge is more clear as shown in Fig. 5 than that of the saturatior region (Fig. 4(a)).

These results suggest that the LT GaAs is effective in reducing the electric field at the drain-side edge of the gate resulting in a high breakdown voltage.

References

[1] M. Arakawa, S. Kishimoto, and T. Mizutani, Extended Abstracts of the 1996 Int. Conf. Solid State Devices and Materials, pp. 100-102, 1996.
[2] T. Mizutani, M. Arakawa and S. Kishimoto: Technical Digest, IEDM, San Francisco 1996 (1996) p. 31.
[3] T. Usunami, M. Arakawa, S. Kishimoto, T. Mizutani, T. Kagawa, and M. Iwamura, Extended Abstract, 1997 Int. Conf. Solid State Devices and Materials, Hamamatsu, 1997, pp. 330-331
[4] K. M. Lipka, B. Splingart, R. Westphalen, E. Kohn, D. Theron, B. Boudart, G. Salmer, L. L. Pond, C. E. Weitzel, IEEE Cornel Conference, August 7-9, 1995, Ithaca

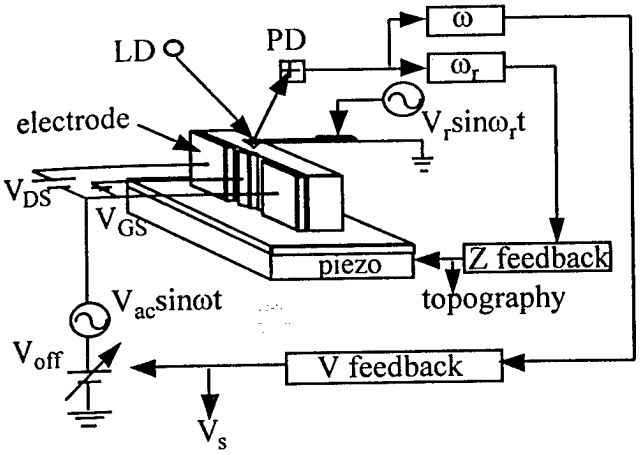

FIG. 1 Schematic diagram of the KFM measurement system.

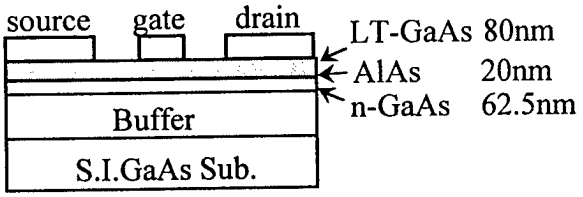

FIG. 2 Schematic cross section of the measured MESFETs.

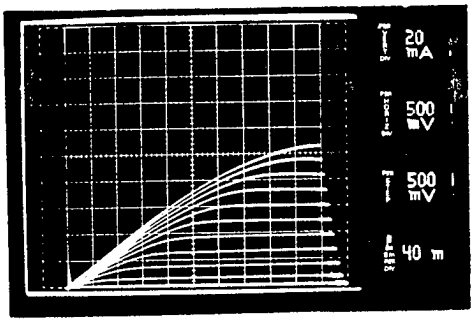

FIG. 3 I-V characteristics of the measured GaAs MESFET with LT GaAs cap layer.

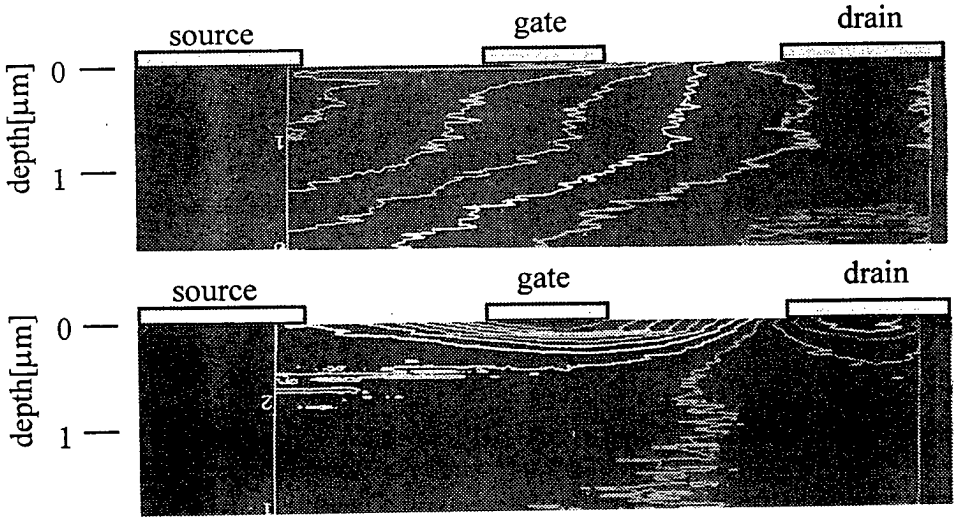

FIG. 4 The contour lines of the measured potential profile of the MESFET with LT GaAs cap layer at (a) a linear region (V_{GS} = 0 Vand V_{DS}= 2.5 V) and (b) a saturation region (V_{GS} = - 3 Vand V_{DS}= 2.5 V) of the I-V characteristics.

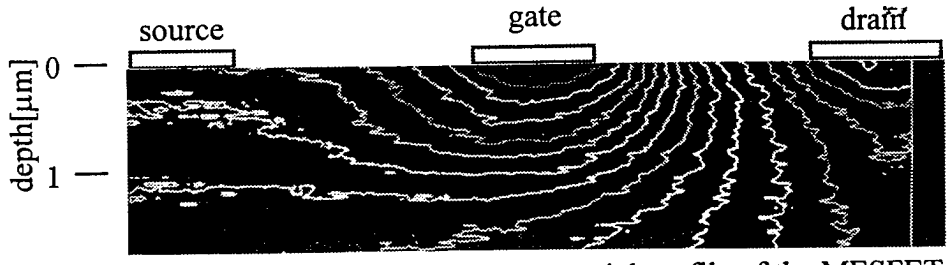

FIG. 5 The contour lines of the measured potential profile of the MESFET without LT GaAs cap layer at a saturation region (V_{GS} = - 1.5 Vand V_{DS}= 2.5 V) of the I-V characteristics.

PHOTOELECTRIC RESPONSE OF HETEROSTRUCTURE TRANSISTORS

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Photoelectric characterization of fully fabricated heterostructure transistors has become an important device characterization tool. Also, heterostructure transistors are excellent optical detectors, which can be monolithically integrated with amplifier and signal processing circuits. In many of these devices, the bandgap in the active transistor area is smaller than in the rest of the structure and backside illumination is feasible. The ability to use backside illumination is significant since the front side of these structures is covered with metals, which would shade these areas with illumination from the front.

Photoelectric techniques, such as photoluminscence, are routinely used for the characterization of semiconductor materials. We have extended photoelectric characterization to the analysis of fully fabricated heterostructure field effect and bipolar transistors.[1],[2] The photoemission and conductance (PEC) studies provide information on the energy profiles in these transistors and on their dependence on applied voltages. The measurements are performed on-wafer, at room temperature and are non-destructive.

Using the PEC technique, we were able to resolve the quantum levels in fully fabricated GaAs based PHEMTs and determined the values of these states.[3] We also were able to observe the changes of the configuration of the quantum wells with applied gate voltage.[4] The HEMTs amplify the photogenerated charge. From the

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[1] Fritz Schuermeyer, C. Cerny and E. Martinez "Photo Emission and Conductance Studies on PHEMTs", Topical Workshop on Heterostructure Microelectronics, Susono-City, Japan, August 17 - 19, 1994.

[2] Fritz Schuermeyer, Charles Cerny, J.P. Loehr, and R.E. Sherriff "Photoelectric Emission and Conductance Studies on Fully Fabricated PHEMTs", Solid State Electronics 38, 1615-1618, 1995.

[3] Fritz Schuermeyer, J.P. Loehr, R.E. Sherriff, C. Cerny, and M. Shur "Photoelectric measurements of interband transitions in fully fabricated pseudomorphic high electron mobility transistors", presented at the 22nd International Symposium on Compound Semiconductors (ISCS), Cheju Island, Korea, 28 August - 2 September 1995. Published in Inst. Phys. Conf. Ser. No 145: Chapter 5, pp 791-796, 1996

[4] Fritz Schuermeyer, Charles Cerny, J.P. Loehr, and R.E. Sherriff "Characterization of Pseudomorphic Heterostructure FETs by the Photoconduction Technique", presented at the 1995 International Semiconductor Device Research Symposium, Charlottesville, VA, December 6 - 8, 1995 (Proceedings pp 31-33)

analysis of the amplitude ...
the photogenerated holes.[5]

While the HEMTs operate at very high frequencies, trap level exist at the interfaces and in the high bandgap material. From the transients of the photocurrents, information on these levels can be obtained.[6,7]

Photoelectric measurements were also performed on fully fabricated InP based HBTs. In these measurements, we studied the photocurrent in the base-emitter and the base-collector junctions. Photocurrents arise from the electron-hole generation in the base and in the depleted junctions. Since backside illumination is used, the energy of the light has to be less than the bandgap of the InP substrate. From the spectral characteristics of the photocurrents and their dependence on the applied bias voltages, one obtains information on energy configuration of the junctions and on the material quality.

The HEMTs and the HBTs can be used as efficient photodetectors.[8,9] The use of these transistors as photodetectors allows the monolithic integration of analog and digital circuits with the photodetectors. No additional processing is required. Flip-chip bonding can be used to provide access to the backside of the chip. The HEMTs and HBTs are high performance devices and their operation as photodetectors reflect their electrical performance.

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[5] Fritz Schuermeyer, C. Cerny and M. Shur "In-situ characterization of lateral and vertical band structure profiles and hole storage effects in PHEMTs by the photoconduction technique", presented at the International Symposium on Compound Semiconductors (ISCS '96), St. Petersburg, Russia, September 23-27, 1996. Also published in Inst. Phys. Conf. Ser. No 155: Chapter 6, pp 495 - 498, 1997

[6] Fritz Schuermeyer, Charles Cerny and Chris Bozada "Charge Storage Effects in PHEMTs", presented at the Solid State Devices and Materials Conference (SSDM '96), Yokohama, Japan, 26 - 29 August 1996. Extended Abstracts Paper B-6-3, pp. 770 - 772

[7] Fritz Schuermeyer, Charles Cerny, Chris Bozada, Z-Q. Fang, and D.C. Look "Charge Storage Effects in Pseudomorphic High Electron Mobility Transistors", Jpn. J. Appl. Phys. 36, pp1330-1334, 1997

[8] Fritz Schuermeyer, Peter J. Zampardi and Peter M. Asbeck "InP-Based HBTs for Optical Signal Detection", presented at The Electrochemical Society Spring Meeting, San Diego, CA, 3 - 8 May 1998

[9] Fritz Schuermeyer "Optoelectronic PHEMTs", presentation at Optoelectronics '97, (SPIE), San Jose, CA, 8-14 February 1997. Proceedings 'Optoelectronic Integrated Circuits' SPIE Vol. 3006, pp110 - 117

In-situ Characterization Technique of Compound Semiconductor Device Processing Steps Based on UHV Contactless Capacitance-Voltage Measurement

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Heterostructure electronic devices such as HEMTs or HBTs are extremely sensitive to process induced defect states at surfaces and interfaces. Thus, *in-situ* non-destructive characterization of each processing step become indispensable for optimization of device fabrication. However, there exists no well-established method for characterizing the electronic properties of the "processed" semiconductor surfaces without changing surface properties.

In this paper, we present a novel characterization technique based on UHV contactless C-V measurement for compound semiconductor device processing which allows, for the first time, non-destructive investigation of the electronic properties of "processed" semiconductor surfaces.

(1) As shown in **Fig. 1(a)**, the principle of the contactless C-V method is to carry out C-V measurements from a field plate that is separated from the sample by a constant UHV gap of 100-300 nm. A constant UHV gap width was maintained by piezo-control and capacitance feedback. The completed UHV C-V chamber is shown in **Fig. 1(b)**. A special UHV transfer mechanism was developed to enable measurements on the processed samples that were attached on standard MBE sample holders for MBE growth. The system developed can be attached to various growth and processing equipments for electronic characterization of each processing step.

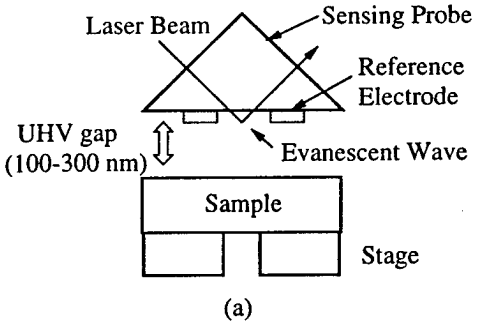
(2) The validity of this newly developed UHV C-V system was checked by using a standard SiO_2/Si MOS samples. For example, a pulsed C-V measurement and subsequent $1/C^2$-V plot on computer can determine the conduction type and carrier concentration profile of the wafer as shown in **Fig. 2**. Then, measurements were made on variously processed GaAs and InP surfaces.

(3) **Figure 3** shows the measured C-V curves of various MBE-grown GaAs surfaces. On the MBE-grown GaAs (2x4) surface, a very limited variation of capacitance was observed, indicating the presence of strong Fermi level pinning. From the flat capacitance, the pinning position was at E_V +0.6 eV. Then, passivation of the GaAs surface was attempted using an ultrathin silicon interface control layer (Si ICL) [1]. The contactless C-V curves of c(4x4) and (2x4)ß surfaces of GaAs after growth of the Si ICL and its partial nitridation are also shown in **Fig. 3**. A large capacitance variation could be obtained after growth of the Si ICL and nitridation on c(4x4) GaAs, indicating removal of surface Fermi level pinning due to reduction of surface states.

(4) **Figure 4** shows the contactless C-V curves of the surface of InP after HF treatment and thermal cleaning. After UHV thermal cleaning, poor C-V curve was obtained, although the oxide layer on surface mostly disappeared, as confirmed by XPS.

(5) **Figure 5** shows the effect of surface passivation by the Si ICL growth and its partial nitridation in terms of the minimum values of Nss calculated by applying the Terman's method on the measured UHV C-V curves. After HF treatment, Nss_{min} was $4x10^{11}$ $cm^{-2}eV^{-1}$. It slightly increased after thermal treatment, but remarkably decreased more than one order of magnitude after nitridation of the Si ICL. Thus, the new technique is extremely powerful for *in-situ* non-destructive characterization of each device processing step.

[1]H. Hasegawa, M. Akazawa, K. Matsuzaki, H. Ishii and H. Ohno, Jpn. J. Appl. Phys. **27** (1988) L226



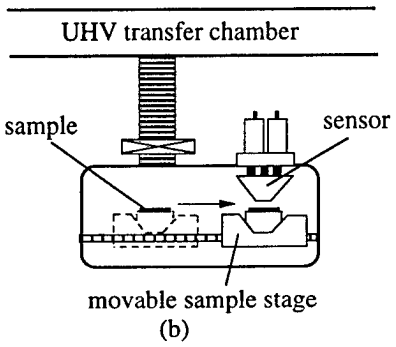


Fig. 1. Schematic illustration of Contactless C-V measurement system. (a) the sensor head and (b) UHV C-V chamber.

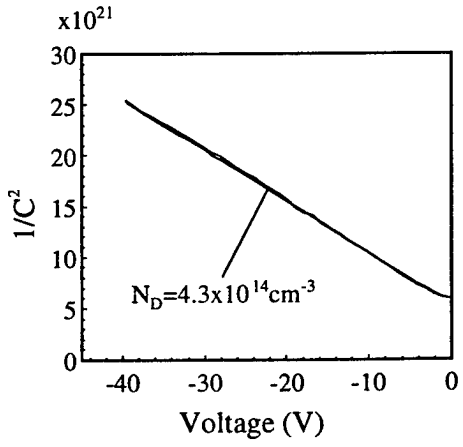


Fig. 2. $1/C^2$-V plot of pulsed C-V curve obtained from a Si surface.

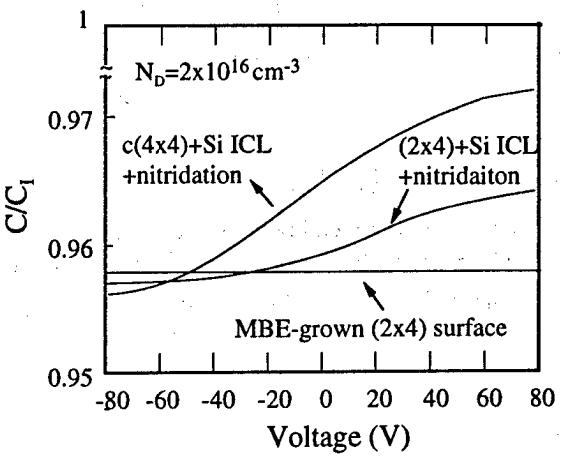


Fig. 3. Contactless C-V curves of MBE-grown GaAs surfaces.

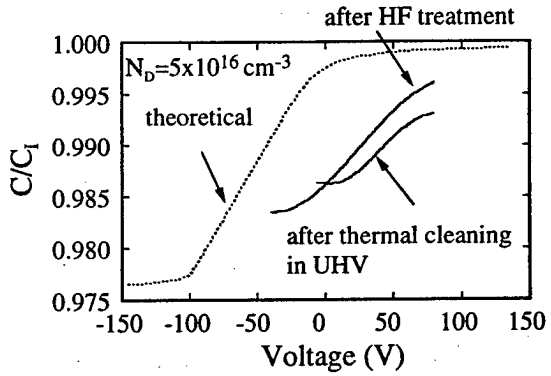


Fig. 4. Contactless C-V curves of InP surfaces.

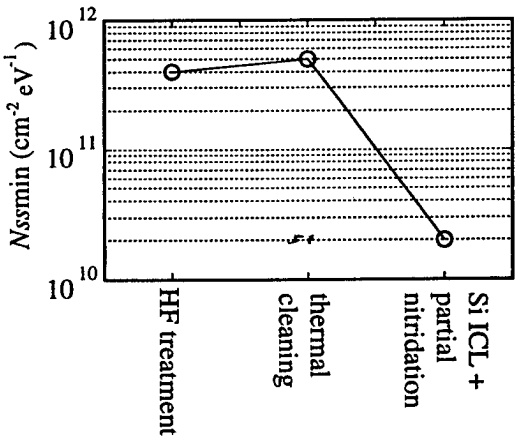


Fig. 5. Minimum values of *Nss* of InP surfaces after various surface treatments.

A Preliminary Study of MIS Diodes with nm-Thin GaAs-Oxide Layers

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1. Introduction : Schottky junction has long been used asthe gate structure of MESFETs and HEMTs. From view point of preventing tunnel current, MIS structure is more desirable than the Schottky junction, because the MIS has higher barrier than the latter, enabling thinner barrier layer. However, MIS structure compound semiconductor devices with nm-thin insulator layers have not been successfully realized. UV & ozone process is one of potential means to realize uniform and very thin oxidized GaAs layer. This paper reports a preliminary study of MIS diodes with nm-thin oxidized GaAs layers which being formed by UV & ozone process.

2. MIS HEMT : Figure 1 shows energy band structures of a Schottky HEMT and a MIS HEMT. As a typical barrier height of a Schottky junction is 0.7 eV, and that of a MIS is 3.9 eV (ex., Ni/Si), replacement of the semiconductor barrier with the insulator layer enables 1/2 or more reduction of the barrier thickness, without increasing the tunnel current. It consequently enables further down-sizing of the gate length. What indespensable for such MIS devices, but not realized, is process technique to form a very thin, uniform and reliable insulating layer on compound semiconductors.

3. Fabrication Process : We used n-GaAs(0.5 μm thick, 3 x 10^{17}/cc)/SI-GaAs epitaxial wafers. They were oxidized in dry oxygen atmosphere, at 300 ℃, under UV irradiation (SAMCO UV & Ozone Cleaner, UV-1), for 15～480min. XPS analysis of the oxidized layer of the 480 min. sample suggested distributions of atomic percentages of Ga, As, and O atoms as shown in Fig. 2. The As concentration is low near the surface region. The oxidized layers were partially removed by buffered fluoric acid in order to form MIS and Schottky diodes on each wafer. Figure 3 shows an AFM image of the border area of the 480 min. sample. Thickness of the oxidized layer were determined by AFM and shown in Fig. 4, in which Driad et al's data [1] are also shown by a thin line. The large spans of the measured thicknesses are partly due to incomplete wet process technique and partly due to roughness of the wafers surfaces. Ni with a diameter of 320 μm, as the Schottky contacts or M (of MIS), and AuGe as the ohmic contact were evaporated, both on the top surfaces, to form diodes.

3. I-V Characteristics : We measured the current-voltage characteristics of both of the Schottky diodes and the MIS diodes of each wafer. Figure 5 shows an example of the measured I-V curves of the Schottky and MIS diodes of the120 min. samples. It is observed that the current is suppressed by the oxide layer about 3 orders of magnitude in the reverse current and about 4 orders in the forward current. The strong voltage dependence in the reverse I-V characteristics of both of the Schottky and the MIS diodes suggests dominance of the tunnel currents [2, 3]. Figure 6 summarizes the current suppression rate vs. UV & ozone process time. Considering a forward/reverse current ratio of L/N InP HEMTs, it is presumed that the oxide layer must suppresses the current at least 4 orders of magnitude in order to replace the semiconductor barrier with the oxide barrier (Fig. 1). Figures 6 and 2 demonstrate that such current suppression effect is achieved by the process time of about 120 min. and the GaAs oxide thickness of 3～5 nm.

4.Conclusions : Oxidized GaAs layers, formed by UV & ozone proces, were studied. XPS analysis suggests that the composition of the oxide layer has depth dependence. The oxide thickness become 3～5 nm by the process time of 120 minutes. Under this condition, the oxide suppresses the current by 4 orders of magnitude.

Acknowledgment : The authors are grateful to Sumitomo Electric Industries and Mitsubishi Electric Corp. for supplying epitaxial GaAs wafers.

References
[1] R. Driad et al., Conf. Proc. of IPRM'98, p.459 [2] Putnum et al., Conf. Proc. of IPRM'97, p.197
[3] S. Takamiya et al., Solid-State Electronics, 42, 3, p447

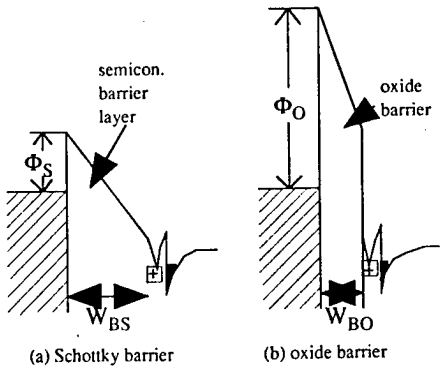

Fig. 1 Schottky HEMT (a) and MIS HEMT (b)

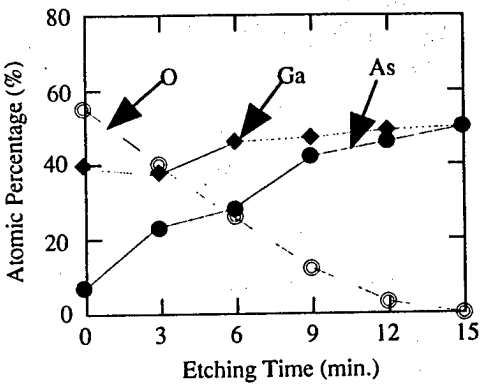

Fig. 2 Distribution of atomic percentage in the oxidized GaAs layer (8 hr sample)

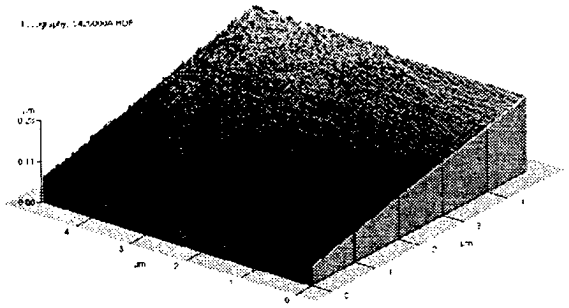

Fig. 3 AFM image of oxide edge portion of the 480min. sample.

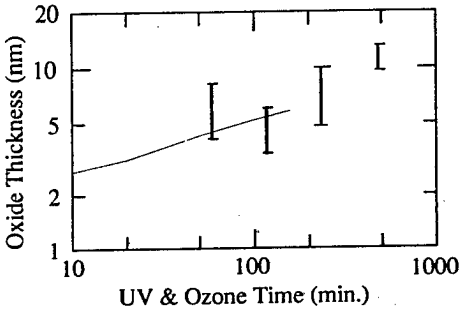

Fig. 4 Oxide thickness vs. UV & ozone time.

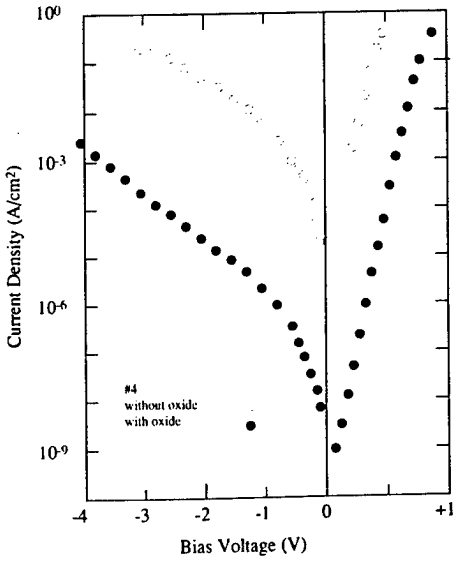

Fig. 5 Current vs. voltage of aSchottky diode (open) a MIS diode (closed) of 120 min. sample

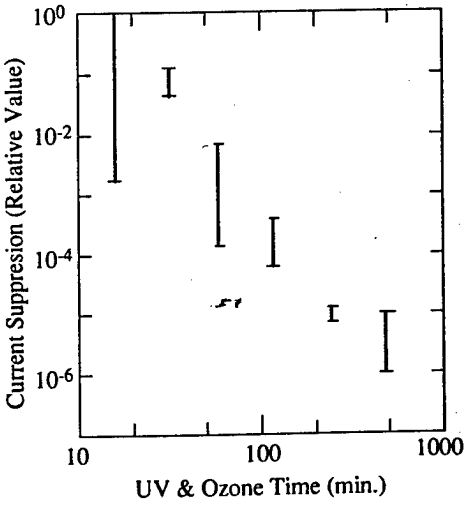

Fig. 6 Current suppression effect vs. UV & ozone process time.

Applications of HEMT Devices in Space Communication Systems and Equipment: A European Perspective

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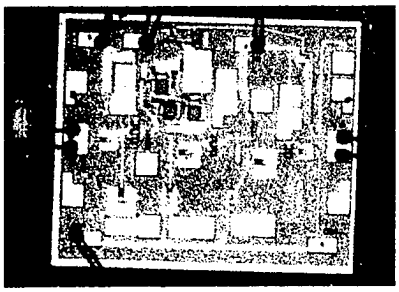
Abstract

In the last years the satellite applications have seen a strong increase in the space hardware demand mainly for commercial communication services like FSS, BSS and Mobile (MSS). The new boundary will be the low cost, high production rate hardware needed for satellite constellations and for Multimedia satellite-based systems. The design and development of microwave and millimeter wave equipment has been deeply modified in order to combine technical requirements and market needs. In this scenario the maturity of Gallium Arsenide MESFET and PHEMT devices and processes for space applications is a key factor and the design and integration of GaAs MMICs is mandatory to achieve the mentioned industrial drivers in the space companies. The paper will focus the application of GaAs MMIC technology in the European space industry taking as reference the space production done by Alenia Aerospazio in Italy and other European space companies and providing a future road map. As result of a fast evolution in the satellite commercial environment the payload complexity is growing with high number of channels either in transparent and regenerative architectures. While the payload complexity and the number of units per repeater is fast growing the required lead time is highly compressed, as consequence the technology solutions must address the miniaturisation issue, the design for production approach and the performance repeatability issue required for relative high volume productions. Only the massive use of MMIC technology allows to integrate complex microwave functions like LNAs, Front Ends, Receivers, Frequency converters, Channel amplifiers. Simple functions like Variable Gain Amplifiers, Flatness Correctors, Medium Power Amplifier, LNAs, Mixers and VCOs have been developed as building blocks and used in different configurations in the various modules and equipment. At present time low noise and power half micron MESFET and 0.25 μm PHEMT processes are used and are flying in space equipment produced by European companies [1,2]. MESFET process has been used to realize a Voltage Gain Amplifiers, medium power amplifiers and flatness corrector working in the bandwidth 10.7-12.7 GHz. PHEMT process has been used to realize LNAs and mixers working at Ku and K frequencies up to 18 GHz.

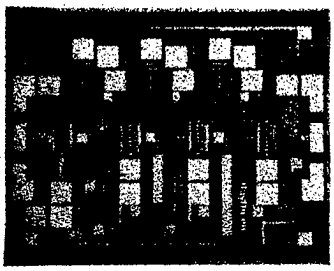
New satellite services (as multimedia transmission) require functions in the range from 20 to 30 GHz and a huge amount of equipment having small dimension and weight is foreseen for the next years. In this frame the application of MMIC technology to Ka family circuits appears again the winning solution. A standard 0.25 um low noise PHEMT process has been chosen to develop a complete MMIC family working at Ka band. Typical process parameter are: Ft = 50 GHz , minimum noise figure of 0.8 dB at 15 GHz, Idss=120mA/mm; Gmp=375 mS/mm; Vp=-0.7 Volts; Vbgd=-10.

The maturity of gallium arsenide technologies for space shapes in a complete different way the design approach, the manufacturing and the assembly techniques in design and development of flight units working in the microwave and millimeter wave frequency region. The processes currently used in the flight production are the well stable and high yield 0.5 μm low pinch-off MESFET, the 0.25 μm PHEMT and in the very next future the 0.15 μm PHEMT process. The Indium Phosphide (InP) based HEMT and HBT technology are becoming mature for space application and research and development activities are planned to prepare the second generation constellation systems that could make use the millimeter wave region (V-Band) for link communication as well as Inter satellite Link.

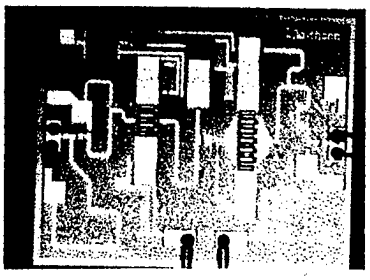
In this paper an overview of the latest technology in the microwave domain for space applications has been presented. The commercial telecommunication satellite application is a driving factor and the HEMT devices and MMIC technology are now massively used in the space hardware production. The trend is impressive in terms of weight, dimensions and recurring cost reduction. New family of components for Ka band systems are presented and a future road map for next generation constellation and millimeter wave systems is presented.



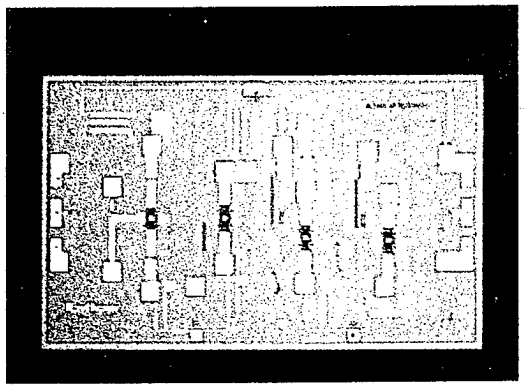
MESFET VGA

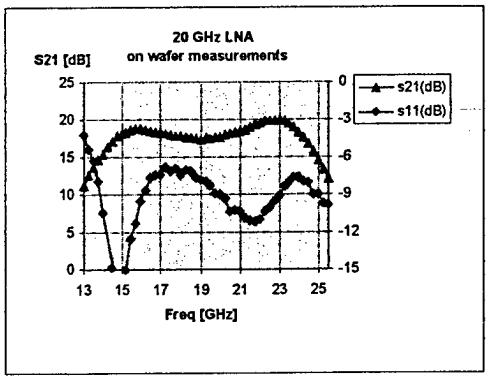


K Band PHEMT LNA

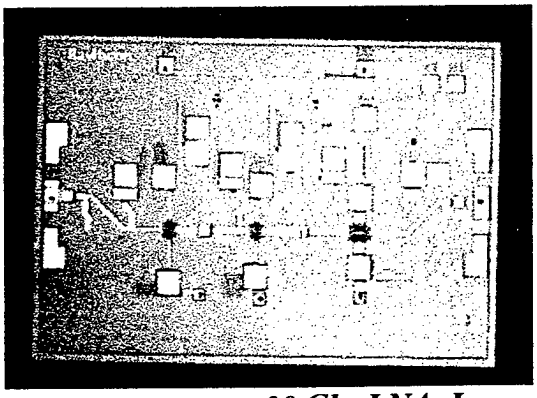


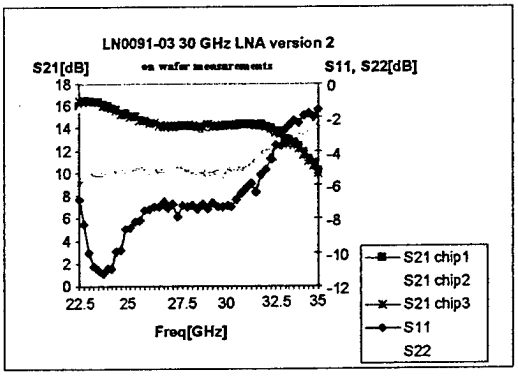
Ku Band MPA



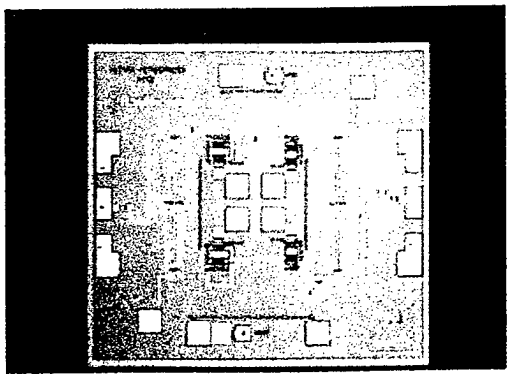


20 Ghz LNA: Layout and On Wafer Measurements

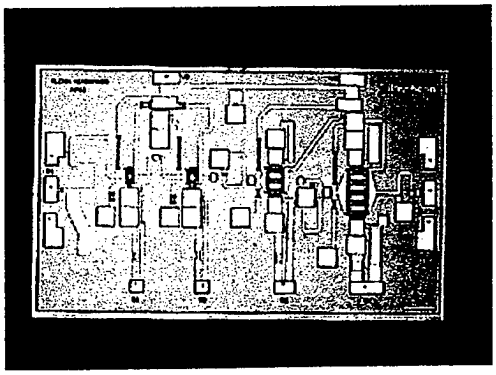




30 Ghz LNA: Layout and On wafer measurements



20 Ghz Variable Attenuator



20 Ghz Medium Power Amplifier

RF Device Trends for Mobile Communications

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1. Introduction

The younger consumers of today primarily desire smaller and lighter wireless mobile terminals with longer talking and standby time. RF IC technologies are of paramount importance as they represent the means by these requirements can be met. Both silicon and GaAs IC technologies have been pursued as solutions for use in wireless terminals. While GaAs ICs have met the technical requirements, their cost is considered to be relatively high for many wireless applications. In contrast, silicon ICs have found application for many of the low-tier products, but have failed to match the performance of GaAs ICs. In fact, a historical pattern has emerged with GaAs ICs winning the competition for initial high tier product introductions, but losing to silicon ICs for higher volume and lower cost products. In the next generation of wireless systems, this pattern may or may not repeat.

2. RF Device Markets

In 1996, the market for all semiconductor devices was 130 billion dollars as shown in Fig. 1 [Ref 1]. The RF device market was about 2.5 billion dollars, which accounted for only 2% of the entire semiconductor market. Silicon devices now occupy 60% of the RF device market, with GaAs device market accounting for 40%. The total GaAs device market, except for opto-electonics devices, is about 1 billion dollars, and GaAs ICs take up just about half of the total. The RF device market is considerable at 2.5 billion dollars, but it is a niche market in comparison with the whole semiconductor market. Handset sales are the primary engine of growth in the RF device market. The number of handsets for cellular and cordless phones reached 66 million units in 1996. Even so, their ranks continue to swell, and may reach 150 million units as soon as 2000. The number of handsets for digital systems exceeded that of analog systems in 1996.

3. Active and Passive Devices for MMICs

Figure 2 shows the trend of RF device cutoff frequency, f_T, in the 1990s. The horizontal axis is years and silicon CMOS technology size, and the vertical axis is f_T in GHz. We can see rapid f_T increase with MOSFET and PHEMT, but this may not be a good indication of their true potential. It may only be a reflection of researchers' enthusiasm supported by high market demand. It should be emphasized that other devices such as GaAs FETs and silicon bipolar transistors, or BJTs, have suffered a drop in market demand. The silicon complementary MOSFET, or CMOS, is the mainstream device of the semiconductor market. By the year 2005, CMOS technology should reach 0.1-μm dimensions with poly gates, and f_T of n-MOS will reach 100 GHz [Ref 2].

MMICs consist of active devices and passive matching circuits. Since reactive (L, C, R) matching provides the best NF (Noise Figure) and PAE (Power-Added Efficiency) performance as well as higher-frequency operation, most GaAs MMICs are designed by reactive matching. In designing conventional Si RF ICs, however, reactive matching cannot be effectively used, because comparatively high conductivity of Si substrate makes it impossible to employ high Q inductors and low-loss transmission lines.

One option to overcome the high attenuation transmission lines on silicon substrate is to use high-resistivity Si wafers. High-resistivity Si wafers are readily available with resistivities above 1000 ohm-cm. These wafers permit transmission lines to be built directly on the Si substrate in the same manner as they are in GaAs circuits. The attenuation per unit length of a CPW (Coplanar waveguide) is shown in Fig. 3 [Ref 3]. By comparing the CPW lines for Si and GaAs, it can be seen that the attenuation is high for moderate resistivity silicon, but that for 2500 ohm-cm silicon is approximately the same as that of similar lines on GaAs. The 3-D or multi-layer thin film technology effectively isolates the wafer properties from passive circuits. Figure 4 shows the structure of a Si 3-D MMIC [Ref 4]. By using the ground plane 1, or GND1, the conductive property of the wafer is effectively isolated from the passive structures created on GND1, and high Q passive circuits are available.

4. Conclusions

Both silicon and GaAs device technologies have been pursued as solutions to the problems inherent in wireless applications. In both technologies, there are tradeoffs between performance, cost, reliability, and time-to-market. Among the various devices, Si-MOSFETs, Si-BJTs, GaAs-MESFETs, P-HEMTs, GaAs HBTs are considered to be those which play the most important roles in the area of wireless terminals.

References

1. COMPOUND SEMICONDUCTOR (published six times yearly), Franklin Publishing, Saint Paul, MN.
2. P.K. Chatterjee and R. R. Doering, "Manufacturing Gigachips in the Year 2005" 1995 Symposium on VLSI Technology Digest, pp. 53-56, Kyoto, 1995.
3. G. E. Ponchak, A. N. Downey, and L. P. B. Katehi, "High Frequency Interconnects on Silicon Substrates," IEEE Radio Frequency Integrated Circuits Symposium, pp. 101-104, 1997.
4. I. Toyoda, K. Nishikawa, T. Tokumitsu, K. Kamogawa, C. Yamaguchi, M.Hirano, and M. Aikawa, "Three-dimensionalmasterslice MMIC on Si substrate," IEEE Radio Frequency Integrated Circuits Symposium, pp. 181-184, 1997.

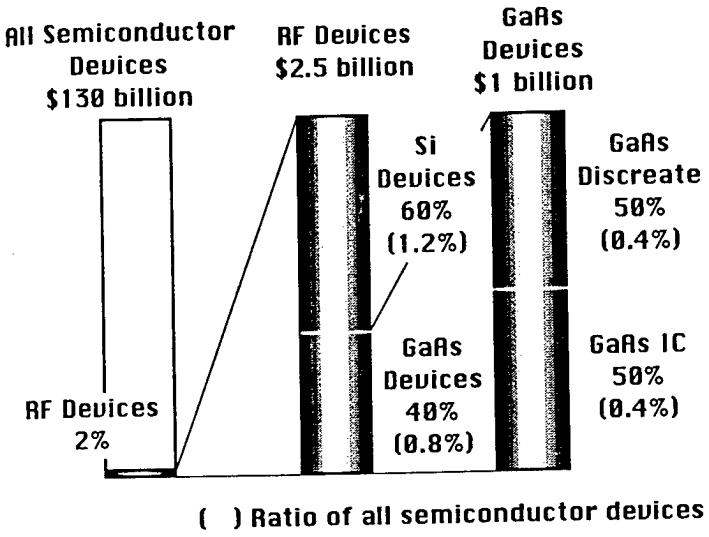

Fig. 1 RF Device Market (1996)

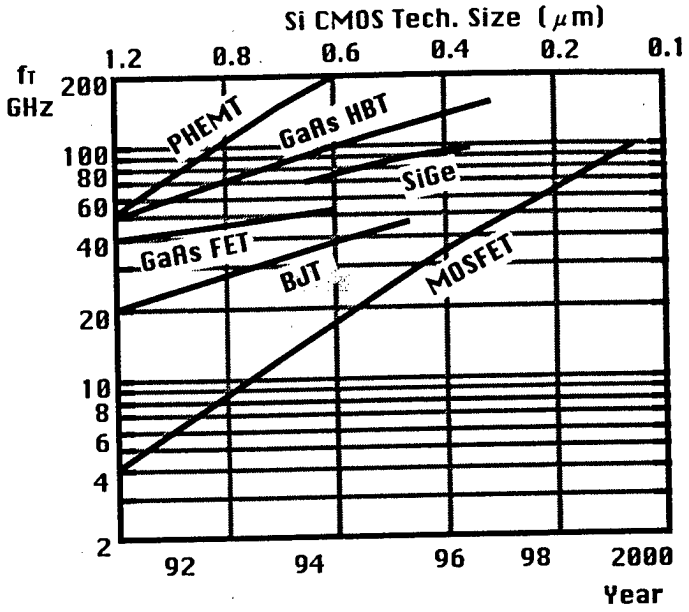

Fig. 2 RF device fT Trend

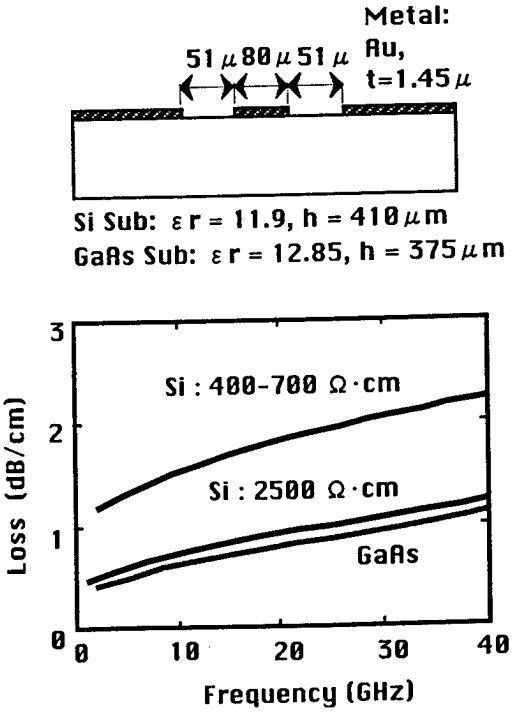

Fig. 3 Transmission Lines on Silicon Substrate

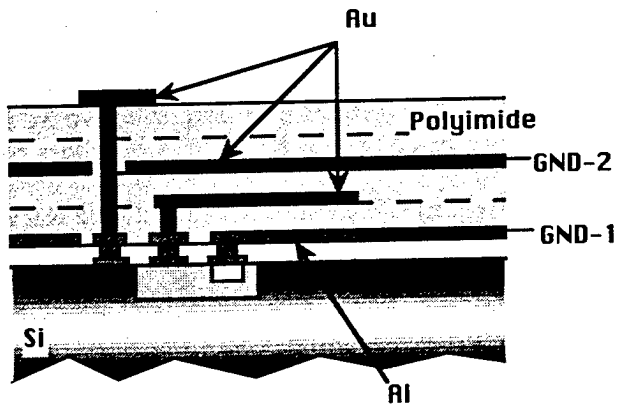

Fig. 4 3-D Passive Devices on Silicon Substrates

MM-Wave Integrated Circuits and Their Applications to Communication and Automotive Systems

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The wireless telecommunications are giving a formidable push to the GaAs MMIC industry. GaAs MMICs are now widely accepted by the high volume consumer market of mobile phone handsets. This application is at the low-end of the frequency range of interest for the GaAs technology which is engaged in a fierce price/performance competition with the Si or SiGe technologies. However, the mobile phone handsets at RF are not the whole story for GaAs and other volume applications - especially at millimetre-wave - are blossoming rapidly and for which the GaAs MMIC technology will have no alternative. Several applications are driving :

- Point-to-point radio links, for mobile phone base station networks. This market is already existing with an estimated today volume of the order of 200,000 radios installed per year worldwide. These telecommunication systems use various frequency bands from 7 to 60 GHz with 38 GHz becoming a standard.
- Point-to-multipoint radio links, for TV broadcast, video distribution, and interactive multimedia services (including telephone, video-on-demand, internet). Several services (LMDS) are already operating, especially in the US and in Canada at 28 GHz ; similar services are being actively developped in Europe at 41 GHz. The predicted market is very huge with an estimated number of above 10 millions of subscribers (each of them equipped with a mm-wave receiver - and a transmitter for interactive services) after 2000.
- Ka-band (20-30 GHz) communications using the satellite constellation systems (Teledesics, Celestri, ...). Considering that each constellation has more than 50 satellites and that active phased array concepts are used for the on-board receivers and transmitters, we come to very respectable numbers for the volume of MMIC chip-sets to be provided for the satellite payloads only, not talking about the ground equipments.
- Collision avoidance car radars at 76 GHz. The introduction on the market of the first generation of adaptative cruise control systems is just starting. These systems use mm-wave diodes, but cost effective MMIC solutions should rapidly take over, with a total volume above 1 million of radars per year before 2005.

We, in UMS, are devoting strong R&D efforts to address all these mm-wave applications, as we consider them to be our priority axis for business development. We are developing all the necessary mm-wave MMICs in order to build a complete catalogue of standard chip sets, including low-phase noise sources, LNAs, down-converters, up-converters, frequency multipliers and power amplifiers. Our technology work-horse is a pseudomorphic HEMT process family, with gate lengths of 0.25 µm (PH25) and 0.15µm (PH15) and with a variant (PPH25) for the power amplifiers.

The presentation will be illustrated by a detailed description of our development of the complete low-cost MMIC chip-sets which will equip the mm-wave front-ends (subscriber segment) for the 41 GHz European interactive LMDS application (also called MVDS). Figs 1 and 2 give the block diagrams and the pictures of the first generation of MMICs for both the receiver and the transmitter (return path) circuits.

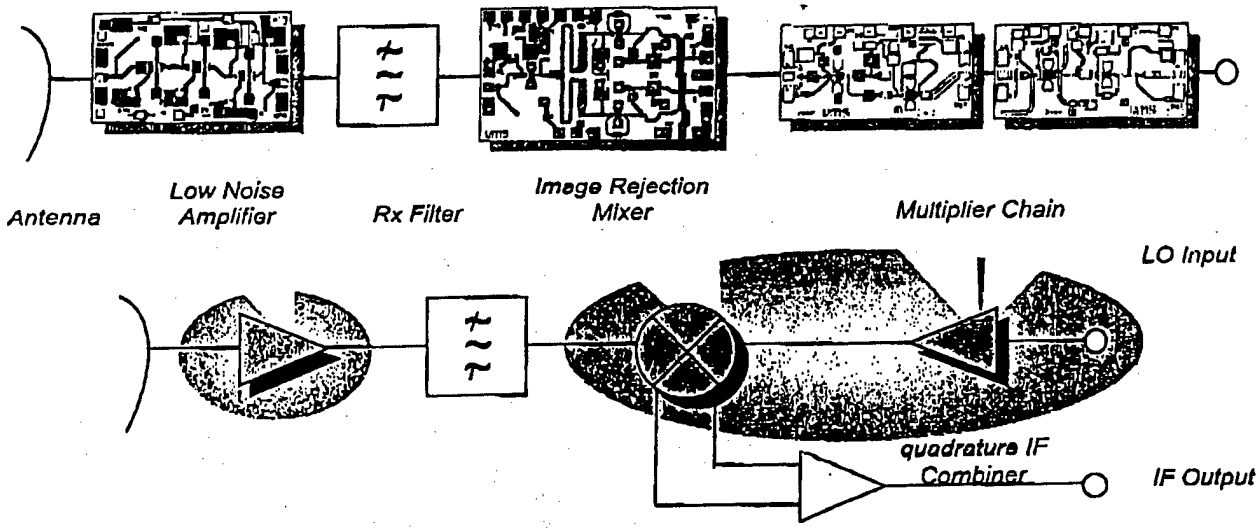

Fig. 1 : 41 GHz MVDS receiver block diagram and MMICs (subscriber unit)

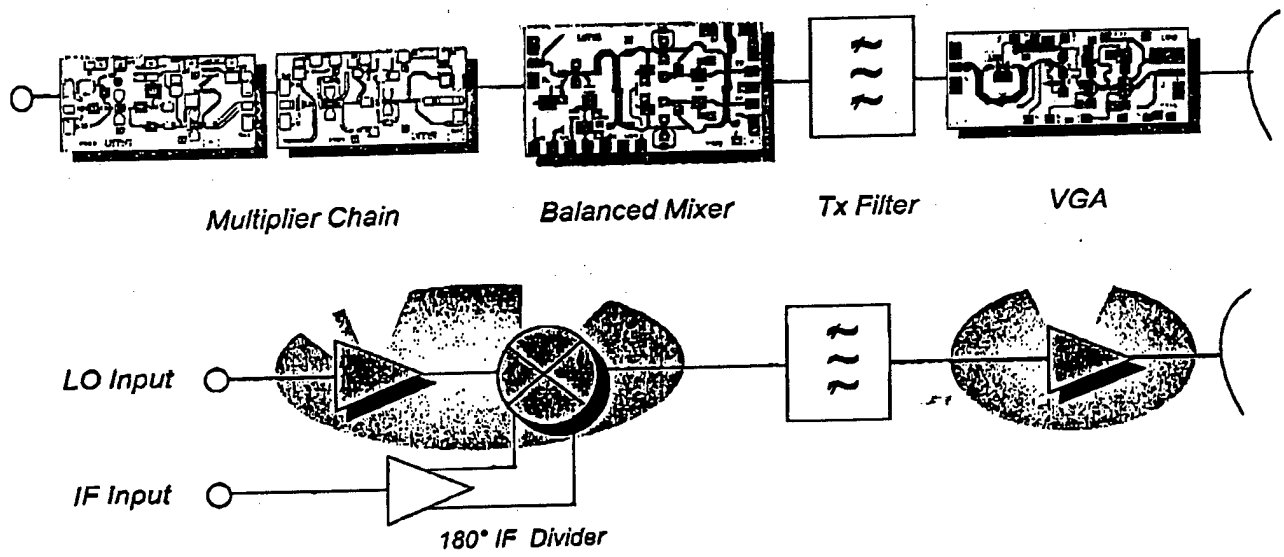

Fig. 2 : 41 GHz MVDS return path block diagram and MMICs (subscriber unit)

MM-wave HEMT based Circuits and Their System Applications

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While mobile communication in the low GHz regime is promoting the use of microwave systems on a large market scale millimeter-wave systems are now also being developed for use in civil systems with potentially high production volumes. This especially holds for radar based sensor systems to be used in cars for intelligent cruise control or collision avoidance systems, but also for advanced communication systems. With increasing requirements concerning reduced power consumption and -- forced by environmental considerations -- reduced RF-power level and higher frequency bands it becomes reasonable to consider supplements to the well established GaAs technology. InP-HEMT based components will have the potential to improve the performance of present systems in terms of power consumption, sensitivity, required chip area per function and since they show comparable electrical performance to their GaAs counterparts at larger gate geometry they offer reduced fabrication costs. Moreover they open higher frequencies to be used for advanced and novel systems. The two high volume markets are mobile communication and automotive sensors for intelligent cruise control and collision avoidance.

The drastic increase in subscribers in mobile communication systems and thus the dramatic increase in data density opens a new field for mm-wave HEMT components: mm-wave basestations. Between 23 GHz and 55 GHz several new communication systems for wireless LANs or for connecting the base stations of mobile Telephone systems are developed. In the 60 GI-Iz range one will find for example military communication systems and some applications for intersatellite communication links. The potential benefit for these systems by use of InP HEMT based MMICs becomes most pronounced with increasing frequency.

Automotive mm-wave radar sensors for intelligent cruise control or collision avoidance systems are realized for a frequency range of 76 to 77 GI-Iz. Presently GaAs MMICs or even discrete devices are used for first systems. Two reasons might enforce the use of InP-based MMICs for these applications: Demand for increased receiver sensitivity or the use of higher frequencies. The demand for increased sensitivity might aase from regulations satisfying environmental considerations. Higher frequencies up to at least 140GHz are envisaged for advanced sensor systems with higher resolution and imaging capabilities, leading to smaller size of the antenna or increased resolution for identical size. These applications will require arrays of T/IR modules, leading to higher "pixel" like resolution. Other applications may be mm-wave phased arry systems. The advantage using InP-based devices is the very low power consumption, the higher power added efficiency of InP-based amplifiers and the possibility of using Schottky-mixer diodes with very low tum-on voltages. To achieve the required resolution for those systems one needs very high frequencies which can only comfortable be covered by InP-based components.

The electrical functions for which InP HEMT-based devices are ideally suited for are buffer, low-noise and power amplifiers where the frequency range and system requirements are determining the economical usefulness of its development. With InP-based HEMTs the lowest noise figures and highest operating frequencies have been achieved. With 0.2pm T-gates for our HEMT devices a minimum noise figure of NF(f=18GHz) = 0.6dB with an associated Gain of G,=11dB, unit current gain cut-off frequency f_T=110 GHz and maximum power gain cut-off frequency of f_{max} >400GHz have been determined. This data is suffizient as a design base for most amplifier circuits.

While in the past mostly microstrip lines (MSLs) have been used in MMICs as the transmission media, coplanar waveguides (CPWs) are now becoming an interesting alternative due to the dramatic advantages with respect to MMIC-fabhcation (no substrate thinning, no via holes, no backside metallization hence much faster through-put) and design simplicity. Moreover they show better electrical behavior (lower grounding parasitics, lower dispersion). Fig.1 and 2 show some examples of low noise amplifier MMICs realized using CPW technology from Daimler-Benz.

The higher thermal conductivity of the InP (40 O/o higher than GaAs), the higher sheet carrier density, and the higher electron velocity in the channel results in superior power performance at higher frequencies especially in the higher mm-wave range f>50GHz. So f.e., at 94 GHz an output power of 21 dBm with 4 dB gain and a power added efficiency of 13 O/o were achieved [11].
Concerning signal-pathing one finds different approaches like circulators or switches. Using InPbased HEMTs as quasi active circulators is an interesting approach for fast signal directing. At Kaband we have realized an active circulator using InP-HEMTs with an insertion loss of 5 dB and an isolation of -30 dB [2].
More detailed discussion with respect to applications will be given at the workshop.

[l] C. Chen et **al.,** "A 94-GHz 130-mW InAlAs/InGaAs/InP HEMT High-Power MMIC Amplifiers', IEEE Microwave and Guided Wave Lett., Vol.7, No.5, pp.133-135,1997

[2] M. Berg et al., "Active Circulator MMIC in CPW Technology Using Quarter Micron InAlAs/inGaAs/InP HFETs", Proc. of the 8th Intern. Conf. on Indium Phosphide and Rel. Materials, Schw_bisch Gm_nd, Germany, pp. 68-71, 1996

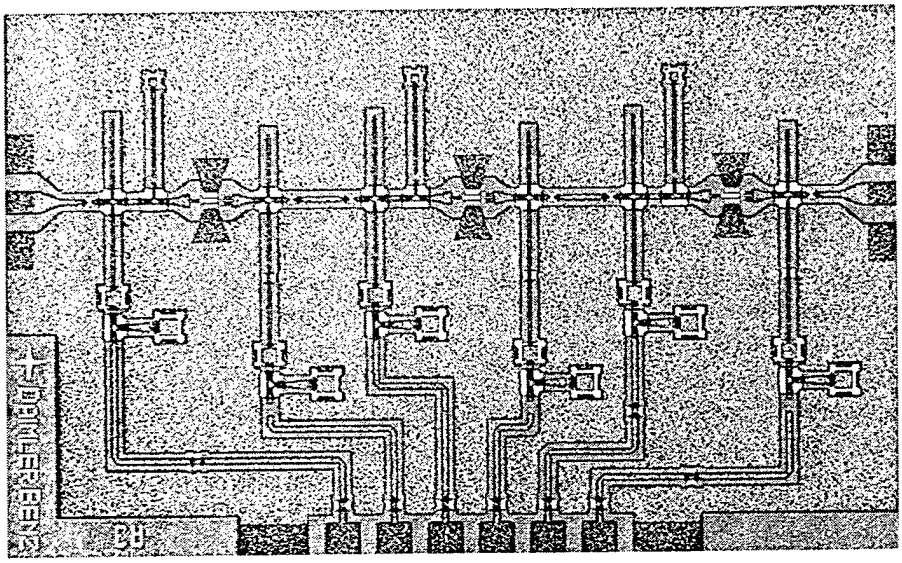

Fig. 1: 3-stage amplifier for 77GHz operation using 0.25pm InP-HEMTs. NF=5.8dB, Ga=15dB.

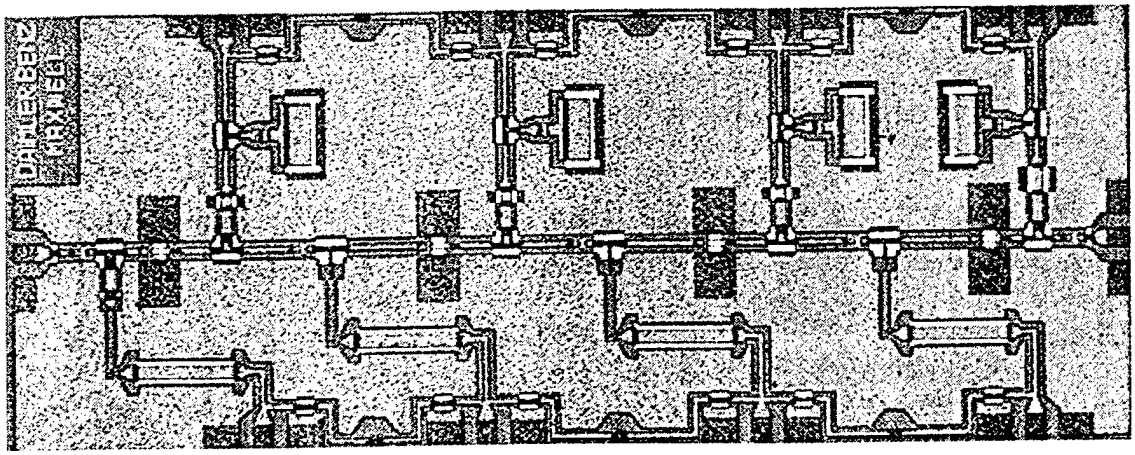

Fig.2: 4-stage amplifier for 80-100 GHz operation using 0.25pm InP-HEMTs. NF=7dB, Ga= 3dB.

Technologies for making full use of high-speed ICs

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1. Introduction

As multimedia services become more sophisticated, there is an increasing call for greater transmission capacity. High-speed optical fiber communication systems are being intensively developed to cope with these demands. A 40 Gb/s system is one research target and some experimental results have already been reported. At these very high speeds, technologies are desired that make full use of the performances of devices. This paper introduces ways to obtain, from high speed IC modules, the high performance needed when these modules are used in equipment operating at 40 Gb/s and above.

2. IC design for high-speed operation

It is known that the transistor cutoff frequency f_T must be three to four times greater than the operating bit rate for wideband analog circuits (baseband amplifiers) and some digital circuits (such as D-F/Fs). Because the f_T obtained so far is around 100 GHz, there is a need for a circuit design that offers broader bandwidth operation at 40 Gb/s and above. Using a distributed amplifier configuration is one approach to extending the analog circuit bandwidth (Fig. 1). Figure 2 shows an example of the frequency response for a packaged 3-stage distributed amplifier. In order to obtain a flat response from almost DC to 40 GHz, frequency dependent termination was applied in both the input and output transmission lines, in addition to the matching stubs. Moreover, in order to obtain good performance after packaging, the effect of the outer bonding wires was taken into account when the circuit was being designed.

The operation speed of digital ICs can also be improved by using new circuit configuration. Reducing the internal clock speed is one typical approach.

3. Package design

In order to take full advantage of the performance of the high-speed IC chips, the

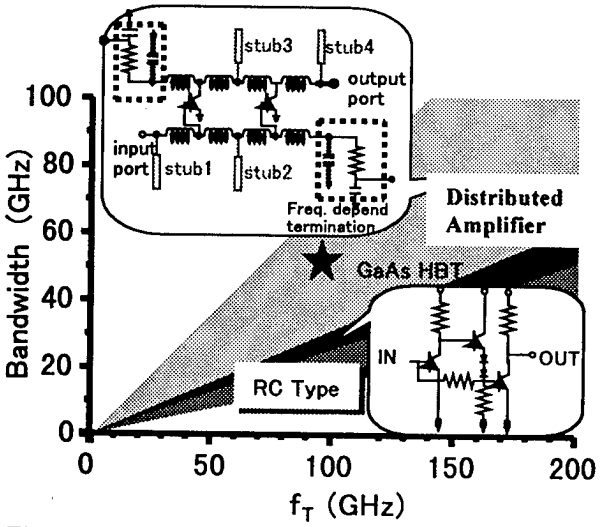

Fig.1 Distributed amplifier for broader bandwidth

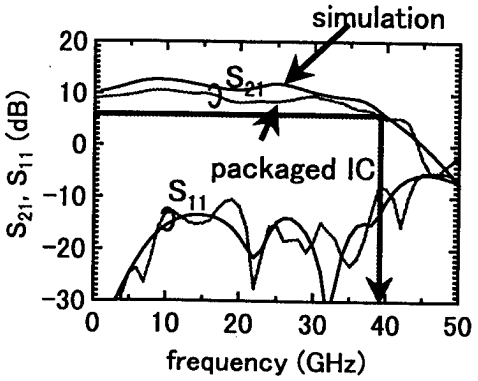

Fig.2 Frequency response for distributed amplifier

package must be designed with care. The cavity influence must be taken into account in the three-dimensional package design. The RF signal line must also be designed so that a high-speed signal can be output. Figure 3 shows an example of the RF feed through line geometry design. To connect the small IC pad to the module outer pin, transformation from coplanar line to strip line is applied. As a result, broadband connection with very low reflection was realized at the 40-GHz range and beyond.

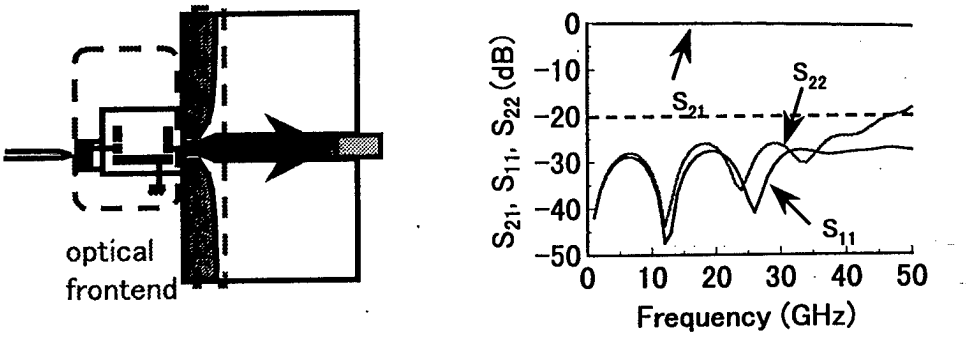

Fig.3 RF signal line for use in the high-speed IC module

4. Compatibility with optical devices

For optical transmitter and receiver, overall design is necessary including optical devices. For the transmitter, driving an optical modulator with a large voltage swing is the most critical issue. A low-driving-voltage optical modulator is needed, as is a large output voltage driver circuit.

For the receiver, transimpedance performance must be designed with a photodetecter (PD), which is basically a current source with stray capacitance. Connection between the PD and IC is an issue. Short bonding wire may still be usable for 40-Gb/s operation. The OEIC approach will likely offer better performance. However, in order to obtain the best performance from optical and electrical devices, further study is required.

5. Conclusion

Practical technologies are being developed so that packaged ICs can operate at speeds of IC performance limit. Figure 4 shows that a receiver is capable of operating at 40 Gb/s. These technical advances will accelerate the deployment of ultrahigh-speed optical communication for next-generation multimedia networks.

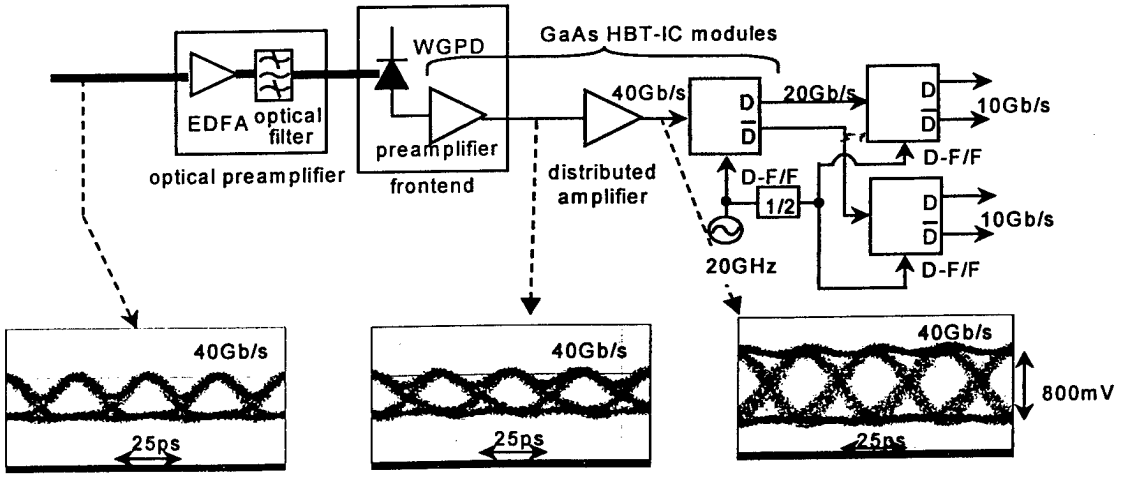

Fig. 4 40Gb/s optical receiver with GaAs HBT-IC modules

SiGe HBTs and Circuits for Optical Fiber Communication Systems

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Ultra-high-speed transistors are essential for future optical-fiber communication systems operating at 10 Gb/s and over. A SiGe-base heterojunction bipolar transistor (HBT) is a very attractive candidate to achieve fast base transit time, and a cutoff frequency of over 100 GHz [1] has been reported. To provide ultra-high-speed operation for 40-Gb/s and/or millimeter-wave systems, however, low parasitic capacitance and low parasitic resistance must be achieved simultaneously. Self-aligned stacked metal/*in-situ* doped poly-Si (IDP) (referred to as SMI) electrode technology is very suitable for obtaining high-speed performance, i.e. 12-ps ECL gate delay and a 45-GHz dynamic frequency divider in an implanted base [2]. In SMI technology, tungsten films are stacked on IDP electrodes in a self-aligned manner using selective deposition without any heat treatment, which prevents unwanted diffusion of the base dopants and keeps a shallow intrinsic base profile. Therefore, a self-aligned selective-epitaxial SiGe-base HBT with SMI electrodes has been demonstrated [3, 4].

An SEM cross-section of a self-aligned selective-epitaxial SiGe HBT with SMI electrodes is shown in Fig. 1. The 0.54-μm-wide SiGe-base and Si-cap multilayer, self-aligned to the 0.14-μm-wide emitter, was selectively grown by using a UHV/CVD system. This self-aligned structure is very effective for reducing collector capacitance. To obtain high-speed characteristics, the 20-nm-thick $1x10^{19}$-cm^{-3}-boron-doped selective-epitaxial $Si_{1-x}Ge_x$ layer with a 10-nm-thick two-step-ramped Ge-profile (from 0 to 10% over 5 nm and from 10 to 15% over 5 nm) was used to an intrinsic base as shallow as 30 nm. A low thermal cycle process also enabled a shallow emitter junction depth of 20 nm (Fig. 2). To reduce the parasitic resistances of the base, emitter, and collector, tungsten films were selectively stacked on *in-situ* boron-doped poly-Si (IBDP) as the base electrode, and on *in-situ* phosphorous-doped poly-Si (IPDP) as the emitter and collector electrodes, in a self-aligned manner. Moreover, a 2-μm-wide BPSG-refilled trench was introduced to reduce the substrate capacitance.

A high current gain of 720 with a low base-recombination current of below 100 pA was obtained. This indicates there were no defects in or relaxation of the strained Si/SiGe multilayer. The collector current was defined by the SiGe-graded drift field, so the Early voltage was high enough — more than 100 V (Fig. 3). The cutoff frequency and the maximum oscillation frequency of the transistors, whose emitter area was 0.14 x 1.5 μm^2, were 95 GHz and 97 GHz at a collector-to-emitter bias voltage of 2 V and a collector current of 2 mA, respectively (Fig. 4). Typical transistor characteristics are summarized in Table 1. The low collector capacitance of 3.6 fF and low substrate capacitance of 0.6 fF at a reverse bias voltage of 5 V are attributed, respectively, to the fully-self-aligned SiGe base structure and the wide SiO_2-refilled trench. The emitter resistance of 50 Ω, despite the very narrow 0.14-μm-wide emitter, is attributed to the stacked tungsten/IDP emitter electrode. The dependence of the gate-delay time on the switching current in 45-stage differential ECL ring oscillators at a single-ended voltage swing of 250 mV is shown in Fig. 5. A record ECL gate-delay time of 8.0 ps for Si technology was measured.

As an example of an IC for optical-fiber-link systems, a chip micrograph of a 1/8 static frequency divider is shown in Fig. 6. The highest maximum operating frequency reported to date for any semiconductor technology, up to 50 GHz, was obtained. Furthermore, a time-division multiplexer and a demultiplexer operating at 40 Gb/s, a preamplifier with a bandwidth of 35 GHz, an AGC amplifier core with a bandwidth of 32 GHz, and a decision circuit operating at 40 Gb/s have been developed [4, 5]. These excellent results show that Si bipolar technology, which offers high reliability and cost-effectiveness, will play an important role in future optical-fiber-link systems operating at a data rate of 40 Gb/s for global communications applications.

[1] K. Oda, E. Ohue, M. Tanabe, H. Shimamoto, T. Onai, and K. Washio, "130-GHz f_T SiGe HBT Technology," in *IEDM Tech. Dig.*, pp. 791-794, 1997.

[2] K. Washio, E. Ohue, M. Tanabe, and T. Onai, "Self-Aligned Metal/IDP Si Bipolar Technology with 12-ps ECL and 45-GHz Dynamic Frequency Divider," *IEEE Trans. Electron Devices*, vol. 44, no. 11, pp. 2078-2082, Nov. 1997.

[3] K. Washio, E. Ohue, K. Oda, M. Tanabe, H. Shimamoto, and T. Onai, "A Selective-Epitaxial SiGe HBT with SMI Electrodes Featuring 9.3-ps ECL-Gate Delay," in *IEDM Tech. Dig.*, pp. 795-798, 1997.

[4] K. Washio, E. Ohue, K. Oda, M. Tanabe, H. Shimamoto, and T. Onai, "95 GHz f_T Self-Aligned Selective Epitaxial SiGe HBT with SMI Electrodes," in *ISSCC Digest of Tech. Papers*, pp. 312-313, 1998.

[5] T. Masuda, K. Ohhata, E. Ohue, K. Oda, M. Tanabe, H. Shimamoto, T. Onai, and K. Washio, "40 Gb/s Analog IC Chipset for Optical Receiver using SiGe HBTs," in *ISSCC Digest of Tech. Papers*, pp. 314-315, 1998.

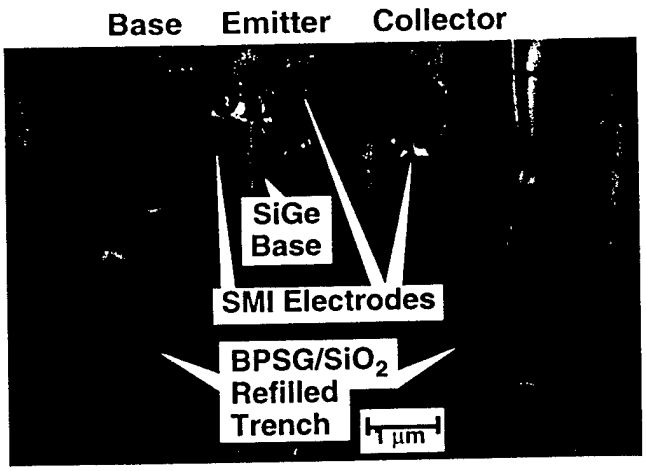

Fig. 1. SEM cross-section of a self-aligned SEG SiGe HBT.

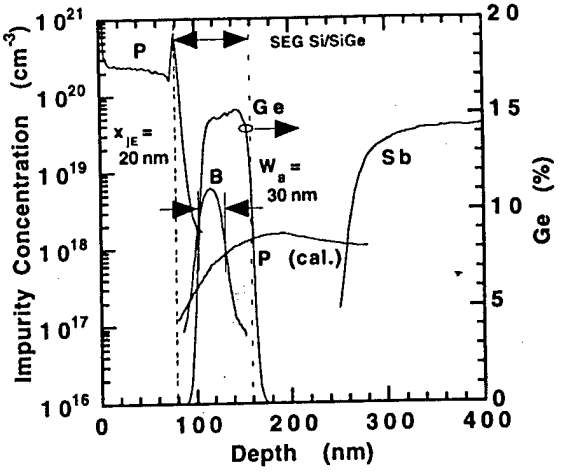

Fig. 2. Impurity profile of the intrinsic region.

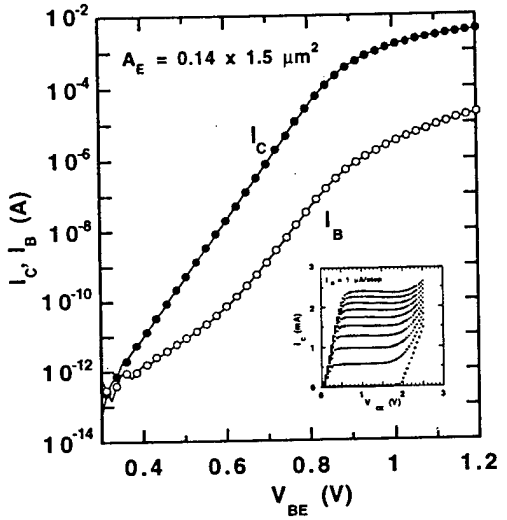

Fig. 3. Gummel plot and I-V characteristics.

Table 1. Typical transistor characteristics.

h_{FE}	720	
BV_{CEO}	2.0	V
V_A	>100	V
R_E	50	Ω
R_B	210	Ω
C_{jC}	3.6	fF
C_{SUB}	0.6 (5 V)	fF

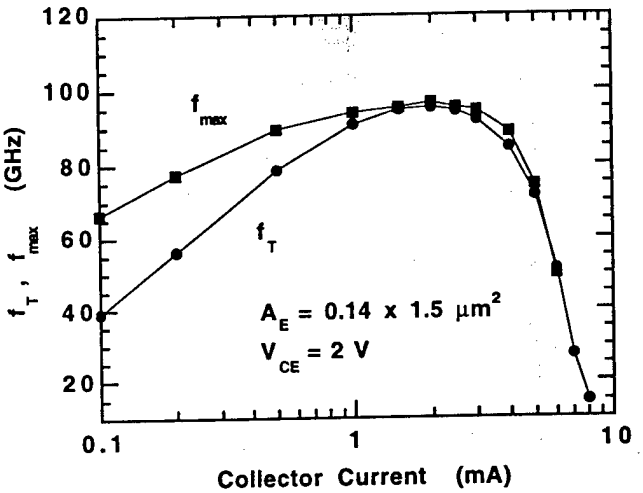

Fig. 4. Cutoff and maximum oscillation frequencies.

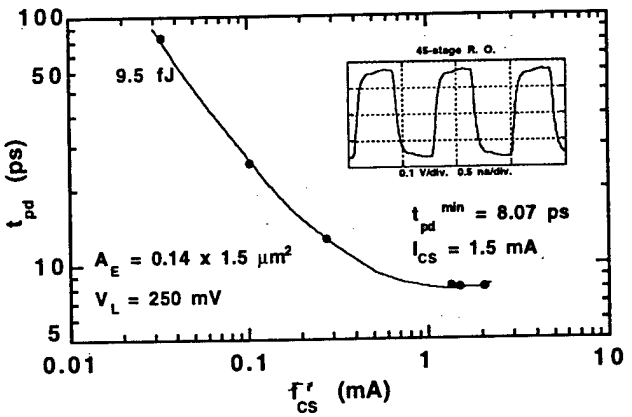

Fig. 5. Differential ECL gate delay performance.

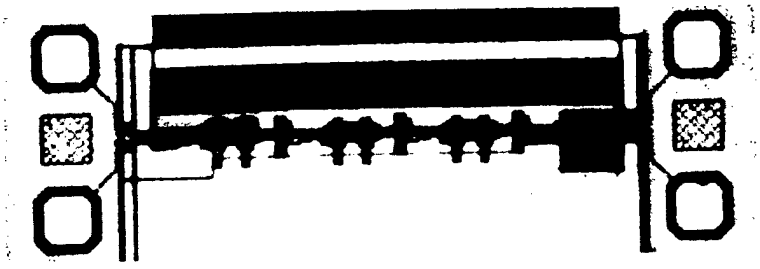

Fig. 6. 1/8 static frequency divider.

Heterostructure Circuit Applications in Optical Communications

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In the last few years, the evolution of large capacity optical networks, due to the ever increasing demand for more bandwidth, has been basically progressing in two directions: high-speed time division multiplexing (TDM) and wavelength division multiplexing (WDM). In TDM systems, high-speed optoelectronic processing exists between source and destination of the optical signals. The complete optical repeater contains components that perform reshaping, time extraction and signal regeneration (the so-called 3R-repeater for reshaping, retiming and regenerating). In the design of such optical repeater, the optimum performance depends on maximizing the speed of each individual circuit, which is primarily limited by the transistor technology used.

On the other hand, WDM systems have become a great successful story for solving the bandwidth crunch. Since WDM uses multiple channels, the systems provide aggregated speeds much higher than those obtained for single channel TDM with fewer demands on the electronic components. However, while the optical signals may propagate through either ring or mesh network architectures without the need for optical repeaters, there are some limitations that impair the ultimate capacity. These impairments arise mainly from optical phenomena, imposing a limitation on the network capacity and requiring dispersion compensation techniques, that does not require electronics [1].

With the development of broadband erbium doped fiber amplifiers, simultaneous amplification of both high-speed TDM and WDM signals are now possible [2]. So future optical networks can be a hybrid mixture of TDM and WDM technologies with fiber dispersion management and depending on the architecture, may include interfaces with high-speed cross-connects or electrical crosspoint switches [3].

In this talk, I will review the state-of-the-art of integrated circuit technologies, focusing mainly on heterostructure transistors-based circuits that have potential applications for TDM and WDM networks [4-6].

References

1. R.W. Tkach, E.L. Goldstein, J.A. Nagel and J.L. Strand, "Fundamental Limits of Optical Transparency," *Optical Fiber Communication Technical Digest*, pp. 161-162, 1998.
2. Y. Sun et al, "Ultra Wide Band Erbium-Doped Silica Fiber Amplifier with 80 nm of Bandwidth," IEEE *Photonic Technology Let.* Vol. 9(12), pp. 1652-1654, 1997.
3. R. Yu et al, "HBT Devices and Circuits for Signal and Data Processing," *Solid State Electronics*, Vol. 41(10), pp.1419-1431, 1997.

4. T.Otsugi, K. Murata, T. Enoki and Y. Umeda, " 80 Gbit/s Multiplexer IC using InAlAs/InGaAs/InP HEMTs," *Electronics Let.*, Vol. 34(1), pp. 113-114, 1998.
5. B. Agarwal, D. Mensa, Q. Lee, R. Pullela, J. Guthrie, L. Samoska and M.J.W. Rodwell, "A 50 GHz Feedback Amplifier with AlInAs/GaInAs Transferred-Substrate HBT," *IEEE IEDM Technical Digest*, pp. 743-746, 1997.
6. K.S. Lowe, " A GaAs HBT 16 x 16 10-Gb/s/Channel Crosspoint Switch," *IEEE J. of Solid State Circuits*, Vol. 32(8), pp.1263-1268, 1997.

"Heterostructure-based high-speed/high frequency electronic circuit applications"

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With the growth of Wireless and Lightwave technologies, heterostructure devices are commodity items in the commercial marketplace. In particular, HBTs are an attractive device for handset PA's at 900 MHz and 1.9 GHz for CDMA applications. At higher frequencies, both HBTs and p-HEMTs are expected to dominate the marketplace. For high-speed lightwave circuit applications, there are HBT based products on the market for OC-48 (2.5 Gb/s), OC-192 (10 Gb/s), with 40 Gb/s demonstrated at a number of research laboratories. Another area where heterojunction devices are having significant impact is for data conversion. We discuss the present and future trends of the heterojunction device applications to these areas.

Impedance matching, device bias, linearity, efficiency, substrate parasitics, output power limitations, and thermal limitations are *ALL* important considerations for power amplifiers. Once a technology sufficiently meets the requirements (Table 1) for the above areas, COST is the dominant factor in the selection of a power amplifier by a customer. Heterojunction Bipolar Transistors provide high gain, high linearity, and excellent efficiency for power amplification at 900 MHz and 1.9 GHz. Companies are shipping in excess of 1 million die per month in these markets. Due to the relative simplicity of the device fabrication and small physical device size (more chips per wafer), HBTs have proven themselves to be competitive on a cost basis with other technologies. In this presentation, we will discuss the relative merits of HBTs, FETs (Epi-FETs and p-HEMT), and silicon devices for these large (and still growing) commercial markets. We will also discuss the relative merits of heterostructure devices as the operating frequencies are increased and the supply voltages reduced.

High bit-rate communication systems require ultra high-speed electronics. There are many different technologies for the "low bit-rate" (<2.5 Gb/s) markets, including heterojunction devices. At higher bit-rates (>10 Gb/s) heterojunction devices can offer a full chip-set solution. Such systems (Fig. 1) include amplifiers, laser drivers, MUX/DEMUX, and clock and data recovery chips. Several companies have commercially available products at both the 2.5 Gb/s and 10 Gb/s using HBTs. HBTs (GaAs, SiGe, and InP) and HEMTs are currently the leading candidates for higher bit rate operation. We present and discuss both commercial and research circuits that address lightwave applications for 10 Gb/s and beyond, taking full advantage of the speed and performance of HBTs and HEMTs.

Data conversion circuits such as DAC's, ADC's, and DDS, are of great interest to military markets. HBT 12-bit 1 GHz DAC's are just one of the commercially available chips for data conversion. The large Early voltages, high-speed, and integrated high performance schottky diodes, make HBTs excellent devices for analog to digital conversion applications. The excellent device matching and high yield achievable with HBTs are also critical for these applications. We discuss several high-speed ADC's (Fig. 2) fabricated leveraging our commercial manufacturing facility. In addition to these applications, a direct digital synthesizer (>10,000 transistors) operating at speeds greater than 1.5 GHz has been demonstrated in this technology.

These application areas stress different elements of the rapid expansion of heterojunction devices into commercial markets. PA's demonstrate that HBTs are cost competitive with other technologies. Communications applications take advantage of the superior performance of heterojunction devices to ease the development and implementation of high-bit rate communication chips. Finally, data conversion applications that require excellent matching of characteristics (and accurate device models), high performance, and high yield for transistor counts >5000 transistors are readily achievable using current HBT devices.

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Operating Frequency Range	Fo	824		849	MHz
Gain * @ Po = 1 dBm	G	26.75	28.5	30.25	dB
Gain @ Po = 32 dBm	Gls	26			
Noise Figure	NF		<6	8	dB
Analog Mode Output Power	Po	1.5			W
Analog Mode Power Added Efficiency	PAE	46	50		%
Digital Mode Output Power	Pod	831			mW
Digital Mode Efficiency	PAEd	26	32		%
Adjacent Channel Power Rejection	ACPR				dBc
- 885 kHz Offset @ Po=28 dBm			-32	-28	dBc
- 1980 kHz Offset @ Po= 28 dBm			-46	-41	dBc
Supply Voltage	Vcc	4.8	5	6.5	V

Table 1. Electrical specifications for typical commercial CDMA PA

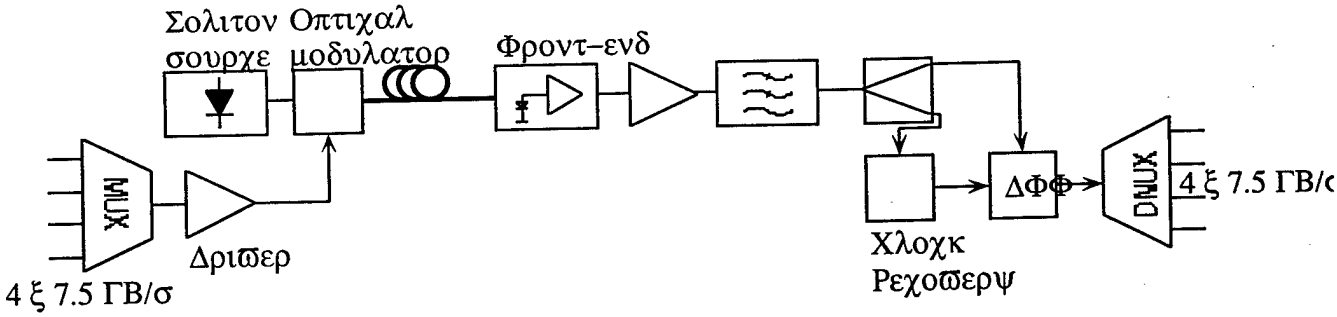

Figure 1. Schematic of fiber optic link. MUX/DEMUX, amplifiers and clock recovery at >30 Gb/s were demonstrated in HBT technology. The driver circuit was implemented in pHEMT

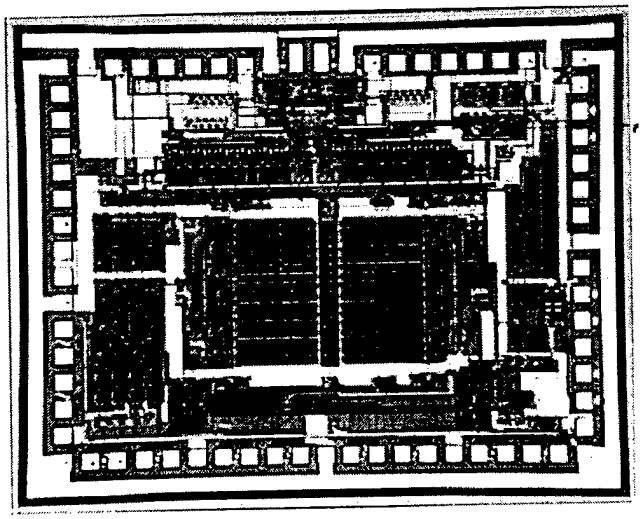

Figure 2. 8-bit 3Gsps ADC used in prototype digital receivers

A 0.1-μm MHEMT Millimeter-Wave IC Technology Designed for Manufacturability

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The need for a low-noise, high-performance FET MMIC technology for future communication and instrument applications can be met with a manufacturable metamorphic HEMT (MHEMT) process [1-4]. Low-cost rugged 3" GaAs substrates can be used to grow InP-type HEMTs, with excellent performance, yield, uniformity, and reliability at low-noise bias. The linearly-graded low-temperature buffer (LGLTB) used to grade the lattice constant from GaAs to InP [5] adds only in a minor way to the fabrication cost, while the seamless fit of the process with existing GaAs IC manufacturing infrastructure is an overriding economic advantage of this technology. Non-alloyed ohmic contacts, etch stop layers and a one-step e-beam T-gate process also add to the manufacturability [1].

The FET process and characteristics have been summarized in [1]. Examples of two circuits fabricated in this technology are shown in Figs. 1 and 2. The high V-band gain in Fig. 1 illustrates the potential of this technology for millimeter-wave applications. The divide-by-4 circuit in Fig. 2 was designed primarily to evaluate the yield of the MHEMT process with a more complex circuit for potential digital applications. As discussed in [1,3] we have seen no reduction in performance, yield or uniformity by using the GaAs+LGLTB as a substrate for InP-type HEMTs. Based on FET and circuit yield we estimate $5 \cdot 10^5$ cm^{-2} as the upper limit of the density (assumed uniform) of harmful threading dislocations. Thus the vast majority of the misfit dislocations are confined to the LGLTB.

At low-noise bias, the reliability of the MHEMTs [4] is comparable to that of HEMTs grown on InP [7]. Fig. 3 shows the MTTF Arrhenius plot for MHEMTs stressed at V_{ds}=1 V and I_{ds}=200 mA/mm. MTTF extrapolates to $7.5 \cdot 10^6$ hours at 125 °C channel temperature. At 220 °C channel temperature even low-noise biasing causes a significant (40-80%) increase in R_d (compared to 0-20% for R_s) [4]. R_d-degradation in these FETs at V_d >1.5V has been experimentally and theoretically correlated with impact ionization in the channel [8,9]. This is likely to be the case also at low-noise bias. While the impact ionization component in I_g is typically too low to be discerned, it has been shown theoretically to exist at V_d<1V [10]. Higher drain biases that are desirable for medium-power applications increase the impact ionization for both MHEMTs and standard HEMTs on InP. The sensitivity of the device to impact ionization can be reduced by optimized material growth. The amount of impact ionization can be reduced by optimized device structure. Since the MHEMT technology lets us choose the lattice constant, one approach is to choose an In mole fraction near 30%, where ΔE_c is maximum and E_g larger [11]. Another approach, applicable with both substrates, is to use a narrow recess in a depleted cap [12]. One drawback with both these approaches is that they require alloyed or sintered ohmic contacts. These typically have higher resistance, and are not as reproducible and easily implemented in manufacturing as the non-alloyed contacts presently used.

Even without considering long-term reliability, impact ionization has an important limiting effect on these narrow-bandgap FETs, whether grown on GaAs or InP. It determines the on-state destructive breakdown voltage $BV_{ds}^{(on)}(I_d)$, and renders the off-state breakdown voltage essentially irrelevant [9]. Comparison of the theoretical and experimental data in Fig. 4 suggests that $BV_{ds}^{(on)}(I_d)$ of these 53%-In FETs follows a locus of $\approx$10 mA/mm impact ionization current, independent of the primary drain current I_d. The 10-mA/mm secondary current corresponds to $\approx$1% of the full channel current. Fig. 4 also illustrates that the load-line for reliable operation cannot be based on the off-state breakdown voltage BV_{ds}^{G}.

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[1] H. Rohdin *et al.*, HP Journal, vol. 49, p. 37, 1998, http://www.hp.com/hpj/98feb/feb98a4.htm.
[2] J.G. Wang *et al.*, Tech. Dig. 1997 GaAs IC Symp., p. 74.
[3] H. Rohdin *et al.*, Proc. 1995 Conf. InP and Related Materials, p. 73.
[4] A. Wakita *et al.*, Proc. 1998 Conf. InP and Related Materials.
[5] A. Fischer-Colbrie *et al.*, 1993 Electronic Materials Conf., paper A4.
[6] C.J. Madden *et al.*, Dig. Tech. 1994 IEEE ISSCC, p. 178.
[7] T. Enoki *et al*, Proc. 1996 Topical Workshop on Heterostructure Devices, p. 92.
[8] A. Wakita *et al.*, Proc. 1997 Conf. InP and Related Materials, p. 376.
[9] H. Rohdin *et al.*, Proc. 1997 Conf. InP and Related Materials, p. 357.
[10] T. Suemitsu *et al.*, Proc. 1997 Conf. InP and Related Materials, p. 365.
[11] A. Cappy, Proc. 1996 Conf. InP and Related Materials, p. 3.
[12] H. Daembkes *et al.*, 1991 Proc. IEEE/Cornell Conf. Advanced Concepts High Speed Semicond. Devices and Circuits, p. 198.

[13] J. Urquhart *et al*, Semicond. Sci. Technol., vol. 5, p. 789, 1990.

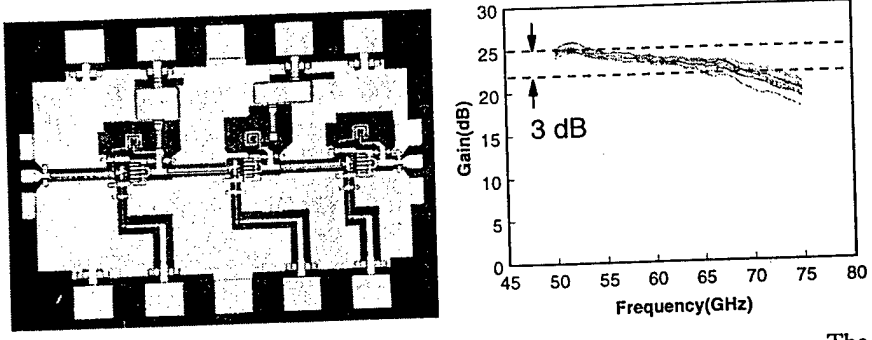

Fig. 1: MHEMT three-stage feedback amplifier and its V-band frequency response. The traces correspond to different circuits locations on the 2" wafer. The circuit design is based on [6].

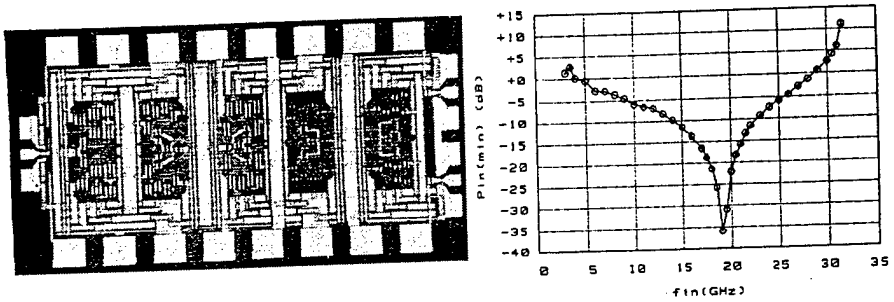

Fig. 2: Static 0.1-μm MHEMT divide-by-4 circuit with input sensitivity curve.

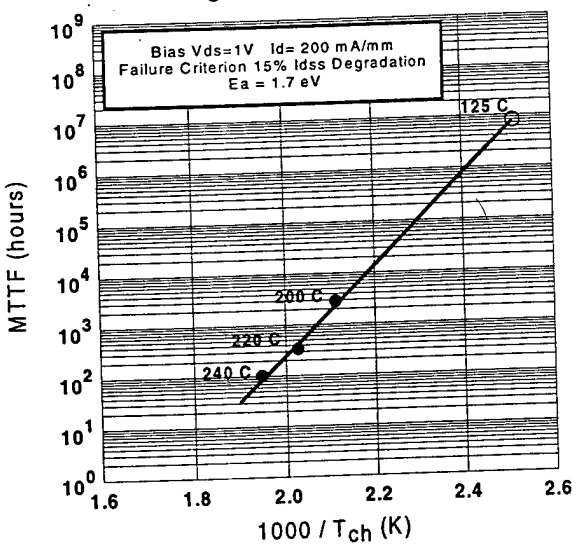

Fig. 3. MTTF Arrhenius plot for 0.1-μm MHEMTs. Solid circles are HTOL MTTF data for the failure criterion of 15% degradation in I_{dss}. The open circle is the extrapolated $7.5 \cdot 10^6$ hrs MTTF for 125 °C channel temperature. With g_m peaking near V_g=0V, I_{dss} degrades more rapidly than $I_d^{(max)}$ [4].

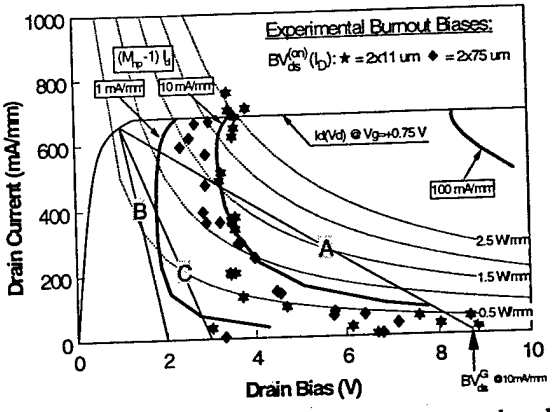

Fig. 4. Measured and modeled on-state breakdown voltage characteristics for 0.1-μm AlInAs/GaInAs/GaAs MHEMTs, modeled maximum current (V_g=+0.75 V), constant DC power loci (dotted lines), and three load-lines (A,B and C). The bold solid lines are calculated loci of constant impact ionization current as in [9], but with more accurate lower impact ionization coefficients [10,13]. Load-line A is based on the measured off-state breakdown voltage BV_{ds}^{G}. Load-lines B and C are for more realistic drain biases (1.5 and 2 V, respectively).

Wafer bonding technology for optoelectronic integrated devices

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Wafer bonding has been attracting considerable interest as a promising technology to integrate dissimilar materials, regardless of differences in lattice constants, crystal structures and orientations. Since the technology was first demonstrated in 1986 for Si-to-Si bonding and silicon-on-insulator (SOI) fabrications,[1-2] it has been extensively studied mainly for Si-based materials and has recently been applied to various III-V semiconductors for optical devices. Among them, bonding of InP to Si is especially generating increasing attention for optical interconnects between Si LSIs, which has been proposed as an effective method to overcome communication bottlenecks in the future LSI systems and/or to realize new functional LSIs.[3] Figure 1 schematically illustrates our target structures of the optically interconnected LSIs. InP lasers, preferably surface emitting lasers, are integrated on Si LSIs and the optical signals are emitted through the transparent Si substrate to another LSI chip. InP lasers are suitable for this purpose because Si is transparent at the emission wavelength and diffractive optical elements (DOEs), such as lenses and beam deflectors, can be integrated on the back-surface of the Si wafer.

Up to now, we have demonstrated InP lasers and LEDs fabricated on Si substrates by wafer bonding, with performances as good as those of conventional devices on InP substrates.[4] Recently, we have also demonstrated the InP LED on Si integrated with back-surface diffractive lenses, which will be a basic building block to realize the target structure illustrated in Fig. 1.

Figure 2 shows the schematic of the InP LED on Si integrated with back-surface (2-phase) diffractive lenses. The LED structure was fabricated with the conventional device process after bonding of the InP/InGaAsP DH thin films, followed by the fabrication of the back-surface lenses by photolithography with double-view mask aligner (with a typical alignment error less than 1.5 μm) and Si etching. The measured output power vs. current (L-I) characteristics of the fabricated LEDs are summarized in Fig. 3. The output power was measured under room temperature CW operation using large-area Ge photodetector (PD). The total power emitted through the Si substrate without the diffractive lens was measured by placing the PD as close to the LEDs as possible, as shown in Fig. 3 (a). The light output power higher than 200–μW was obtained. Fig. 3 (b) and (c) show the power from the LEDs (b) with and (c) without the diffractive lens, which were detected by the PD placed at some distance away from the LEDs so as to cover the solid angle of only 20 °, as illustrated in the inset of Fig. 3 (c). Higher power was detected with the lens (b), which obviously indicates that the LED light is collimated by the back-surface diffractive lens.

The wafer bonding is a promising technology to achieve new devices by integrating different materials, e.g. Si LSIs integrated with InP lasers, as described above. In this presentation, basic process and properties of wafer bonding as well as detailed characteristics of the fabricated devices will be discussed.

References: **[1]** Simbo et al., J. Appl. Phys. **60**, p. 2987 (1986). **[2]** Lasky, Appl. Phys. Lett. **48**, p.78 (1986). **[3]** Goodman et al., Proc. IEEE **72**, p. 850 (1984). **[4]** Wada et al., Jpn. J. Appl. Phys. **37**, p. 1383 (1998).

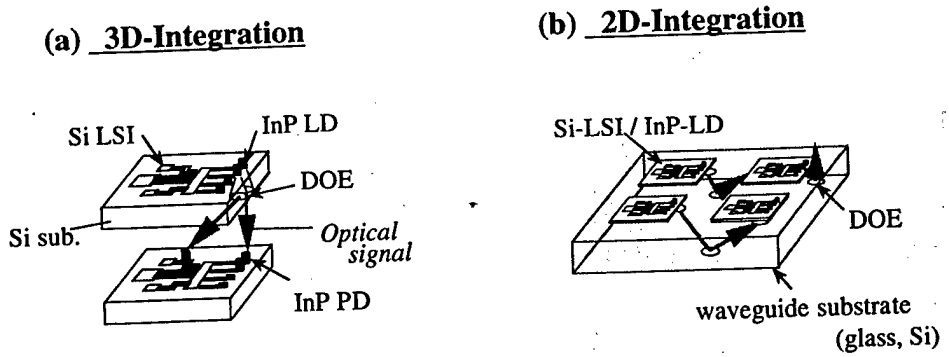

Fig. 1 Schematic pictures of proposed optically interconnected Si LSIs.

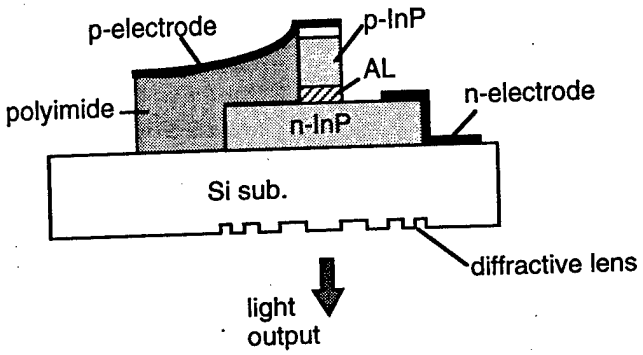

Fig. 2 Schematic structure of InP LEDs fabricated on Si with backside diffractive lenses.

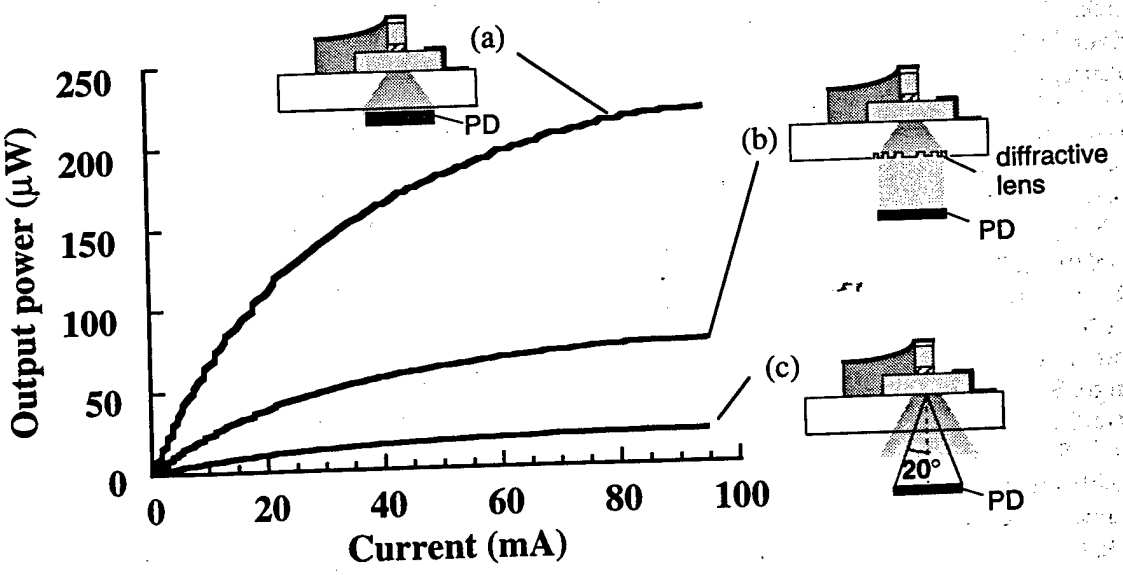

Fig. 3 Output power vs. current characteristics with different configurations.

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REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. AGENCY USE ONLY *(Leave blank)*	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	15 March 99	Final/ 01 May 98 through 30 Oct.98

4. TITLE AND SUBTITLE
Workshop for Heterostructure Microelectronics Information Systems Applications (TWHM-ISA '98)

5. FUNDING NUMBERS
N00014-98-1-0582

6. AUTHOR(S)
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7. PERFORMING ORGANIZATION NAMES(S) AND ADDRESS(ES)
Office of Naval Research
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536 S. Clark St., Room 208
Chicago, IL 60605-1583

8. PERFORMING ORGANIZATION REPORT NUMBER
Regents of The University of Michigan
Tax# 386-00-6309

9. SPONSORING / MONITORING AGENCY NAMES(S) AND ADDRESS(ES)
Dr. John C. Zolper
Electronics Division, Code-312
Office of Naval Research
800 N. Quincy St.
Arlington, VA 22217-5660

10. SPONSORING / MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES

a. DISTRIBUTION / AVAILABILITY STATEMENT
APPROVED FOR PUBLIC RELEASE

12. DISTRIBUTION CODE
DOD

13. ABSTRACT *(Maximum 200 words)*

The 3rd Topical Workshop on Heterstructure Microelectronics for Information Systems Applications (TWHM-ISA '98), held in in Hayama-machi, Japan. A special emphasis was placed on the applications in information systems for this workshop. The Workshop sessions contain a variety of contributions on devices, materials, circuits and systems. The technologies employed are based on heterostructure bipolar transistors, heterostructure field effect transistors and resonant tunneling diodes, and make use of a variety of heterostructure material systems including III-Vs (e.g. GaAs, InP and related compounds), group IV semiconductors (e.g. SiGe), and wide bandgap semiconductors (e.g. III-V Nitrides and SiC). Special emphasis was also placed on the effective insertion of these devices and circuits into systems such as mobile, fiber optic, space communications, as well as signal and data processing.

14. SUBJECT TERMS	15. NUMBER OF PAGES
Heterostructure devices, III-V and SiGe components, Systems for Communication and Information	113
	16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT