



*Global Standards for the Microelectronics Industry*

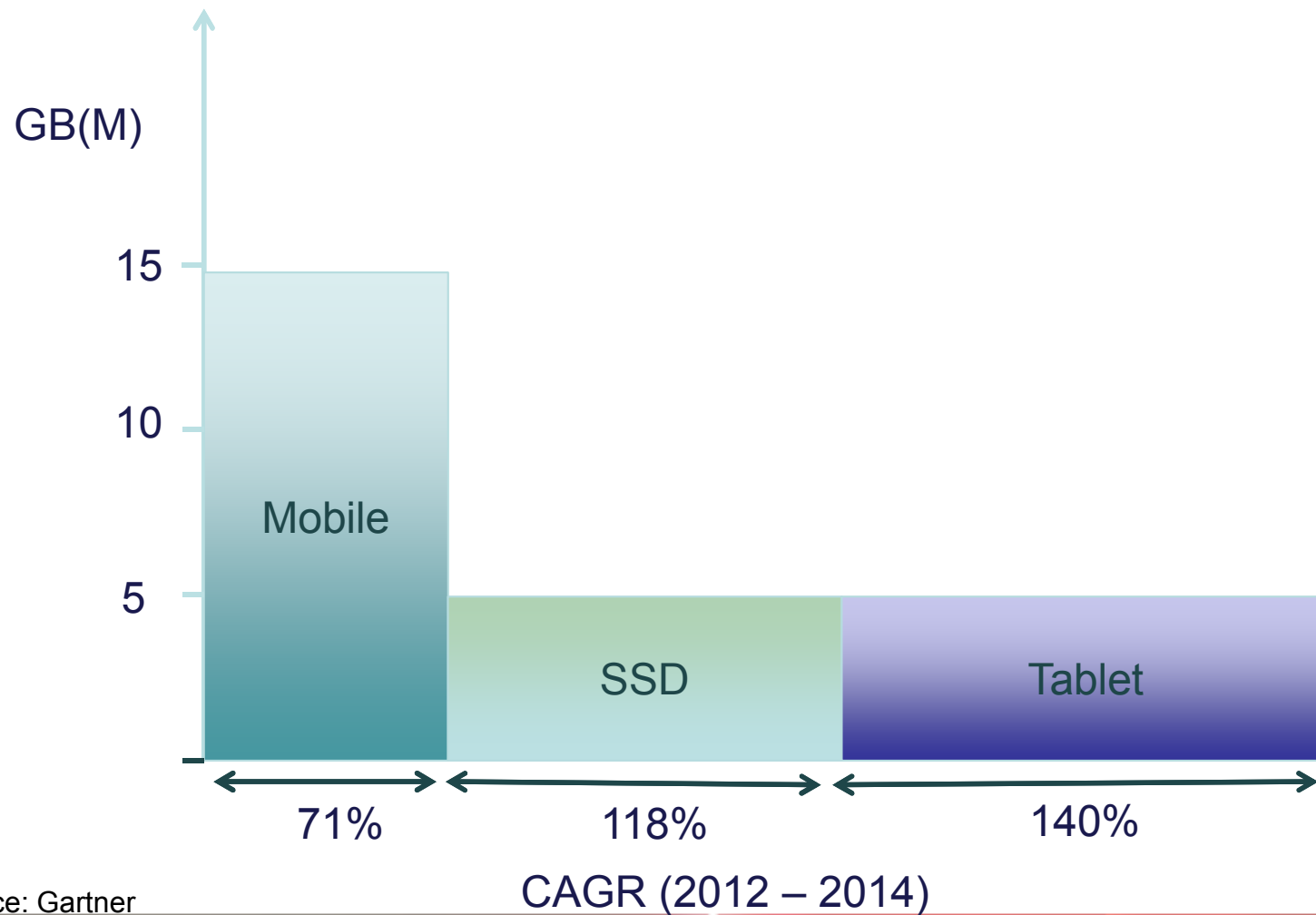
# Total IP Solution for Mobile Storage UFS & NAND Controllers

**Yuping Chung**  
**Arasan Chip Systems**  
**San Jose, CA**



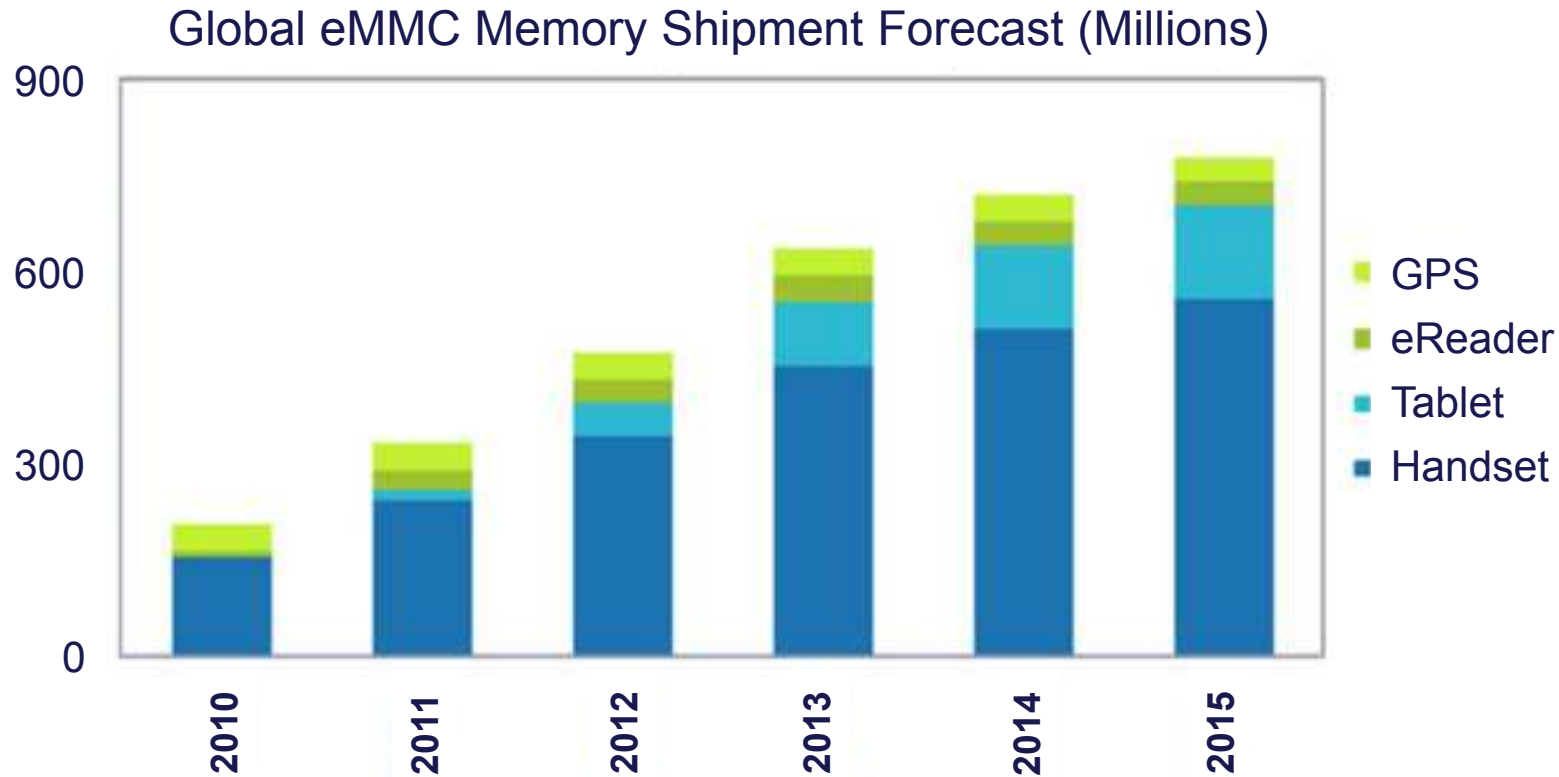
*Mobile Forum Taiwan & Korea 2012*

# Fast Growing NAND Storage Markets



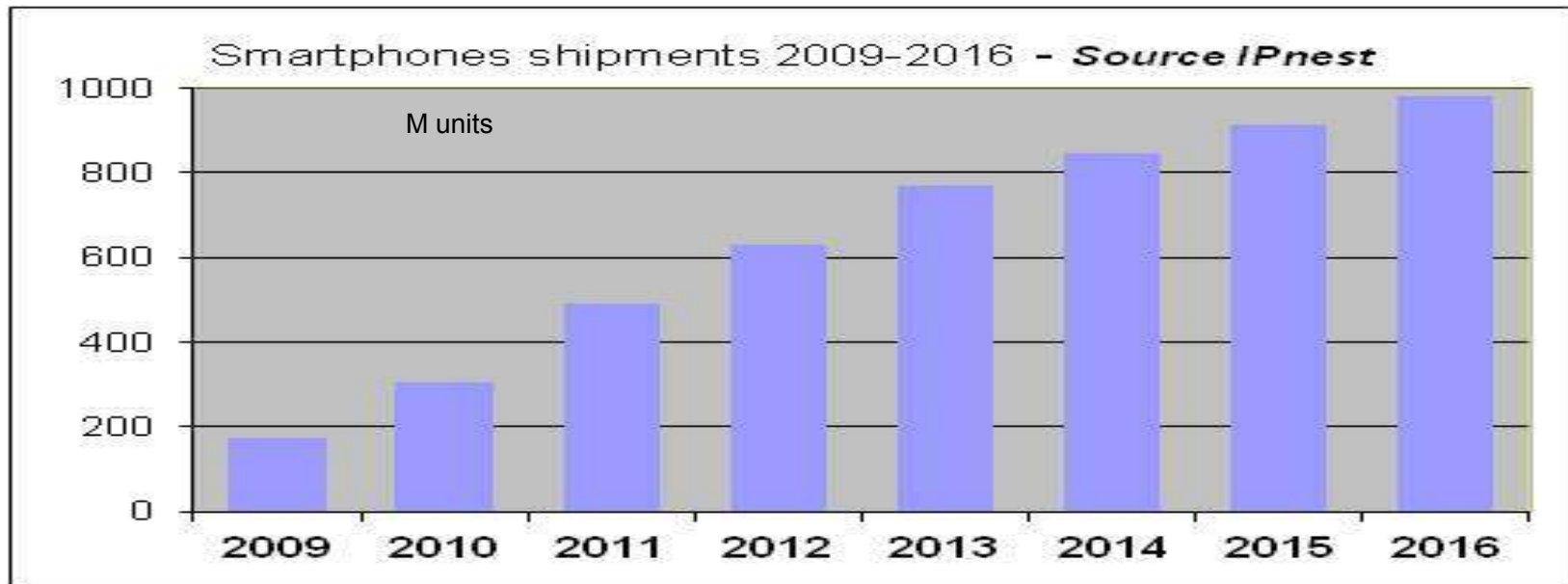
Source: Gartner

# Mobile Storage Keeps Growing



Source: IHS iSuppli Research June 2011

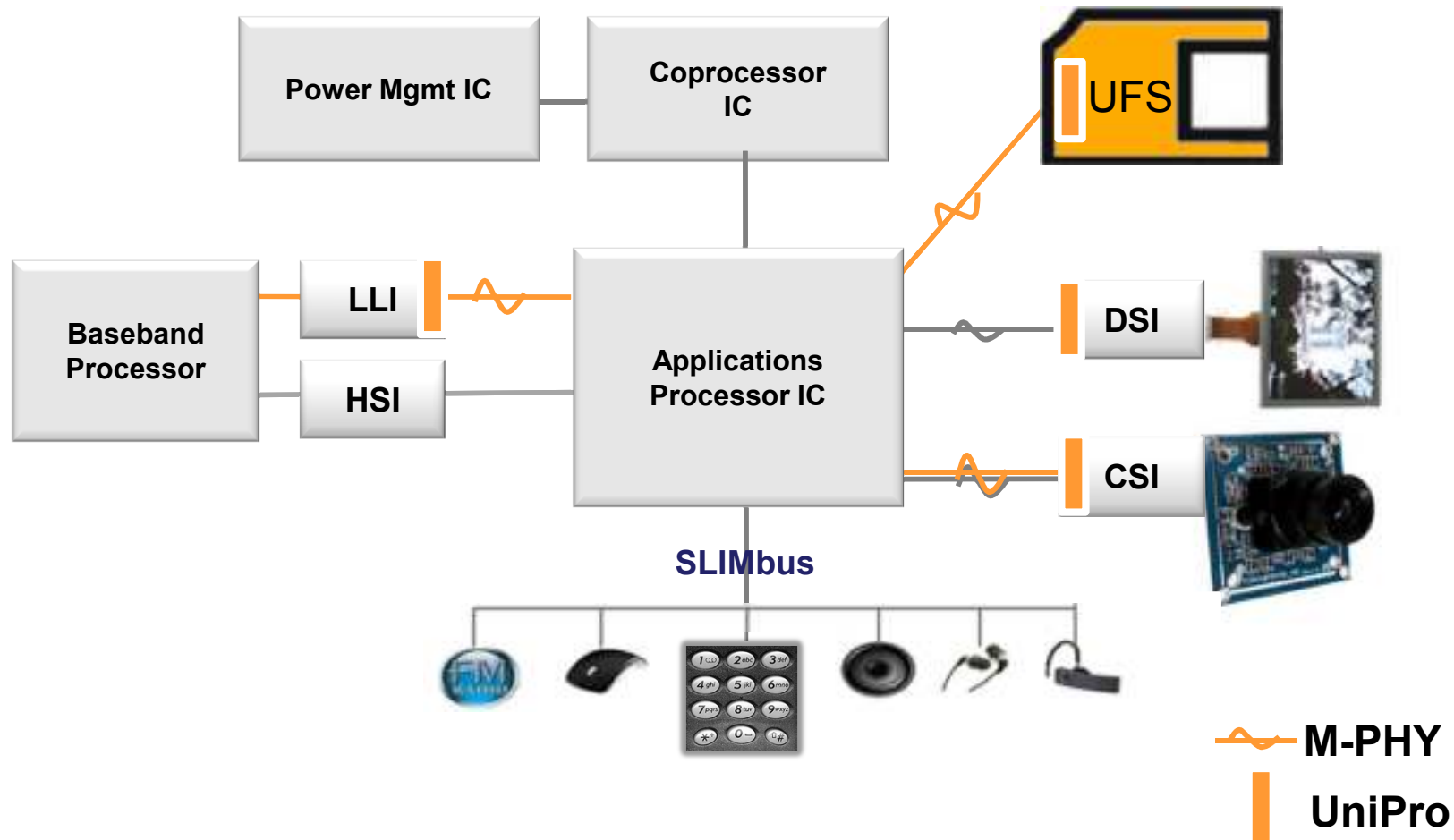
# MIPI Adoption Driven by Smart Mobile



MIPI – Mobile Industry Processor Interface Alliance; The standard body defining M-PHY & UniPro adopted by JEDEC UFS

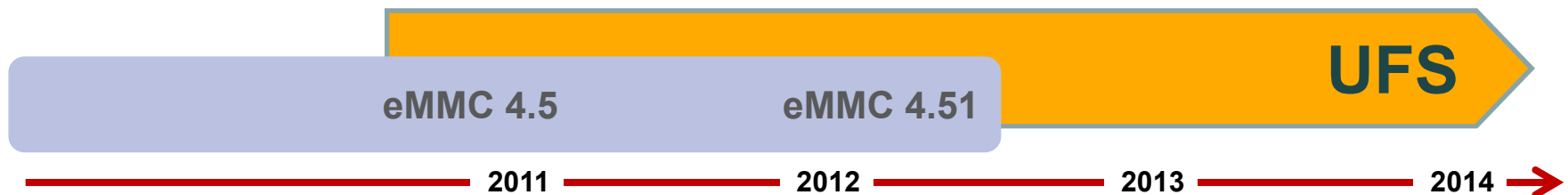
# UFS Integrated with MIPI protocols

Using same M-PHY and UniPro<sup>®</sup> specs

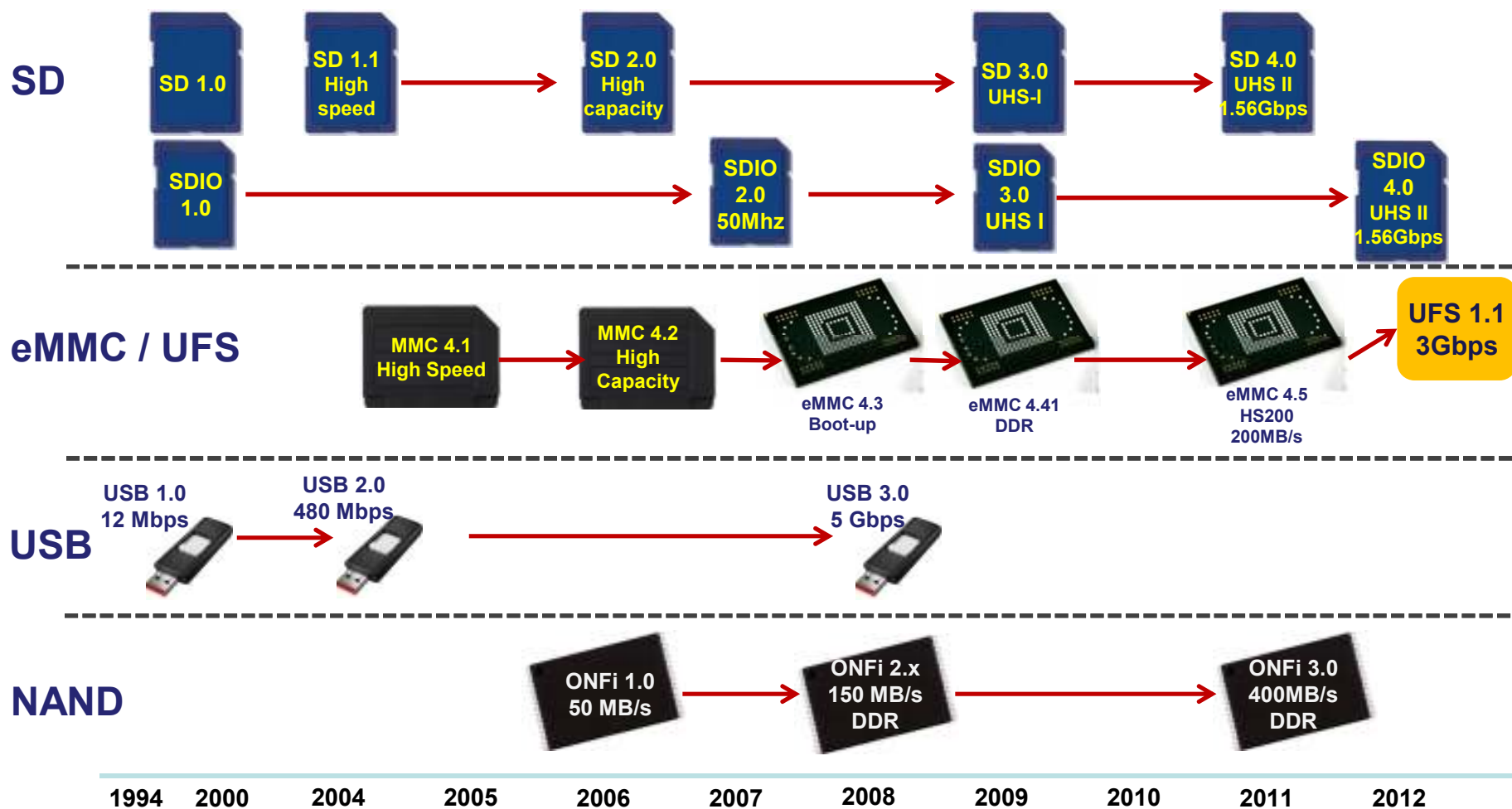


# Why UFS ?

- JEDEC standard (JES220)
- Leverage and **Reuse** Existing Standards
  - MIPI Architecture – UniPro, M-PHY
  - SCSI Command Sets
- Serial Interface Rx / Tx - SoC **Lower Pin Count**
- **High Bandwidth** Migration Path for eMMC - 1.5/3/6 Gbps
- **Lower Power** for Mobile Applications



# Mobile SoC Support Multiple Storage Interfaces and Backward Compatibility



# Total Solution Supporting Mobile Storage

## 1. Complexity of Integration

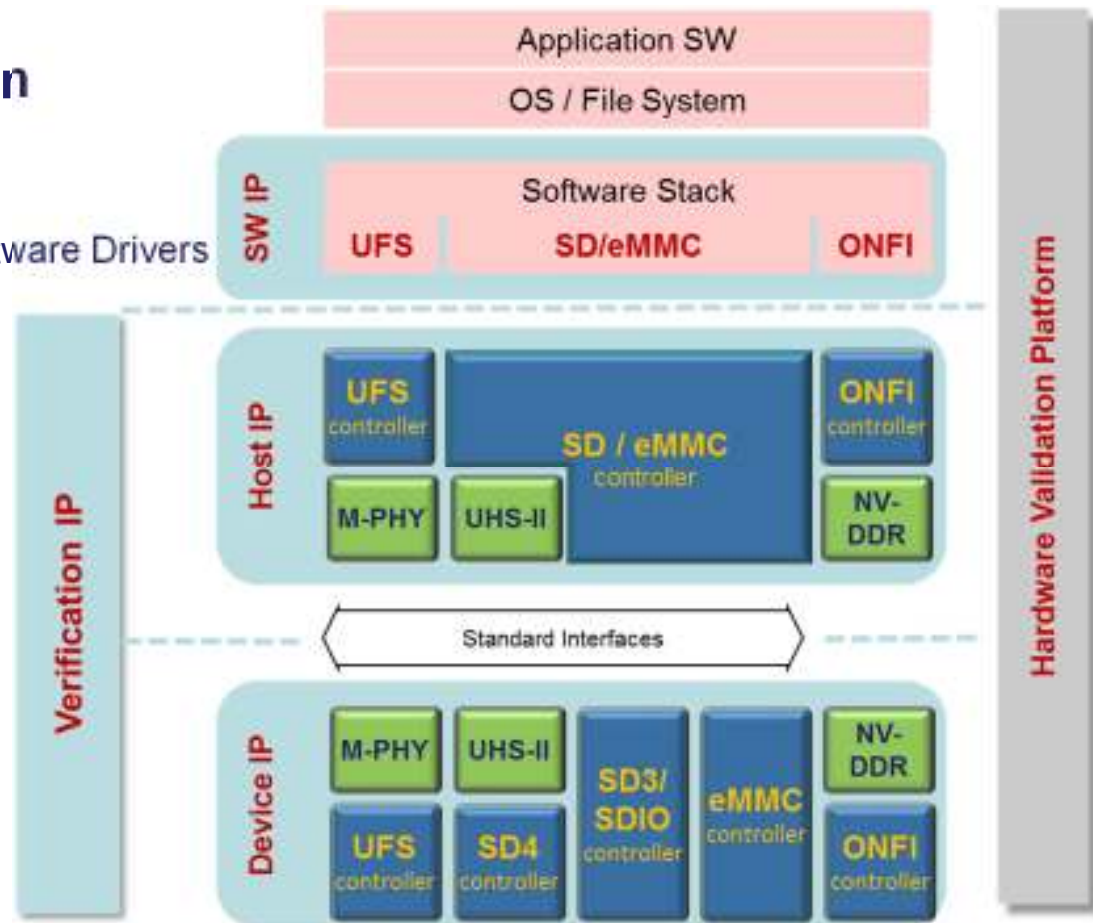
- Physical Layer Analog Interface
- Controller Digital Design
- Controller Firmware and OS Software Drivers
- OS File Systems & Stacks

## 2. Compliance

- Meet specifications

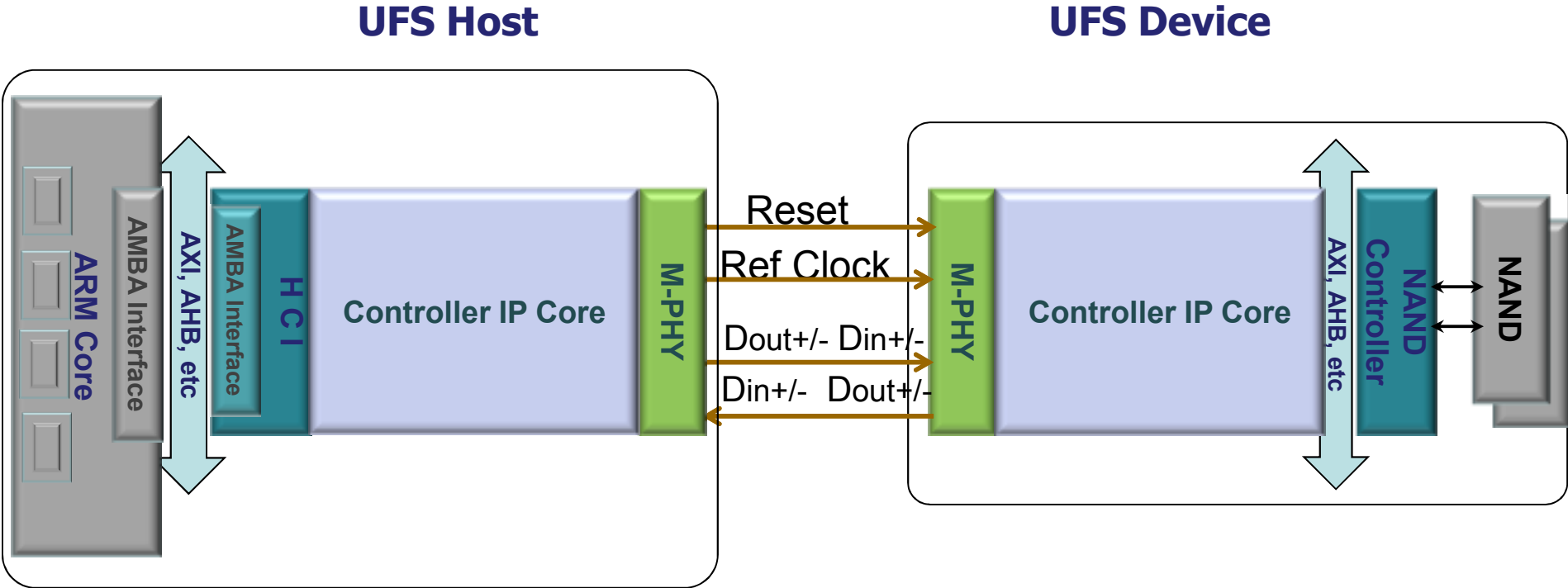
## 3. Compatibility

- Comprehensive Interoperability

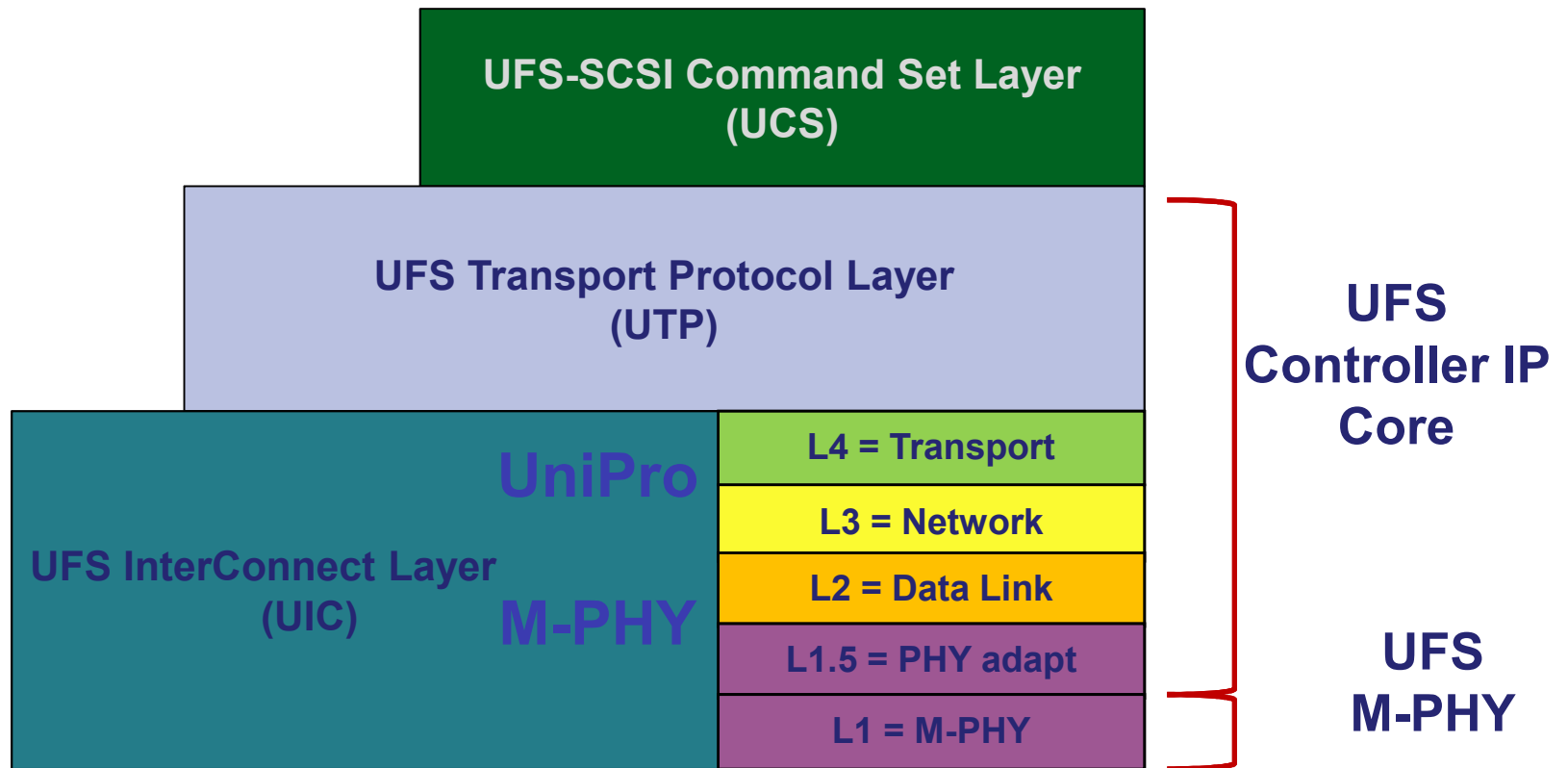




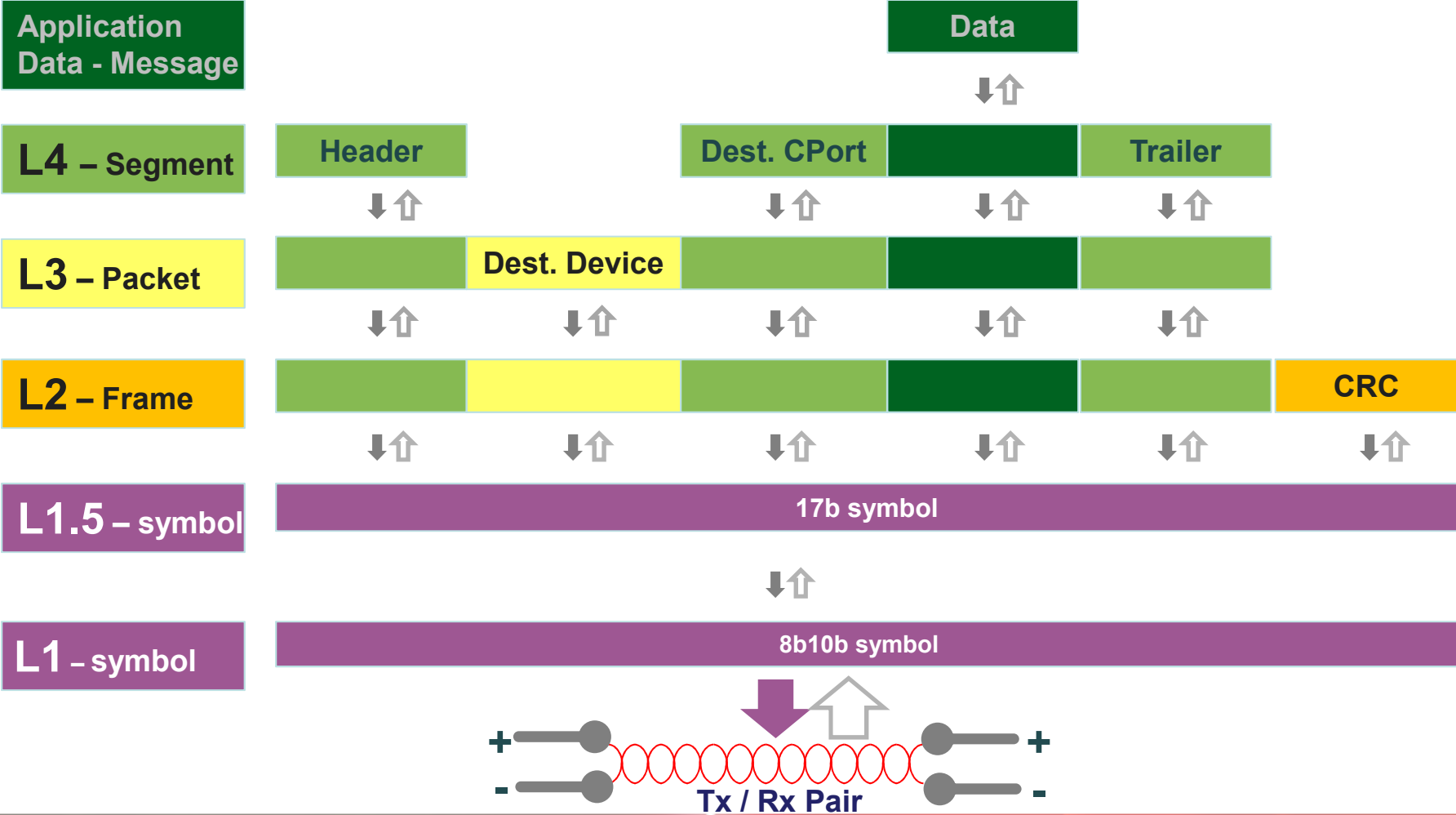
# UFS Mobile Storage Implementation



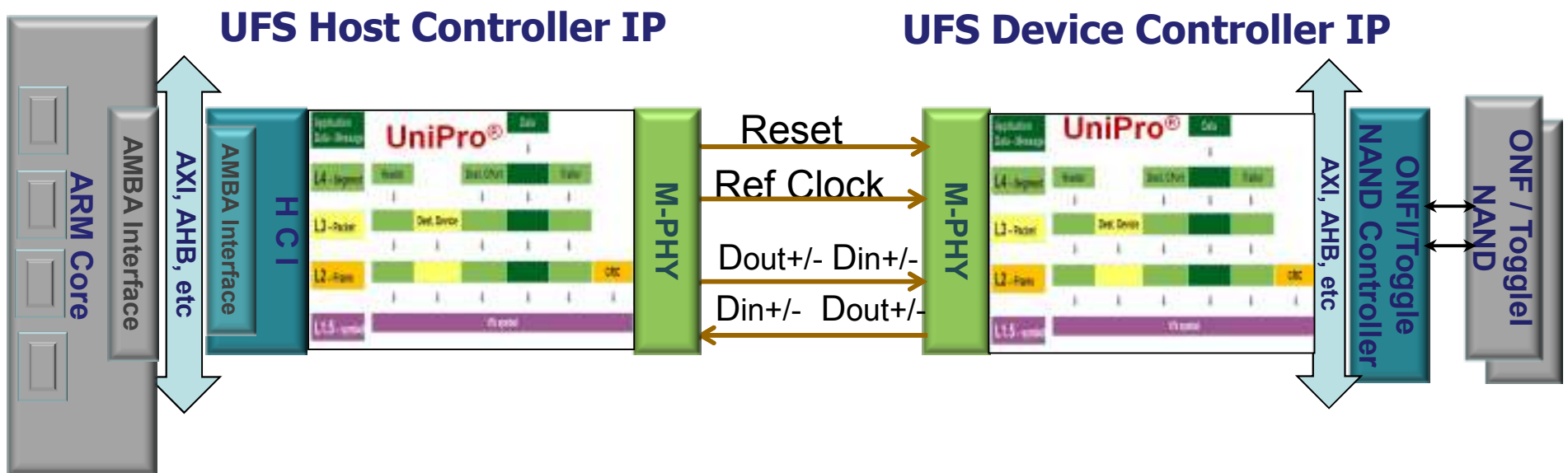
# Layered Architecture



# UniPro<sup>®</sup> Ensures Data Integrity



# UFS Controller with Certified UniPro®



# M-PHY Type 1 Key Features for UFS (con't)

- HS Gear 1, 2, 3
- LS PWM Gear 0-7
- Configurable up to 4 lanes
- Ref clock - 19.2 / 26 / 38.4 / 52 MHz

HIGH SPEED			
Gear	Rate A	Rate B	Implementation
1	1.25 Gbps	1.5 Gbps	Mandatory
2	2.5 Gbps	3 Gbps	Optional
3	5 Gbps	5.8 Gbps	Optional

LOW SPEED		
Gear	Bit Rate Mbps	Implementation
0	below Gear 1	not supported
1	3 to 9	Mandatory
2	6 to 18	
3	12 to 36	
4	24 to 72	
5	48 to 144	Optional
6	96 to 288	
7	192 to 576	

# M-PHY Type 1 Key Features for UFS

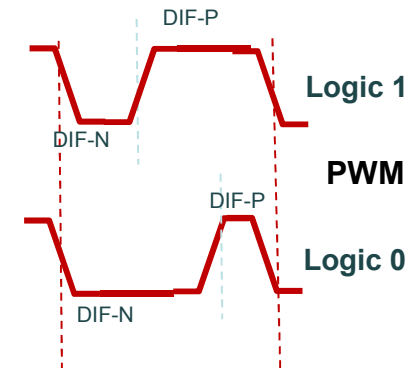
- Differential Serial Interfaces

- Type 1 M-PHY

- High Speed NRZ Signaling
    - Low Speed PWM Signaling

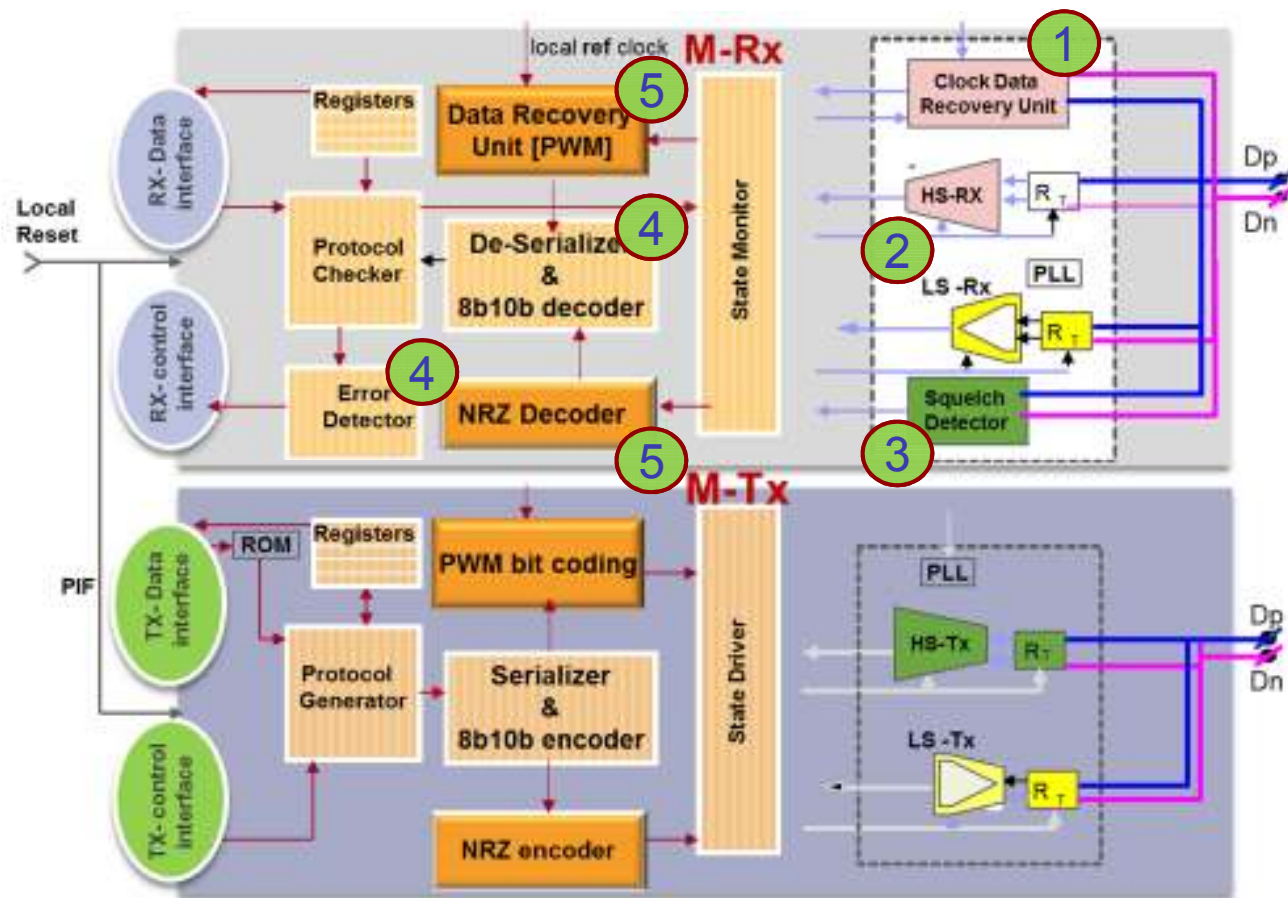
- Up to 4 Lanes

- Power Savings



Power States	Description
Stall	HS-Mode power saving state; Allows fast recovery time
Sleep	LS-Mode power saving state;
Hibern8	Ultra Low Power State; Configuration still intact
Disabled	Disabled by Reset; Configuration reset to default
Unpowered	Power Supply Removed

# M-PHY for UFS Implementation



① Synchronization

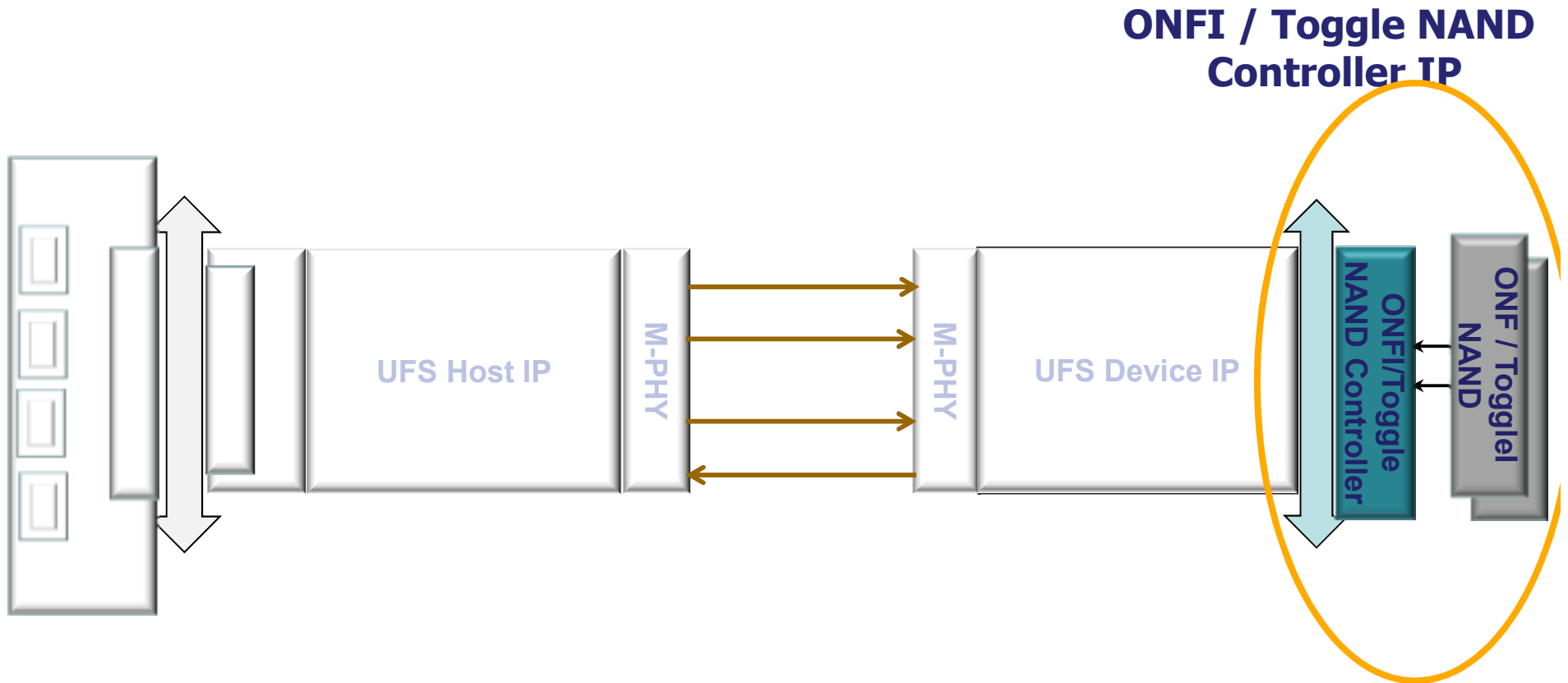
② Type-1:  
HS & LS Mode

③ Power Saving

④ Data Integrity



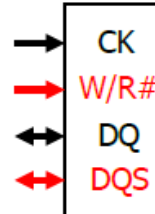
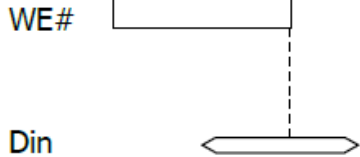
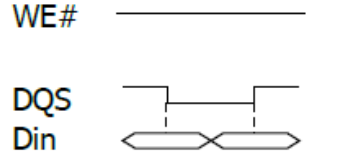
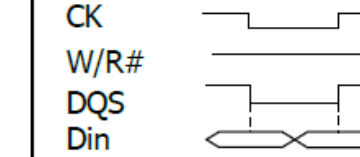
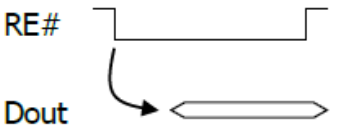
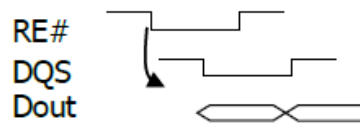
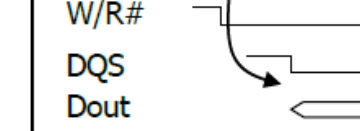
⑤ Coding for  
NRZ & PWM

# High Performance NAND for UFS Device





# NAND Flash Interface Evolution

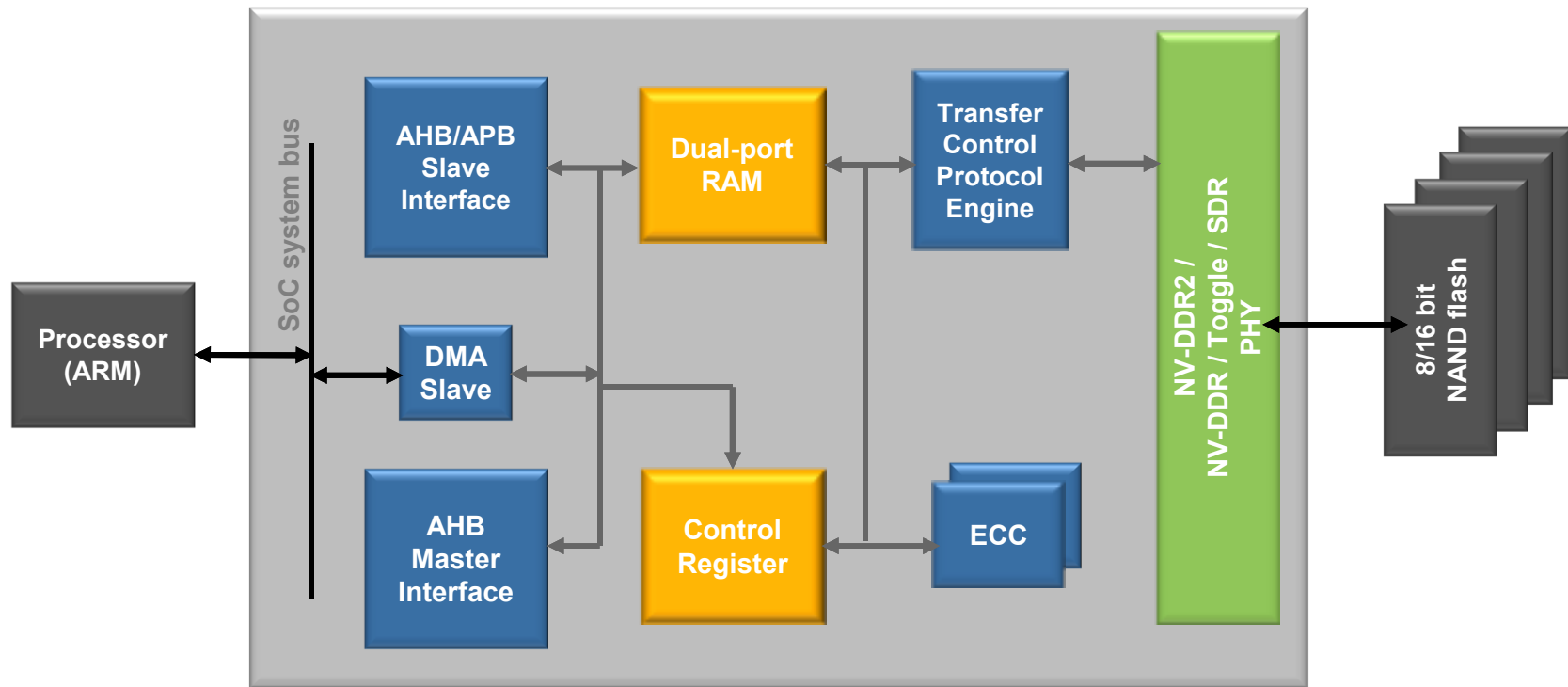
	JEDEC	Proprietary	JEDEC/ONFI
	Legacy SDR	Toggle-mode DDR	Synchronous DDR
Pinout			
Writes			
Reads			

Source: JEDEC 2010

# ONFI Interface 2.x, 3.0

Feature	ONFI 2.0	ONFI 2.3	ONFI 3.0
	SDR	NV-DDR	NV-DDR2
Max Speed	Mode 5 (20ns)	200 MT/s (100Mhz)	<b>400 MT/s (200Mhz)</b>
CE_n Pin Reduction	Yes	Yes	Yes
Volume Addressing	Yes	Yes	Yes
On-die termination (ODT)	No	No	<b>Yes</b>
Differential Signaling	No	No	<b>Yes, optional for DQS and/or RE_n</b>
I/O VccQ	3.3V / 1.8V	3.3V / 1.8V	<b>1.8V</b>
External VREFQ	No	No	<b>Yes</b>

# Versatile NAND Flash Controller IP



NAND Controller IP includes:

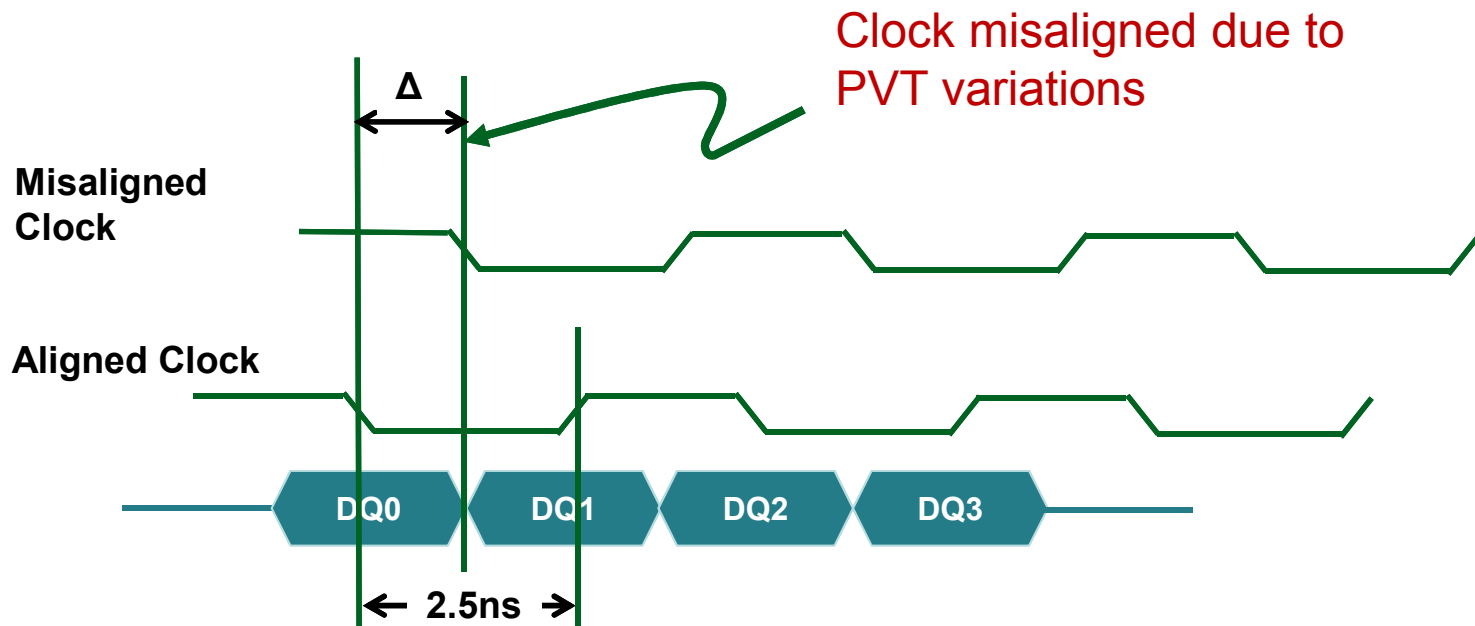
- ONFI NV-DDR2 PHY, Toggle DDR 1/2, Legacy SDR
- ECC engine
- ARM interface – AMBA (AXI, AHB)

# Challenge of Designing for 400MT/s

Process, Voltage, and Temperature (PVT) lead to clock misalignment

A synthesized solution cannot meet the 2.5ns DDR data period

**A hard IP DLL or Delay Circuit** is required to ensure the clock edge is aligned to the center of data for correct sampling

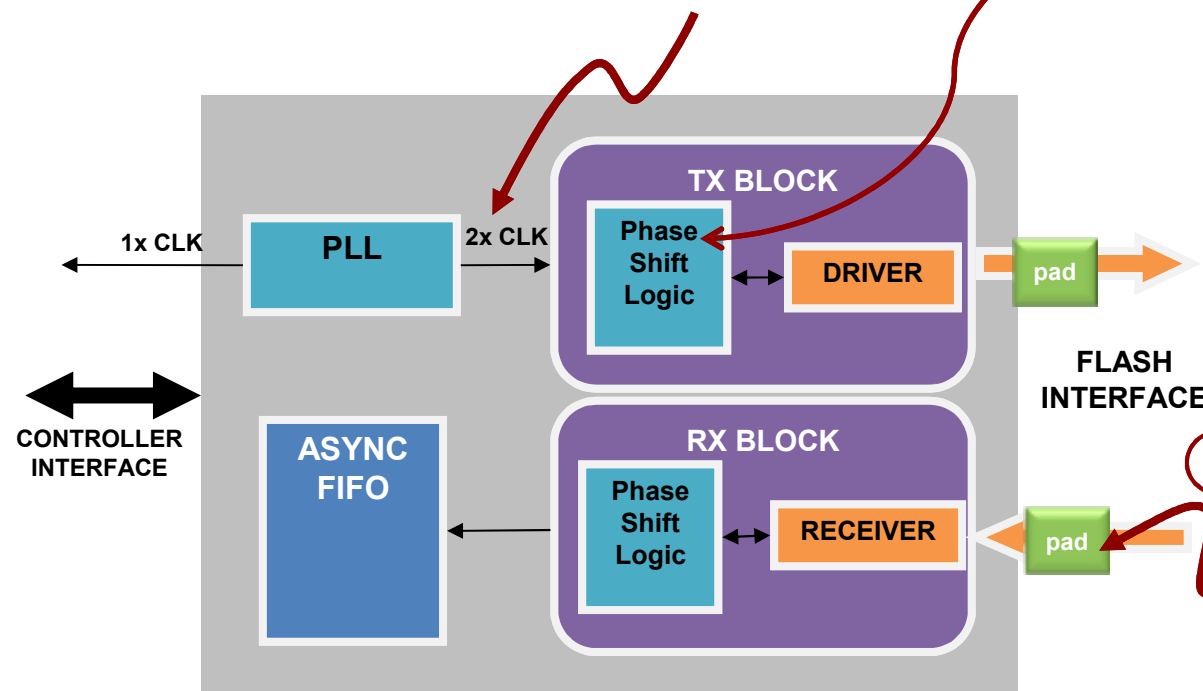


# Optimized ONFI 3.0 PHY

② 2X clock into Tx generates more accurate sampling clock

① DLL Circuit

- More accurate than typical delay circuit
- Allows designer to align and optimize for data sampling;
- Smaller die size and lower power consumption

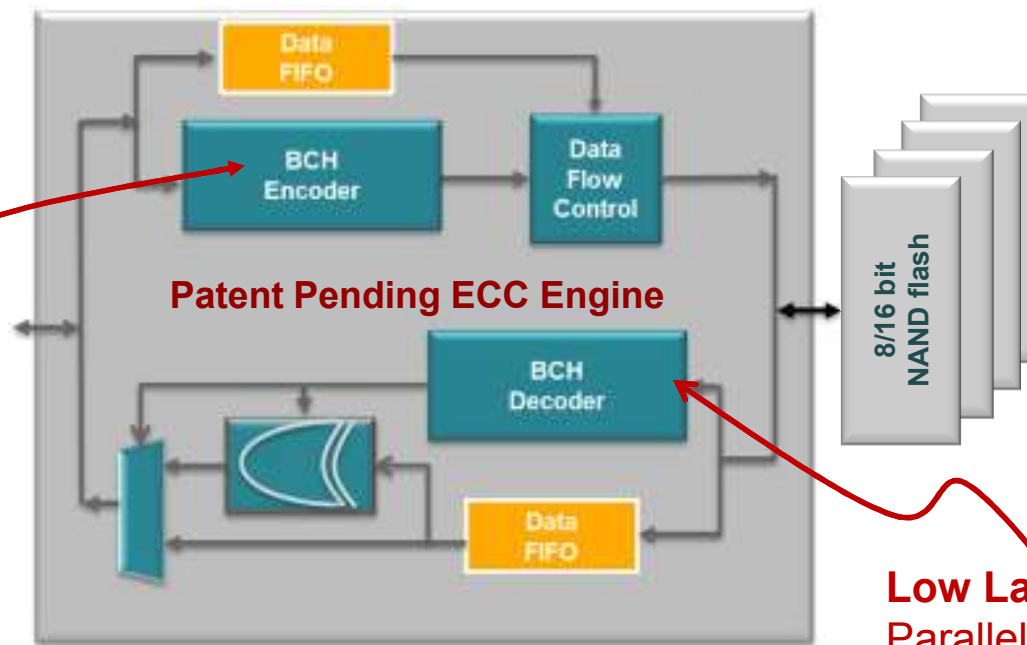


③ ONFI 3.0 compliant I/O pad  
- 1.8v / 3.3v dual voltage  
(not a typical DDR pad)

# Dynamically Configurable ECC Engine

1. Modular design expandable to 32-bit or more ECC capability
2. Match different ECC requirements for different NAND ICs

**High Performance:**  
Parallel bit processing  
on BCH encoder



**Low Latency:**  
Parallel syndrome generation  
on BCH decoder

**BCH Decoder:**

Inversion-less *Berlekamp-Massey* algorithm for Key Equation Solver

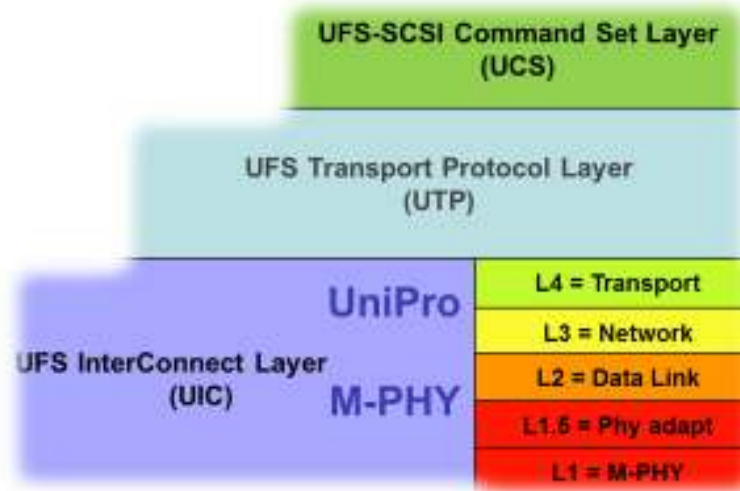
Parallel computation for Key Equation Solver using parallel *Chien* search algorithm

# UFS / NAND Total IP Solution

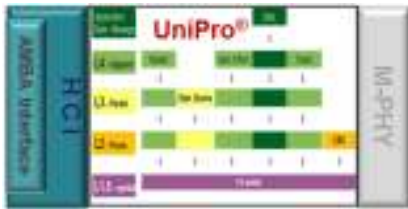
## Companion Software Stacks



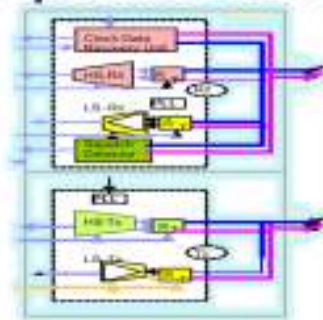
## UFS Host & Device



## Certified Digital IP Core



## InterOperable Analog PHY



## IP & Software Validation Platform



**Yuping Chung**  
**yuping.chung@arasan.com**

**Arasan Chip Systems**  
**San Jose , CA**

**THANK YOU**