

## ESE 570: Digital Integrated Circuits and VLSI Fundamentals

Lec 25: December 9, 2020  
Transmission Lines



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## Where Transmission Lines Arise



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## Transmission Lines

- ❑ This is what wires/cables look like
  - Aren't an ideal equipotential
  - Signals do take time to propagate
  - Maintain shape of input signal
    - Within limits
  - Shape and topology of wiring effects how signals propagate
- ❑ Need theory/model to support design
  - Reason about behavior
  - Understand what can cause noise
  - Engineer high performance/speed communication

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## Lecture Outline

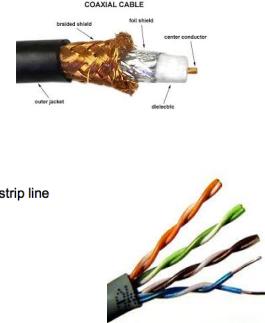
- ❑ Transmission Lines
  - Where transmission lines arise?
  - Lossless Transmission Line
  - Termination
  - Lossy Transmission Line

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## Transmission Lines

- ❑ Cable: coaxial
- ❑ PCB
  - Strip line
  - Microstrip line
- ❑ Twisted Pair (Cat5)



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## Wire Formulation



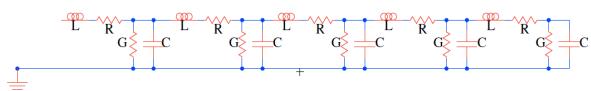
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## Wires

- In general, our “wires” have distributed R, L, C components

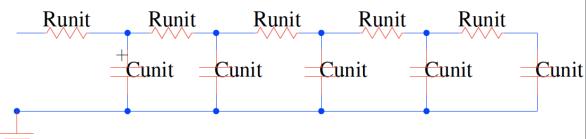


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## RC Wire

- When R dominates L
  - We have the distributed RC Wires
  - Typical of on-chip wires in ICs

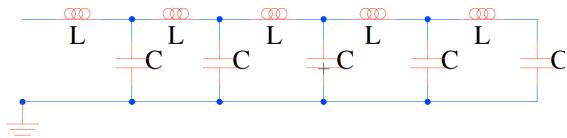


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## Lossless Transmission Line

- When resistance is negligible
  - Have LC wire = Lossless Transmission Line
    - No energy dissipation (loss) through R's
  - More typical of Printed Circuit Board wires and bond wires



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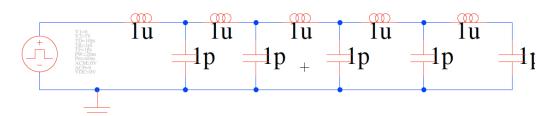
## Intuitive: Lossless

- Pulses travel as waves without distortion
  - (up to a characteristic frequency)

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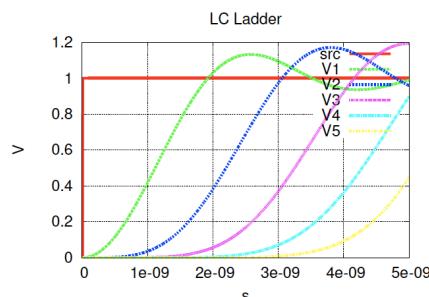
## SPICE Simulation



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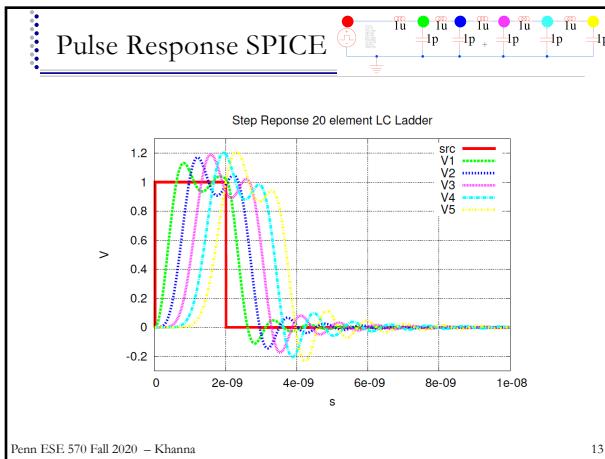
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## Step Response SPICE

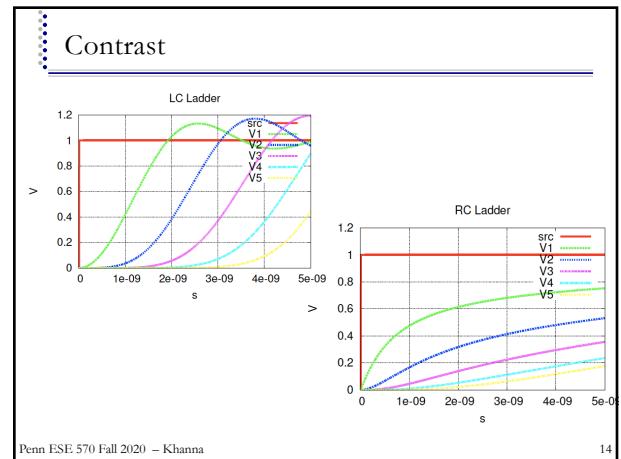


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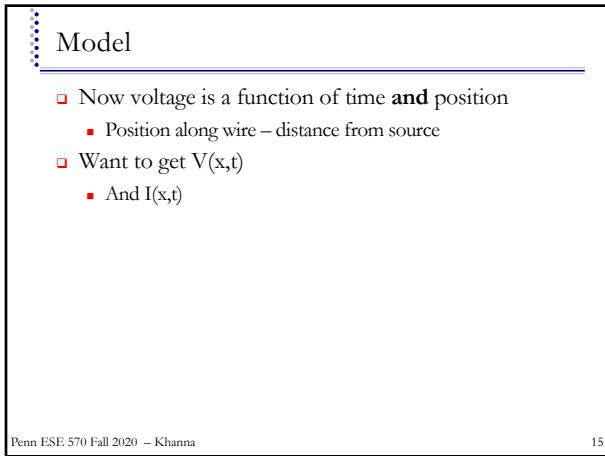
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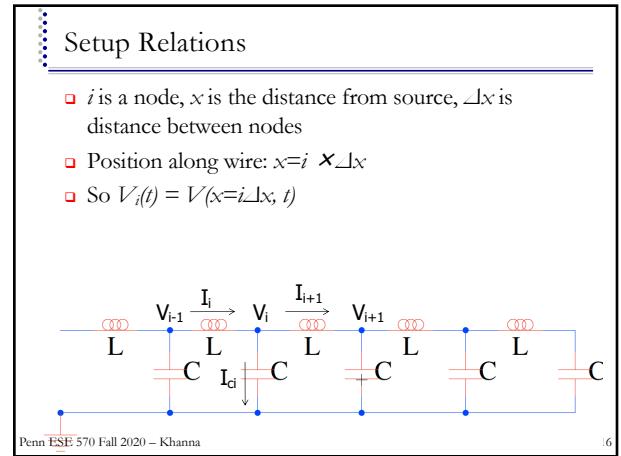
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Implication

- Wave equation:
$$\frac{\partial^2 V}{\partial x^2} = LC \frac{\partial^2 V}{\partial t^2}$$

- Solution:
$$V(x,t) = A + Be^{x-wt}$$

- What is  $w$ ?
$$Be^{x-wt} = LCw^2 Be^{x-wt}$$

$$w = \sqrt{\frac{1}{LC}}$$

w is the rate of propagation

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Propagation Rate in Example

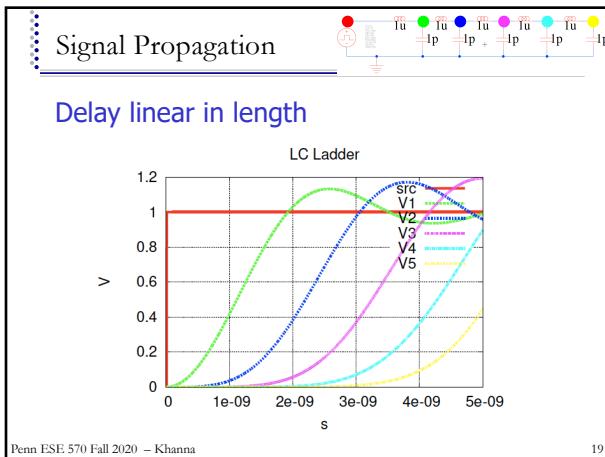
- ❑  $L=1\mu H$
- ❑  $C=1pF$
- ❑ What is  $w$ ?

$$w = \frac{1}{\sqrt{LC}}$$

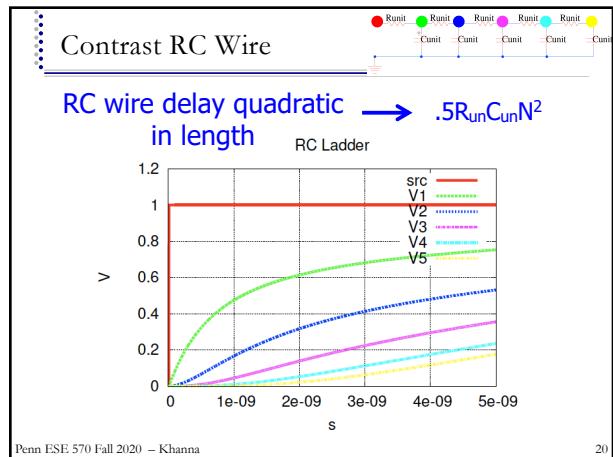
A circuit diagram of a transmission line example. It shows a pulse source connected to the left end of a line. The line consists of several segments, each with an inductor  $1\mu H$  and a capacitor  $1pF$ . The total length of the line is indicated as  $1$ .

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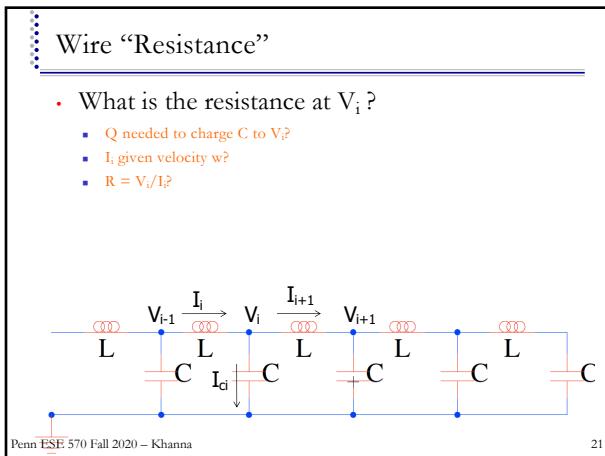
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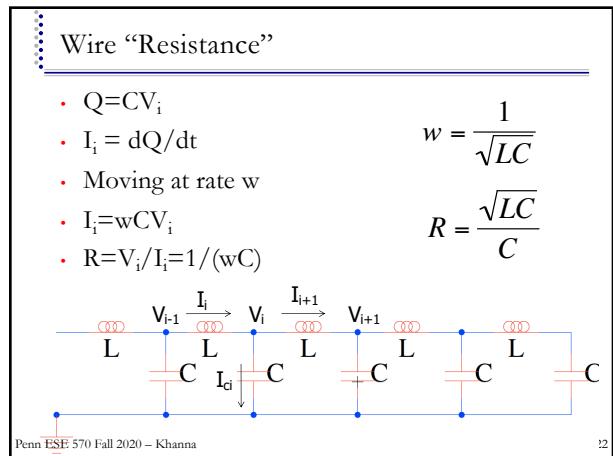
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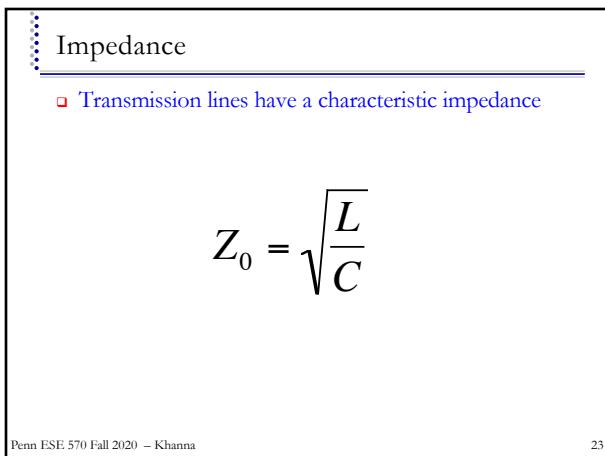
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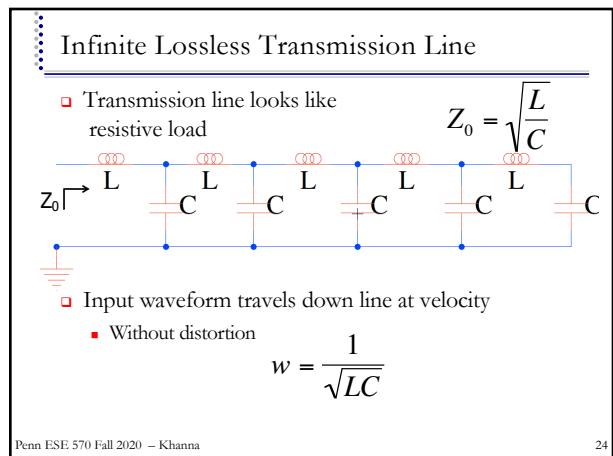
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## Termination

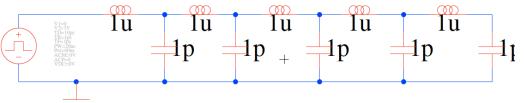


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## End of Line

- What happens at the end of the transmission line?

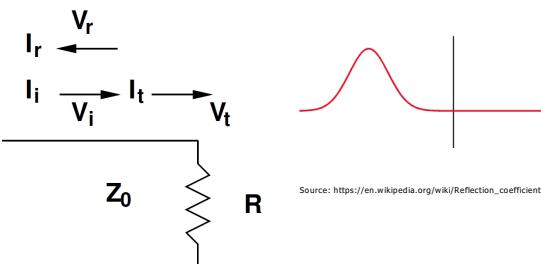


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## Analyze End of Line

- Incident Wave, Reflected Wave, Transverse Wave



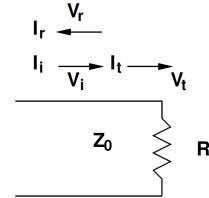
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## Reflection

Reflection coefficient

$$V_r \left( \frac{R - Z_0}{R + Z_0} \right) = V_r$$



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## Analyze End of Line

- $V_i + V_r = V_t$

$$V_i \left( \frac{R - Z_0}{R + Z_0} \right) = V_r$$

$$V_i \left( \frac{R - Z_0}{R + Z_0} \right) = V_t - V_i$$

$$V_i \left( \frac{R - Z_0}{R + Z_0} + 1 \right) = V_t$$

$$V_i \left( \frac{2R}{R + Z_0} \right) = V_t$$

Transmission coefficient

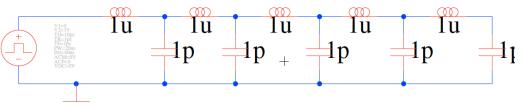
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## End of Line

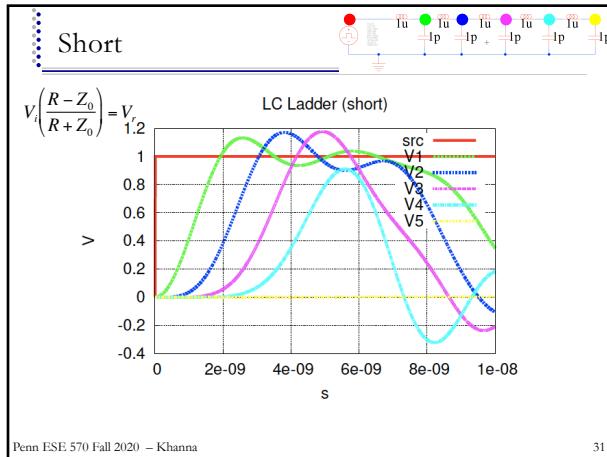
- What happens at the end of the transmission line?

- Short Circuit,  $R=0$ 
  - Hint: what must happen in steady state?
- Terminate with  $R=Z_0$
- Open Circuit,  $R=\infty$

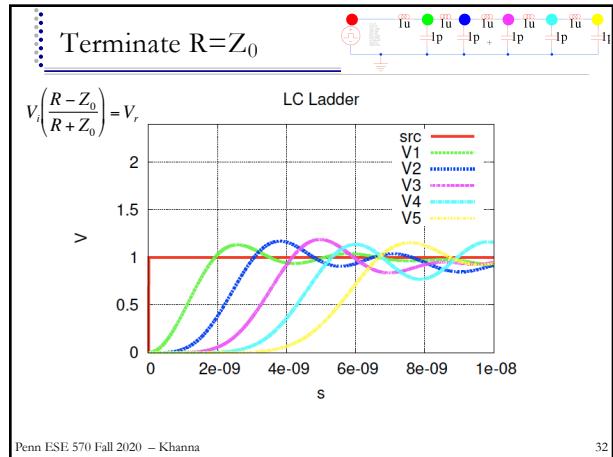


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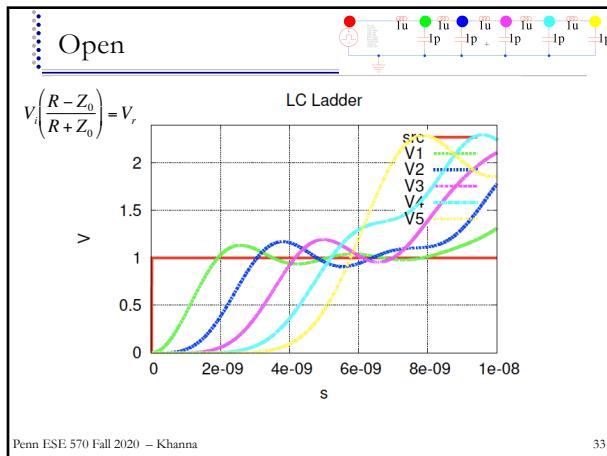
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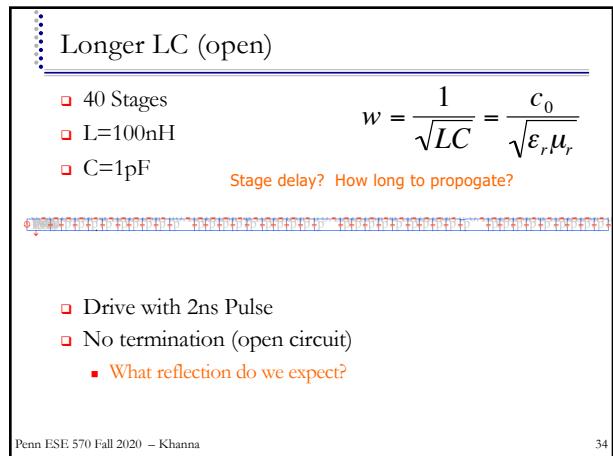
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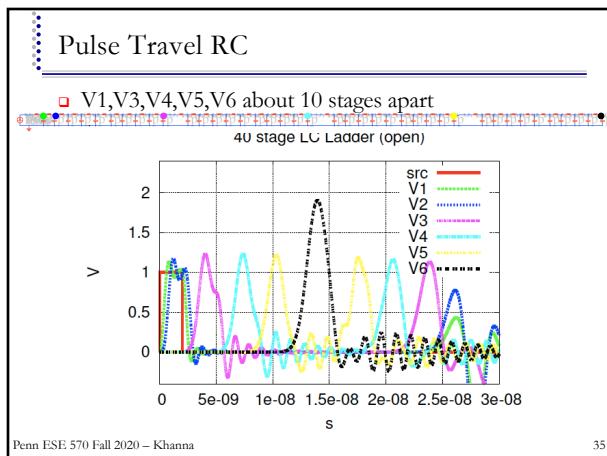
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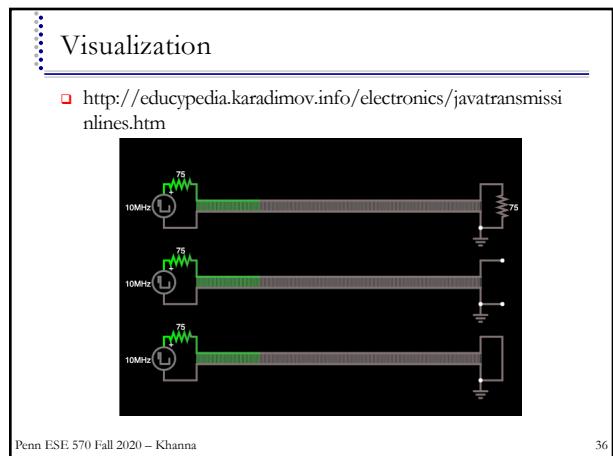
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## Back to Source

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## Back at Source?

- ❑ What happens at source?
  - Depends on how it's terminated

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## $R \neq Z_0$

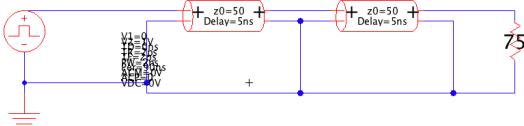
- ❑ What happens?
  - $75\Omega$  termination on  $50\Omega$  line

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## Transmission Line Symbol

- ❑ Specify delay of full Tline and characteristic impedance
- ❑ Need reference

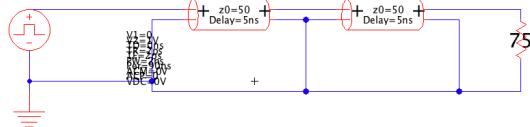


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## Simulation

- ❑ For these, with direct drive from voltage source
  - Source looks like short circuit (not typical of CMOS)
  - Source cannot be changed

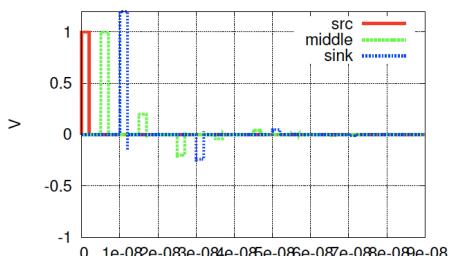


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## $50\Omega$ line, $75\Omega$ termination

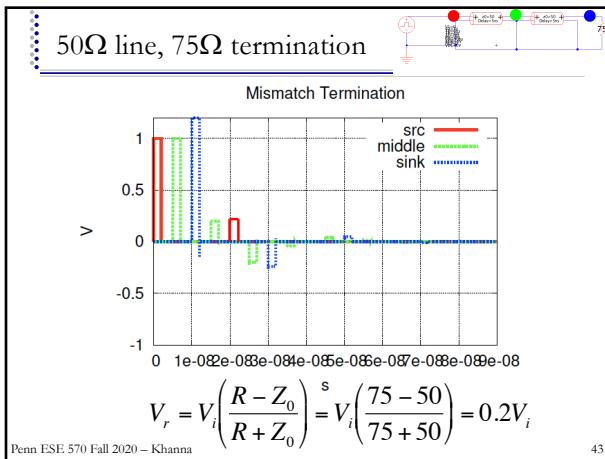
Mismatch Termination



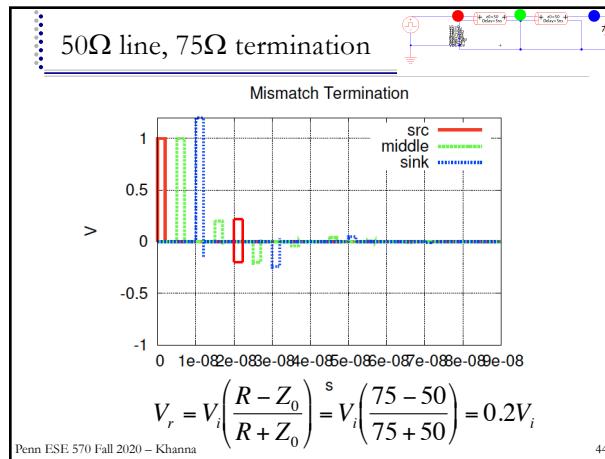
$$V_r = V_i \left( \frac{R - Z_0}{R + Z_0} \right)^s = V_i \left( \frac{75 - 50}{75 + 50} \right) = 0.2V_i$$

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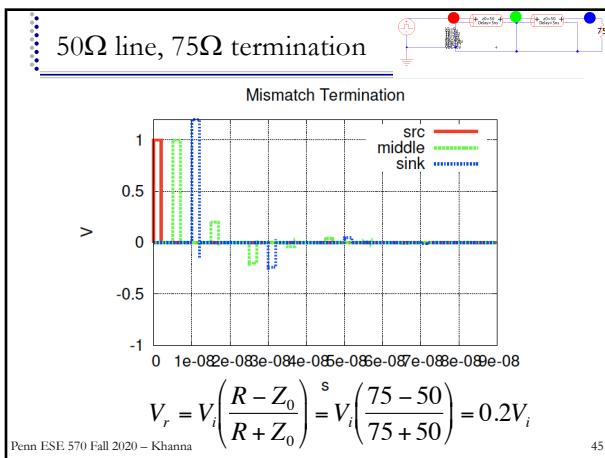
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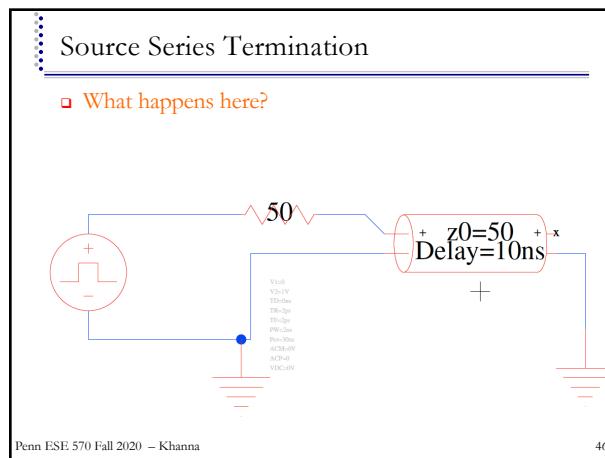
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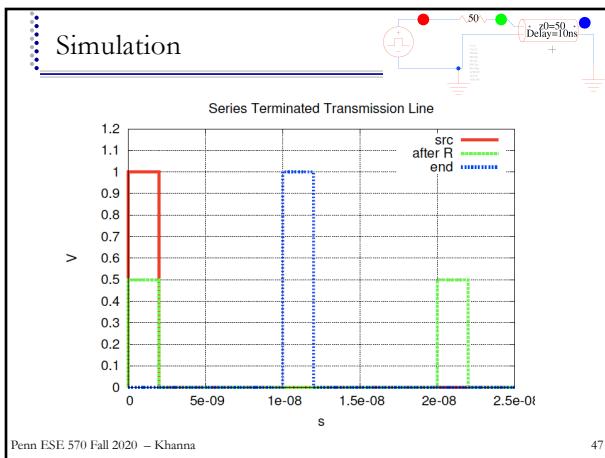
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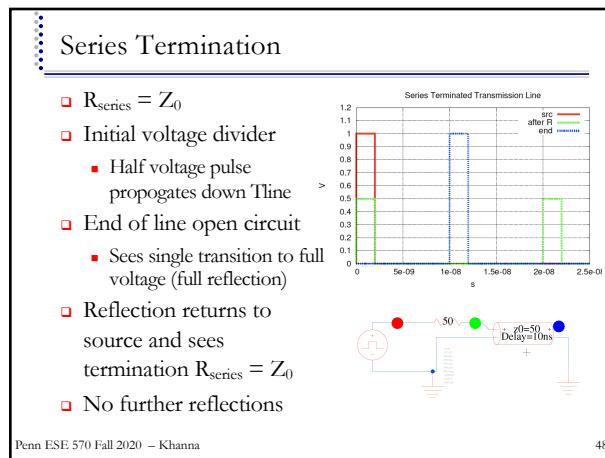
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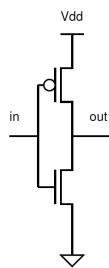
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## CMOS Driver / Receiver

- Driver: What does a CMOS driver look like at the source?

■  $I_{d,sat}=1200\mu A/\mu m$  @ 45nm,  $V_{dd}=1V$

- Receiver: What does a CMOS inverter look like at the sink?



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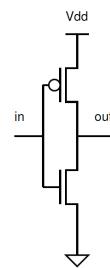
## CMOS Driver / Receiver

- Driver: What does a CMOS driver look like at the source?

■  $I_{d,sat}=1200\mu A/\mu m$  @ 45nm,  $V_{dd}=1V$

- Receiver: What does a CMOS inverter look like at the sink?

■ Infinite resistance  $\rightarrow$  Open circuit



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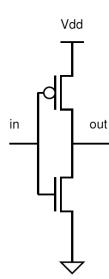
## CMOS Driver

- Driver: What does a CMOS driver look like at the source?

■  $I_{d,sat}=1200\mu A/\mu m$  @ 45nm,  $V_{dd}=1V$

- Min size:

■  $I_{drive}=1200\mu A/\mu m * 45nm = 54\mu A$   
■  $R_{out}=V_{dd}/I_{drive}=18k\Omega$



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## CMOS Driver

- Driver: What does a CMOS driver look like at the source?

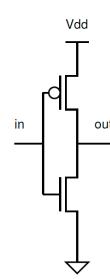
■  $I_{d,sat}=1200\mu A/\mu m$  @ 45nm,  $V_{dd}=1V$

- Min size:

■  $I_{drive}=1200\mu A/\mu m * 45nm = 54\mu A$   
■  $R_{out}=V_{dd}/I_{drive}=18k\Omega$

- W=370

■  $I_{drive}=1200\mu A/\mu m * 45nm * 370 = 20mA$   
■  $R_{out}=V_{dd}/I_{drive}=50\Omega$

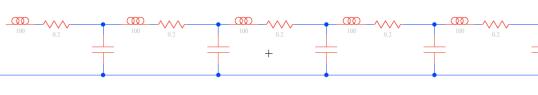


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## Lossy Transmission Line

- How do addition of R's change?

- Concretely, discretely think about  $R=0.2\Omega$  every meter on  $Z_0=100\Omega$
- what does each R do?



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## Lossy Transmission Line

- Each R is a mismatched termination

$$V_t = V_i \left( \frac{2(R + Z_0)}{(R + Z_0) + Z_0} \right)$$

- Each R is a voltage divider

$$V_{i+1} = V_i \left( \frac{Z_0}{R + Z_0} \right)$$



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### Lossy Transmission Line

$$V_{i+1} = V_i \left( \frac{2(R + Z_0)}{(R + Z_0) + Z_0} \right) \left( \frac{Z_0}{R + Z_0} \right)$$

$$V_{snk} = V_{src} \left( \left( \frac{2(R + Z_0)}{(R + Z_0) + Z_0} \right) \left( \frac{Z_0}{R + Z_0} \right) \right)^N$$



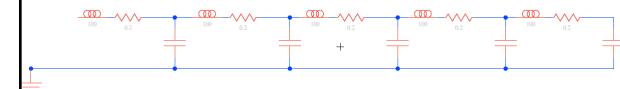
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### Lossy Transmission Line

- How long before drop voltage by half?
- $R=0.2\Omega$  every meter on  $Z_0=100\Omega$

$$V_{snk} = V_{src} \left( \left( \frac{2(R + Z_0)}{(R + Z_0) + Z_0} \right) \left( \frac{Z_0}{R + Z_0} \right) \right)^N$$



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### More Examples...

Time Permitting



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### $Z_0=75, Z_1=50$ (Preclass 5)

- At junction:

- Reflects

$$V_r = (50-75)/(50+75)V_i = -0.2V_i$$

- Transmits

$$V_t = (100/(50+75))V_i = 0.8V_i$$



$$V_i \left( \frac{R - Z_0}{R + Z_0} \right) = V_r \quad V_i \left( \frac{2R}{R + Z_0} \right) = V_t$$

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### Impedance Change $Z_0=75, Z_1=50$ (Preclass 5)

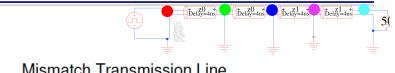
At junction:

Reflects

$V_r = -0.2V_i$

Transmits

$V_t = 0.8V_i$



Mismatch Transmission Line

$V_i = 0.8V$

$V_t = -0.2V_i$

$V_r = -0.2V_i$

$V_s = 1.0V$

$V_j = 0.8V$

$V_m = 0.6V$

$V_l = 0.4V$

$V_d = 0.2V$

$V_n = 0.0V$

$V_o = -0.2V$

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$V_l = 0.4V$

$V_d = 0.2V$

$V_n = 0.0V$

$V_o = -0.2V$

$V_r = -0.2V$

$V_t = 0.8V$

$V_s = 1.0V$

$V_j = 0.8V$

$V_m = 0.6V$

$V_l = 0.4V$

$V_d = 0.2V$

$V_n = 0.0V$

$V_o = -0.2V$

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$V_o = -0.2V$

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$V_t = 0.8V$

$V_s = 1.0V$

$V_j = 0.8V$

$V_m = 0.6V$

$V_l = 0.4V$

$V_d = 0.2V$

$V_n = 0.0V$

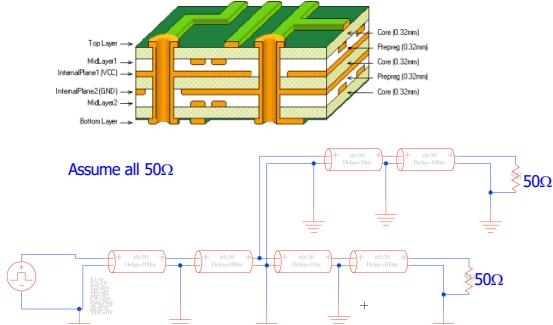
$V_o = -0.2V$

$V_r = -0.2V$

$V_t = 0.8V$

$V_s = 1.0V$

## What happens at branch?



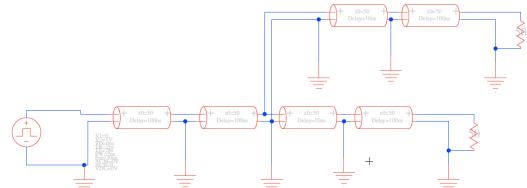
Assume all  $50\Omega$

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## Branch

- Transmission line sees two  $Z_0$  in parallel
  - Looks like  $Z_0/2$



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$Z_0=50, Z_1=25$

### At junction:

- Reflects
  - $V_r = (25-50)/(25+50)V_i = -0.33V_i$
- Transmits
  - $V_t = (50/(25+50))V_i = 0.67V_i$

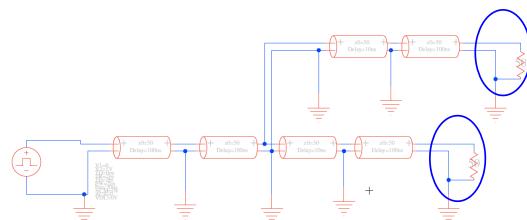
$$V_i \left( \frac{R - Z_0}{R + Z_0} \right) = V_r \quad V_i \left( \frac{2R}{R + Z_0} \right) = V_t$$

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## End of Branch

- What happens at end?
  - If ends in matched, parallel termination
    - No further reflections



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Branch Simulation

### At junction:

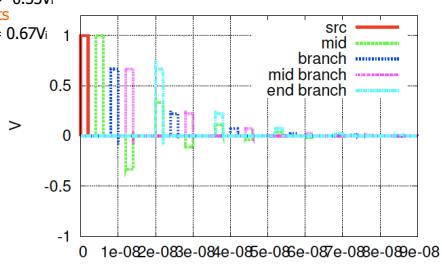
Reflects

$V_r = -0.33V_i$

Transmits

$V_t = 0.67V_i$

Branch LineTermination

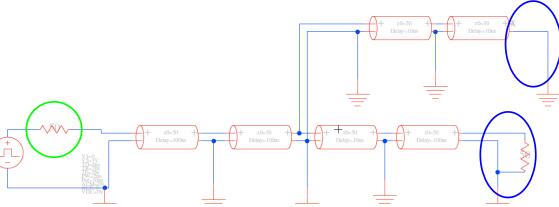


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## Branch with Open Circuit?

- What happens if branch open circuit?
- And source termination?



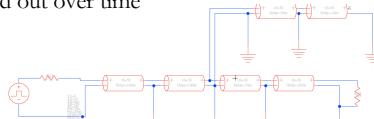
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## Branch with Open Circuit

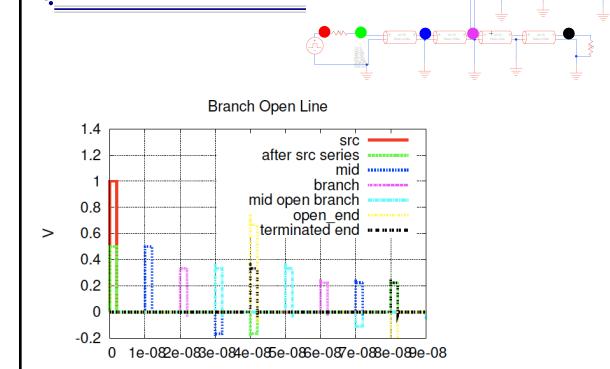
- ❑ Reflects at end of open-circuit stub
- ❑ Reflection returns to branch
  - ...and encounters branch again
  - Send transmission pulse to both
    - Source and other branch
- ❑ Sink sees original pulse as multiple smaller pulses spread out over time



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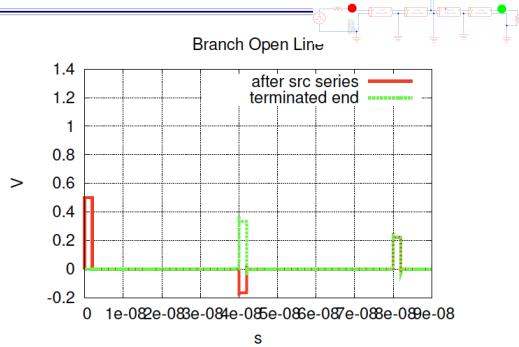
## Open Branch Simulation



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## Open Branch Simulation



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## Idea

- ❑ Transmission lines
  - high-speed
  - high throughput
  - long-distance signaling
  - termination

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## Admin

- ❑ Final Project
  - Design CLB
    - EC for best figure of merits
      - FOM = Area\*avgEnergy/maxFrequency
  - Due 12/10 (last day of class)
    - Can turn in up to 12/17 with no penalty

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