

Cadence Tutorial

for Cadence version 6.1

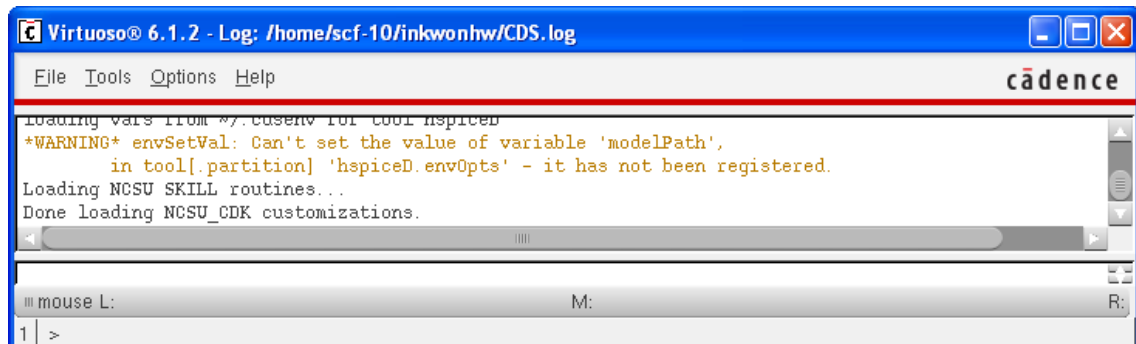
Inkwon Hwang

Feb, 2010

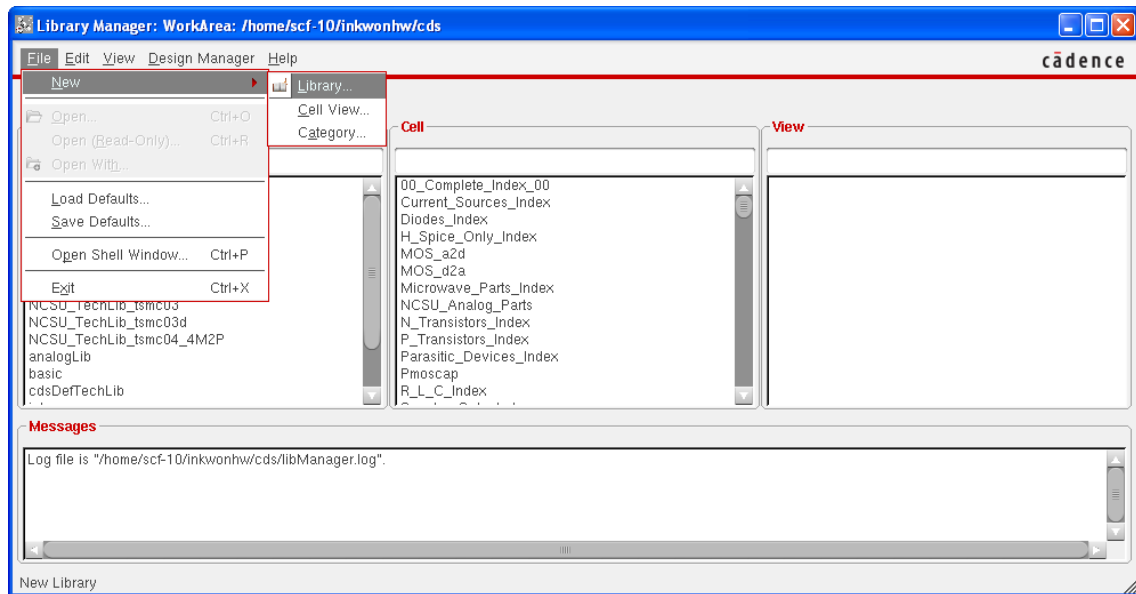
1. Create Library	2
2. Schematic.....	3
A. Create a cell view	3
B. Draw a schematic.....	4
3. Run Spectre simulation	9
A. Launch ADE (Analog Design Environment) L.....	9
B. Basic setup	10
C. Model Libraries	10
D. Simuli	11
E. Choose a type of analysis - transient.....	13
F. Select signals to plot.....	14
G. Run simulation.....	14
4. Layout	16
A. Create a layout	16
B. Add an instance - nmos	17
C. Add more instances – pmos, ptap, ntap, and m1_ploy	18
D. Draw metal1	19
E. Run DRC	20
F. Add pins.....	22
G. Extract	24
H. Run LVS.....	25
I. Run Spectre simulation	26

1. Create Library

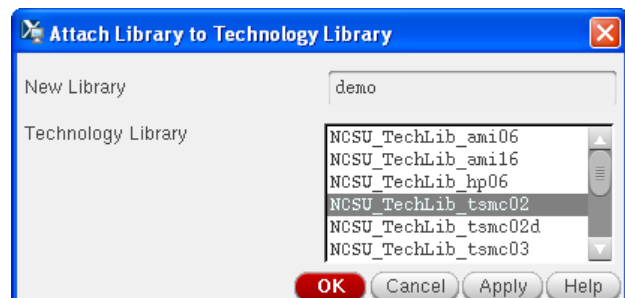
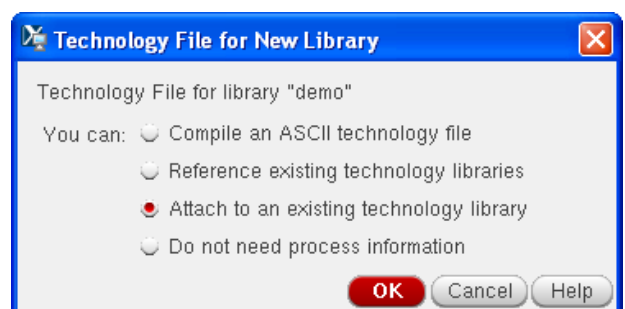
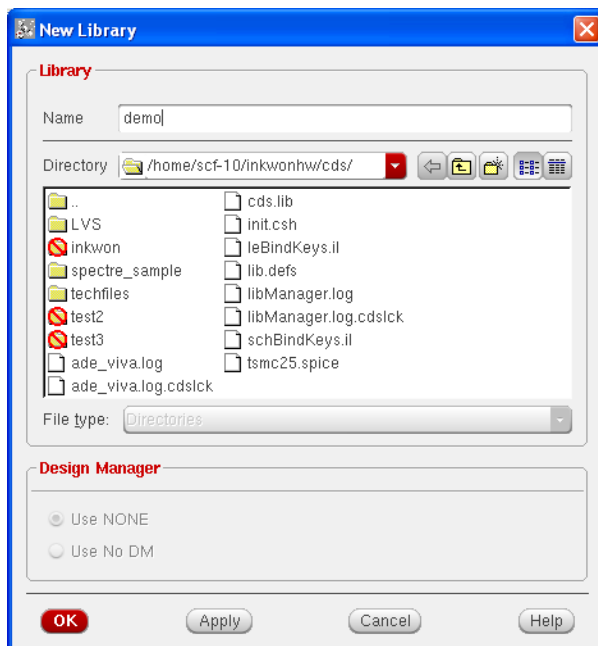
A. Tools → Library Manager



B. File → New → Library

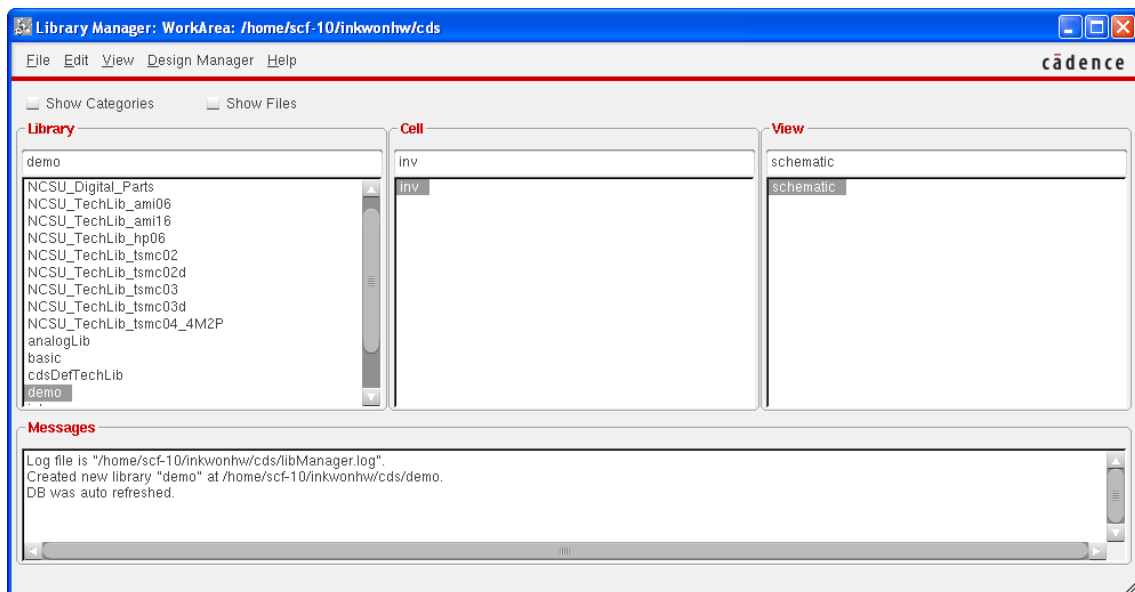
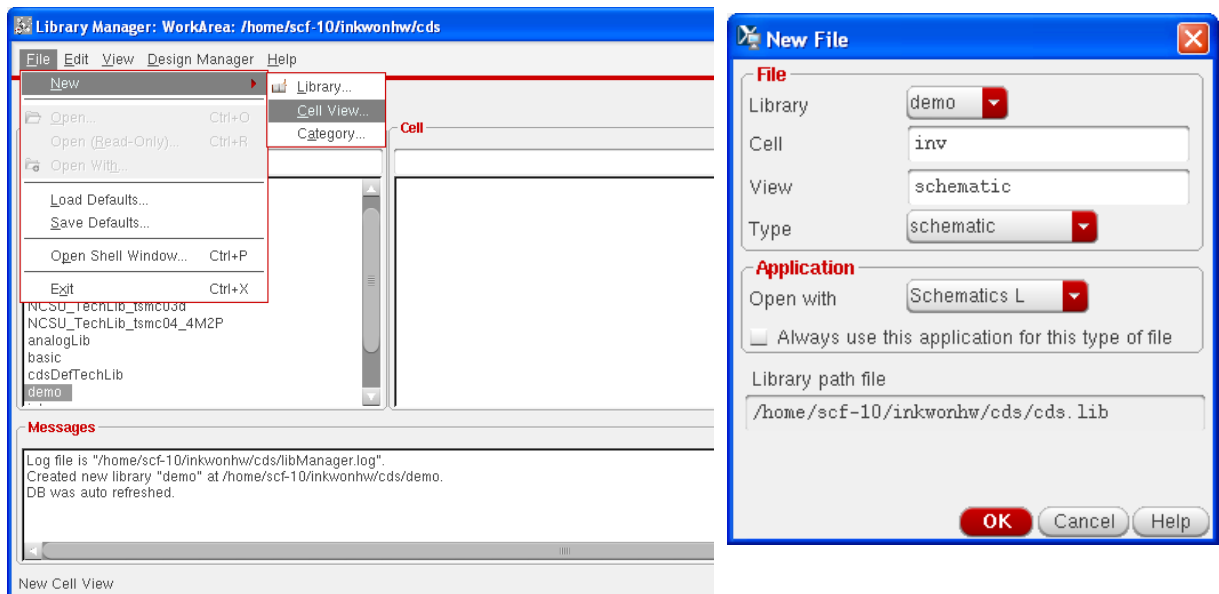


C. Give a name and attach it to a technology library



2. Schematic

A. Create a cell view

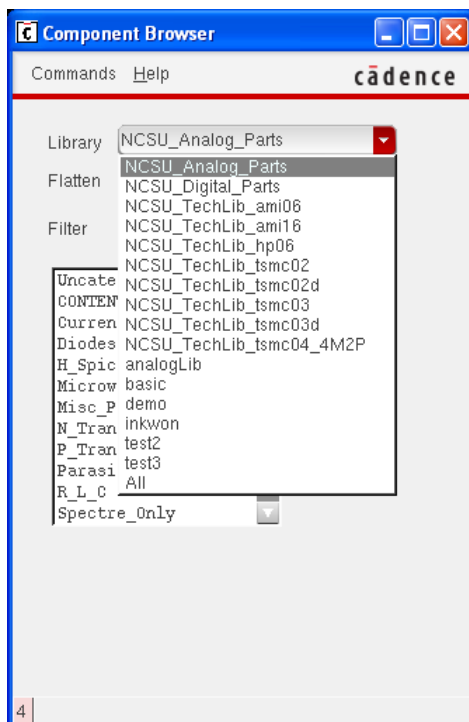
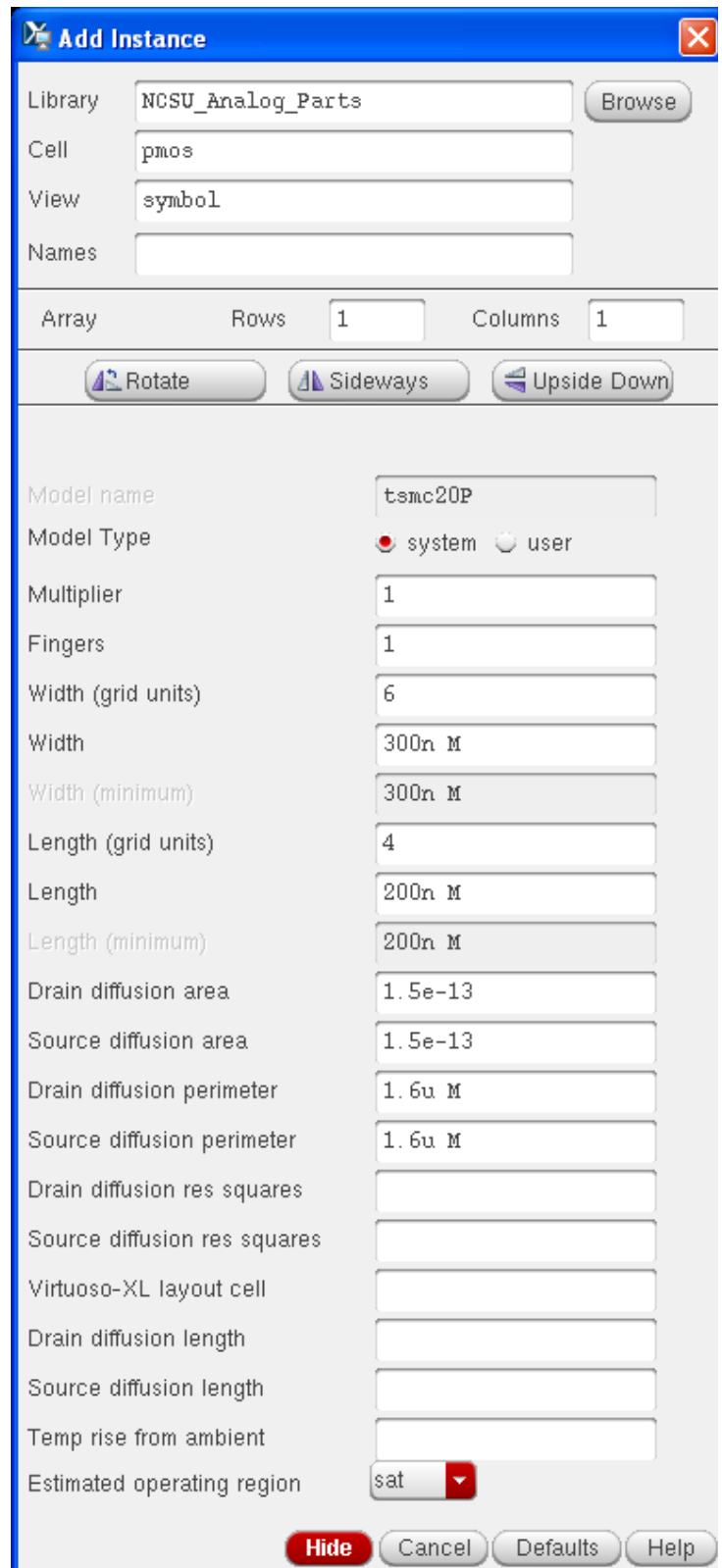
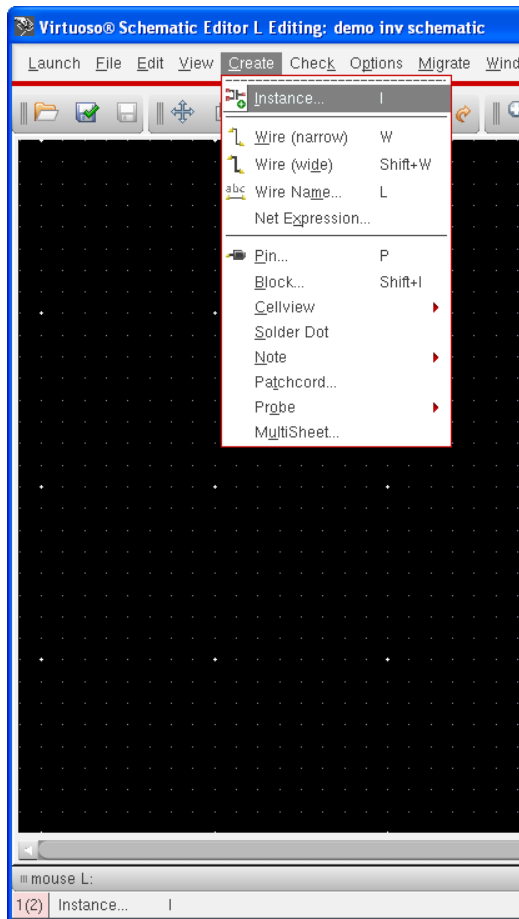


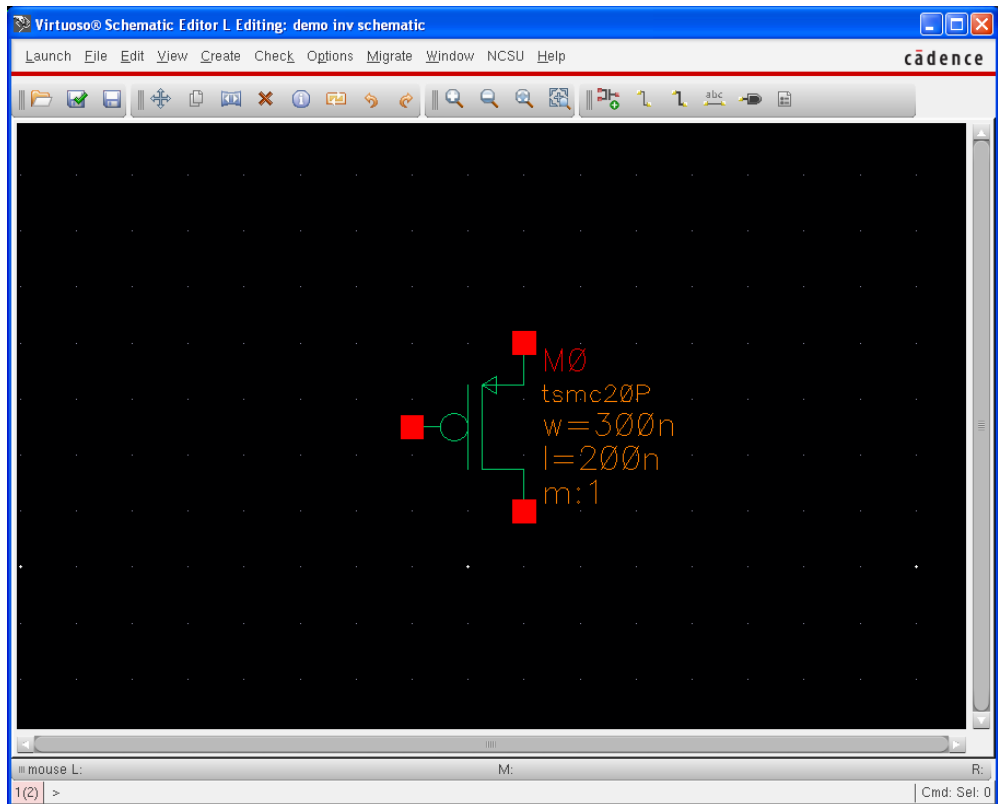
B. Draw a schematic

i. Add instances – pmos

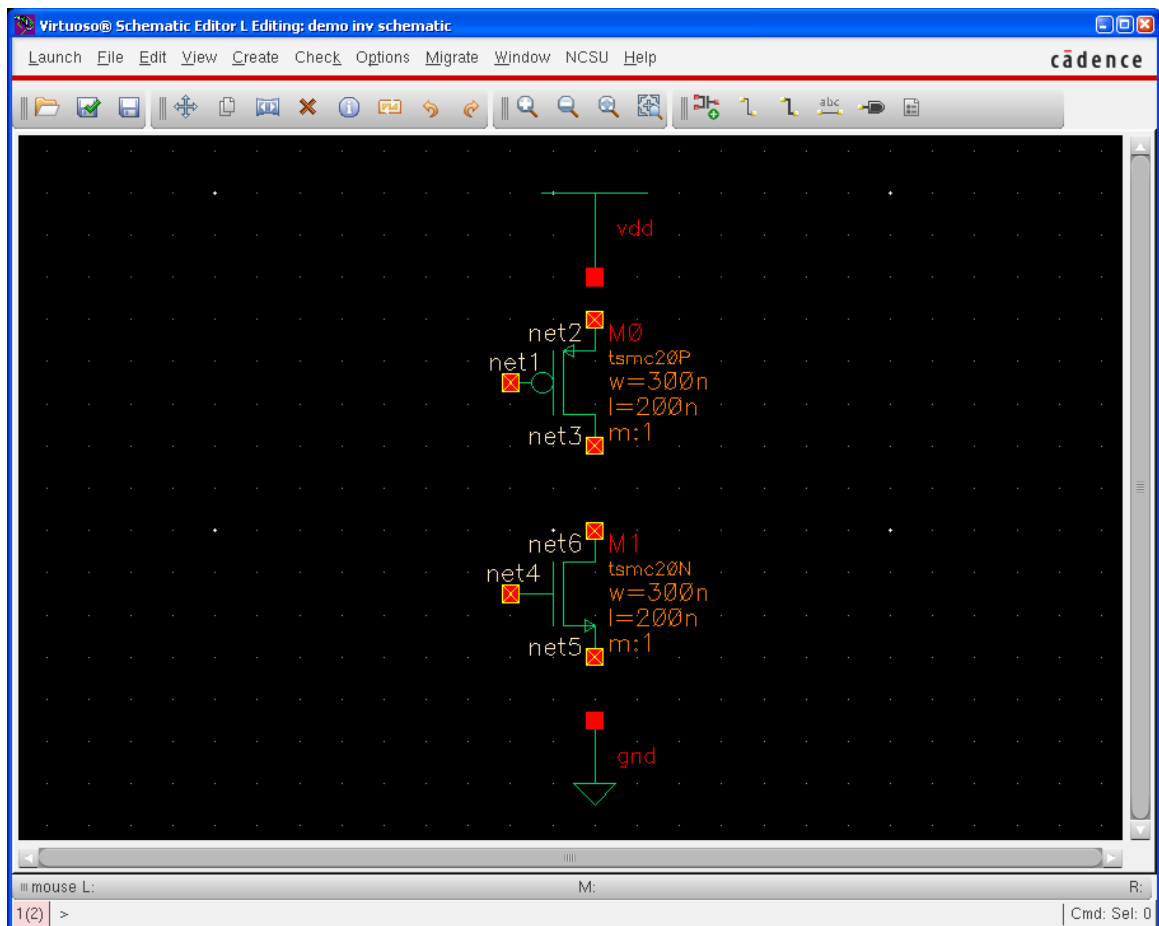
You can modify Width of transistors. Don't modify length unless you have a special purpose.

You should select a NCSU_Analog_Parts library.

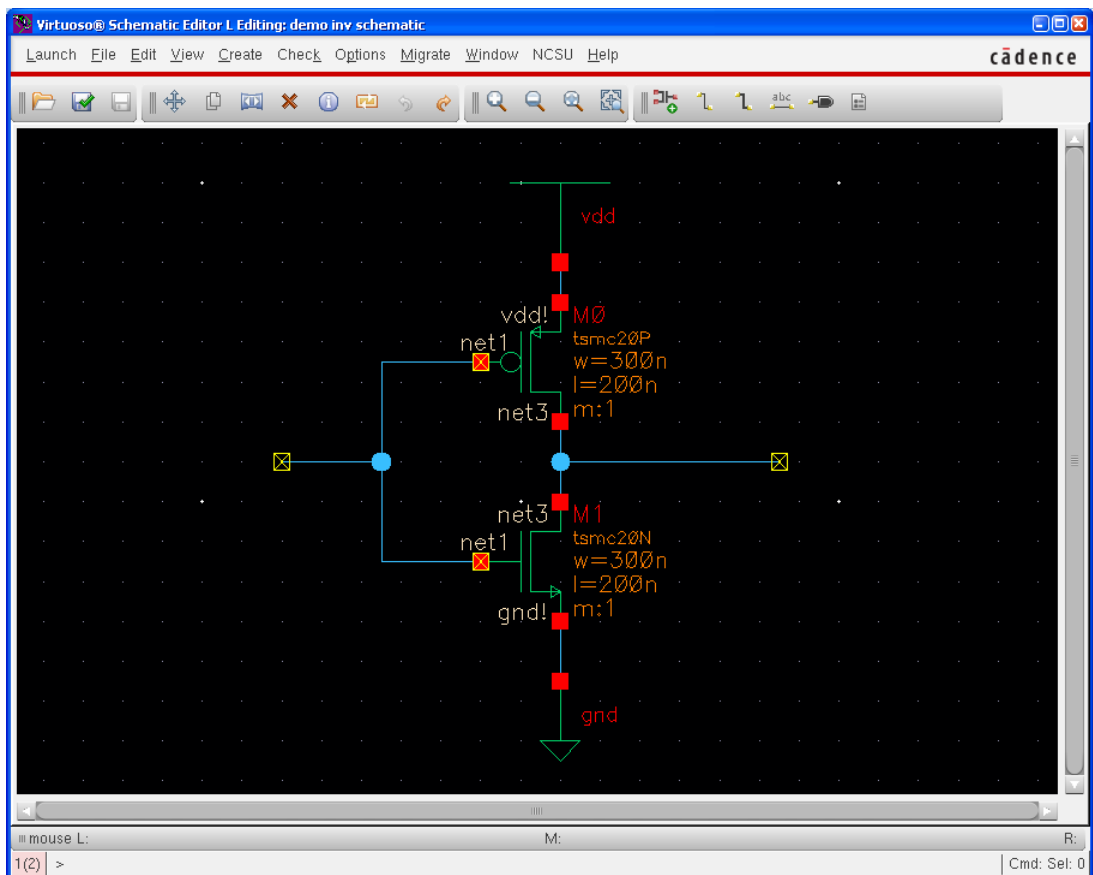
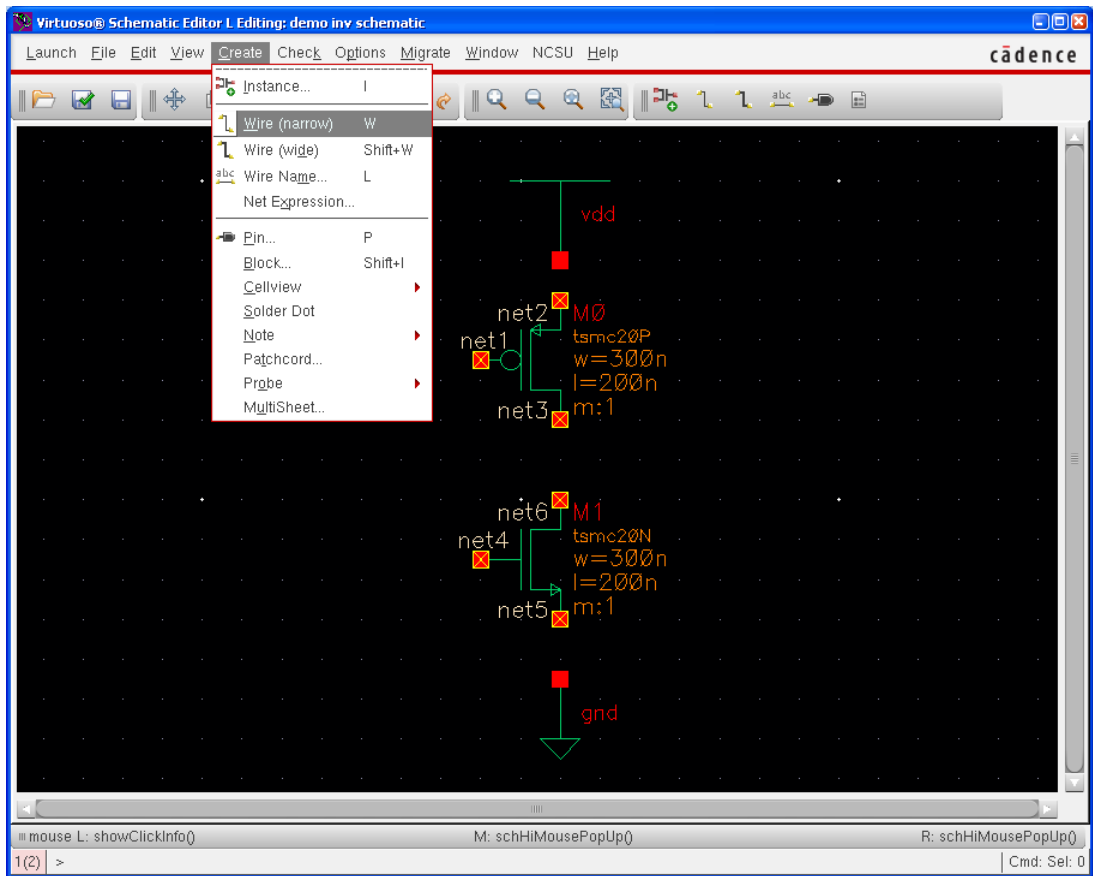




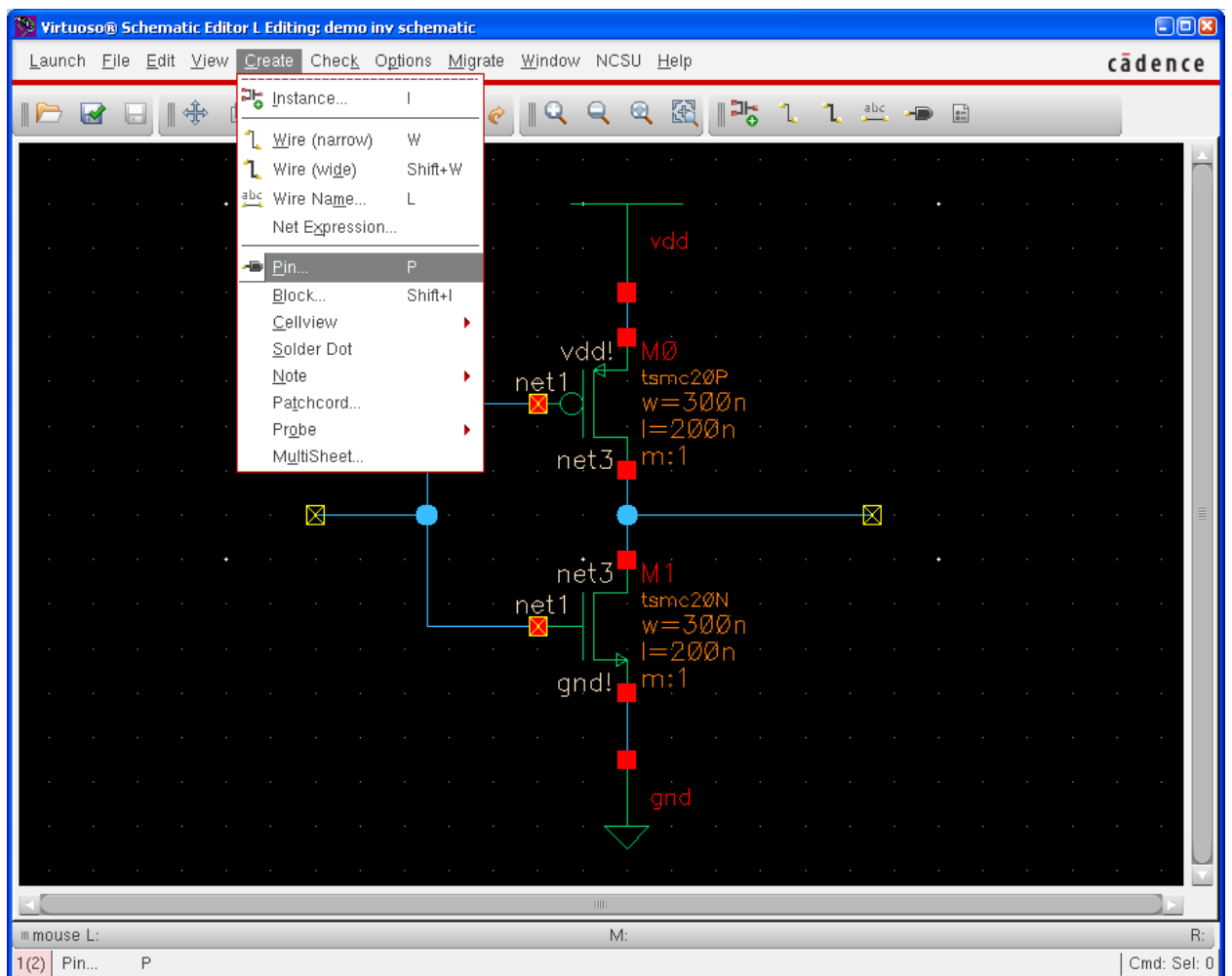
ii. Add instances – nmos, vdd, and gnd



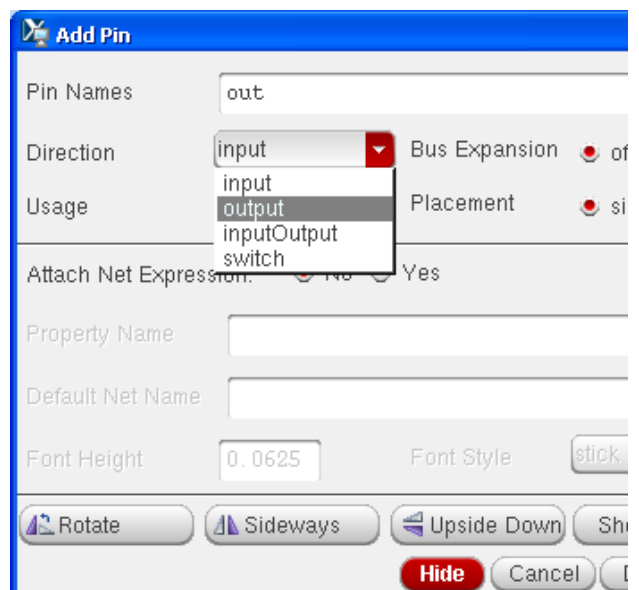
iii. Add wires: Create → Wire

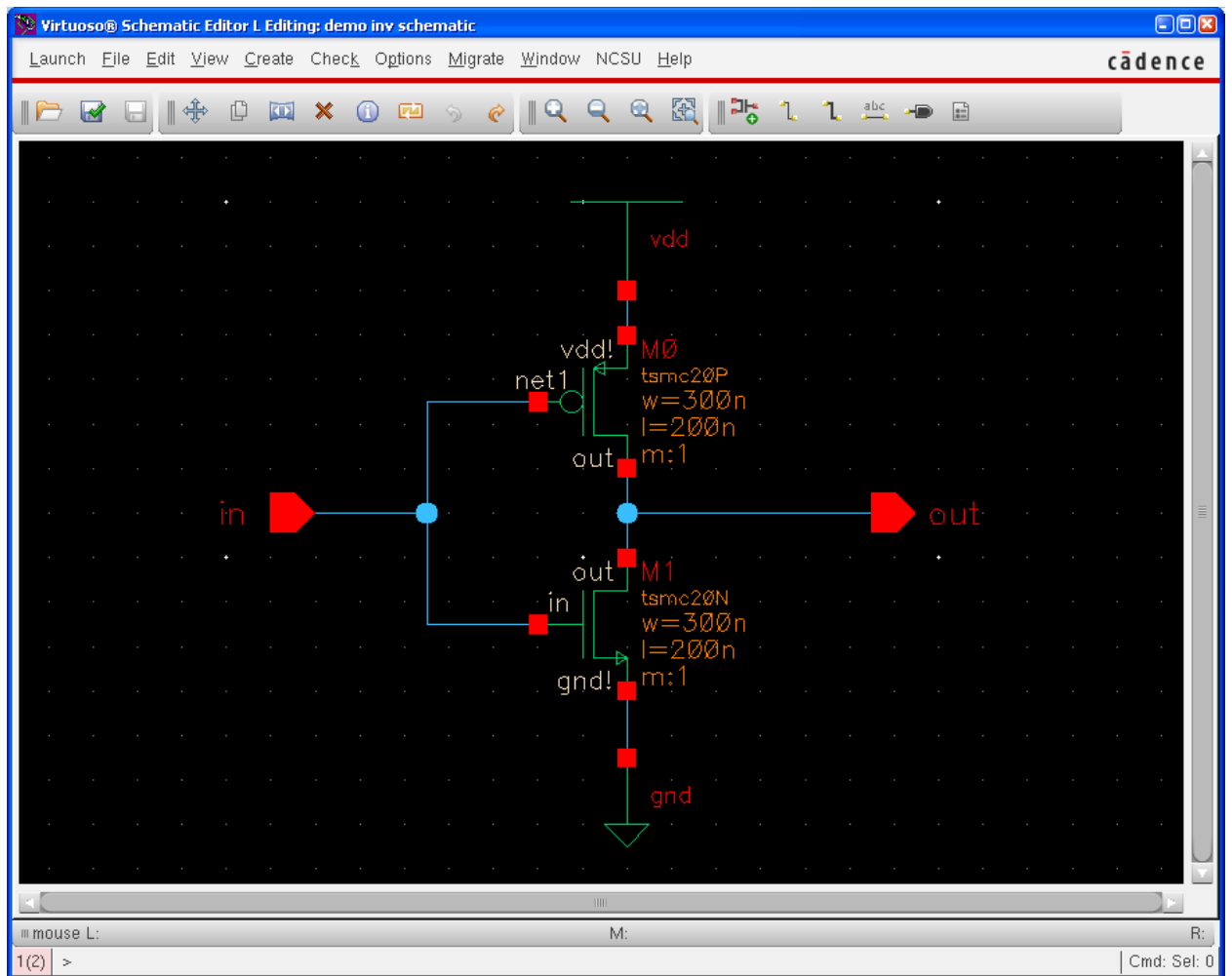


iv. Add pins: Create → Pin



We have for different types of direction. For schematics, we only use two types, input and output. InputOutput type is for supply changes, and it is necessary only for layout. We will discuss about this later.





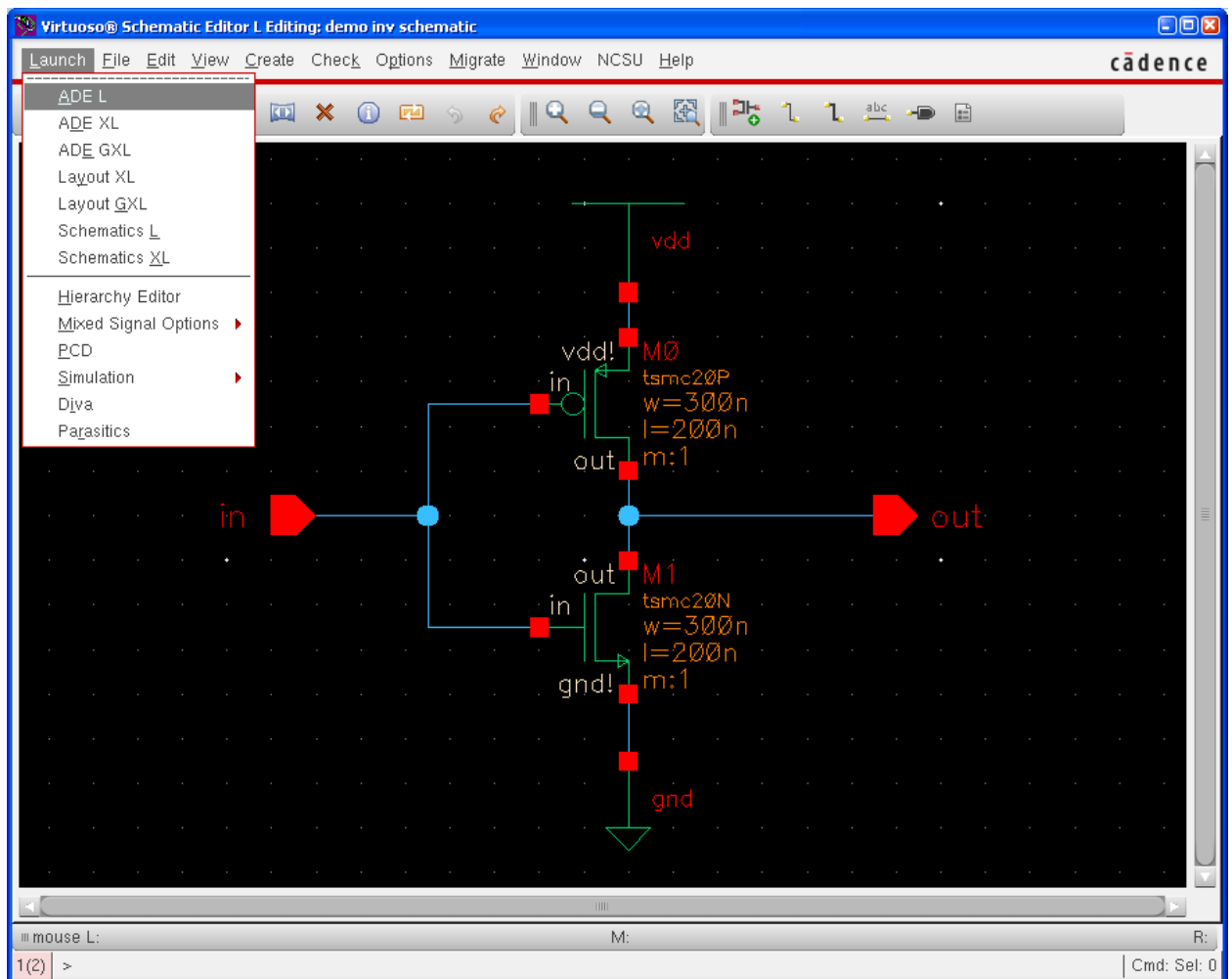
Now, we completed a schematic design. Let's move on the next phase.

3. Run Spectre simulation

We will run spectre simulation. This section is for **both** schematics and layouts. I will show an example for a schematic. You can do the same thing for a layout.

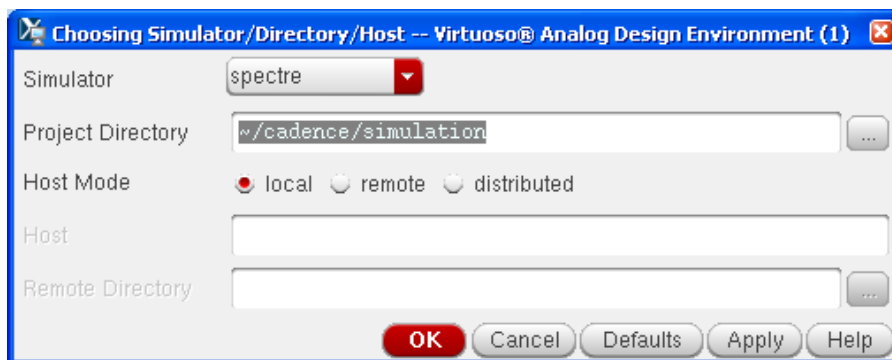
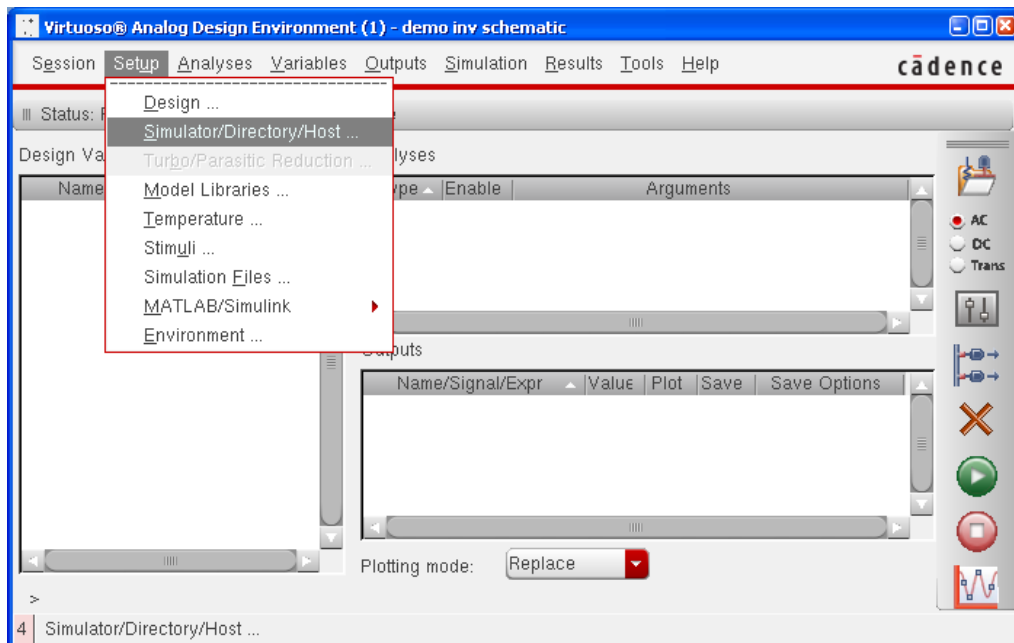
A. Launch ADE (Analog Design Environment) L

Launch → ADE L



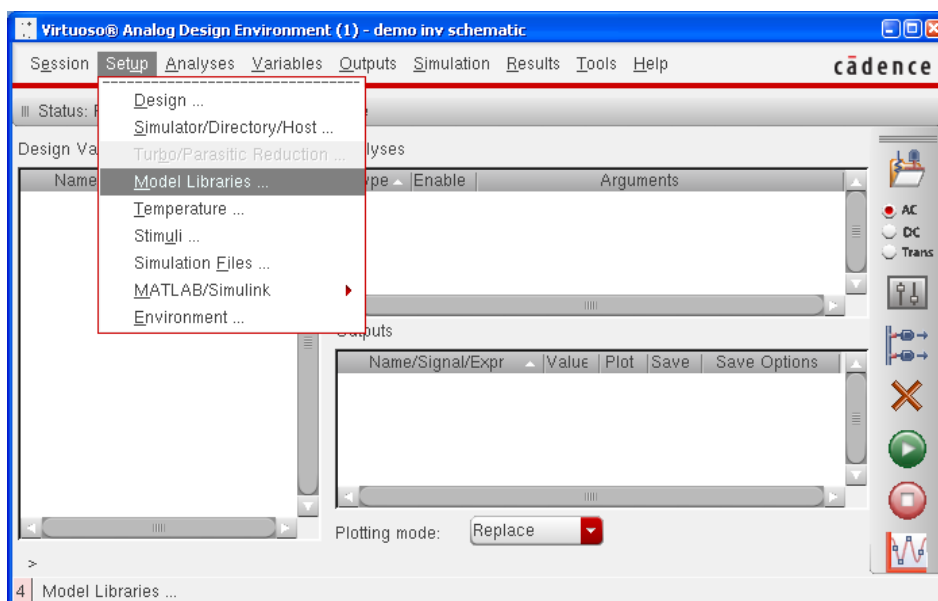
B. Basic setup

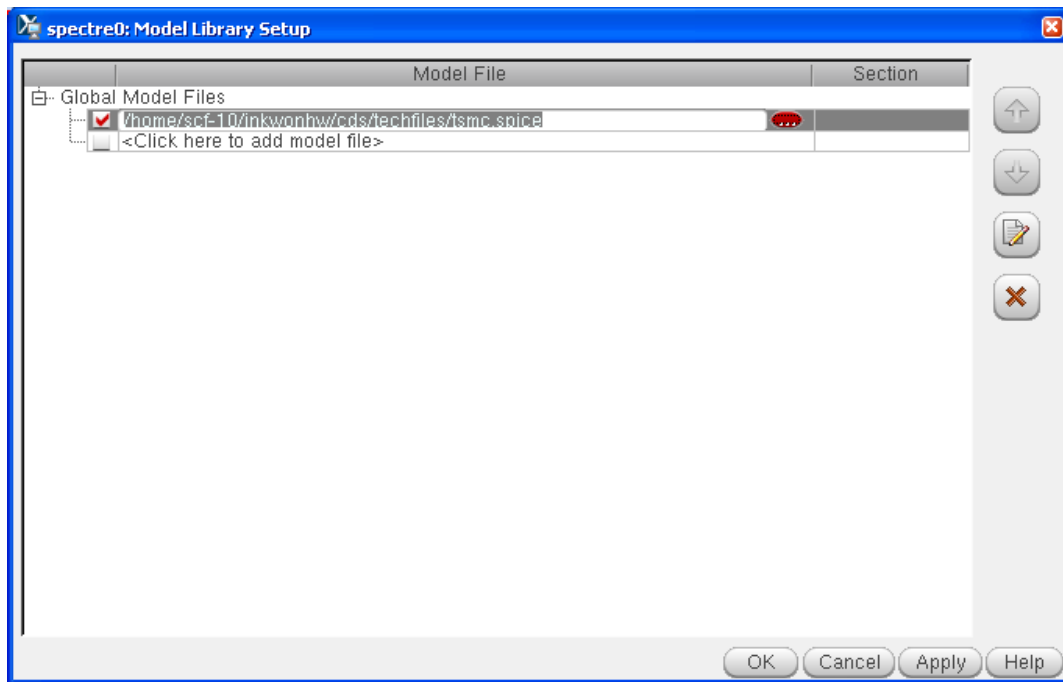
Check if your simulator is spectre. You can modify project directory.



C. Model Libraries

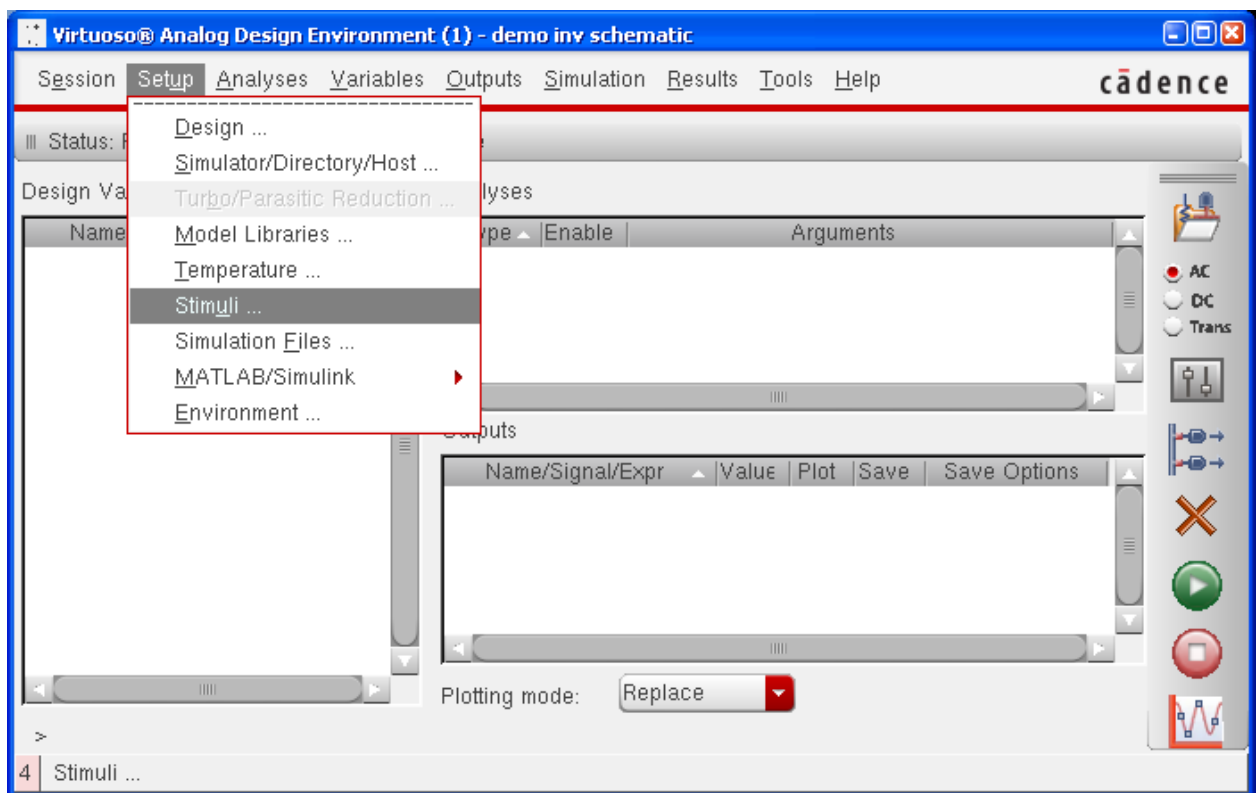
You can download a library file at the DEN blackboard.





D. Simuli

Define input signals include supply nets



Global sources

Setup Analog Stimuli

Stimulus Type

☐ Inputs

☒ Global Sources

ON

vdd! /gnd!

Voltage dc

"DC voltage"=1.5

Enabled ☒

Function

dc

Type

Voltage

DC voltage

1.5

AC magnitude

AC phase

XF magnitude

PAC magnitude

PAC phase

Temperature coefficient 1

Temperature coefficient 2

Nominal temperature

Source type

dc

Noise file name

Number of noise/freq pairs

0

Freq 1

Noise 1

Freq 2

Noise 2

Freq 3

OK

Cancel

Apply

Input

Setup Analog Stimuli

Stimulus Type

☒ Inputs

☐ Global Sources

ON

in /gnd!

Voltage pulse

"Voltage 1"=0 "Voltage 2"=1.5

Enabled ☒

Function

pulse

Type

Voltage

DC voltage

AC magnitude

AC phase

XF magnitude

PAC magnitude

PAC phase

Voltage 1

0

Voltage 2

1.5

Period

2n

Delay time

0

Rise time

200p

Fall time

200p

Pulse width

1n

Temperature coefficient 1

Temperature coefficient 2

Nominal temperature

Source type

pulse

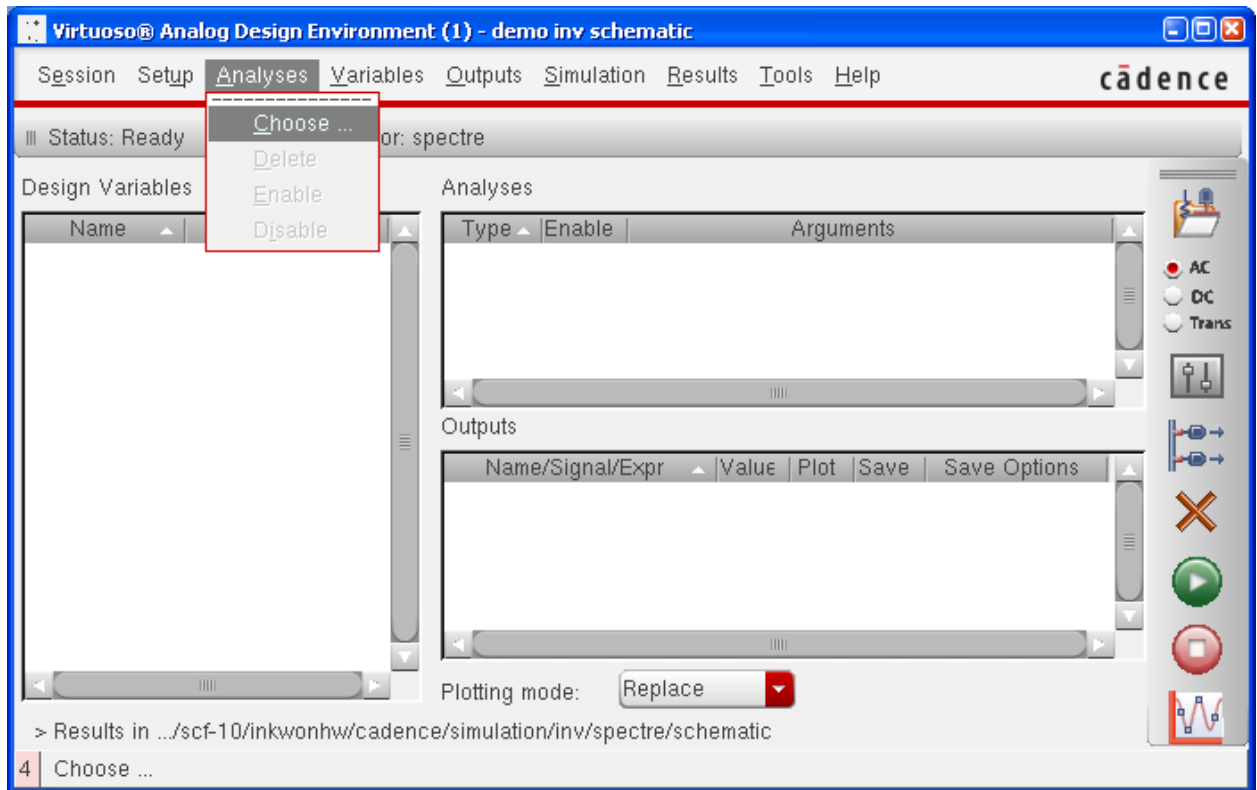
OK

Cancel

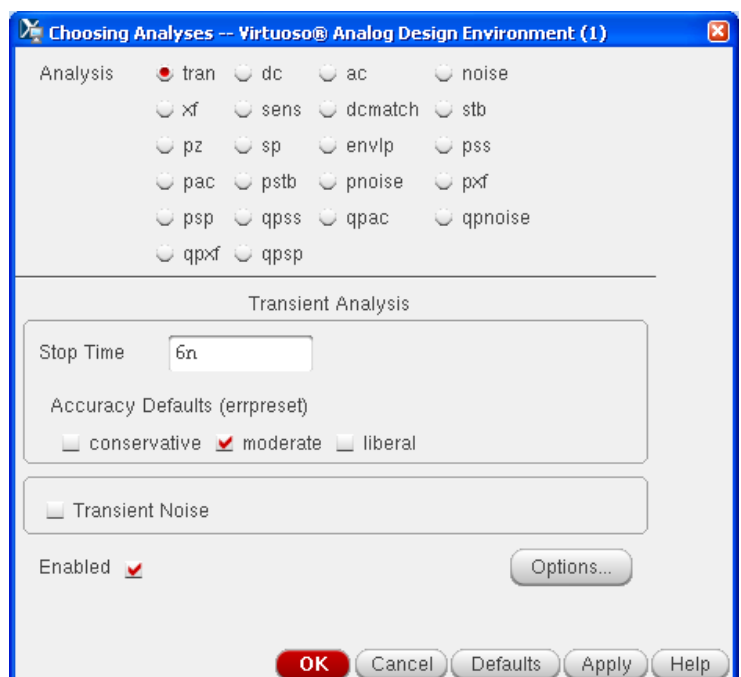
Apply

E. Choose a type of analysis - transient

You can choose 'dc' if you want to do dc analysis



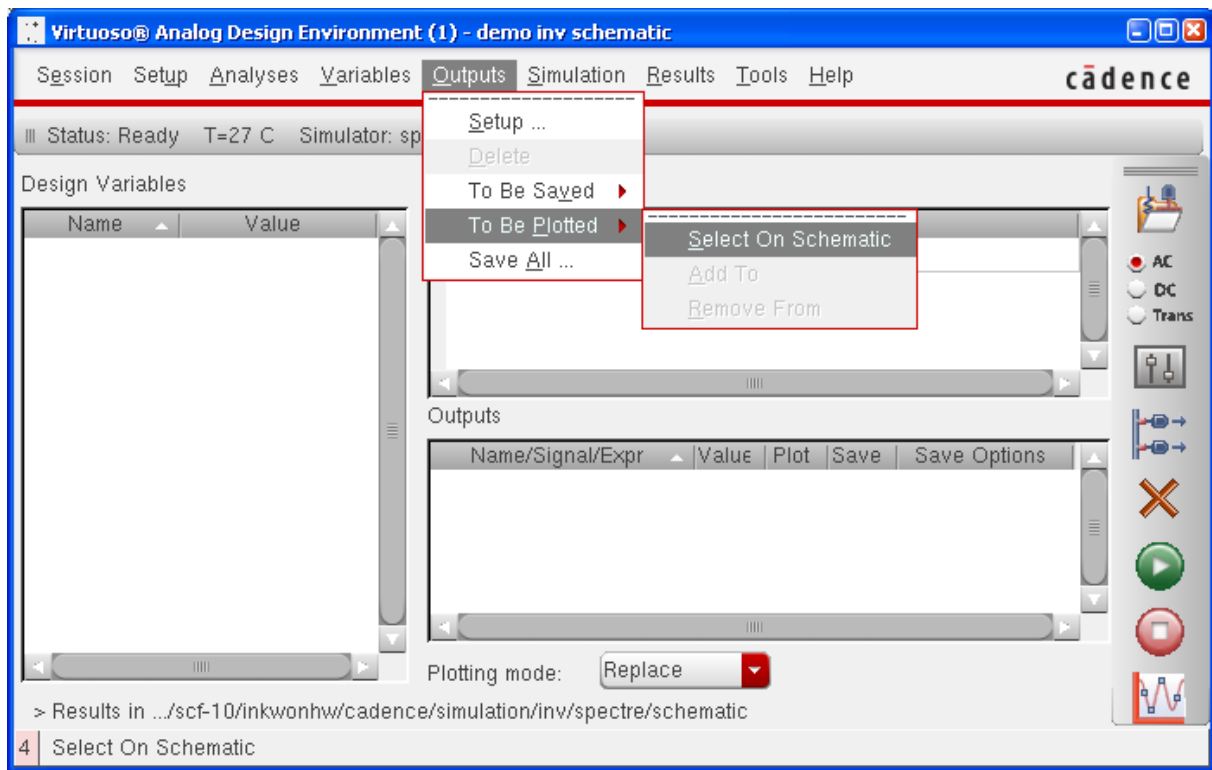
- A. Choose tran
- B. Give Stop time which means how long you want to simulate
- C. Select moderate as accuracy defaults
- D. Do not check Transient Noise
- E. Check Enabled



F. Select signals to plot

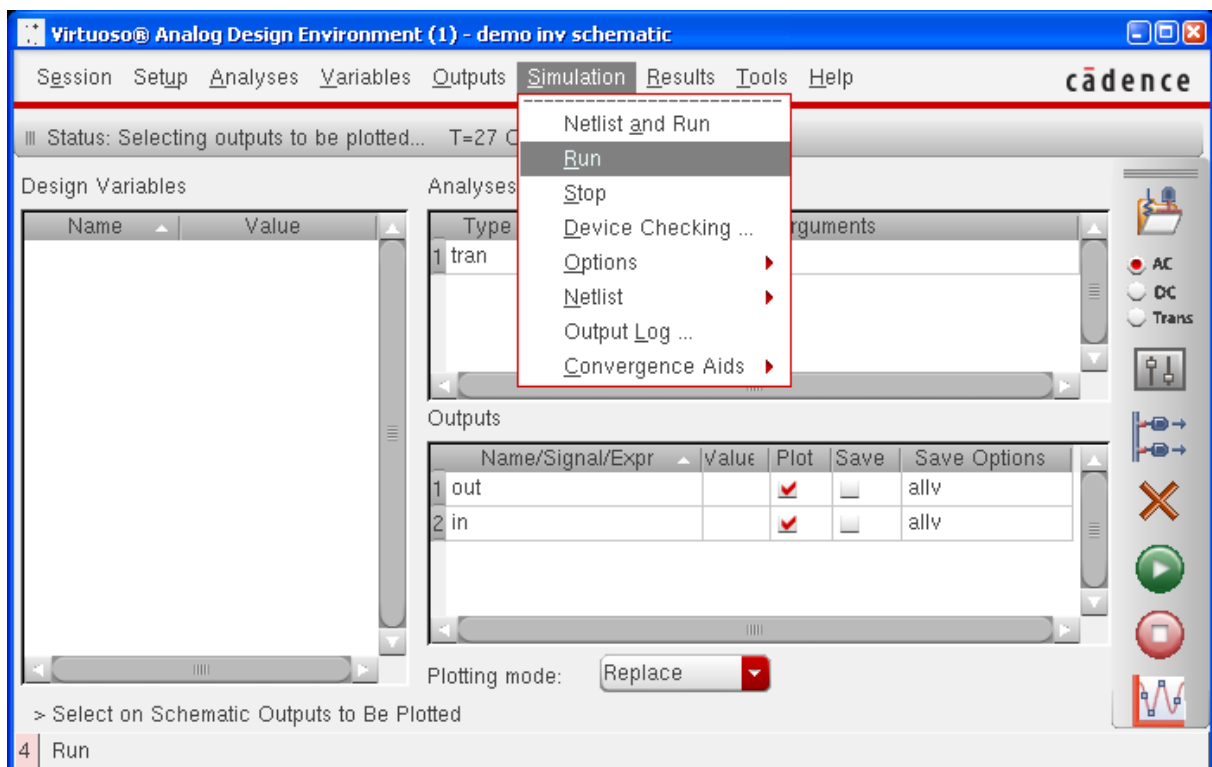
Outputs → To Be Plotted → Select On Schematic

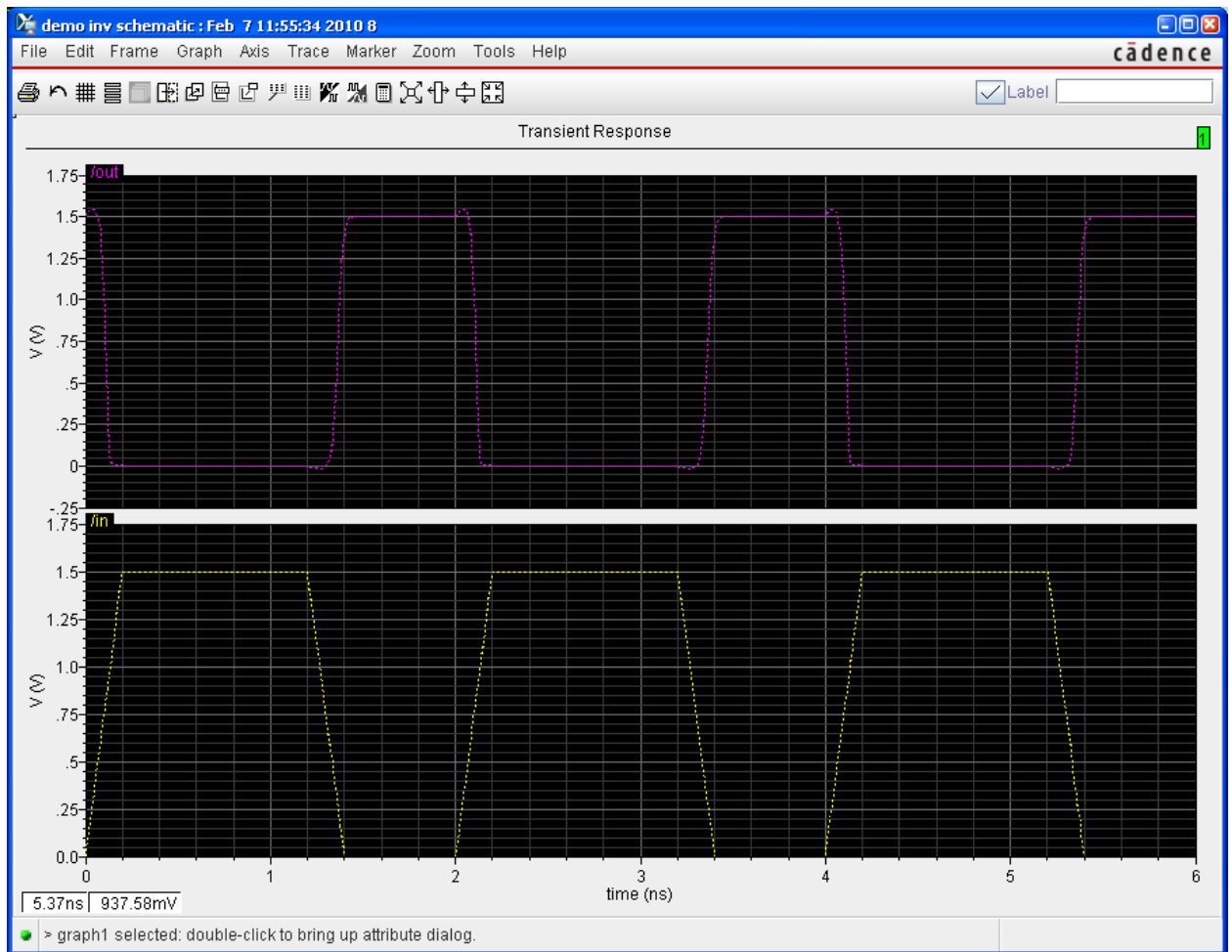
Click a signal (Pin) on a schematic/extracted.



G. Run simulation

Simulation → Run





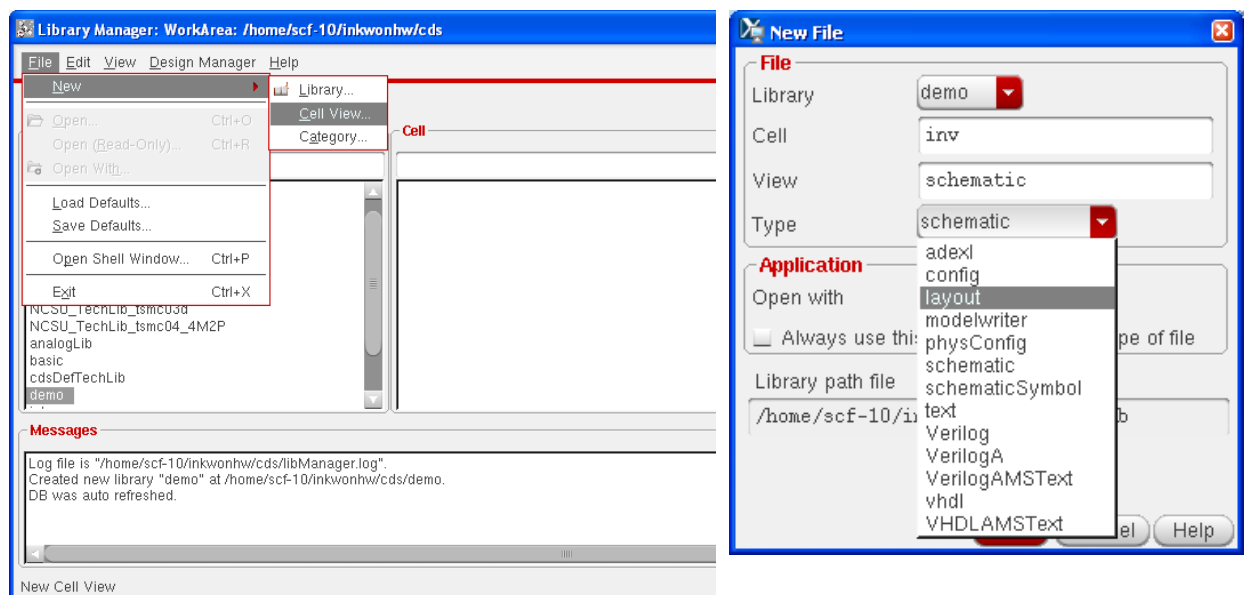
If you see a waveform like above picture, you followed every step properly.
Good job!.

4. Layout

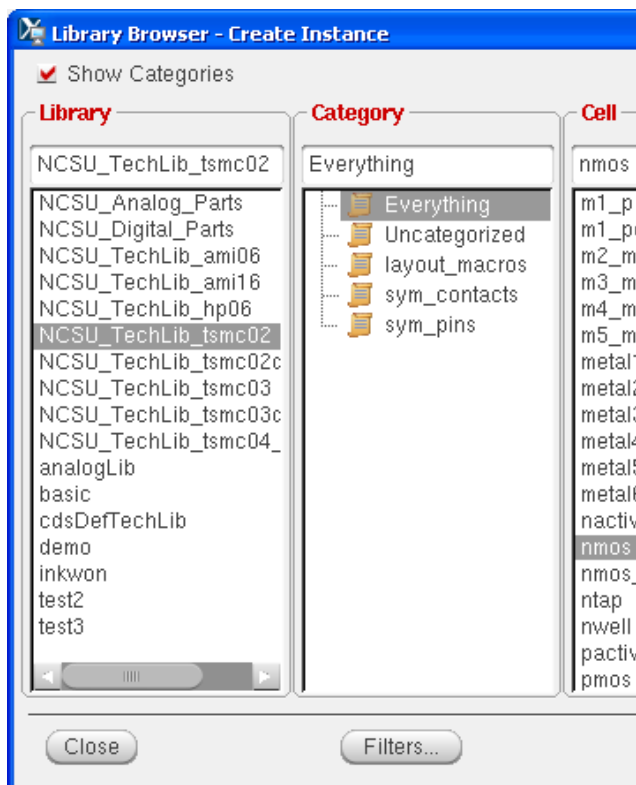
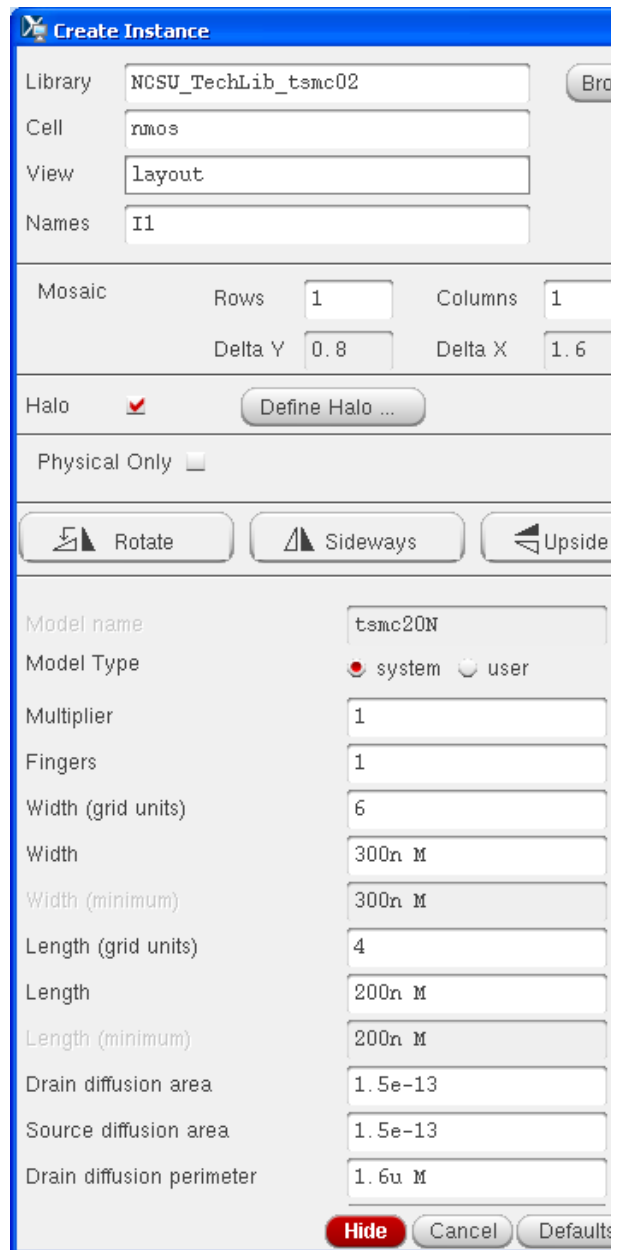
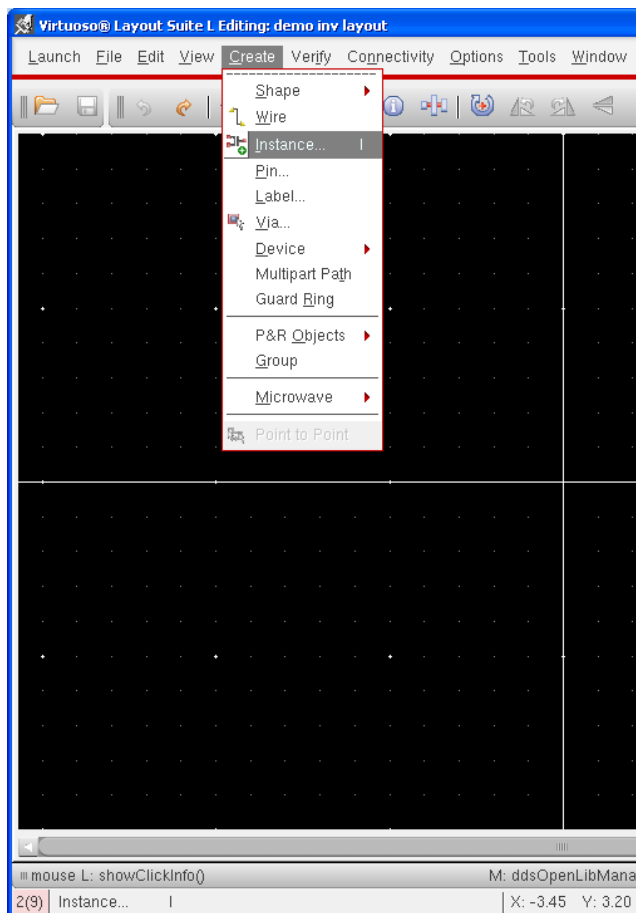
It's time to draw layout. Schematics are for verifying your design very roughly. They don't consider physical features like parasitic capacitances. After determining your design variables by schematics, you need to draw layouts.

Design flow of layouts is very similar to one of schematics, but it has additional step which is LVS check. It is for check if your layout is identical to the schematic or not. Hence, this step is very important. If your logic doesn't pass this step, you may lose significant points for that.

A. Create a layout

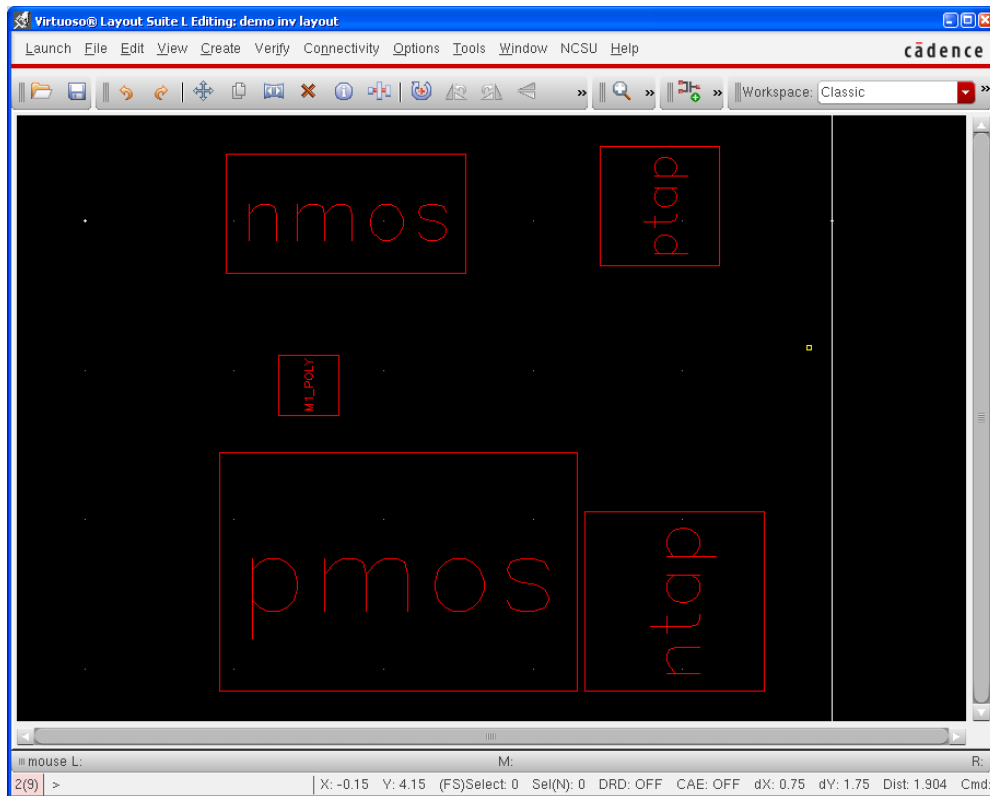


B. Add an instance - nmos

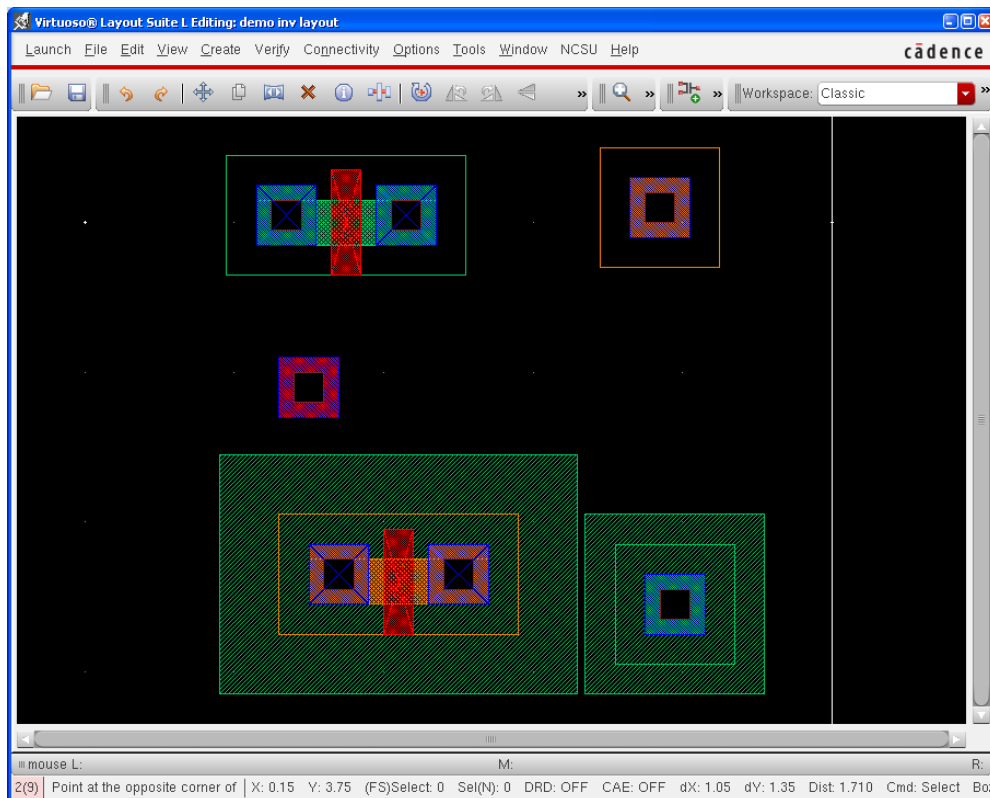


You can modify width of transistors.

C. Add more instances – pmos, ptap, ntap, and m1_ploy



You can select alternate view of a layout. Try 'Shift + f' and 'Ctrl + f'.

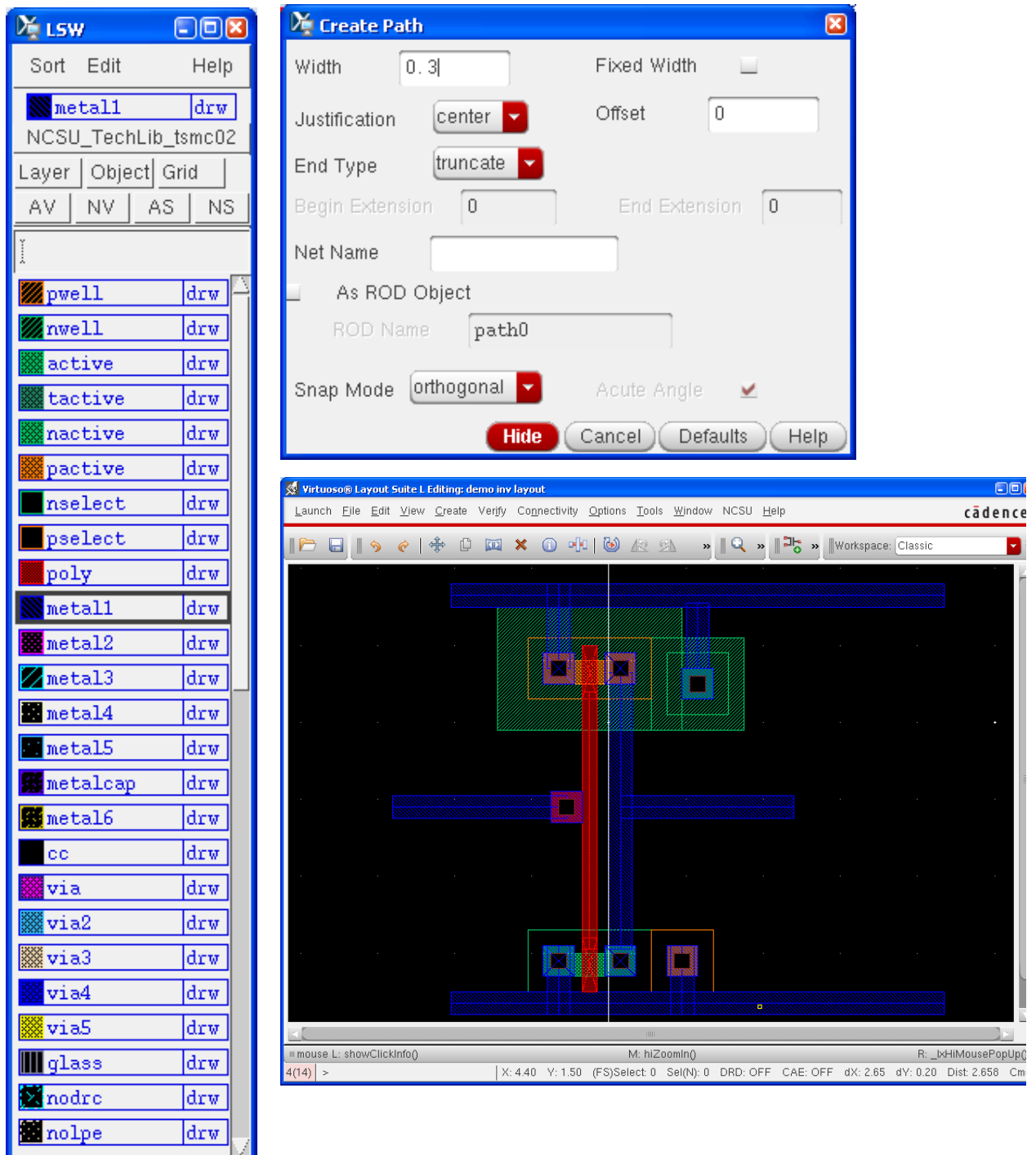


D. Draw metal1

There are few ways for drawing metal, but I recommend you use 'path'. It's quite convenience than others.

Create → Shape → Path

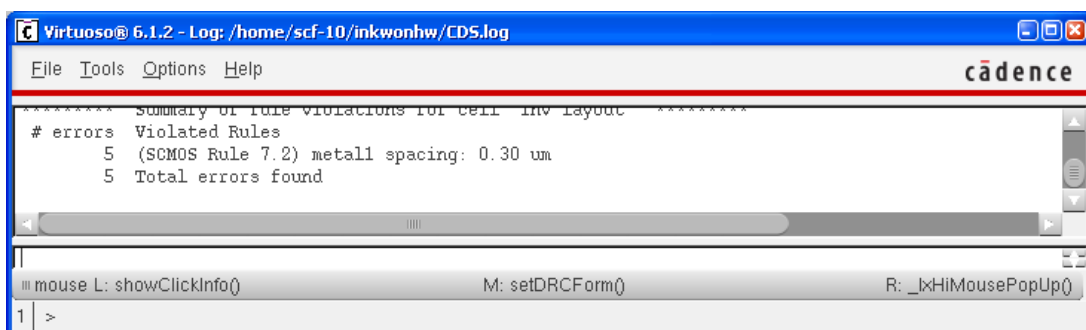
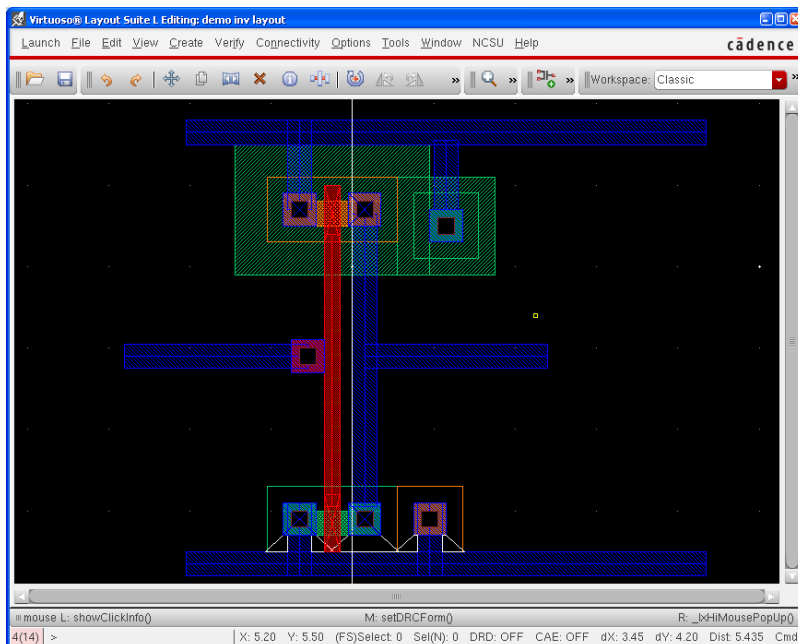
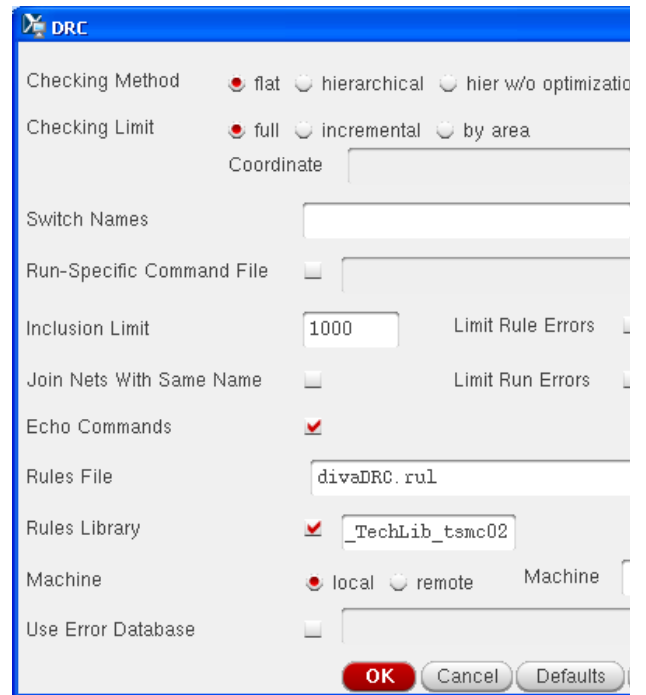
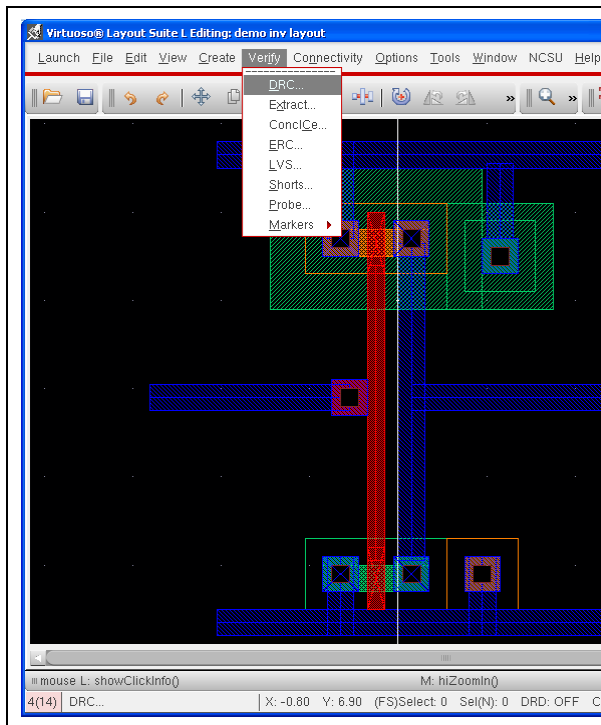
First of all, you should select metal1 on LSW window. Default width for metal1 is 0.3, which means 300nm (3 λ). You can draw metal layer simply by clicking



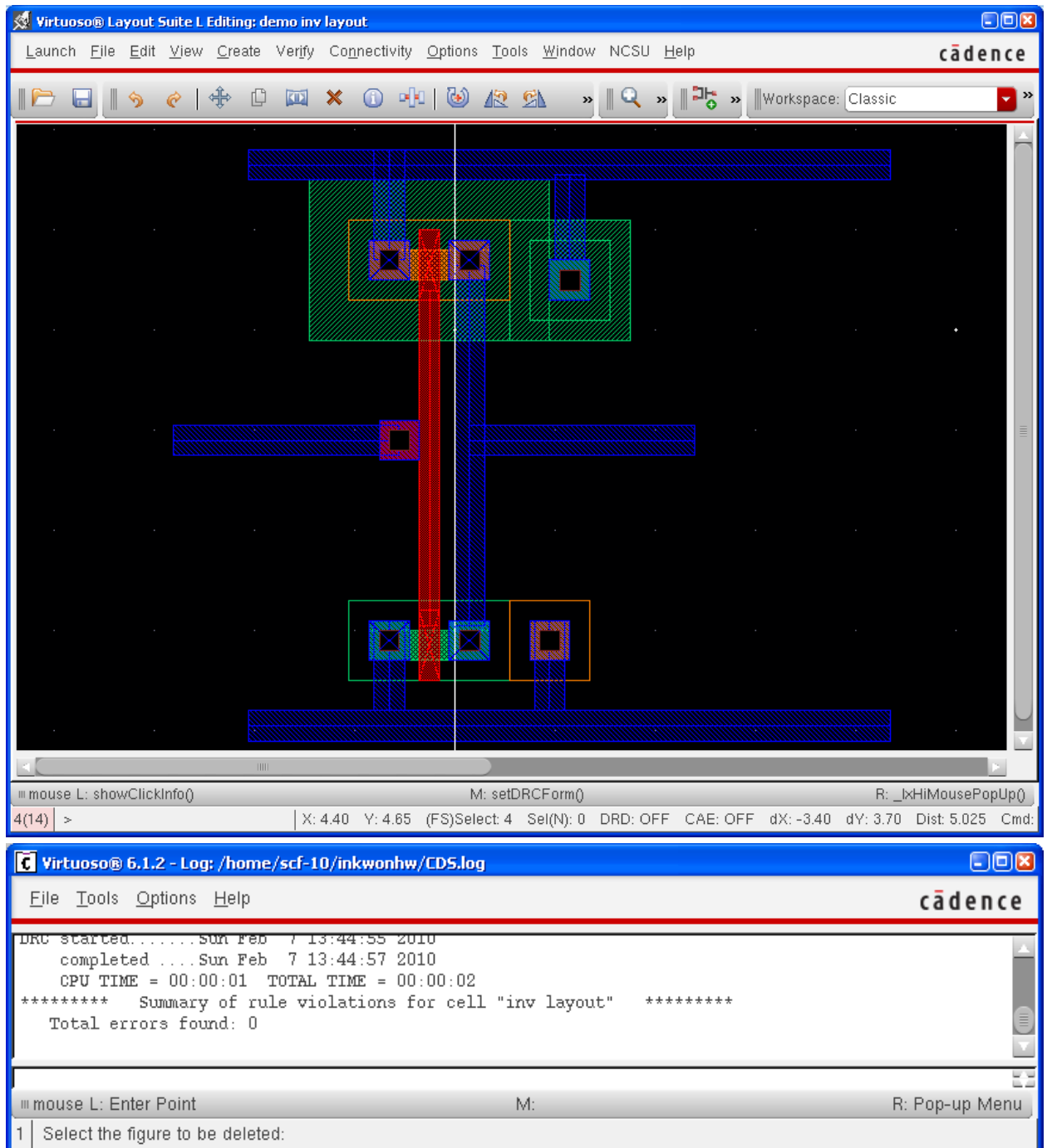
E. Run DRC

This step checks if your layout follows design rules.

Verify → DRC



We have five errors. It is because a gnd metal layer is too close to an nmos transistor. After modifying layout, run DRC again.

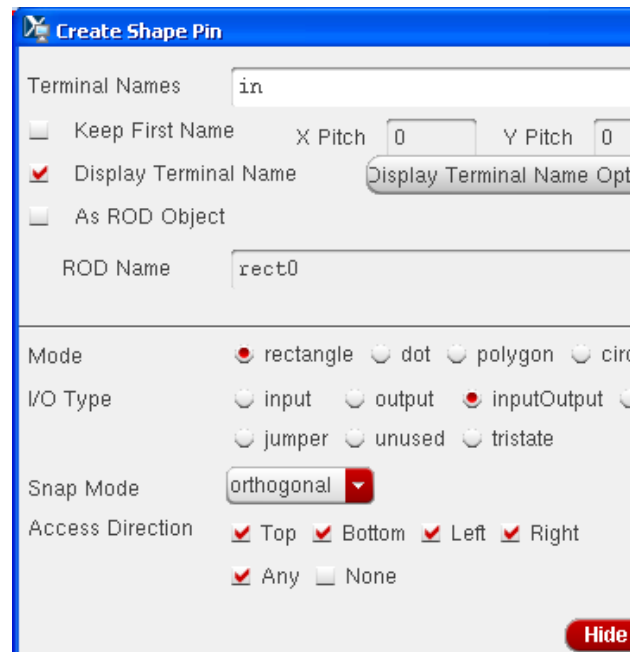
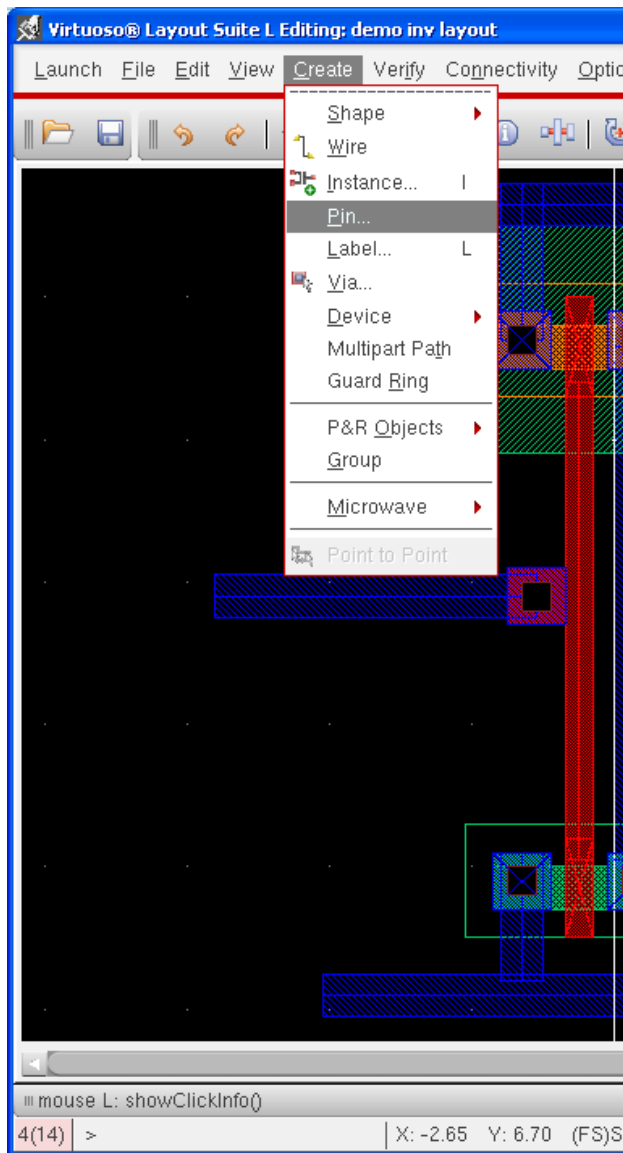


There is no error!!

F. Add pins

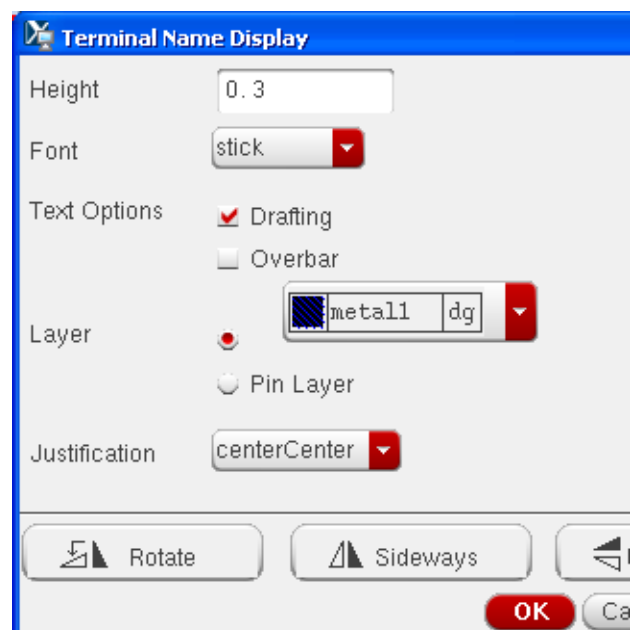
We had two pins on a schematic, which are 'in' and 'out'. Pins are for assigning signals to physical device, so we assign voltage level of gnd and vdd by using pins. Hence, we have 4 pins for the layout, which are 'in', 'out', 'gnd!', and 'vdd!'.

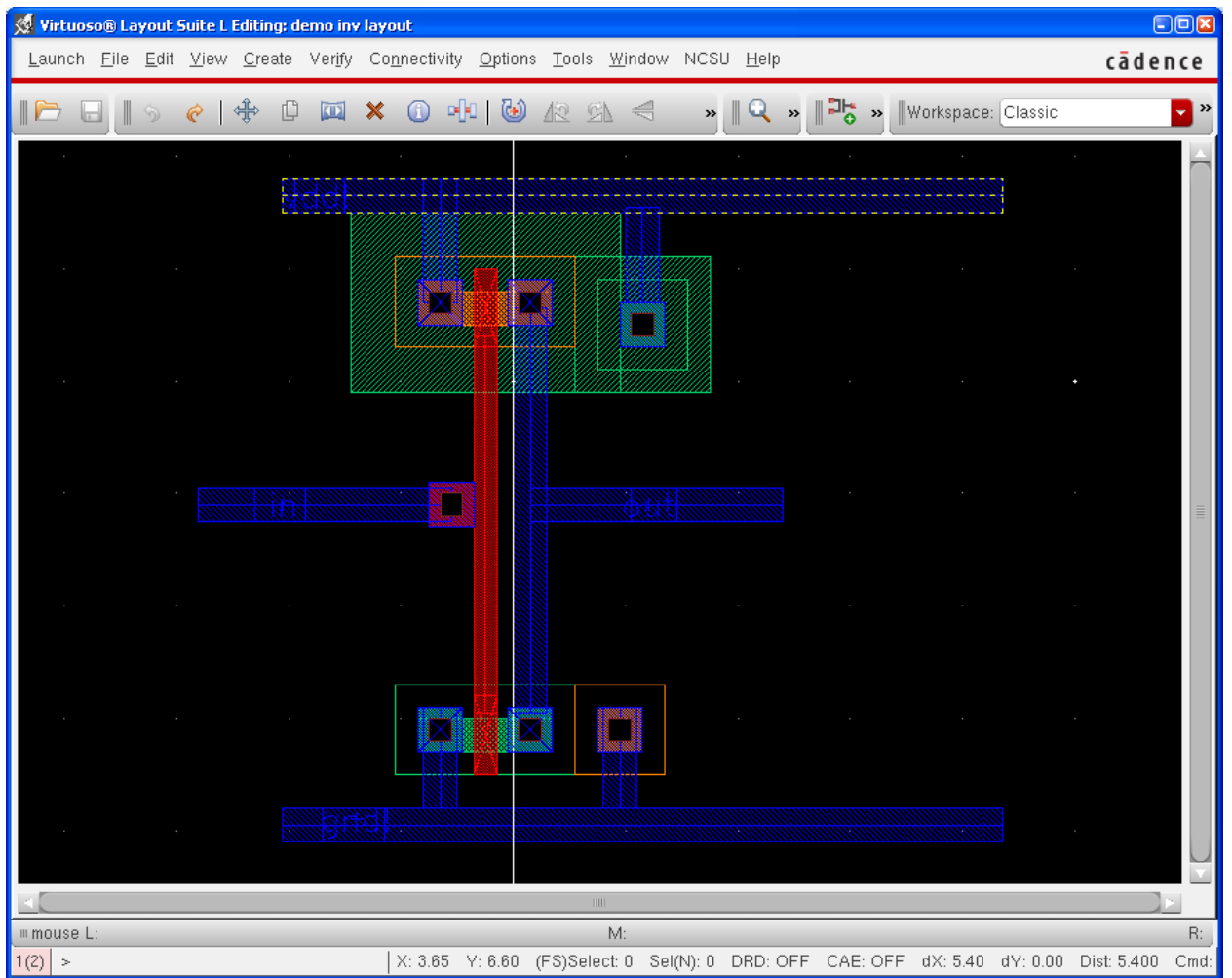
Create → Pin



Check 'Display Terminal Name' if you want to see pin name on the layout.

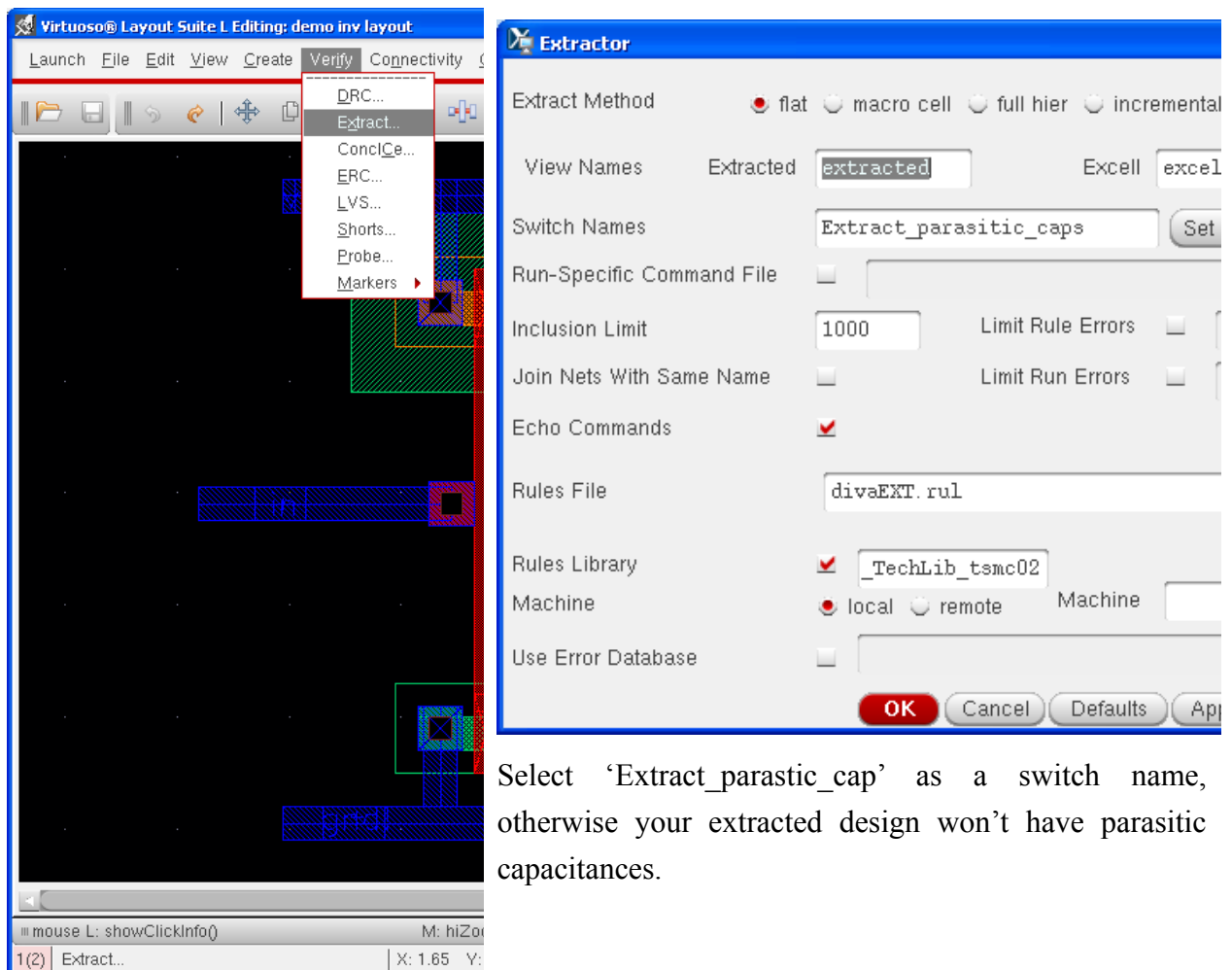
Click 'Display Terminal Option'



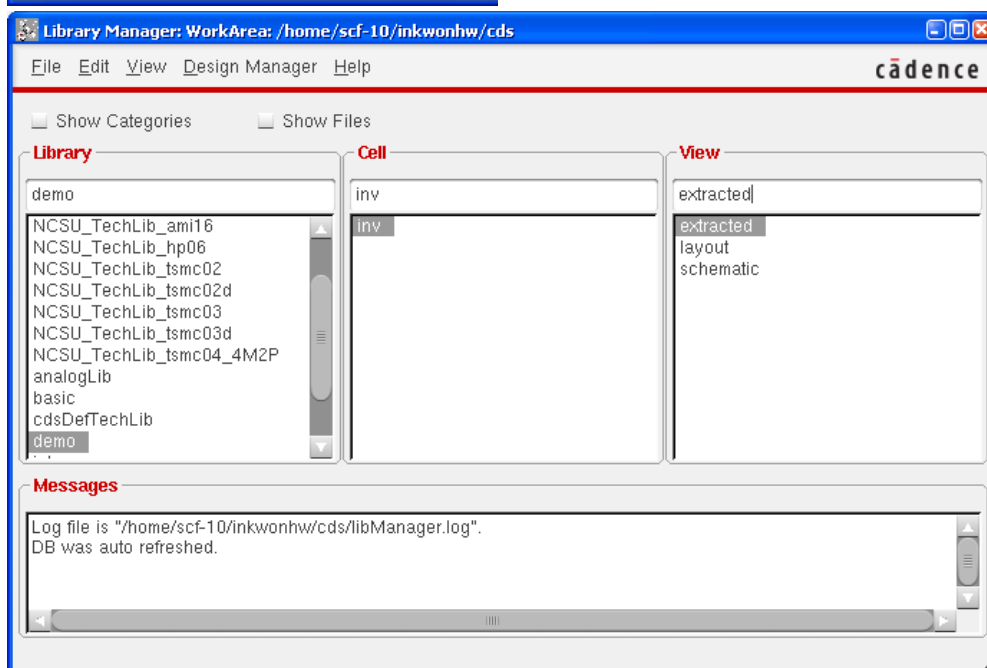


G. Extract

A layout is just a picture. If you need to run simulation using the layout, you should convert it to the other format. It is done by extracting. It's something like compiling a code.



Select 'Extract_parasitic_cap' as a switch name, otherwise your extracted design won't have parasitic capacitances.

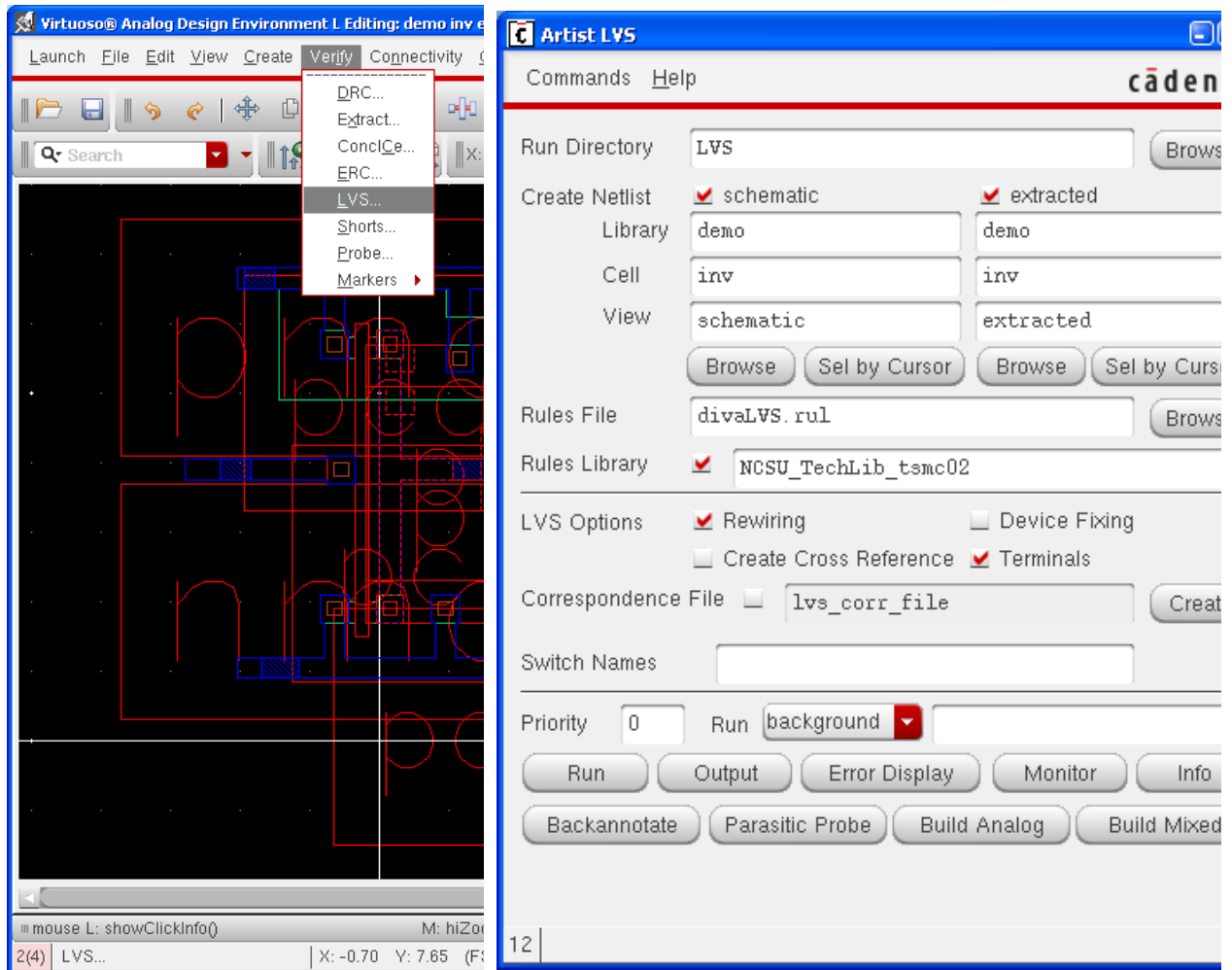


H. Run LVS

As I mentioned before, this step is very important for your grading. More complicated design, more time will be required for debugging LVS.

Verify → LVS

Keep in mind. You **SHOULD** compare your schematic with **EXTRACTED**.



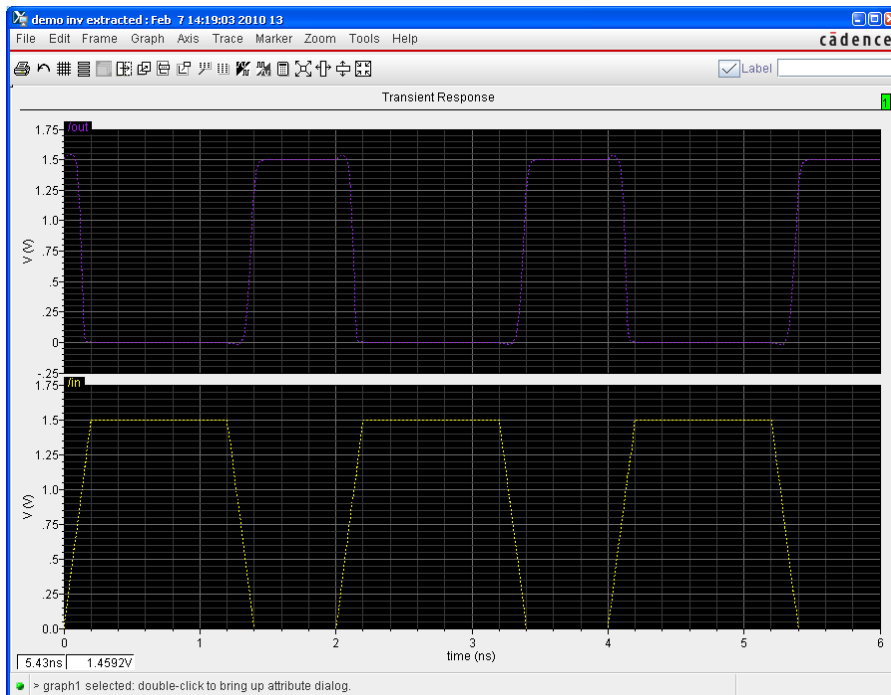
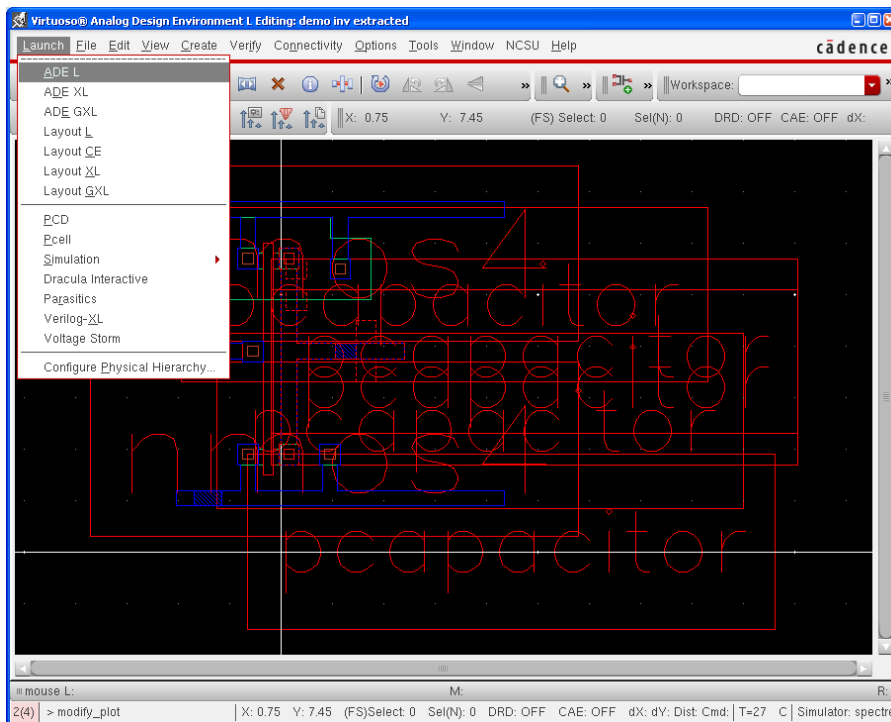
I hope all of you will see the following window.



If there are errors, you can check the results by clicking 'Output' button. 'Error Display' also might be helpful.

I. Run Spectre simulation

It is same as schematics. Go to step '4. Run Spectre simulation'.



Congratulations!!

You followed all steps I prepared. Let's do the same thing for more complicated designs.