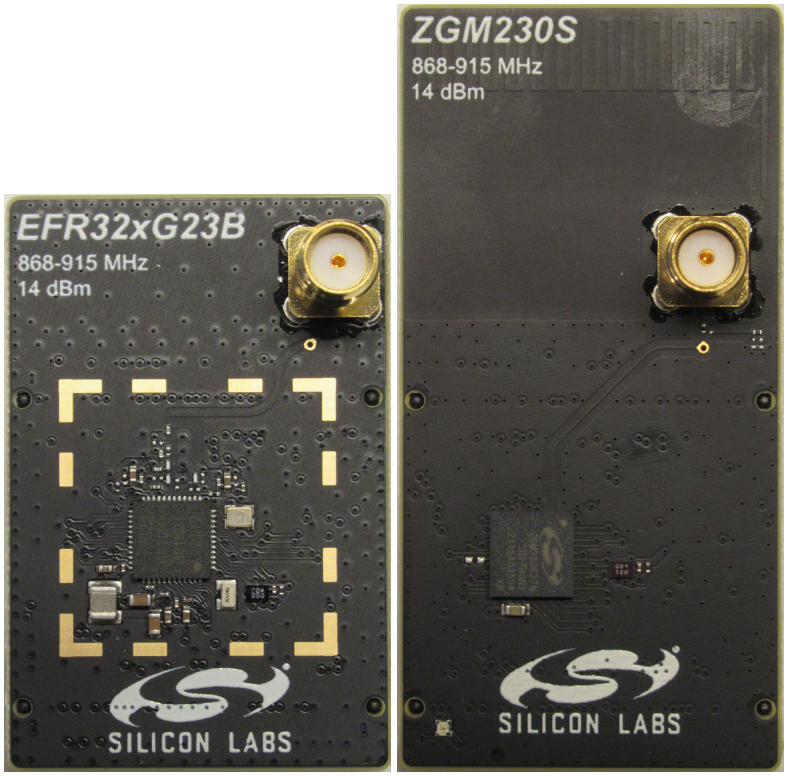
UG517: Z-Wave 800 Series Integration Guide

The purpose of this document is to provide an implementation guide for integrating Z-Wave 800 devices into product designs. It is intended for product design engineers who aim for a fast integration of Z-Wave 800 devices.

KEY FEATURES OR KEY POINTS

- Provides an overview of the Z-Wave 800 device protfolio
- Gives guidance on programming and debug interfaces, crystal calibration, and matching network



1. Overview

The Z-Wave 800 device portfolio is shown in the table below. The EFR32ZG23 SoC and ZGM230S SiP module expose the Z-Wave serial API via UART and both can be used as a gateway, controller, or end-device application. The ZGM230S SiP module combines a general-purpose SoC, crystal, supply decoupling components, and RF matching components into a single small-footprint module requiring only one or two decoupling capacitors, depending on the level of GPIO activity in the application.

Refer to [1] for an overview of supported Z-Wave regions and frequency bands supported by the Z-Wave protocol.

Table 1.1. Z-Wave 800 Device Portfolio

Type	QFN40 SoC 5x5 mm	QFN48 SoC 6x6 mm	LGA64 SiP 6.5x6.5 mm
Chip	EFR32ZG23		
Module			ZGM230S

The applicable modules are clearly stated at the beginning of each of the following sections.

2. Programming and Debugging Interface

EFR32ZG23	ZGM230S
Applicable	Applicable

A programming interface is **mandatory** if in-system programming of a Z-Wave 800 device is required, i.e., programming a new/erased chip while soldered onto the product PCB. To design in a footprint for the Mini Simplicity header, Silicon Labs recommends using a small 10-pin, 1.27 mm SMD header for both programming and debugging chips from the Silicon Labs Gecko family.

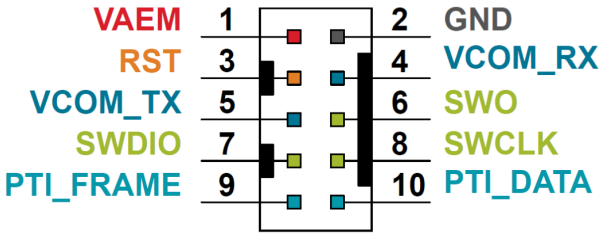


Figure 2.1. Silicon Labs Mini Simplicity Header

If a connector is used, the Samtec FTSH-105-01-F-DH surface mounted or Harwin M50-3500542 through-hole male connector is recommended and can be used directly with the BRD8010A STK/WSTK Debug Adapter. The functionality of the pins from the programmer's perspective is shown in the table below. Refer to [2] and [6] for programming instructions and more about the Mini Simplicity Header.

Table 2.1. Z-Wave 800 Mini Simplicity Header Pin Functionality

Pin Location	Pin Name	Type	Function
1	VAEM	S	Supply voltage for the circuit / Z-Wave device. If connected to a WSTK, this pin is equivalent to VAEM.
2	GND	S	Common ground between the programmer and Z-Wave 800 device
3	RST	O	Driven low by the programmer to place the Z-Wave 800 device in a reset state
4	VCOM_RX	O	Transmit UART serial data to Z-Wave 800 device
5	VCOM_TX	I	Receive UART serial data from Z-Wave 800 device
6	SWO	I	Serial Wire Output
7	SWDIO	I/O	Serial Wire Data
8	SWCLK	O	Serial Wire Clock
9	PTI_FRAME	I	Packet Trace Frame Signal
10	PTI_DATA	I	Packet Trace Data Signal

2.1 Programming Interface Overview

The table below shows which interfaces can be used to program the flash memory of the various Z-Wave 800 products:

	EFR32ZG23	ZGM230S
SWD programming	X	X
Boot Loader UART programming	X	X

Note:
- Boot Loader is not programmed into the chip at delivery.
- SWD interface will be needed for new chips and after full chip/flash erase.

3. Calibration

It is **mandatory** to calibrate the crystal in EFR32ZG23 Z-Wave 800 devices during product development to make sure that the mean value of the crystal frequency is correct. Refer to [5] for calibration instructions. Furthermore, for best possible performance, Silicon Labs recommends that calibration be performed during production to minimize the spread in crystal frequency. All ZGM230S Z-Wave 800 devices are calibrated during production and therefore do not need any further crystal calibration.

3.1 Crystal

EFR32ZG23	ZGM230S
Applicable	N/A

It is mandatory to calibrate the crystal frequency for the EFR32ZG23 devices to ensure minimum error of the radio carrier frequency.

4. RF Verification Tool

EFR32ZG23	ZGM230S
Applicable	Applicable

The RailTest tool can be used to verify the RF performance of a device without the overhead of the Z-Wave protocol. The RailTest tool supports both ZGM230S and EFR32ZG23 devices. The same RF PHY present in the Z-Wave protocol is used. The tool is suitable when investigating RF performance and performing RF regulatory tests. To use the tool, the chip must be programmable and the UART0 interface must be connected to a terminal over RS-232 or through the WSTK. For a comprehensive user's manual for the RailTest tool, refer to [3] and [4].

As the RF PHY can be updated for new software releases, it is important to compile a RailTest version based on the same software release that will be used in the final product.

5. Component Specifications

5.1 Saw Filter

EFR32ZG23	ZGM230S
Applicable	Applicable

Silicon Labs recommends using a SAW filter in Z-Wave 800 gateway designs also containing GSM or LTE transceivers operating in the sub-GHz band. A SAW filter attenuates unwanted radio emissions and improves the receiver blocking performance. Three regions are defined to cover the global Z-Wave frequency range. The SAW filter specifications described in Table 5.1 Region E on page 7, Table 5.2 Region U on page 8, and Table 5.3 Region H on page 8 are recommended for new designs. An overview of supported Z-Wave regions and frequencies can be found in [1].

Find a guideline on when to use a SAW filter in [13].

Table 5.1. Region E

	Frequency Range	Unit	Minimum	Typical	Maximum
Operating temperature	—	°C	-30	—	+85
Insertion loss	865.0 to 870.1 MHz	dB	—	—	3.5
Amplitude ripple	865.0 to 870.1 MHz	dB	—	—	2.0
Relative attenuation	0.1 to 800.0 MHz	dB	40	—	—
	805 to 830 MHz	dB	35	—	—
	835 to 855 MHz	dB	—	—	—
	860 to 862 MHz	dB	—	—	—
	890 to 1000 MHz	dB	40	—	—
	1005 to 2000 MHz	dB	30	—	—
	2005 to 3000 MHz	dB	30	—	—
	3005 to 4000 MHz	dB	30	—	—
	4005 to 6000 MHz	dB	—	—	—
In / out impedance	—	Ω	—	50	—

Table 5.2. Region U

	Frequency Range	Unit	Minimum	Typical	Maximum
Operating temperature	—	°C	-30	—	+85
Insertion loss	908.2 to 916.3 MHz	dB	—	—	2.5
Amplitude ripple	908.2 to 916.3 MHz	dB	—	—	1.5
Relative attenuation	720 to 800 MHz	dB	45	—	—
	805 to 840 MHz	dB	—	—	—
	845 to 870 MHz	dB	40	—	—
	870 to 895 MHz	dB	—	—	—
	940 to 1000 MHz	dB	9	—	—
	1005 to 2000 MHz	dB	9	—	—
	2005 to 3000 MHz	dB	17	—	—
	3005 to 4000 MHz	dB	—	—	—
	4005 to 6000 MHz	dB	—	—	—
In / out impedance	—	Ω	—	50	—

Table 5.3. Region H

	Frequency Range	Unit	Minimum	Typical	Maximum
Operating temperature	—	°C	-30	—	+85
Insertion loss	919.5 to 926.5 MHz	dB	—	—	3.2
Amplitude ripple	919.5 to 926.5 MHz	dB	—	—	1.0
Relative attenuation	40 to 870 MHz	dB	40	—	—
	875 to 885 MHz	dB	35	—	—
	890 to 905 MHz	dB	20	—	—
	945 to 955 MHz	dB	20	—	—
	960 to 1000 MHz	dB	20	—	—
	1005 to 1500 MHz	dB	40	—	—
	1505 to 3000 MHz	dB	20	—	—
	3005 to 4000 MHz	dB	—	—	—
	4005 to 6000 MHz	dB	—	—	—
In / out impedance	—	Ω	—	50	—

5.1.1 Recommended Components for GSM/LTE Gateways

Table 5.4. SAW Filters

Region	Distributor	Component Number	Note
E	ACTE A/S, www.acte.dk, salessupport@acte.dk	SF4000-868-07-SX	Preferred
U	ACTE A/S, www.acte.dk, salessupport@acte.dk	SF4000-914-06-SX	Preferred
H	ACTE A/S, www.acte.dk, salessupport@acte.dk	SF1256-923-02	Preferred

5.1.2 Optional Components for GSM/LTE Gateways

Table 5.5. LTE Improved SAW Filters

Region	Distributor	Component Number	Note
E	ACTE A/S, www.acte.dk, salessupport@acte.dk	SF4000-869-14-SX	Improved LTE rejection

5.2 Crystal

EFR32ZG23	ZGM230S
Applicable	N/A

The crystal is part of the oscillator that generates the reference frequency for the digital system clock and RF carrier. It is a critical component of a Z-Wave 800 device. Further, it is **mandatory** to calibrate the crystal for EFR32ZG23-based designs. Refer to section 3. Calibration for more information.

The EFR32ZG23 has internal crystal capacitors and does not need any external circuitry apart from the crystal itself.

The ZGM230S has an integrated crystal and is calibrated at the time of production.

For more information about the crystal oscillator, crystals, and the EFR32ZG23 device, refer to [7].

Table 5.6. Crystal Specification for Z-Wave 800 Devices

Parameter	Symbol	Min	Typ	Max	Unit
Crystal frequency	fHFXO	—	39	—	MHz
Supported crystal equivalent series resistance (ESR)	ESRHFXO_39M	—	40	60	Ω
Supported range of crystal load capacitance	CHFXO_CL	—	10	—	pF
Combined tolerance for the crystal	FTtotalHFXO	-27	—	27	ppm/5yr

5.2.1 Recommended Components

Table 5.7. Recommended 39 MHz Crystals

Manufacturer	Component Number	ESR (Ω)	C0 (max) (pF)	Temp (°C)	Temp Tolerance (ppm)	Mfg Tolerance (ppm)	Aging	CL (pF)	Footprint (mm)
Tai-Saw	TZ3541C	35	2	0 to +50	±16	±8	±3	10	2.0 x 1.6
Tai-Saw	TZ3541B	35	1	-40 to +105	±16	±7	±2	10	2.0 x 1.6
Siward	XTL501170-S315-031	35	3	-40 to +105	±17	±6	±2	10	2.0 x 1.6
Siward	XTL501350-S315-027	40	3	-40 to +85	±15	±8	±3	10	2.0 x 1.6
TXC	8Y39072002	35	1	-40 to +95	±13	±7	±2	10	2.0 x 1.6
TXC	8Y39072004	35	2	-40 to +105	±16	±7	±2	10	2.0 x 1.6

6. Supply Filter

A good power supply filter is strongly recommended as part of the schematic. A filter with a ferrite and a capacitor can be used as shown in the figure below. The ferrite suppresses high frequency noise, while the capacitors decouple the power supply by acting as a source for fast transient currents.

For Z-Wave 800 devices, the filter shown in the figure below is **strongly recommended**. For normal scenarios, this will provide adequate filtering with a low BOM cost. In case of excessive supply noise, the 0 Ω resistor can be swapped for a ferrite bead to improve filtering.

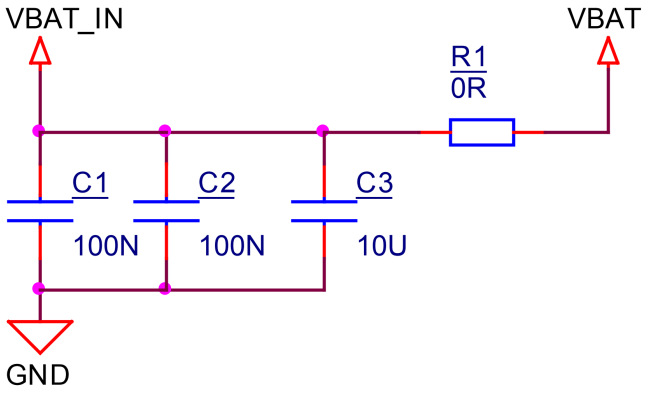


Figure 6.1. Recommended Supply Filter for Z-Wave 800 Devices

For more information about supply decoupling, refer to section 8.4 Decoupling. Refer to [8] and [9] for more in-depth information about decoupling strategies and the power supply systems of Z-Wave devices.

7. Matching Circuit

The PA of the transmitter should be matched for maximum power transfer and the LNA of the receiver must be matched for best sensitivity. The matching is divided into the following operations:

1. Matching the SoC transceiver to a 50 Ω RF line on the PCB.
2. Matching the 50 Ω RF line of the PCB to the antenna.

The first part is already done in the ZGM230S SiP and is therefore only applicable to the EFR32ZG23. The second part must be done for all implementations unless a naturally matched antenna is used.

7.1 Summary of Matching Networks

The recommended matching networks for general Z-Wave and Z-Wave long range is shown in the table below:

Table 7.1. Z-Wave Recommended Matches

	General Z-Wave		Z-Wave Long Range		
	EFR32ZG23	ZGM230S	EFR32ZG23		ZGM230S
	14 dBm	14 dBm	14 dBm	20 dBm	14 dBm
Matching w/o SAW	• TX match: 4-element discrete match + dc-blocking cap • RX match: 1 series inductor (BRD4204D)	No external match needed (BRD4205B)	• TX match: 4-element discrete match + dc-blocking cap • RX match: 1 series inductor (BRD4204D)	• TX match: 6-element discrete match + dc-blocking cap • RX match: 1 series inductor (BRD4210A)	No external match needed (BRD4205B)
Matching w/SAW	• TX match: 4-element discrete match + dc-blocking cap • RX match: 1 series inductor + SAW in TX/RX path	SAW in TX/RX path	• TX match: 4-element discrete match + dc-blocking cap • RX match: 1 series inductor + SAW in TX/RX path	• TX match: 6-element discrete match + dc-blocking cap • RX match: 1 series inductor + SAW in TX/RX path	SAW in TX/RX path
Max. power for US	-1 dBm	-1 dBm	14 dBm	20 dBm	14 dBm
Max. power for EU	14 dBm	14 dBm	N/A	N/A	N/A

The matching network solutions listed above are detailed in section 7.2 SoC to RF Line Matching.

7.2 SoC to RF Line Matching

EFR32ZG23	ZGM230S
Applicable	N/A

The EFR32ZG23 antenna interface consists of two single-ended input pins (SUBG_I0 and SUBG_I1) that interface directly to two LNAs and two single-ended output pins that interface directly to two +14 dBm or +20 dBm PAs (SUBG_O0 and SUBG_O1). Integrated switches select either SUBG_O0 or SUBG_O1, SUBG_I0, or SUBG_I1 to be the active paths.

Note: The Z-Wave gateway or end-device FW for EFR32ZG23 delivered as part of the Z-Wave SDK enables RF interface 0 only. Therefore, only SUBG_O0 and SUBG_I0 can be used as active ports on EFR32ZG23 when using the Z-Wave gateway or end-device FW.

EFR32ZG23 parts are available either with the +14 dBm (LPA) or +20 dBm (HPA) Class-D PAs. These are internally bonded options, so different OPN part numbers are used for the chip variants with different maximum TX power levels.

The typical RF impedance matching network topology for EFR32ZG23 is shown in the figure below, where all components do not need to be populated but different BOM options are required for different output power level requirements (14 or 20 dBm). Series dc-blocking capacitor of C5 in the TX path is required, while dc decoupling in the RX path is not needed. The unused RF ports should be left floating, i.e., terminated with an open load.

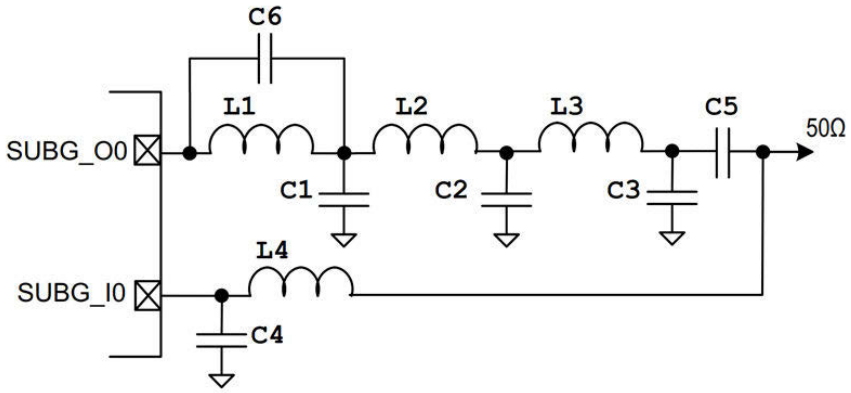


Figure 7.1. RF Matching Circuit for EFR32ZG23

The TX matching network includes the low-pass filtering function as well to suppress the TX harmonics, while the RX matching network provides the highest possible voltage gain to the LNA by transforming the impedance up while the LNA capacitance is resonated out.

Table 7.2. Summary of Matching Component Values vs. Output Power

P_OUT	PAVDD	L1	L2	L3	L4	C1	C2	C3	C4	C5	C6
14 dBm	1.8 V	4.2 nH	16 nH	0R	18 nH	5.9 pF	2.1 pF	N.M.	N.M.	220 pF	N.M.
20 dBm	3.3 V	1.5 nH	1.3 nH	13 nH	18 nH	N.M.	7.2 pF	1.3 pF	N.M.	220 pF	1.9 pF

7.3 RF Line to Antenna Matching

EFR32ZG23	ZGM230S
Applicable	Applicable

Finding appropriate values for the components should be considered an iterative task. Silicon Labs recommends adding a pi network for matching as shown in the figure below. The following matching strategy is proposed:

1. Calibrate your Vector Network Analyzer (VNA) for a frequency range larger than the intended bandwidth of the antenna.
2. Connect an RF coaxial cable to the RF line (for instance, by soldering a pigtail to the line). Connect the RF coaxial cable to a VNA to measure the reflection coefficient, S11, looking into the antenna through the matching network.
   a. Be sure to have a good connection to the ground plane to get the best electrical performance and the highest mechanical robustness during the measurement.
   b. Make sure to route the pigtail towards the center of the PCB and then perpendicularly away from the PCB at the center point. This will limit the effect of the cable on the measured data as much as possible.
3. Start out with no components on the antenna network shown in the figure below:
   a. The shunt components are not mounted.
   b. The series component is not mounted.
4. Use line extension on the VNA to move the reference point to the footprint of R1 and R2.
   a. This is achieved when the locus of the S-parameters in the Smith chart on the VNA have assembled in a point at the right edge of the Smith chart.
5. Mount a 0 Ω resistor at R2 in the figure below.
6. Measure reflection coefficient for the frequency of interest (the frequency halfway between the lowest frequency and the highest frequency of the region of interest).
7. Use an online matching tool to calculate series and shunt component values to achieve 50 Ω match on the coaxial line.
   a. This will give a good starting point and should result in a reasonably good match at first attempt.
8. Iteratively change component values until match is acceptable.
   a. The standard matching criterion is either -6 dB or -10 dB reflection across all frequencies of interest.
   b. When this goal is achieved, Silicon Labs recommends using the same values on a small sample of boards to make sure that the matching is acceptable across production tolerances.

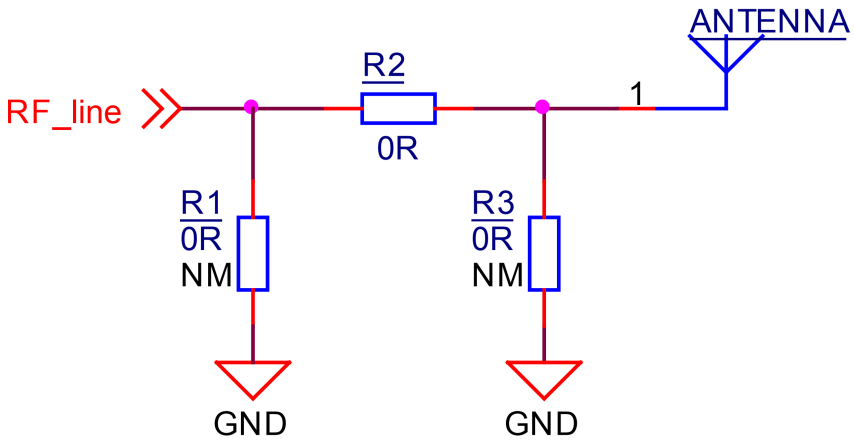


Figure 7.2. Recommended Antenna Matching Pi Network

7.4 Measurement Setup

The output power should be measured with a spectrum analyzer as shown in the figure below and sensitivity as shown in Figure 7.4 Measuring Receiver Sensitivity on page 15. In both cases, place the fixed attenuator as close as possible to the transmitter. The fixed attenuator prevents RF reflections in the measurement setup.

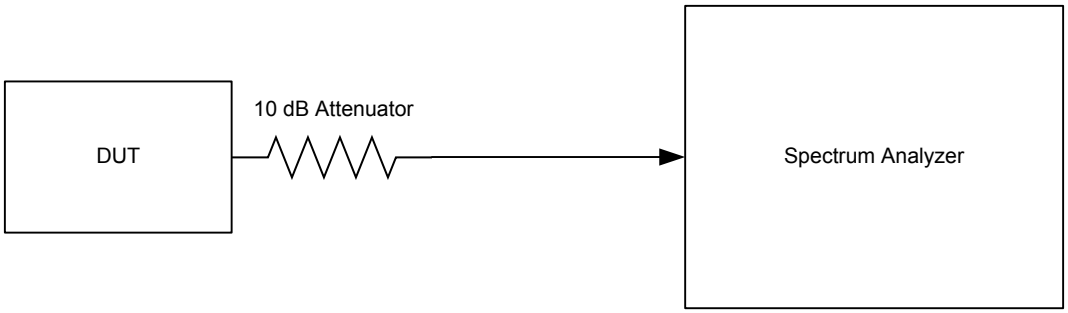


Figure 7.3. Measuring Transmitter Output Power

When measuring the sensitivity, first measure and record the output power of the Z-Wave frame generator using the spectrum analyzer. A Z-Wave 800 module programmed with the RailTest tool can be used as the Z-Wave frame generator. Then, a fixed attenuator can be used along with a variable attenuator to adjust the input power of the DUT. For example, by setting the output power of the Z-Wave generator to -20 dBm, a fixed 50 dB attenuator and a variable 50 dB attenuator can be used to measure the sensitivity with a 1 dB resolution. Place the fixed attenuator close to the Z-Wave generator and conduct the measurements in a radio silent environment, e.g., by placing the DUT in an RF shielded box.

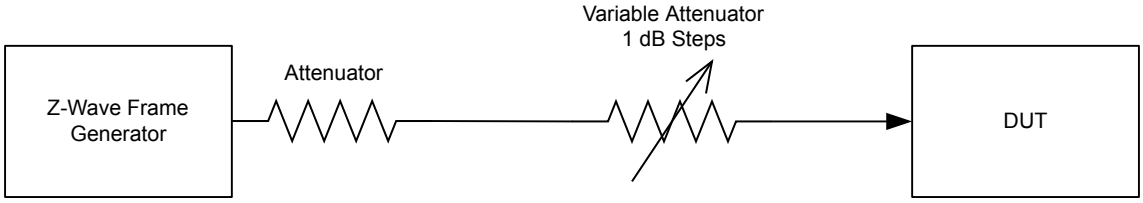


Figure 7.4. Measuring Receiver Sensitivity

8. PCB Implementation

EFR32ZG23	ZGM230S
Applicable	Applicable except section 8.6 IC Grounding

A good PCB implementation is required to obtain the best performance from a Z-Wave 800 device. The following subsections describe items that should be considered when designing the PCB layout.

Besides the descriptions below, use the reference designs for the ZGM230S and the EFR32ZG23 devices as guidelines. The reference design for the ZGM230S is BRD4205B. The reference designs for the EFR32ZG23 are BRD4204D and BRD4210A.

Further layout guidelines can be found in [12].

8.1 Placement

In general, it is **mandatory** that all decoupling and matching components are placed as close as possible to the Z-Wave 800 device, and on the same layer to reduce trace parasitics. For gateway devices with GSM or LTE transceivers, Silicon Labs also **strongly recommends** placing the SAW filter as close as possible to the EFR32ZG23 matching network or to the ZGM230S RF pin.

When implementing a Z-Wave system into a product, it is **strongly recommended** that the Z-Wave 800 device is placed close to a corner of the product's PCB, away from any high frequency switching circuits used elsewhere in the product, e.g. host CPU systems, switching dc supplies, motor-controllers, etc.

8.2 Stack-up

If designing a product with the EFR32ZG23, Silicon Labs recommends using a 4-layer stack-up PCB as shown in the figure below. Choose the thickness of the PCB stack-up that best optimizes cost. The distance between L1 and L2 layers should be as close to 300 µm as possible. We **strongly recommended** using a solid copper plane as the ground plane layer L2.

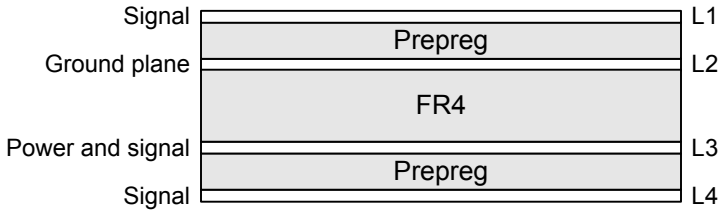


Figure 8.1. 4-layer Stack-up

With the ZGM230S, the complex circuitry is contained inside the SiP. Therefore, there are good possibilities for making a cheap, two-layer PCB design with ZGM230S. This does require extra care in designing the RF routing, power supply, and ground layout as no full-layer power and ground planes can be included.

Refer to the BRD4204D, BRD4205B, and BRD4210A designs for more information.

8.3 Power Routing

Use as short VDD traces as possible. The VDD trace can be a hidden, unwanted radiator so it is important to simplify the VDD routing as much as possible and use large, continuous GND pours with many stitching vias. To achieve the simplified VDD routing, try to avoid star topology of VDD traces (i.e., avoid connecting all VDD traces in one common point).

Consider using the reference designs BRD4204D, BRD4205B, and BRD4210A as the reference designs when creating the power routing.

8.4 Decoupling

Power should be driven through decoupling capacitors to prevent parasitic inductances as shown in Figure 8.3 Grounded Components on page 17. At least two grounding vias is recommended for each component as shown in Figure 8.4 Pin Decoupling on page 17.

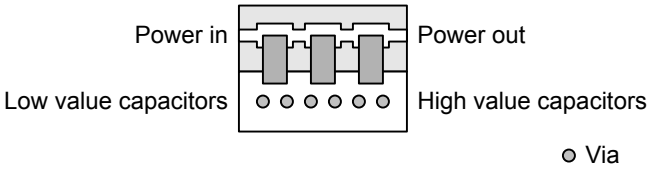


Figure 8.3. Grounded Components

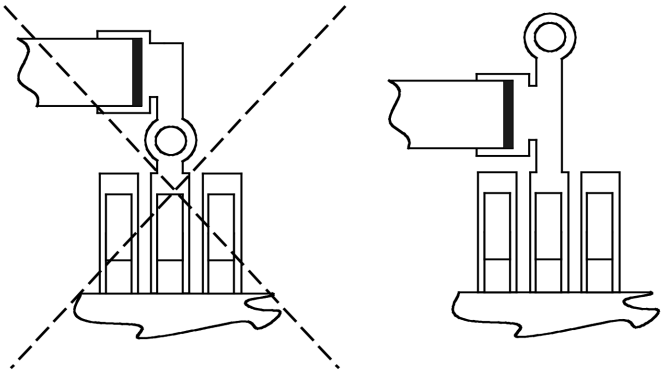


Figure 8.4. Pin Decoupling

8.4.1 ZGM230S SiP Module

For the ZGM230S, most of the decoupling is built in. This includes all supply decoupling except for one 10 µF capacitor on VREGVDD and IOVDD combined. If high switching activity is expected on the GPIO interface, Silicon Labs recommends 10 µF on each of the supply lines (VREGVDD, IOVDD).

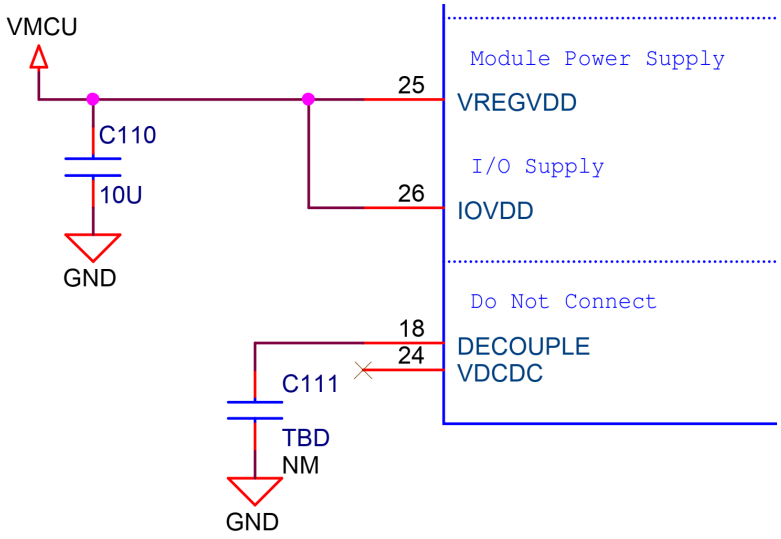


Figure 8.4. Recommended External Supply Decoupling for the ZGM230S

8.4.2 EFR32ZG23 SoC

For an EFR32ZG23 device, Silicon Labs **strongly recommends** the decoupling topology shown in the figure below.

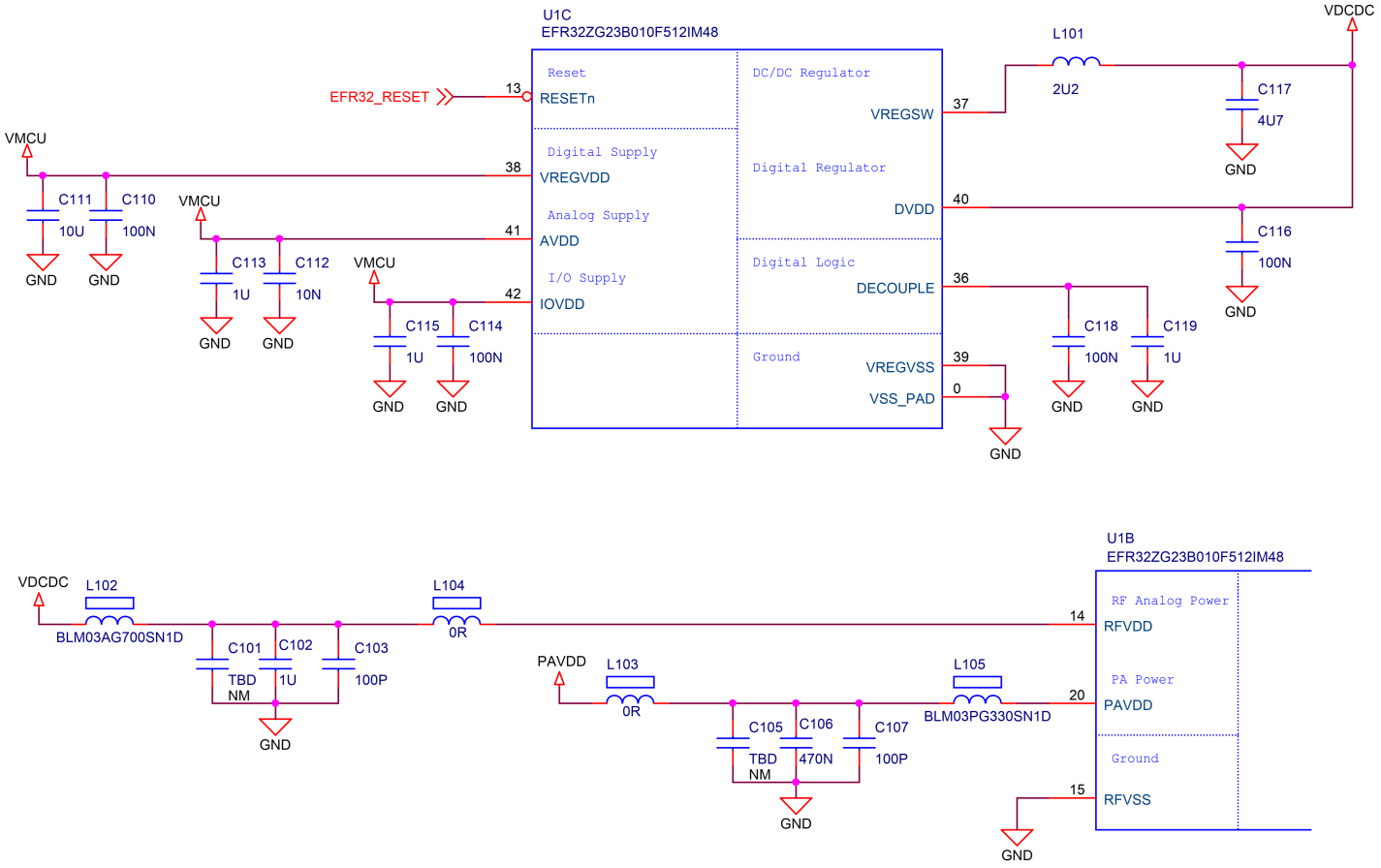


Figure 8.5. Minimum Supply Decoupling Required for the EFR32ZG23 SoC

8.5 RF Trace

For RF traces longer than λ/16 at the fundamental frequency, it is **mandatory** to design the trace as a transmission line with a 50 Ω characteristic impedance. A coplanar waveguide similar to the figure below is recommended for a transmission line on signal layer L1.

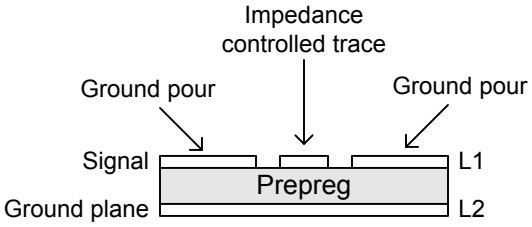


Figure 8.6. Coplanar Waveguide

A via fence is recommended on both sides of a coplanar waveguide, as shown in the following figure, to short any return currents induced on the top layer to ground.

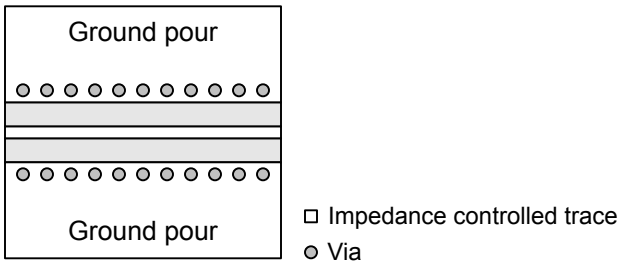


Figure 8.7. Via Fence

A free tool, such as Saturn PCB Design Toolkit (http://www.saturnpcb.com/pcb_toolkit.htm), can be used to calculate the dimensions of the traces conveniently.

8.6 IC Grounding

QFN chips should be provided with a ground paddle with stitched-vias to minimize parasitic inductance and to provide a good thermal heat sink as shown in the following figure.

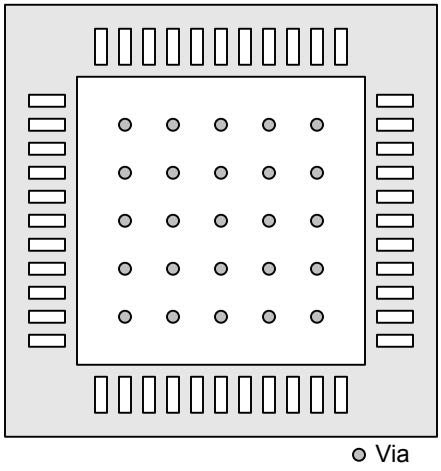


Figure 8.8. IC Ground Paddle

Refer to the BRD4204D or BRD4210A layout to see a practical implementation of a QFN footprint with exposed pad.

9. Antenna Design

EFR32ZG23	ZGM230S
Applicable	Applicable

Because antenna design is very product dependent, it is **mandatory** to perform the antenna matching as described in section 7.3 RF Line to Antenna Matching. Each product requires an individual antenna design for best power transfer and radiation characteristics.

10. ESD

EFR32ZG23	ZGM230S
Applicable	Applicable

Because ESD can damage the Z-Wave 800 product, great care must be taken during manufacturing and assembly of final goods to avoid ESD.

By design, all EFR32ZG23 and ZGM230S pins are ESD protected up to a level of **2.5 kV HBM**.

The ESD level of a SAW filter is typically **<< 2 kV HBM**.

11. Abbreviations

Abbreviation	Description
2FSK	2-key Frequency Shift Keying
2GFSK	2-key Gaussian Frequency Shift Keying
ACM	Abstract Control Model
ACMA	Australian Communications and Media Authority
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
API	Application Programming Interface
APM	Auto Programming Mode
AV	Audio Video
BALUN	Balanced to Unbalanced converter
BOD	Brown-Out Detector
CBC	Cipher-Block Chaining
CDC	Communications Device Class
CE	Conformité Européenne
COM	Communication
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
D	Differential
D-	Differential Minus
D+	Differential Plus
DAC	Digital-to-Analog Converter
dc	Direct Current
DMA	Direct Memory Access
DUT	Device Under Test
ECB	Electronic CodeBook
EMS	Electronic Manufacturing Services
EOL	End Of Life
ESD	Electro Static Discharge
ESR	Equivalent Series Resistance
FCC	Federal Communications Commission
FET	Field Effect Transistor
FER	Frame Error Rate
FLiRS	Frequently Listening Routing Secondary
FR4	Flame Retardant 4
FSK	Frequency Shift Keying
GFSK	Gaussian Frequency Shift Keying

Abbreviation	Description
GP	General Purpose
GPIO	General Purpose Input Output
HBM	Human Body Model
I	Input
I/O	Input / Output
IC	Integrated Circuit
IDC	Insulation-Displacement Connector
IF	Intermediate Frequency
IGBT	Insulated-Gate Bipolar Transistor
INT	Interrupt
IPC	Interconnecting and Packaging Circuits
IPD	Integrated Passive Device
IR	Infrared
IRAM	Indirectly Addressable Random Access Memory
ISM	Industrial, Scientific, and Medical
ISP	In-System Programming
ITU	International Telecommunications Union
JEDEC	Joint Electron Device Engineering Council
LED	Light-Emitting Diode
LNA	Low-Noise Amplifier
LO	Local Oscillator
lsb	Least Significant Bit
LSB	Least Significant Byte
MCU	Microcontroller Unit
MIC	Ministry of Internal affairs and Communications, Japan
MISO	Main In, Secondary Out
MOSI	Main Out, Secondary In
msb	Most Significant Bit
MSB	Most Significant Byte
NA	Not Applicable
NMI	Non-Maskable Interrupt
NRZ	Non-Return-to-Zero
NVM	Non-Volatile Memory
NVR	Non-Volatile Registers
O	Output
OEM	Original Equipment Manufacturer
OFB	Output FeedBack

Abbreviation	Description
OTP	One-Time Programmable
PA	Power Amplifier
Pb	Lead
PCB	Printed Circuit Board
PHY	L1 Physical Layer
POR	Power-On Reset
PWM	Pulse Width Modulator
QFN	Quad-Flat No-leads
RAM	Random Access Memory
RF	Radio Frequency
RoHS	Restriction of Hazardous Substances
ROM	Read Only Memory
RS-232	Recommended Standard 232
RX	Receive
S	Supply
SAW	Surface Acoustic Wave
SCK	Serial Clock
SFR	Special Function Register
SiP	System-in-Package
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
T0	Timer 0
T1	Timer 1
TX	Transmit
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus
VNA	Vector Network Analyzer
WUT	Wake-Up Timer
XRAM	External Random Access Memory
XTAL	Crystal
ZEROX	Zero Crossing

12. References

1. https://www.silabs.com/wireless/z-wave/global-regions
2. Silicon Labs, “AN136: Silicon Labs Production Programming Options”
3. Silicon Labs, “UG523: Bring-Up/Test HW Development User's Guide ”
4. Silicon Labs, “UG409: RAILtest User's Guide”
5. Silicon Labs, “UG522: Mandatory Crystal Adjustment for EFR32ZG14/EFR32ZG23 Based Products User's Guide”
6. Silicon Labs, “AN958: Debugging and Programming Interfaces for Custom Designs”
7. Silicon Labs, “AN0016.2: Oscillator Design Considerations”
8. Silicon Labs, “AN0948.2: EFM32 and EFR32 Series 2 DC-to-DC Converter”
9. Silicon Labs, “AN0002.2: EFM32 and EFR32 Wireless Gecko Series 2 Hardware Design Considerations”
10. Silicon Labs, “AN923.2: EFR32 Series 2 sub-GHz Matching Guide”
11. Silicon Labs, “APL10045: Antennas for Short Range Devices”
12. Silicon Labs, “AN928.2: EFR32 Series 2 Layout Design Guide”
13. Silicon Labs, “Z-Wave 700/800: SAW filter recommendations”

13. Revision History

Revision 1.00

December, 2021

- Initial draft based on INS14487: "Z-Wave 700 Series Integration Guide”.

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