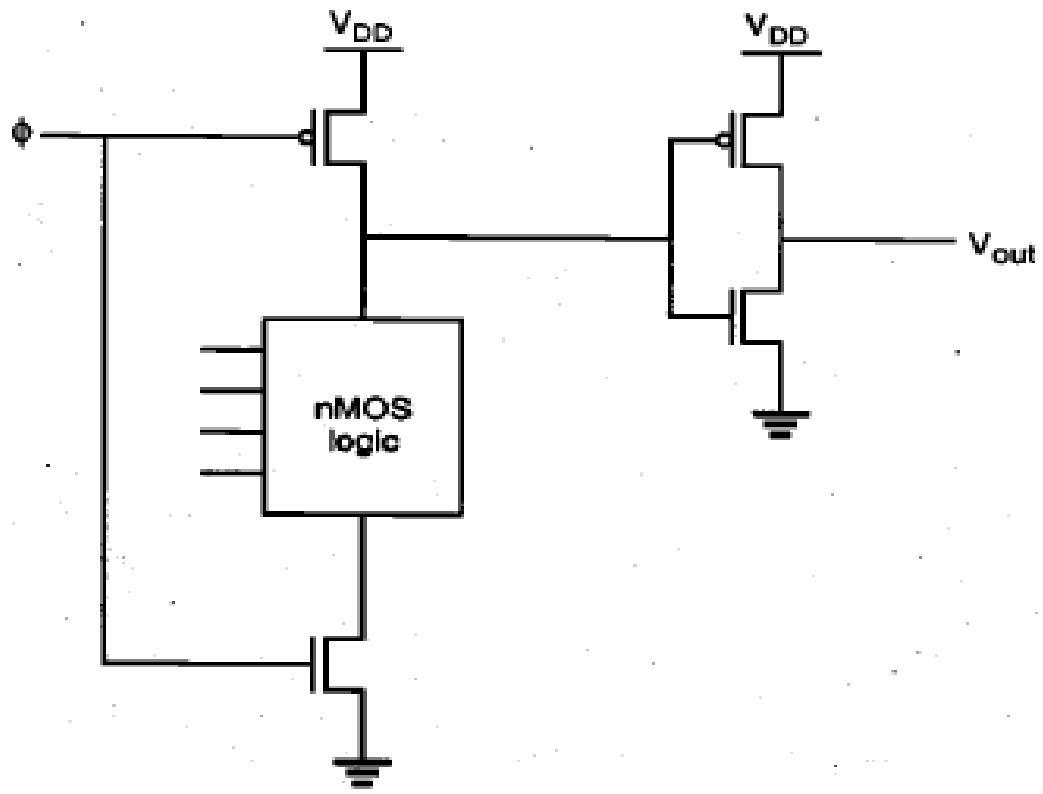
UNIT 4:
Dynamic logic circuits

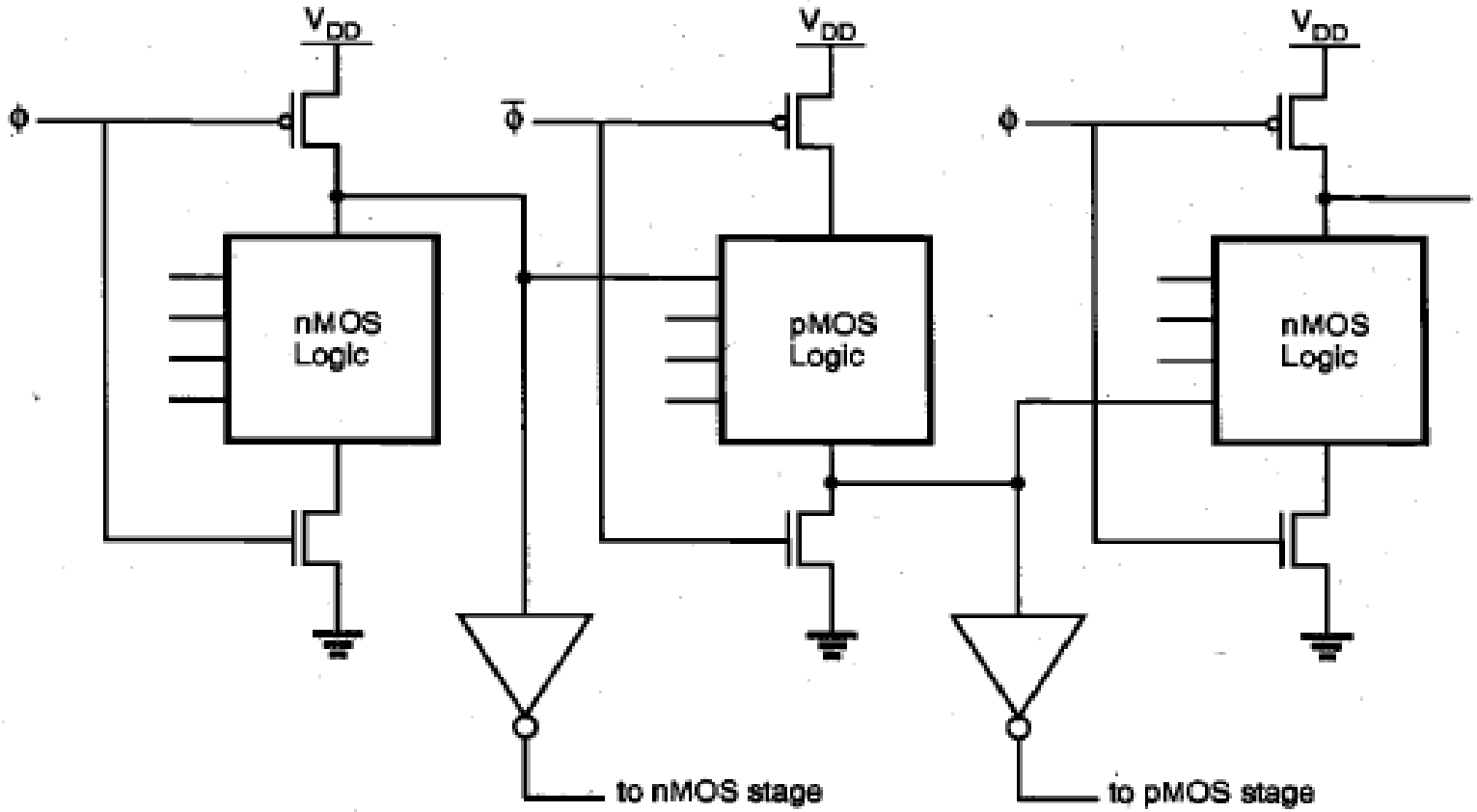
Dynamic CMOS Circuits

- The circuits presented here are variants of the basic dynamic CMOS logic gate structure.
- We will see that they are designed to take full advantage of the obvious benefits of dynamic operation and at the same time, to allow unrestricted cascading of multiple stages.
- The ultimate goal is to achieve reliable, high-speed, compact circuits using the least complicated clocking scheme possible.

Domino CMOS Logic



NORA CMOS Logic (NP-Domino Logic)



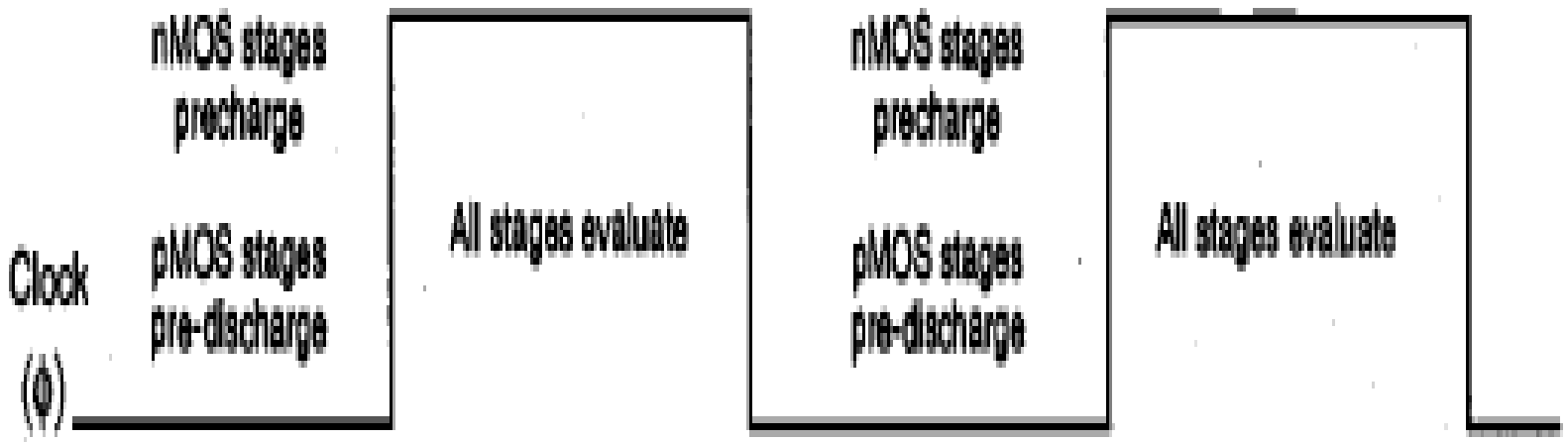
- Note that the precharge-and-evaluate timing of nMOS logic stages is accomplished

  by the clock signal Φ, whereas the pMOS logic stages are controlled by the inverted clock signal, ΦT.

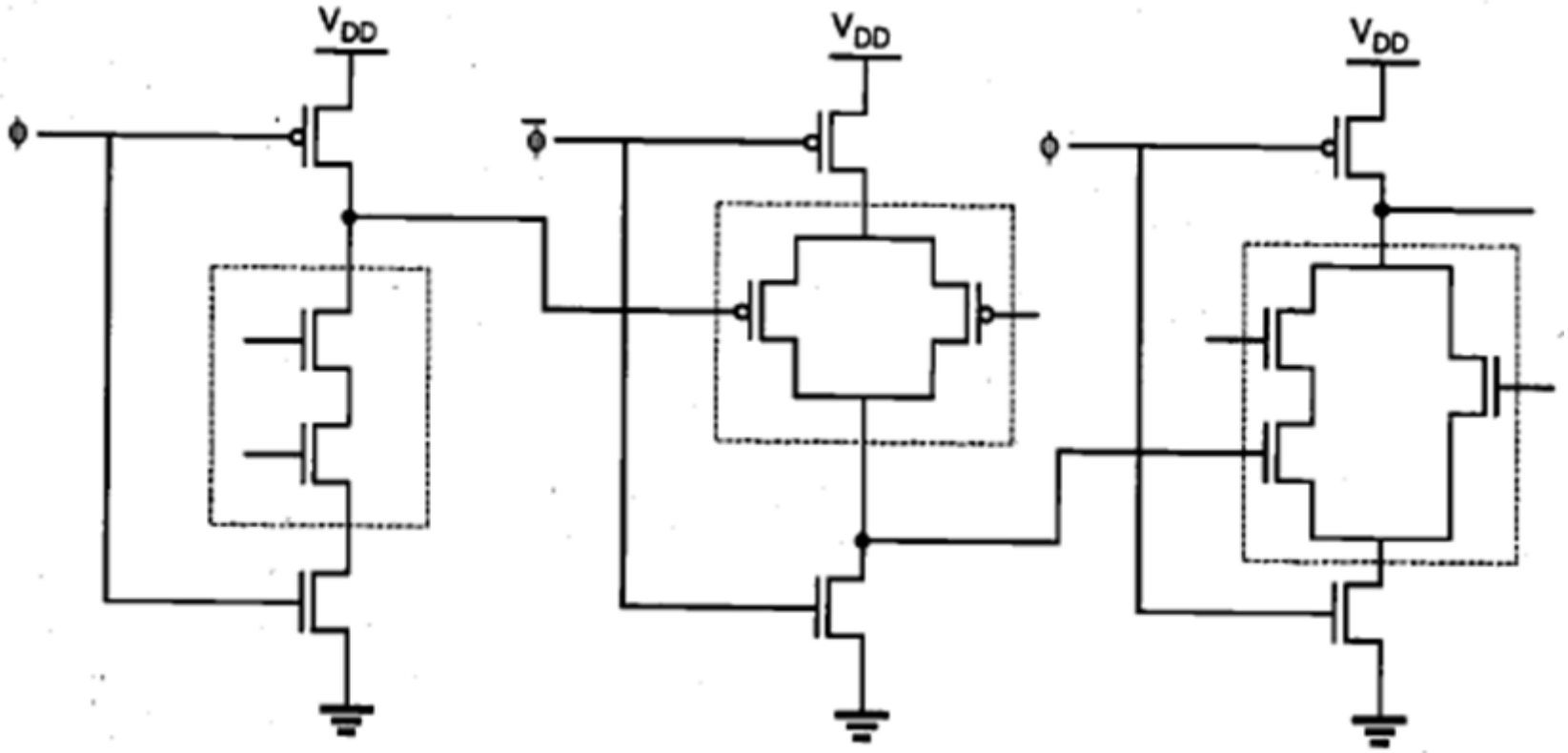
The operation of the NORA CMOS circuit is as follows:

- When the clock signal is low, the output nodes of nMOS logic blocks are precharged to *VDD through the pMOS* precharge transistors, whereas the output nodes of pMOS logic blocks are pre-discharged to 0 V through the nMOS discharge transistors, driven by Φbar .

- When the clock signal makes a low-to-high transition (note that the inverted clock signal Φbar makes a high-to-low transition simultaneously), all cascaded nMOS and pMOS logic stages evaluate one after the other, much like the domino CMOS examined earlier


nMOS stages
precharge
pMOS stages
pre-discharge
All stages evaluate
nMOS stages
precharge
pMOS stages
pre-discharge
All stages evaluate
Clock
(φ)

NORA CMOS logic circuit example.



Zipper CMOS Circuits

- The basic circuit architecture of Zipper CMOS is essentially identical to NORA CMOS, with the exception of the clock signals.

- The Zipper CMOS clock scheme requires the generation of slightly different clock signals for the precharge (discharge) transistors and for the pull-down (pull-up) transistors.

- In particular, the clock signals which drive the pMOS precharge and nMOS discharge transistors allow these transistors to remain in weak conduction or near cut-off during the evaluation phase, thus compensating for the charge leakage and charge-sharing problems.

- The generalized circuit diagram and the clock signals of the Zipper CMOS architecture are shown in Fig.

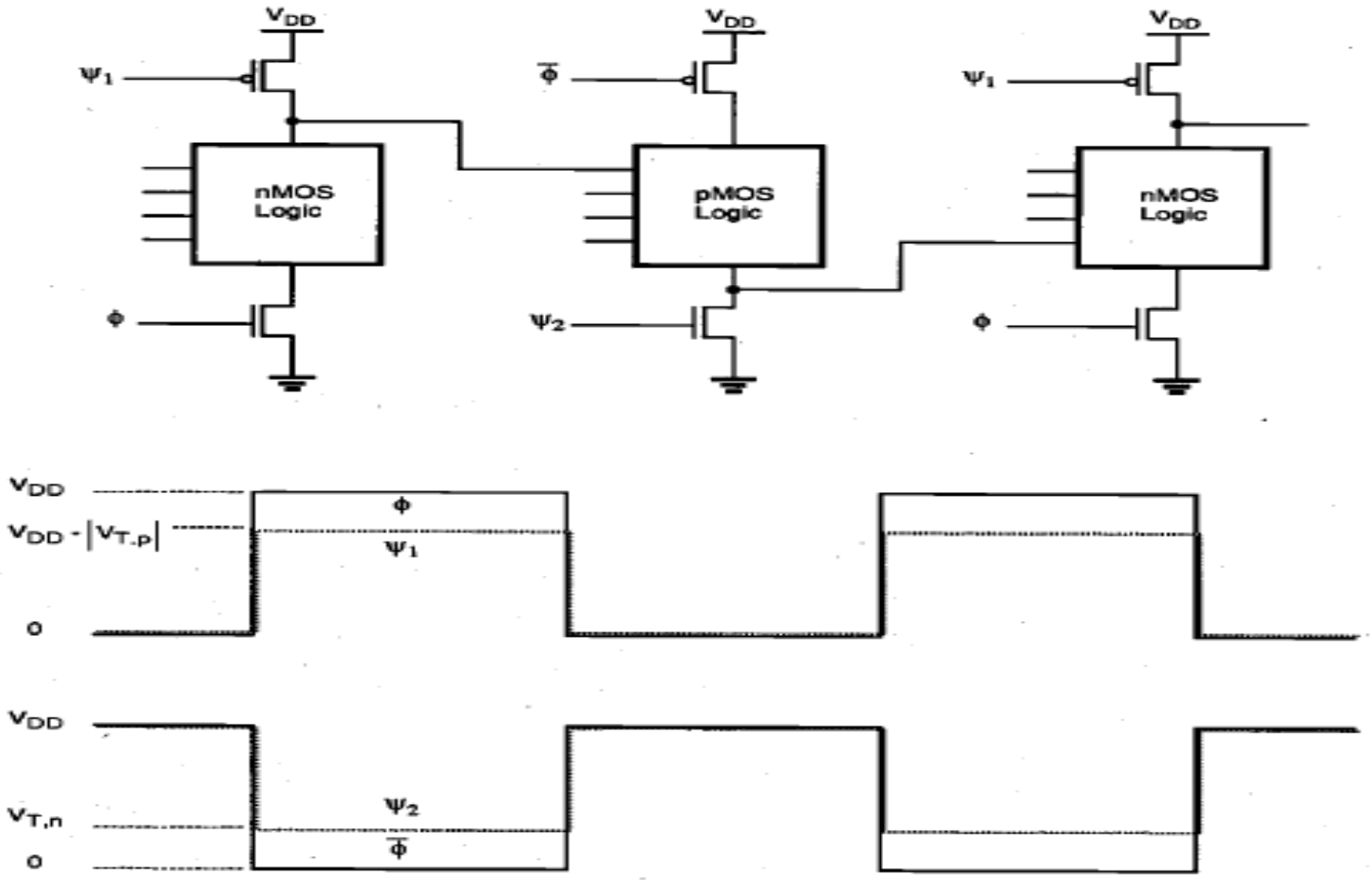


Fig. General circuit structure and the clock signals of Zipper CMOS

True Single-Phase Clock (TSPC) Dynamic CMOS