UNIVERSITY OF CALIFORNIA

Santa Barbara

Wide Bandwidth Power Heterojunction Bipolar Transistors and Amplifiers

A Dissertation submitted in partial satisfaction of the

requirements for the degree Doctor of Philosophy

in

Electrical and Computer Engineering

by

Yun Wei

Committee in charge:

Professor Mark Rodwell, Chair

Professor Steve Long

Professor Umesh Mishra

Professor Robert York

March, 2003

The dissertation of Yun Wei is approved.

Professor Steve Long

Professor Umesh Mishra

Professor Robert York

Professor Mark Rodwell, Committee Chair

November, 2002

Wide Bandwidth Power Heterojunction Bipolar Transistors and Amplifiers

Copyright © 2003

by

Yun Wei

To my wife and daughter.

ACKNOWLEDGEMENTS

I would like to say that I feel lucky of being a student of Prof. Rodwell. I am always indebted to him for his advice and assistance during my graduate school career. I have learned not only the knowledge, but also gained a lot from his enthusiasm for scientific research and willingness to help others. I would also like to thank my committee members Prof. Umesh Mishra, Prof. Stephen Long and Prof. Robert York for their patience, encouragement and support.

It was my greatest pleasure of working with my colleagues, who gave me both helps and friendliness. Thanks to Dino, James, Shri, Tomas and PK, who gave me the first laboratory training. Special thanks to Paidi, Miguel and Dennis; this thesis would not have been possible without their contributions. Also thanks to Sangmin, Zach, Shouxuan, Mattias, and Navin for their suggestions and support during this work. The excellent support received from Jack Whaley, Mike Anzlowar, Bob Hill, and Neil Baker led to the successful fabrication of the devices and MMICs described in this work.

No words in the world can express my gratitude to my wife Yuhong. I am always encouraged by her love but her smile always makes me feel deep guilty when I came back from work in the late midnight. Also I would like to thank my parents for bringing me up and supporting me to pursue my dream.

VITA

EDUCATION

B.S	Electrical and Computer Engineering, Fudan University, Shanghai, China, July, 1991
M.S	Electrical and Computer Engineering, Oregon Graduate Institute of Science and Technology, Portland, Oregon, July, 1998
Ph.D	Electrical and Computer Engineering, University of California, Santa Barbara, December, 2002

PROFESSIONAL EMPLOYMENT

1991-1997:	Researcher, High Speed Device and Circuit Lab, Institute of Semiconductors, Chinese Academy of Sciences, Beijing, China
1999-2002:	Research Assistant, Picosecond Electronics Research Lab, Department of Electrical and Computer Engineering, University of California, Santa Barbara

PUBLICATIONS

Y. Wei, M. Urteaga, Z. Griffith, D. Scott, S. Xie, V. Paidi, N. Parthasarathy, M. Rodwell, "75 GHz, 80 mW InP DHBT Power Amplifier." *IEEE Radio Frequency Integrated Circuits Symposium,* Philadelphia, PA, June 8-13.2003

Y. Wei, S. Lee, K. Sundararajan, M. Dahlstrom, M. Urteaga, M. Rodwell. "High current (100 mA) InP/InGaAs/InP DHBTs with 330 GHz f_{max}," *14th Indium Phosphide and Related Materials Conference,* p.47-50. Piscataway, NJ (2002).

Y. Wei, S. Lee, K. Sundararajan, M. Dahlstrom, M. Urteaga, M. Rodwell, "W-band InP/InGaAs/InP DHBT MMIC power amplifiers," *2002 IEEE MTT-S International Microwave Symposium Digest*, Vol.2, p.917-20, Piscataway, NJ (2002)

Y. Wei, K. Sundararajan, M. Urteaga, Z. Griffith, D. Scott, V. Paidi, N. Parthasarathy, M. Rodwell, "40 GHz MMIC Power Amplifier in InP DHBT *IEEE Lester Eastman Conference on High Performance Devices*, Newark, Delaware, August 6-8. 2002

S. Krishnan, D. Scott, M. Urteaga, Z. Griffith, Y. Wei, M. Dahlstrom, N. Parthasarathy, M. Rodwell, "An 8-GHz Continuous-Time Sigma-Delta DHBT Analog-Digital Converter in an InP-based Technology." *International Microwave Symposium,* Philidelphia, June 8-13. 2003

M. Urteaga, D. Scott, S. Krishnan, Y. Wei, M. Dahlstrom, Z. Griffith, N. Parthasarathy, M. Rodwell, "Multi-stage G-band (140-220 GHz) InP HBT amplifiers," *24th Annual Technical Digest,* p.44-7. Piscataway, NJ (2002).

S. Lee, H. Kim, M. Urteaga, S. Krishnan, Y. Wei, M. Dahstrom, M. Rodwell, "Transferred-substrate InP/InGaAs/InP double heterojunction bipolar transistors with f_{max}=425 GHz. *Electronics Letters,* vol.37, no.17, p.1096-8. Publisher: IEE, UK (2001)

M. Urteaga, D. Scott, T. Mathew, S. Krishnan, Y. Wei, M. Dahlstrom, M. Rodwell, "Characteristics of submicron HBTs in the 140-220 GHz band," *Device Research Conference. Conference Digest. IEEE.,* p.101-2. Piscataway, NJ (2001)

S. Jaganathan, S. Krishnan, D. Mensa, T. Mathew, Y. Betser, Y. Wei, D. Scott, R. Urteaga, M. Rodwell, "An 18-GHz continuous-time Sigma - Delta analog-digital converter implemented in InP-transferred substrate HBT technology," *IEEE Journal of Solid-State Circuits,* vol.36, no.9, Sept. 2001, p.1343-50. USA (2001)

T. Mathew, S. Jaganathan, D. Scott, S. Krishnan, Y. Wei, M. Urteaga, M. Rodwell, S. Long, "2-bit adder carry and sum logic circuits clocking at 19 GHz clock frequency in transferred substrate HBT technology," *Electronics Letters,* vol.37, no.19, p.1156-7. Publisher: IEE, UK (2001)

S. Lee, M. Urteaga, Y. Wei, Y. Kim, M. Dahlstrom, S. Krishnan, M. Rodwell, "Ultra high f_{max} InP/InGaAs/InP transferred substrate DHBTs," *Device Research Conference, IEEE.* p. 107-8. Piscataway, NJ (2002)

Y. Kim, M. Dahlstrom, S. Lee, Y. Wei, M. Rodwell, A. Gossard, "High speed (207 GHz f_T), low thermal resistance, high current density metamorphic InP/InGaAs/InP DHBTs grown on a GaAs substrate," *Conference Proceedings. 14th Indium Phosphide and Related Materials Conference, IEEE.* p. 39-41. Piscataway (2001)

M. Urteaga, D. Scott, T. Mathew, S. Krishnan, Y. Wei, M. Rodwell, "Single-stage G-band HBT amplifier with 6.3 dB gain at 175 GHz," *IEEE Gallium Arsenide Integrated Circuit Symposium. 23rd Annual Technical Digest 2001, IEEE.* p. 83-7. Piscataway, NJ (2001).

S. Krishnan, M. Dahlstrom, T. Mathew, Y. Wei, D. Scott, M. Urteaga, M. Rodwell, W. Liu, D. Lubyshev, X. Fang, Y. Wu, "InP/InGaAs/InP double heterojunction bipolar transistors with 300 GHz F_{max}," *Conference Proceedings. 2001 International Conference on Indium Phosphide and Related Materials. IEEE.* p.31-4. Piscataway, NJ (2001)

M. Urteaga, D. Scott, T. Mathew, S. Krishnan, Y. Wei, M. Rodwell. "185 GHz monolithic amplifier in InGaAs-InAlAs transferred-substrate HBT technology," *2001 IEEE MTT-S International Microwave Sympsoium Digest, IEEE.* vol.3, p.1713-16 vol.3. Piscataway, NJ (2001)

T. Mathew, H. Kim, D. Scott, S. Jaganathan, S. Krishnan, Y. Wei, M. Urteaga, S. Long, M. Rodwell, "75 GHz ECL static frequency divider using InAlAs/InGaAs HBTs," *Electronics Letters,* vol.37, no.11, p .667-8. Publisher: IEE, UK (2001)

S. Krishnan, D. Mensa, J. Guthrie, S. Jaganathan, T. Mathew, R. Girish, Y. Wei, M. Rodwell, "Broadband lumped HBT amplifiers," *Electronics Letters,* vol.36, no.5, p.466-7. Publisher: IEE, UK (2000)

M. Rodwell M, Y. Betser, S. Jaganathan, T. Mathew, K. Sundararajan, S. Martin, R. Smith, Y. Wei Y, M. Urteaga, D. Scott, S. Long, "Submicron lateral scaling of HBTs and other vertical-transport devices: towards THz bandwidths," *GAAS 2000. Conference Proceedings. Microwave Eng. Eur.* p.4, London, UK (2000)

ABSTRACT

Wide Bandwidth Power Heterojunction Bipolar Transistors and Amplifiers

By

Yun Wei

Wide bandwidth power hetero-junction bipolar transistors (HBT) fabricated in a transferred-substrate technology have been developed, which exhibit 330 GHz power gain cut-off frequency at 100 mA collector current and 3.6V collector-emitter voltage. The collector-emitter breakdown voltage is 7V. These power HBTs were realized in a multiple finger topology that substantially reduces the base-collector parasitic capacitance, which typically limits the bandwidth of power HBTs. While thermal effects may be of concern in small area HBT design, the thermo-electric feedback effects are much more complex and significant in large-area devices. Methods of characterizing electrical and thermal properties of multiple finger HBTs are demonstrated and approaches for improving both their bandwidth and power performance are presented. AN HBT large-signal model is developed based on device electrical and thermal characterization. The model demonstrates accurate agreement with measurement data and has been used in power amplifier design.

W-band (75 GHz to 110GHz) monolithic integrated circuit (MIC) power amplifiers with transferred-substrate power HBTs have been developed. Amplifier results include 40 mW saturated output power at 85 GHz and 80 mW saturated output power at 75 GHz. These are the highest output power reported in HBT technology at these frequencies. A V-band power amplifier using the same technology was also developed and demonstrates output power of 80mW at 40 GHz with 1-dB gain-compression.

A millimeter-wave air dipole antenna fabrication technology was developed to enable the development of high efficiency 94 GHz quasi-optical arrays. The process is compatible with the transferred-substrate HBT monolithic microwave integrated circuit technology. By using quasi-optical power combining technique, the output power of numerous W-band power amplifiers can be combined in the free space to achieve high-power amplifiers.

TABLE OF CONTENTS

1 Introduction 1
2 Wide bandwith power heterojunction bipolar transistors (DHBT) 3
2.1 III-V HBT scaling………………………………………………….. 3
2.2 Transferred-substrate HBTs……………………………………….. 6
2.3 Kirk effect in HBTs………………………………………………… 7
2.4 Offset, saturation voltage and avalanche breakdown……………….10
2.5 HBT Self-heating……………………………………………………11
2.6 Current hogging in multiple finger HBTs………………………….. 13
2.6.1 Thermal coupling and coupling thermal resistance................. 13
2.6.2 Systematic analysis of current hogging in multiple finger HBTs 13
2.6.3 Prevention of current hogging in multiple finger HBTs 22
2.7 Current distribution along long emitter fingers……………………..23
2.7.1 Emitter current crowding in long finger HBTs 23
2.7.2 Thermal stability and ballast resistance under constant V_{be} bias 25
2.8 RF bandwidth degradation in power HBTs…………………………28
2.8.1 Device topology and layout geometry 28
2.8.2 Premature Kirk effect.. 30
2.8.3 Base metal resistance 30
2.8.4 Emitter resistance 34
3 Power HBT characterization.. 37
3.1 HBT DC characteristics……………………………………………..37
3.2 HBT small signal measurements and hybrid-π model extraction….. 37
3.3 HBT thermal effects……………………………………………….. 40
3.4 Self-heating thermal resistance……………………………………...42
3.5 Coupling thermal resistance and current hogging loci……………...46
3.6 Thermal time constant………………………………………………50
3.7 HBT modeling………………………………………………………51
3.7.1 Large signal modeling based on S-parameter extraction and finite element mode1.. 51
3.7.2 Device large-signal model with thermal effects..................... 53
4 Power HBT in transferred-substrate technology 56
4.1 Transferred-substrate InP DHBT layer structure…………………. 56
4.2 Transferred-substrate InP DHBT fabrication……………………... 58
4.3 Multiple finger DHBT topology………………………………….. 60
4.3.1 Multiple finger DHBT thermal-electric characterization........ 63
4.3.2 Multiple finger DHBT device results..................................... 64
4.3.3 Hybrid-π model extraction.. 69
4.3.4 Large signal model.. 71
4.4 Power DHBTs with a lightly doped emitter epitaxial layer………. 73

4.4.1 LDE DHBT design 73
4.4.2 LDE transferred-substrate DHBT results 75
4.5 Discussion 79
5 High frequency DHBT MMIC power amplifiers 80
5.1 Class-A power amplifier design.. 80
5.2 HBT power amplifier topologies.. 84
5.2.1 Single stage power amplifier 84
5.2.2 Multi-stage power amplifier 85
5.2.3 Cascode power amplifier... 87
5.2.4 Balanced power amplifier 88
5.3 InP DHBT Power amplifiers in transferred-substrate technology... 89
5.3.1 40 GHz cascode power amplifier... 90
5.3.2 94 GHz cascode power amplifier... 94
5.3.3 85 GHz common base power amplifier................................. 99
5.3.4 75 GHz LDE power amplifier 102
5.3.5 Other W-band power amplifiers in transferred-substrate DHBT technology 106
5.4 Conclusions.. 109
6 Conclusion...110
6.1 Achievements... 110
6.2 Future Work..111
Reference..112
Appendix: Fabrication of 94 GHz antenna array in HBT technology 119
A.1 94 GHz antenna array fabrication... 120
A.2 Process design... 121
A.3 Process with very thick photo resist.......................................123
A.4 Au plating... 127
A.5 Results of antenna process on GaAs substrate......................... 129
A.6 94 GHz antenna array fabricated in TS HBT technology.......... 132
A.7 Conclusion.. 136

LIST OF FIGURES

Figure 2.1: III-V mesa HBT cross-section 4
Figure 2.2: Transferred-substrate HBT cross-section 6
Figure 2.3 Electric charge, field and conduction energy band profiles of base and collector under different injection current level 7
Figure 2.4 Band profile simulation of Kirk effect (current blocking) in DHBT 8
Figure 2.5: Quasi-saturation due to Kirk effect in DHBTs 9
Figure 2.6: Typical HBT DC common-emitter characteristics 10
Figure 2.7: Current hogging in a 4-finger HBT 14
Figure 2.8: Current hogging-common mode and differential mode 14
Figure 2.9: Topology of an N-finger HBT 15
Figure 2.10: Two modes of current variation in a 2-finger HBT 18
Figure 2.11: Current variation modes in 3-finger HBTs 19
Figure 2.12: Layout modification of 4-finger HBT to suppress current hogging 21
Figure 2.13: Air-bridged multiple finger HBT 22
Figure 2.14: Current and temperature profiles in a long-emitter HBT 23
Figure 2.15: Long emitter diagnostic TS HBT 24
Figure 2.16: Current distribution among emitter sections at V_{ce}=3V. Each emitter section has dimensions of 1 μm × 10 μm 25
Figure 2.17: Thermo-electric feedback loop in HBT 25
Figure 2.18: Current distribution along the three emitter sections at V_{ce}=3V with different external emitter ballast resistors. Each emitter section has a dimension of 1 μm × 10 μm 27
Figure 2.19: Layout of multiple finger mesa HBT 29
Figure 2.20: Cross-section of transferred-substrate multiple finger HBT 29
Figure 2.21: Base metal resistance and base current flow 30
Figure 2.22: Voltage distributions along base contact stripe 31
Figure 2.23: Layout of multiple finger transferred substrate DHBT 32
Figure 2.24: Base RC network with multiple finger DHBT 32
Figure 2.25: Layout of multiple finger transferred substrate DHBT. The grey shaded region is the base contact pad area. 34
Figure 2.26: Hybrid-π model of transferred substrate DHBT with 1 μm × 8 μm emitter and 2 μm × 10 μm collector. This model was extracted at I_C=7 mA and V_{ce}=2 V 35
Figure 2.27 Unilateral gain, maximum available power gain and current gain simulations of the HBT model of Figure 2.26 in common emitter configuration 35
Figure 2.28: Unilateral gain, maximum available power gain and current gain simulations of the HBT model of Figure 2.26 in common base configuration 36
Figure 3.1: On-wafer LRL calibration patterns 38
Figure 3.2: HBT small signal hybrid-π model 39

Figure 3.3: Current collapse arising from current distribution instability in a 4-finger DHBT with A_E=1 μm × 16 μm/finger 41
Figure 3.4: V_{be}-V_{ce} plot, for an HBT with A_E=1 μm × 32 μm , taken at base current steps of 260 μA, with and offset of 260 μA. The HBT has β=25. 41
Figure 3.5: DHBT self-heating simulation schematic 44
Figure 3.6: DC common-emitter characteristics of the self-heating HBT model. 44
Figure 3.7: Circuit schematic and experimental data of thermal resistance 45
Figure 3.8: Current hogging loci on I-V plot 47
Figure 3.9: Schematic of multiple finger HBT thermal resistance measurement. The X marks denote open connections. 47
Figure 3.10: Multiple finger DHBT thermal resistance measurement results 49
Figure 3.11: Another thermal resistance measurement circuit for 4-finger HBT 50
Figure 3.12: Distributed model of transferred-substrate HBT 51
Figure 3.13: Distributed hybrid-π model of transferred-substrate HBT 52
Figure 3.14: Large-signal model of transferred-substrate HBT 53
Figure 3.15: Thermal feedback HBT large signal model 54
Figure 3.16: Schematic of large signal model of finger 1 in a 2-finger HBT 55
Figure 4.1: Band diagram of InP HBT 58
Figure 4.2: Diagram of transferred-substrate technology 59
Figure 4.3: Die photograph of a first generation 8-finger TS HBT. Each finger has 1 μm×16 μm emitter and 2 μm×20 μm collector 60
Figure 4.4: DC common-base characteristics of an 8-finger TS-HBT. 61
Figure 4.5: RF gains of the first generation 8-finger TS HBT 61
Figure 4.6: Comparison of two multiple finger DHBT topologies 62
Figure 4.7: Thermal resistance test structure for multiple finger TS DHBT 63
Figure 4.8: 4-finger 1 μm × 16 μm common emitter TS DHBT 65
Figure 4.9: DC common-emitter characteristics of 4-finger 1 μm × 16 μm TS DHBT 65
Figure 4.10: RF gains of 4-finger 1 μm × 16 μm common emitter TS DHBT 66
Figure 4.11: 4-finger 1 μm × 16 μm common base TS DHBT 66
Figure 4.12: DC common-base characteristics of 4-finger 1 μm × 16 μm TS DHBT 67
Figure 4.13: RF gains of a 4-finger 1 μm × 16 μm common base TS DHBT 67
Figure 4.14: 8-finger 1 μm × 16 μm common base TS DHBT 68
Figure 4.15: DC common-base characteristics of 8-finger 1 μm × 16 μm TS DHBT 68
Figure 4.16: RF gains of 8-finger 1 μm × 16 μm common base TS DHBT 69
Figure 4.17: 4-finger common emitter TS DHBT hybrid-π model 69
Figure 4.18: hybrid-π model simulation compared to the measured S-parameters 70

Figure 4.19: 4-finger hierarchy large signal model 71
Figure 4.20: Large signal model simulation compared to the measured S-parameters at I_C=57 mA and V_{ce}=2.2 V 72
Figure 4.21: DC large signal model simulation compared to measurement for 4-finger 1 μm × 16 μm common emitter TS DHBT 72
Figure 4.22: LDE DHBT band diagram 74
Figure 4.23: Equivalent ballasting circuits of long emitter DHBTs 76
Figure 4.24: DC common-emitter characteristics of a 4-finger 1 μm × 24 μm HBT with a lightly-doped emitter epitaxy 76
Figure 4.25: DC common-emitter characteristics of a 4-finger 1 μm × 24 μm HBT without the lightly-doped emitter epitaxy 77
Figure 4.26: DC common-base characteristics of 8-finger 1 μm × 24 μm DHBT with lightly doped emitter epitaxy 77
Figure 4.27: DC common-base characteristics of an 8-finger 1 μm × 32 μm DHBT with lightly doped epitaxy 78
Figure 4.28: RF gains of an 8-finger 1 μm × 32 μm common base DHBT with lightly doped epitaxy 78
Figure 5.1: Class-A power amplifier optimum output load line 81
Figure 5.2: Reduced output power loading conditions 82
Figure 5.3: Load contour on Smith Chart 83
Figure 5.4: Load contour matching schematic 83
Figure 5.5: Harmonic simulated dynamic load line 84
Figure 5.6: Single stage power amplifiers 84
Figure 5.7: 2-stage power amplifier schematic 85
Figure 5.8: Gain compression in multi-stage power amplifier 86
Figure 5.9: Low frequency stability factor simulations of a two stage power amplifier 86
Figure 5.10: Cascode power amplifier architecture schematics 87
Figure 5.11: Balanced power amplifier with Wilkinson power combiner 88
Figure 5.12: Cross-section of passive circuits in transferred-substrate MMIC technology 89
Figure 5.13: 40 GHz power amplifier schematic 91
Figure 5.14: S-parameter simulation of power amplifier 92
Figure 5.15: Harmonic balance simulation at 40 GHz 92
Figure 5.16: Die photograph of 40 GHz power amplifier 93
Figure 5.17: Measured v-band S-parameters 94
Figure 5.18: Measured output power at 40 GHz 94
Figure 5.19: Schematic of 94 GHz cascode power amplifier 95
Figure 5.20: S-parameter simulation of 94 GHz cascode power amplifier 96
Figure 5.21: Harmonic balance simulation at 94 GHz 96
Figure 5.22: Dynamic load line simulation at 94 GHz on a single finger of the common base stage 97
Figure 5.23: Die photograph of 94 GHz cascode power amplifier 97

Figure 5.24: Measured w-band S-parameters 98
Figure 5.25: Measured output power at 90 GHz 98
Figure 5.26: 94 GHz common base power amplifier schematic 99
Figure 5.27: S-parameter simulation of common base amplifier 100
Figure 5.28: Harmonic balance simulation at 94 GHz 100
Figure 5.29: Die photograph of common-base amplifier 101
Figure 5.30: Measured W-band S-parameters 101
Figure 5.31: Measured output power at 85 GHz 102
Figure 5.32: Schematic of l6-finger common base power amplifier 103
Figure 5.33: S-parameter simulation of 16-finger common base amplifier 104
Figure 5.34: Harmonic balance simulation at 94 GHz 104
Figure 5.35: Die photograph of 16-finger common base power amplifier 105
Figure 5.36: Measured W-band S-parameters 105
Figure 5.37: Measured output power at 75 GHz 106
Figure 5.38: Die photograph of 32-finger common base power amplifier 107
Figure 5.39: Die photograph of two stages 16-finger common base power amplifier 108
Figure 5.40: SEM photograph demonstrating thinner metal ramp 108
Figure 5.41: Die photograph of W-band balanced power amplifier 109
Figure A.1: Diagraph of dipole antenna array and amplifier H-tree 120
Figure A.2: SEM photograph of plated air bridge 121
Figure A.3: 94 GHz air dipole antenna process flow 123
Figure A.4: Resist uniformity compensation process 125
Figure A.5: SEM photos of AZP9260 lithography 126
Figure A.6: Hot plate air-gap post-baking set-up cross-section 127
Figure A.7: Patterned plating diagraph 128
Figure A.8: Mechanism of high rate plating failure 129
Figure A.9: SEM photograph of high rate plating failure 129
Figure A.10: Photoresist peeled off during plating 129
Figure A.11: SEM photographs of the first generation antenna structure 130
Figure A.12: Wrinkles of thick photoresist after baking 131
Figure A.13: SEM photographs of second generation antennas 132
Figure A.14: Antenna with transferred-substrate MMIC 132
Figure A.15: Schematic of dipole antenna 133
Figure A.16: SEM photographs of 94 GHz dipole antenna 134
Figure A.17: Schematic of γ-matched antenna cross-section 135
Figure A.18: SEM photographs of 94 GHz γ-matched antennas 135
Figure A.19: RF measurement of γ-matched antenna 136

LIST OF FIGURES

Table 2.1: Three types of current variations and their thermal resistance matrix transformations…………………………………………………….....31
Table 4.1 InP/InGaAs DHBT layer structure.…………………………………...57
Table 4.2 InP/InGaAs DHBT layer structure.…………………………………75

Chapter 1

Introduction

This work presents characterization, design and fabrication of power heterojunction bipolar transistors (HBTs) with very high bandwidth. High frequency HBT power amplifiers are also demonstrated with record output power.

Despite the high efficiency and high linearity characteristics of III-V HBTs, III-V high-electron-mobility field-effect-transistors (HEMT) have dominated the microwave monolithic integrated circuits (MMIC) at frequencies above 50 GHz. Deep submicron InP-based HEMTs [1] have established record power levels for W-band solid-state power amplifiers [2] [3], substantially exceeding the power levels attained by HBTs.

The transferred-substrate HBT process [4] [5] allows simultaneous scaling of emitter and collector dimensions. With this technology, the base-collector parasitic capacitance of HBT can be substantially reduced and high bandwidth can be achieved. Scaling of HBTs has resulted in devices with very high measured power gains at mm-wave frequencies [6], enabling high-gain amplifiers in W-band [7] [8] and at 195GHz [9]. These previously reported HBTs have an InGaAs collector and subsequently, have low breakdown voltage and low output power. Several groups have recently reported InP-based double hetero-junction bipolar transistors (DHBTs) with > 300GHz f_{max} and collector breakdown voltage > 6V. Reported wideband InP-based DHBTs [10] [11] were small-area devices with < 16 mA maximum collector current. Higher current levels are required for microwave power applications. For example, a 5V-breakdown DHBT, with 160 mA peak collector current is required for 100mW unsaturated class-A output power. Large-emitter-area power HBTs, however, face additional design difficulties. Thermal instabilities result in current hogging between emitter fingers, decreasing the allowable HBT current before bandwidth collapse due to the Kirk effect. Further, large-area HBTs have large C_{cb} and very small intrinsic base resistance R_{bb}, due to the large number of emitter fingers. Small residual excess base resistance arising in either the base metallization or base contact interconnects can substantially increase the total base resistance, reducing f_{max}. In this work, electrical and thermal characterization for multiple finger HBTs are described and methods of improving thermal stability and bandwidth are also presented. Using transferred-substrate technology, large-junction-area InP DHBTs were developed exhibiting f_{max} of 330GHz when measured at 100 mA collector bias current and 3.6V collector-emitter bias voltage. By adding a lightly doped epitaxial (LDE) layer between the emitter and the emitter contact layer, a differential ballast scheme is achieved that significantly improves the thermal stability of large-area HBTs. Long-finger LDE InP DHBTs in transferred-substrate

technology thereby were fabricated, demonstrating 235 GHz f_{max} with bias current of 140 mA at a collector-emitter voltage of 3.7V.

An HBT large signal model suitable for electronic design automation (EDA) is needed for power amplifier design at frequencies above 75GHz. The development of the model is difficult because load-pull systems are either unavailable or costly at these frequencies. Since available commercial HBT models with a thermal sub-circuit can only be used in simulating self-heating effects of single-finger devices [12] [13], a large signal model for multiple finger HBTs based on a Gummel-Poon model was developed to include thermal and electrical coupling effects. This model was verified by comparing simulations with small-signal RF and DC measurements of fabricated devices and used in the design of power amplifiers.

InP DHBT transferred-substrate technology has been successfully applied in realizing millimeter wave power amplifiers with record output power. In the present work, reactively matched common-base amplifier MMICs were designed and fabricated, exhibiting 8.5 dB insertion gain at 85 GHz and a saturated output power of 42 mW. Other reactively matched common-base amplifiers with LDE layer structures demonstrate 80 mW saturated output power at 75GHz. Applications of the millimeter wave power amplifiers include: automotive and military radar, wireless networks, and mm-wave communications. The DHBT technology thus exhibits high power density and high linearity that is comparable to the state-of-the-art submicron PHEMTs.

By using quasi-optical power combining techniques, the output power of numerous wideband power amplifiers can be combined in free space in order to achieve high level output power at mm-wave frequencies. An integrated dipole antenna array is one such combiner. The dipole can be driven by single ended power amplifiers with balanced input signals. To reduce the signal loss by radiation into dielectric slab modes, an air-dielectric antenna is preferred for the spatial power combiner. In this work, an antenna array process utilizing gold electroplating was developed. The process is compatible with the transferred-substrate DHBT technology, and a number of antenna architectures were fabricated and integrated with on-wafer passive elements. The antennas were designed for 94 GHz, a minimum in the atmospheric absorption spectrum, and measurements showed a shift in the design frequency to 100GHz.

Chapter 2

Wide bandwidth Power heterojunction bipolar transistor (HBT)

Very wide bandwidth HBTs are required in high-frequency radar and communications. Monolithic millimeter integrated circuits (MMICs) include low-noise RF preamplifiers, multiple stages of amplification, and frequency conversion (mixers) that compose the microwave and millimeter-wave receiver and transmitter. The progressive improvements of the bandwidth of the transistors will drive the evolution of the radar and communication systems.

In an HBT, the emitter material has a wider band gap than the base. In forward bias, there is a barrier in the valence band at the base-emitter junction interface. The step prevents the back injection of holes from the *P* type base to the emitter. The base of an HBT can thus be heavily doped without decreasing the current gain (β). With such heavy base doping, the base resistance can be substantially reduced. With heavy base doping, the collector-base depletion region is mainly in the collector with negligible penetration into the base, and the base punch-through is prevented. Hence, a very thin base can be used to reduce the electron base transit time. Above all, compound semiconductor materials for HBTs have superior minority carrier diffusivity and majority carrier mobility in the base, and superior saturated drift velocity in the collector, factors which contribute to the high bandwidth of HBTs.

In Section 2.1, analysis of III-V HBT scaling is presented, in an effort to provide insight into the physics that determine the bandwidth of HBTs. As an effective approach of HBT scaling, transferred-substrate technology is introduced in Section 2.2. Power HBTs demonstrate complex thermal and electrical properties that affect the device power and frequency characteristics. Gain collapse, current hogging, premature Kirk effect, semi-saturation and excessive base feed resistance are the factors that degrade device performance. These will be introduced in the sections 2.3-2.9.

2.1 III-V HBT scaling

In high-speed digital and mixed-signal integrated circuits, Si based integrated circuits have the primary advantages of higher scales of integration and lower cost. However, for HBTs grown on GaAs or InP substrates, the energy band gap of emitter materials is much larger than that of the base allowing higher base doping. In contrast, constraints of allowable lattice mismatch in Si/SiGe HBTs limit the

allowable Ge:Si alloy ratio and the energy band difference ΔE_g is then much smaller than in III-V. For a C-doped InGaAs base of 300 **Å** thickness, the doping density can be up to $\sim 10^{20}$ cm^{-3} giving base sheet resistance of 500Ω/square, much less than the typical 4-8KΩ/square base sheet resistivity of a Si/SiGe HBT. In InAlAs/InGaAs HBTs with 0.2-0.3 μm collector thickness, effective collector velocities exceed 3×10^7 cm/s, approximately 3:1 higher than those observed in Si.

Despite the above advantages in III-V HBT, Si/SiGe HBTs have demonstrated competitive bandwidth to InP-based mesa HBTs. The high bandwidth of Si/SiGe HBTs comes from the aggressive submicron scaling that has matured in planar Si/SiGe technology. In addition, the self-aligned polysilicon contact processing in Si/SiGe reduces the base contact resistance and parasitic base-collector capacitance resulting in a reduction in the related charging time.

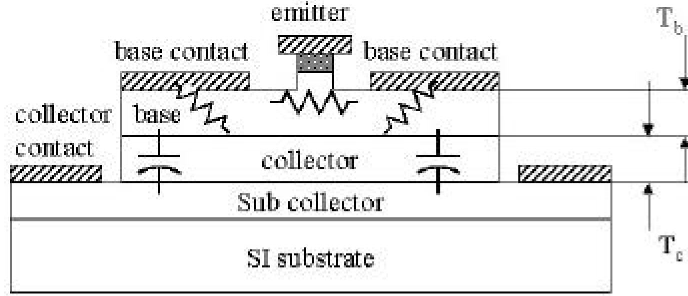


Figure 2.1: III-V mesa HBT cross-section

Figure 2.1 shows a simplified III-V mesa HBT cross-section. The current gain cut-off frequency f_t is described as:

$$\frac{1}{2\pi f_t} = \tau_b + \tau_c + \frac{kT}{qI_c}(C_{je} + C_{cb}) + (R_{ex} + R_c)C_{cb} \quad . \tag{2.1}$$

In Eqn. 2.1, τ_b and τ_c are the electron base transit time and collector transit time respectively; C_{je} is the emitter junction capacitance; C_{cb} is the parasitic base-collector capacitance; R_{ex} is the emitter resistance and R_c is collector resistance. $\tau_b \approx T_b^2 / 2D_{nb}$ is proportional to the square of the base thickness T_b. τ_c is the mean delay of the collector displacement current, which is $\tau_c = T_c/(2V_{eff})$, where T_c is the collector thickness and v_{eff} is the electron effective velocity under a voltage bias. Thinning the base and collector layers will reduce both τ_b and τ_c components of $1/2\pi f_t$.

The maximum current density of HBT is determined by the space-charge screening effect (Kirk effect) in the collector depletion layer, which will be discussed in detail in Section 2.3. The maximum collector current is [14]

$$I_{c,\max} = A_e (V_{cb} + \phi) 2\varepsilon v_{sat} / T_c^2 + qN_d v_{sat} A_{ec}^2 \quad . \tag{2.2}$$

The maximum allowable collector doping in order to ensure a fully depleted collector at minimum collector-emitter bias voltage $V_{cb,\min}$ is given by

$$N_{d,\max} = (V_{cb,\min} + \mathbf{f})2\mathbf{e} / qT_c^2 \quad , \tag{2.3}$$

where A_e is the area of the emitter junction area. Since C_{cb} is $\mathbf{e}A_c/T_c$, with the maximum current bias at $I_{c,\max} \propto A_e / T_c^2$, and $(kT / qI_c)C_{cb} \propto T_c(A_c / A_e)$. Scaling T_c and A_c reduces the collector capacitance charging time but requires an increase of the current density. C_{je} is the sum of two components, the depletion capacitance (C_{je_dep}), and the emitter-base depletion region diffusion capacitance (C_{je_dff}) [14]. As shown in [14], C_{je_dff}, which results from charge storage in the depletion region, is proportional to the square root of the depletion layer thickness, while C_{je_dep} is inversely proportional to the same thickness. R_{ex}, composed of the contact resistance and emitter bulk semiconductor resistance, plays an important role in limiting the scaling of HBT for high $f_{\mathbf{t}}$. For simplicity, this resistance is approximated as R_{ex}~$\mathbf{r}_e/A_e$, where $\mathbf{r}_e$ parameter including both bulk and contact terms.

The $R_{ex}C_{cb}$ charging time can thus be written as: $R_{ex}C_{cb}=(\mathbf{e}\mathbf{r}_e/T_c)(A_c/A_e)$, from which it can be seen that either the collector thickness scaling or increasing the collector-emitter area ratio will increase $R_{ex}C_{cb}$.

High $f_{\mathbf{t}}$ requires thinner base and collector layers and increased collector current density. But the thinning of collector will introduce low breakdown and larger C_{cb}. The increase of current density may also impose a limit to device reliability.

Lateral scaling of HBTs is significant in achieving high f_{max}. The HBT's power gain cut-off frequency f_{max} is approximately:

$$f_{\max} = \sqrt{\frac{f_{\mathbf{t}}}{8\mathbf{p}R_{bb}C_{cbi}}} \quad . \tag{2.4}$$

C_{cbi} is the component of the collector capacitance internal to the base resistance. R_{bb} is the base resistance that is composed of the contact resistance R_{b_cont}, base-emitter gap resistance R_{gap} and the spreading resistance under emitter layer:

$$R_{bb} = R_{b,cont} + R_{gap} + R_{spread} \quad ,$$

$$R_{b,cont} = \sqrt{\mathbf{r}_s \mathbf{r}_c} / 2L_e \quad ,$$

$$R_{gap} = \mathbf{r}_s W_{eb} / 2L_e \quad ,$$

$$R_{spread} = \mathbf{r}_s W_e / 12L_e \quad . \tag{2.5}$$

In Eqn. 2.5, $\mathbf{r}_s$ is the base sheet resistivity; $\mathbf{r}_c$ is the metal-base contact resistivity. The geometry W_{eb} is the undercut of the emitter, W_e is emitter junction width and L_e is emitter length. Given that $C_{cb}=\mathbf{e}A_c/T_c=\mathbf{e}W_cL_c/T_c$, the product of the base resistance and the collector base capacitance is:

$$R_{bb}C_{cb} = \left[(\sqrt{\mathbf{r}_s \mathbf{r}_c} + \mathbf{r}_s W_{eb})(\frac{\mathbf{e}}{2})(\frac{L_c}{L_e})\right]\left[\frac{W_c}{T_c}\right] + \left[(\frac{\mathbf{r}_s \mathbf{e}}{12})(\frac{L_c}{L_e})\right]\left[\frac{W_c W_e}{T_c}\right] \quad . \tag{2.6}$$

Note that $C_{cbi} \neq C_{cb}$, hence the above analysis is highly simplified. Nevertheless, from Eqn. 2.6 it can be seen that scaling of the collector width is effective in increasing the power gain bandwidth. In mesa HBTs, however, the base transfer length $L_{contact} = \sqrt{\rho_c / \rho_s}$ determines the minimum width of the base contact region, setting a minimum collector junction size independent of lithographic limitations on the collector-base junction width.

2.2 Transferred-substrate HBTs

Transferred-substrate technology [15] [16] was developed to circumvent this limit to collector width scaling. Figure 2.2 shows the cross-section of a transferred-substrate HBT.

In transferred-substrate technology, the collector contact is formed underneath the emitter but only a small fraction of the base mesa by means of a direct metal deposition step after inverting the transistor by using substrate transfer. As denoted in Figure 2.2, the width of the collector is then $W_C = W_E + W_{BE} + W_{BC}$, where W_{BE} is the undercut of the emitter-base mesa and W_{BC} is the base-collector-contact overlap. Therefore, collector scaling is only dependent upon lithographic limitations. By using high-resolution tools such as electron beam lithography, the collector and emitter can be simultaneously scaled to submicron dimensions and the bandwidth of HBTs can be substantially increased. A brief description of this technology will be presented in the Chapter 4.

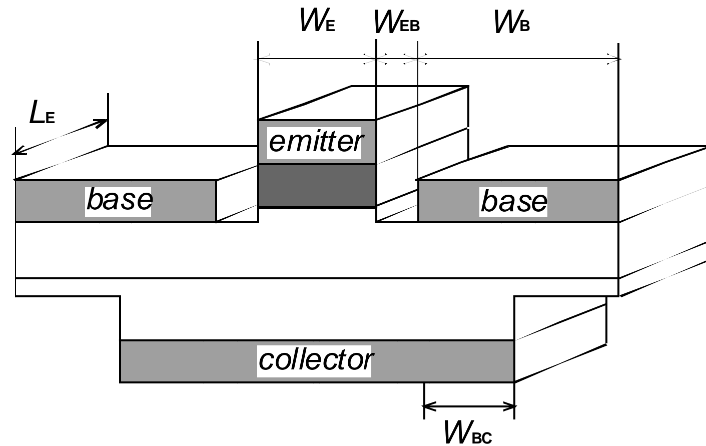


Figure 2.2: Transferred-substrate HBT cross-section

HBTs with record mm-wave power gain were developed in transferred-substrate technology that exhibit 23 dB Mason's gain (U) at 100 GHz [6]. By using electron-beam lithography, the emitter and collector of this device are scaled down to 0.4 µm × 6 µm and 0.6 µm × 10 µm respectively. Transferred-substrate technology is also used in the fabrication of InP DHBTs and a maximum power gain cut-off frequency

of 425 GHz was reported [10]. This DHBT also demonstrated 7 Volts breakdown at low collector current density.

2.3 Kirk effect in HBTs

Kirk effect [17], screening of the applied collector field by the collector electron flux, is observed in bipolar transistors at high biased collector current density. In both homojunction and single heterojunction bipolar transistors, Kirk effect leads to base push-out, which results in current gain collapse and increased base transit time. Base push-out, however, is prevented in double heterojunction bipolar transistors because the valence energy band barrier at the base-collector junction blocks the holes from spilling into collector. Instead, Kirk effect in DHBTs results in formation of a barrier in the collector depletion region which impedes current flow.

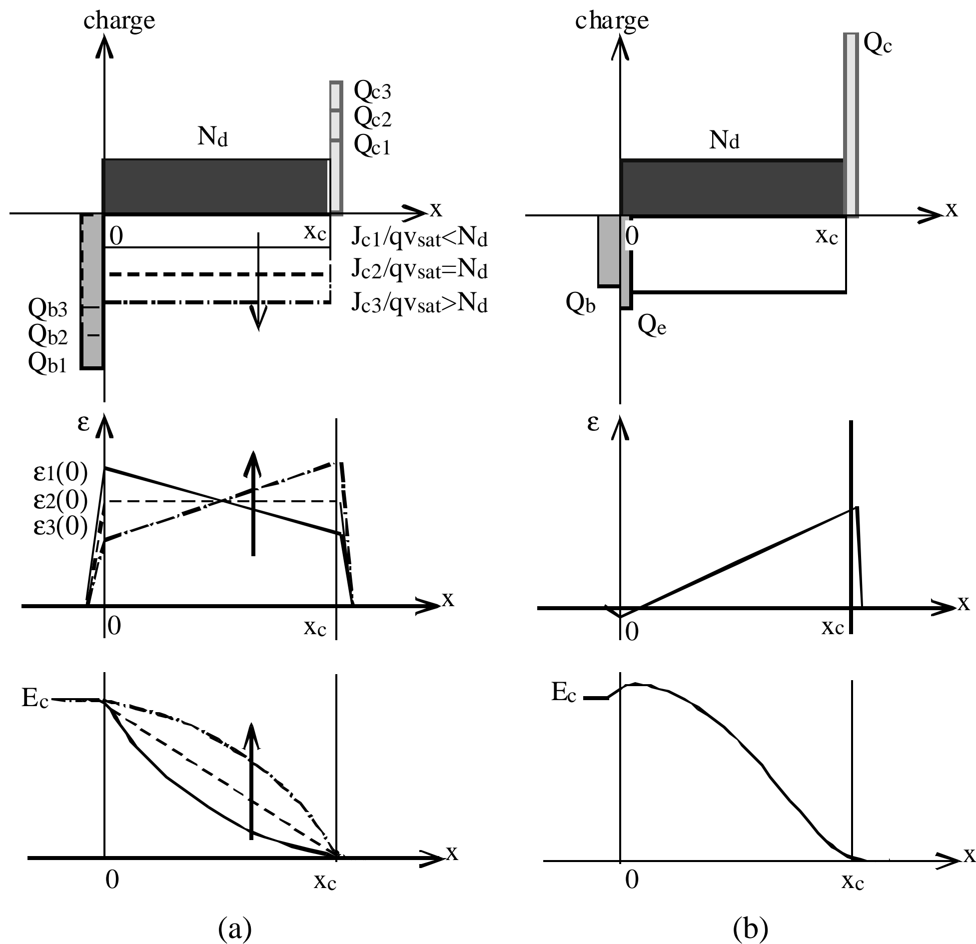


Figure 2.3 Electric charge, field and conduction energy band profiles of base and collector under different injection current

In DHBTs, the collector doping density N_D is usually chosen so that the collector is fully depleted at zero bias current. Figure 2.3 shows diagrams of the electric

charge, field and conduction energy band profiles of DHBTs at different bias currents. At low current density ($J_{c1}<qv_{sat}N_D$), the injected electrons travel at a saturated velocity v_{sat} to the n^+ sub-collector as shown in Figure 2.3 (a). As the current density increases from J_{c1} to J_{c3}, the injected electron density (J_c/qv_{sat}) in the depleted n^- region can exceed that of the ionized dopant, reversing the sign of the rate of change of the electric field (ε) in that region. Kirk effect is defined as the current at which the electric field near the base-collector junction is below the threshold to sustain the electron's saturated velocity. This increases the electron density near the junction (Q_e in Figure 2.3 (b)). If the current is further increased, the retarded electrons Q_e will reverse the electric field near the collector-base junction, forming a barrier in the conduction band, as shown in Figure 2.3 (b). Figure 2.4 (provided by Mr. Mattias Dahlstrom) demonstrates the conduction energy band simulations at different collector bias currents using Band profile simulation software.

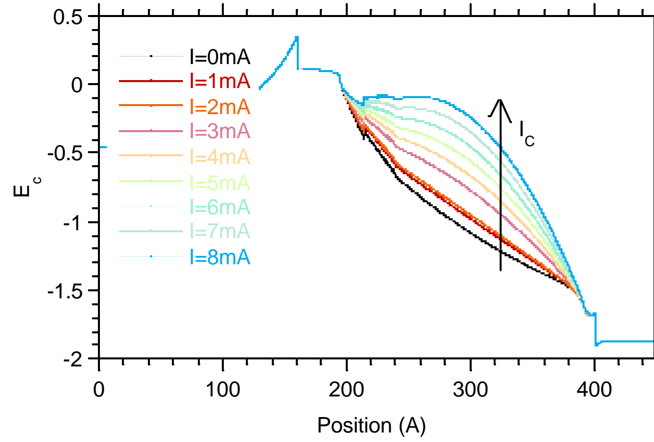


Figure 2.4 Band profile simulation of Kirk effect (current blocking) in DHBT

As Kirk effect is approached in a DHBT, the collector transit time τ_c is increased, as is expressed by:

$$\tau_c = \int_0^{T_c} \frac{(1-x/T_c)}{v(x)}\,dx \equiv \frac{T_c}{2v_{eff}} \quad . \tag{2.7}$$

T_c is the collector thickness and v_{eff} is the effective electron velocity. At higher current densities, such that a potential barrier is formed in the collector base junction, electrons are trapped in the base, and τ_b increases.

The Kirk threshold current density J_{Kirk} through the emitter junction is then approximately given by

$$J_{Kirk} = \frac{2\varepsilon v_{efft}(V_{CE,\min} + V_{CE})}{T_C^2} \quad . \tag{2.8}$$

ε is the semiconductor dielectric constant, T_c is the collector thickness, V_{CE} is the collector-emitter bias voltage, and $V_{CE,\min}$ is the bias voltage necessary to fully deplete the collector base junction. Eqn. 2.8 shows that Kirk threshold current increases with an increased collector-emitter bias voltage V_{CE} or thinner collector, while the latter will increase the base-collector parasitic capacitance and have an impact on the breakdown voltage.

The base-collector and base-emitter charging time decrease with an increase in the current density. Since Kirk effect limits the maximum current density, it plays a significant role in limiting the bandwidth of DHBTs.

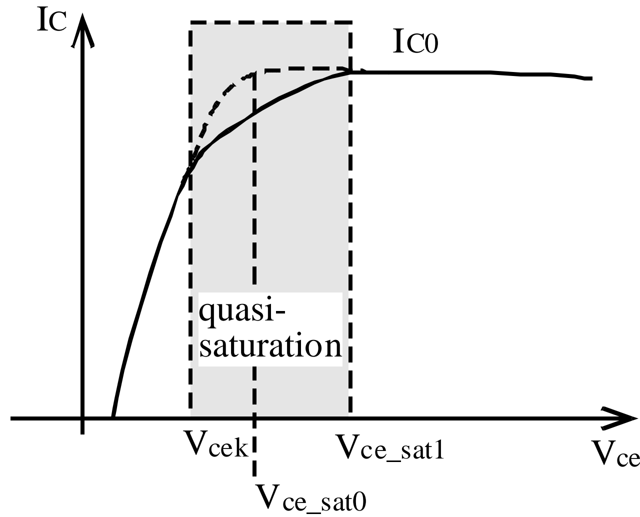


Figure 2.5: Quasi-saturation due to Kirk effect in DHBTs

Kirk effect also leads to an effect similar to saturation in the DC common-emitter characteristics of DHBTs. In Figure 2.5, as collector current increases above the Kirk threshold current at collector voltage V_{cek}, current gain collapse occurs. As collector voltage increases, the Kirk threshold current also increases. At V_{CE_sat1}, Kirk threshold current reaches I_{C0} and the device then operates without normally. As a result, the effective saturation voltage moves from V_{CE_sat1} to V_{CE_sat0}. The region between V_{cek} and V_{ce_sat1} is termed quasi-saturation.

2.4 Offset, saturation voltage and avalanche breakdown

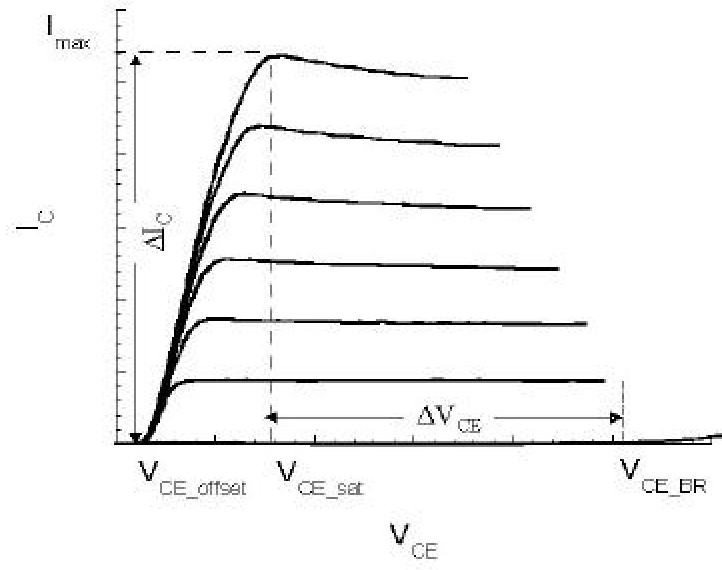


Figure 2.6: Typical HBT DC common-emitter characteristics

Figure 2.6 shows the typical DC common-emitter characteristics of an HBT. ΔI_C and ΔV_{CE} determines the dynamic operating range of the device and thereby determines the maximum output power of the DHBTs. The DC characteristics of a bipolar transistor can be described using Ebers-Moll equations. For HBTs with the considerations of parasitic terminal resistances and unequal ideality factors, the Ebers-Moll equations are modified as [18]:

$$\begin{aligned} I_E &= I_{ES}\left[\exp\frac{q(V_{BE}-I_BR_B-I_ER_E)}{\eta_{BE}kT}-1\right]-\alpha_R I_{CS}\left[\exp\frac{q(V_{BC}-I_BR_B+I_CR_C)}{\eta_{BC}kT}-1\right] \\ I_C &= \alpha_F I_{CS}\left[\exp\frac{q(V_{BE}-I_BR_B-I_ER_E)}{\eta_{BE}kT}-1\right]-I_{CS}\left[\exp\frac{q(V_{BC}-I_BR_B+I_CR_C)}{\eta_{BC}kT}-1\right] \end{aligned} \tag{2.9}$$

The offset voltage V_{CE_offset} is the base-emitter voltage when I_C=0, thus

$$V_{CE_offset}=\frac{\eta_{BC}kT}{q}\ln\left(\frac{I_{CS}}{I_{ES}}\right)-\frac{\eta_{BC}kT}{q}\ln(\alpha_F)+\frac{\eta_{BC}}{\eta_{BE}}I_BR_E+\left(1-\frac{\eta_{BC}}{\eta_{BE}}\right)(V_{BE}-I_BR_B) \ . \tag{2.10}$$

This equation can be simplified given the reciprocity theory and assuming that the I_BR_B term is negligible:

$$V_{CE_offset}=\frac{\eta_{BC}kT}{q}\ln\left(\frac{1}{\alpha_R}\right)+\frac{\eta_{BC}}{\eta_{BE}}I_BR_E \ . \tag{2.11}$$

Since α_R is far less than unity, V_{CE_offset} is mainly determined by the first term and the emitter resistance has little effect on the offset voltage.

The saturation voltage V_{CE_sat} can be obtained from Eqn. 2.10:

$$V_{CE_sat} = \frac{\eta_{BE} kT}{q} \ln\left(\frac{I_E - \alpha_R I_C}{I_{ES}(1-\alpha_F \alpha_R)} \right) - \frac{\eta_{BC} kT}{q} \ln\left(\frac{\alpha_F I_E - I_C}{I_{CS}(1-\alpha_F \alpha_R)} \right) + I_E R_E + I_C R_C \quad . \tag{2.12}$$

It can be seen from Eqn. 2.10 that collector and emitter resistance increase the saturation voltage and therefore reduce the output power of the transistor.

From the discussion in the previous section, Kirk effect can cause quasi-saturation in DHBTs. Eqn. 2.8 gives the Kirk threshold current of a DHBT and hence, the saturation voltage under Kirk effect can be derived as:

$$V_{CE_sat} = \left(\frac{T_C^2}{4\varepsilon v_{efft} A_C} + R_E + R_C\right) I_{Kirk} \quad . \tag{2.13}$$

The breakdown voltage denotes the point at which current increases dramatically with increased bias voltage. During transport, electrons leave the base and enter the collector where there is a high electric field. If the magnitude of the electric field is sufficient, electrons can acquire sufficient energy to generate electron-hole pairs before losing energy to various scattering mechanisms. The generated holes and electrons are then swept to the base and collector respectively by the electric field. Before being collected by the sub-collector, the generated electrons can cause additional impact ionization events, resulting in a total collector current M:1 larger than the electron flux entering the collector. Since this collector-base avalanche multiplication current adds to the base and the collector currents, the total collector current, as a function of the total base current is given by:

$$I_C = \left[\frac{\alpha_n M}{1-\alpha_n M}\right] I_B + \left[\frac{M}{1-\alpha_n M}\right] I_{CBO} \quad . \tag{2.14}$$

α_n is the base transport factor and M the multiplication factor, and ICBO is the base-collector leakage current. Note that the collector current in common-emitter operation becomes infinite (e.g. $V_{br,ceo}$ is reached) when $M = 1/\alpha_N = 1 + 1/\beta$. This is why $V_{br,ceo}$ is smaller than $V_{br,cbo}$, the latter being reached when M becomes infinite.

In DHBTs with large collector bandgap, the energy required to generate electron-hole pairs for impact ionization increases substantially, resulting in much higher breakdown voltage than in SHBTs. For example, the InAlAs/InGaAs SHBT has a V_{CE_BR} of 2V while an InP/InGaAs DHBT has a V_{CE_BR} of 10V with the same collector thickness.

2.5 HBT Self-heating

HBT self-heating is increased junction temperature arising from the dissipation of the transistor itself [19] [20], as opposed to heating from the overall dissipation on an IC. Junction temperature rise (ΔT_j) due to self-heating is proportional to the power dissipation through a factor called the thermal resistance (R_{th}):

$$\Delta T_j = R_{th} \cdot P = R_{th} \cdot (V_{ce} \cdot I_c) \quad . \tag{2.15}$$

P is the power dissipation, V_{ce} and I_c are the collector bias voltage and current respectively. R_{th} has units of $^oC/W$ and depends on the thermal conductivities of semiconductor materials and the device structure.

Unlike Si BJTs, the current gain of HBTs generally decreases when junction temperature rises [21] [22]. Self-heating, therefore, introduces a characteristic output negative differential resistance (NDR) in the common-emitter characteristics of an HBT. Shown in Figure 2.5, at constant base current, the collector current is decreased with increased collector voltage.

The most important self-heating effect in HBTs is base voltage regression. To maintain the same collector current as the junction temperature is increased, the base bias voltage must be reduced. The expression of collector current of an HBT was given by [23] [24] [25] that describes the current dependence on junction temperature:

$$I_C = I_{S0} \exp\left[\left(V_{be} - \frac{E_{g0}}{q} + \frac{\beta^*}{q} T\right) q / \eta k T\right] \quad . \tag{2.16}$$

V_{be} is the junction bias voltage, η is the ideality factor, I_{S0} is the saturation current, E_{g0} is the energy bandgap at 0 K, β^* is the bandgap shrinkage coefficient and T is the junction temperature. Notice that the saturation current in Eqn. 2.14 is also dependent upon on temperature. Including both these effects, an empirical expression for I_c is [18]:

$$I_C = I_{c0} \exp\left\{\frac{q}{\eta k T_A}\left[V_{be} - I_c (R_E + \frac{R_B}{\beta}) - \Phi(T - T_A)\right]\right\} \quad . \tag{2.17}$$

I_{c0} is a temperature independent term, R_E and R_B are the base and emitter resistance, β is the current gain, T_A is the ambient temperature, and Φ, called the thermo-electric feedback coefficient, is the rate of change of V_{be} over temperature at a fixed collector current. Base voltage regression is a positive thermal-electric feedback effect that can cause thermal run-away. The thermo-electric feedback coefficient is usually determined by measurement [25]. An expression for Φ determined by least-square-fitting to experimental data for a 2 μm $\times$ 20 μm emitter InP/InGaAs/InP DHBT is given in [26]:

$$\Phi = 6.600 \times 10^{-4} - 7.958 \times 10^{-5} \cdot \ln(I_C) \quad . \tag{2.18}$$

From Eqn. 2.15, 2.17 and 2.18, collector current can be determined by:

$$I_C = I_{c0} \exp\left\{\frac{q}{\eta k T_A}\left[V_{be} - I_c (R_E + \frac{R_B}{\beta}) - \Phi(R_{th} I_c V_{be} + \Delta T_A)\right]\right\} \quad . \tag{2.19}$$

The other DC property affected by self-heating is the base-collector leakage current. Given the presence of defect-introduced states near the base-collector junction, these states will generate electrons and holes at high temperature, which will then be swept into base and collector respectively, producing a collector-base

leakage current which is then multiplied by the transistor current gain, Eqn. (2.15). In addition to its increased breakdown field, the wider bandgap of InP results in greatly reduced I_{cbo} due to carrier thermal generation. However, the InGaAs used in the base-collector grade of a DHBT has a narrow bandgap and hence can produce significant leakage current. This the leakage current will increase with temperature.

2.6 Current hogging in multiple finger HBTs

Power HBTs are usually fabricated in a multiple finger topology. A multiple finger HBT is composed of several parallel HBT fingers with bases and collectors connected together. These fingers are always close to each other to reduce circuit parasitics, to improve component matching and to increase circuit density. Thermal coupling, therefore, arises between fingers. Due to thermo-electric feedback effects, multiple finger HBTs demonstrate complex thermo-electric characteristics, which affect the performances the device.

2.6.1 Thermal coupling and coupling thermal resistance

In multiple finger HBTs, the power dissipation in each HBT finger causes a variable degree of heating in all nearby fingers, with closer fingers being more strongly heated. The temperature rise of an HBT finger is, therefore, proportional to the power dissipation of another finger. Similar to self-heating thermal resistance, coupling thermal resistance is a factor relating the junction temperature of one HBT finger to the power dissipation of another. The junction temperature of an HBT finger is expressed as:

$$T_i = T_A + \sum_{j=1}^{N} R_{th_ij} \cdot P_j \quad . \tag{2.20}$$

In Eqn. 2.20, T_i is the junction temperature of the ith finger of an N finger HBT. P_j is the power dissipation in the jth finger. When i=j, R_{th_ij} is the self-heating thermal resistance, while, R_{th_ij} is the coupling thermal resistance from the jth finger. In addition to the semiconductor material and the device geometry, coupling thermal resistance is rapidly decreased with increased finger spacing.

2.6.2 Systematic analysis of current hogging in multiple finger HBTs

Current hogging is a mechanism producing current nonuniformity among the fingers in multiple finger HBTs. Figure 2.7 shows the schematic of a test circuit for the measurement of current hogging on a multiple finger DHBT, together with experimental data. In Figure 2.7, the DC common-emitter characteristics of I_{C1} and the current in the edge finger (Q_1) are plotted together with I_{C2}, the current in the three remaining fingers. These fingers are connected together (Q_2, Q_3 and Q_4). As V_{ce} is increased above 1.5 volts, I_{C1} rapidly decreases while I_{C2} increases. At certain V_{ce}, the distribution of currents between the 4 fingers becomes thermally unstable, and almost all of the total current is carried by the fingers Q2-Q4.

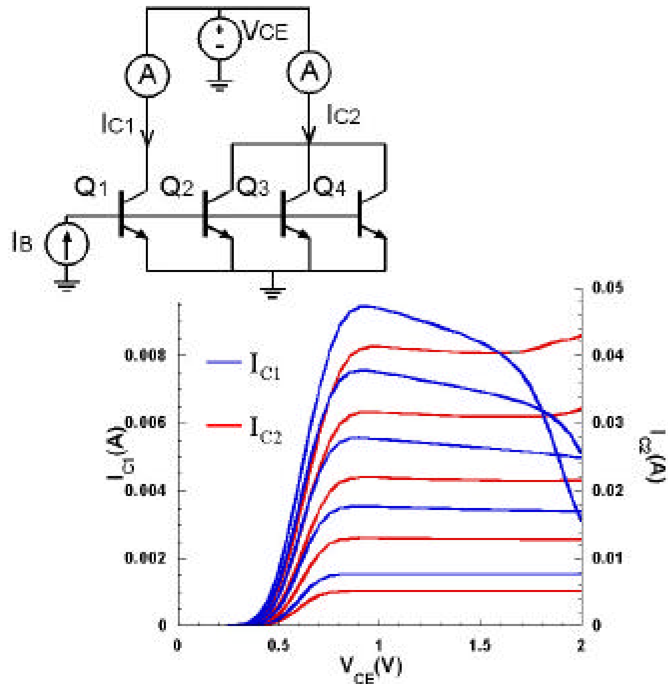


Figure 2.7: Current hogging in a 4-finger HBT

Since junction temperature increases with power dissipation, the fingers carrying larger currents become hotter than other fingers. Base voltage regression then decreases the V_{be} required for a fixed Ic; with I_c instead fixed, finger current increases. The effect is therefore self-reinforcing by positive feedback.

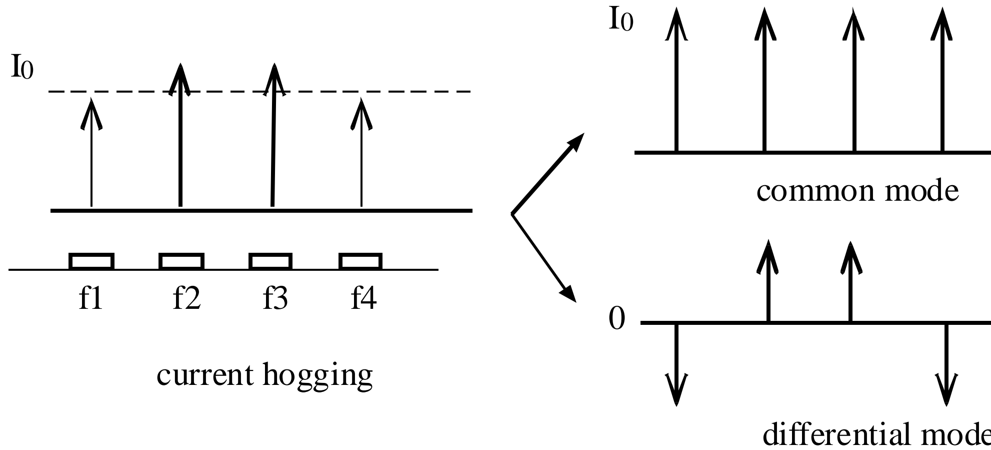


Figure 2.8: Current hogging-common mode and differential mode

Current instability in a multi-finger device is here analyzed by analyzed by considering various modes of fluctuation in the current distribution. With 4 fingers, there are 4 allowed modes. Symmetry reduces these 4 cases to 2 cases, that of common-mode and differential-mode current fluctuations, as is illustrated in Figure

2.8. Further, the common-mode instability is suppressed in those cases where the total transistor current is held constant by the external bias circuit. In that case, we must analyzer for thermal stability only for the differential mode.

In multiple finger HBTs, current hogging must be prevented because it degrades the bandwidth of device due to premature Kirk effect and inactive HBT finger operation. In the following paragraphs, the current variation mode with the related bias condition is studied and the maximum current at a certain bias voltage can be derived, below which current hogging will not occur. This current is thereby named the hogging current. The ratio in currents between the hottest and the coldest fingers is another figure of merit in evaluating current hogging: the higher the ratio, the stronger the differential mode which leads to significant current hogging.

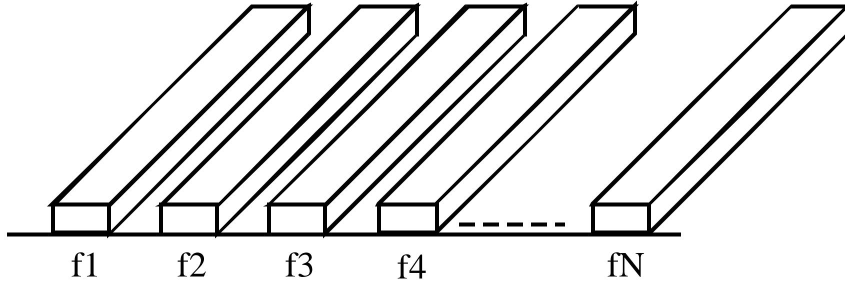


Figure 2.9: Topology of an N-finger HBT

Figure 2.9 shows the topology of an N-finger HBT. Substituting Eqn. 2.20 into 2.17, the current of the ith finger (I_{ci}) is:

$$I_{Ci} = I_{c0}\exp\left\{\frac{q}{\eta k T_A}\left[V_{be} - I_{ci}(R_{Ei} + \frac{R_{Bi}}{\beta}) - \Phi\left(\sum_{j=1}^{N} R_{th_ij}\cdot P_j + \Delta T_A\right)\right]\right\} \quad . \quad (2.21)$$

Given that the power dissipation of the Jth finger is $P_j = I_{cj}V_{ce}$, Eqn. 2.21 can be rewritten as:

$$I_{Ci} = I_{c0}\exp\left\{\frac{q}{\eta k T_A}\left[V_{be} - I_{ci}(R_{Ei} + \frac{R_{Bi}}{\beta}) - \Phi\left(V_{ce}\sum_{j=1}^{N} R_{th_ij}\cdot I_{cj} + \Delta T_A\right)\right]\right\} \quad . \quad (2.22)$$

Here we define a thermal resistance matrix $\vec{R}_{th}$ and current vector $\vec{I}_c$:

$$\vec{R}_{th} = \begin{pmatrix} R_{th_11} & R_{th_12} & \cdots & R_{th_1N} \\ R_{th_21} & R_{th_22} & \cdots & R_{th_2N} \\ \vdots & \vdots & \ddots & \vdots \\ R_{th_N1} & R_{th_N2} & \cdots & R_{th_NN} \end{pmatrix} \quad . \quad (2.23)$$

$$\vec{I}_c = \begin{pmatrix} I_{c1} \\ I_{c2} \\ \vdots \\ I_{cN} \end{pmatrix} \quad . \tag{2.24}$$

We also have

$$\vec{I}_c = I_{c0} EXP\left\{ \frac{q}{\eta k T_A} \left[V_{be}\vec{E} - (\vec{R}_E + \frac{\vec{R}_B}{\beta})\vec{I}_c - \Phi\left(V_{ce}\vec{R}_{th} \cdot \vec{I}_c + \Delta T_A \vec{E}\right) \right] \right\} \quad , \tag{2.25}$$

We define:

$$\vec{E} = \begin{pmatrix} 1 \\ 1 \\ \vdots \\ 1 \end{pmatrix}, \ \vec{R}_E = \begin{pmatrix} R_{E1} \\ R_{E2} \\ \vdots \\ R_{EN} \end{pmatrix}, \ \vec{R}_B = \begin{pmatrix} R_{B1} \\ R_{B2} \\ \vdots \\ R_{BN} \end{pmatrix} \quad . \tag{2.26}$$

$$EXP\begin{pmatrix} a_{11} & a_{12} & \cdots & a_{1n} \\ a_{21} & a_{22} & \cdots & \vdots \\ \vdots & \vdots & \ddots & \vdots \\ a_{n1} & \cdots & \cdots & a_{nn} \end{pmatrix} = \begin{pmatrix} \exp(a_{11}) & \exp(a_{12}) & \cdots & \exp(a_{1n}) \\ \exp(a_{21}) & \exp(a_{22}) & \cdots & \vdots \\ \vdots & \vdots & \ddots & \vdots \\ \exp(a_{n1}) & \cdots & \cdots & \exp(a_{nn}) \end{pmatrix} \quad . \tag{2.27}$$

Although Eqn. 2.25 is a similar expression to that applying to single finger HBTs (Eqn. 2.19), the current of each finger is mutually dependent on the other fingers in multiple finger HBTs. With common applied base-emitter bias voltage, the relative magnitudes of the currents in multiple finger HBTs will vary (current hogging) due the device physical variation or due to thermal coupling. Since there is no trivial solution to Eqn. 2.25, a dynamic analysis to the multiple finger system is given below.

Assuming the current in each finger is I_0 initially. At time t_0, a perturbation is applied and triggers current variation δI_{ci}. A new steady state can be reached if at any continuous instant $t_1 < t_2$:

$$\frac{\delta I_{ci}(t_2)}{\delta I_{ci}(t_1)} \leq 1 \quad . \tag{2.28}$$

From Eqn. 2.25, it can be obtained that:

$$\delta\vec{I}_c(t_2) = \frac{qI_0}{\eta k T_A}\left[-(\vec{R}_E + \frac{\vec{R}_B}{\beta})\delta\vec{I}_c(t_1) - \Phi V_{ce}\vec{R}_{th} \cdot \delta\vec{I}_c(t_1) \right] \quad . \tag{2.29}$$

The base and emitter resistances of each finger are usually designed to be identical in multiple finger HBTs. Therefore, if current hogging occurs at the hogging current I_h, by taking the ratio in Eqn. 2.28 as unity, we have:

$$\vec{R}_{th} \cdot \delta\vec{I}_c = -\frac{\frac{\eta k T_A}{q I_h} + (R_E + \frac{R_B}{\beta})}{\Phi V_{ce}} \delta\vec{I}_c \quad . \tag{2.30}$$

Further modifying Eqn. 2.30 gives:

$$\vec{R}_{th} \cdot \delta\vec{I}_c = \lambda \delta\vec{I}_c \quad . \tag{2.31}$$

$$\lambda = -\frac{\frac{\eta k T_A}{q I_h} + (R_E + \frac{R_B}{\beta})}{\Phi V_{ce}} \quad . \tag{2.32}$$

Eqn. 2.31 shows that the current variation is an eigenvector of the thermal resistance matrix and the hogging currents are determined by the eigenvalues.

For a 2-finger HBT, the thermal resistance matrix is:

$$R_{th} = \begin{pmatrix} R_{th_11} & R_{th_12} \\ R_{th_21} & R_{th_22} \end{pmatrix} \quad . \tag{2.33}$$

Because of symmetry, $R_{th_11}= R_{th_22}$ and $R_{th_12}= R_{th_21}$. Therefore, the eigenvalue equation of a 2-finger HBT is:

$$\begin{pmatrix} R_{th_11} & R_{th_12} \\ R_{th_21} & R_{th_22} \end{pmatrix} \begin{pmatrix} \delta I_{c1} \\ \delta I_{c2} \end{pmatrix} = \lambda \begin{pmatrix} \delta I_{c1} \\ \delta I_{c2} \end{pmatrix} \quad , \tag{2.34}$$

The eigenvalue can be obtained by:

$$\det \begin{pmatrix} R_{th_11} - \lambda & R_{th_12} \\ R_{th_12} & R_{th_11} - \lambda \end{pmatrix} = 0 \quad . \tag{2.35}$$

Eqn. 2.35 can be further expressed:

$$(R_{th_11} - \lambda)^2 = R_{th_12}{}^2 \quad . \tag{2.36}$$

Solutions of Eqn. 2.36 are: $\lambda_1=R_{th_11}+R_{th_12}$ and $\lambda_2=R_{th_11}-Rth_{_12}$. The corresponding eigenvectors are:

$$\lambda_1 = R_{th_11} + R_{th_12} \Rightarrow \begin{pmatrix} \delta I_{c1} \\ \delta I_{c2} \end{pmatrix} = \delta I_{c0} \begin{pmatrix} 1 \\ 1 \end{pmatrix} \quad , \tag{2.37}$$

$$\lambda_2 = R_{th_11} - R_{th_12} \Rightarrow \begin{pmatrix} \delta I_{c1} \\ \delta I_{c2} \end{pmatrix} = \delta I_{c0} \begin{pmatrix} 1 \\ -1 \end{pmatrix} \quad . \tag{2.38}$$

The current eigenvectors fall exactly into the two modes (Figure 2.10) for 2-finger HBTs. Eqn. 2.37 describes the common mode, in which the current variations are equal. Eqn. 2.38 describes the differential mode, in which the current variations are opposite. From the eigenvalues, the corresponding hogging currents are:

$$I_{h_com} = \frac{\frac{\eta k T_A}{q}}{|\Phi| V_{ce}(R_{th_11} + R_{th_12}) - (R_E + \frac{R_B}{\beta})} , \tag{2.39}$$

$$I_{h_diff} = \frac{\frac{\eta k T_A}{q}}{|\Phi| V_{ce}(R_{th_11} - R_{th_12}) - (R_E + \frac{R_B}{\beta})} , \tag{2.40}$$

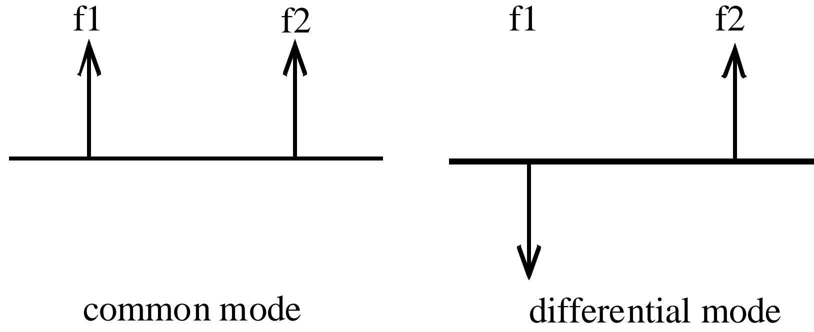


Figure 2.10: Two modes of current variation in a 2-finger HBT

There is an ambiguity in terminology. While the hogging current refers to formation of a nonuniform current distribution in all modes, in the common-mode this current corresponds to the condition under which the total bias current is thermally unstable in the case of a transistor biased with constant V_{be}. In the case of the power amplifiers in this thesis, transistors are biased under conditions of forced constant total I_c, and hence this case is not relevant. This mechanism will be discussed in the next section.

From Eqn. 2.40, the hogging current in the differential mode is increased with coupling thermal resistance, which means that the coupling thermal resistance increases the stability of 2-finger HBTs.

For 3-finger HBTs, considering the symmetry of the device structure, we have $R_{th_11}= R_{th_33}$, $R_{th_12}= R_{th_21}= R_{th_32}= R_{th_23}$, $R_{th_13}= R_{th_31}$, the thermal resistance matrix is:

$$\vec{R}_{th} = \begin{pmatrix} R_{th_11} & R_{th_12} & R_{th_13} \\ R_{th_12} & R_{th_22} & R_{th_12} \\ R_{th_13} & R_{th_12} & R_{th_11} \end{pmatrix} . \tag{2.41}$$

The matrix of Eqn. 2.41 has three eigenvalues and eigenvectors. The hogging currents and current variations are given without derivations:

$$
\text{(i)}\begin{cases} I_{h1} = \dfrac{\dfrac{\eta k T_A}{q}}{|\Phi| V_{ce}(R_{th_11} - R_{th_13}) - (R_E + \dfrac{R_B}{\beta})} \\ \delta\vec{I} = k\{1, 0, -1\} \end{cases}
$$

$$
\text{(ii)}\begin{cases} I_{h2} = \dfrac{\dfrac{\eta k T_A}{q}}{|\Phi| V_{ce}(R_{th_11} + \dfrac{R_{th_13}}{2} + \dfrac{\sqrt{R_{th_13}{}^2 + 8R_{th_12}{}^2}}{2}) - (R_E + \dfrac{R_B}{\beta})} \\ \delta\vec{I} = k\left\{1, \dfrac{-R_{th_13} + \sqrt{R_{th_13}{}^2 + 8R_{th_12}{}^2}}{2R_{th_12}}, 1\right\} \end{cases}, \qquad (2.42)
$$

$$
\text{(iii)}\begin{cases} I_{h3} = \dfrac{\dfrac{\eta k T_A}{q}}{|\Phi| V_{ce}(R_{th_11} + \dfrac{R_{th_13}}{2} - \dfrac{\sqrt{R_{th_13}{}^2 + 8R_{th_12}{}^2}}{2}) - (R_E + \dfrac{R_B}{\beta})} \\ \delta\vec{I} = k\left\{-1, \dfrac{R_{th_13} + \sqrt{R_{th_13}{}^2 + 8R_{th_12}{}^2}}{2R_{th_12}}, -1\right\} \end{cases}
$$

f1 f2 f3 f1 f2 f3 f1 f2 f3

(i) (ii) (iii)

Figure 2.11: Current variation modes in 3-finger HBTs

There are three modes of current variation that are shown in Figure 2.11. The first mode is exactly the differential mode while the others are composed of both common and differential modes. Therefore, all the three modes lead to current hogging. From Eqn. 2.42, since the hogging currents have relationships as $I_{h3} > I_{h1} > I_{h2}$, current hogging is most likely to occur in the second mode for 3-finger HBTs if the transistors are bias under constant V_{be} conditions. However, under constant-total-

I_c conditions, mode (ii) may be suppressed and mode (iii) then dominates. From Eqn. 2.42 (ii), the ratio of currents between the central and edge fingers is:

$$\frac{d\vec{I}_{c2}}{d\vec{I}_{c1}} = \frac{-R_{th_13} + \sqrt{R_{th_13}^{\ 2} + 8R_{th_12}^{\ 2}}}{2R_{th_12}} = \frac{-\left(\frac{R_{th_13}}{R_{th_12}}\right) + \sqrt{\left(\frac{R_{th_13}}{R_{th_12}}\right)^2 + 8}}{2} \quad . \tag{2.43}$$

Since $R_{th_13}/ R_{th_12} \leq 1$, $\delta I_{C2}/ \delta I_{C1}$ decreases as R_{th_13}/ R_{th_12} increases. Hence, as R_{th_13} approaches R_{th_12}, the current variation moves toward common mode and when $R_{th_13}=R_{th_12}$, a single common mode is attained. Mode (iii) then dominates, and the hogging current is given by 2.42 (iii). The physical explanation to the realization of the single common mode is that as R_{th_13} is increased to R_{th_12}, the thermal properties of the central finger become equal to those of the others. In other words, all fingers see identical thermal coupling, as in the case of the 2-finger HBTs. It is concluded that the current distribution in HBTs with fully identical fingers falls into either common mode or differential mode, and the stability is increased with increased thermal coupling.

For HBTs with more than four fingers, the eigenvalue equation becomes hard to solve. Symmetry methods aid thermal analysis of multiple finger HBTs with larger number of fingers: fingers are physically identical if they are symmetrically placed in the device layout. For example, the two fingers of the 2-finger HBT are identical while finger 1 and finger 3 are identical in a 3-finger HBT. Identical fingers always hold the same magnitude of current variation, as was shown earlier in the examples of 2-finger and 3-finger HBTs. This can simplify the analysis of multiple finger devices.

Type A:	$dI_1=dI_4$, $dI_2=dI_3$, $\boldsymbol{d\vec{I}} = \{dI_1, dI_2, dI_2, dI_1\}$ $\Rightarrow \boldsymbol{d\vec{I}}' = \{dI_1, dI_2\}$ $\Rightarrow \begin{pmatrix} R_{th_11}+R_{th_14} & R_{th_12}+R_{th_13} \\ R_{th_12}+R_{th_13} & R_{th_22}+R_{th_23} \end{pmatrix}$
Type B:	$dI_1=-dI_4$, $dI_2=-dI_3$, $\boldsymbol{d\vec{I}} = \{dI_1, dI_2, -dI_2, -dI_1\}$ $\Rightarrow \boldsymbol{d\vec{I}}' = \{dI_1, dI_2\}$ $\Rightarrow \begin{pmatrix} R_{th_11}-R_{th_14} & R_{th_12}-R_{th_13} \\ R_{th_12}-R_{th_13} & R_{th_22}-R_{th_23} \end{pmatrix}$
Type C:	$dI_1=dI_4$, $dI_2=-dI_3$, $\boldsymbol{d\vec{I}} = \{dI_1, dI_2, -dI_2, dI_1\}$ $\Rightarrow \boldsymbol{d\vec{I}}' = \{dI_1, dI_2\}$ $\Rightarrow \begin{pmatrix} R_{th_11}+R_{th_14} & R_{th_12}-R_{th_13} \\ R_{th_12}+R_{th_13} & R_{th_22}-R_{th_23} \end{pmatrix}$

Table 2.1: Three types of current variations and their thermal resistance matrix transformations

For 4-finger HBTs, finger 1 is physically identical to finger 4 and finger 2 is identical to finger 3. Therefore, the 4×4 thermal resistance matrix can be transformed to 2×2, which is shown in table 2.1*.

The new thermal resistance matrix can be expressed as:

$$\bar{\tilde{R}}_{th} = \begin{pmatrix} \tilde{R}_{th_11} & \tilde{R}_{th_12} \\ \tilde{R}_{th_21} & \tilde{R}_{th_22} \end{pmatrix} \quad . \tag{2.44}$$

The values of $\tilde{R}_{th_ij}$ in Eqn. 2.44 can be obtained from table 2.1 for different types of eigenvectors. The eigenvalues of Eqn. 2.44 can be solved from:

$$(\tilde{R}_{th_11} - \lambda)(\tilde{R}_{th_22} - \lambda) = \tilde{R}_{th_12}\tilde{R}_{th_21} \quad . \tag{2.45}$$

Solutions to Eqn. 2.45 are

$$\lambda_{1,2} = \frac{\tilde{R}_{th_11} + \tilde{R}_{th_22}}{2} \pm \frac{\sqrt{(\tilde{R}_{th_11} - \tilde{R}_{th_22})^2 + 4\tilde{R}_{th_12}\tilde{R}_{th_21}}}{2} \quad , \tag{2.46}$$

The corresponding eigenvectors are

$$k\left\{1, \frac{\tilde{R}_{th_22} - \tilde{R}_{th_11}}{2\tilde{R}_{th_12}} \pm \frac{\sqrt{(\tilde{R}_{th_11} - \tilde{R}_{th_22})^2 + 4\tilde{R}_{th_12}\tilde{R}_{th_21}}}{2\tilde{R}_{th_12}}\right\} \quad . \tag{2.47}$$

Finally, the hogging currents are:

$$I_{h_1,2} = \frac{\dfrac{\eta k T_A}{q}}{|\Phi| V_{ce} \lambda_{1,2} - (R_E + \dfrac{R_B}{\beta})} \quad . \tag{2.48}$$

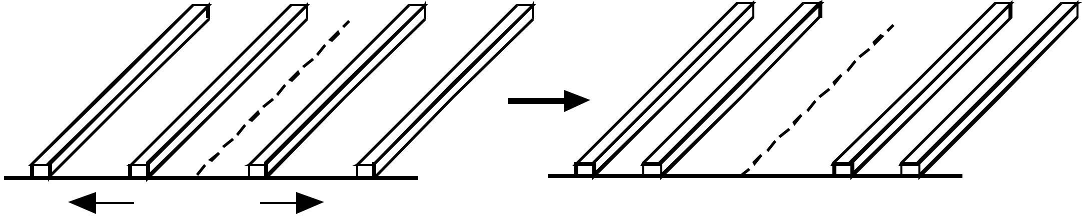


Figure 2.12: Layout modification of 4-finger HBT to suppress current hogging

Figure 2.12 shows a method to improve the stability of a 4-finger HBT. By increasing the spacing between finger 2 and 3 while decreasing the spacing between fingers 1 and 3 and between fingers 2 and 4, R_{th_23} is decreased towards R_{th_14}.

* Table 2.1 was obtained with the transformations: $R_{th_ij}=R_{th_ji}$, $R_{th_1(1+i)}=R_{th_4(4-i)}$, $R_{th_2(2+j)}=R_{th_3(3-j)}$ where $i = \{0,1,2,3\}$, $j = \{-1,0,1,2\}$.

Therefore, $(\tilde{R}_{th_22} - \tilde{R}_{th_11}) / 2\tilde{R}_{th_12}$ is reduced to zero so that $\boldsymbol{dI}_2 / \boldsymbol{dI}_1 \to 1$. From another point of view, this method makes fingers 1 and 3 have thermal characteristics identical to fingers 2 and 4. The two groups of fingers then form another 2-finger system so that the current hogging current is increased. This method introduces no processing modification.

2.6.3 Prevention of current hogging in multiple finger HBTs

In section 2.1.2, a method is developed to systematically analyze current instabilities in multiple finger HBTs. Current hogging occurs only when the differential mode is involved and the degree of current hogging can be evaluated by the current differential ratio. To prevent current hogging, the device must be biased according to the hogging current expression, which is the stable threshold at a given voltage.

Another method to improve thermal stability is to use a plated air bridge structure, as is shown in Figure 2.13. By providing a thick electroplated metal connection between either the HBT emitter or collector terminals [30], coupling thermal resistance can be greatly increased. As a result, all the fingers are thermally identical and their differential mode current distribution can be suppressed. But this method is less effective for high bandwidth power HBT. Those devices usually have submicron emitter dimensions that make the air bridge processing very difficult.

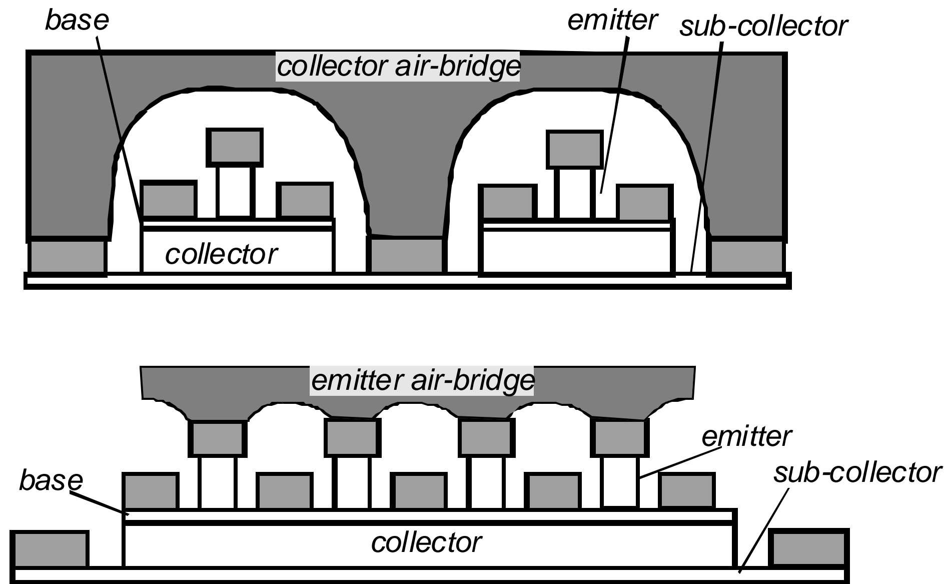


Figure 2.13: Air-bridged multiple finger HBT

According to the expression of the hogging current, the base and emitter resistances play important role in increasing device stability. These produce negative feedback to the B-E junction voltage and thereby tend to suppress current hogging.

The roles of base and emitter resistances in power HBTs will be discussed in Section 2.7.2

2.7 Current distribution along long emitter fingers

In the previous section, instabilities of current distribution among the fingers of a multiple finger HBT are analyzed. There is another source of internal instability due to the current distribution within an individual emitter finger.

2.7.1 Emitter current crowding in long finger HBTs

Non-uniformity in the current density within an emitter finger is referred to as emitter current crowding. The term emitter current crowding is usually used to describe the situation in which high current density appears at the edges of the emitter stripe, resulting from a lateral voltage drop across the base semiconductor. HBTs, however, have very low base sheet resistance and narrow emitter junction widths. Therefore, this kind of current crowding is negligible in HBTs.

Device self-heating can also cause a nonuniform current distribution along the length of the HBT emitter finger. Although thermal coupling between each part of the emitter finger is strong, at high power dissipation, the central part is most strongly heated. The increased heating results in a higher current density at a fixed bias voltage, similar to the case of the 3-finger HBTs. The effect is self-reinforcing, and with high thermal resistance and low emitter resistance the current distribution can be unstable. In this case the center part of the emitter takes the majority of the bias current and has the highest temperature (Figure 2.14). A simplified thermal model is given in [18].

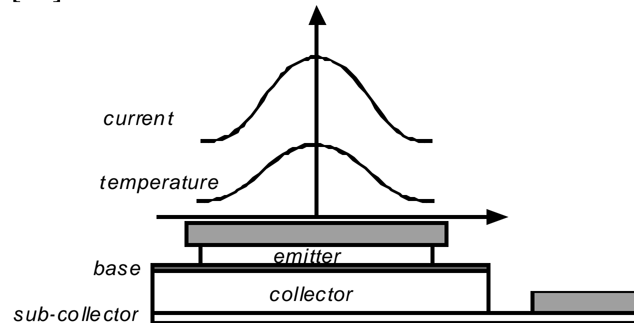


Figure 2.14: Current and temperature profiles in a long emitter HBT

To characterize HBTs with long emitter fingers, the test structure in Figure 2.15 was developed. In this structure, a 30 µm emitter of a transferred-substrate InP DHBT is separated into three sections, each of which is grounded through an external 8 Ω resistor. These emitter sections have a small 1 µm spacing and share common collector and base terminals. The break in the emitter contact metal unavoidably results in some reduction in the thermal coupling between emitter sections. In addition to the base and collector terminals, a pad is connected to each

emitter section, through which voltages on the emitter resistors can be sampled during DC I-V measurements. In this way, the current on each emitter section can be determined.

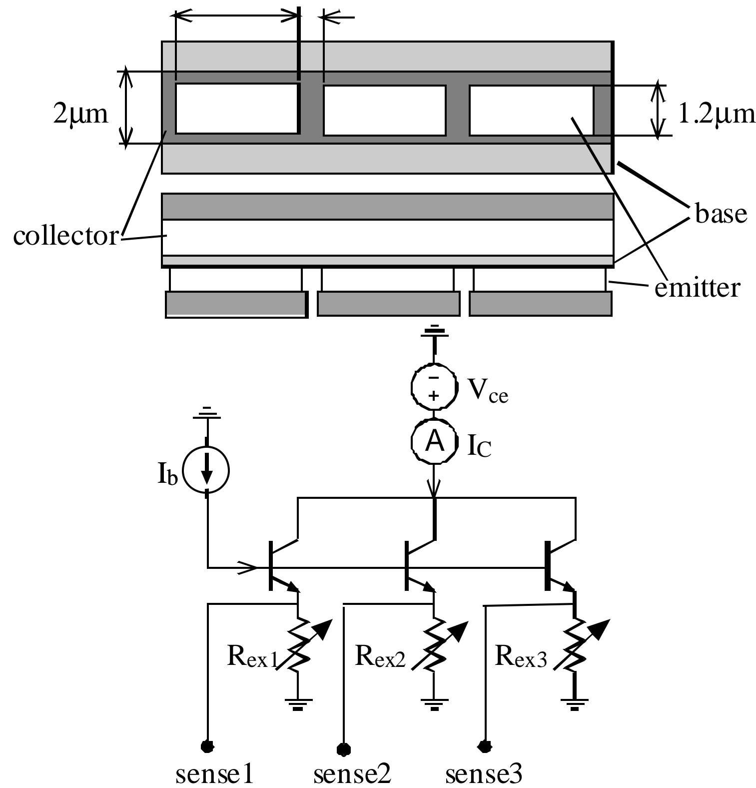


Figure 2.15: Long emitter diagnostic TS HBT

Figure 2.16 shows the current distribution on the three emitter sections at a V_{ce} of 3V. The five curves in Figure 2.16 correspond to five different base bias currents I_B. As power dissipation is increased, current density is no longer uniform along the emitter length. Current crowding is observed with the highest current density presented in the center of the emitter with more than a 50% variation along the emitter length at high V_{ce}.

Note that the stability within an HBT finger can be treated analytically in a manner similar to that of the multi-finger case, wherein the total emitter finger is analyzed in terms of infinitesimal length elements Δl having self- and mutual thermal resistances.

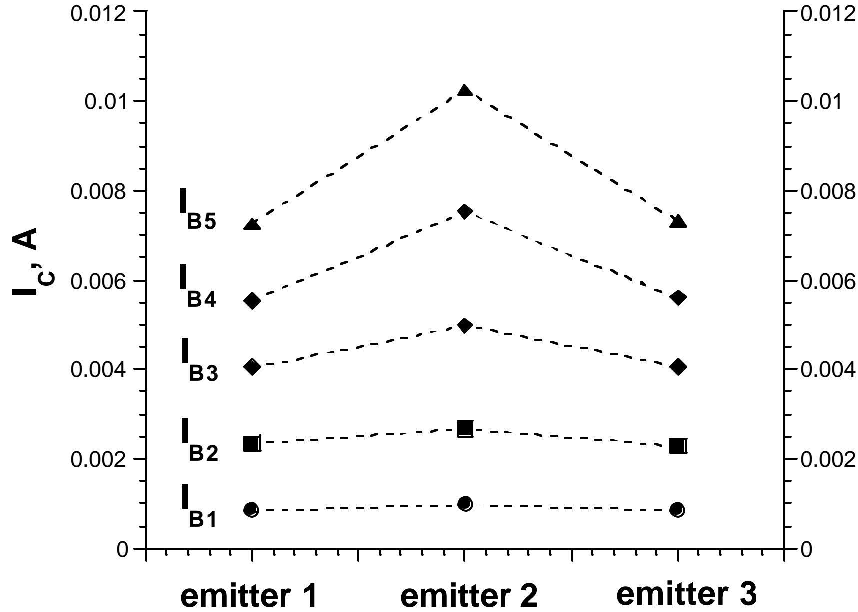


Figure 2.16: Current distribution among emitter sections at V_{ce}=3V. Each emitter section has dimensions of 1 µm × 10 µm

2.7.2 Thermal stability and ballast resistance under constant V_{be} bias

For the case of an HBT, single-finger or multiple fingers, operated under conditions of a forced base-emitter voltage, the thermal stability is more easily analyzed. This case approximates the case of thermal stability in a multi-finger HBT with negligible thermal coupling between fingers. We now cover this simplified case.

To analyze thermal runaway, Eqn. 2.19 is re-written here:

$$I_C = I_{c0} \exp\left\{ \frac{q}{\eta k T_A} \left[V_{be} - I_c (R_E + \frac{R_B}{\beta}) - \Phi\left(R_{th} I_c V_{be} + \Delta T_A\right) \right] \right\} \quad . \tag{2.19}$$

According to Eqn. 2.18, a thermo-electric feedback loop is drawn (Figure 2.17):

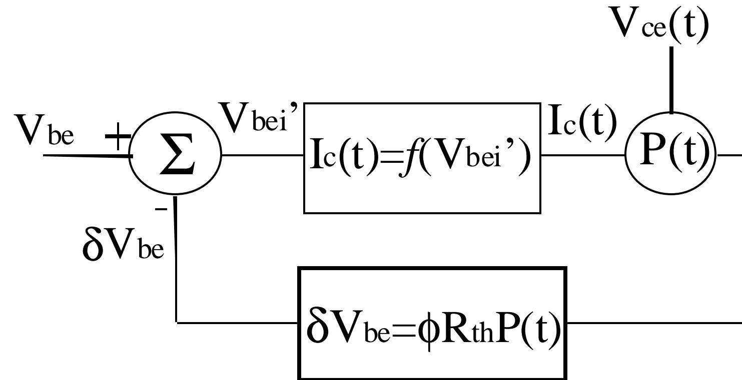


Figure 2.17: Thermo-electric feedback loop in HBT

At a certain collector current $I_C(t)$ and collector-emitter voltage $V_{ce}(t)$, the instantaneous power dissipation causes the junction temperature to rise by an amount of $P(t)R_{th}$. The change in temperature results in a reduction ($\delta V_{be} = \phi P(t)$) in the base-emitter voltage required for a constant collector current I_c. Given constant V_{be}, the collector current I_c must increase by an amount $\boldsymbol{d}I_C = (dI_c / dV_{be})\boldsymbol{d}V_{be}$, which then causes a change in power dissipation of $\boldsymbol{d}P = V_{ce}\boldsymbol{d}I_c$. In Figure 2.17, the gain of the forward and feedback paths in the thermo-electric feedback loop is described in Eqn. 2.49 and 2.50:

$$\frac{\partial I_C}{\partial T} = \frac{\partial I_C}{\partial V_{be}} \frac{\partial V_{be}^{'}}{\partial T} = \frac{|\Phi|}{\frac{\boldsymbol{h}kT_A}{qI_C} + R_E + \frac{R_B}{\boldsymbol{b}}} \quad , \tag{2.49}$$

$$\frac{\partial T}{\partial I_C} = \frac{\partial T}{\partial P} \cdot \frac{\partial P}{\partial I_C} = R_{th} V_{ce} \quad . \tag{2.50}$$

Thus the thermo-electric loop gain, which is defined as the thermal stability factor f, is:

$$f = \frac{|\Phi| I_C V_{CE} R_{th}}{\frac{\boldsymbol{h}kT_A}{q} + I_C R_E + \frac{I_C R_B}{\boldsymbol{b}}} \quad . \tag{2.51}$$

From elementary feedback theory, the system is unstable if $f \geq 1$. Eqn. 2.51 can be further simplified to:

$$f = \frac{|\Phi| V_{CE} R_{th}}{\frac{1}{g_m} + R_E + \frac{R_B}{\boldsymbol{b}}} \tag{2.52}$$

When f is less than unity, the system of Figure 2.17 is stable. If f exceeds unity, the closed-loop gain becomes unbounded and the positive thermo-electric feedback will drive current into infinity under conditions of constant applied V_{be} -this is called thermal runaway. From Eqn. 2.22 it can be seen that g_m is the only term in f related to the transistor bias current and is negligible at high current level if R_e is significant. In that case the bias dependence in f is therefore, only through the collector bias voltage.

The above expression neglects variation in of current gain with temperature. This effect becomes significant only if $d\boldsymbol{b}/dT$ is large and substantial base ballast resistance is employed. Such is not the case in the InP DHBTs here considered.

When f=1, Eqn. 2.52 can be modified to give:

$$I_h = \frac{\frac{\boldsymbol{h}kT_A}{q}}{|\Phi| V_{ce} R_{th} - (R_E + \frac{R_B}{\boldsymbol{b}})} \quad . \tag{2.53}$$

In Eqn. 2.53, I_h is the maximum current that the device can be biased without thermal runaway.

The base and emitter resistances stabilize the collector current through local electrical negative feedback and are therefore termed ballast resistance. The voltage drops on both the emitter and the base resistances increase as the collector current is increased, decreasing the voltage applied to the transistor junction. Using base ballast resistance is advocated in references [18] and [31], but from Eqn. 2.53 it can be seen that to achieve the same degree of ballasting, the value of R_B has to be β times that of R_E. Addition of base ballast resistance substantially reduces the transistor high-frequency power gain, and hence it must be by-passed by large capacitors to maintain the RF power gain. It is difficult to fit the required resistors and large by-pass capacitors within the allowed dimensions of a high-frequency integrated circuit. Although emitter ballasting has the drawbacks of increasing the collector-emitter saturation voltage and reducing the maximum stable common-emitter power gain, it is the more effective method for improving thermal stability.

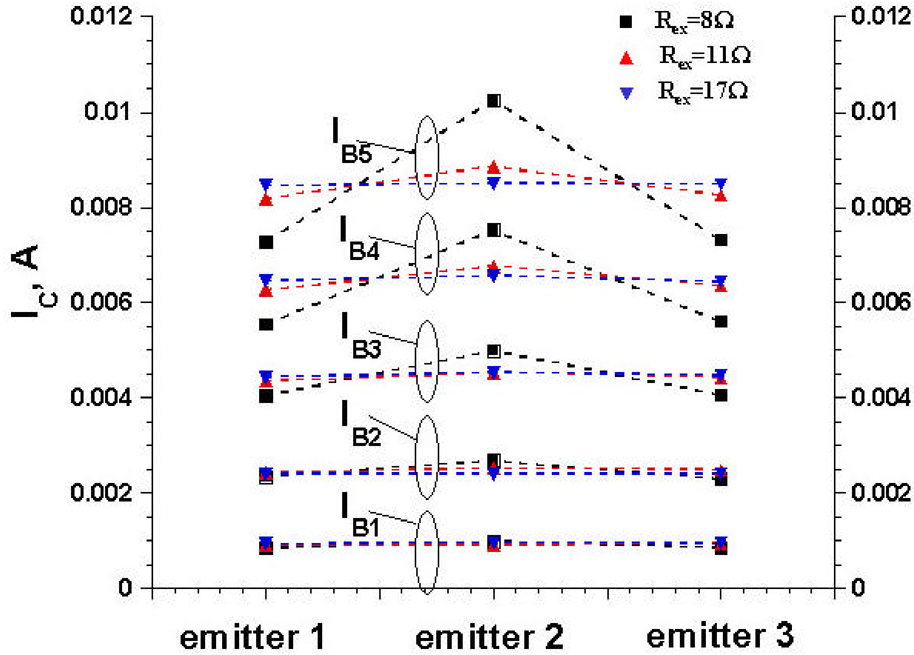


Figure 2.18: Current distribution along the three emitter sections at V_{ce}=3V with different external emitter ballast resistors. Each emitter section has a dimension of 1 μm × 10 μm

Emitter contact resistance contributes to the total emitter resistance and increases thermal stability. This resistance is unusually insufficient for thermal stability. Power HBTs usually employ additional external ballast resistance. Figure 2.18 shows the current distribution in a single finger HBT as a function of external ballast

resistance. The data was taken using the circuit of Figure 2.15. In the experiment, the total transistor current is varied, and the current distribution along the emitter finger is examined. Data was taken with external emitter ballast resistors (R_{ex}) of 8, 11, and 17 Ω, which were employed to each emitter section. It can be seen that the current distribution becomes strongly nonuniform when small emitter ballast resistors are employed, while a larger external ballast resistor (17 Ω), stabilizes the device**.**

Methods of obtaining R_{th} will be given in next chapter, by which the thermal resistance R_{th} for the device is measured to be 2 ^{o}C/mW, corresponding to 6 ^{o}C/mW for each individual emitter section. Φ=0.96mV/^{o}C from Eqn. 2.18, and the device is tested at V_{CE}=3V. From Eqn. 2.22, when the total current in the 3 fingers is I_{C_total}=24 mA, and hence the individual finger current is 8 mA, the stability factor requires:

$$R_E > |\Phi| V_{CE} R_{th} - \frac{1}{g_m} = 0.96mV \times 3V \times 6^o C/mW - \frac{26\,mV}{8\,mA} = 14.8\ \Omega \quad . \qquad (2.54)?$$

Given that the measured contact resistance (R_{cont}) of each emitter section is 2 Ω, the required external ballast resistor for each emitter section is:

$$R_{ex} > R_E - R_{cont} = 12.8\ \Omega \quad . \qquad (2.55)?$$

This calculation is consistent with the results of the measurement, where 11 Ω results in a relatively uniform distribution and 17 Ω a highly uniform distribution.

The same method can be applied to multiple finger HBTs. The required ballast resistance can be derived from the hogging current expression. By employing the calculated ballast resistance to real transferred substrate multiple finger DHBTs, current hogging was prevented and the device demonstrated very high bandwidth at high power dissipations. Those results will be presented in Chapter 4.

2.8 RF bandwidth degradation in power HBTs

In Section 2.1, it is concluded that the bandwidth of the device has a significant dependence on the scaling of the device dimensions. The complex layout of power HBTs, however, introduces significant additional high-frequency parasitics. In addition, thermal instability can result in a nonuniform current distribution, which can further degrade the bandwidth of power HBTs. Factors affecting the RF characteristics of power HBTs are introduced in this section.

2.8.1 Device topology and layout geometry

Figure 2.19: shows a typical layout for a multiple finger HBT in a mesa process. As addressed in Section 2.1, with a sub-collector underneath the whole base-collector junction, mesa HBTs may have significant excess base-collector parasitic capacitance unless a the mask layout is designed with care. In order to prevent excess C_{cb} in a multiple finger device, each emitter finger has a separate base mesa, with individual transistors connected by metal interconnects running over the semi-insulating substrate. These interconnections produce distributed parasitics which are significant at mm-wave frequencies.

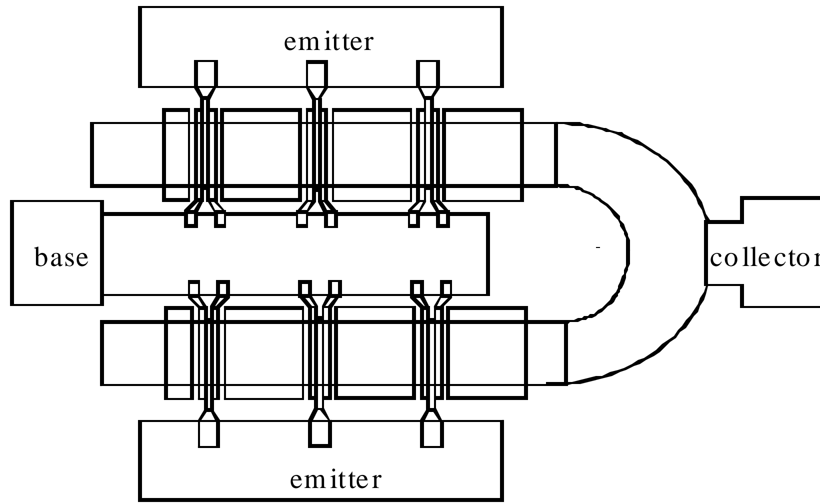


Figure 2.19: Layout of multiple finger mesa HBT

This thesis reports the development of multiple finger DHBTs in transferred-substrate technology. Figure 2.20 shows the diagram of the cross-section of the device.

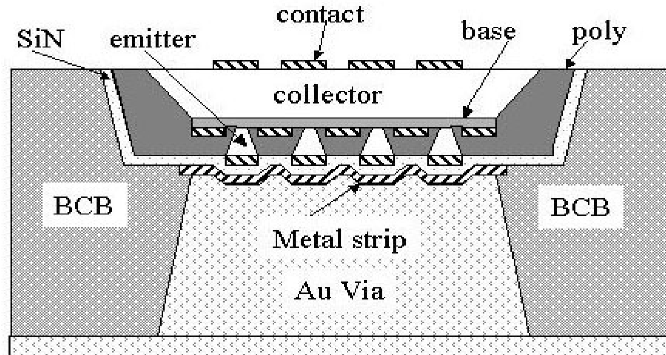


Figure 2.20: Cross-section of transferred-substrate multiple finger HBT

The substrate transfer process allows the base-collector parasitic capacitance to be substantially reduced. The transferred-substrate process also produces microstrip transmission lines on a dielectric of 5-µm thickness. Most interconnects are therefore well-characterized as microstrip lines.

Lee et al at UCSB [6] had earlier reported small-area DHBTs in the transferred-substrate with 460 GHz f_{max}. In the work of this thesis, power DHBTs of comparable bandwidth but much higher current-carrying capability were developed. The devices have exhibited greater than 300 GHz power gain cut-off frequency at 100 mA bias and V_{ce}=3.6 Volts. The devices are thermally stable for power dissipation less than 380 mW, and the low-current breakdown voltage is 7V. Power amplifiers using transferred-substrate multiple finger HBT have been developed, demonstrating 80

mW output power at 75 GHz. Design and fabrication of multiple finger HBTs and power amplifiers in transferred-substrate technology will be presented in the following chapters.

2.8.2 Premature Kirk effect

Kirk effect in DHBTs has been discussed in Section 2.3. When current hogging occurs in multiple finger DHBTs, or current crowding occurs within an individual finger, the collector current density can be far beyond the Kirk threshold in specific fingers for multiple finger HBT or specific locations within an emitter. Although the total bias current is well below the product of the emitter junction area and the Kirk-effect-limited current density, Kirk effect then still occurs. We refer to this effect as premature Kirk effect. This effect degrades the bandwidth of power HBT and raises the saturation voltage.

2.8.3 Base metal resistance

In HBT fabrication, the base contact is usually formed through a self-aligned evaporation of the base metallization over the emitter contact. The undercut emitter etch profile results in break in this metal as it passes over the emitter. To avoid short circuits between base and emitter, the thickness of the base contact must be at most a few hundred angstroms. Although the contact material is Au, which has high bulk conductivity, the base metal thickness is small and introduces significant metal sheet resistance. A 200Å Ti/400Å Pt/800Å Au base contact has a calculated sheet resistance of 0.3 Ω/?, a value that is sufficient to reduce the mm-wave power gain and cause current nonuniformity in HBTs with long emitter fingers. Figure 2.21 shows a diagram of the HBT with the distributed base metal resistance.

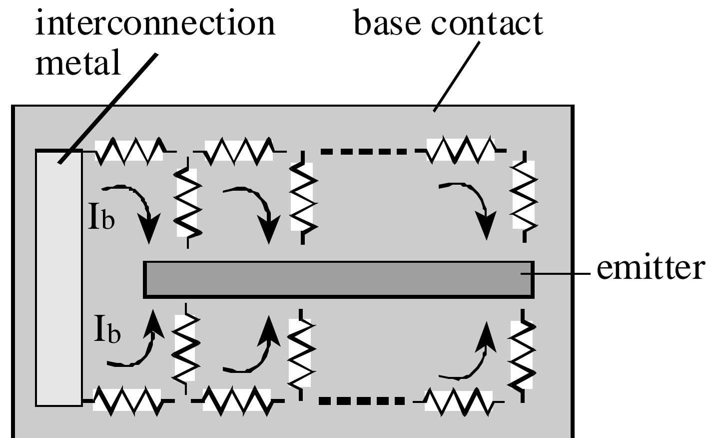


Figure 2.21: Base metal resistance and base current flow

In Figure 2.21, base current leaves the base contact metal and enters the base semiconductor in a region of one transfer length surrounding the emitter junction. Outside this region, the base current flows through the base metal primarily in a direction parallel to the emitter finger, producing a voltage drop along that path. The

voltage drop caused by the parasitic resistances produces a non-uniform base-emitter junction bias, V_B(x) that is shown in Figure 2.22, where x is the direction parallel to the emitter stripe.

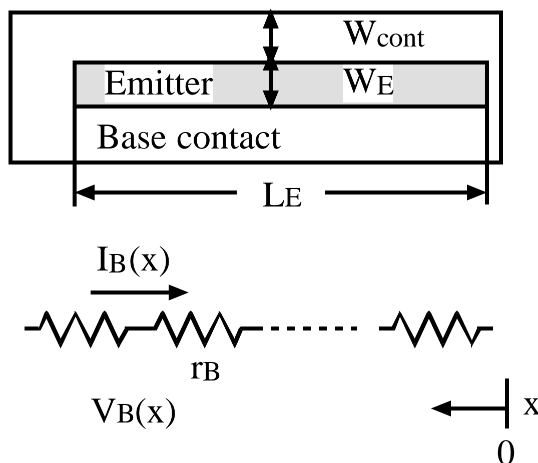


Figure 2.22: Voltage distributions along base contact stripe

In Figure 2.22, W_{cont} is the lateral width of base contact metal on either side of the emitter. The emitter length and width are L_E and W_E. When the transistor is operating at current density J_e and the base contact metal has a sheet resistance ρ_m, if x=0 is set at the end of the emitter away from the base contact, then the base current is

$$I_B(x) = \frac{J_e \cdot W_E \cdot x}{\beta} \quad . \tag{2.56}$$

β is current gain. The resistance per unit length of base metal is

$$r_B = \frac{\rho_m}{2W_{cont}} \cdot dx \quad . \tag{2.57}$$

Therefore, we have:

$$dV_B(x) = I_B(x) r_B = \frac{J_e \cdot W_E \cdot x}{\beta} \cdot \frac{\rho_m}{2W_{cont}} \cdot dx \quad . \tag{2.58}$$

By integrating Eqn. 2.58 from x=0 to x=L_E, we have:

$$\Delta V = \frac{L_e W_e J}{\beta} \cdot \frac{L_e \rho_m}{2W_{cont}} \cdot \frac{1}{2} = I_b \cdot \frac{R_{end-end}}{2} \quad . \tag{2.59}$$

Hence, the effective base resistance is 1/2 the end-end resistance $R_{end-end}$=($L_e\rho_m$)/($2W_{cont}$), given that the base current is distributed along the base metal stripe.

This voltage drop will induce a variation in current density along the emitter finger:

$$\Delta J_e = \Delta V \frac{g_m}{A_e} = \frac{\Delta V}{(kT/qJ_e) + (R_e A_e)} \quad . \tag{2.60}$$

To ensure that the current density variation ($\Delta J_e/J_e$) along the finger is below 20%, the emitter length must be:

$$L_E^{\ 2} \le 20\% \cdot \frac{(kT/qJ_e)+(R_e A_e)}{\dfrac{W_e}{\boldsymbol{b}} \cdot \dfrac{\boldsymbol{r}_m}{4W_{cont}}} \quad . \tag{2.61}$$

For an HBT with J_e=1 mA/μm^2, W_E=1 μm, ρ_m=0.3 Ω, W_{cont}=2 μm, $R_e A_e$=20 Ω–μm^2 and β=30, L_E must be smaller than 37 μm to make the maximum current variation along emitter below 20%.

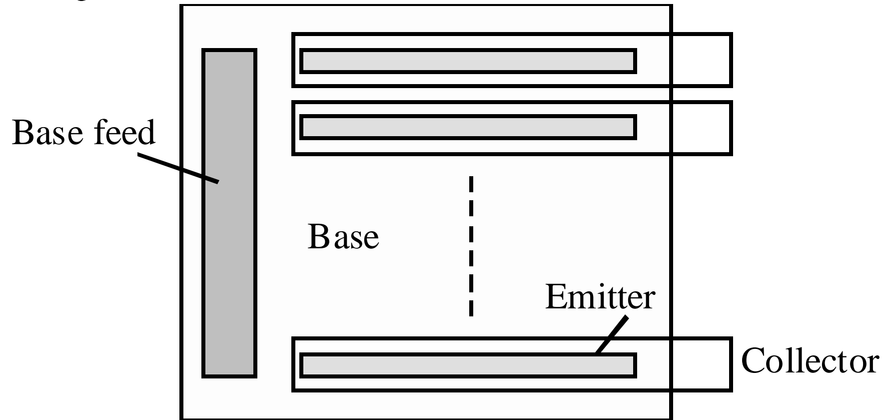


Figure 2.23: Layout of multiple finger transferred substrate DHBT

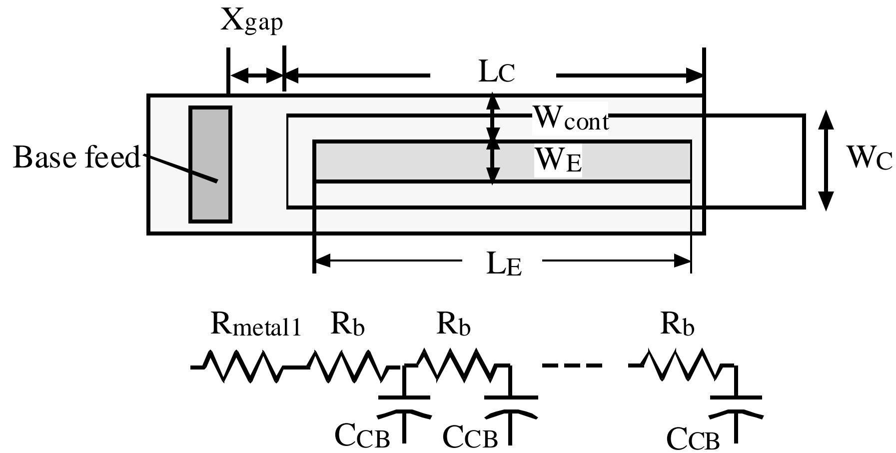


Figure 2.24: Base RC network with multiple finger DHBT

In addition to producing a non-uniform DC current distribution, the base metal also degrades the transistor bandwidth.

Figure 2.23 shows the layout of a multiple finger DHBT in transferred substrate technology. For each finger, the distributed RC network is sketched in Figure 2.24:

In Figure 2.24, the resistance in the gap between the feed and the base is

$$R_{metal1} = \boldsymbol{r}_m X_{gap} / (W_E + 2W_{cont}) \quad . \tag{2.62}$$

The end-end metal resistance in the emitter region is $R_{end\text{-}end}=(L_e\rho_m)/(2W_{cont})$. As with other base-collector problems, this RC network is distributed, and the lumped-element fit to first order in frequency consists of an added effective base resistance of $R_{basemetal} = R_{metal1} + R_{end-end}/3$. The power gain cutoff frequency is:

$$f_{\max} = \sqrt{\frac{f_t}{8\pi\tau_{cb}}} \quad ,$$

$$\tau_{cb} = R_{bb}C_{cb} \quad . \tag{2.63}$$

R_{bb} is the total base charging resistance, C_{cb} is the base-collector parasitic capacitance and τ_{cb} is the RC charging time. Given Eqn. 2.2, R_{bb} in Eqn. 2.63 is:

$$R_{bb} = R_{bb0} + R_{basemetal} \quad . \tag{2.64}$$

The base charging time is now modified:

$$\tau_{cb} = \tau_{cb0} + R_{basemetal}\left(\epsilon W_c L_c / T_c\right) \ ,$$

$$\tau_{cb0} = R_{bb0}C_{cb} \quad . \tag{2.65}$$

τ_{cb0} can be determined approximately from Eqn. 2.3. Since L_C is approximately equal to L_E, τ_{cb0} does not vary significantly with L_E. Therefore, the increase of base charging time $\Delta\tau_{cb}$ due to the increased L_E is:

$$\Delta\tau_{cb} = \rho_m\left(\frac{X_{gap}}{W_E + 2W_{cont}} + \frac{L_E}{2W_{cont}}\right)\left(\epsilon W_C L_E / T_c\right) \quad . \tag{2.66}$$

The above expressions are helpful to determine the maximum emitter length. For 25% f_{max} degradation, we must have:

$$\Delta\tau_{cb} = \rho_m\left(\frac{X_{gap}}{W_E + 2W_{cont}} + \frac{L_E}{2W_{cont}}\right)\left(\epsilon W_C L_E / T_c\right) \le 0.77\tau_{cb0} \quad . \tag{2.67}$$

For a transferred-substrate HBT with 3000Å InP collector, when W_E=1 μm, ρ_m=0.3 Ω, W_{cont}=2 μm, X_{gap}=6 μm, W_C=2 μm and $L_C \sim L_E$, an equation of the maximum L_E is derived from Eqn. 2.67:

$$0.25L_{E_\max}{}^2 + 1.2L_{E_\max} - 410 = 0 \quad . \tag{2.68}$$

From Eqn. 2.68, we determine that L_{E_max}=38 μm, coincidently consistent with that obtained from Eqn. 2.60.

In multiple finger HBTs, if the base feed contact is too narrow, additional base series resistance results from lateral current flow on the base metal, and again degrades bandwidth. This is illustrated in

Figure 2.25 (a). The base feed in multiple finger HBTs should use the layout of Figure 2.25 (b).

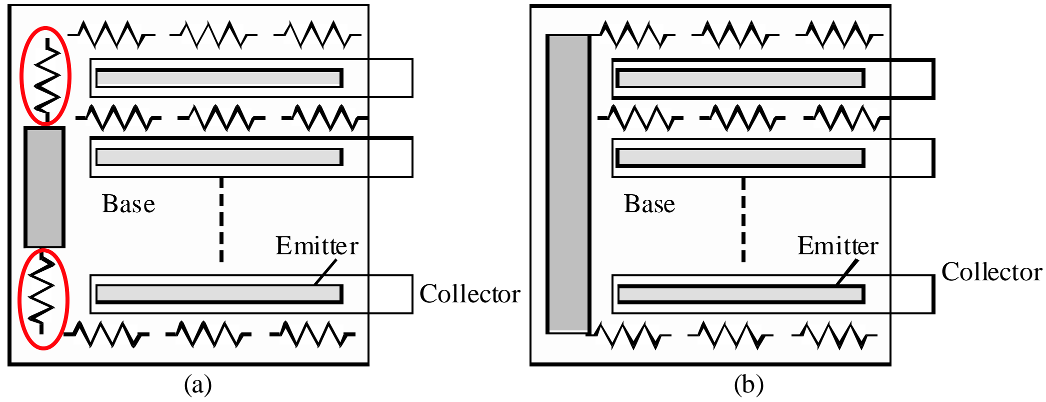


Figure 2.25: Layout of multiple finger transferred substrate DHBT. The grey shaded region is the base contact pad area.

2.8.4 Emitter resistance

As discussed in Section 2.1, emitter resistance increases the base-collector parasitic capacitance charging time. The small-signal maximum stable gain (MSG) (assuming a potentially unstable device) is given by $G_{ms} = \| S_{21}/S_{12} \| = \| Y_{21}/Y_{12} \|$ and at low frequencies, in common-emitter mode is $Y_{21} \approx (1/g_m + R_{ex} + R_{ballast})^{-1} = g_{m,extrinsic}$, while $Y_{12} \approx j\omega C_{cb}$. Adding emitter ballast resistance thus decreases the device extrinsic transconductance and therefore decreases the maximum stable power gain. Figure 2.26 is the hybrid-π model of a transferred substrate DHBT, whose emitter is 1 µm × 8 µm and collector is 2 µm × 10 µm. This model was extracted at I_c=7 mA and V_{ce}=2 V. While varying the emitter resistor R_e as 0, 8, 16 and 32 Ω, the maximum stable gain (MSG), unilateral Gain (U) and current gain (h21) are simulated. Figure 2.27 and Figure 2.28 are the simulation results from 75 GHz to 140 GHz with the device in common emitter and common base configurations respectively. The plots show a decrease of MSG/MAG more than 2 dB at R_e=32 Ω in both configurations. In contrast, the current gain and the unilateral power gain change little. A an accurate expression for f_{max} will be introduced in Section 3.7.1, which shows that R_e has little or no effect on the power gain and current gain cutoff frequencies.

Since power amplifiers do not operate under the conditions of small-signal output impedance matching, their power gains are significantly below the MSG and therefore, emitter ballast resistance must be carefully selected.

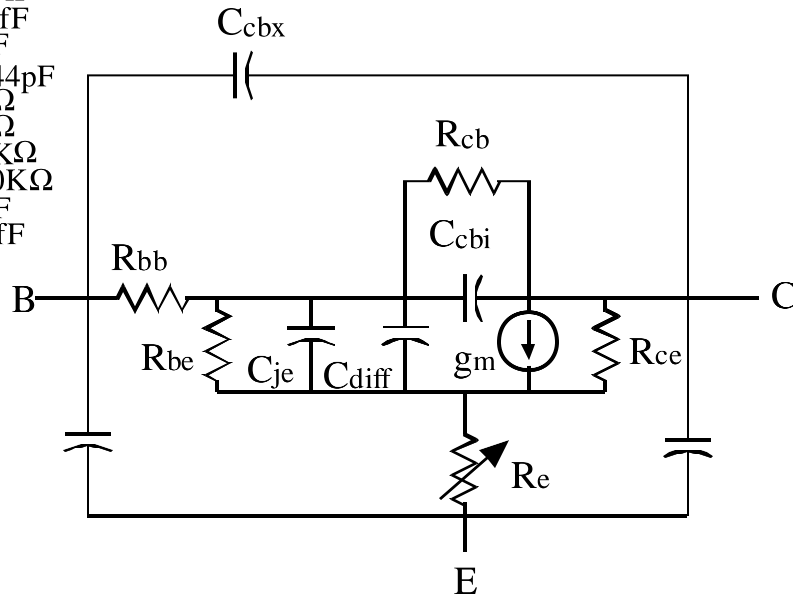


Figure 2.26: Hybrid-π model of transferred substrate DHBT with 1 μm × 8 μm emitter and 2 μm × 10 μm collector. (I_C=7 mA and V_{ce}=2 V)

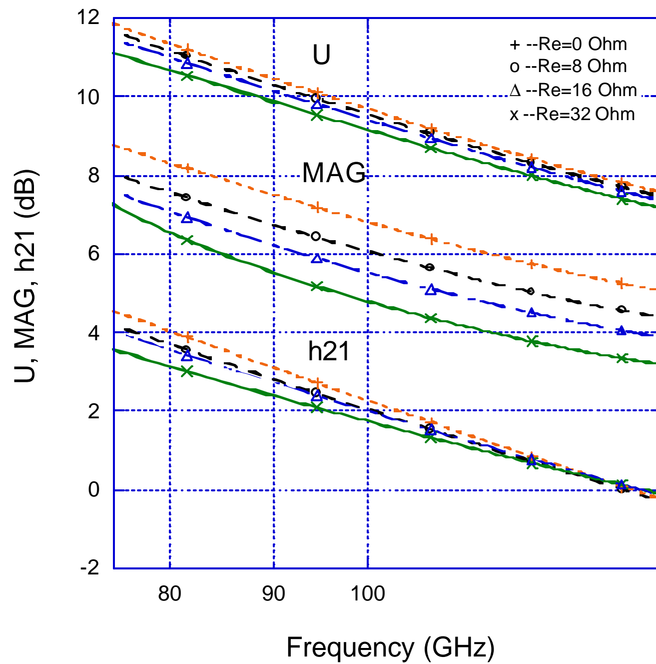


Figure 2.27 U, MAG and h21 simulations of the HBT model of Figure 2.26. in common base configuration

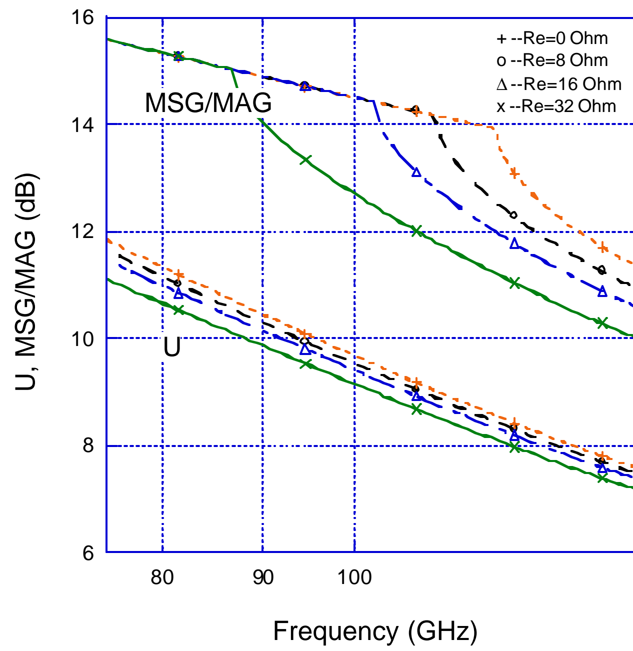


Figure 2.28: U, MAG and h21 simulations of the HBT model of Figure 2.26 in common base configuration

Chapter 3

Power HBT characterization

In Chapter 2, the thermal and electrical properties of power HBTs are introduced, which are important in determining the power and RF performance. In designing microwave integrated circuits, the first step is to develop a device model. A power HBT model must accurately simulate the DC properties, thermal effects, small-signal and large-signal RF characteristics. In this chapter, methods to characterize power HBT are given, with a concentration on the RF and thermal properties. A large signal model for multiple finger HBTs is developed in an effort to simulate both the electric and thermal characteristics.

3.1 HBT DC characteristics

The DC characteristics of power HBTs include current gain (β); base and collector ideality factors (η); breakdown voltages (BV_{ceo}, BV_{cbo}); collector leakage current (I_{cbo}); emitter, and collector resistances; offset voltage (V_{CE_offset}) and saturation voltage (V_{CE_sat}). By DC measurements (using an automated curve tracer), these characteristics can be obtained directly from the common-emitter characteristics, the Gummel characteristics, measurements of V_{CE}(sat) as a function of emitter current, and characteristics of the base-emitter and base-collector diodes. All these are fundamental characterization methods for bipolar transistors and will not be repeated here.

3.2 HBT small signal measurements and hybrid-π model extraction

The network analyzer is used to measure the small signal S-parameters of the HBTs. A set of S-parameters for an HBT under different bias conditions are necessary for the extraction of the device parasitics. The bias is applied through a highly inductive bias-tee so that the device sees only an AC open at the bias port. Specific frequency range ground-signal-ground (GSG) probes are selected to conduct the microwave signals from either coaxial cable or waveguide to the device under test (DUT). The system is calibrated before measurement using a set of known calibration standards. Wideband HBTs usually have very small C_{cb}, and hence small $Y_{12} \approx -j\omega C_{cb}$. If probe pads are placed close to the DUT input and output, the capacitive coupling between the probe tips is significant and causes significant measure errors. To obtain more accurate measurements, therefore, the probe

separation is increased by inserting a length of 230 μm 50Ω transmission line between the probe pad and the DUT. This transmission line is included in the on-wafer line-reflect-line (LRL) calibration standards (Figure 3.1) and therefore, its characteristics are corrected after the calibration.

In the LRL calibration procedure, the measurements are calibrated with reference to the characteristic impedance of the long line standard. This must therefore be known accurately. Significant factors impacting this line impedance include the presence of nearby Si_3N_4 dielectric layers, slope of the metal sidewalls reducing the effective conductor width, and the complex characteristic impedance resulting from the skin effect.

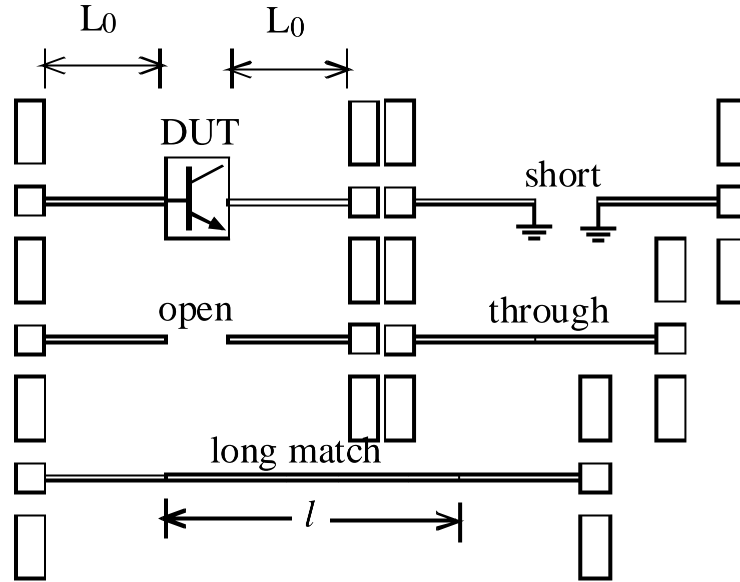


Figure 3.1: On-wafer LRL calibration patterns

Although the transistor T-model approximates the device physics more closely, the hybrid-π model is more readily extracted from the measurement data, largely because, as a parallel network with only a limited number of series elements, the individual model elements can be closely associated with the real and imaginary parts of the four admittance parameters.

Figure 3.2 shows an HBT small signal hybrid-π model that is sufficient to simulate the S-parameters of the device. The base resistance consists of base contact resistance, spreading resistance and gap resistance. The base sheet resistance and specific contact resistance can be obtained by on-wafer TLM measurements. Therefore, using Eqn. 2.4, the base resistance, R_{bb}, can be calculated. Base emitter resistance, R_{be} is equals β/g_m, where g_m is the transconductance. From the hybrid-π model, Y_{21} at low frequency is expressed as:

$$Y_{21} = (R_{ex} + \frac{1}{g_m})^{-1} \cdot \frac{\beta(R_{ex} + 1/g_m)}{R_{bb} + \beta(R_{ex} + 1/g_m)} = (R_{ex} + \frac{R_{bb}}{\beta} + \frac{\eta kT}{qI_E})^{-1} \quad . \tag{3.1}$$

R_{ex} is the emitter resistance, and I_E is the emitter current. The current gain β and ideality factor η can be obtained from the DC measurement.

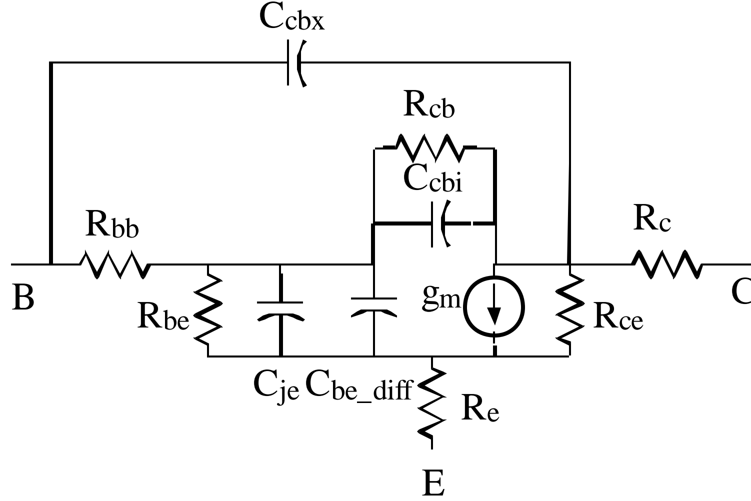


Figure 3.2: HBT small signal hybrid-π model

The emitter resistance R_{ex} can therefore be obtained by plotting the measured real part of Y_{21} versus I_E^{-1}. Note that unless the complex impedance corrections are applied to the S-parameter data, the low-frequency Y_{21} will be significantly in error, resulting in errors in the extracted R_{ex}. R_{ex} can also be extracted by the fly-back method (V_{CE_sat} vs. I_C)

Analysis of the network gives

$$Y_{12} \cong (1/R_{cb} + \omega^2 C_{cbi}^2 R_{bb}) + j\omega(C_{cbx} + C_{cbi}) \quad . \tag{3.2}$$

R_{cb} represents variation of collector-base leakage with bias, likely due to impact ionization; C_{cbi} and C_{cbx} are the intrinsic and extrinsic base-collector capacitance [14] respectively. By plotting the measured real and imaginary part of the admittance parameter Y_{12} versus frequency, R_{cb} and the total $C_{cb}= C_{cbi}+C_{cbx}$ can be extracted.

Transit times and C_{je} are now determined. Here we rewrite Eqn. 2.1:

$$\frac{1}{2\pi f_t} = \tau_b + \tau_c + \frac{kT}{qI_c}(C_{je} + C_{cb}) + (R_{ex} + R_c)C_{cb} \quad . \tag{3.3}$$

Using Eqn. 3.3 and plotting $1/2\pi f_t$ versus $1/I_C$ (f_t is obtained by a –20dB/decade extrapolation to 0 dB in the plot of H_{21} versus frequency), the sum of the total transit time, $\tau_b+\tau_c$, and $(R_{ex} + R_c)C_{cb}$ can be obtained from the infinite-current intercept. $C_{je} + C_{cb}$ can be obtained from the slope of the plot. Since R_{ex} and C_{cb} have already been determined, and assuming that R_C is negligible, $\tau_b+\tau_c$ and the base-emitter depletion capacitance C_{je} can be determined. This procedure assumes negligible variation of the transit times with current, a assumption which does not hold well at

very high current densities. In the hybrid-pi model, the base-emitter diffusion capacitance is given by $C_{be_diff} = g_m(\tau_b+\tau_c)$.

Being highly doped, the base has negligible width modulation. Thus, R_{ce} is very large and can be neglected.

Thus far, all the elements in the hybrid-π model have been determined except for the value of R_{bb} and the ratio of C_{cbi} to C_{cbx}. In the presence of negligible emitter resistance, and assuming that $C_{cb} << C_{je} + g_m(\tau_b + \tau_c)$ one can write

$$Y_{11} \approx j\omega(C_{cb} + C_{je} + g_m(\tau_b + \tau_c)) + \omega^2(C_{cb} + C_{je} + g_m(\tau_b + \tau_c))^2 R_{bb} + (R_{bb} + R_{be})^{-1}. \tag{3.4}$$

While a more complex expression can be written in the presence of nonzero emitter resistance, the resulting expression also involves the delay associated with the g_m element, and so becomes dependent upon an increasing number of unknowns. Instead, since R_{ex} is known, a resistance of value $-R_{ex}$ is first added in series with the emitter terminal of the measured 2-port parameters, and the Y-parameters of the composite network are computed. Then, Y_{11} is given in Eqn. (3.4), and R_{bb} is determined from the quadratic variation of $\mathrm{Re}\{Y_{11}\}$ with frequency. Eqn. 3.2 is then used to determine the partition between C_{cbi} and C_{cbx}.

The expressions above are approximate. This alters the details of the procedure but not the overall method. In each step above, a first estimate of the element value is found from the expression given. This is then entered into an equivalent circuit network, and the Y-parameters of the network computed and compared to the data, and the individual parameters are adjusted to obtain best fit to the *relevant* Y-parameter as identified in the expressions above.

3.3 HBT thermal effects

The power dissipation in HBTs is mainly in the base-collector junction where the sum of applied and built-in potentials is large. In InP mesa HBTs, the heat flows through an InGaAs sub-collector layer and then passes through the GaAs substrate. Thermal effect leads to reduced RF bandwidth because of both DC current gain collapse and premature Kirk effect. InGaAs has very poor thermal conductivity, and hence thick InGaAs layers must be avoided in the subcollector of power DHBTs.

Thermal effects can be directly observed in the DC common-emitter characteristics. The power dissipation $P_d = I_C \cdot V_{CE}$ increases with both emitter current and collector voltage. Figure 3.3 shows the DC common-emitter characteristics of an eight-finger HBT, which demonstrates a sudden reduction in the DC current gain as the collector voltage is increased. Above a critical value of V_{CE}, the current distribution becomes highly nonuniform, and the hottest fingers carry the entire full collector current. Those fingers are then biased at a current density above the Kirk threshold, resulting in current gain collapse, while the cooler fingers carry negligible current. This effect appears as a sharp drop in the collector current in the common-

emitter characteristics. The current collapse loci, which are formed by the current drop points, define the safe operation area (SOA) of an HBT.

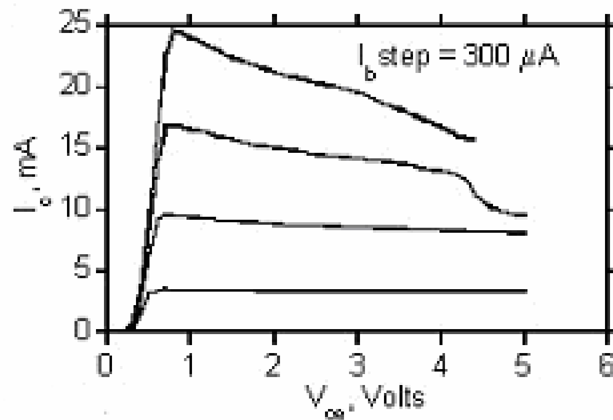


Figure 3.3: Current collapse arising from current distribution instability in a 4-finger DHBT with A_E=1 μm × 16 μm/finger

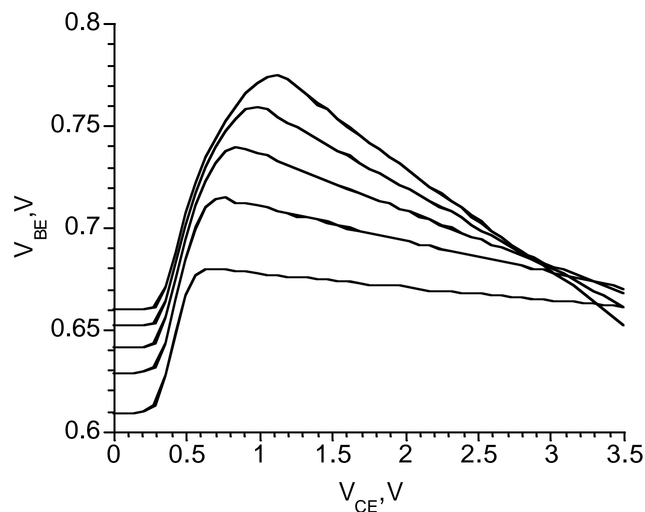


Figure 3.4: V_{be}-V_{ce} plot, for an HBT (β=25) with A_E=1 μm × 32 μm, taken at base current steps of 260 μA, with offset of 260 μA.

The thermal resistance of an HBT is determined by measuring V_{be} as a function of V_{ce} with a fixed I_C. This is shown in Figure 3.4. After the applied V_{CE} exceeds the saturation voltage, the base voltage curve decreases with increased V_{ce}. At higher collector bias currents, the effect becomes more pronounced. Increased V_{ce} results in increased power dissipation, causing a decrease in the base-emitter voltage required for a given collector current. In this specific plot, it can be seen the variation of V_{be} with device dissipation is 120 mV.

3.4 Self-heating thermal resistance

Power dissipation in HBTs results in a temperature rise within the device above the ambient temperature. The temperature rise introduces strong thermo-electric effects that degrade the HBT's DC and AC performance. Thermal resistance, R_{th}, describes the variation in junction temperature as a function of power dissipation, with $R_{th}(T_A) \equiv -\partial T / \partial P$ where P is the power dissipation and T_A is the ambient temperature. The junction temperature T_j with power dissipation P then can be expressed as:

$$T_j = T_A + R_{th} \cdot P = T_A + R_{th} \cdot (V_{ce} \cdot I_c) \quad , \tag{3.5}$$

V_{ce} and I_C are the collector bias voltage and current respectively. R_{th} is a function of the semiconductor layer structure, the device geometry, and the device emitter junction area (device size).

The literature describes several methods to determine R_{th}. Thermal resistance can be determined by calculation, using 2-demensinal or 3-dimensional analyses [35] [36]. While such calculations are valuable to develop understanding, they must be experimentally confirmed. Additionally, modeling does not include process-induced variations between the intended and actual device dimensions.

In very large devices, R_{th} can be obtained directly from a temperature measurement using an external temperature-measurement device, such as a thermal imaging system. In transistors, the junction dimensions are small (often smaller than an optical wavelength), and the junction temperature is substantially above the surface temperature, so such methods cannot be used. Since it is very difficult to directly measure the junction temperature with an external thermometer, the variation of transistor current gain and base-emitter voltage with temperature are instead usually employed as an experimental probe of the junction temperature.

As described in Chapter2, current gain decreases with increased junction temperature, arising from either increased power dissipation or increased ambient temperature. The HBT base current is composed of hole back-injection into the emitter, surface recombination current in the exposed extrinsic base region, interface recombination current at the base contact, bulk recombination current in the base region, and the space-charge recombination current in the base-emitter space-charge region. Among these components, the base hole back-injection current has strongest thermal dependence. If this current dominates the base current, then, from [37], the current gain of the HBT can be expressed as:

$$\boldsymbol{b}(T) = \boldsymbol{b}_0 \exp(\frac{q\Delta E}{kT_j}) \quad . \tag{3.6)?$$

ΔE is the difference between emitter and base bandgap energies.

In the more general case, where several mechanisms contribute to the base current, the variation of β with temperature has a more complex variation with temperature. For all sources of base current described above, $\boldsymbol{b}$ decreases with increased temperature. This results in a negative differential output resistance in the

common-emitter characteristics. Using data over a limited current range, reference [38] uses a linear fit to the variation of current gain with temperature:

$$\boldsymbol{b}(T_j) = \boldsymbol{b}_0 + \frac{\partial \boldsymbol{b}}{\partial T} T_j \quad . \tag{3.7}$$

Substituting Eqn. 3.5 into 3.6, the current gain at an ambient temperature T_A and power dissipation P can be written as:

$$\boldsymbol{b}(T_A, P) = \boldsymbol{b}_0 + \frac{\partial \boldsymbol{b}}{\partial T} \cdot T_A + \frac{\partial \boldsymbol{b}}{\partial T} \cdot R_{th} \cdot P = \boldsymbol{b}_0 + \boldsymbol{q} \cdot T_A + \boldsymbol{q} \cdot R_{th} \cdot P \quad . \tag{3.8}$$

In Eqn. 3.8, $\theta = \partial\beta/\partial T$ is determined by measuring the variation of β at constant power dissipation P_0 while varying the ambient temperature T_A. This can be done by performing measurements with the transistor placed on a hot-plate. Then, by measuring β versus power dissipation at a constant ambient temperature T_A, R_{th} can be determined:

$$R_{th} = \frac{\partial \boldsymbol{b} / \partial P}{\boldsymbol{q}} \quad . \tag{3.9}$$

The variation of $\boldsymbol{b}$ with temperature can now be included in the device simulation model. At constant base current (I_{B0}) and fixed ambient temperature (T_0), the collector current can be derived as followed:

$$I_C = I_{B0} \boldsymbol{b}(T_j) = I_{B0}[\boldsymbol{b}_0 + \boldsymbol{q} \cdot R_{th} \cdot P] = \boldsymbol{b}_0 \left[I_{B0} + \frac{I_{B0}}{\boldsymbol{b}_0} \cdot \boldsymbol{q} \cdot R_{th} P \right] \quad . \tag{3.10}$$

Since θ is negative, this can be reorganized to represent the collector current change through self-heating as an effective reduction of magnitude $I_{B0}\boldsymbol{b}_0\boldsymbol{q} \cdot R_{th}P$ in the base current, with current gain unchanged. Eqn. 3.10 provides a means of modeling self-heating using the Gummel-Poon model that is available in typical EDA tools. Figure 3.5 shows the schematic of such a model. The base current change is simulated as a base leakage current by a voltage controlled current source. The control voltage is the product of the instantaneous external base current I_{b0} and the power dissipation P, averaged over the period of one thermal time constant. The transconductance is $\boldsymbol{q}R_{th}/\boldsymbol{b}_0$. Figure 3.6 demonstrates the DC common-emitter characteristics of the simulation. This method will be used in the HBT large signal model that will be addressed in Section 3.7.2.

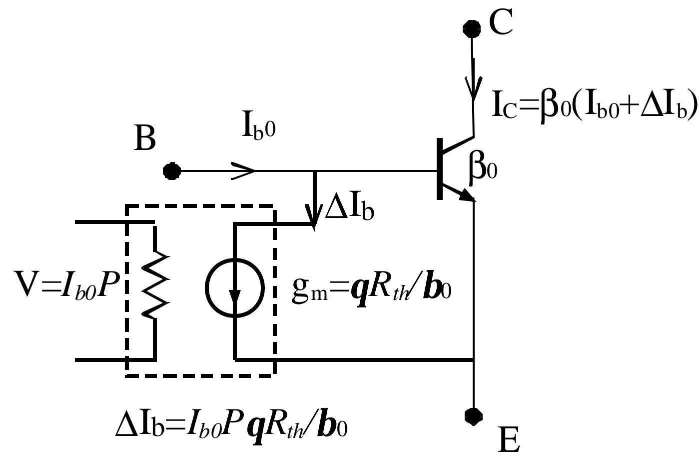


Figure 3.5: DHBT self-heating simulation schematic

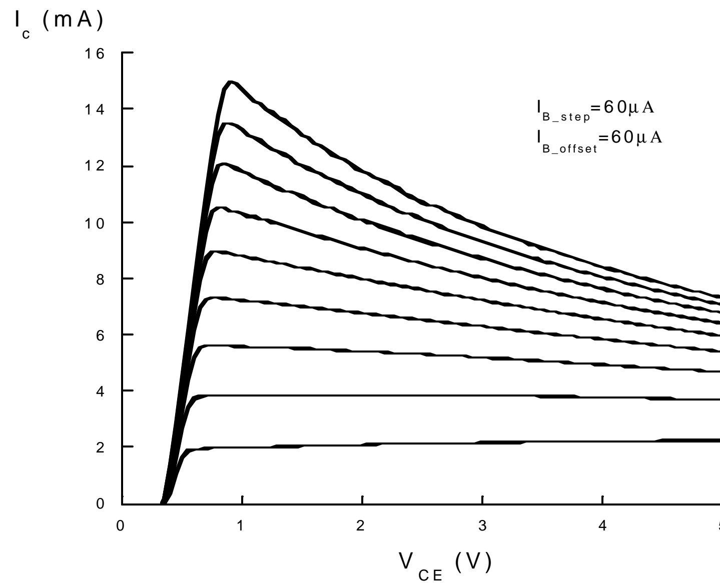


Figure 3.6: DC common-emitter characteristics of the self-heating HBT model.

The second method measurement of R_{th} involves measuring the base-emitter voltage. From chapter2, the rate of variation of base-emitter voltage with temperature is $\Phi = -\partial V_{be} / \partial T$, a factor dependent on the base semiconductor and the bias current density. Φ can be determined by calculation (Eqn. 2.16), or by biasing the transistor at constant collector current, varying its temperature by placing it on an adjustable hot-plate, and measuring (Eqn. 2.17) the resulting variation in V_{be}. Given Φ, under conditions of fixed collector current, the junction temperature rise can be

calculated by $\Delta T_j = \Delta V_{be}/\Phi$, where ΔV_{be} is the variation of base-emitter voltage. From Eqn. 3.4, since the change in junction temperature is:

$$\Delta T_j = R_{th} \cdot \Delta P \quad . \tag{3.11}$$

R_{th} can then be determined by:

$$R_{th} = \frac{\Delta T_j}{\Delta P} = \frac{\Delta V_{be}/\Phi}{\Delta P} \quad . \tag{3.12}$$

This measurement is shown in Figure 3.7. I_C is measured as a function of V_{be} at a series of collector bias voltages. In Figure 3.7, I_C curves are plotted with V_{CE} of 1, 2, 3, and 4 volts. Examining the curves for V_{CE}=3 V and V_{CE}=4 V at a fixed I_C=4 mA, the change in device dissipation is 4 mW, while V_{be} has changed by 16 mV. The junction temperature rise is therefore 16 mV/(0.98 mV/^{o}C)=16 ^{o}C, hence the device thermal resistance is R_{th}=16 ^{o}C/4 mW=4 ^{o}C/mW.

The plot (Figure 3.7) provides a graphical illustration of thermal instability. The point of infinite slope corresponds to an infinite rate of change of I_C with V_{be}. It can be seen that as the collector bias voltage increases, thermal instability is reached at reduced collector current.

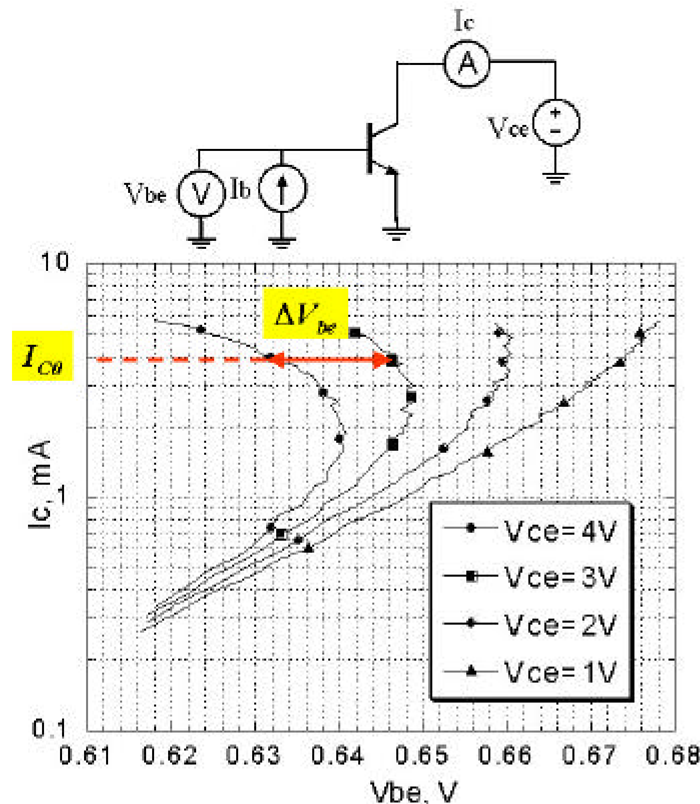


Figure 3.7: Circuit schematic and experimental data of thermal resistance

Thus far, the discussion on thermal resistance measurement has assumed (Eqn. 3.4) a linear relationship between the junction temperature and the power dissipation.

Variation of thermal resistance with temperature has been neglected. To a better approximation, the junction temperature will also show a quadratic variation with power dissipation, arising from the variation of thermal conductivity with temperature [18]:

$$T_j = T_A + R_{th} \cdot P + R_{th}^{'} \cdot P^2 \quad . \tag{3.13}$$

The method of Figure 3.7 can still be applied in this more general case; the variation of V_{be} with V_{CE} at fixed I_C still provides a measurement of junction temperature rise as a function of device power dissipation. The junction temperature rise is simply no longer a linear function of the device dissipation.

3.5 Coupling thermal resistance and current hogging loci

Power HBTs usually have multiple emitter fingers where by design intent each finger should carry the same current. According to the analysis of thermo-electric effects in multiple finger HBTs in Chapter 2, thermal coupling can introduce differential modes of current distribution among fingers and therefore, current hogging can occur. We generalize the definition of thermal resistance for a transistor with multiple emitter fingers:

$$R_{th_ij} = \frac{\partial T_i}{\partial P_j} \quad . \tag{3.14}$$

R_{th_ij} is the coupling thermal resistance of dissipation in the jth finger resulting in heating of the ith finger. For $i=j$, R_{th_ii} refers to the self-heating thermal resistance of a single finger.

From the discussion in Section 2.6.2, when differential mode involved, the eigenvalue (λ) of the current variation vector in a multiple finger HBT determines the hogging current (I_h) at a certain V_{CE}:

$$I_h = \frac{\dfrac{\mathbf{h} k T_A}{q}}{\left|\Phi\right| V_{ce} \mathbf{l} - (R_E + \dfrac{R_B}{\mathbf{b}})} \quad . \tag{3.15}$$

Below I_h, current hogging will not occur. Instability in multiple finger HBTs will arise first in that differential mode which has the smallest hogging current (I_{h_min}) and therefore, I_{h_min} and the corresponding V_{CE} define the safe operating area for multiple finger HBTs.

The role of ballast resistance can also be seen in Eqn. 2.22. Eqn. 3.15 is obtained assuming each finger has its own ballast resistance. This is termed distributed ballast resistance. By using Eqn. 3.15, ballast resistance to be used to suppress a differential mode, can be expressed as:

$$R_E = \left|\Phi\right| V_{ce} \mathbf{l} - \frac{\mathbf{h} k T_A}{q I_h} - \frac{R_B}{\mathbf{b}} \tag{3.16}$$

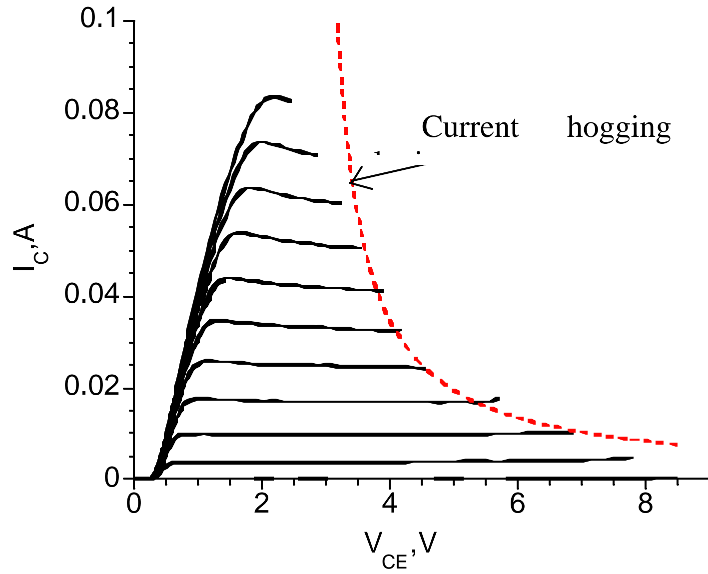


Figure 3.8: Current hogging loci on I-V plot

In Figure 3.8, the hyperbolic hogging current loci, calculated from Eqn. 2.47 for a 4-finger transferred substrate InP DHBT with dimensions of A_E=1 μm × 24 μm/finger, are plotted with its I-V curve. The calculated results are accurate in predicting current hogging loci.

Self-heating and coupling thermal resistances in a multi-finger transistor can be measured in a method similar to that used to measure self heating. The test circuit schematic is shown in Figure 3.9.

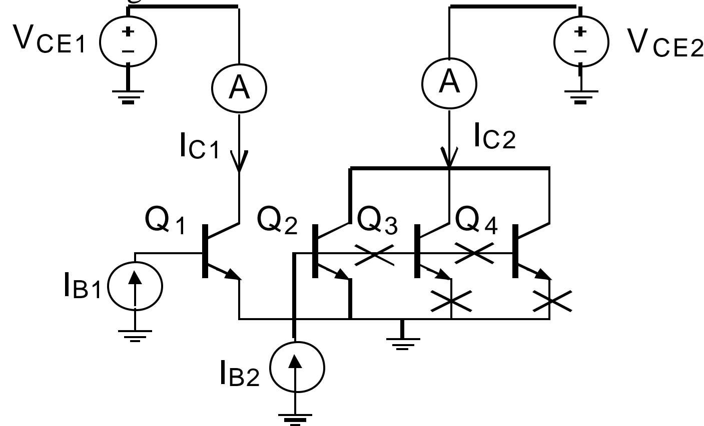


Figure 3.9: Schematic of multiple finger HBT thermal resistance measurement. The X marks denote open connections.

In Figure 3.9, the transistor fingers Q_1 and Q_2 can be biased and monitored separately. Q3 and Q4 are physically present but unbiased, so as to ensure that the thermal coefficients remain representative of a 4-finger device. V_{be1} is plotted as a

function of I_{C1}. Varying V_{CE1} during this measurement causes a change in power dissipation in Q1, and hence self-heating of Q1. This causes a measurable variation in V_{be1} at fixed I_{C1} as V_{CE1} is changed, from which the device self thermal resistance is determined. Varying V_{CE2} during this measurement changes the dissipation in Q2, and hence causes some degree of heating of Q1. Varying V_{CE2} also adds a measurable variation in V_{be1} as well as that caused by self-heating and from which, the device thermal coupling (also called mutual thermal resistance) is determined.

The devices Q_3 and Q_4 are open-circuited at their bases and emitters while their collectors are connected in common with Q_2. In this way, the thermal effects on Q_3 and Q_4 as heat sinks of Q_1 are maintained without the devices being electrically biased.

Figure 3.10 consists of three sets of curves of I_C vs. V_{be} for Q_1. To measure the self-heating thermal resistance, the collector bias, V_{CE1} is varied from 1 V to 3 V in 1V steps, with V_{CE2} maintained at a constant value. The three groups of curves are measured under three collector biases, V_{CE2} of Q_2, of 1, 2, and 3V and at a constant collector current I_{C2}=10 mA. Q_1's self thermal resistance can be extracted from Figure 3.10 (b) when Q_2 is biased at V_{CE2}=1V and I_{C2}=10 mA. The self thermal resistance is:

$$R_{th_11} = \frac{\Delta V_{be_self}}{|\Phi|\Delta V_{ce1} I_{C1}} \quad . \tag{3.17}$$

The coupling thermal resistance is obtained from Figure 3.10 (c), where the collector bias voltage of Q_1 and the collector current of Q_2 are held constant at V_{CE1}=3V and I_{C2}=10 mA, respectively. V_{CE2} is increased from 1 V to 3 V. The coupling thermal resistance R_{th_12} determines the junction temperature rise of Q_1 by the power dissipation variation of Q_2 that is $\Delta P2=I_{C2}\Delta V_{ce2}$. Therefore:

$$R_{th_12} = \frac{\Delta V_{be_coup}}{|\Phi|\Delta V_{ce2} I_{C2}} \quad . \tag{3.18}$$

By plotting the variation of V_{be2} versus the bias in Q1 and Q2 in the same way, the self-thermal resistance of Q_2, R_{th_22}, and coupling thermal resistance, R_{th_21}, from Q_1 can also be obtained.

The other thermal resistances can be determined by the same procedure for multiple finger devices with different topologies. Figure 3.11 gives another test structure for a 4-finger HBT. Thermal coupling is strongly dependent on spacing and empirically, coupling thermal resistances between fingers with the same spacing are almost the same, for example, $R_{th_ij}=R_{th_(i+1)(j+1)}$. Also due to the symmetry in the topology, the ith finger is identical to the $(5-i)^{th}$ finger and hence so are the associated thermal resistances.

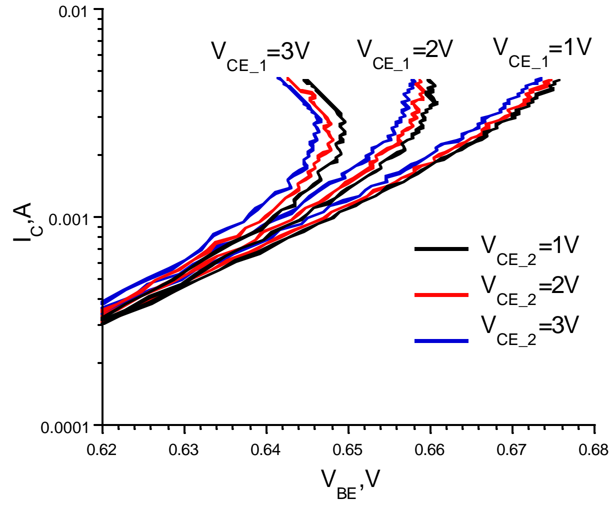


Figure 3.10 (a): Multiple finger thermal resistance measurement plot.

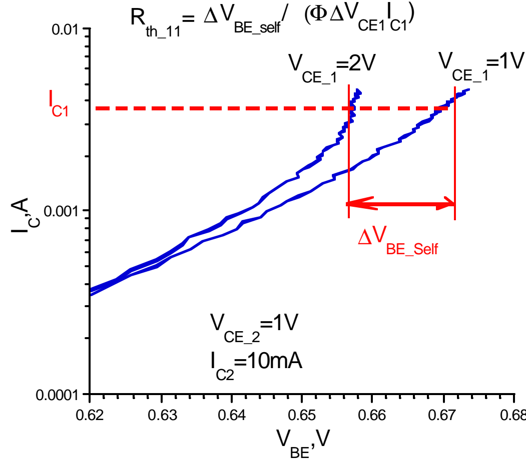


Figure 3.10 (b): Self-heating measurement plot-R_{th_11}

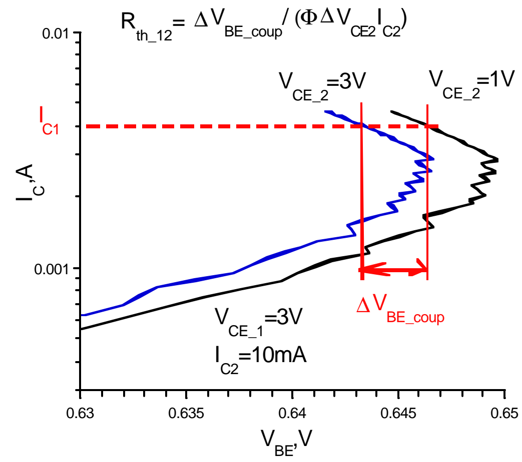


Figure 3.10 (c):Thermal-coupling measurement plot-R_{th_12}

From **Error! Reference source not found.**, R_{th_33}, R_{th_31} and R_{th_13} can be obtained. The thermal resistances of Q_4 and Q3 are the same as that of Q_1 and Q2 due to the device symmetry.

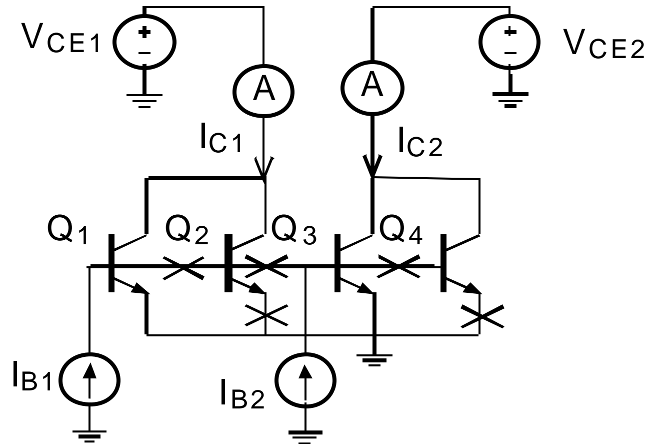


Figure 3.11: Another thermal resistance measurement circuit for 4-finger HBT

3.6 Thermal time constant

In the previous discussions, the thermo-electric analysis was in DC steady state. Since the device temperature does not change instantaneously with the power dissipation, the thermal time response of the HBT also needs to be characterized.

A thermal time constant $\tau_{thermal}$ is used to characterize the thermal time response in power HBTs and it is usually obtained using a pulse measurement. When a pulsed voltage is applied to the base, the base current encounters a sharp initial rise, followed by a slowly increasing component associated with the device heating. For the case of a transistor with negligible variation of current gain with temperature, the collector current with show a similar transient behavior.

For transistors with a strong negative temperature coefficient in $\boldsymbol{b}$, under a step-function pulsed base current drive, the collector current will show an initial step increase, followed by an exponential decay from its maximum to its steady state value. This is consistent with the device thermal effects. Initially, the device is cool and the current gain is at a maximum. As the device is biased, junction temperature gradually increases resulting in gain reduction.

In either of the two cases above, the time required for the collector current to become stable is called the thermal time constant.

The thermal time constant introduces a pole-zero pair in the transistors gain-frequency characteristics. At frequencies near $1/\tau_{thermal}$, the junction temperature variation is able to *follow* the instant power dissipation in of the device, leading to harmonic thermo-electric feedback. As a function of the dominant thermal mechanism (current gain or V_{be} variation), this results in either increased or decreased power gain at lower frequencies. Measurement of device gain at low frequencies thus provides a method to estimate the thermal time constant.

Typically, for InP DHBTs with junction areas of a few square micrometers, $\tau_{thermal}$ is at the order of ~1μs. For power amplifiers operating in RF and microwave frequency, this thermal time constant has no influence.

3.7 HBT modeling

Power HBTs are usually characterized using a load-pull system. These provide the input and load impedance required for maximum saturated output power, the power added efficiency, linearity, and output power as a function of bias. With such data, power amplifiers can be designed. A RF load-pull system is composed of a network analyzer, a high power signal source, a power meter, an electromechanical load impedance tuner, and the software operating system.

A load-pull system can also be used to verify an HBT's large signal model. Power amplifier design requires an accurate model describing the power performance of the device at the working frequency. The large signal model also provides insight into the device physics, which is helpful in generating device innovations.

3.7.1 Large signal modeling based on S-parameter extraction and finite element model

Large signal models of HBT have been reported in the literature [13] [39] [40] [12]. Some of these include self-heating effects. In contrast, we have developed a thermal model which is based upon addition of electrical parasitics and thermal characteristics to the Gummel-Poon large model within SPICE. It can therefore be used within an Agilent's ADS microwave circuit simulation program, or similar software.

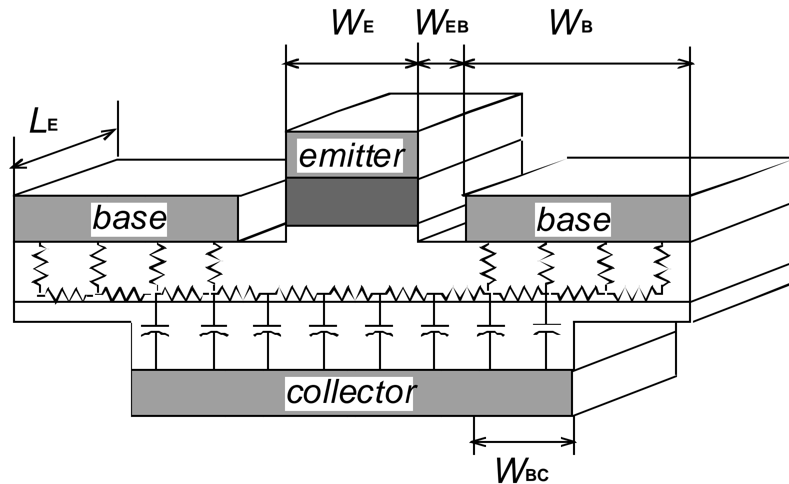


Figure 3.12: Distributed model of transferred-substrate HBT

The S-parameter extraction technique was presented in Section 3.2, in which the HBT parasitic elements are determined from the small signal S-parameter measurements. This model has been successfully applied to the small signal

modeling of transferred-substrate HBTs [5] [15]. Figure 3.12 shows a modified] finite element model of the base-collector junction [14] of transferred-substrate HBTs. This model draws strongly from the work of Vaidyanathan and Pulfrey [41] and hence we refer to it as the VP model. Figure 3.13 shows its equivalent circuit. The VP model allows an accurate circuit simulation model to be developed from the underlying physical transistor parameters. Thus, unlike models derived exclusively from S-parameter models, circuit simulations of reasonable accuracy can be performed as a function of variable device geometry, including geometries of devices not yet fabricated and measured. In this work, models based on both S-parameter extraction and finite-element analysis are both employed. The 2 models are compared to confirm model assumptions.

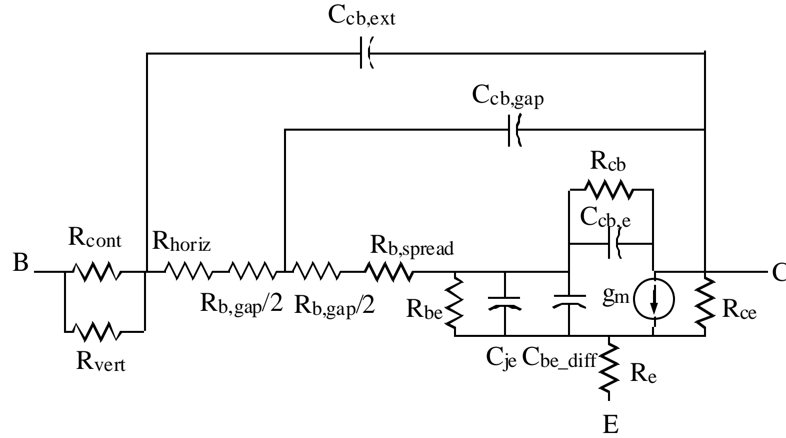


Figure 3.13: Distributed hybrid-π model of transferred-substrate HBT

In a VP model, in addition to the base resistances defined in Chapter 2, under the base contact, a vertical contact resistance is defined as $R_{vert}=\mathbf{r}_c/2W_{bc}L_e$ and a lateral contact resistance is $R_{horiz}=\mathbf{r}_sW_{bc}/2L_e$. Three distributed base-collector capacitances are also defined in this model. $C_{cb,e}=\mathbf{e}L_eW_e/T_c$ is the junction capacitance lying under the emitter, $C_{cb,gap}=2\mathbf{e}L_eW_{eb}/T_c$ is the capacitance under the gap region between base and emitter contact: $C_{cb,cont}=2\mathbf{e}L_eW_{cb}/T_c$ is the capacitance under the base contact.

Using this model, the total base-collector charge time is [41] [14]:

$$\mathbf{t}_{cb} = C_{cb,e}(R_{b,cont} + R_{gap} + R_{spread}) + C_{cb,gap}(R_{b,cont} + R_{gap}/2) + C_{cb,ext}(R_{b,vert} \| R_{vert})\ . \quad (3.19)?$$

The large signal model is produced by replacing the voltage controlled current source in the hybrid-pi model of Figure 3.13 with the Gummel-Poon model, as shown in Figure 3.14.

Comparing Figures 3.13 and 3.14, R_{be}, C_{je}, C_{be_diff} and R_{ce} are included as elements within the Gummel-Poon model as this correctly represents their variation as a function of device bias. In contrast, all elements in the base-collector junction, together with the emitter resistance, are represented externally. In this manner, a more complex model of these elements is possible than is provided in the Gummel-

Poon model. The base-collector parasitic parameters in the Gummel-Poon model are therefore set to zero. Procedures for determining the DC parameters were discussed in Section 3.1.

The main limitation of this model is that it does not account for the thermal effects, nor does the Gummel Poon model correctly model the Kirk effect or current-dependent breakdown. Addition of elements to model thermal effects will be discussed in the next section. For power amplifiers, the safe operating area is primarily determined by thermal stability. With Kirk effect not modeled, the designer must ensure by hand calculations that the device does not experience a combination of I_C and V_{CE} which would cause this, either under bias or under signal conditions.

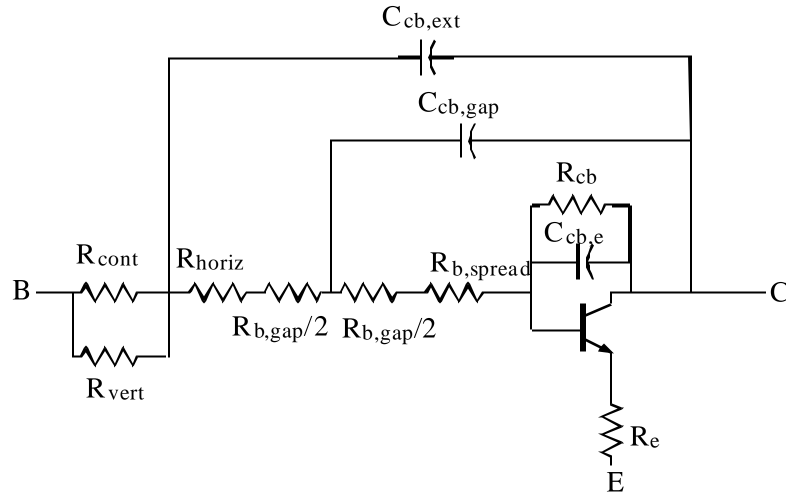


Figure 3.14: Large-signal model of transferred-substrate HBT

3.7.2 Device large-signal model with thermal effects

As discussed in the previous sections, when an HBT dissipates high power, the device temperature is increased. This results in a series of thermal effects which can degrade the device performance. The model of section 3.7.1 uses a standard Gummel-Poon model available in both ADS and most other circuit simulation programs. The Gummel-Poon model itself has no thermal parameters. To amend this shortcoming, a large signal model with thermal feedback is developed and is shown in Figure 3.15.

In the large signal model in Figure 3.15, two equation based non-linear components are inserted. The two inputs of the first component are the sensed collector current, I_C, and the collector-emitter bias, V_{ce}. These are measured by the indicated ammeter and voltmeter. The output current is $I_p = I_C V_{ce}$. This current then charges the thermal sub-circuit with $C_{th}=\tau_{thermal}/R_{th}$, where R_{th} is the measured self-thermal resistance. The thermal time constant is thereby measured. The port voltage, V_{th}, is then proportional to the device temperature deviation resulting from the transistor power dissipation. By using the second equation-based component, the

variation in base-emitter voltage at fixed I_C, $\Delta V_{be}(T)$ is calculated (Eqn. 3.14) and is fed back to the base-emitter junction by a voltage-controlled-voltage source. As temperature rises, both the base recombination and back injection rates increase, resulting in a reduction of current gain. This mechanism is simulated using $\Delta \boldsymbol{I}_b\ (T) = I_{B0}\boldsymbol{b}_0\boldsymbol{q} \cdot R_{th}P$ in Figure 3.15.

For a multiple finger device, by adding more equation-based components to the model, the thermal coupling effects can be simulated. Figure 3.16 shows the schematic of a 2-finger HBT modeling with the equivalent circuit of finger 1 (Q1). In addition to the self-heating calculation, the current I_{p2} represents (is proportional to) to the instant power dissipation in finger 2 (Q2). I_{p2} charges the thermal sub-circuit and produces a port voltage V_{th12}, which is proportional to and represents the junction temperature rise of Q1 due to the thermal coupling from Q2. V_{th12} and V_{th11} are then used to determine the base voltage regression ($\Delta V_{be1}(T)$) and current gain reduction ($\Delta I_{b1}(T)$) of Q1.

As shown in Figure 3.15 and Figure 3.166, the thermal effects of the HBT are included into the large signal model by electrical feedback elements. No subroutine programming is needed. Nodal equations for this network can be written easily, and no harmonic procedure is involved for the circuit simulation. The networks have never given difficulties with numerical convergence.

Comparisons of the large signal model with the measurements in both DC and RF will be given in the next chapter.

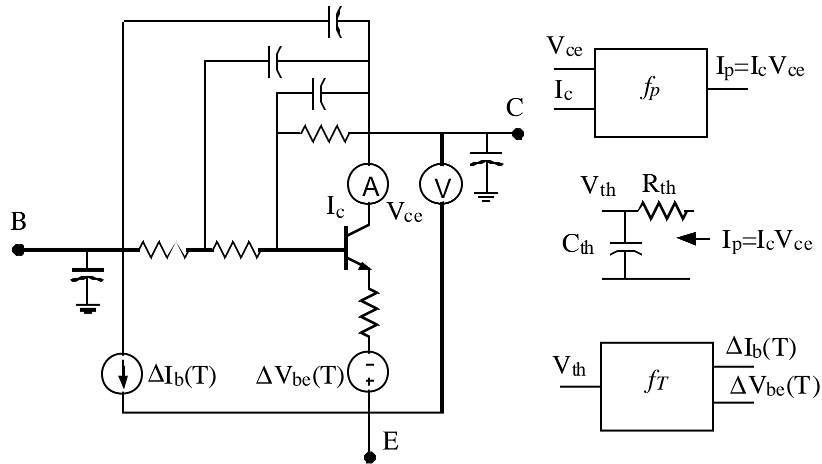


Figure 3.15: Thermal feedback HBT large signal model

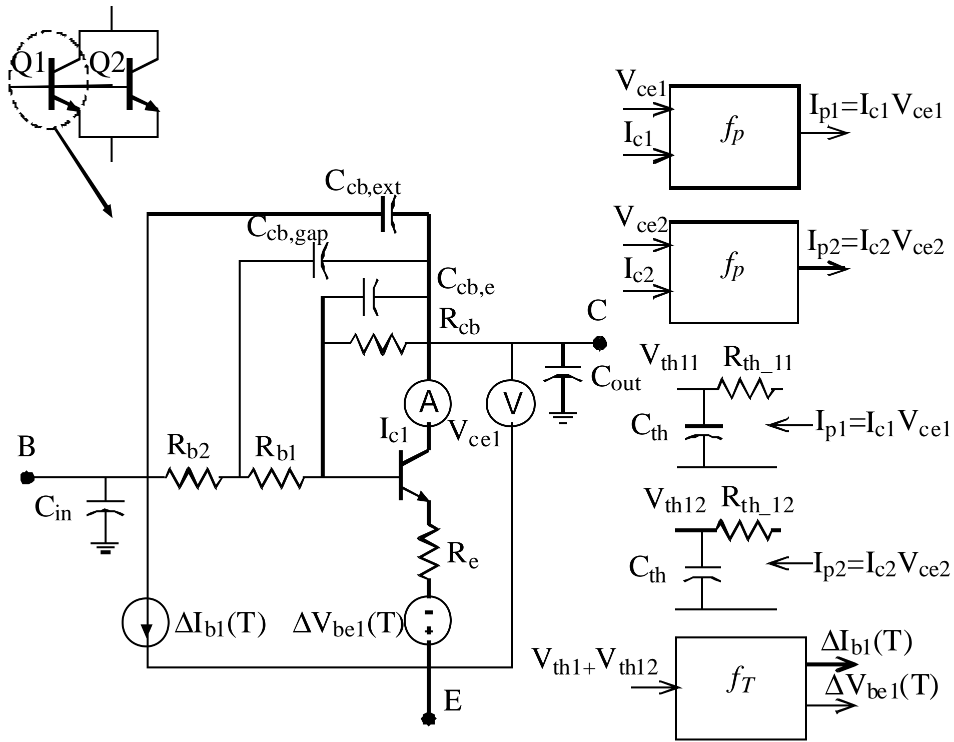


Figure 3.16: Schematic of large signal model of finger 1 in a 2-finger HBT

Chapter 4

Power DHBTs in transferred substrate technology

Single-heterojunction transferred-substrate HBTs with InGaAs collectors have demonstrated very high power gain cutoff frequencies [5]. However, these devices suffer from the low thermal conductivity and low breakdown voltage (BV_{CEO} = 2V) limiting their use in millimeter-wave power applications. In this work, InP double-heterojunction devices were fabricated in the transferred-substrate technology. The devices exhibited high power gain and high power handling capability in the W-band (75~110 GHz) frequency range [43].

In this chapter, the layer structures and fabrication techniques for power HBTs in the transferred-substrate technology are described. The development of multiple finger power devices is then considered and the thermal characterization of these devices is discussed. Finally, DC and RF transistor measurements are presented and these measurements are used to develop both large and small signal transistor models.

4.1 Transferred-substrate InP DHBT layer structure

The DHBT layer structures used in this work have both InP emitter and collector layers with an InGaAs base. The band gap difference between InP and the InGaAs base material is about 0.6 eV. At the emitter-base heterojunction this band offset will simply increase the turn-on voltage of the device. At the base-collector junction, the offset will result in current blocking causing a severe degradation in device performance. In this work an InAlAs/InGaAs chirped super lattice (CSL) grade is used to remove the conduction band discontinuity at both the emitter-base and base-collector heterojunctions [44].

In the collector, compositional grading introduces a quasi-electric field, which will result in collector current blocking at high current densities (Kirk effect). This quasi-electric field can be neutralized by creating an equal and opposite charge dipole. The dipole can be realized by introducing a delta-doped layer at the collector end of the base-collector grade [45]. It also has been shown that a InGaAs setback layer immediately before the base-collector grade can further prevent Kirk effect in DHBTs. This is also significant in improving the saturation voltage of the DHBT at high current densities.

Table 4.1 shows a typical InP DHBT layer structure used in this work. The base-collector grade period is set to 1.5 nm to avoid superlattice mini-band effects and

resulting variations in $\boldsymbol{b}$ with V_{ce} [18]. The 3000Å collector is chosen for high f_{max} and high breakdown with a moderate f_t.

In the transferred-substrate technology, the InP substrate is removed through a wet etching process. Therefore, stop etch layers are inserted between the substrate and the collector to protect the InP collector from being attacked during substrate removal. Design considerations for these stop etch layers will be introduced later.

Layer	Material	Doping	Thickness(Å)
Emitter Cap	InGaAs	1×10^{19} : Si	300
Grade	InGaAs/ InAlAs	1×10^{19} : Si	200
N^{++} Emitter	InP	1×10^{19} : Si	900
N^{-} Emitter	InP	8×10^{17} : Si	300
Grade	InGaAs/ InAlAs	8×10^{17} : Si	233
Grade	InGaAs/ InAlAs	2×10^{18} : Be	67
Base	InGaAs	4×10^{19} : Be	400
Grade	InGaAs/ InAlAs	1×10^{16} : Si	480
Delta Doping	InP	1.6×10^{18} : Si	20
Collector	InP	1×10^{16} : Si	2500
Sub Collector	In Ga As	1E19 : Si	750
Stop etch layer	InP	Undoped	500
Stop etch layer	In Ga As	Undoped	1500
Buffer layer	In Al As	Undoped	2500
	SI : InP		Substrate

Table 4.1 InP/InGaAs DHBT layer structure

Figure 4.1shows the band diagram of the HBT under bias of V_{be}=0.7 V and V_{ce}=1.5 V simulated using 1-dimension Poisson simulator.

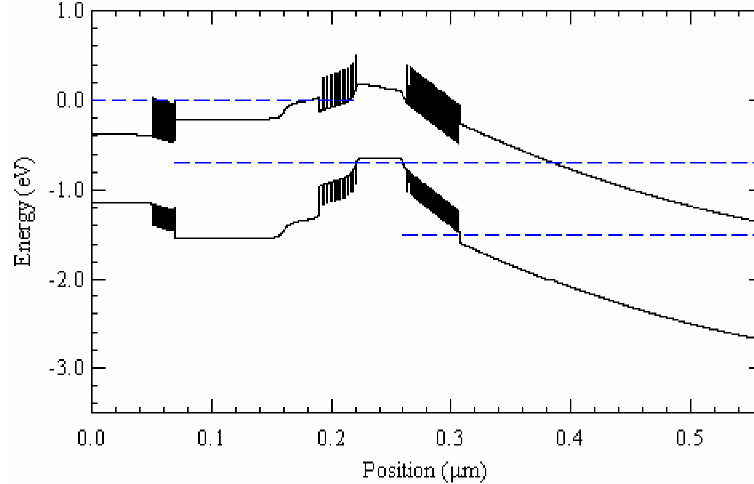


Figure 4.1: Band diagram of InP HBT

4.2 Transferred-substrate InP DHBT fabrication

The transferred-substrate process flow has been discussed in detail in previous publications [46] [5]. For completeness, a brief discussion of process features is presented here. Specific process features for high power DHBT devices are considered in detail.

Figure 4.2 shows a diagram of the transferred-substrate process flow. The emitter-mesa is defined using an all wet etch self-aligned process. After emitter contact evaporation, the emitter cap and grade layer are etched using an InGaAs/ InAlAs etchant that is composed of H_2O_2:H_3PO_4:H_2O. The InP emitter layer is removed by HCl/H_3PO_4 solution and the etch stops at the InAlAs/InGaAs base emitter grade layer. A non-selective citric etch with very slow etching rate is used to etch the remaining grade and part of the base layer. The citric etchant is composed of citric:H_2O_2:H_3PO_4:H_2O. Details of the etch concentrations and rates can be found in the process flow sheets included in the appendix.

Self-aligned base contacts are evaporated around the emitter contact, and a patterned photoresist is used as the mask for the device mesa etch. The mesa etch goes through the base, collector and subcollector epitaxial layers to isolate the devices. After the isolation and interconnect metallization, a 6µm thick spin-on-polymer, BCB, is applied and cured for wafer planarization. A CF_4/O_2 RIE is used to form thermal and electrical vias through the BCB and etch back the BCB to a final thickness of 6µm. A gold ground plane is then electroplated over the entire BCB surface. The wafer is bonded topside down to a GaAs or AlN carrier wafer using In/Pb solder. A selective wet etch is used to remove the InP substrate stopping on the InAlAs and InGaAs protection layers. These protection layers and the InP stop etch layer are then removed using the same etchants as in emitter and base mesa etches.

After the sub-collector layer is removed, Schottky collector contacts are formed by direct metal evaporation with alignment to the emitter metal on the other side of the device epitaxy.

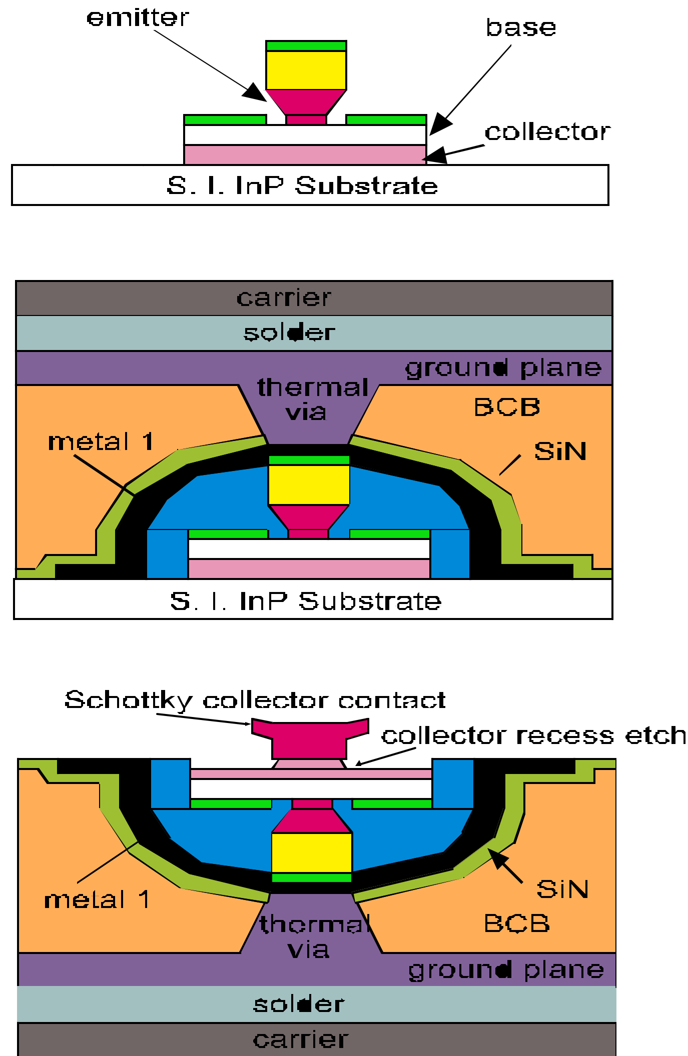


Figure 4.2: Diagram of transferred-substrate technology

The substrate bonding scheme is designed to reduce the biaxial compression, induced by the different coefficients of thermal expansion of materials [42], and has proven effective in improving fabrication yield. However, for large device structures, biaxial compression can accumulate and still cause damage to the collector protection layer. This topic will be addressed in the chapter describing power amplifier fabrication. A process trailer for the transferred-substrate InP DHBT is given in the appendix.

4.3 Multiple finger DHBT topology

In Chapter 2, the topology of a multiple finger transferred-substrate HBT has been described (Figure 2.20) and compared to that of the normal horse-hoof multiple finger mesa HBT (Figure 2.19). The transferred-substrate multiple finger HBT has the advantages of low parasitic base-collector capacitance, low transmission phase delay, ease of modeling, and compactness.

However, the transferred-substrate HBT experiences strong thermal effects due to its unique device structure. As shown in Figure 4.2, the thermal heat sink for the device is located underneath the emitter contact, formed by an Au/Solder via to the carrier wafer. The whole device island is surrounded by the polymer BCB, which has very low thermal conductivity. A majority of power dissipation in a HBT occurs in the base-collector region, and the heat must flow vertically into the sink, passing through the base and emitter epitaxy layers. For a transferred-substrate device with its emitter grounded, the emitter metal makes direct contact to the via heat sink. For a non-grounded emitter device, a 4000Å SiN film electrically isolates the emitter metal from the thermal via. This configuration further worsens the devices thermal performance, since SiN is a poor thermal conductor. Due to their poor thermal characteristics, multiple finger TS-HBTs are very prone to current hogging.

Figure 4.3 shows a die photograph of a first generation multiple finger transferred-substrate DHBT. The device has eight 1 μm $\times$16 μm emitter fingers. The collector stripes are 2 μm $\times$ 20 μm. A nominal 9 Ω NiCr ballast resistor is connected to each emitter finger. Figure 4.4 and Figure 4.5 show the device DC and RF measurement results, respectively.

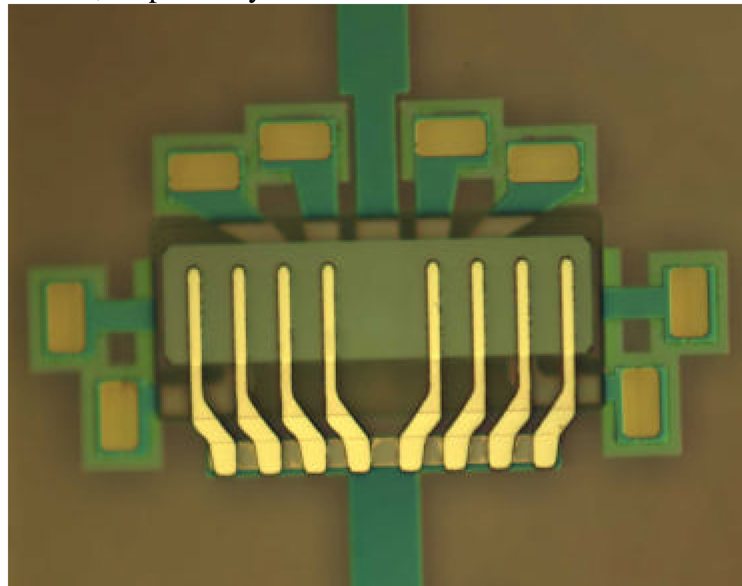


Figure 4.3: Die photograph of a first generation 8-finger TS HBT. Each finger has 1 μm $\times$ 16 μm emitter and 2 μm $\times$ 20 μm collector

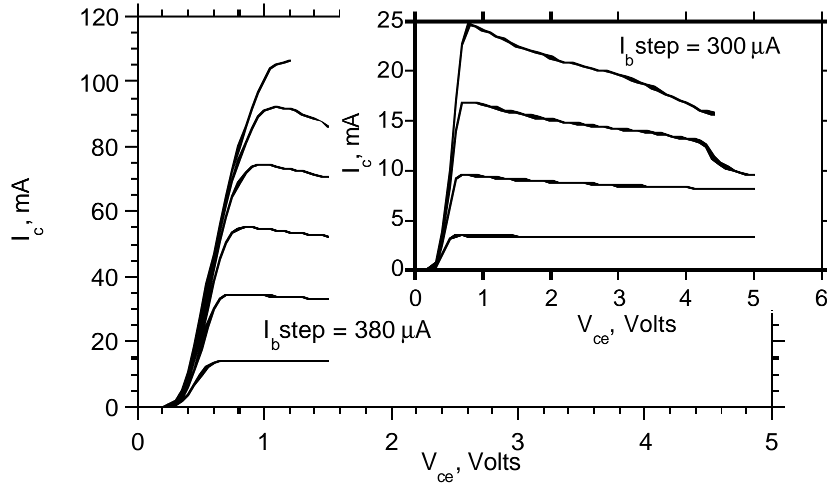


Figure 4.4: DC common-emitter characteristics of an 8-finger TS-HBT.

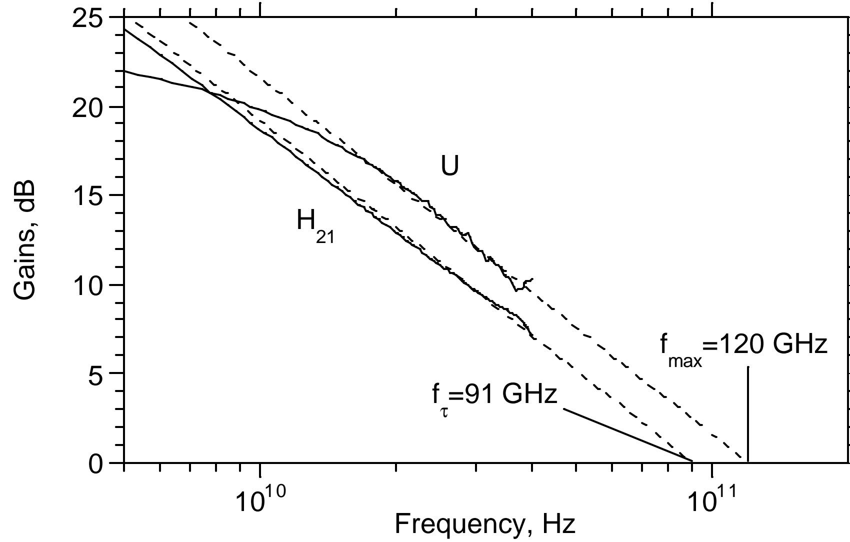


Figure 4.5: RF gains of the first generation 8-finger TS HBT

On the same wafer as the multiple finger device, a single finger device (A_E=1 × 16 µm^2) exhibited an f_{max} of greater than 300 GHz while the 8-finger device shows an f_{max} of only 120 GHz. The f_{max} collapse of the multiple finger device is attributed to a large base feed resistance and pre-mature Kirk effect caused by current hogging, effects which have been discussed in Chapter 2. The DC common-emitter characteristics of the device (Figure 4.4) shows evidence of current hogging at V_{ce}=1.2 V.

To improve both the power and high frequency performance of the device, thermal-electric characterization was performed to determine the appropriate emitter

spacing and ballasting scheme for stability. The thermal-electric characterization of TS DHBTs will be presented in the next section.

To improve the base feed resistance, a new base feed topology was developed, and is shown in Figure 4.6.

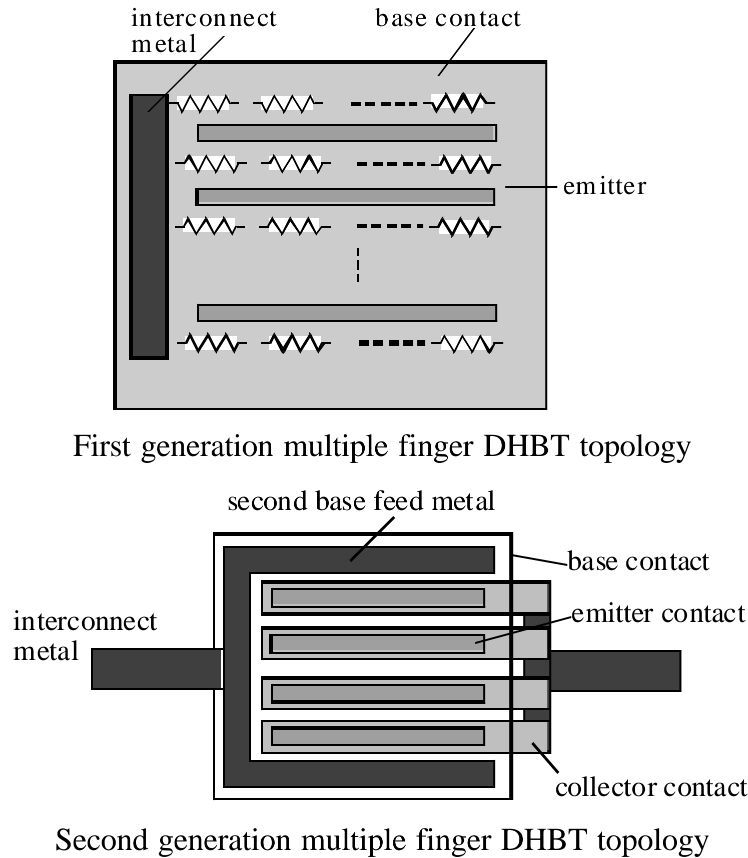


Figure 4.6: Comparison of two multiple finger DHBT topologies

Figure 4.6 shows two possible multiple finger HBT topologies. In the first 8-finger device, a single large area base contact is placed over the entire base mesa region with a single thick metal interconnect at one side of the structure. In the second topology, four emitter fingers are realized with a thicker base metal feed surrounding the entire device. This new device topology has three advantages. First, the second base feed metal can substantially reduce the base metal feed resistance. Secondly, the possibility of thermal-current non-uniformity is decreased with the reduction of the number of fingers. Thirdly, larger power DHBTs can be formed by connecting a number of 4-finger unit cells in parallel with their input and output connected by microstrip lines. The low input and output impedances of the unit cell can be pre-matched through their interconnecting microstrip lines. This simplifies the design of an amplifier's matching networks.

The thermal coupling effects of power HBTs described in Chapter 2 depend upon the emitter stripe length. Current non-uniformity along the emitter finger

increases with the emitter length, and as a result, current hogging within a finger can easily occur in multiple finger HBTs with long emitter fingers. The optimum emitter length of the 4-finger DHBT unit cell was determined by thermal characterization. Large area devices were realized by connecting in parallel a number of 4-finger unit cells. Reduced lengths are obtained for the wires interconnecting emitter and collector fingers within the multiple finger cell. This is a key advantage in computer-aided design, as layout parasitics within the multiple finger cell are electrically significant yet difficult to model with commercially available CAD tools. The longer wires connecting two 4-finger unit cells into an eight finger transistor are microstrip lines with negligible line coupling, and are readily and accurately modeled

4.3.1 Multiple finger DHBT thermal-electric characterization

Figure 4.7: shows a test structure used to measure the thermal resistance of a 4-finger TS HBT using the methods described in Chapter 3.

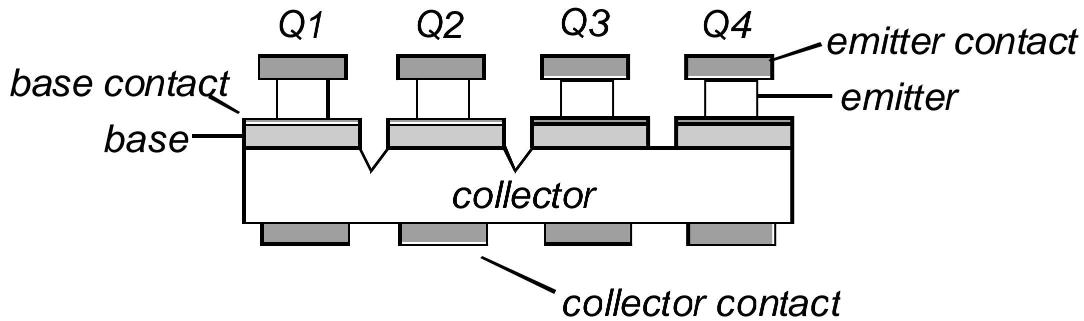


Figure 4.7: Thermal resistance test structure for multiple finger TS DHBT

In the test structure of Figure 4.7, the base of fingers Q_1 and Q_2 are isolated so that they can be biased separately. A shallow etched collector groove prevents current modulation between the fingers while providing a continuous path for thermal conduction.

Using the method described in section 3.5, the thermal resistances of Q_1 and Q_2 can be obtained. The regression plots shown are the measurement results of this device that are re-plotted here:

The self-heating thermal resistances obtained are $R_{th11}=R_{th22}=3.03$ ^{o}C/mW and the coupling thermal resistance are $R_{th12}=R_{th21}=0.18$ ^{o}C/mW. The emitter finger of this device is 1 μm × 16 μm; the collector finger is 2 μm × 20 μm and the emitter spacing is 7 μm. The same thermal characteristics are observed between Q_2/Q_3 and Q_3/Q_4. The thermal coupling between Q_1 and Q_3 is too small to be measured. To maintain the thermal stability of all the fingers when biased at J_c=100 kA/cm^2 and V_{ce}=3 V, the emitter ballast resistance required to satisfy Eqn. 2.45 to 2.47 can be calculated:

$$\mathbf{l} = \frac{\tilde{R}_{th_11} + \tilde{R}_{th_22}}{2} + \frac{\sqrt{(\tilde{R}_{th_11} - \tilde{R}_{th_22})^2 + 4\tilde{R}_{th_12}\tilde{R}_{th_21}}}{2} = 3.32^oC/mW$$

$$R_{E2} \geq |\Phi| V_{CE}\mathbf{l} - \frac{1}{g_m} = 7.4\,\Omega \quad . \tag{4.1}$$

R_{E2} is the emitter ballast resistance, g_m is the transconductance and V_{CE} is the collector bias voltage. From Eqn. 4.1, R_{E2} should be greater than 7.4 Ω.

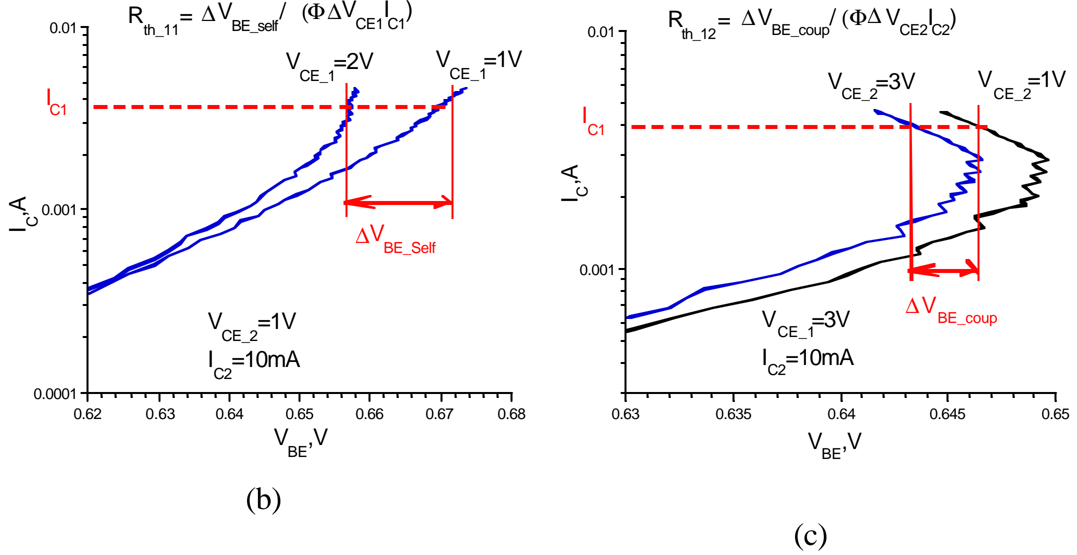


Figure 3.10: (b) self-heating measurement plot-R_{th_11};
(c): Thermal-coupling measurement plot-R_{th_12}

4.3.2 Multiple finger DHBT device results

A submicron transferred-substrate DHBT with the layer structure of table 4.1 has been reported with an f_{max} of 462 GHz at current density of 1.5 mA/μm^2 [10]. This device has emitter size of 0.5 μm× 8 μm and the collector breakdown voltage is 8 V.

Using the same layer structure, 4-finger power DHBTs have been developed. These devices have emitter finger dimension of 1 μm ×16 μm and collector dimension of 2 μm ×20 μm. The base mesa dimension is 56 μm × 38 μm. The emitter finger spacing was chosen to be 7 μm in order to achieve a very small coupling thermal resistance. In accordance with the thermal-electric characterization described previously (Eqn. 4.1), an 8 Ω NiCr ballast resistor is connected to each emitter finger. Because each emitter finger has an intrinsic series resistance of 3 Ω, the total emitter ballast resistance is 11 Ω satisfying the stability requirement. Figure 4.8 shows a die photograph of the 4-finger DHBT in a common-emitter configuration.

Figure 4.9 shows the common-emitter characteristics of the 4-finger DHBT. The transistor demonstrates a maximum current density of 1 mA/μm^2 at V_{CE}=1.2 V and

low current collector breakdown of 7 V. The RF gains of the device are plotted in Figure 4.10. When biased at I_C=57 mA and V_{ce}=2.5 V, the device exhibits an extrapolated f_{max} of 371 GHz and a f_T of 107 GHz.

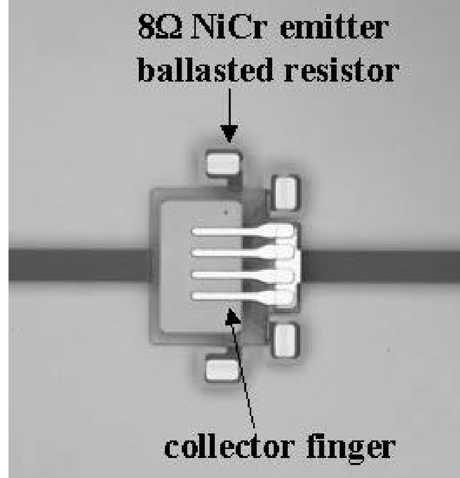


Figure 4.8: 4-finger 1 μm × 16 μm common emitter TS DHBT

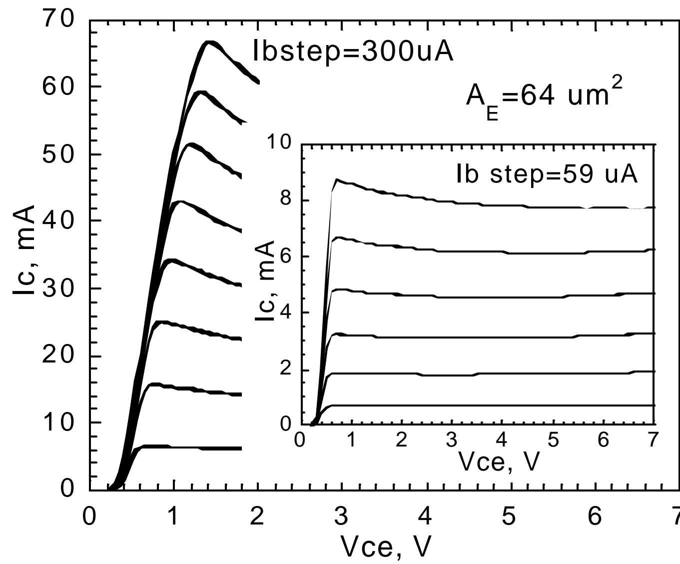


Figure 4.9: DC common-emitter characteristics of 4-finger 1 μm × 16 μm common emitter TS DHBT

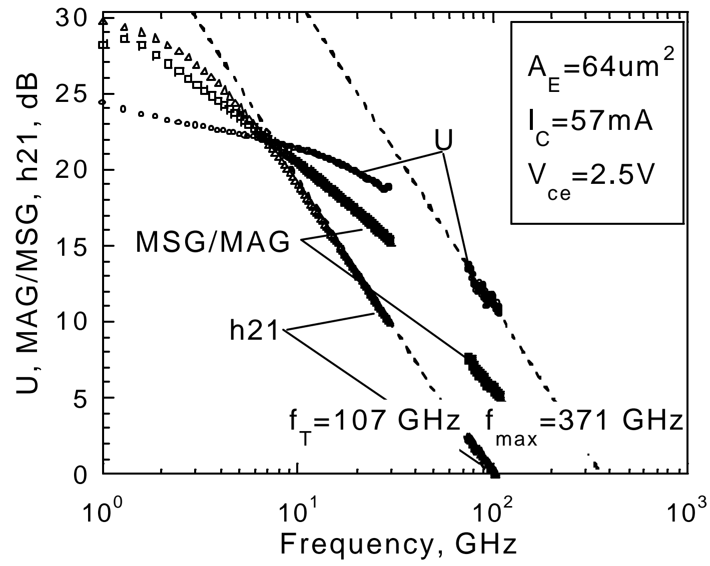


Figure 4.10: RF gains of 4-finger 1 μm × 16 μm common emitter TS DHBT

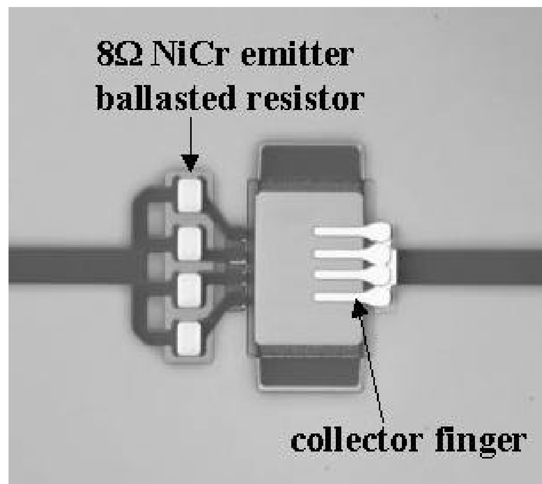


Figure 4.11: 4-finger 1 μm × 16 μm common base TS DHBT

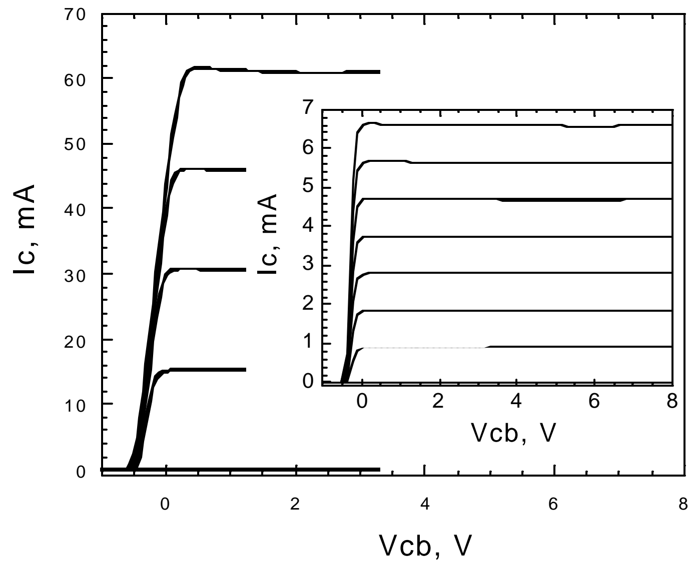


Figure 4.12: DC common-base characteristics of 4-finger 1 µm × 16 µm TS DHBT

Figure 4.11 shows a die photograph of the 4-finger DHBT in common-base configuration. Figure 4.12 shows the DC common-base characteristics for the 4-finger 1 µm × 16 µm device. Mason's unilateral power gain U and MAG/MSG of the common-base device are plotted in Figure 4.13. The transistor extrapolated f_{max} is 342 GHz.

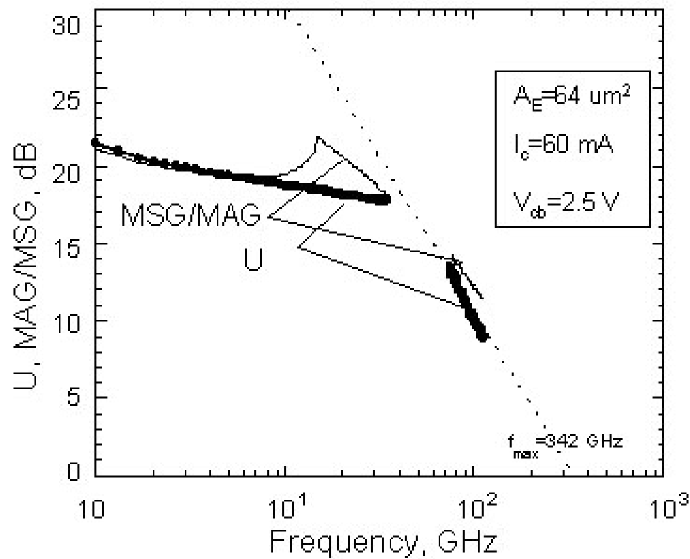


Figure 4.13: RF gains of a 4-finger 1 µm × 16 µm common base TS DHBT

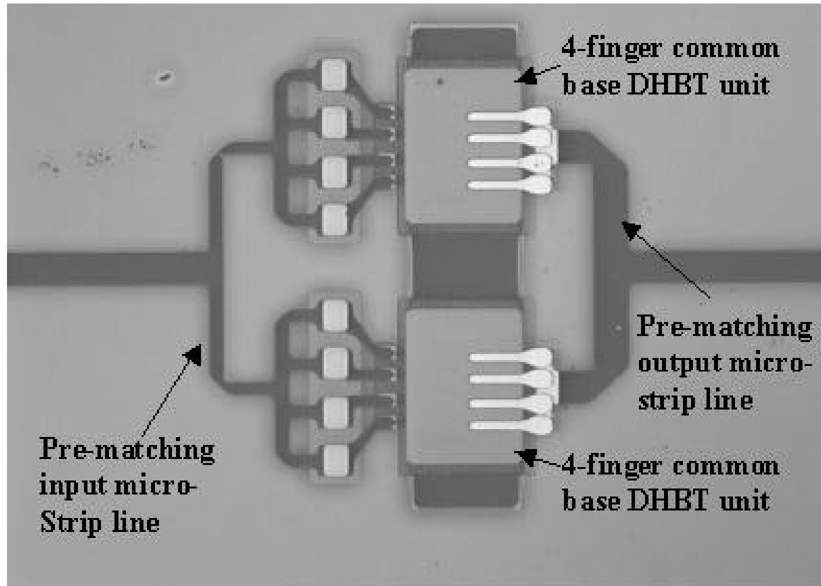


Figure 4.14: 8-finger 1 μm × 16 μm common base TS DHBT

To achieve even higher output power, an 8-finger TS DHBT was developed with two 4-finger common base cells lumped in parallel. The cells are connected by microstrip transmission lines which also act as pre-matching networks to transform the very low input/output impedances of the device. Figure 4.14 shows a die photograph of the device.

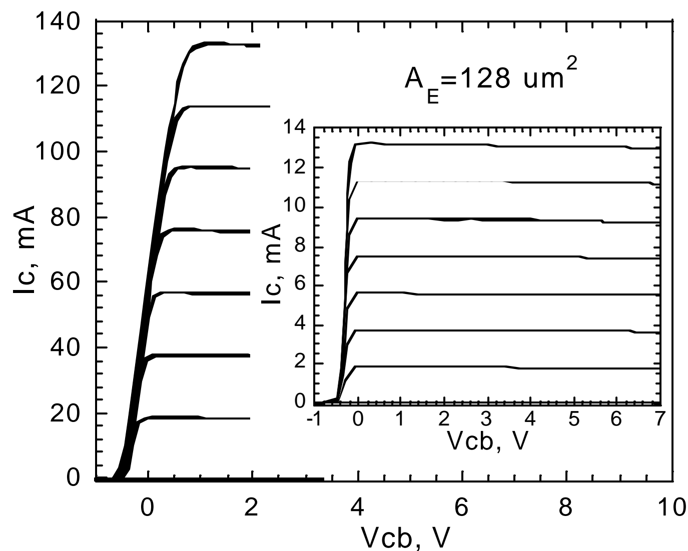


Figure 4.15: DC common-emitter characteristics of 8-finger 1 μm × 16 μm TS DHBT

The DC common-emitter characteristics of the 8-finger device are plotted in Figure 4.15. The maximum current of this device is 130 mA at V_{CB}=0.8 V and the collector breakdown voltage is 8V at low current. The RF gains of the device are plotted in Figure 4.16. When biased at I_c=100 mA and V_{ce}=3.6 V (V_{cb}=2.9 V), the device exhibits an f_{max} of 330 GHz. This result represents the highest f_{max} of an HBT operating at greater than 100 mA current.

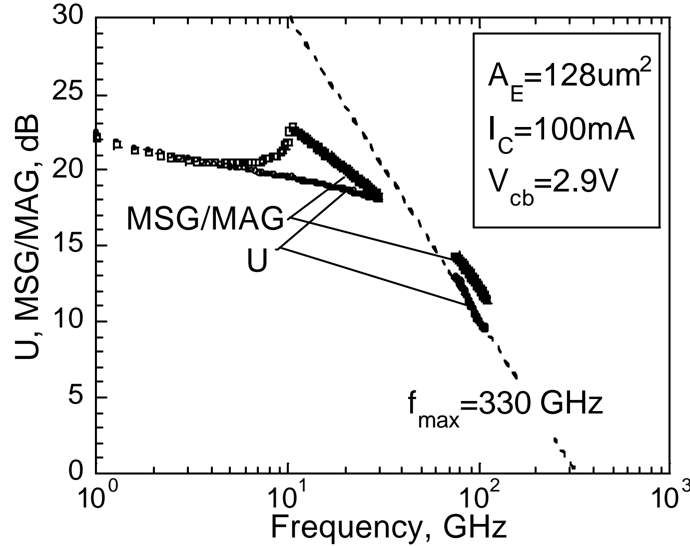


Figure 4.16: RF gains of 8-finger 1 µm × 16 µm common base TS DHBT

4.3.3 Hybrid-π model extraction

The small signal hybrid-π model of the 4-finger common emitter TS HBT was extracted using the methods presented in Chapter 3. Figure 4.17 shows the hybrid-π model schematic.

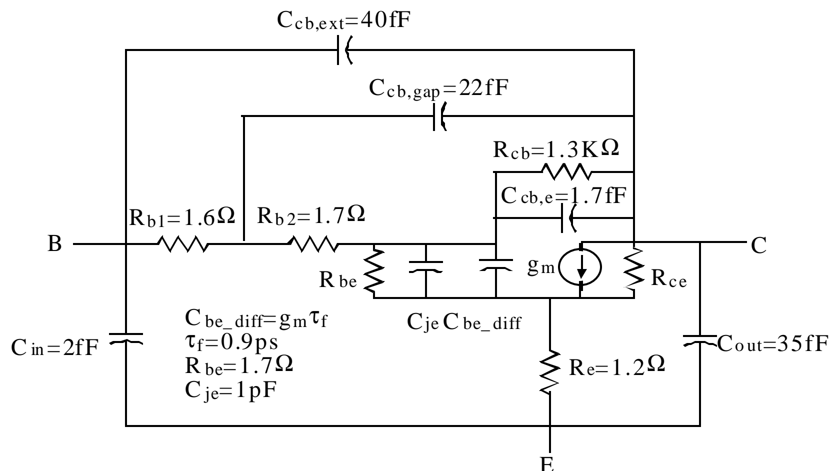
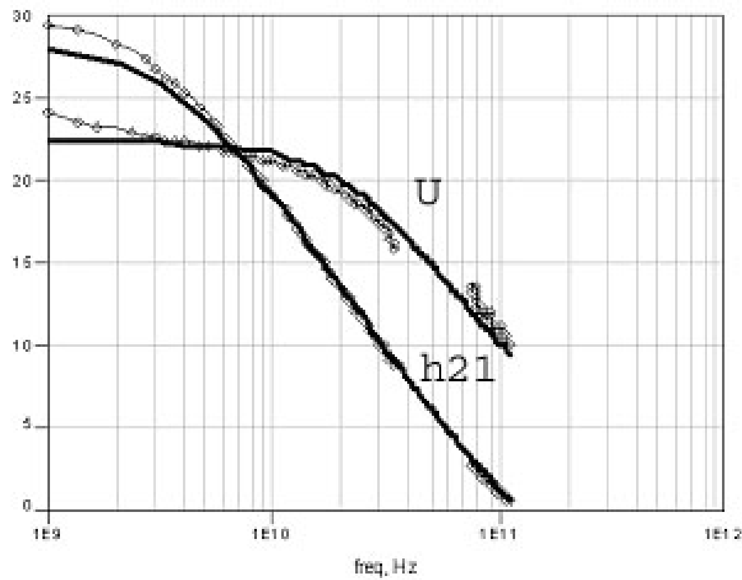


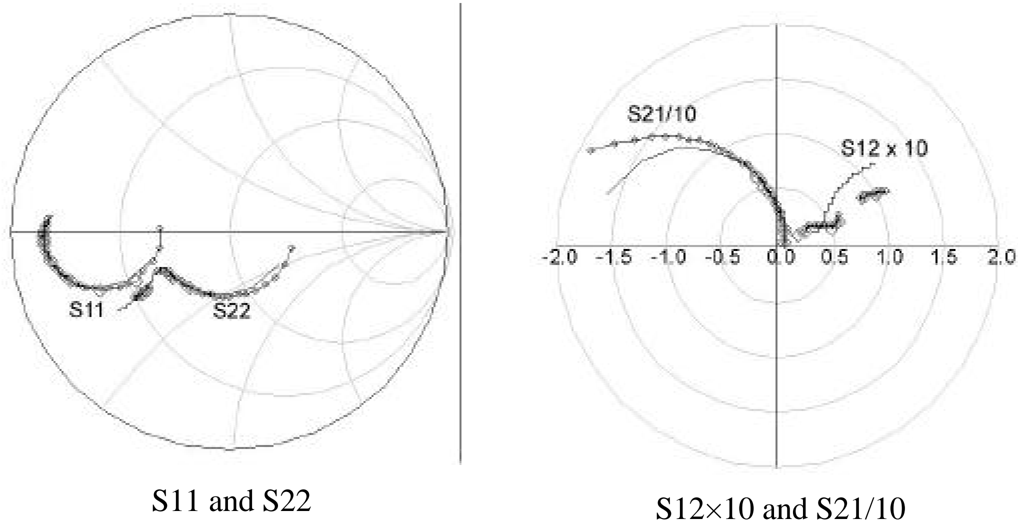
Figure 4.17: 4-finger common emitter TS DHBT hybrid-π model

The small signal model was obtained at bias conditions of I_C=57 mA and V_{ce}=2.2 V. The extracted model parameters normalized with respect to area show close agreement with those extracted for a single finger devices fabricated in the same layer structure [10]. The small extracted base resistance of 3.3 Ω, verifies that the effectiveness of the second base feed metal in reducing the metal feed resistance.

Figure 4.18 shows the plots comparing the hybrid-π model simulation with the measured S-parameters and gains. The LRL calibration method employed only exhibits good calibration in the range from 6 GHz to 45 GHz, which explains the discrepancy in the frequency below 6 GHz.



U and h_{21} versus frequency



S11 and S22

S12×10 and S21/10

Figure 4.18: hybrid-π model simulation compared to the measured S-parameters

4.3.4 Large signal model

The large signal model of the 4-finger common emitter device is extracted by considering the small-signal hybrid-π model, the measured DC characteristics and thermal-electric properties of the transistor. Because the thermal-electric properties are different for different fingers within the unit cell, the large signal model must have unique models for the individual fingers.

Figure 4.19 shows the schematic of the large signal model of the 4-finger common-emitter device. The large signal model uses a hierarchical structure. The top level is composed of 4 parallel transistors, and the second level is the individual transistor large signal model including thermal effects, as described in Chapter3.

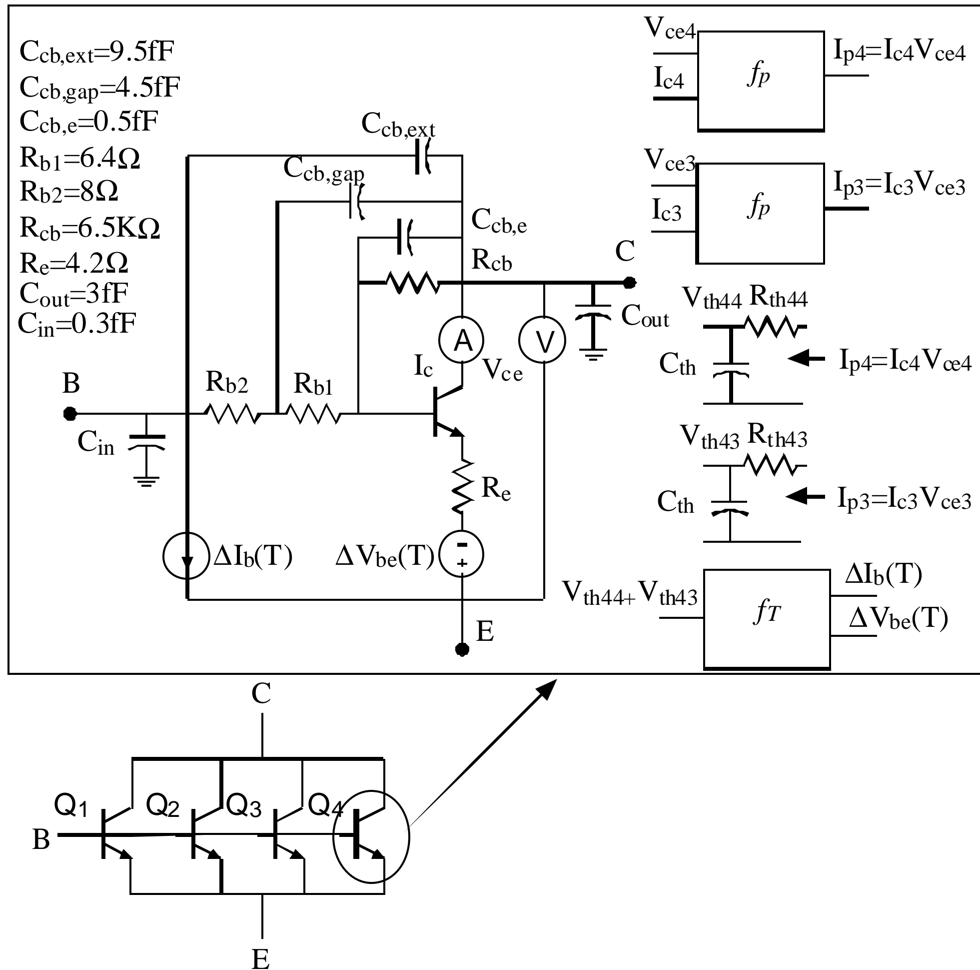


Figure 4.19: 4-finger hierarchy large signal model

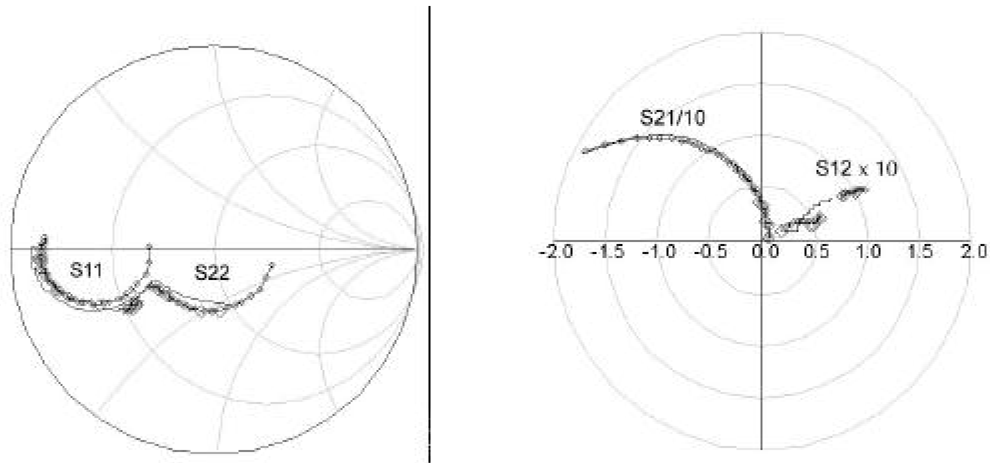


Figure 4.20: Large signal model simulation compared to the measured S-parameters at I_C=57 mA and V_{ce}=2.2 V

The parasitic elements in the second level large signal model are obtained from the hybrid-π model of the multiple finger device. Small adjustments to the model have been made to match measured results. The thermal resistances in the model are obtained from the thermal characterization. The two central fingers are thermally coupled to two neighboring fingers while the two edge fingers are only coupled to one neighboring finger.

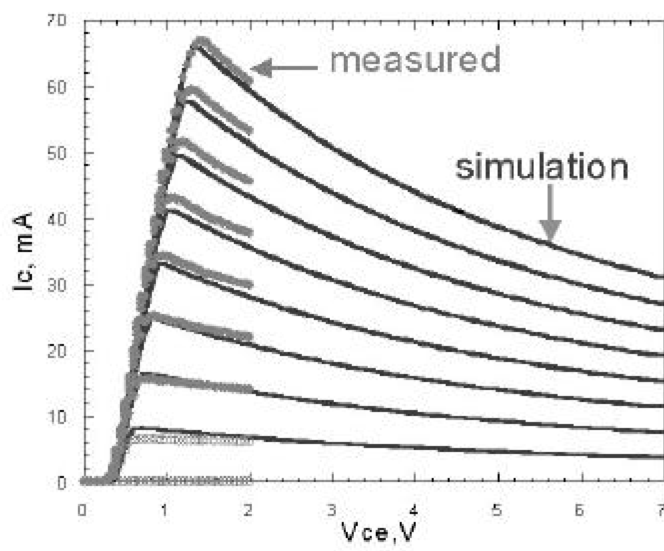


Figure 4.21: DC large signal model simulation compared to measurement for 4-finger 1 µm × 16 µm common emitter TS DHBT

The large signal model has been tested at different bias conditions and compared with the corresponding measured results. The simulations show good agreement with

the measurements. Figure 4.20 shows the RF simulation and measurement result at I_C=57 mA and V_{ce}=2.2 V. Figure 4.21 shows the measured and simulated DC common-emitter characteristics.

4.4 Power DHBTs with a lightly doped emitter epitaxial layer

Multiple finger HBTs have complex thermal-electric effects. In Chapter 2, it was found that the thermal gradients between fingers become stronger when the device operates at high power levels. Current hogging occurs between the fingers, with the central fingers taking the majority of the bias current. For a long emitter device, the same phenomenon may arise, leading to a non-uniform current distribution along the emitter with a high current density in the center region. This current non-uniformity drives the device into both thermal instability and into premature Kirk effect, which reduces device bandwidth.

In Chapter 3, device thermal stability was analyzed (Eqn. 3.19), from which it is seen that the safe operating area of a multi-finger HBT can be improved by either improving the thermal conductivity between the device and the substrate, by increasing thermal coupling between fingers, or by choosing a suitable resistive ballasting scheme. In the first sections of this chapter, efforts to optimize the topology of a multiple finger device so as to reduce the thermal coupling were described. In this section, a DHBT structure with a lightly doped emitter epitaxial layer is presented to provide an efficient emitter-ballasting scheme.

4.4.1 LDE DHBT design

In Chapter 2, different resistive ballasting approaches were analyzed and verified experimentally. It was concluded that emitter ballasting is more applicable than base ballasting in MMIC design, and that distributed emitter ballast resistors are more efficient in increasing the stability of the device without a significant impact on bandwidth.

The long emitter finger experiment presented in Section 2.4.3 demonstrates that by properly assigning the emitter ballast resistance to each section of the emitter, a uniform current distribution can be achieved. However, this scheme results in a complex transistor layout with significant parasitics, and is not suitable for amplifier design. Both the interconnects and the physical resistor itself consume a large area which makes distributed ballasting with thin film resistors impractical for multiple finger HBT realization.

By adding a lightly doped epitaxial layer between the emitter and the emitter contact layer, a distributed ballast scheme can be achieved [47]. In this work, a lightly doped InP layer was used as the resistive epitaxy. InP has a high thermal conductivity thus this layer will not significantly increase the thermal resistance. In contrast to the work in [47] that utilizes an AlAs emitter layer, the InP LDE introduces no bandgap discontinuity in the emitter.

Table 4.2 shows the epitaxial layer structure of the LDE DHBT and Figure 4.22 is the band diagram simulation. The InP LDE is inserted into the emitter with a doping density of 5×10^{16} cm^{-3}. To simplify its integration into the process flow, the total emitter thickness was kept the same as the layer structure in table 4.1. If the InP emitter thickness is too large, the wet etching time has to be increased and this produces an unpredictable etch undercut of the emitter region.

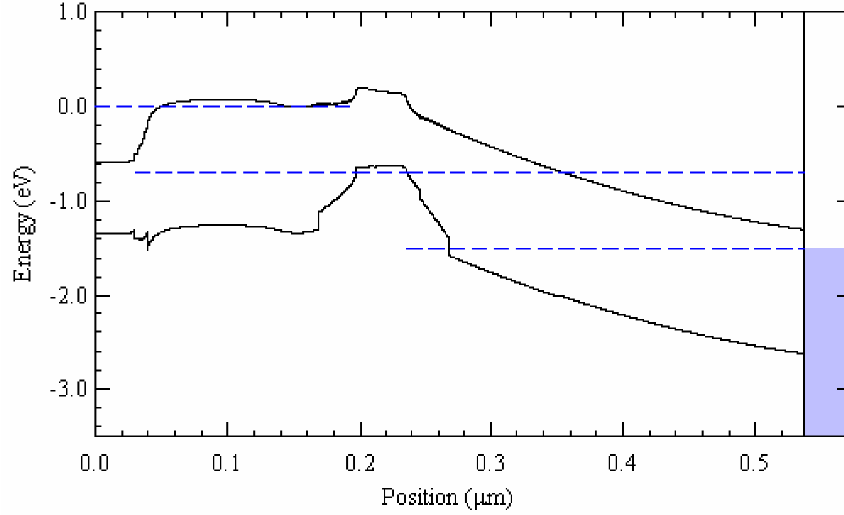


Figure 4.22: LDE DHBT band diagram

The resistance of the LDE layer is given by:

$$R_{LDE} = \rho_{LDE} \frac{t_{LDE}}{A_E} = \frac{t_{LDE}}{q u_n n_E A_E} \quad . \tag{4.2}$$

u_n is the electron mobility; n_E is the mobile electron density; A_E is the emitter contact area and t_{LDE} is LDE thickness. R_{LDE} should be chosen to satisfy the thermal stability criteria of Eqn. 3.18. There is a second restriction on the layer design. The doping density in the LDE region must be high enough to support the transistors emitter current. Thus, the doping density, N_{d_LDE}, must satisfy the expression

$$q N_{d_LDE} v_{sat} > J_{\max} \quad . \tag{4.3}$$

J_{max} is the maximum current density of the device, and v_{sat} is the electron saturation velocity in the emitter. Assuming J_{max}=1 mA/µm^2 and v_{sat}=1.5 × 10^7 cm/S, N_{d_LDE} must be greater than 4.16 × 10^{16} cm^{-3}. The doping density in this work was chosen to be N_{d_LDE} =5 × 10^{16} cm^{-3}. Assuming an electron mobility of u_n=2000 cm^2/V.S, the LDE resistance is thereby calculated (Eqn. 4.2) as 64 Ω−µm^2.

Layer	Material	Doping(cm^{-3})	Thickness(Å)
Emitter Cap	InGaAs	1×10^{19} Si	300
Grade	InGaAs/ InAlAs	2×10^{19} Si	90
LDE Emitter	InP	5×10^{16} Si	1000
N^- Emitter	InP	8×10^{17} Si	300
Grade	InGaAs/ InAlAs	8×10^{17} Si	233
Grade	InGaAs/ InAlAs	2×10^{18} Be	67
Base	InGaAs	4×10^{19} Be	400
setback	InGaAs	1×10^{16} Si	100
Grade	InGaAs/ InAlAs	1×10^{16} Si	216
Delta Doping	InP	3.75×10^{18} Si	20
Collector	InP	1×10^{16} Si	2664
Sub Collector	In Ga As	1E19 Si	1000
Stop etch layer	InP	Undoped	1000
Stop etch layer	In Ga As	Undoped	1500
Buffer layer	In Al As	Undoped	2500
	SI : InP		Substrate

Table 4.2 InP/InGaAs DHBT layer structure with lightly doped epitaxy

4.4.2 LDE transferred-substrate DHBT results

Two 4-finger DHBTs were fabricated with emitter widths of 1 µm and emitter lengths of 24 µm and 32 µm. The collector dimensions are 2 µm × 26 µm for the 24 µm emitter device and 2 µm × 34 µm for the 32 µm emitter device. To reduce the thermal coupling between fingers, the 24 µm emitter design has an emitter spacing of 8 µm and the 32 µm emitter device spacing is 9 µm.

The LDE resistance is determined by Eqn. 4.2. For the 24 µm emitter device, the LDE resistance of each emitter finger is R_{LDE}=2.6 Ω. For the 32 µm emitter device,

R_{LDE}=2 Ω. To ensure thermal stability in the multiple finger structure, external ballast resistances are still required for these devices. The equivalent circuit of the long finger LDE HBT is show as the right schematic of Figure 4.23.

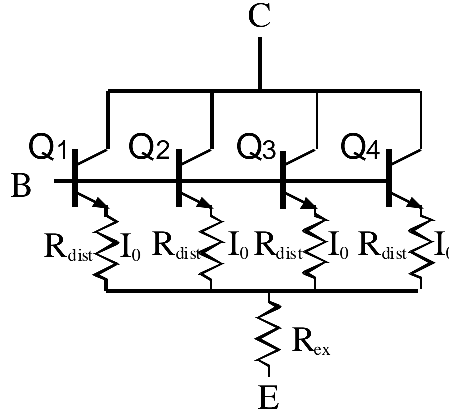


Figure 4.23: Equivalent ballasting circuits of long emitter DHBTs

The distributed resistance R_{dist} of each emitter finger is composed of the device contact resistance and the LDE resistance. An external NiCr resistance R_{ex} of 4.5 Ω is connected to each emitter finger. Given the measured 20 Ω–μm^2 contact resistance, the total emitter ballast resistance for each finger is 5.7 Ω for the 4-finger 24 μm^2 device and 5.1 Ω for the 4-finger 32 μm^2 device.

For comparison, devices were also fabricated without the LDE layer. The layer structure of these devices is the same as that of LDE except that the LDE layer is replaced by a 1000 **Å** InP doped at 1×10^{19} cm^{-3}. These devices also use an external 9 Ω NiCr ballast resistor for each finger. Thus, the total emitter ballast resistance is 9.8 Ω for the 4-finger 24 μm^2 device and 9.6 Ω for the 4-finger 32 μm^2 device.

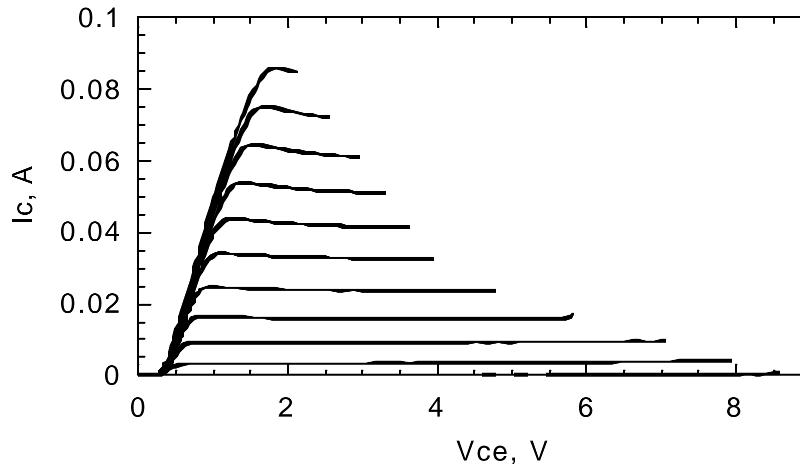


Figure 4.24: DC common-emitter characteristics of a 4-finger 1 μm × 24 μm HBT with a lightly-doped emitter epitaxy

Figure 4.24 shows the DC common-emitter characteristics of the 4-finger 1 μm × 24 μm LDE DHBT. In comparison, Figure 4.24 shows the DC common-emitter characteristics of a similar DHBT but without the lightly-doped emitter layers.

Comparing the DC characteristics, we see that although the 4-finger DHBT without the LDE layer has a total emitter ballast resistance almost twice that of the LDE device, it shows earlier current collapse than its LDE counterpart. This verifies the effectiveness of differential ballast resistance in stabilizing long finger HBTs.

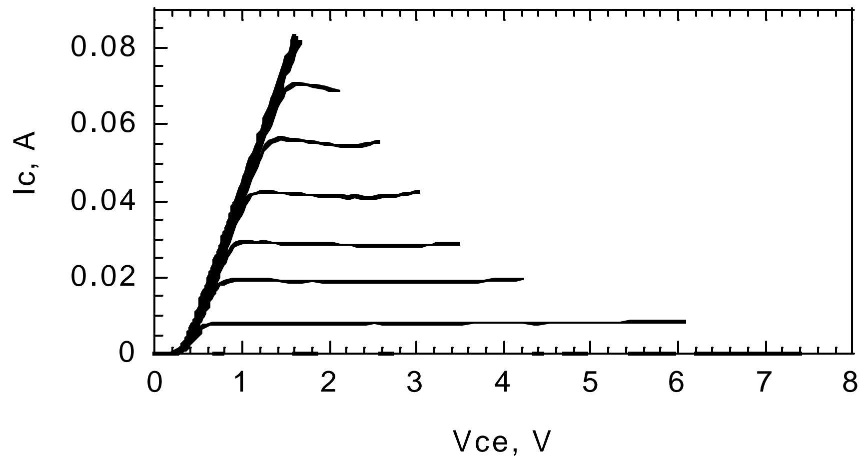


Figure 4.25: DC common-emitter characteristics of a 4-finger 1 μm × 24 μm HBT without the lightly-doped emitter epitaxy

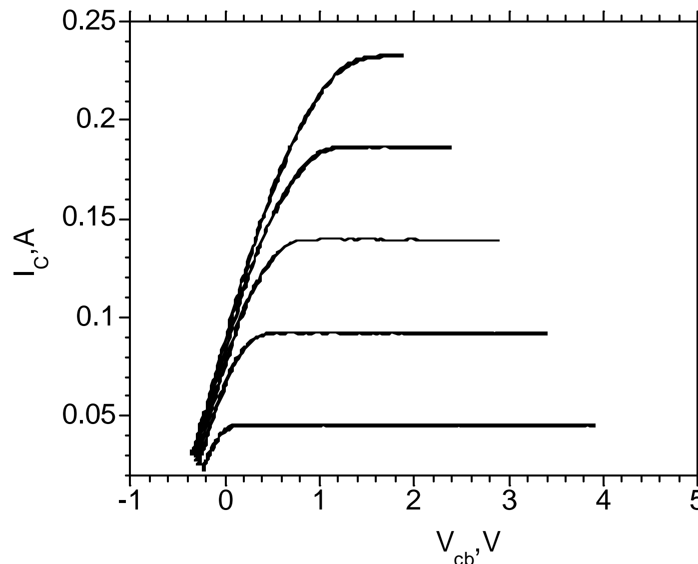


Figure 4.26: DC common-base characteristics of 8-finger 1 μm × 24 μm DHBT with lightly doped epitaxy

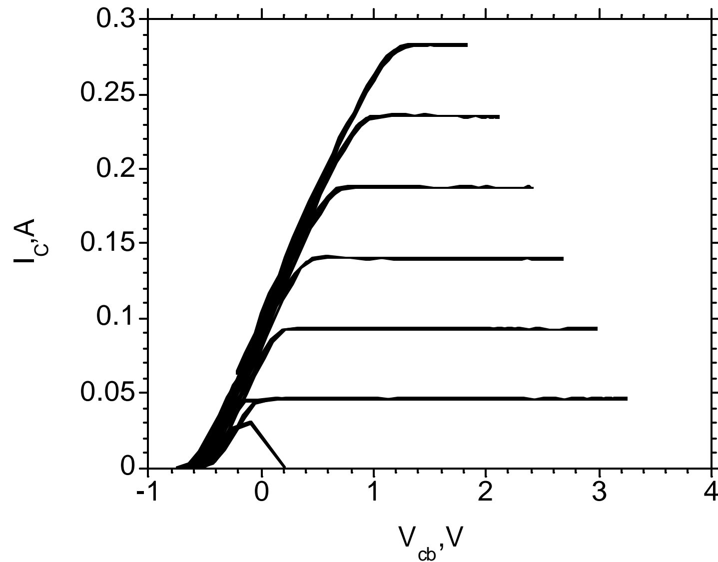


Figure 4.27: DC common-base characteristics of an 8-finger 1 µm × 32 µm DHBT with lightly doped epitaxy

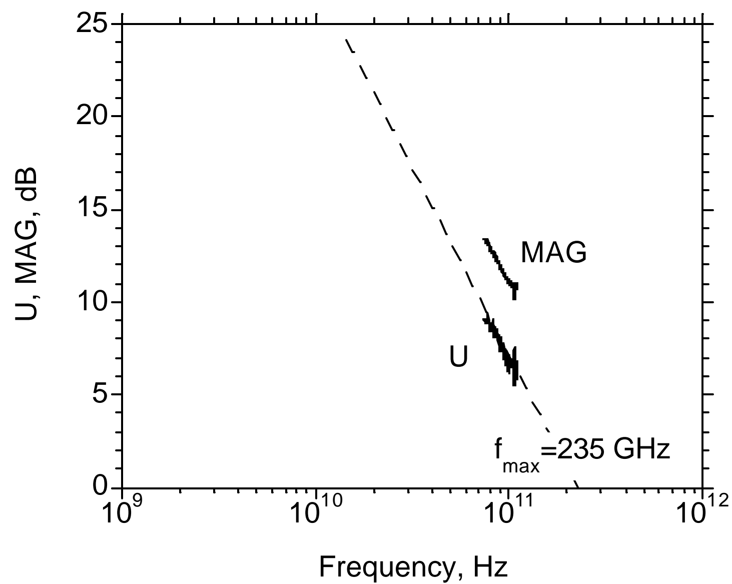


Figure 4.28: RF gains of an 8-finger 1 µm × 32 µm common base DHBT with lightly doped epitaxy

Multiple finger common-base devices were also developed with the LDE epitaxy. The DC common-base characteristics of an 8-finger 1 µm × 24 µm device are shown in Figure 4.25. The maximum current density of this device is J_C=1.25 mA/µm^2 at V_{CB}=1.5 V. Figure 4.26 shows the DC common-base characteristics of

an 8-finger 1 µm × 32 µm LDE DHBT. The device exhibits a maximum safe bias current of 280 mA. The device current is limited by the current carrying capacity of the input transmission line (1 µm thick and 12.5 µm wide).

RF measurements of the LDE DHBT devices were performed. The 4-finger 1 µm × 24 µm common-emitter device exhibited an f_{max}=227 GHz when biased at I_C=65 mA and V_{CE}=2.5 V. The 8-finger 1 µm × 32 µm common-base LDE DHBT had an f_{max}=170 GHz when biased at I_C=110 mA and V_{CB}=2.2 V, and the 8-finger 1 µm × 24 µm common-base LDE DHBT had an f_{max}=235 GHz when biased at I_C=140 mA and V_{CB}=3 V. Figure 4.28 shows a plot of Mason's gain and MAG of the 8-finger 1 µm × 32 µm common-base LDE DHBT. The lower f_{max} of the 8-finger 1 µm × 32 µm common base LDE DHBT is due to the increased base-collector parasitics resulting from the wide emitter separation required for thermal stability.

4.5 Discussion

In the transferred-substrate technology, the emitter and collector can be simultaneously scaled resulting in a substantial reduction of the parasitic base-collector capacitance. Multiple finger DHBTs in the transferred-substrate technology can thus achieve very high bandwidth and while maintaining high output power. To maintain thermal stability in power HBTs, the thermal-electric properties of the device must be characterized to optimize the device topology and ballasting scheme. Emitter ballasting is very effective for ensuring thermal stability for power HBTs in MMIC technologies. Differential emitter ballasting is the preferred ballasting scheme because it is more efficient in power HBT design. A DHBT with lightly doped emitter epitaxy is presented that demonstrates both high output power and high bandwidths.

In this work, a common-base transferred-substrate DHBT is reported with 330 GHz f_{max} when biased at 100 mA and 3.6 V; a common-base device with the LDE epitaxial structure demonstrated an f_{max} of 235 GHz when biased at 140 mA and 3.7 V. These are the first reported high bandwidth and high current/voltage HBTs.

With the methods and approaches described in this chapter, higher power and high bandwidth HBTs were developed in the transferred-substrate DHBT technology and directly applied in W and G-band power amplifiers.

Chapter 5

High frequency DHBT MMIC power amplifiers

Linear power amplifiers can be classified as Class-A and Class-B/AB by the quiescent bias point and the operating mode. The class-A power amplifier has a conduction angle of 2π, and a bias point set to half the maximum current and half the breakdown voltage. The maximum power added efficiency (PAE) of Class-A is 50%. The class-B power amplifier has a conduction angle of π, exhibits a theoretical 78.5% PAE, is biased at zero current and half the breakdown voltage. The conduction angle of Class AB is between π and 2π, thus achieving PAE between that of Class-A and Class-B. Class-B can present both high efficiency and high output power, therefore it is used in most RF wireless applications. Class B amplifiers have lower gain than class A [48], and are thus less suitable for millimeter wave amplifiers, where feasible gains are limited. For this reason, all the power amplifiers in this work are Class-A. Design of Class-A power amplifier will be presented in Section 5.1.

The architectures of linear power amplifiers include single stage, cascode, multi-stage and balanced amplifiers, which will be described in Section 5.2.

Transferred-substrate DHBT MMIC technology has been used for the development of both V-band and W-band power amplifiers in various architectures. The design and measurement results of these amplifiers will be presented in Section 5.3.

5.1 Class-A power amplifier design

Class-A power amplifier bias is depicted in Figure 5.1. The maximum current I_{max}, collector saturation and breakdown voltages V_{CE_sat} and V_{CE_BR} define an optimum output load line that passes through the quiescent point. There is thus and optimum load impedance R_{L_opt}, for maximum output power. Eqn. 5.1 shows the optimum output load, maximum output power and power added efficiency.

$$R_{L_opt} = \frac{V_{CE_BR} - V_{CE_sat}}{I_{\max}}$$

$$P_{opt} = \frac{I_{\max}\left(V_{CE_BR} - V_{CE_sat}\right)}{8} = \frac{\left(V_{CE_BR} - V_{CE_sat}\right)^2}{8R_{L_opt}} \quad . \tag{5.1}$$

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} = \frac{1}{2} \cdot \frac{V_{CE_BR} - V_{CE_sat}}{V_{CE_BR} + V_{CE_sat}} \left(1 - \frac{1}{G}\right)$$

In Eqn. 5.1, P_{opt} is the maximum linear output power, PAE is the peak power added efficiency and G is the insertion gain. From Eqn. 5.1, the maximum output power is to the breakdown and maximum current, while the PAE increases with the insertion gain of the amplifier and is less than 50%.

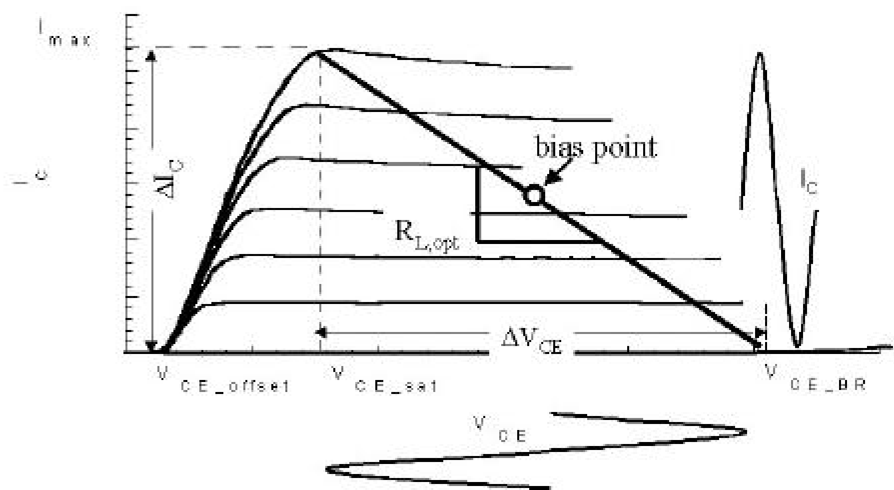


Figure 5.1: Class-A power amplifier optimum output load line

If the load resistance differs from that given above, or if load has a series or parallel reactive component, the saturated output is reduced. Two load lines are drawn in Figure 5.2. The first load line has a load impedance $R_{LH}=P\cdot R_{L_opt}$ larger than the optimum. This results in the same dynamic voltage range but lower dynamic current range than the optimum load line in Figure 5.1. The output power is reduced to $P_{out}=P_{opt}/P$. The second load line has a load impedance of $R_{LL}=R_{L_opt}/P$. For this load line, the dynamic voltage range is reduced P:1 while the dynamic current range is the same as that of the optimum load line. Its maximum output power is also reduced to $P_{out}=P_{opt}/P$.

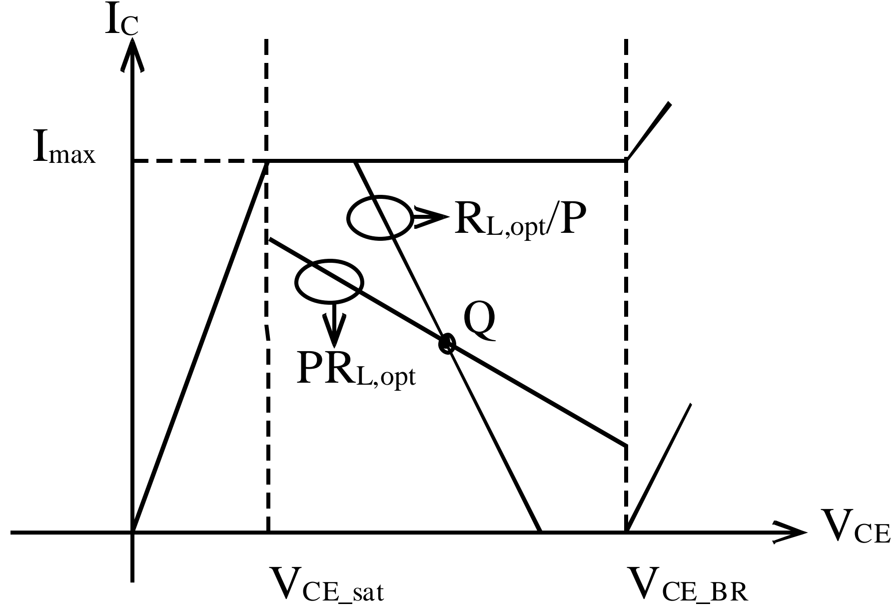


Figure 5.2: Reduced output power loading conditions

In [48], loading conditions with reactance jX in a series connection with R_{LH} and a susceptance jB parallel connected to $G_{LL}=1/R_{LL}$ can be plotted on the Smith chart, which forms the load contours exactly as that obtained by the load-pull system. For a constant output power $P_{out}=P_{opt}/P$, the traces of R_{LH}+jX and G_{LL}+jB form two circles of constant resistance R_{LH} and constant conductance G_{LL} on Smith Chart (Figure 5.3). The intercepts of the two circles are defined by

$$R_{\text{LH}}^2 + X_M^2 = \frac{1}{G_{LL}^2 + B_M^2} = R_{opt}^2 \ , \tag{5.2}$$

In power applications, the transistor must always operate within its safe operating area (SOA). Hence the load dynamic line must always lie within the maximum current and breakdown voltage. In Figure 5.2, the two ellipses can not extends beyond I_{max} or V_{CE_BR}. This can be guaranteed if both $R_{\text{LH}}^2 + X^2$ and $\frac{1}{G_{LL}^2 + B_M^2}$ are less than ${R_{opt}}^2$. With the restrictions, two arcs on Smith Chart (Figure 5.3) form a close loop that represents the load contour for a constant output power.

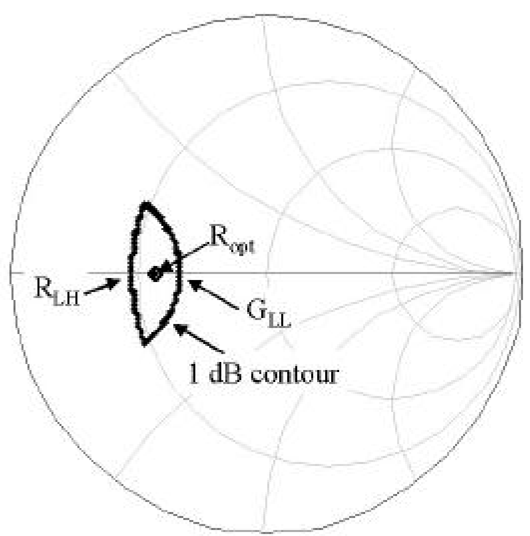


Figure 5.3: Load contour on Smith Chart

In power amplifier design, extrinsic parasitic elements of the transistor must be considered in designing for the correct load impedance. Given the transistor large signal model, the extrinsic parasitics can be included in the matching networks as shown in Figure 5.4. The loadline $R_{L,opt}$ must be presented to the *intrinsic* collector-emitter current, e.g. at the position of the voltmeter and ammeter in figure 4.19.

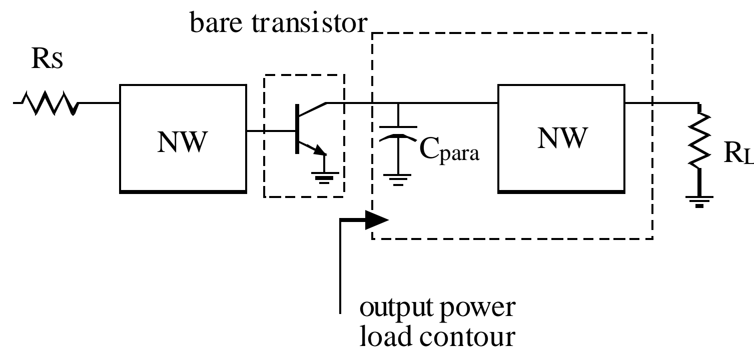


Figure 5.4: Load contour matching schematic

The design of Class-A power amplifier is, therefore, as follows. The output-matching network is designed to present the optimum load impedance to the intrinsic transistor. The input network is then designed to match the amplifier to the 50Ω source impedance. The design is then verified by harmonic balance simulations, checking linearity and output power. These simulations can also plot the dynamic load line. Figure 5.5 is an example.

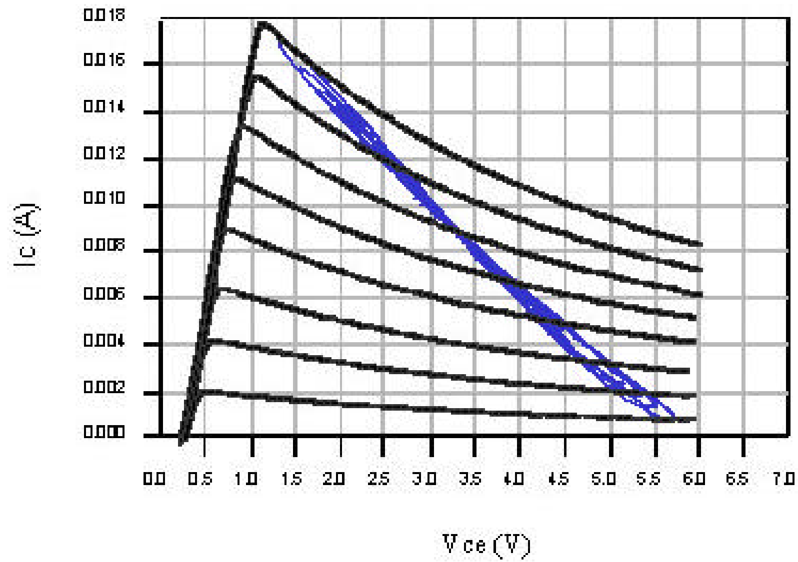


Figure 5.5: Harmonic simulated dynamic load line

5.2 HBT power amplifier topologies

HBT power amplifiers can be designed with different topologies based on the stages and the power combining architecture. Both thermal and low frequency circuit instabilities must be considered.

5.2.1 Single stage power amplifier

Single stage HBT power amplifiers are the simplest topology. Figure 5.6 shows the common emitter and common base single stage HBT power amplifiers.

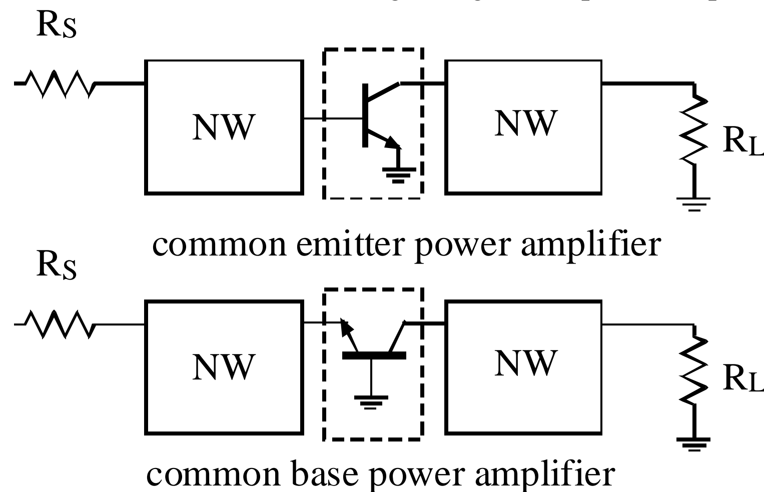


Figure 5.6: Single stage power amplifiers

To deliver high output power, the transistor is usually designed with lumped transistors, using a multiple finger structure, resulting in large emitter area. At high frequency, both the input and the output impedances of the transistor decrease substantially with the device size or the number of the fingers. Therefore the network Q at the input and output ports are high and it becomes difficult to design wideband-matching networks. A solution to this problem is to use a device pre-matching. This will be addressed subsequently.

The common base HBT has higher maximum stable power gain because of reduce device feedback. Also it is more straightforward to bias the common base configuration than the common emitter configuration under constant-emitter-current conditions, resulting in superior thermal stability. However, since the common base Rollette stability factor is usually less than unity at low frequencies, the power amplifiers must be designed for low frequency stability.

In most HBT technologies, ground vias through substrate introduce substantial inductance. This can causes electrical instability, particularly in common-base mode. In transferred-substrate technology, however, the inductive impedance related to ground vias through the 5μm BCB dielectric is substantially reduced. InP DHBT W-band common base power amplifiers have been developed and the results will be discussed in Section 5.3.

5.2.2 Multi-stage power amplifier

Multi-stage power amplifier consists of several cascaded single stage amplifiers. Figure 5.7 shows the schematic of a 2-stage power amplifier.

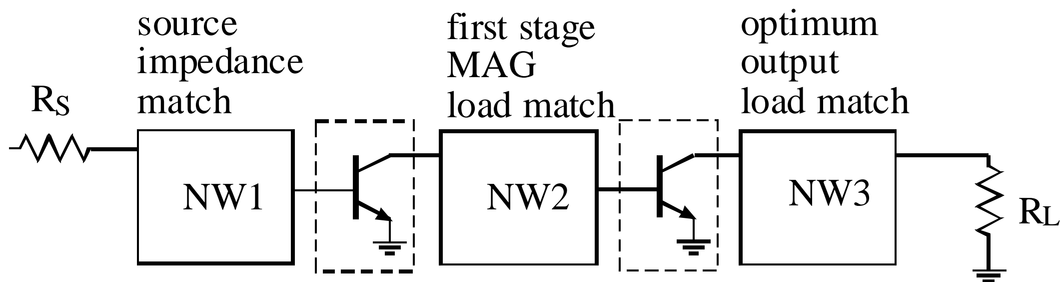


Figure 5.7: 2-stage power amplifier schematic

In multi-stage power amplifiers, the last stage is designed for the maximum output power. The loading of the intermediate stages is designed to provide some compromise between maximum gain and maximum saturated output power, and the first stage has its input matched to source impedance. In this way, the total power gain of the multi-stage power amplifier can be increased substantially.

There are two main considerations in the multi-stage power amplifier design. The first consideration is power gain compression. In Figure 5.8, the first stage is designed for its maximum power gain but has low saturated output power. If the compressed output power of the first stage is within the input linear power range of the final stage, the amplifier chain will show gain compression at power levels well

below saturation. This is illustrated in Figure 5.8. Therefore, in multi-stage power amplifier design, although the front stages are designed for high gain, their power performance must also be checked to prevent gain compression of the cascaded amplifier chain. Examination of the load line of the intermediate stage design allows one to easily make trade-offs between gain and output power.

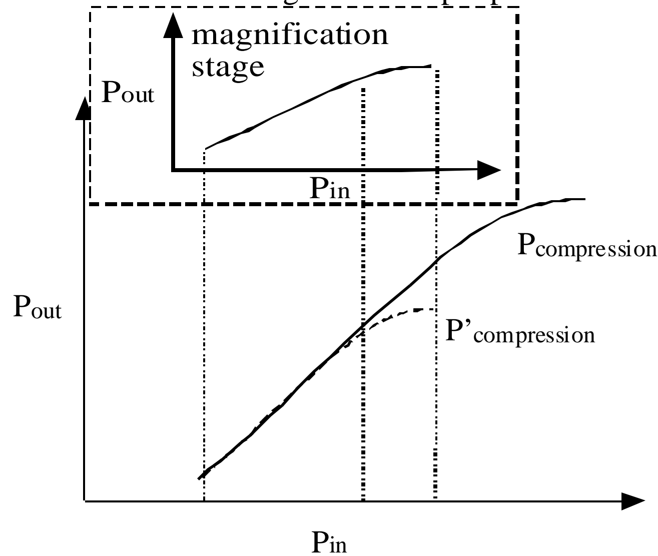


Figure 5.8: Gain compression in multi-stage power amplifier

The second design consideration is intermediate stage stability. The 2-port stability factors (K and B) of the cascaded amplifier are not sufficient to ensure that the amplifier is immune from low frequency oscillations caused by the bias circuitry [49] [50]. Stability simulations from DC to f_{max}, using the bias insertion ports as the RF ports (Figure 5.9), are required for to check for unconditional stability.

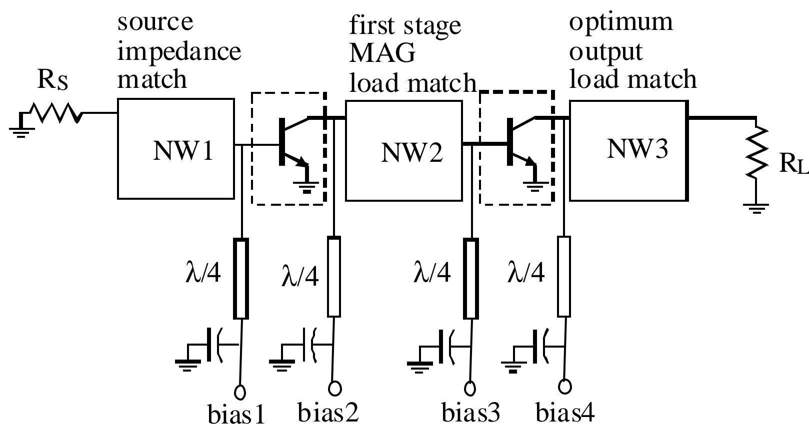


Figure 5.9: Low frequency stability factor simulations of a two stage power amplifier

5.2.3 Cascode power amplifier

A cascode power amplifier (Figure 5.10 (a)) is composed of cascaded common emitter input stage and common base power stage [51]. With the collector connected to the emitter of the common base stage, the common emitter stage takes the same dynamic current as that of the common base stage, while the collector voltage of the common emitter stage can be chosen separately. By Eqn. 3.21, thermal stability factor of HBT is strongly dependent upon the collector-emitter bias voltage. Because the common emitter stage is biased with a low collector voltage, the necessary emitter ballast resistance can be reduced. Therefore, although the common base stage dissipates higher power, the current distribution that flows through the two stages is determined by the thermal stability of the common emitter stage, provided that individual connections are provided [52] between the collector fingers of the common-emitter device and the emitter fingers of the common-base device (fig 5.10 (c)).

At high frequency, the power gain of cascode power amplifier can be reduced by the nonzero impedance base by-pass capacitor of the common base stage. At high frequencies, the MIM capacitor has significant series parasitic inductance and can no longer be treated as an ideal capacitor. This substantially reduces the power gain of the amplifier at higher frequencies.

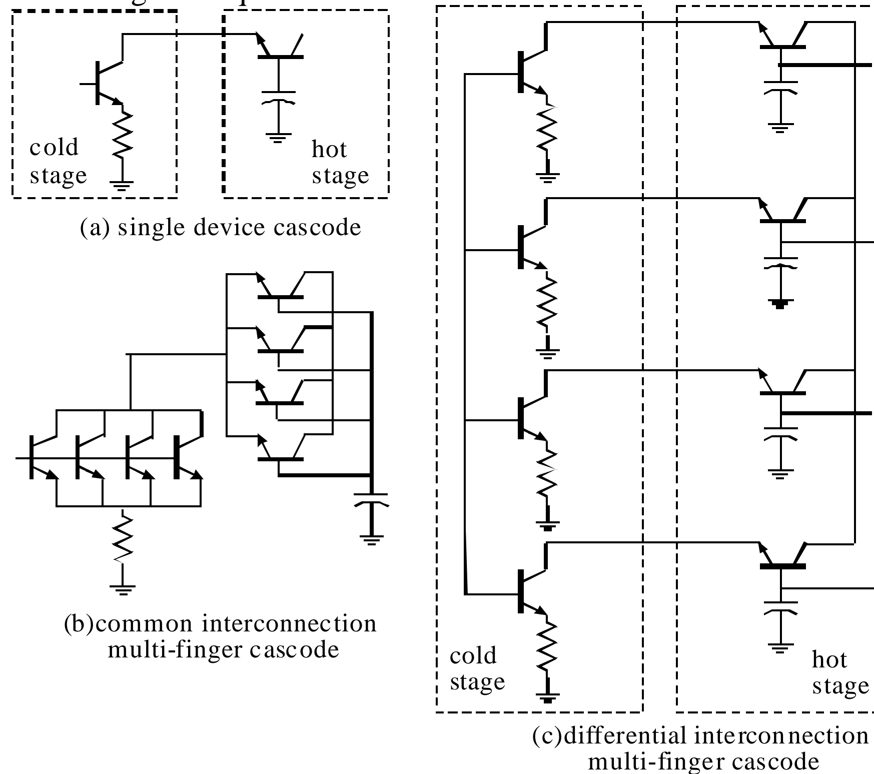


Figure 5.10: Cascode power amplifier architecture schematics

5.2.4 Balanced power amplifier

The design of power amplifier for maximum output power usually results in high VSWR at the output. The balanced power amplifier (Figure 5.11) suppresses this high VSWR through use of a combination of a 3-dB Wilkinson power combiner and quarter-wave phasing sections. The reflected output power is thus absorbed in the termination. In addition to the wideband input and output match, this balanced power amplifier has the advantages of 3-dB increased output power and improved low frequency stability [48]. The quarter-wave transmission line of Wilkinson power combiner can be designed as impedance transformer with characteristic impedance Z_{Wilk}, as part of the power amplifier load matching network, and the balanced resistor can thereby be designed with the value of $(Z_{Wilk}^2/25)\ \Omega$ [42]. The Wilkinson balanced power amplifier is widely used MMIC technology, where microstrip lines are used in the Wilkinson power combiner. At high frequencies the power combiner can introduce significant power loss. A DHBT W-band balanced power amplifier in transferred-substrate technology was fabricated but demonstrated poor saturated output power for this reason. This result will be presented in Section 5.3.

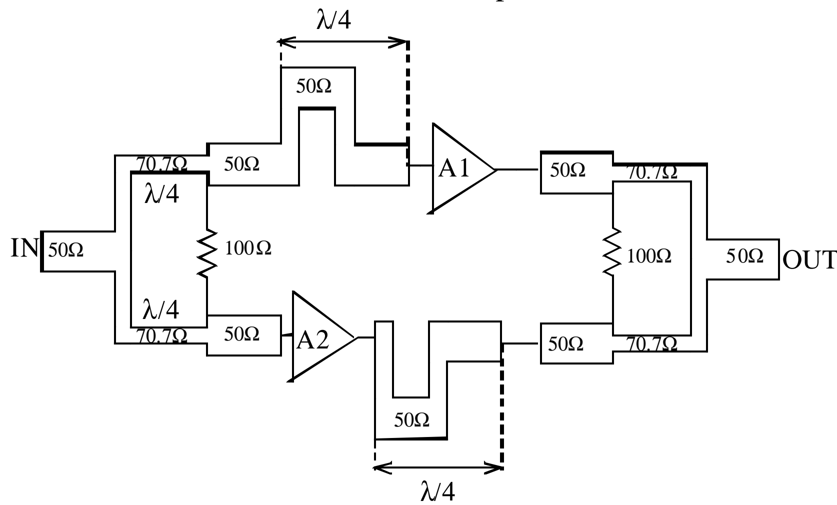


Figure 5.11: Balanced power amplifier with Wilkinson power combiner

5.3 InP DHBT Power amplifiers in transferred-substrate technology

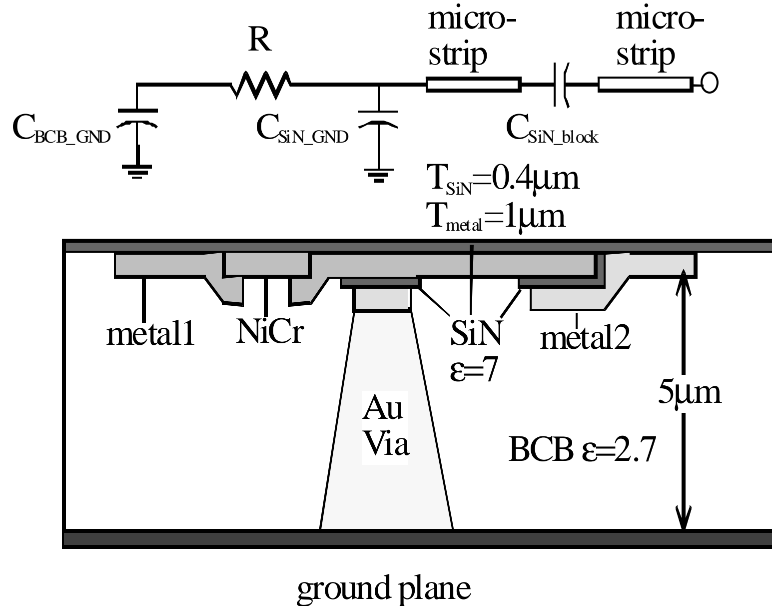


Figure 5.12: Cross-section of passive circuits in transferred-substrate MMIC technology

The fabrication of transferred-substrate DHBT has been introduced in Chapter 4. Figure 5.12 shows the wiring environment and the passive circuit cross-section in transferred-substrate MMIC technology.

The microstrip lines in transferred-substrate MMIC are realized by 1µm thick Au conductors and a 5 µm thick polymer dielectric (BCB), whose relative dielectric constant is 2.7. Resistors are fabricated using a 0.03 µm thick NiCr thin film with sheet resistance of 30 Ω/square. 0.4 µm thick PECVD-deposited SiN is used as the electrical insulator and capacitor dielectric material (ε_r=7). Therefore, there are two types of MIM capacitor available in UCSB transferred-substrate MMICs (Figure 5.12). Capacitors with SiN capacitor and metal-1 and metal-2 electrodes can be used for either DC blocking (C_{SiN_block}) or for bypass capacitors (C_{SiN_GND}) grounded through gold via. Capacitors can also be formed using with BCB dielectric (C_{BCB_GND}), with metal-1 and the ground plane as the two plates. The capacitance per unit area of the SiN capacitors is 32 times that of the BCB capacitor, an advantage in MIMIC layout. But the thickness of the SiN dielectric has a process variability of approximately 10%, which is 10:1 poorer than that of the BCB capacitor. Therefore SiN capacitors are used in realizing large AC bypass capacitors, as these need not be precisely controlled. Die area is thus reduced. Large area capacitors which are part of the tuning networks, on the contrary, must have tightly controlled capacitance. A solution to this problem is to paralleling these two capacitor types, whose values are appropriately partitioned, trading off the die area and the variation tolerance. For example, a large composite capacitor with C_{BCB}=2C_{SiN} will have a 3% process

variation while consuming 30% of the die area compared to using a single BCB capacitor.

The InP transferred-substrate power amplifiers are designed with two multiple finger unit cells as in Figure 4.8 and Figure 4.11. These exhibit high bandwidth and high output power and have been well modeled. Each multiple finger device consists of 4 emitter and collector fingers with emitter spacing of 7 μm. Each emitter finger has a contact size of 1 μm × 16 μm and the corresponding collector area is 2 μm × 20 μm. Larger size devices can be realized by parallel connection of several 4-finger unit cells. This device architecture is chosen for two reasons. First, the low input and output impedances of each unit cell are pre-matched through their interconnecting microstrip lines. This eases the design of amplifier's matching networks. Second, by reducing the size of the multiple finger transistor to 4 fingers, reduced lengths are obtained for the wires interconnecting emitter and collector fingers within the multiple finger cell. This is a key advantage in computer-aided design, as layout parasitics within the multiple finger cell are electrically significant yet difficult to model with finite-element CAD tools. The longer wires connecting the two 4-finger cells into an 8 finger transistor are microstrip lines with negligible line coupling, and are readily and accurately modeled.

5.3.1 40 GHz cascode power amplifier

Ka-band power amplifiers have been widely used in satellite communication systems, wireless LANs, local multi-point distribution systems, personal communication network links, and digital radio.

The schematic of a 40 GHz power amplifier in transferred-substrate technology is shown in Figure 5.13. The amplifier is designed in the cascode topology, taking advantage of the DHBT's high breakdown voltage. In this thermally stable Cascode configuration, stability against current hogging by a single emitter finger is ensured with less emitter ballasting than is required for a common-base HBT operating at the same collector bias voltage. Emitter ballast resistance, nevertheless, significantly reduces gain. Gain degradation due to parasitic layout impedance of the base bypass capacitor is another major difficulty in cascode amplifier design. Even a small parasitic inductance in the bypass capacitor results in a significant reduction in gain.

The 40 GHz power amplifier employs two parallel multiple finger cascode cells. Each multiple finger cascode consists of 4 emitter and 4 collector fingers. Each emitter finger has a contact size of 1 μm × 16 μm and the corresponding collector area is 2 × 20 μm^2. An 8 Ω ballast resistor is connected to each emitter finger of the common emitter stage to ensure thermal stability. The amplifier was designed using the methodology in section 5.1.

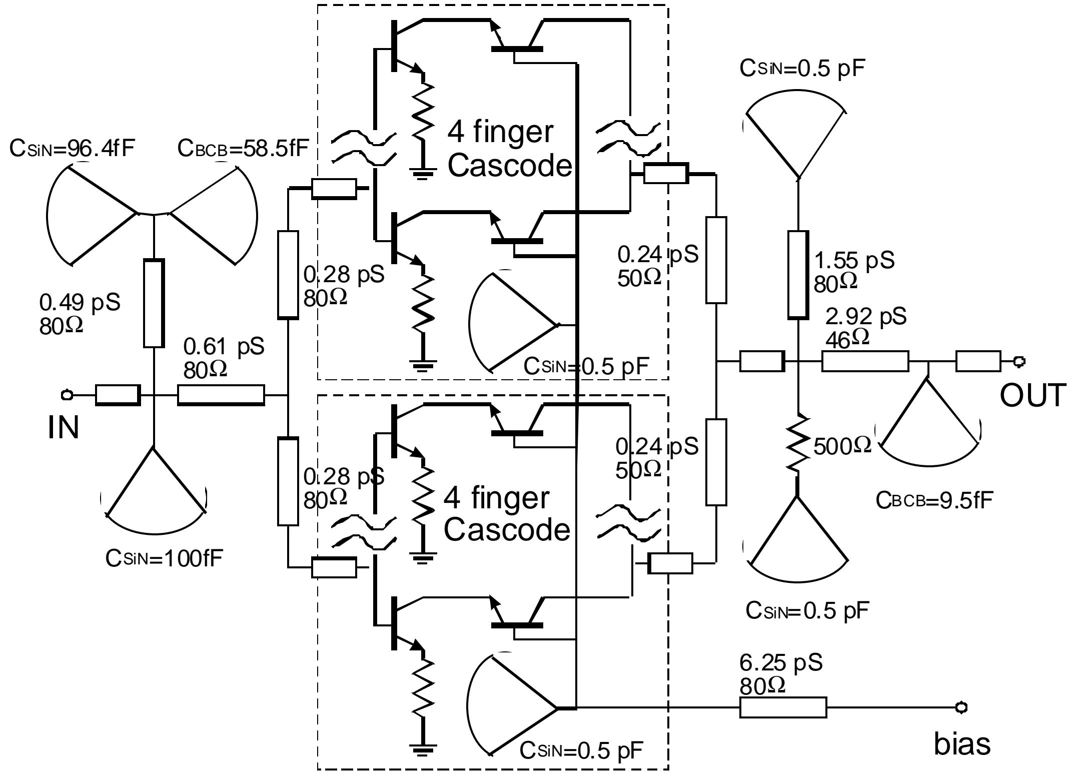


Figure 5.13: 40 GHz power amplifier schematic

The input network matches the transistor to 50 Ω using an inductive microstrip line and MIM radial stub capacitors. A large shunt AC-grounded resistor connected to the cascode output provides unconditional stability. In the output-matching network, a shunt AC–grounded inductive microstrip line compensates the HBT output parasitic susceptance arising from the base-collector capacitance, and a low-impedance transformer converts the 50 Ohm load to the HBT optimum load impedance, for Class-A bias condition,

$$R_{opt} = (V_{CE,\max} - V_{CE,sat}) / I_{C,\max} = 41\ \Omega \ . \tag{5.3}$$

The maximum DHBT current $I_{C,max}$ is 128 mA and the saturation voltage $V_{CE,sat}$ is 1.2 V. The maximum collector emitter voltage $V_{CE,max}$ is chosen to be 6.5 V, a voltage less than the breakdown voltage, to avoid risk of device destruction. Therefore, the expected Class-A saturated output power is approximately:

$$P_{\max} = I_{\max}(V_{CE,\max} - V_{CE,sat})/8 = 80\ \text{mW} \ . \tag{5.4}$$

Figure 5.14 shows the simulations of the small signal performance of the power amplifier. At 40 GHz, the designed amplifier has a power gain of 11 dB and less than –10 dB input return loss.

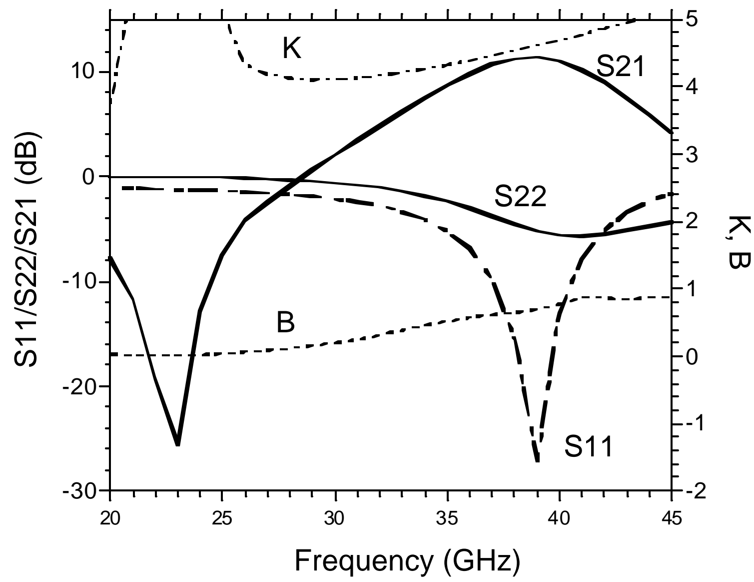


Figure 5.14: S-parameter simulation of power amplifier

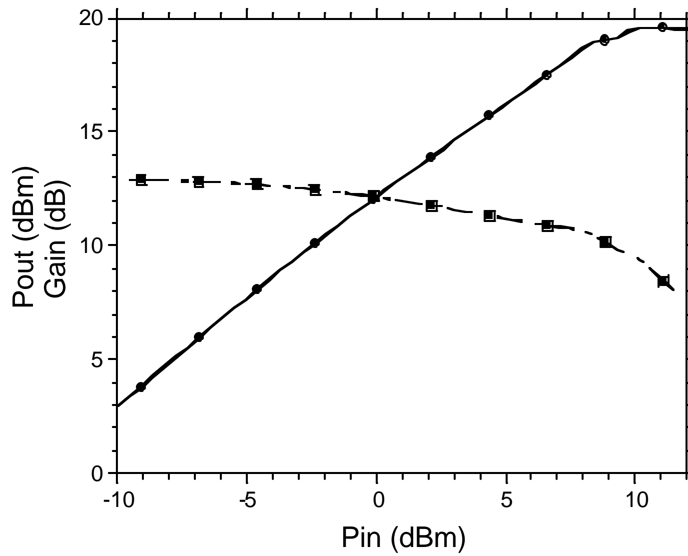


Figure 5.15: Harmonic balance simulation at 40 GHz

Using the harmonic balance simulator of ADS, the power performance is simulated. The power amplifier demonstrates 19 dBm (80 mW) saturated output power (Figure 5.15).

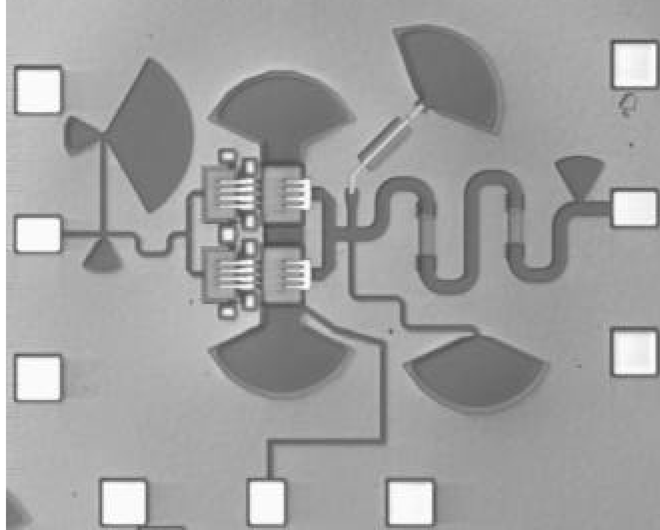


Figure 5.16: Die photograph of 40 GHz power amplifier

Figure 5.16 shows the die photograph of the 40 GHz power amplifier. The die size is 0.7 mm × 0.6 mm. The small signal measurements of the amplifier were performed using an HP8150 network analyzer with on-wafer TRL calibration. Output power was measured using micro-coaxial wafer probes. Reported power measurements include corrections for the calibrated attenuation of bias tees, probes, and cables. The circuit is biased at 80 mA collector current, V_{CE} =3.5 V for the common-base device, and V_{CE} =1.5 Volts for the common emitter stage. Hence the total power supply is 5V. Figure 5.17 shows the small-signal S-parameter measurements. The small-signal power gain is 6.8 dB. The input return loss is less than –20 dB and the output return loss is less than -6 dB. Low output return loss is not expected in single stage power amplifiers, unless the balanced configuration is employed. The 3-dB bandwidth of S_{21} is 16 GHz.

Figure 5.18 shows output power measurement results at 40 GHz. The output power at 1-dB gain compression point is 14 dBm, while the saturated output power is 17 dBm with a corresponding 4 dB gain. The peak power added efficiency is 12.5% when the amplifier is operating close to full power saturation.

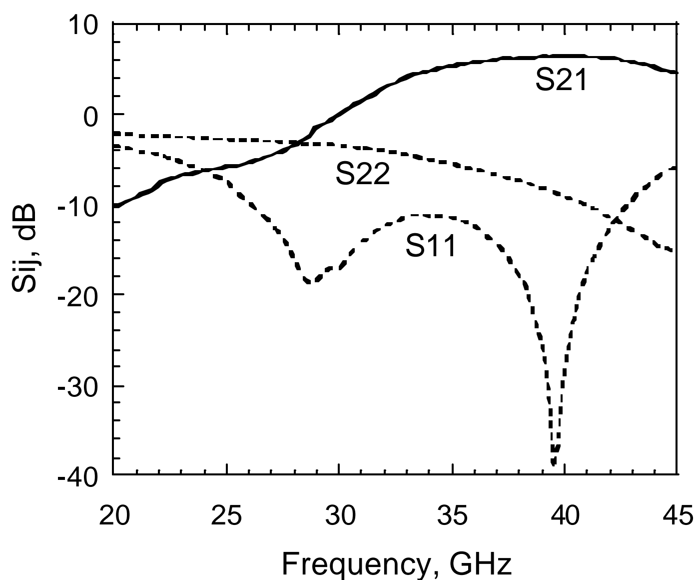


Figure 5.17: Measured v-band S-parameters

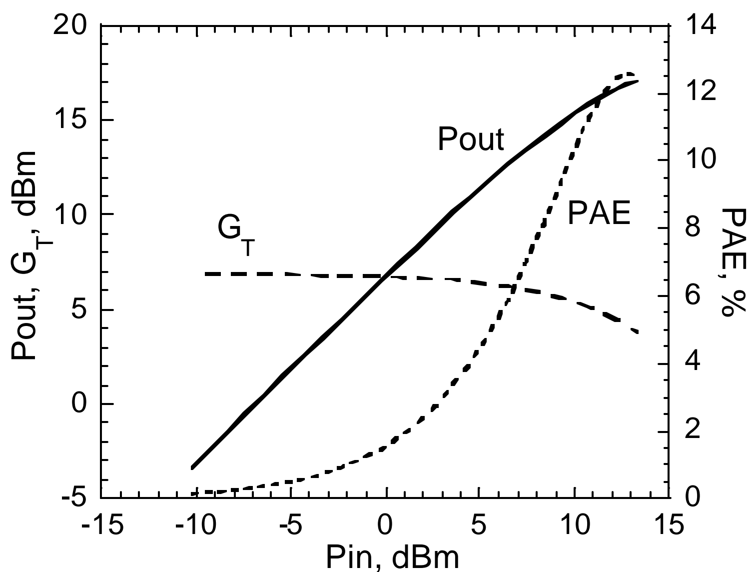


Figure 5.18: Measured output power at 40 GHz

5.3.2 94 GHz cascode power amplifier

The 94 GHz cascode power amplifier is designed for the quasi-optic phase array driver. The amplifier employs only a single 4-finger cascode cell with the same size and emitter ballasting as that of the 40 GHz cascode power amplifier. The schematic is shown in Figure 5.19.

In Figure 5.19, the amplifier is designed for high gain with moderate output power. The design is intended for use in a balanced power amplifier. The output

network is designed for the maximum available power gain. The network comprises of a shunt inductive stub and a quarter-wave transformer. The input is matched for the 50 Ω source impedance using a T-section tuning network. A 500 Ω AC grounded resistor is shunted at the output to ensure low frequency stability. The common base stage is biased using a quarter wave high impedance microstrip transmission line.

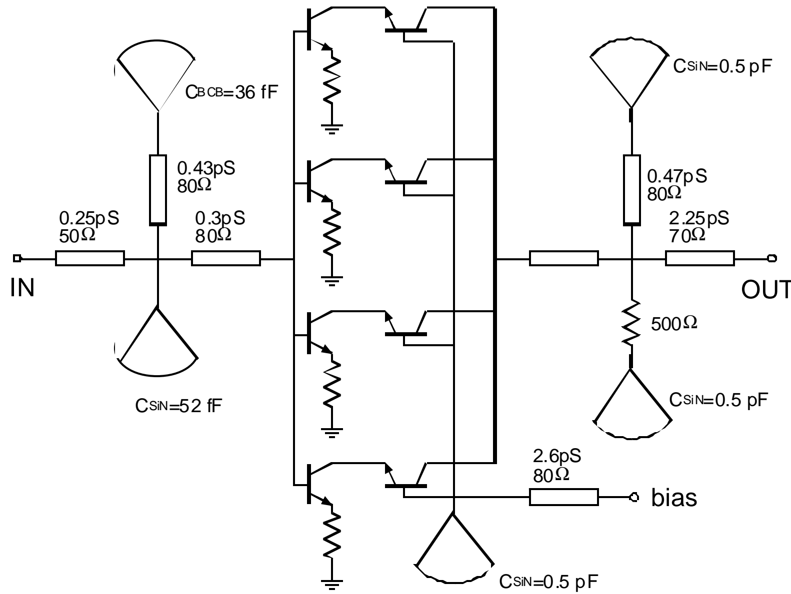


Figure 5.19: Schematic of 94 GHz cascode power amplifier

The small signal simulation of the 94 GHz power amplifier is shown in Figure 5.20 with unconditional stability and fairly low return loss at each port.

The simulated power performance of the amplifier (Figure 5.21) shows 9 dB gain and 15 dBm saturated output power. Figure 5.22 shows the simulated dynamic load line of one collector finger of the common base stage. The load is matched with a small parallel inductive susceptance without additional tuning required.

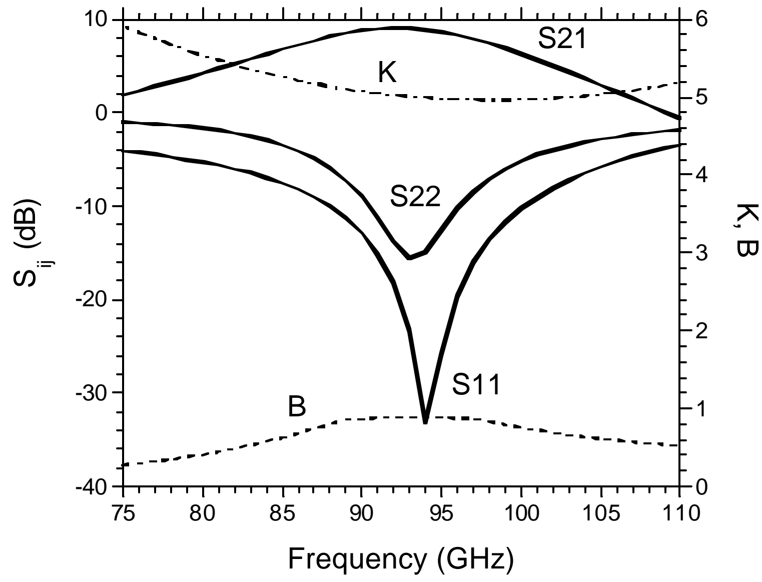


Figure 5.20: S-parameter simulation of 94 GHz cascode power amplifier

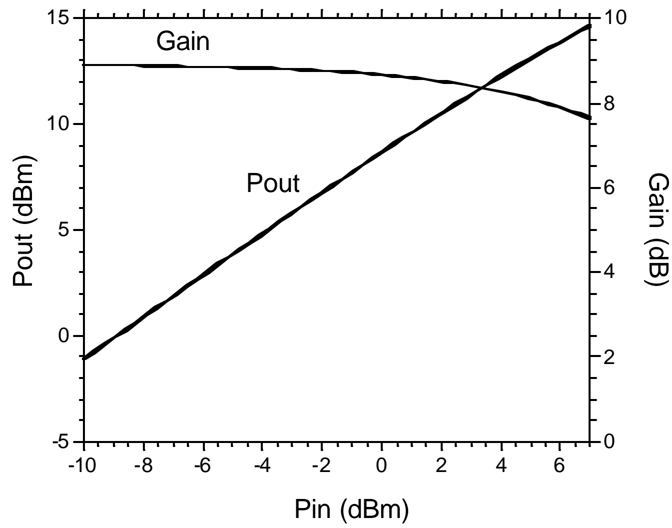


Figure 5.21: Harmonic balance simulation at 94 GHz

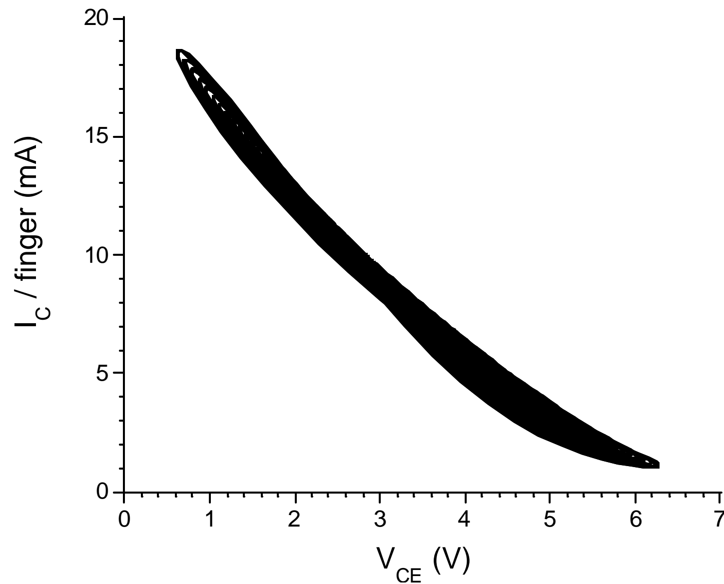


Figure 5.22: Dynamic load line simulation at 94 GHz on a single finger of the common base stage

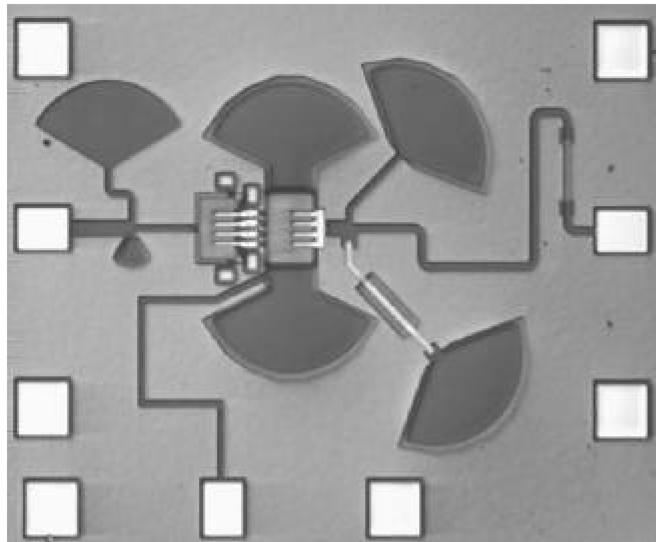


Figure 5.23: Die photograph of 94 GHz cascode power amplifier

Figure 5.23 shows a die photograph. The die size is 0.5 mm × 0.4 mm. The W-band small signal S-parameters are measured when the device is biased for maximum power gain (Figure 5.24). Figure 5.25 shows the measured output power when the common base stage is biased at I_C =40 mA and V_{CE} =3.5 V, with the common emitter stage biased at V_{CE} =1.2 V.

The measured S-parameters shown in Figure 5.24 are consistent with the simulation except that the measured resonant frequency low by 4 GHz. The 3-dB

bandwidth is 20 GHz. The amplifier has an insertion power gain of 8.6 dB and the 1-dB gain compression output power is 9.5 dBm. The saturated output power is 12.5 dBm with a corresponding 4 dB gain. Although electromagnetic simulations (using Agilent MOMENTUM) of individual elements were performed, E&M analysis of the whole network was not performed for this design. Such electromagnetic passive element simulations have proved essential for good agreement between circuit simulation and measurement.

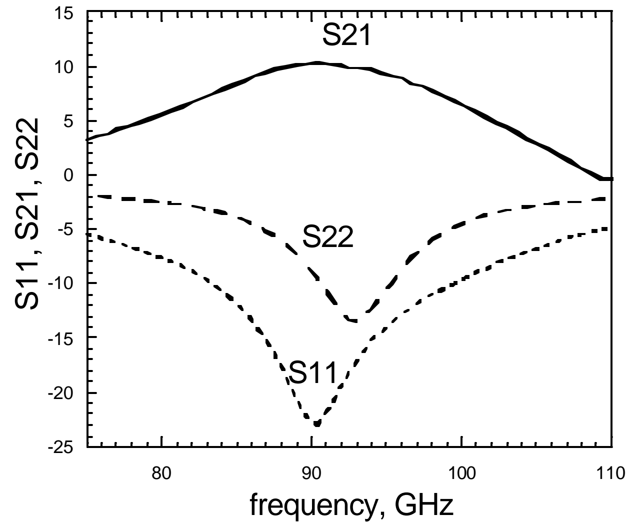


Figure 5.24: Measured w-band S-parameters

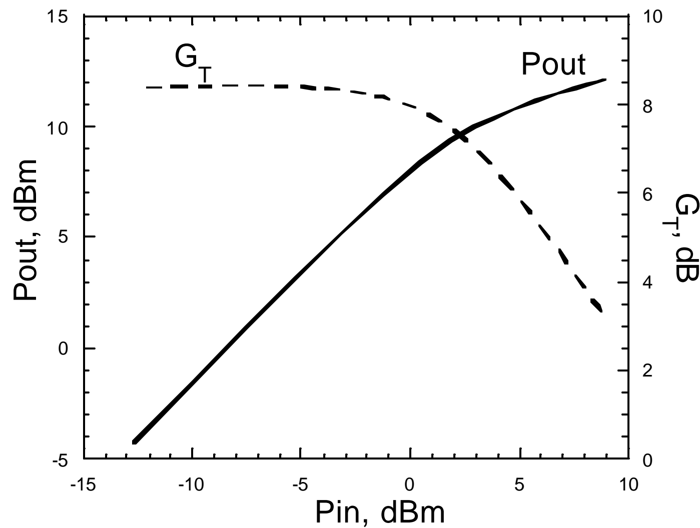


Figure 5.25: Measured output power at 90 GHz

5.3.3 85 GHz common base power amplifier

A 94 GHz common-base power amplifier was designed (Figure 5.26) using 2 parallel 4-finger power DHBT cells, forming a composite 8-finger device with 128 μm^2 emitter junction area. The microstrip line interconnections are designed to pre-match the very low impedances at both input and output ports of each cell. The output tuning network is designed for the optimal output load of the 8-finger DHBT, comprising two cascaded Π-sections. At the design frequency, the output tuning network loads the HBT in the optimum admittance for saturated output power as $Y_{L,opt} = G_L + jB_L$, where the load susceptance $B_L = -\omega C_{cb}$ compensates for the HBT output capacitance and $G_L = I_{c,\max} / (V_{CE\max} - V_{CE,sat})$ is the optimum load conductance. With design values of $V_{CE,\max}$ =6.1 V, $V_{CE,sat}$ = 1.1 V, and $I_{C,\max}$ =128 mA, G_L is 1/40 Ω^{-1} and the expected saturated output power is

$$P_{sat} = I_{C,\max} (V_{CE,\max} - V_{CE,sat}) / 8 = 80 \text{ mW} . \tag{5.5}$$

The input is matched to 50 Ω with T-section networks, incorporating shunt composite capacitor strategy. A 500 Ω AC grounded resistor is shunted at the output to ensure low frequency stability.

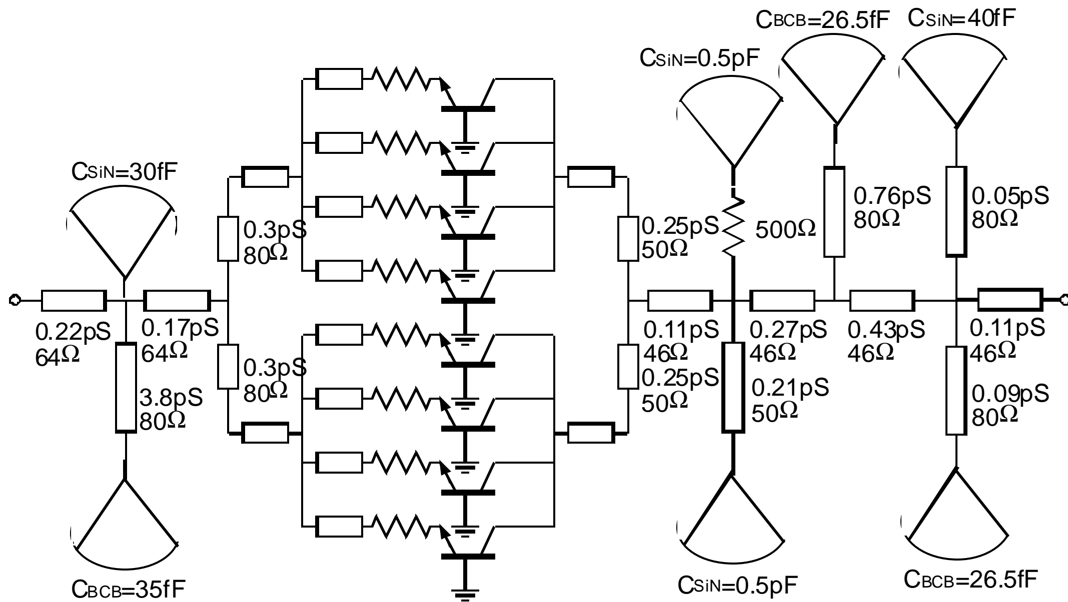


Figure 5.26: 94 GHz common base power amplifier schematic

The amplifier's simulated W-band S-parameters (Figure 5.27) and power performance at 94 GHz (Figure 5.28) show broad bandwidth and 80 mW saturated output power.

Figure 5.29 is the die photograph of the common base power amplifier with a die size of 0.5 mm × 0.4 mm. Figure 5.30 and Figure 5.31 are the plots of the small signal and power measurement results respectively.

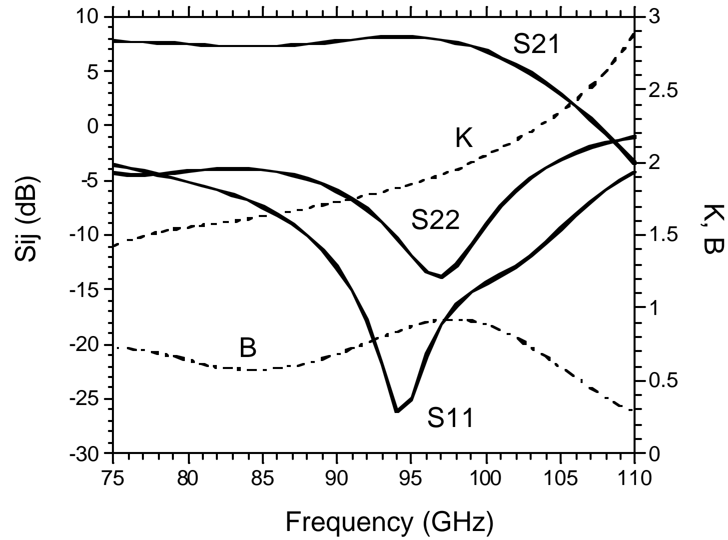


Figure 5.27: S-parameter simulation of common base amplifier

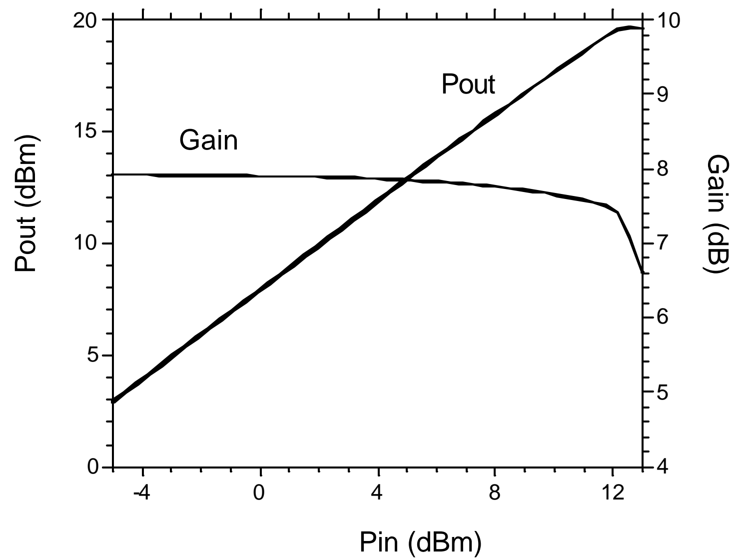


Figure 5.28: Harmonic balance simulation at 94 GHz

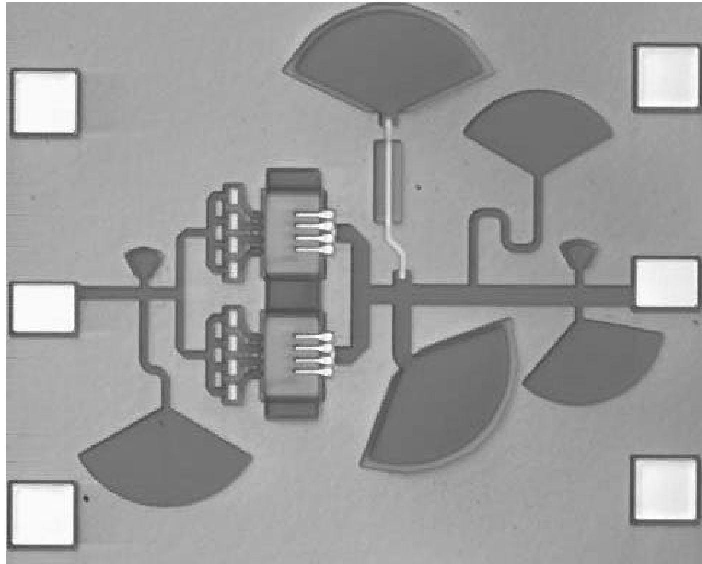


Figure 5.29: Die photograph of common-base amplifier

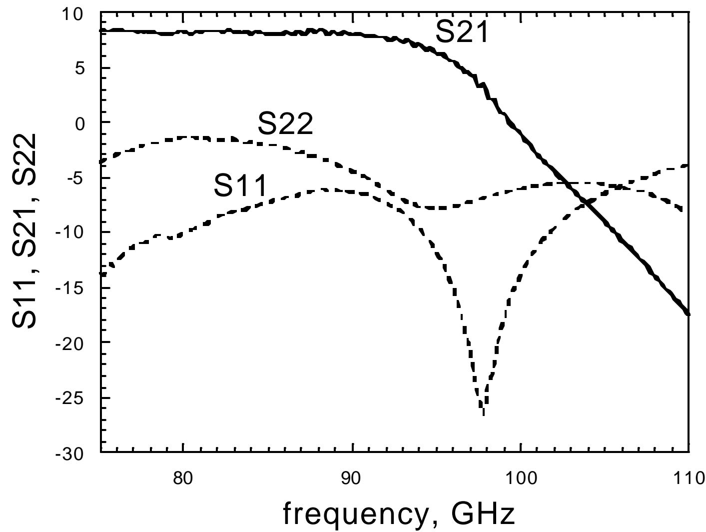


Figure 5.30: Measured W-band S-parameters

The device is biased at I_c=78 mA and V_{ce}=3.6 V. The measurements (Figure 5.30) show a constant 8 dB power gain below 90 GHz. The 3-dB gain bandwidth is 20 GHz. The amplifier's maximum saturated output power is obtained at 85 GHz, 9 GHz below the designed 94 GHz. The resonant shift is due to the process variation during the MMIC fabrication. In Figure 5.26, the input T-network includes a 3.8 ps high-impedance microstrip line terminated with 35 fF BCB capacitor. The center frequency of this tuning network is very sensitive to the values of its element, and contributes to measured amplifier center frequency. The amplifier exhibits 8.5 dB

insertion gain at 85 GHz and the 1 dB gain compression output power is 14 dBm. The saturated output power is 16.2 dBm (42 mW) with a corresponding gain of 4.6 dB.

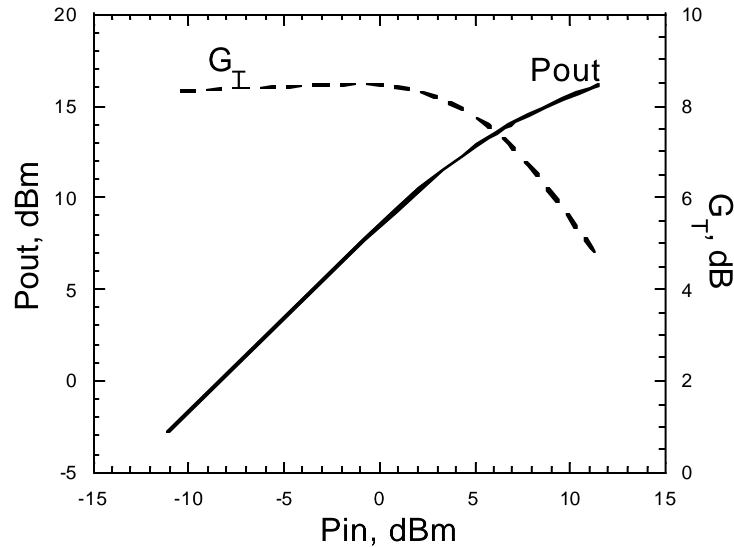


Figure 5.31: Measured output power at 85 GHz

5.3.4 75 GHz LDE power amplifier

To achieve higher output power, DHBTs with larger emitter area must be employed. Figure 5.32 is the schematic of a 16-finger common base W-band power amplifier, which comprises of four 4-finger common-base LDE DHBTs. The LDE DHBT is chosen because it is effective in suppressing current filamentation within the finger (Section 4.4). Table 4.2 is the layer structure of the LDE DHBT. The 4-finger common-base LDE DHBT has the same topology as that in Figure 4.11. For each $16\mu m^2$ emitter finger, the LDE layer provides 3.75 Ω resistance, while the emitter ohmic contact provides 1.25 Ω . A further 2.5 Ω external NiCr resistance is provided for each finger to force equal currents between fingers. The combination of ballast resistances in the LDE and NiCr layers reduces the degree of circuit performance variation from variation in the NiCr sheet resistance.

The input and output impedances decrease substantially with the number of DHBT fingers employed, hence the matching network design becomes more complex. Similar to the 85 GHz common base power amplifier design, the output network was designed to match the 20 Ω optimal pure resistive load. A Π network followed by a T-section with less than $\lambda/8$ length inductive arms compensates for the capacitive output admittance of the HBTs. The low impedance quarter wave microstrip line connecting between the transistor and the 50 Ω load is an impedance transformer. The long-arm input T-section with large bypass capacitors is designed

to synthesize low Q value LC network. The input is then matched to 50 Ω by a low impedance quarter wave transformer.

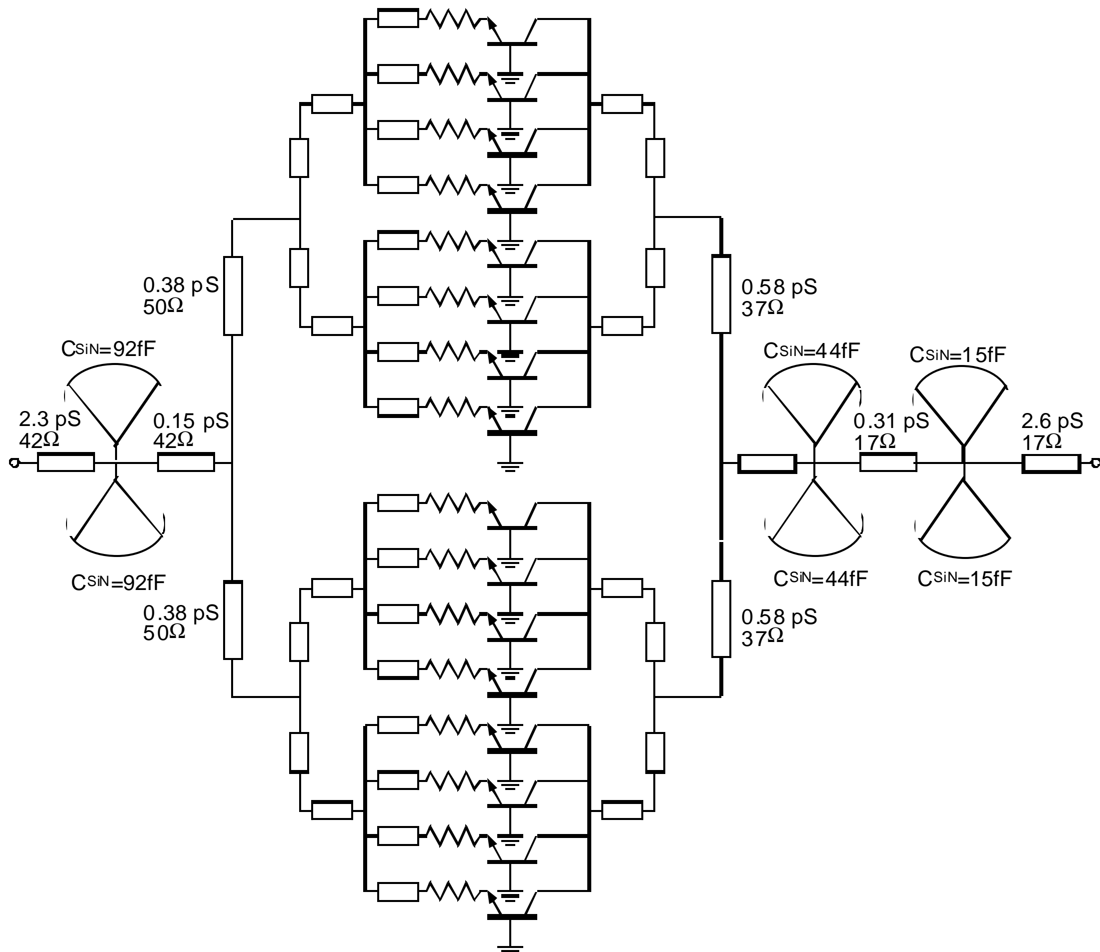


Figure 5.32: Schematic of l6-finger common base power amplifier

The power amplifier is designed to operate at 94 GHz. Small signal S-parameter and power simulations are shown in Figure 5.33 and Figure 5.34 respectively. Figure 5.35 is the die photograph of the power amplifier. The die size is 0.38 mm × 0.89 mm.

As shown in Figure 5.35, the (light-colored) input microstrip transmission line is composed of two layers of metal: metal1 and metal3, with Metal3 deposited in the process of collector contact evaporation. In this way, current handling ability of the narrow input transmission line is increased.

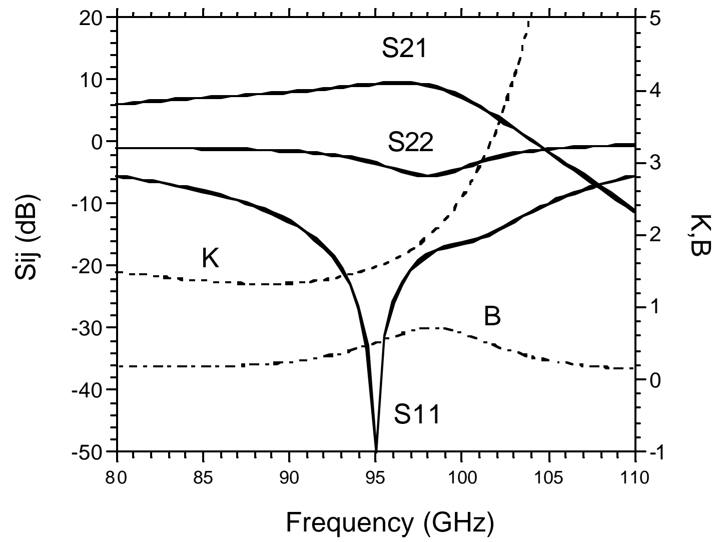


Figure 5.33: S-parameter simulation of 16-finger common base amplifier

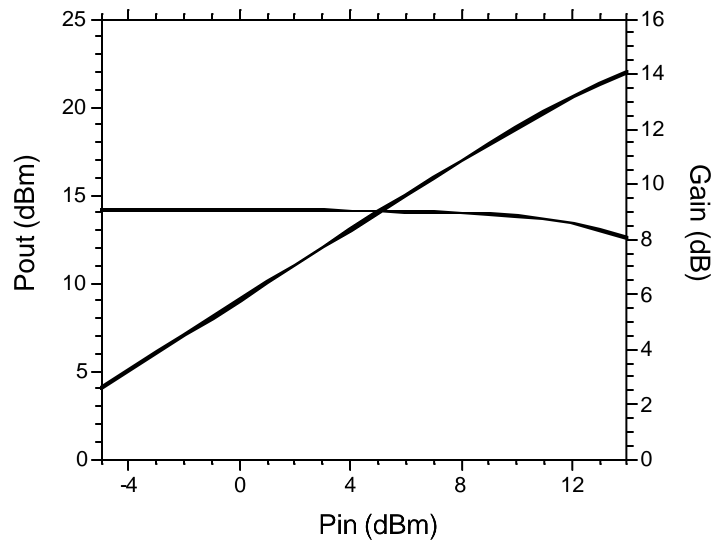


Figure 5.34: Harmonic balance simulation at 94 GHz

Figure 5.36 shows the measured small signal S-parameters in W-band. The plot shows 20 GHz resonant frequency shift from the design frequency and highly reduced power gain.

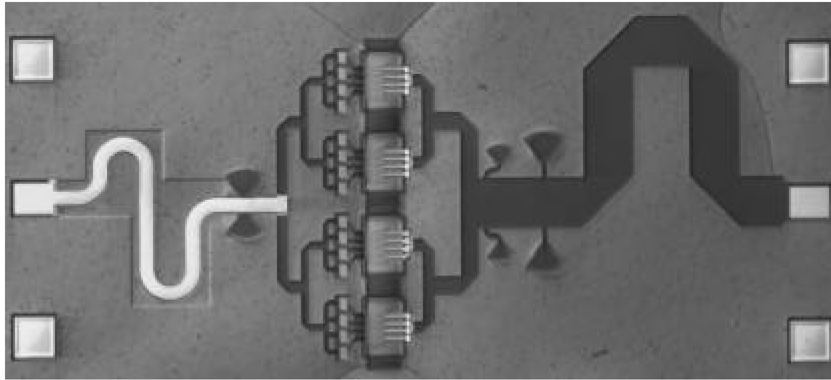


Figure 5.35: Die photograph of 16-finger common base power amplifier

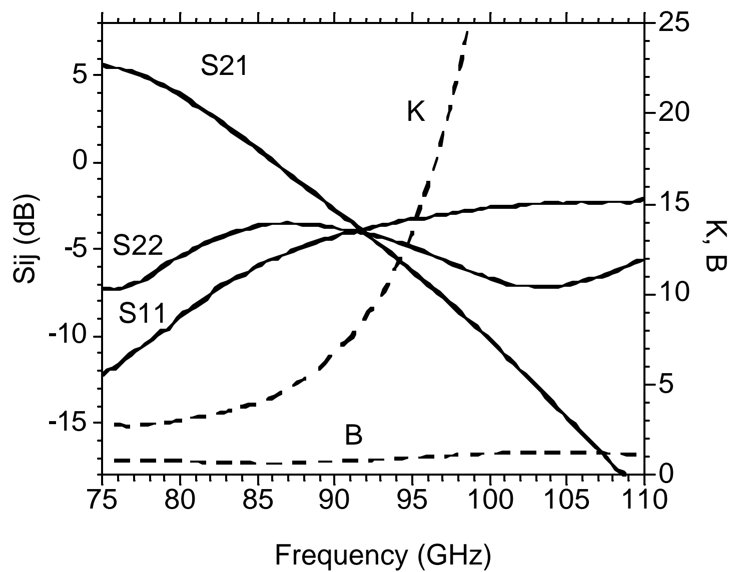


Figure 5.36: Measured W-band S-parameters

The large variations between the S-parameters and the measurements are due to the MMIC fabrication, in which the SiN film thickness is measured to be 15% larger than the design value. From Figure 5.32, it can be seen that SiN MIM capacitors are used as tuning bypass capacitors. Composite capacitors were not used because large value capacitors are required and BCB MIM capacitors with partitioned value will consume very large die areas. The matching networks, therefore, differ substantially from design, resulting in the measured resonant frequency shift.

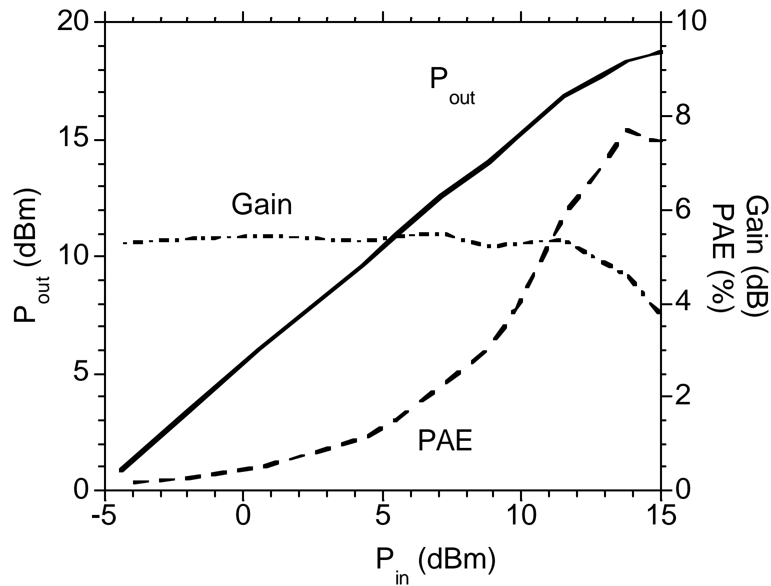


Figure 5.37: Measured output power at 75 GHz

A power measurement of the amplifier is performed at 75 GHz, which is plotted in Figure 5.31. The power amplifier is biased at 130 mA of I_C and 4.5 V of V_{CE}, exhibiting an 80 mW of 1-dB gain compression output power and a peak PAE of 8%.

5.3.5 Other W-band power amplifiers in transferred-substrate DHBT technology

Other W-band power amplifiers designed for higher output power and high gain were fabricated in this work. These amplifiers failed to function to design specification as a result of fabrication failures. These are discussed for reference.

32-finger common base power amplifier

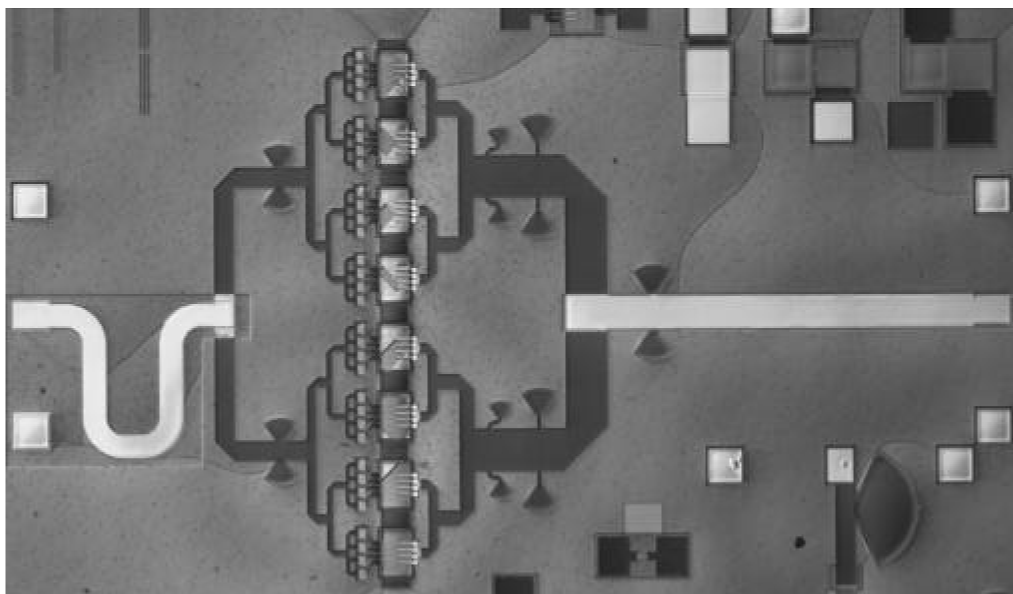


Figure 5.38: Die photograph of 32-finger common base power amplifier

Employing twice the number of DHBT fingers as that of the 16-finger common base amplifier, the 32-finger common base power amplifier cannot be designed by lumping devices in parallel. The impedance of simple lumping structure is so low that it is comparable to the series resistive loss impedance of the matching networks. The large susceptance at input and output makes W-band reactive tuning extremely difficult. Therefore the power amplifier is designed based on the 16-finger amplifier, maintaining the input and output reactive matching networks while using combiners only for pure resistance transformation. The simulation predicts 3-dB increased output power and the same insertion gain as that of the 16-finger common base power amplifier.

Figure 5.38 shows the die photograph of the 32-finger power amplifier, from which it can be seen that the collector mesa of most of the multiple finger transistors are damaged. Damage of the multiple finger devices is a process failure mechanism due to biaxial compression that was explained in detail in chapter 4. Although new layer structure was used to reduce this compression, for large devices that are regularly arranged, the compression of each device extends and joins with the others'. The accumulated strain damages the collector protection layer during substrate removal. A solution to this problem is to irregularly arrange the multiple finger devices so that the extension of the compression is interrupted to avoid protection layer breaking.

16-finger W-band common base power amplifier

A two-stage 16-finger W-band common base power amplifier was also designed for the purpose of increasing the insertion gain of the amplifier. The input of the

second stage is matched to the optimal output load of the first stage and a SiN MIM block capacitor is inserted for DC blocking. The amplifier is designed to double the power gain while maintaining the same saturated output power as that of the 16-finger power amplifier. Figure 5.39 is the die photograph of this power amplifier.

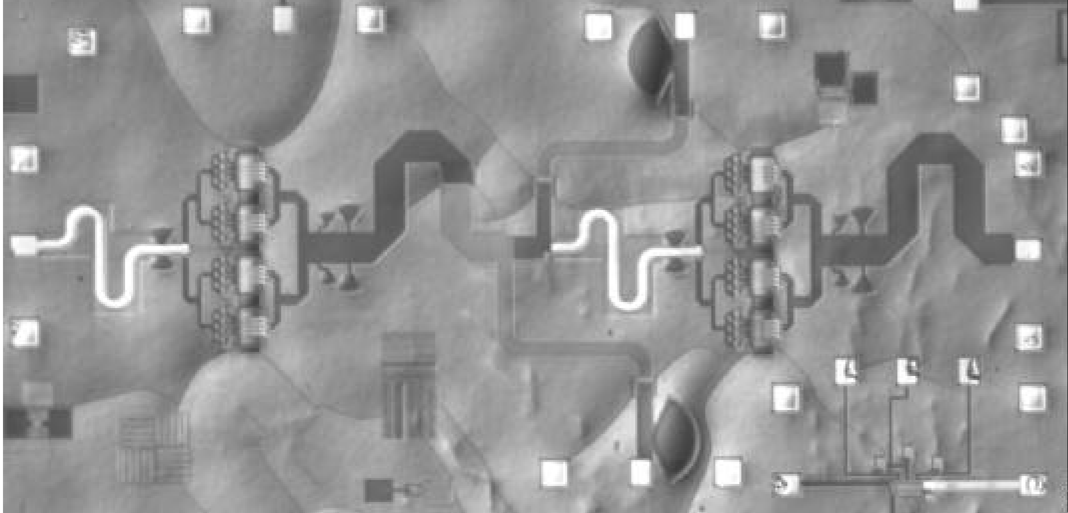


Figure 5.39: Die photograph of two stages 16-finger common base power amplifier

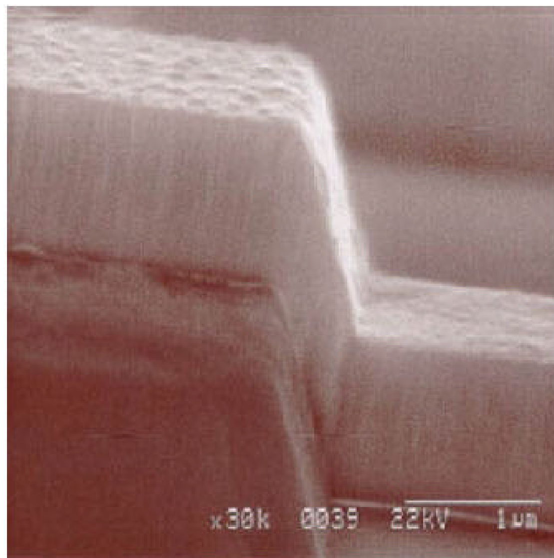


Figure 5.40: SEM photograph demonstrating thinner metal ramp

The two inter-stage bias isolation inductors are realized through quarter wave microstrip lines terminated with blocking capacitors and the 0.5 fF decoupling radial stub capacitor at the bias port. The quarter wave microstrip lines are composed of both metal 1 and metal 2, interconnected by the via through the SiN insulator, which can introduce another fabrication failure mechanism. The interconnection metal has

a thickness of 1 μm and a width of 20 μm, which is enough to carry the bias current. Unfortunately the metal ramp over the SiN edge is of reduce metal thickness due the angle of evaporation. This is illustrated in Figure 5.40. The thin metal layer cannot carry the amplifier bias current and is destroyed during testing.

Balanced power amplifier

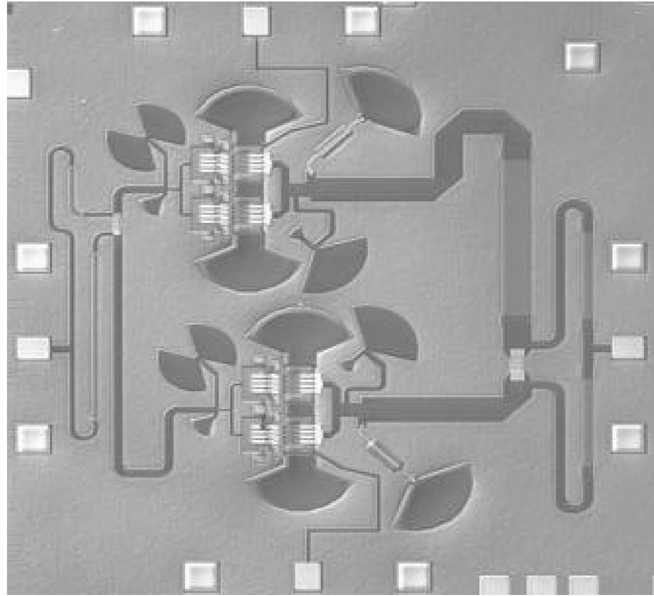


Figure 5.41: Die photograph of W-band balanced power amplifier

A W-band balanced power amplifier is designed for achieving high power high linearity and wide band matching. This is composed of two 8-finger pre-matched cascode cells whose outputs are combined using a Wilkinson power combiner. Figure 5.41 is the die photograph of the amplifier.

The balanced power amplifiers failed due to short-circuits from the emitter to ground. The mechanism of this failure mode has been discussed in [53]. A new transferred-substrate technology with an additional patterned intrinsic Si evaporation on the emitter region has been developed that substantially improves the yield of DHBT MMICs. This new process is attached in the appendix.

5.4 Conclusions

InP DHBT transferred-substrate technology has been successfully applied in realizing millimeter wave power amplifiers with record output power. Applications of the millimeter wave power amplifiers include automotive and military radar, wireless networks, and mm-wave communications. The DHBT technology thus exhibits high power density and high linearity that is comparable with state-of-the-art submicron PHEMTs.

Chapter 6

Conclusion

6.1 Achievements

In this work, multi-finger InGaAs/InAlAs/InP DHBTs were designed and characterized. Both power-combining parasitics and thermal characteristics are essential factors in developing high-power mm-wave transistors. A systematic strategy to improve the thermal stability and bandwidth has been developed in this work. Large-junction-area InP DHBTs were designed and fabricated using transferred-substrate technology. A DHBT with emitter area of 128 μm^2 exhibited f_{max} of 330GHz when measured at 100 mA collector bias current and 3.6V collector-emitter bias voltage. By adding a lightly doped epitaxial (LDE) layer between the emitter and the emitter contact layer, a differential ballast scheme is designed and employed that significantly improves the thermal stability of large area HBTs. Long finger LDE InP DHBTs in transferred-substrate technology were fabricated, demonstrating f_{max} of 235 GHz when biased with 140 mA current and 3.7V collector-emitter voltage.

A multiple finger HBT large signal model was developed in this work for the simulation of thermal and electrical coupling effects. The model was based on a standard Gummel-Poon Model and showed good agreement with measurement results.

InP DHBT millimeter-wave power amplifiers with record levels of output power were designed and fabricated. Reactively matched common-base amplifier MMICs, with 8.5 dB insertion gain at 85 GHz, delivered saturated output power of 16.6 dBm. A cascode amplifier demonstrated an insertion gain of 8.6 dB and saturated output power of 12.5 dBm at 90 GHz. Other reactively matched common-base amplifiers with the LDE layer structure demonstrated 80 mW saturated output power at 75GHz.

In this work, an antenna array process utilizing gold electroplating was developed [Appendix]. The process is compatible with the transferred-substrate DHBT technology, and a number of antennas were fabricated and integrated with on-wafer passive elements. The antennas were designed for 94 GHz operation, and showed best impedance match at 100 GHz.

6.2 Future Work

Although transferred-substrate HBT technology has been improved since its first demonstration, low device yield still prevents the development of larger scale MMICs. Sources of device failures include: 1) electrical short circuits between the interconnect metals in regions near emitter contacts; 2) epitaxial shrinkage after flip-chip bonding; 3) failures of emitter contact formation by lift-off; 4) collector damage during substrate removal. Solutions to the first two problems have been obtained. By inserting a 0.2µm thick intrinsic Si film between metal layers, electrical short circuits are prevented. Epitaxial shrinkage was eliminated by substituting an AlN carrier substrate for the GaN substrate earlier used. This reduces by an order of magnitude the dimensional variation after substrate transfer. Although the emitter liftoff failures do not significantly impact HBTs with one-micron emitter widths, high yield submicron devices will require advances in self-aligned base emitter junction fabrication. The fourth problem is caused by semiconductor material biaxial compression. Although new layer structures have been used that can effectively reduce this compression for small devices, for large devices that are closely arranged, the compression of each device can accumulate and extend in the direction with biaxial compression. This strain may cause damage to the collector protection layer during the substrate removal. This failure mechanism has been observed in fabrication of high power multiple finger HBTs. A solution to this problem might be to intentionally misalign the multiple finger devices in the X-axis, so as to break the accumulation of the compression in the Y-direction.

Near the time of the end of this work, mesa InP-DHBTs with f_{max} above 400 GHz have been developed at UCSB. These devices demonstrated twice the achievable current density of the transferred-substrate DHBTs because of superior thermal characteristics. Multiple finger power HBTs can thus be designed and fabricated using the same methods as for transferred-substrate power HBTs, and with which, wideband HBT high power amplifiers can be developed.

Using either transferred-substrate technology or new mesa-DHBTs, the antenna array spatial power combiners can be fabricated and can be integrated with the wideband power amplifiers to realize efficient high-power amplifiers.

Reference

[1] R. Grundbacher, R. Lai, M. Barskey, Y. C. Chen, R. Tsai, R. M. Dia, L. Tran, T. P. Chin, T. Block, A. Oki, "A. 0.1 μm enhancement-mode pseudomorphic InGaAs/InAlAs/InP HEMT," *International Conference on Indium Phosphide and Related Materials, IEEE.* p.180-3. Piscataway, NJ (2001)

[2] H. Wang; L. Samoska, T. Gaier, A. Peralta, H Liao, Y. C. Leong, S. Weinreb, Y. C. Chen, M. Nishimoto, R. Lai, "Power-amplifier modules covering 70-113 GHz using MMICs," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 49, p. 9-16, Boston, MA (2001)

[3] Y. C. Chen, D. L. Ingram, R. Lai, M. Barsky, R. Grunbacher, T. Block, H. C. Yen, D. C. Streit, "A 95-GHz InP HEMT MMIC amplifier with 427-mW power output," *IEEE Microwave and Guided Wave Letters*, vol. 8, p. 399-401 (1998)

[4] M. Rodwell, et al, "Submicron Lateral Scaling of Vertical-Transport Devices: Transferred-Substrate Bipolar Transistors and Schottky Collector Tunnel Diodes." *Proc. o OSA Topical Meeting on Ultrafast Electronics and Optoelectronics*, p. 192-193 Incline Village, Nevada (1997)

[5] Q. Lee, S. C. Martin, D. Mensa, R. P. Smith, J. Guthrie, and M.J.W. Rodwell, "Submicron Transferred-Substrate Heterojunction Bipolar Transistors." *IEEE Electron Device Letters,* Vol. 20, No. 8. p. 396-398 (1999)

[6] Q. Lee, S. C. Martin, D. Mensa, R. P. Smith, J. Guthrie, S. Jaganathan, T. Mathew, S. Krishnan, S. Creran, M. Rodwell, "Submicron transferred-substrate heterojunction bipolar transistors with greater than 8000 GHz f_{max}," *International Conference on Indium Phosphide and Related Materials, IEEE*, p.175-8. Piscataway, New Jersey (1999)

[7] T. Morf, S. Hubschuer, D. Huber, A. Huber, V. Schwarz, H. Jackel, "98 GHz InP/InAsGas HBT Amplifier with 26 dB gain", *IEEE Trans. Microwave and Guided Wave Lett.*, Vol. 9, No. 12, p. 523-525 (1999)

[8] J. R. Guthrie, M. Urteaga, D. Scott, D. Mensa, T. Mathew, Q. Lee, S. Krishnan, S. Jaganathan, Y. Betser, M. Rodwell, "HBT MMIC 75 GHz and 78 GHz power amplifiers." *Proceedings of 2000 International Conference on Indium Phosphide and Related Materials*, p.246-2499, Piscataway, New Jersey (2000)

[9] M. Urteaga, D. Scott, S. Krishnan, Y. Wei, M. Dahlstrom, S. Lee, M.J.W. Rodwell, "Multi-stage G-band (140-220 GHz) InP HBT Amplifiers." *GaAs IC Symposium*, Monterey, California, Oct. 20-23 (2002)

[10] S. Lee, H. J. Kim, M. Urteaga, S. Krishnan, Y. Wei, M. Dahlstrom and M. Rodwel, "Transferred-Substrate InP/InGaAs/InP Double Heterojunction Bipolar Transistors with f_{max}=425 GHz" *IEE Electronics Letters*, Vol. 37, No. 17, p. 1096-1098 (2001)

[11] M. W. Dvorak, C. R. Bolognesi, O. J. Pitts, S. P. Watkins, "300 GHz InP/GaAsSb/InP double HBTs with high current capability and BV_{CEO}>6 V," *IEEE Electron Device Letters*, vol. 22, (no. 8), p. 361-3 (2001)

[12] P. C. Grossman, "A physically based large signal HBT model with self heating and transit time effects," *IEEE MTT-S International Microwave Symposium Digest,* p. 233-6 vol. 1, New York (1991)

[13] P. Baureis, W. McKinley, D. Seitzer, "A new large signal model for heterojunction bipolar transistors including temperature effects," *Proceedings of the IEEE 1991 Custom Integrated Circuits Conference*, p. 231-4, New York (1991)

[14] M. Rodwell, M. Urteaga, D. Mensa, Q. Lee, J. Guthrie, Y. Betser, S. Martin, R. Smith, S. Jaganathan, T. Mathew, P. Krishnan, S. Long, R. Pullela, B. Agarwal, U. Bhattacharya, L. Samoska, D. Scott, M. Dahlstrom, "Submicron Scaling of HBTs," *IEEE Transactions on Electron Devices,* Vol. 48, No. 11, p. 2606-2624 (2001)

[15] M.J.Rodwell, M. Urteaga, Y. Betser, D. Scott, M. Dahlstrom, S. Lee, S. Krishnan, T. Mathew. S. Jaganathan. Y. Wei, D. Mensa, J. Guthrie, R. Pullela, Q. Lee, B. Agarwal, U. Bhattacharya, S. Long "Scaling of InGaAs/InAlAs HBTs for high speed mixed-signal and mm-wave ICs," *International Journal of High Speed Electronics and Systems*, Vol. 11, No. 1, p. 159-215 (2001)

[16] Q. Lee, B. Agarwal, R. Pullela, D. Mensa, J. Guthrie, L. Samoska, and M.J.W. Rodwell, "A > 400 GHz f_{max} Transferred-Substrate Heterojunction Bipolar Transistor IC Technology." *IEEE Electron Device Letters*, Vol 19, No. 3, p. 77-79 (1997)

[17] Kirk, C.T., "A theory of transistor cutoff frequency falloff at high current densities." IRE Trans. Electronics. Dev. 9, p. 164-174 (1962)

[18] W. Liu, "Handbook of III-V hetero-junction bipolar transistors", *A Wiley-Interscience publication*, ISBN 0-471-249041 (1998)

[19] W. R. McKinnon, R. Driad, S. P. McAlister, A. Renaud, Z. R. Wasilewski, "Temperature independent current blocking due to hot electrons in InAlAs/InGaAs double heterojunction bipolar transistors with composite collectors," *Journal of Vacuum Science & Technology (Vacuum, Surfaces, and Films)*, Vol. 16, (No.2), Ottawa, Canada (1997)

[20] W. Liu, "Failure mechanism in AlGaAs/GaAs hetero-junction bipolar transistors", *IEEE Trans. Electron Devices*, vol.43, No. 2, p. 220 -227 (1996)

[21] J. R. Waldrop, K. C. Wang, P. M. Asbeck, "Determination of junction temperature in AlGaAs/GaAs heterojunction bipolar transistors by electrical measurement," *IEEE Transactions on Electron Devices*, Vol. 39, (No. 5), p.1248-50 (1992)

[22] S. Tiwari, S. L. Wright, A. W. Kleinsasser, 'Transport and related properties of (Ga, Al)As/GaAs double heterostructure bipolar junction transistors," *IEEE Transactions on Electron Devices*, Vol. ED-34, (No. 2, pt. 1), p. 185-98 (1987)

[23] H. Kroemer, "Heterostructure bipolar transistors: what shall we build?" *J.Vac.Sci.Technol.B*, Vol. 1, p. 126-130 (1983)

[24] R. P. Arnold, D. S. Zoroglu, "A quantitative study of emitter ballasting," *IEEE Trans. Electron Devices*, Vol. ED-21, p. 385-391 (1974)

[25] J. R. Waldrop, E. A. Kraut, C. W. Farley, R. W. Grant, "Measurement of InP/$In_{0.53}Ga_{0.47}As$ and $In_{0.53}Ga_{0.47}As$/$In_{0.52}Al_{0.48}As$ heterojunction band offsets by X-ray photoemission spectroscopy," *Journal of Applied Physics*, Vol. 69, (No. 1), p. 372-8 (1991)

[26] W. Liu, S. Nelson, D. G. Hill, A. Khatibzadeh, "Current gain collapse in microwave multi-finger hetero-junction bipolar transistors operated at very high power densities", *IEEE Trans. Electron Devices*, vol.40, No.11 (1993)

[27] A. Benvenuti, W. M. Coughrau, M. R. Pinto, "A thermal-fully hydrodynamic model for semiconductor devices and applications to III-V HBT simulation," *IEEE Transactions on Electron Devices*, Vol. 44, No. 9, p. 1349-59 (1997)

[28] T. Peyretaillade, M. Perez, S. Mons, R. Sommet, Ph. Auxemery, J. C. Lalaurie, R. Quere, (Edited by: Koepf, G.A.) "A pulsed-measurement based electrothermal model of HBT with thermal stability prediction capabilities," *1997 IEEE MTT-S International Microwave Symposium Digest*, Vol. 3, p. 1515-18, New York (1997)

[29] E. Martins, J. W. Swart, M. Akpinar, I. Wolff, "A new thermal model for HBT RF circuit simulation," *1997 SBMO/IEEE MTT-S International Microwave and Optoelectronics Conference*, Vol.2, pp.526-30 New York (1997)

[30] S. Tanaka, Y. Amamiya, S. Murakami, H. Shimawaki, N. Goto, Y. Takayama, K. Honjo, "Design considerations for millimeter-wave power HBT's based on gain performance analysis". *IEEE Trans. Electron Devices*, vol.45, No.1, p.36-44 (1998)

[31] Y. Zhu, J. K. Twynam, M. Yagura, M. Hasegawa, T. Hasegawa, Y. Eguchi, Y. Amano, E. Suematsu, K. Sakuno, N. Matsumoto, H. Sato, N. Hashizume, "Self-heating effect compensation in HBTs and its analysis and simulatiuon," *IEEE Trans. Electron Devices*, vol.48, No.11, p. 2640-2646 (2001)

[32] C. Y. Chu, "ESD performance optimization of ballasted resistor on power AlGaAs/GaAs hetero-junction bipolar transistor technology", *Electrical Overstress/Electrostatic Discharge Symposium Proceedings*, p.235-40, Orlando, Florida (1999)

[33] D. Mensa, Q. Lee, J. Guthrie, S. Jaganathan, and M.J.W. Rodwell, "Transferred-Substrate HBTs with 254 GHz *f*." *IEE Electronics Letters*, Vol. 35, No. 7, pp. 605-607 (1999)

[34] Y. Bester and D. Ritter, "Reduction of the base-collector capacitance in InP/GaInAs heterojunction bipolar transistors due to electron

velocity modulation," *IEEE Transactions on Electron Devices*, Vol. 46, No. 4, p. 628-33 (1999)

[35] R. Anholt, "Thermal impedance computations using realistic power dissipation profiles," *Proceedings of 1998 GaAs Reliability Workshop*, Atlanta, Georgia, Nov. 1998

[36] F. Dhondt, J. Barrette, P. A. Rolland, S. Delage, "3-D electrothermal model of multifinger, high-power HBTs," *1998 International Conference on Modeling and Simulation of Microsystems, Semiconductors, Sensors and Actuators.* p. 105-10. Cambridge, Massachusetts (1998)

[37] L. L. Liou, B. Bayraktaroglu, C. I. Huang, "Thermal runaway analysis of high power AlGaAs/GaAs heterojunction bipolar transistors," *IEEE/Cornell Conference on Advanced Concepts in High Speed Semiconductor Devices and Circuits*, p. 468-77, New York (1993)

[38] D. E. Dawson, A. K. Gupta, M. L. Salib, "CW measurement of HBT thermal resistance," *IEEE Transactions on Electron Devices*, Vol. 39, No. 10, p. 2235-9 (1992)

[39] C. C. McAndrew (Edited by: J. Jopke), "A complete and consistent electrical/thermal HBT model," *Proceedings of the 1992 BIPOLAR/BiCMOS Circuits and Technology Meeting*, p. 200-3, New York (1992)

[40] Q. M. Zhang, J. Hu, J. Sitch, R. K. Surridge, J. M. Xu (Edited by: Kuno, H.J.; Wen, C.P.), "A new large signal HBT model" *1994 IEEE MTT-S International Microwave Symposium Digest*, Vol. 2, p. 1253-6, New York (1994)

[41] M. Vaidyanathan, D. L. Pulfrey, "Extrapolated f_{max} of heterojunction bipolar transistors," *IEEE Transactions on Electron Devices*, Vol.46, No.2, p. 301-9 (1999)

[42] J. Guthrie, "HBTs on a copper-polymer substrate for aggressive wiring parasitic reduction, millimeter-wave amplifier ICs ," *Ph.D thesis*, University of California, Santa Barbara (2000)

[43] Y. Wei, S. Lee, K. Sundararajan, M. Dahlstrom, M. Urteaga, M. Rodwell, "W-band InP/InGaAs/InP DHBT MMIC Power

Amplifiers," *2002 IEEE MTT-S International Microwave Symposium Digest*, Vol.2, p. 917-20, Piscataway, New Jersey (2002)

[44] C. Nguyen, T. Liu, M. Chen, R. Virk, M. Chen, "Bandgap engineered InP-based power double heterojunction bipolar transistors", *1997 International Conference on Indium Phosphide and Related Materials*, p. 15-19, Cape Cod, Massachusetts (1997)

[45] J. Shrinivasan "8 Ghz clock rate oversampled Analog-digital converters, InP double heterojunction bipolar transistors," *Ph.D thesis*, University of California, Santa Barbara (2000)

[46] M. Rodwell, et al, "Submicron Lateral Scaling of Vertical-Transport Devices: Transferred-Substrate Bipolar Transistors and Schottky Collector Tunnel Diodes." *Proc. of OSA Topical Meeting on Ultrafast Electronics and Optoelectronics*, Incline Village, Nevada, p. 192-193 (1997)

[47] M. Chen, C. Nguyen, T. Liu, D. Rensch, "High-performance AlInAs/GaInAs/InP DHBT X-band power cell with InP emitter ballast resistor," *IEEE/Cornell Conference on Advanced Concepts in High Speed Semiconductor Devices and Circuits*, p. 573-82. New York (1995)

[48] S. C. Cripps, "RF Power Amplifiers for Wireless Communications", *Artech House, Inc.* ISBN: 0-89006-989-1 (1999)

[49] R. G. Freitag, " A Unified Analysis of MMIC Power Amplifier stability," *MTT-S International Microwave Symposium Digest* (1992)

[50] L. Samoska, K. Lin, H. Wang, Y. Chung, M. Aust, S. Weinreb, D. Dawson, " On the stability of millimeter-wave power amplifiers," *2002 IEEE MTT-S International Microwave Symposium Digest*, Vol. 1, p. 429-32, Piscataway, New Jersey (2002)

[51] R. Ramachandran and A.F. Podell, "Segmented cascode HBT for microwave-frequency power amplifiers", *U.S. Patent 5066926,* November 1991, Filed Jun. 26, 1990.

[52] B. Bayraktaroglu and M. Salib, "Unconditionally Thermally stable Cascode GaAs HBT's for Microwave Applications", *IEEE Microwave and Guidewd Wave Lett.*, Vol. 7, No. 7, p. 187-189 (1997)

[53] T Mathew, "High Speed HBT Digital ICs ," *Ph.D thesis*, University of California, Santa Barbara (2001)

[54] J. Yoon, etc. "Monolithic Fabrication of Electroplated Solenoid Inductors Using Three-Dimensional Photolithography of a Thick Photoresist", *Japanese Journal of Applied Physics*. Vol. 37, p. 7081-7085 (1998)

Appendix

Fabrication of 94 GHz antenna array in HBT technology

In Chapter 5, the design and fabrication of mid-power W-band power amplifiers in transferred-substrate DHBT technology has been presented. By using quasi-optical power combining technique, the output power of numerous W-band power amplifiers can be combined in free space. An integrated dipole antenna array is one method for spatial power combining. The dipole can be driven by single ended power amplifiers with balanced input signals. To avoid losses due to radiation into the dielectric substrate, an air-dielectric antenna has been designed for the spatial power combiner. Development of this process was also necessary for the integration of antennas into the transferred-substrate process, where the metal ground plane used in substrate bonding prevents radiation into the substrate, the mode of operation of most on-wafer antennas.

Figure A.6.1 shows the circuit diagram of the quasi-optical dipole antenna array integrated with amplifiers fed by an H-tree distribution network.

In this work, a process for fabrication of a 94 GHz antenna array has been developed by means of Au plating. In section 6.1, antenna arrays with different testing architectures are demonstrated. The dipole antenna process that is compatible with the MMIC transferred-substrate technology will be discussed in section 6.2. 94 GHz antenna arrays were fabricated with a microstrip Wilkinson power divider.

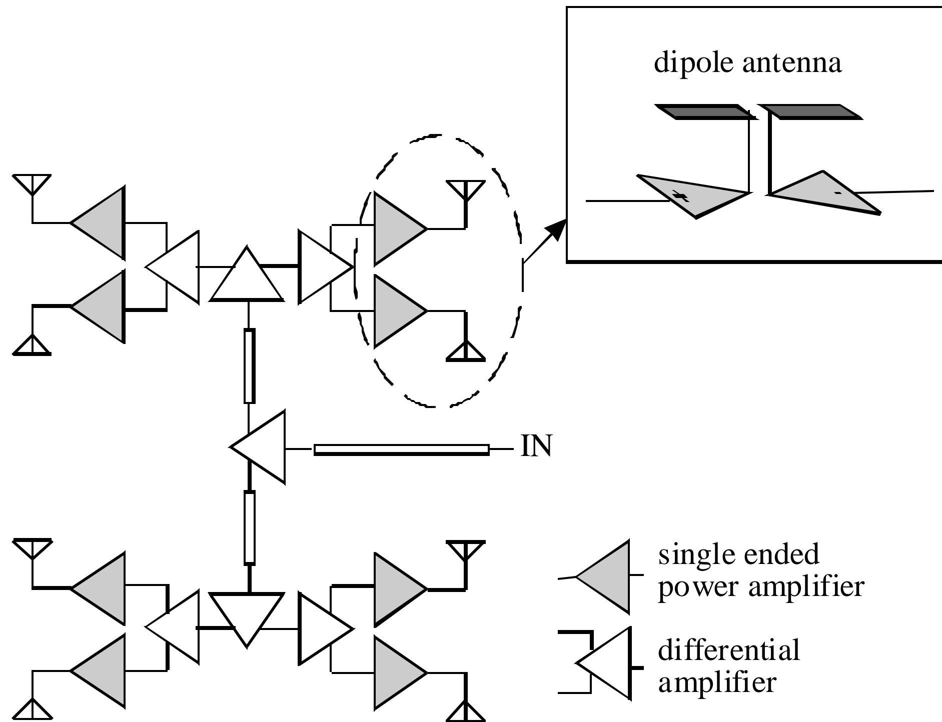


Figure A.6.1: Diagraph of dipole antenna array and amplifier H-tree

A.1 94 GHz antenna array fabrication

Air bridge processes have been widely used in the fabrication of mm-wave circuits. Air bridges can be formed by either metal evaporation or plating. Figure A.6.2 shows the SEM photograph of an Au plated Air Bridge. This structure is very similar to the dipole antenna we will later describe. Air bridges are usually less than 10 μm in height, while the antenna height must be much larger for effective radiation.

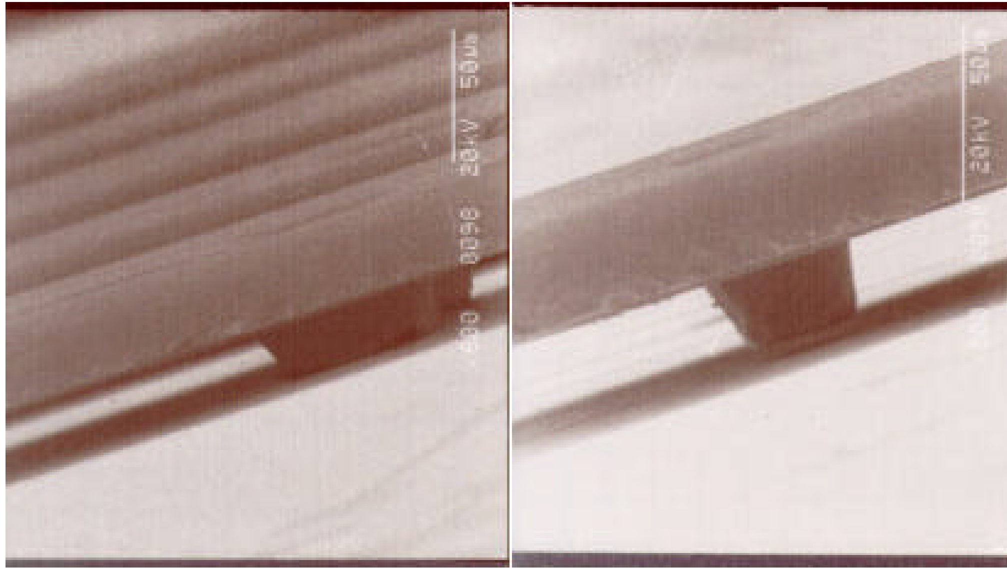


Figure A.6.2: SEM photograph of plated air bridge

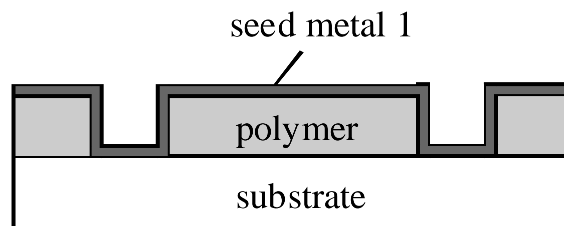
To realize an efficient antenna, the antenna must be a significant distance from the ground plane. Otherwise, induced currents in the ground plane, together with the surface impedance of conductors, will result in excessive resistive losses. Electromagnetic simulations by Prof. Rutledge's group at Caltech indicated that this height must be greater than 100 μm. Standard air bridge process therefore cannot be used. In [54], fabrication by air-bridge processes of on-wafer solenoid inductors of large diameters was reported. In this process, an 80 μm thick photoresist film is employed to form a plating mold. Since the post and the bridge are plated simultaneously, the surface of the bridge has a deep central dip profile and therefore is not suitable for antenna fabrication.

Based on the above air bridge technology, a millimeter wave antenna process has been developed. This process involves plating both posts with different seed metals. Hence, the height of the post and the thickness of the antenna can be controlled separately and a flat antenna top surface can be achieved. The process flow is shown in Figure A.6.3.

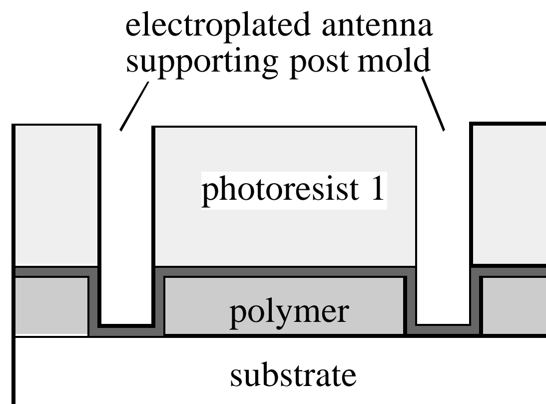
A.2 Process design

Three different photoresists are employed in this process. First, the polymer PMGI is spun onto the wafer, isolating the seed metal from the substrate. The resist is exposed by deep ultraviolet light, patterning the antenna pads. After 200°C curing, the PMGI layer has good thermal stability and demonstrates strong resistivity to most developers and acetone. Hence, PMGI is stable in the subsequent high temperature and developing process. The seed metal is composed of Ti/Au/Ti with thickness of 300Å/1100Å/300Å and is blanket deposited on the full wafer surface (Figure A.6.3 (a)). A plasma-sputtering deposition process provides a continuous flash layer. Ti is used to improve the adhesion of metal to photoresist.

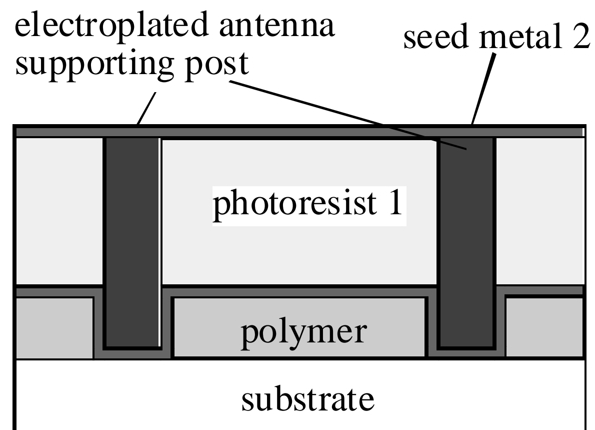
Very thick photoresist (photoresist 1 in Figure A.6.3(b)) is then applied on the flash layer. After multiple exposures at different focus offsets, the photoresist is developed to form the plating mold for the posts. The thick photoresist mold blocks the current flow in the electroplating path, so that only open regions are plated. The supporting posts are, thereby, plated up to the surface. The second seed metal is deposited for the antenna plating (Figure A.6.3 (c)). A third and thinner photoresist layer is then spun and patterned on the second flash layer (Figure A.6.3 (d)). The wafer is then again electroplated. Photoresists and flash layers are then removed from the wafer step by step. The top photoresist is flood exposed for a short time, avoiding the exposure of the thick photoresist underneath, and stripped away by the developer. The seed metal is then etched away by dipping the wafer into buffer HF and Au etchant respectively. Immersing in cold acetone removes the thick photoresist by slightly agitating and the PMGI remains un-attacked. After the final flash layer etching, the wafer is put into warm plastic stripper to dissolve the PMGI. Antenna process is finished by drying up the wafer on the hot plate at 50°C.



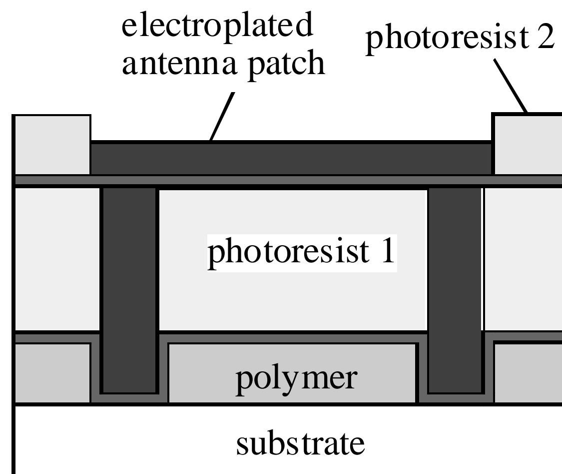
(a)



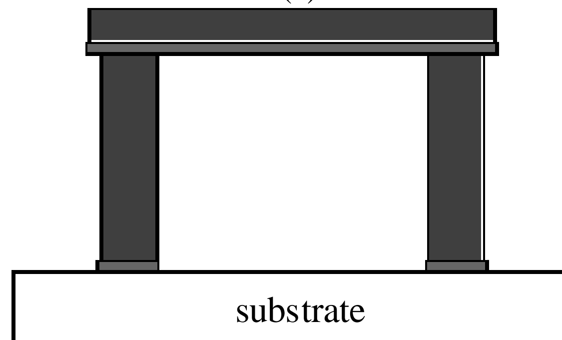
(b)



(c)



(d)



(e)

Figure A.6.3: 94 GHz air dipole antenna process flow

A.3 Process with very thick photo resist

Like LIGA (Lithographie Galvanoformung Abformung), the air antenna fabrication requires the sacrificial layer to act as a mold that is then electroplated

with metal. After subsequent processing, the sacrificial layer is removed to allow the antenna to form freestanding structure. The photoresist must have high thermal and chemical stability as a sacrificial layer.

Commercial photoresists such as Clariant AZ4000 series and Shipley SJR5000 series have been applied for magnetoresistive and inductive thin film recording head coil plating, air bearing fabrication, permanent insulation layers and tape automated bonding wafer bumping processes. A series experiments were performed with these photoresists. A maximum 54μm thickness was achieved using triple coating of AZ4620. A single coating of SJR5740 can achieve thicknesses up to 40 μm, while AZ4903 gives 30 μm. In multiple-coating processes one sees progressively smaller added thickness as the number of coatings is increased. This is because the previous photoresist layers are partly re-liquidized by absorbing the solvent from the fresh photoresist, and are thereby partially lost during spinning. This mechanism is similar to photoresist "self-etch". The soft bake time of each layer is reduced in multiple-coating process so as to prevent the bottom layers of photoresist from excessive loss of solvent and hence sensitivity. As a result, the photoresist self-etch becomes significant as the number of photoresist layer increases. Another problem with multiple coating is the edge bead accumulating effect, and the edge bead removal has to be performed in the process of each layer.

Clarient AZ9200 series photoresist replaces the AZ4000 series in applications requiring high resolution and aspect ratios, wide focus, exposure latitude, and good sidewall profiles. AZ9200 series has improved viscosity and thus can be thicker than AZ4000 series. In this work, experiments have revealed that a single coating process with AZ9260 can achieve thickness more than 100μm.

The nominal AZ9200 spin curve provided by Clarient shows nearly constant thickness for spin speeds more than 2500 RPM, and this regime is recommended for normal photoresist process. In single-coating thick photoresist processes, the spin speed is usually reduced to below 1000 RPM with a spin time less than 10 seconds. The term "spread" is more accurate than "spin" in describing the thick photoresist coating process. In the 150μm single coating process, 5ml AZP9260 is spread on a quarter of 2 inch GaAs wafer at a spin speed of 800 rpm with a spin time of 3 second. Absent of an available programmable spinner, this coating process has been proved to be repeatable in the UCSB clean room after the calibration of the spinner. A 20-minute air stabilization at room temperature is needed for the thick photoresist to reflow so as to release entrapped air and stress. The wafer is then put into a 90° C forced convection oven for a 2-hour soft bake. This long-duration soft bake is necessary for thick photoresist so that the photoresist can be hardened completely. Further, nitrogen arising from the solvent can cause bubbles in the following process. These bubbles are be driven out by a long duration soft bake. Contrary to the edge bead formation of thin photoresist, the thick photoresist has a central-convex profile. This is due to the short time spin and long duration air stabilization, during which time the liquid surface forms a drop shape before it is hardened. To improve the resist uniformity, an additional thin photoresist is applied at spin speed

of 1500 RPM for 30 seconds and is baked in a 90°C convection oven for an additional hour. Figure A.6.4 demonstrates the uniformity compensation process.

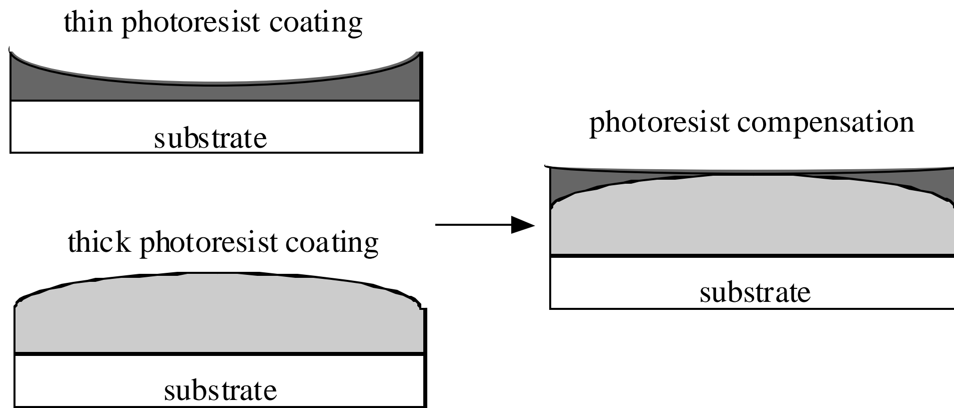
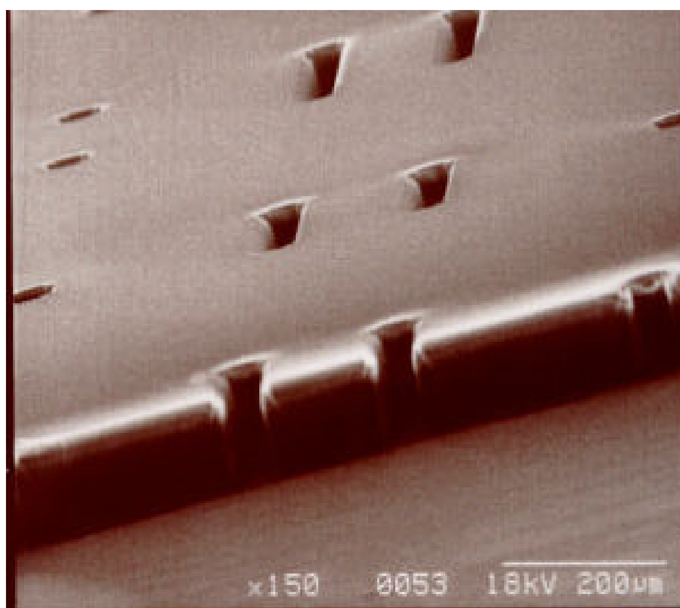
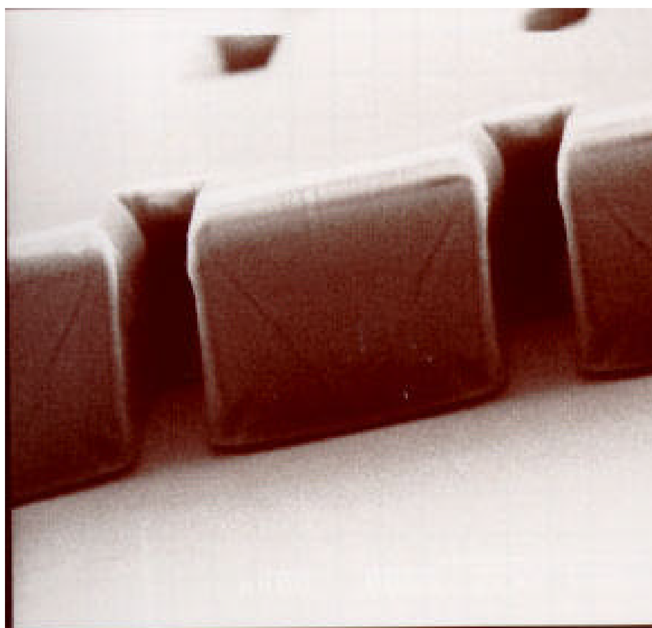


Figure A.6.4: Resist uniformity compensation process

(a)



(b)



(c)

Figure A.6.5: SEM photos of AZP9260 lithography

The wafer is then put on 110°C hot plate for 6 minute hard bake. This process is designed to increase the adhesion of the photoresist and to prevent photoresist peel-off during plating. To recover the sensitivity of the photoresist, the wafer is left in air for a 5-hour re-absorption.

The photoresist is then exposed with the post mask focused at half the thickness for 88 seconds using an RTS 6300B DSW wafer stepper and then developed in diluted AZ400K:H_2O (1:4) for 14 minutes with agitation.

Figure A.6.5 shows the SEM photographs after the development of AZ9260. Figure A.6.5 (a) is the top view and Figure A.6.5 (b) is an over view of the cross-section of the thick photoresist, which clearly demonstrates a smooth surface and uniform thickness film. Figure A.6.5 (c) is the close-up image of a post pattern, showing a thickness of 150 μm.

The post-bake after development is performed on a hotplate. The thick photoresist can wrinkle when heated rapidly or non-uniformly. Therefore (Figure A.6.6), an air gap is introduced between the wafer and hot plate during the soft bake. In Figure A.6.6, the center part of the paper towel is cut into with the same shape as wafer but with reduced diameter. Dozens of such porous paper towels are piled up on the hot plate to form a sealed air gap with the wafer on top of them. As the towel is a good thermal insulator, the wafer is heated up mainly by the air in the gap. Changing hot plate temperature setting or the number of paper towels lead to slow and uniform changes of the wafer baking temperature. In this way, the photoresist can be dehydrated gradually without introducing wrinkles.

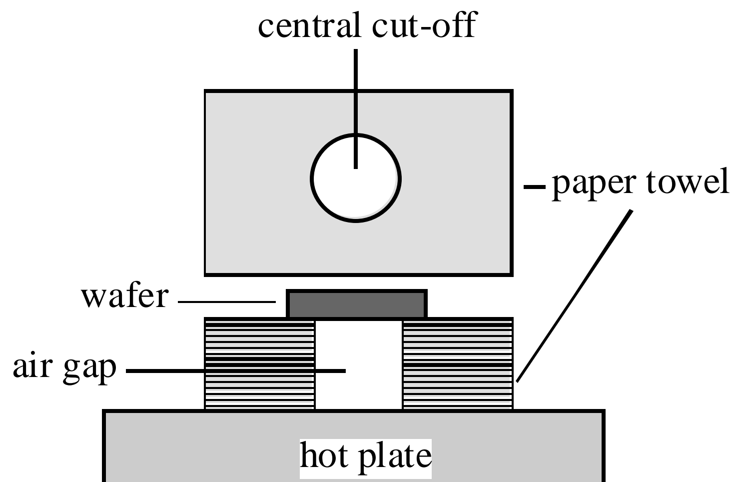


Figure A.6.6: Hot plate air-gap post-baking set-up cross-section

A.4 Au plating

The Au plating solution employed in this work is Techni-Gold 25, a buffered non-cyanide gold plating formulation. The plating rate is primarily determined by the supply current and plating area, although the solution concentration and temperature also have influence. In patterned plating, proximity effects also impact plating rate. Figure A.6.7 shows local plating around the antenna pattern and the cathode clip.

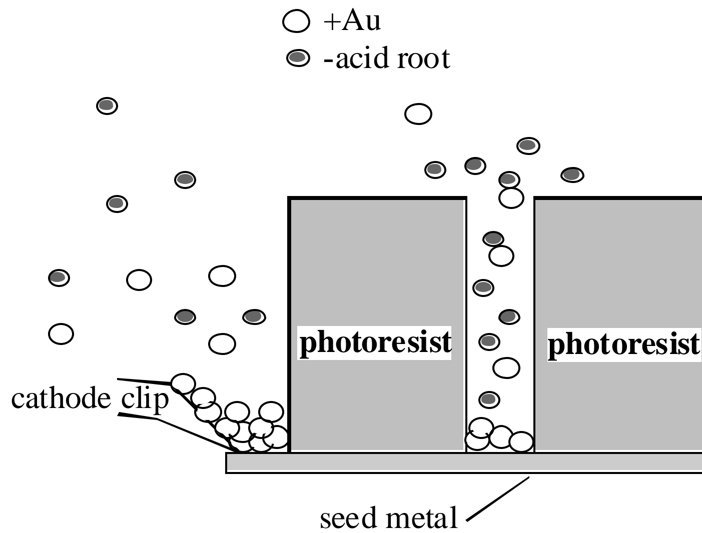


Figure A.6.7: Patterned plating diagraph

In the patterned region, both the Au ion and the negative charges have to pass through a narrow channel drifting in opposite directions. The pattern well is thus rich in negative charges as the positive Au ions deposit on the seed metal. In contrast, in open regions such as the where the cathode clip contacts the seed metal, the positive ions are easily supplied. The plating rate in the patterned region is limited by ion diffusion while in open regions, the plating rate is reaction-limited, determined only by the supply current density. There exists a plating rate competition between the two regions in that the open region has higher plating rate than the patterned region. This may lead to the whole patterned plating to fail. Further, the shortage of positive ions increases the solution PH near patterned regions, and photoresist will then be attacked. Therefore, in patterned plating, stirring is essential. The PH value of the plating solution must be monitored and plating stabilizer should be added whenever it is necessary. Open regions should be minimized to prevent plating competition with patterned regions.

High supply current can increase the plating rate while degrading the quality of the plated metal Figure A.6.8 illustrates plating failure mechanism due to high rate plating. Instead of depositing uniformly on the seed metal, the metal particles deposit rapidly on some specific sites, consuming the plating current and blocking the plating in other locations. Figure A.6.9 shows the SEM photograph showing hollow posts due to excessively high plating rate.

Long duration plating can result in loss of photoresist adhesion. The photoresist then peels off during plating (Figure A.6.10). Lowering the solution temperature can reduce this effect, but reduces the plating rate.

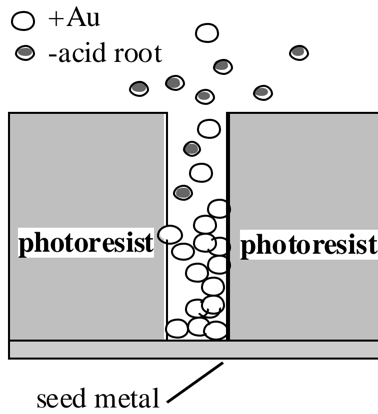


Figure A.6.8: Mechanism of high rate plating failure

Figure A.6.9: SEM photograph of high rate plating failure

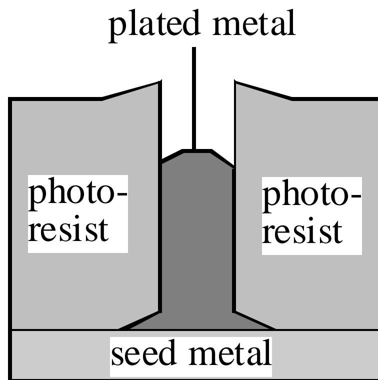


Figure A.6.10: Photoresist peeled off during plating

A.5 Results of antenna process on GaAs substrate

The first generation antenna structure is shown in Figure A.6.11. The antenna is 50 µm while the length varies from 150 µm to 800 µm.

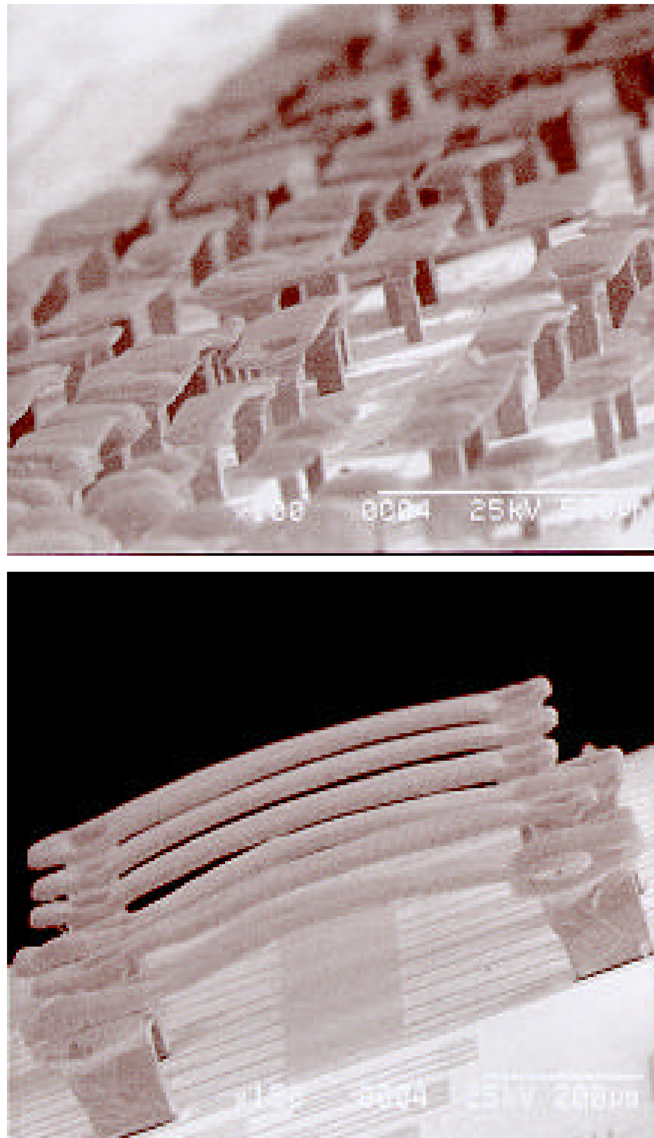


Figure A.6.11: SEM photographs of the first generation antenna structure

In these pictures, the antennas show arc shaped bridges. This is due to the wrinkles of the thick photoresist, caused by the bridge baking process in step (d) of Figure A.6.12. The picture in Figure A.6.13 shows an extreme case of such wrinkles.

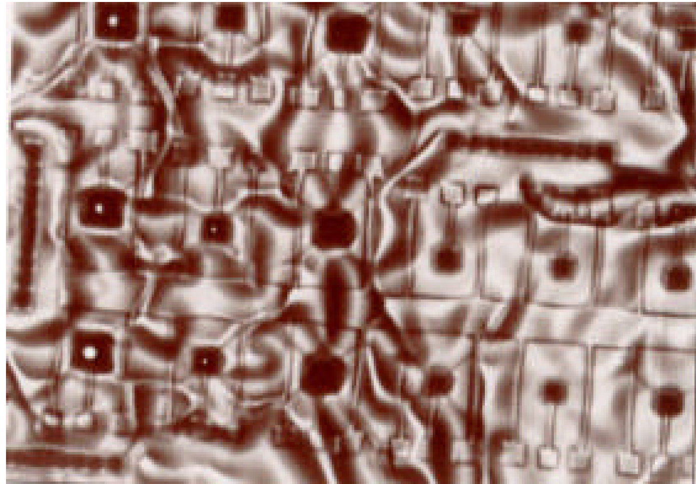
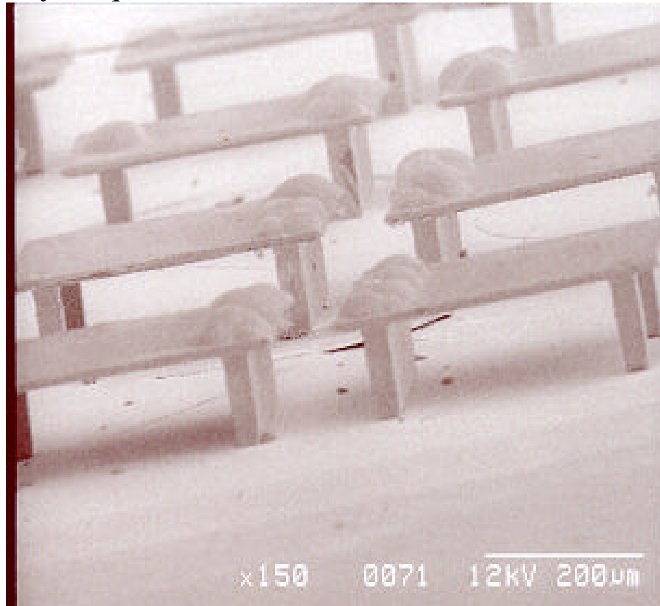
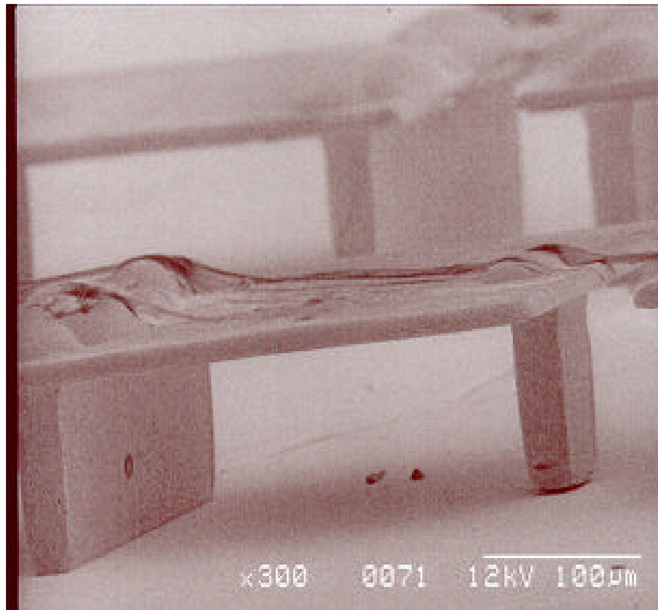


Figure A.6.12: Wrinkles of thick photoresist after baking

To solve this problem, both the baking temperature and baking time of the photoresist (photoresist2 in Figure A.6.3 (d)) are reduced, and the baking is performed using the air-gap soft baking set-up of Figure A.6.6. Figure A.6.13 includes the photographs of the second generation antennas on GaAs substrates. Caltech antenna designs had varying numbers of feed and support posts. Figure A.6.13 (b) exhibits an antenna with single supporting post, whose height is 100 µm and whose dimension are 400 µm × 600 µm. The thickness of the antenna is 10 µm. The flatness of the bridges has been substantially improved and the process has high yield and uniformity on quarters of 2" wafers.



(a)



(b)

Figure A.6.13: SEM photographs of second generation antennas

A.6 94 GHz antenna array fabricated in TS HBT technology

The antenna process can be incorporated with the transferred-substrate MMIC process to realize the 94GHz spatial power combiner module. During the MMIC fabrication, the antenna support pads are formed using the interconnect metal. Figure A.6.14 shows the cross-section of an antenna that is fed by transferred-substrate microstrip line.

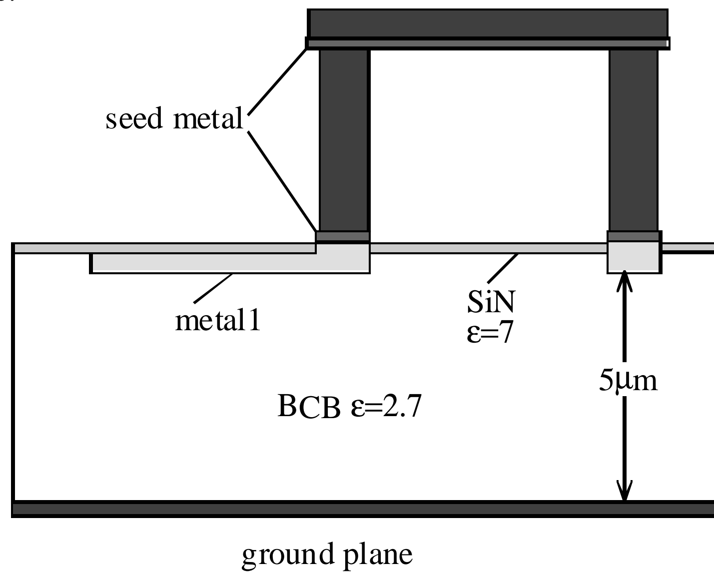


Figure A.6.14: Antenna with transferred-substrate MMIC

In transferred-substrate technology, an In/Pd alloy solder bonds the circuits to the carrier wafer. The solder's liquidus and solidus temperatures increase with the percentage of Pd in the alloy. In normal transferred-substrate process, the solder is chosen with 90 percent of indium and the liquidus temperature is 180°C. In the antenna process, the nominal curing temperature of PMGI is 200°C. This will melt the solder. It was determined that PMGI can maintain its lithographic sensitivity and stability with a curing temperature of 170 ^{o}C. Therefore, a solder with 50% Pd and 50% In is chosen for the transferred-substrate bonding. The liquidus and solidus temperatures are then 210 ^{o}C and 184 ^{o}C respectively. Higher percentage Pd alloy solders are available but their liquidus temperature is beyond the BCB's highest stable temperature and, therefore, cannot be used here.

Figure A.6.15 and Figure A.6.16 shows the 94 GHz antennas that are integrated with the transferred-substrate MMICs. The antennas were designed by the RF and microwave group in California institute of technology, and include both dipole and γ-matched dipole antennas.

As shown in Figure A.6.17, a Wilkinson power divider is used for a wide bandwidth input match, as addressed in Chapter 5. A $\lambda/2$ microstrip line inserted in one of the two branches produces 180° phase difference between the signals to each unit of the dipole antenna. The dipole antenna has a height of 150 μm and dimension of 400 μm $\times$ 310 μm with spacing of 100 μm. Figure A.6.18 show the antenna arrays.

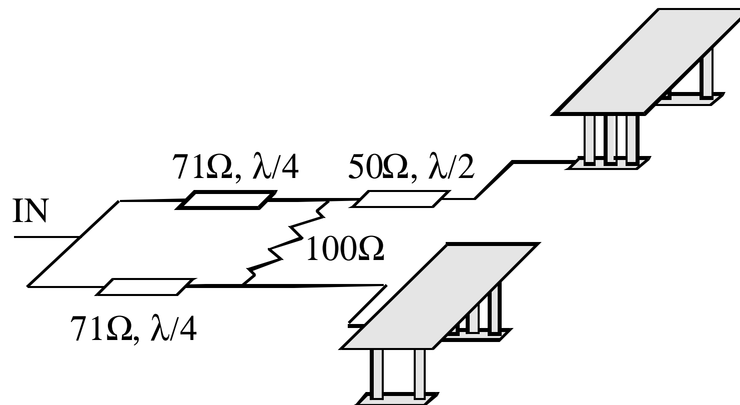
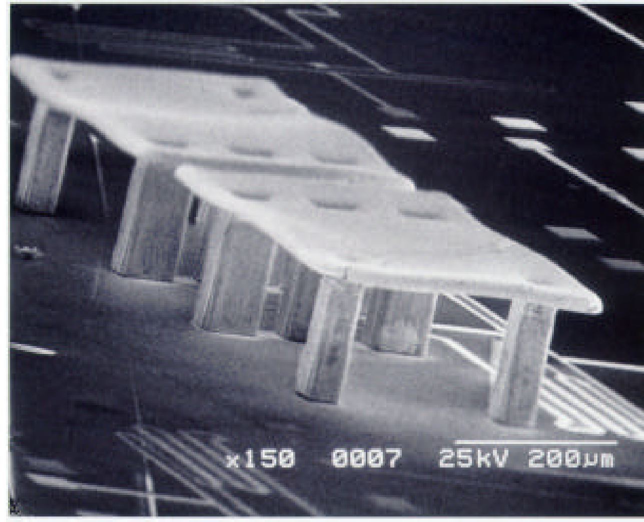
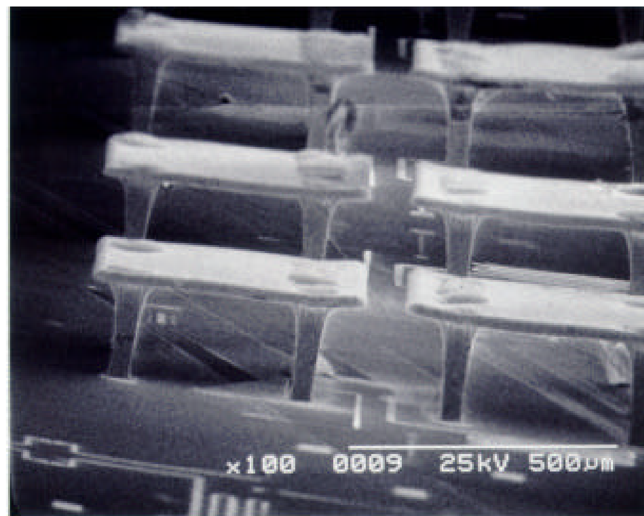


Figure A.6.15: Schematic of dipole antenna



(a)



(b)

Figure A.6.16: SEM photographs of 94 GHz dipole antenna

The γ-matched antenna has a height of 150 μm and dimensions of 1100 μm × 700 μm. Figure A.6.18 shows photographs of 94 GHz γ-matched 4 × 4 antenna array.

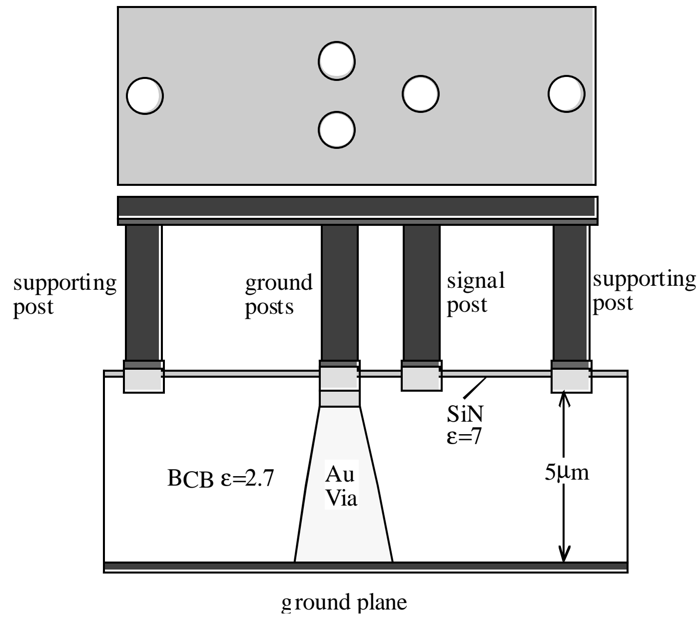


Figure A.6.17: Schematic of γ-matched antenna cross-section

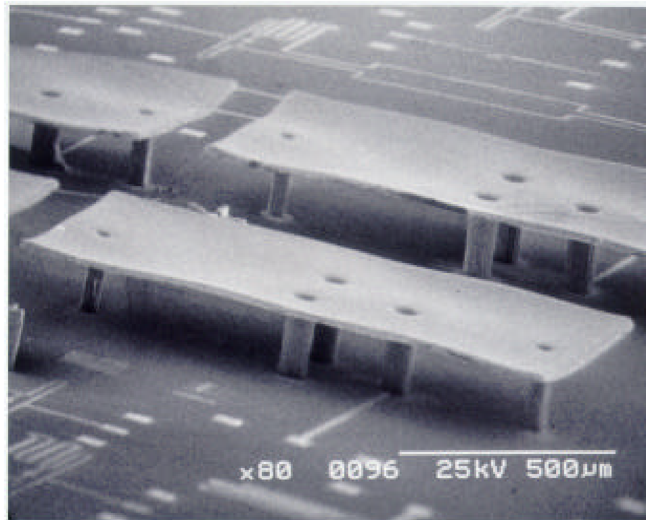


Figure A.6.18: SEM photographs of 94 GHz γ- matched antennas

Small signal RF characteristics of these antennas were measured using a vector network analyzer. The γ-matched antenna exhibits minimum return loss at 100 GHz, at which frequency the impedance is $50 + j0\ \Omega$ (Figure A.6.19).

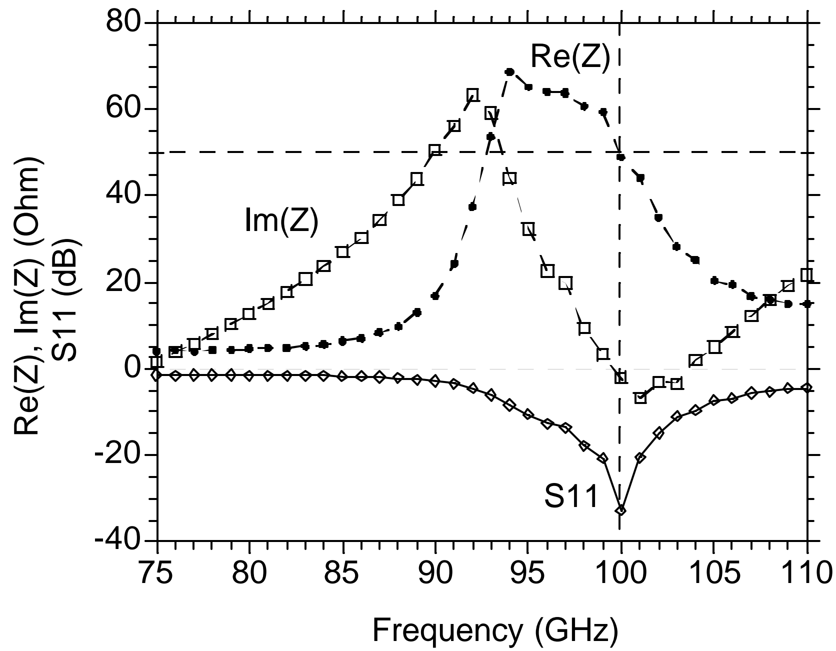


Figure A.6.19: RF measurement of γ-matched antenna

A.7 Conclusion

A plating process for 94 GHz air-dielectric antennas was developed. The process uses thick photoresist as the plating mold. The process was further incorporated into the transferred-substrate HBT MMIC technology. Gamma-matched antennas have demonstrated a 100 GHz center frequency.