Updating APVDAQ, a software designed for testing APV25 Chips

Andreas Doblhammer
(e1025831)

December 22, 2014

Introduction

The main goal of this work was to improve the data acquisition software (APVDAQ) used to test PCB hybrids with APV25 readout chips. These chips are used in the new Silicon Vertex Detector (SVD) in the Belle-II experiment currently under construction at the KEKb collider in Japan.
The KEKb particle collider is located at the High Energy Accelerator Research Organization (KEK) in Tsukuba, Japan. It is an asymmetric electron-positron collider. Asymmetric means, that the accelerated electrons and positrons have different energies. In KEKb, electrons have an energy of 8 GeV, while positrons have an energy of 3.5 GeV. At the Super KEKb, the successor experiment, this energy asymmetry will be reduced to electrons having an energy of 7 GeV and positrons having an energy of 4 GeV.
KEKb has a circumferential length of 3016 meters and holds the record for being the accelerator with the world's highest luminosity of $2.11{*}10^{34}cm^{-2}s^{-1}$. In Super KEKb, this factor will be increased even further to achieve a luminosity of $8 * 10^{35}cm^{-1}s^{-1}$.

Due to the energy asymmetry, copious amounts of B-mesons are produced. These particles are an important tool for studying CP-violation, as it is especially distinct and well observable in the decay of these mesons. It also is the reason why KEKb is called a B-factory.
The experiment designed for observing the CP-violation is the Belle detector,

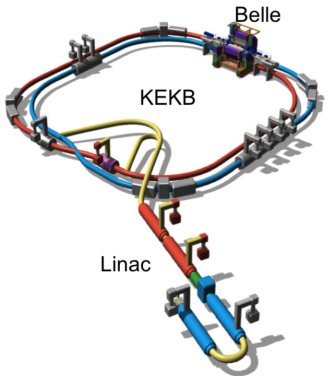


Figure 1: The KEKb collider with the preceding linear accelerator (LINAC)

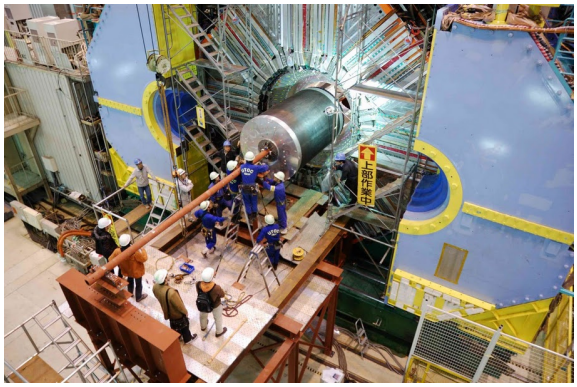


Figure 2: Construction of the Belle Detector

which is located at the single collision point of the KEKb collider. The Belle experiment is a multilayer particle detector arranged cylindrically around the beam axis. The whole detector (except the muon detectors) is built within a solenoid coil providing a 1.5 Tesla magnetic field, forcing the particles on circular trajectories and making it possible to determine charge and momentum of the particles.
Each of its subdetectors is designed for a specific purpose: a silicon vertex detector for determining the location of particles with precision of the order of tens of micrometers, drift chambers for measuring trajectories, momenta and energy loss of particles, an electromagnetic calorimeter comprised of scintillator crystals for determining a particle's total energy, Time-of-Propagation counters that reconstruct the light cones emitted from particles passing through radiator crystals through the Cherenkov-Effect, as well as K_0^L meson and muon detectors outside of the solenoid coil.

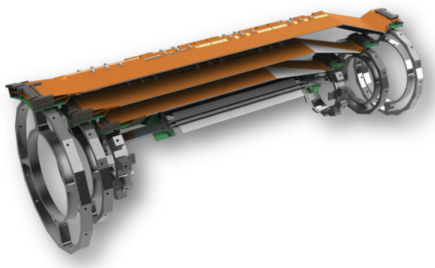


Figure 3: Illustration of the Silicon Vertex Detector

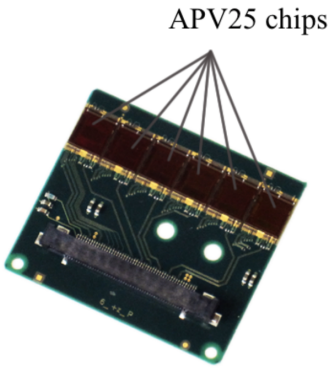


Figure 4: APV25 Readout chips on a PCB

The Vienna Institute for High Energy Physics has been assigned with the task of building the third layer of the Silicon Vertex Detector (SVD). This task includes development, construction, assembly and testing. The SVD layers consist of double-sided silicon strip detectors, where the strips on the two sides are perpendicular to each other, creating a spatial resolution in the micrometer range.
When a particle passes through a silicon strip, it creates a very small current, too small to be processed. APV25 chips, mounted on either a PCB or an Origami flex structure, are used to amplify the incoming signal. Each chip has 128 input channels, one channel per strip.

After a PCB hybrid is assembled, it needs to be tested to ensure that all APV25 chips operate reliably. For this purpose, the APV Data Acquisition (APVDAQ) system has been developed at the HEPHY.

APVDAQ

The APVDAQ test system and software has been developed at the Vienna Institute for High Energy Physics in order to test APV25 chips. The APVDAQ software is a Windows application programmed in C in LabWindows^{TM} /CVI from National Instruments. In the following section, the main run types are explained briefly, while the next section focuses on the changes being made during the time of this thesis.
More detailed information on the APVDAQ software and test system can be found in the reference manual [1], as well as in [2] and [3].

The following tests are used in order to test the functionality of a hybrid board:

ADC Delay Scan

Readout chips provide an analog output signal, which has to be converted by an analog to digital converter (ADC). Its sampling phase depends on clock frequency and cable length. To allow easy timing configuration, it comes with an adjustable delay. The ADC Delay Scan was developed to find the optimal delay settings. This run type scans all possible delay settings of an APV25 tick mark with a time resolution of 1 ns. Fig. 5 shows the result of an ADC Scan. The optimal delay setting can be obtained from the x-axis.

FIR Calculation

When transmitting analog signals over long cables, one faces two problems: the transfer function of the cable is dependent on frequency and, if the impedance changes, reflections occur, in particular at both ends of the transmission line. The latter can in principle be avoided by terminating the line with its impedance. In reality, however, there are always imperfections.
To solve these problems, a digital FIR (finite impulse response) filter was implemented on the receiving end of the transmission, i.e. in the APVDAQ firmware, just after the ADC.
A FIR filter convolves the (distorted) incoming signal $v(n)$ with filter coef-

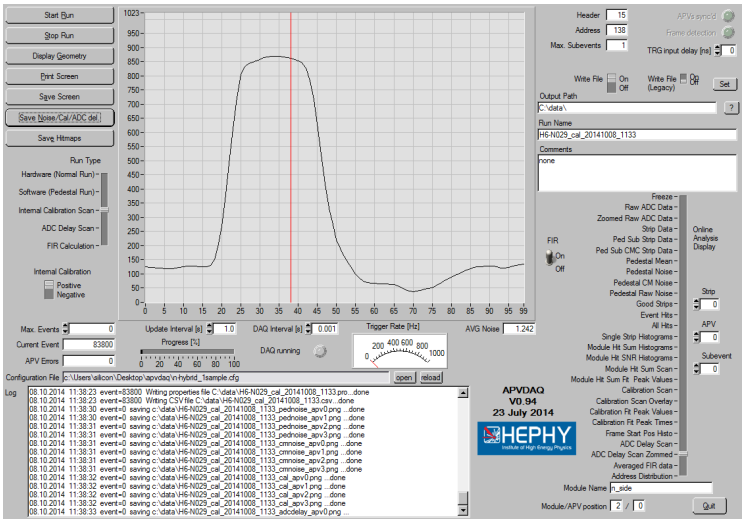


Figure 5: Result of an ADC Delay Scan

ficients $f(k)$ in the following form:

$$s(n) = \sum_{k=0}^{m} f(k)v(n-k) \tag{1}$$

The number of filter coefficients, i.e. m+1, is called the filter order. In APVDAQ, a FIR filter of the order 8 is used. The output signal after the convolution is ideally identical to the detector signal.
However, before a FIR filter can be used, the filter coefficients need to be calculated. This is done in the FIR calculation run. More information on this FIR filter can be found in [2].

Pedestal Run (Software)

In this run type, periodical software triggers cause the software to read out data from the APV25 chips randomly, i.e., there is no correlation between data acquisition and particle hits (given that there are any). This run type is used to determine pedestals and noise of each APV channel. It is also suitable to check the functionality of a setup in the lab. Fig. 6 shows the result of a noise calculation.

Calibration Scan

In calibration scan mode, the shape of the calibration pulse of each APV25 chip is recorded by using its internal calibration functionality. Several calibration requests with different timing are sent to the chips in order to scan the whole shaping curve with a time resolution of 1/8 clock period. This run

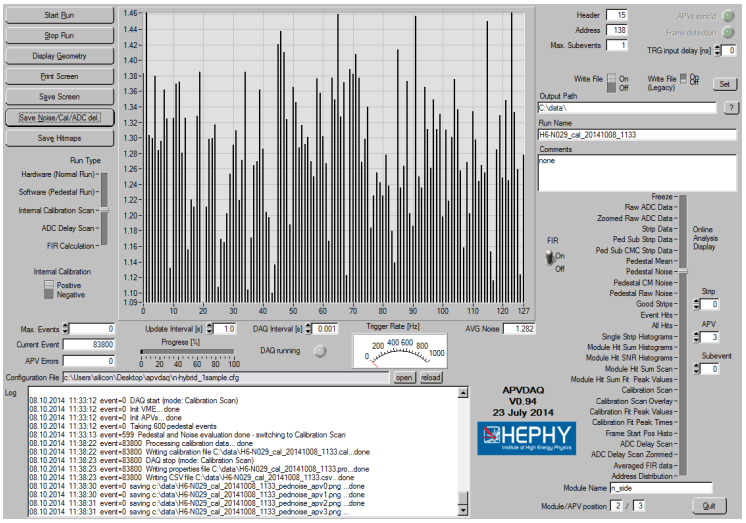


Figure 6: Result of a noise calculation

type is suitable to check the peaking time and obtain calibration constants for each channel. The APVDAQ software provides plots of each channel separately as well as an overlay plot of all channels of one APV chip. In these plots, shortened channels are detected, as their calibration signal is significantly lower. Channels not connected to the sensor, on the other hand, are characterized by a slightly higher calibration signal. Both, however, can be identified easily in the calibration scan plot. Fig. 7 shows the result of a calibration scan. Several shortened channels are clearly visible.

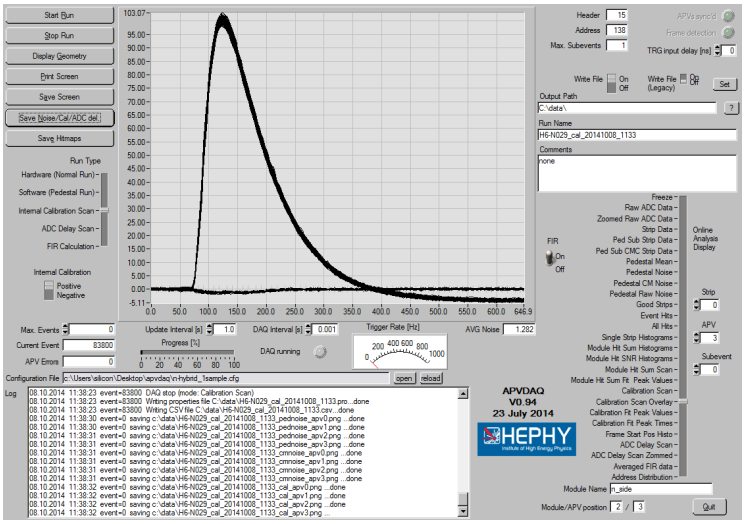


Figure 7: Result of a Calibration Scan

New Features of Version 0.95

This section is about the changes implemented in the APVDAQ software during the time of this thesis. Most of them are minor improvements making the life of the software's user a little easier. Some of them, however, were important fixes of bugs that would otherwise affect the functionality of the software. The list of improvements reads as follows:

- Until now, the whole file name including current date and time had to be entered and updated with every measurement. In the latest version, all that is required is the Object-ID. The software automatically adds date and time, as well as the combination "ped" or "cal" for Pedestal Run or Calibration Scan, respectively.
- Files can now only be saved in Hardware Run, Pedestal Run and Calibration Scan.
- In the previous version, if the Online Analysis Display was set on Calibration Scan Overlay during a measurement, it produced a warning, claiming that the display would be very slow in named setting, as a lot of CPU capacity would be required. For being written within a loop, this warning was produced continuously during a measurement. As modern computers can handle the required CPU capacity with ease, the warning was erased and Calibration Scan Overly can now be safely used during measurements.
- In the latest version, an Operator ID has to be entered before any measurement can be started. Any combination of characters can be used, except "-" and " ", as it is the initial combination. The Operator ID is written into the saved CVS files.
- Until now, APVDAQ could be opened multiple times, causing communication problems with the corresponding hardware. Version 0.95 can only be opened once. Attempting to start another instance will merely foreground or maximize it, if it's minimized.
- Up to now, if APVDAQ was running in multi-peak mode and a signal was spread out across several subevents, the software produced multiple entries in both the Sum and SNR Histogram, as each subevent

was counted separately. In the latest version, only that subevent, in which the signal amplitude is highest, is processed and thus each event is counted only once despite of having multiple samples.

- The raw mode file output was adapted to the new file format by changing a header file to match other modes.
- Files and Plots can now optionally be saved to a specifically created subfolder named after the Object ID.
- The bug causing a calibration measurement to be conducted with inverted polarity, after an error was detected in an APV, was fixed.
- It is now possible to pause running measurements.
- In previous versions, Common Mode Correction (CMC) was performed by dividing the strips into groups of 32, discarding the 5 highest and lowest readings and then averaging the 22 remaining values. This CMC-value was then subtracted from the reading. In the latest version, a switch was created to change the way the groups are formed. In its default -or 32- setting, the groups are composed of 32 consecutive stripes, while in the "4" setting the groups are built modulo 4, i.e. the first group consists of the first, the fifth, the ninth strip, the second group of the second, the sixth, the tenth strip and so on.
- A TCP socket was created, making it possible to control APVDAQ remotely via a number of commands listed below. As APVDAQ automatically closes the connection after each command, it is possible for any number of computers to control the program simultaneously. APVDAQ listens on TCP port 2001.

TCP socket commands

The TCP input has to have the following syntax:

[command] or [command],[option]

- **st**: start run
- **pause**: pause run
- **end**: stop run
- **save**: save all plots
- **m**: enter max. events
- **o**: enter object ID
- **n**: enter operator name
- **p**: enter path name of destination folder

- **c**: enter path name of configuration file
- **l**: write content into log file
- **t**: select runtype
  options: (0) Hardware Run, (2) Pedestal Run, (3) IntCal vs. Vsep Scan (as of V0.96), (4) Internal Calibration Scan, (5) FIR Calculation, (6) ADC Delay Scan
- **cmc**: CMC switch *options: (0) 32, (1) 4*
- **f**: FIR switch
  options: (0) OFF, (1) ON
- **w**: write file
  options: (0) OFF, (1) ON
- **s**: write files into subfolder
  options: (0) OFF, (1) ON

for example: If one wants to select a maximum of 10.000 events, one types "m,10000". If one wants so enter a certain path name, one types "p,C:\\...." (when entering path names, double backslashes are necessary)

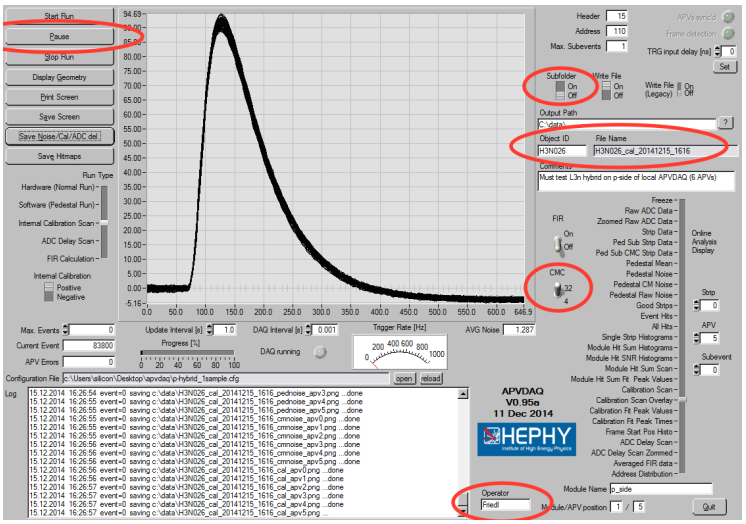


Figure 8: Changes in the new user interface: Pause button, Subfolder and CMC switches, Object ID and Operator boxes

Measurements

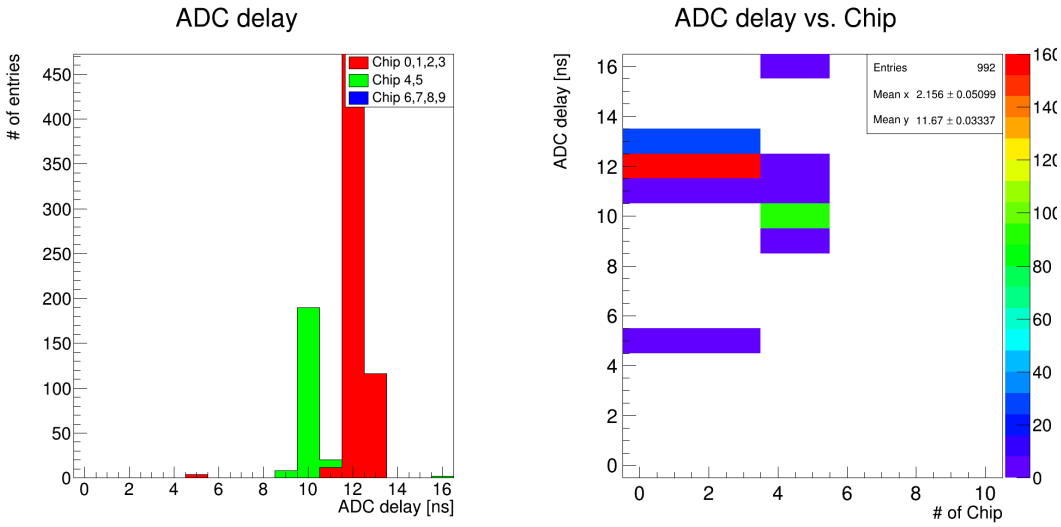
During the time this thesis was written, 75 APV25 hybrids were tested with the APVDAQ software. Two of them have been found to be defective, so they were excluded from the tests and have been set aside for repair.
In the following section, the result of these tests, as well as the results of the chips tested in [4] creating a total of 190 tested chips, were combined into histograms.
For more information on the ROOT software creating these histograms and the initial results, see [4].
For this thesis, the ROOT software was upgraded to the effect that it now also creates histograms picturing the temporal evolutions of pedestal, noise, raw noise, CMC (common mode noise), calibration peak and calibration time. In these histograms, the x-axis represents the day of the measurement, starting from July 1^{st} 2014. I.e., day 54 is August 23^{rd} and so on.
In the following, the results of [4] are briefly reviewed and new histograms are explained.

ADC Delay

No major changes in ADC delay tests have been noted between the newly tested chips and those tested in [4], although in [4], there are outliers at 5, 9 and 16 nanoseconds, which don't occur in the latest measurements. The mean value of the ADC delay is 11.77 ns if only the latest chips are considered and 11.66 ns in general.

FIR Coefficients

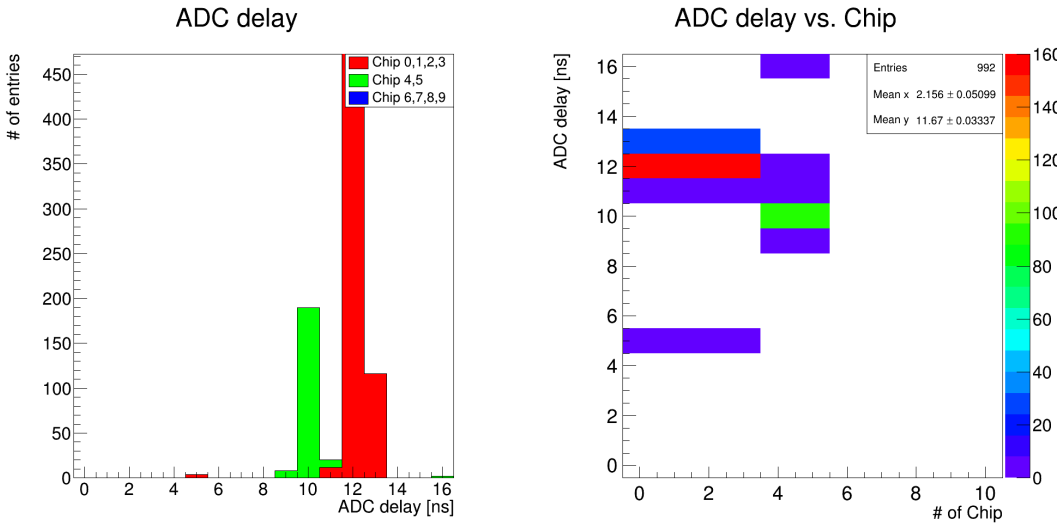
The mean values of the FIR coefficients changed only negligibly, as can be seen in table 1, as well as in fig. 11, 12 and 13:



(a) ADC delay

(b) ADC delay vs. chip

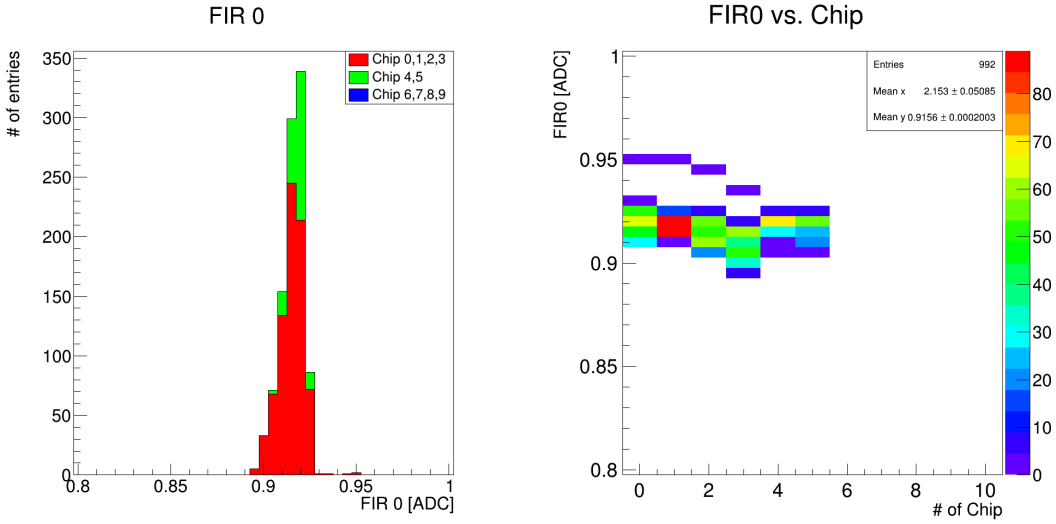
Figure 9: ADC delay histograms of all hybrids



(a) ADC delay

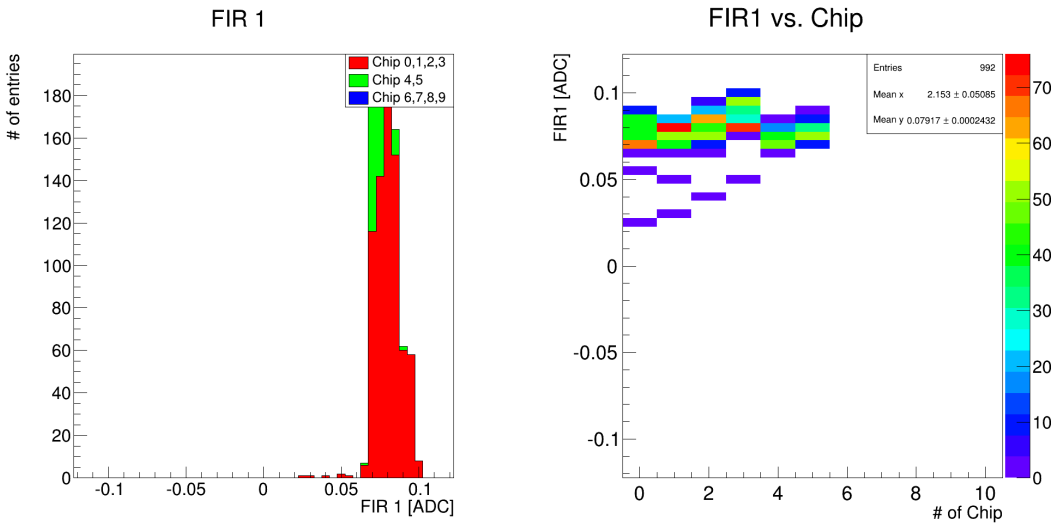
(b) ADC delay vs. chip

Figure 10: ADC delay histograms of the newly measured hybrids



(a) FIR0 (b) FIR0 vs. chip

Figure 11: Histograms of the FIR0 and FIR0 vs. chip distributions

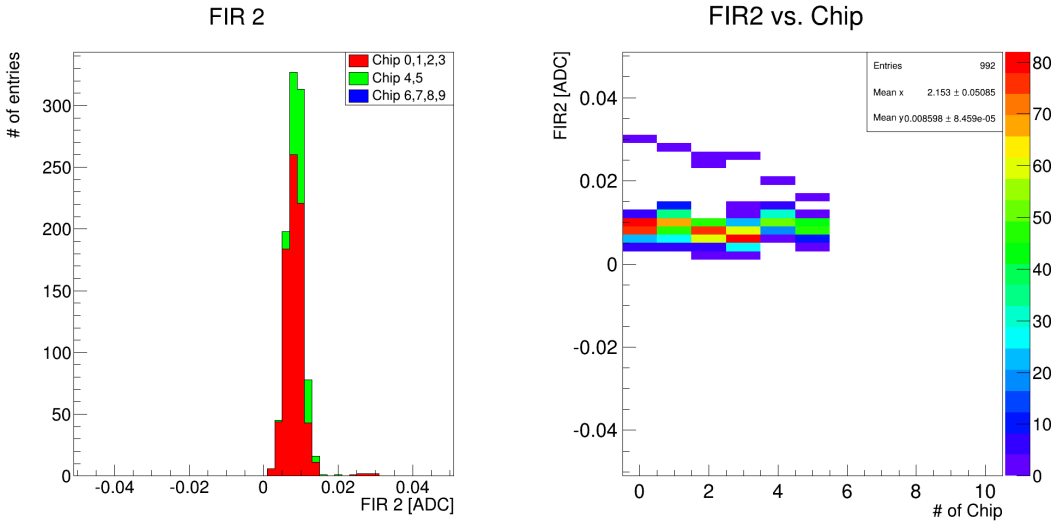


(a) FIR1 (b) FIR1 vs. chip

Figure 12: Histograms of the FIR1 and FIR1 vs. chip distributions

FIR coefficient	mean old	mean new	mean total
FIR0	0.9171	0.9134	0.9156
FIR1	0.0775	0.0817	0.0792
FIR2	0.00869	0.00846	0.0086

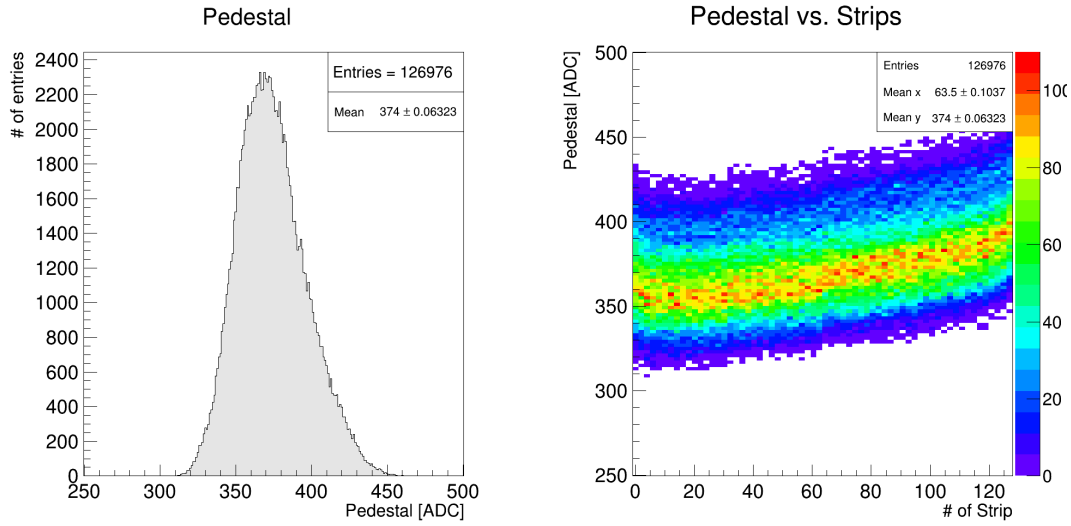
Table 1: Mean value of FIR coefficients



(a) FIR2

(b) FIR2 vs. chip

Figure 13: Histograms of the FIR2 and FIR2 vs. chip distributions



(a) Pedestal

(b) Pedestal vs. strips

Figure 14: Pedestal and pedestal vs. strips histograms

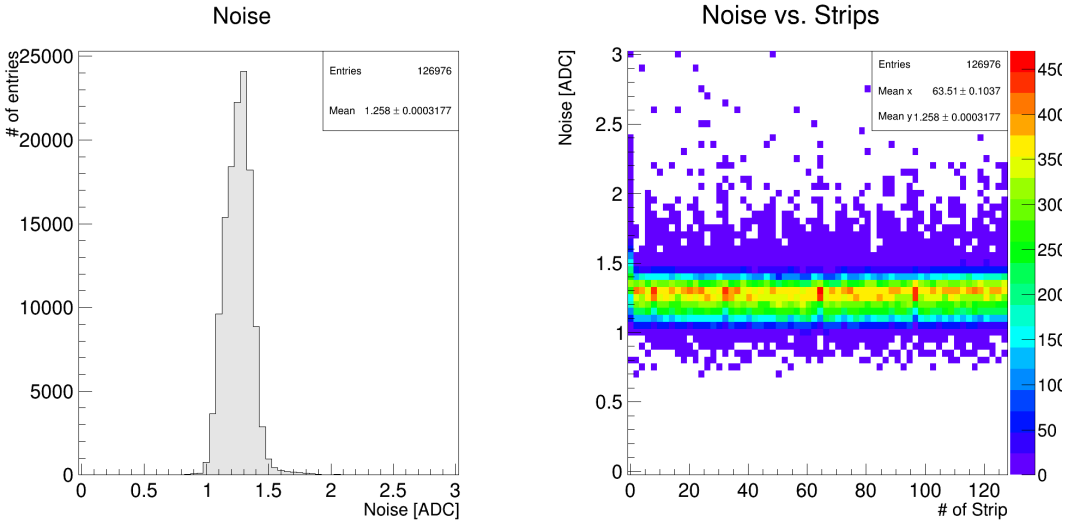
Pedestal, Noise, Raw Noise and CMN

In [4], a characteristic tail towards greater values is noticed in the raw noise and CMN histograms. If only the newly tested chips are evaluated, this tail can be reproduced, even though it is not quite as distinct as in was in the previous measurements. This means, that the newly tested chips are behaving similarly to the older ones regarding raw noise and CMN. The histograms in fig. 16, 17 and 18 give a comparison of the raw noise, fig. 19, 20 and 21 a comparison of CMN behavior of the old and the new chips, as well as all chips together.

	old	new	total
Pedestal	374.6	373.2	374
Noise	1.263	1.25	1.258
Raw Noise	5.468	5.49	5.477
CMN	5.258	5.304	5.277

Table 2: Mean values of pedestal, noise, raw noise and CMN measurements

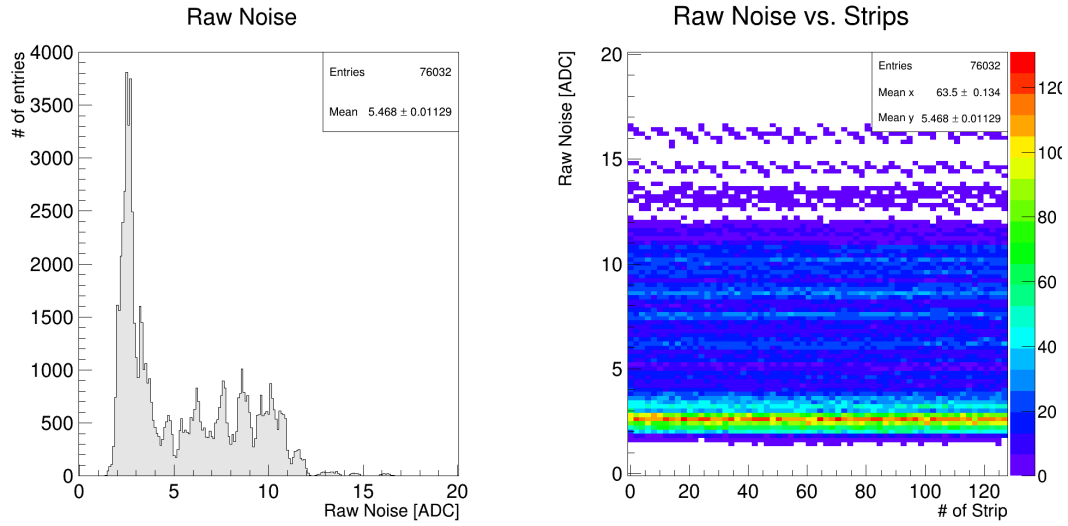
Looking at the time evolution histograms, one can clearly see that the values of the pedestal, calibration pulse and calibration time don't vary much in time. This is a good sign, as it indicates that both hybrid boards and APVDAQ test setup are operating steadily and no temporal dependency needs to be taken into consideration.



(a) Noise

(b) Noise vs. strips

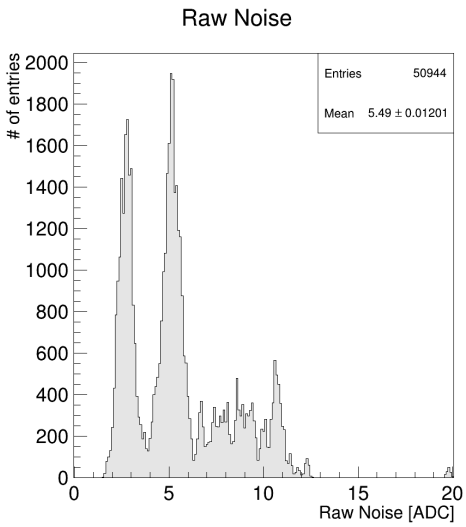
Figure 15: Noise and noise vs. strips histograms



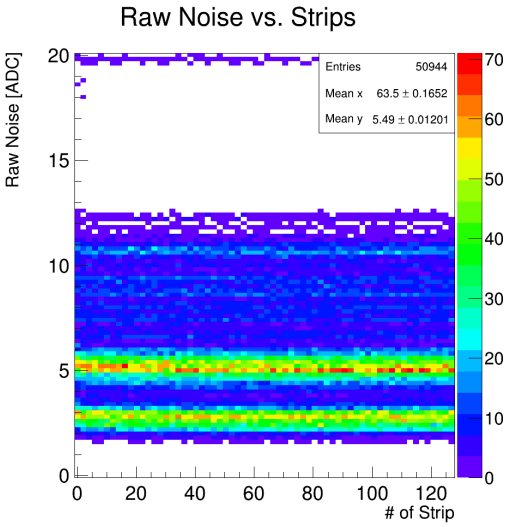
(a) Raw noise

(b) Raw noise vs. strips

Figure 16: Raw noise and raw noise vs. strips histograms of the old chips

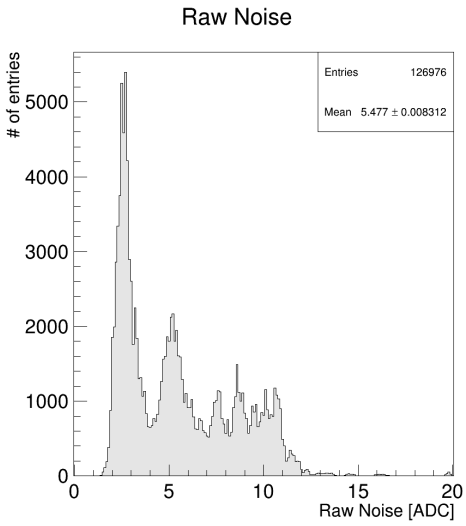


(a) Raw noise

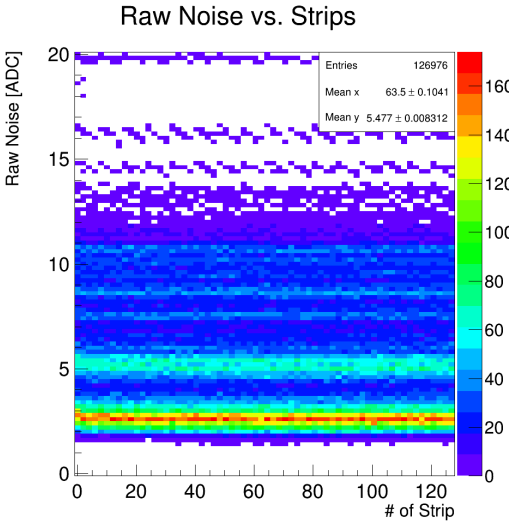


(b) Raw noise vs. strips

Figure 17: Raw noise and raw noise vs. strips histograms of the newly bonded chips

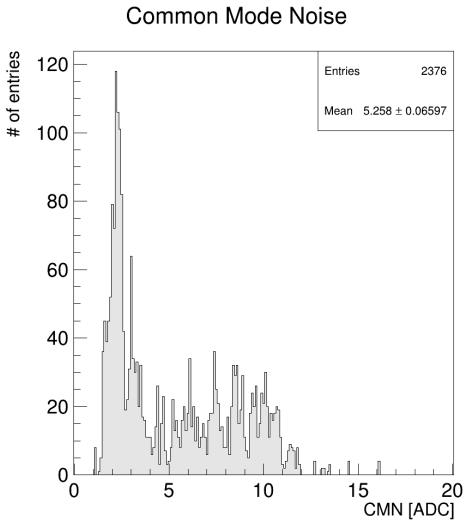


(a) Raw noise

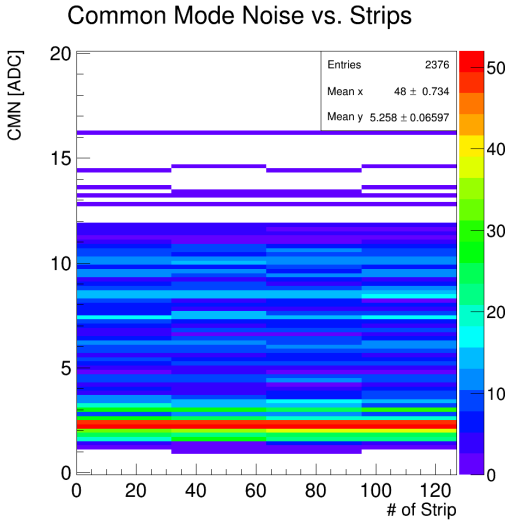


(b) Raw noise vs. strips

Figure 18: Raw noise and raw noise vs. strips histograms of all chips

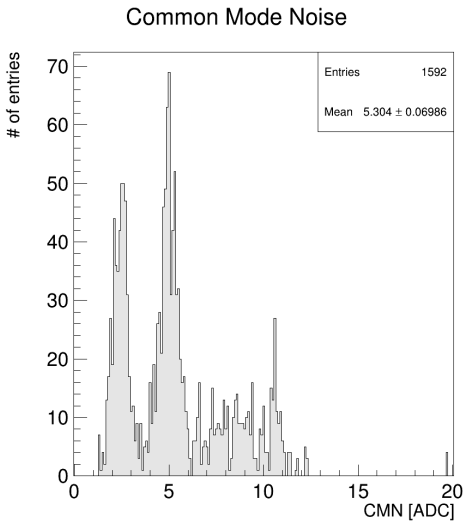


(a) CMN

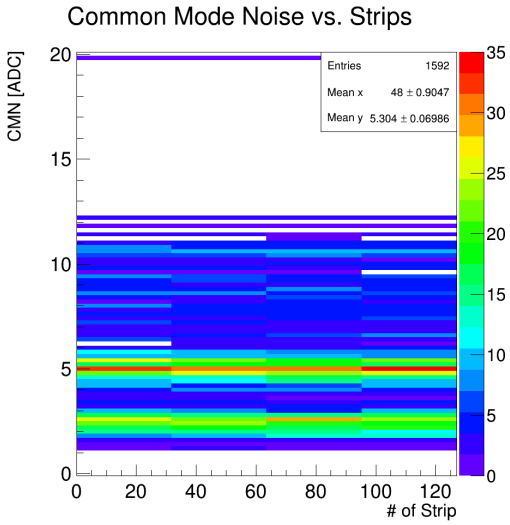


(b) CMN vs. strips

Figure 19: CMN and CMN vs. strips histograms of the old chips

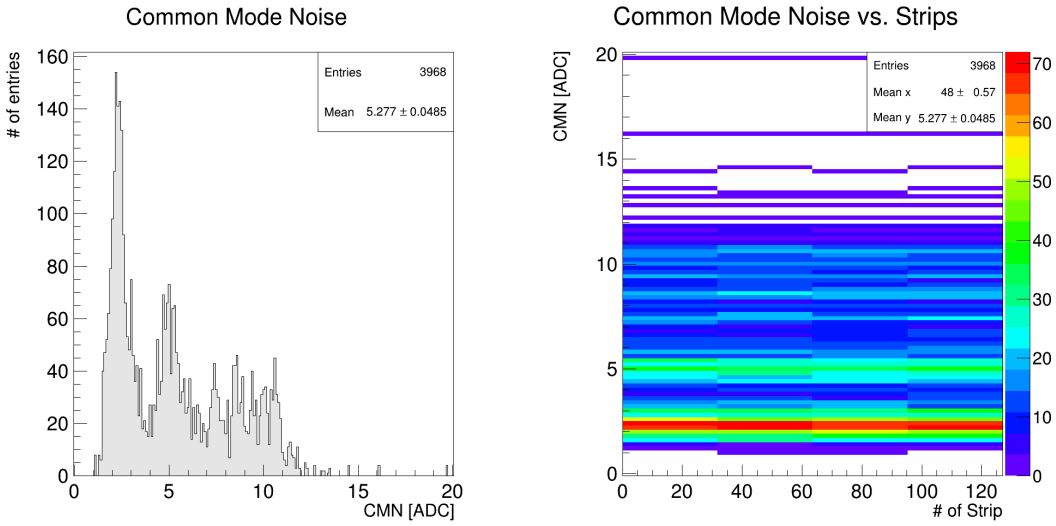


(a) CMN



(b) CMN vs. strips

Figure 20: CMN and CMN vs. strips histograms of the newly bonded chips



(a) CMN

(b) CMN vs. strips

Figure 21: CMN and CMN vs. strips histograms of all chips

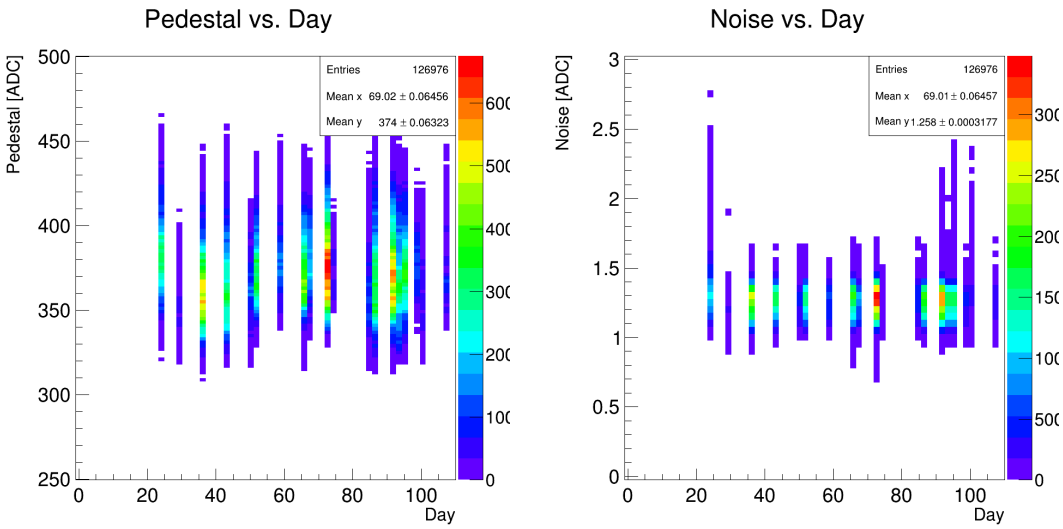
The noise, raw noise and CMN values, however, show a temporal dependency. These dependencies turned out the be minor and were a consequence of an imperfectly configured APVDAQ system, which caused the noise, raw noise and CMN values to be higher at the beginning of the measuring process.

Calibration Pulse and Time

The mean values of calibration pulse and time again don't differ much from the values achieved in [4]. Also, they seem to be virtually constant in time. The areas far off the mean value in the 2D histograms originate from the two faulty chips mentioned in [4].

	mean value
Calibration Pulse	95.02
Calibration Time	130.6

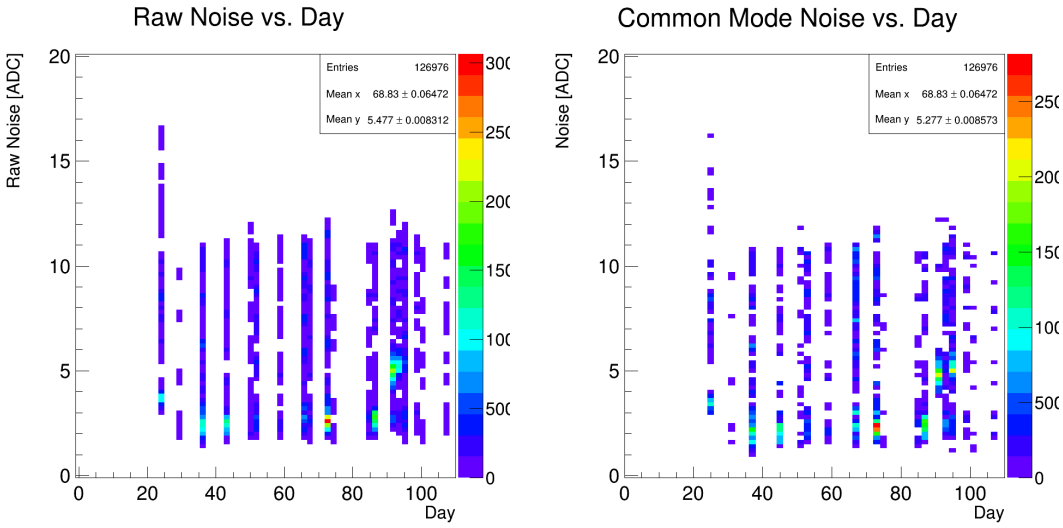
Table 3: Mean values of calibration pulse and time



(a) Pedestal vs. date

(b) Noise vs. date

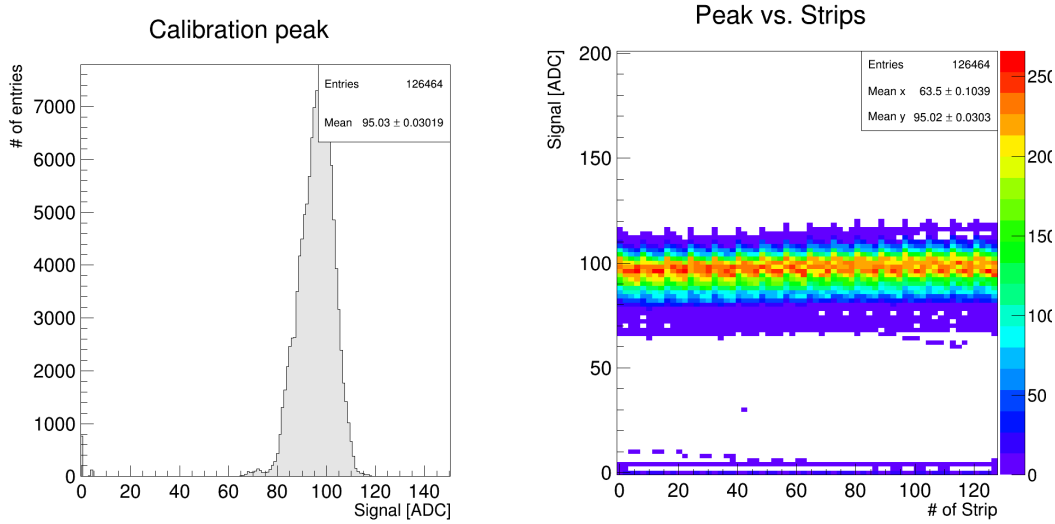
Figure 22: Pedestal and noise vs. date histograms



(a) Raw noise vs. date

(b) CMN vs. date

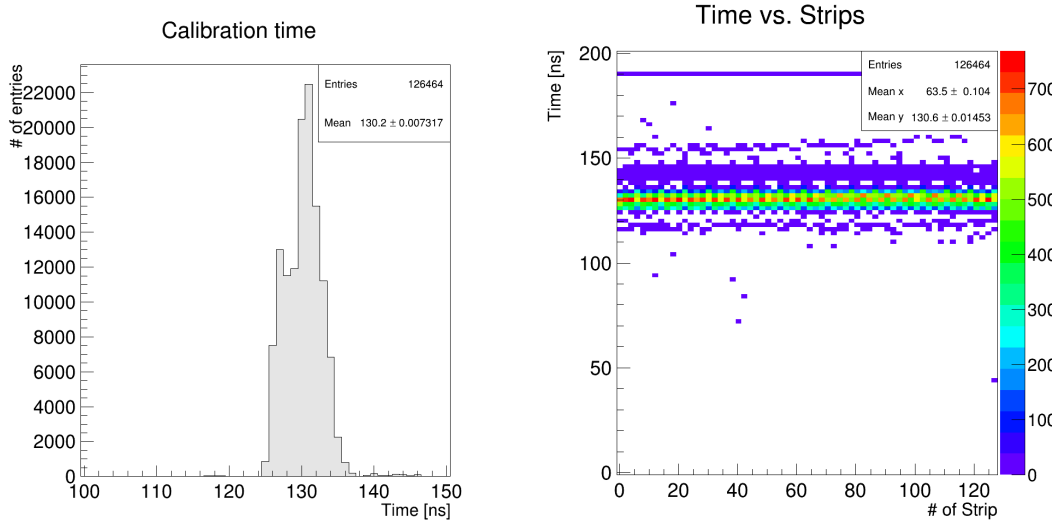
Figure 23: Raw noise and CMN vs. date histograms



(a) Calibration pulse

(b) Calibration pulse vs. strips

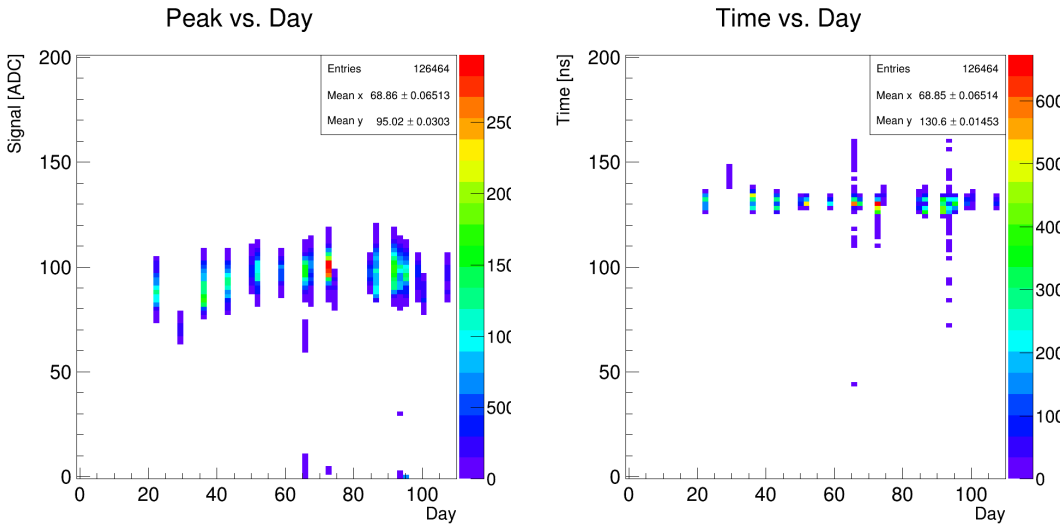
Figure 24: Calibration pulse and calibration pulse vs. strips histograms



(a) Calibration time

(b) Calibration time vs. strips

Figure 25: Calibration time and calibration time vs. strips histograms



(a) Calibration pulse vs. date

(b) Calibration time vs. date

Figure 26: Calibration pulse and time vs. date histograms

Conclusions

Now that there is a second set of measurements, one can compare current measurements with older ones (i.e. measurements conducted in [4]) and, as the measurements were conducted over a period of four months, study the temporal development of hybrid boards.
It appears that both the hybrid boards and the APVDAQ testing system are running steadily. The minor temporal dependencies of noise, raw noise and CMN can be ascribed to imperfect calibration of the APVDAQ system at the beginning of the measuring process.
Ultimately, the APVDAQ testing system can ensure that the manufactured hybrid boards have a high quality standard and are suitable for the Belle II Detector.

Bibliography

[1] HEPHY: **APVDAQ Reference Manual**, Nov. 2009

[2] M. Friedl, J.W. van Hoorne, H. Steininger: **The Incredible Power of an FIR Filter**, 2011

[3] C.Irmler: **Upgrade Studies for the Belle Silicon Vertex Detector**, Aug. 2008

[4] D.Handl **Readout Hybrid tests for the Belle II Silicon Vertex Detector**, Oct. 2014

List of Figures