VLSI Fabrication Process

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Abstract

VLSI stands for "Very Large Scale Integration". This is the field which involves packing more and more logic devices into smaller and smaller areas. Thanks to VLSI, circuits that would have taken boardfuls of space can now be put into a small space few millimeters across! This has opened up a big opportunity to do things that were not possible before. VLSI circuits are everywhere ... your computer, your car, your brand new state-of-the-art digital camera, the cell-phones, and what have you.We must have a working knowledge of chip fabrication to create effective designs and in order to optimize the circuits with respect to various manufacturing parameters. Also, the circuit designer must have a clear understanding of the roles of various masks used in the fabrication process, and how the masks are used to define various features of the devices on-chip.

Introduction

An Integrated Circuit (IC) is an electronic network fabricated in a single piece of a semiconductor material.
The semiconductor surface is subjected to various processing steps in which impurities and other materials are added with specific geometrical patterns
The fabrication steps are sequenced to form three dimensional regions that act as a transistors and interconnects that form the network.

Why VLSI ?

1. Greater Functionality

Its results in average energy savings of 35% to 70% with an average speedup of 3 to 7 times.

2. Embedded Characteristics

After fabrication many applications could share commodity economics for the production of a single IC and the same IC could be used to solve different problems at different points in time.

3. Lower System Cost

By eliminating the ASIC design lower system cost on a low-volume product is achieved. For higher-volume products, the production cost of fixed hardware is actually very much lower.

History

The final step in the development process, starting in the 1980s and continuing through the present, was "very large-scale integration" (VLSI). The development started with hundreds of thousands of transistors in the early 1980s, and continues beyond several billion transistors as of 2007.

There was no single breakthrough that allowed this increase in complexity, though many factors helped. Manufacturing moved to smaller rules and

cleaner fabs, allowing them to produce chips with more transistors with adequate yield, as summarized by the International Technology Roadmap for Semiconductors (ITRS). Design tools improved enough to make it practical to finish these designs in a reasonable time. The more energy efficient CMOS replaced NMOS and PMOS, avoiding a prohibitive increase in power consumption.

In 1986 the first one megabit RAM chips were introduced, which contained more than one million transistors. Microprocessor chips passed the million transistor mark in 1989 and the billion transistor mark in 2005[9]. The trend continues largely unabated, with chips introduced in 2007 containing tens of billions of memory transistor VLSI began in the 1970s when complex semiconductor and communication technologies were being developed.

The first "generation" of computers relied on vacuum tubes. Then came discrete semiconductor devices, followed by integrated circuits. The first Small-Scale Integration (SSI) ICs had small numbers of devices on a single chip — diodes, transistors, resistors and capacitors (no inductors though), making it possible to fabricate one or more logic gates on a single device. The fourth generation consisted of Large-Scale Integration (LSI), i.e. systems with at least a thousand logic gates. The natural successor to LSI was VLSI (many tens of thousands of gates on a single chip). Current technology has moved far past this mark and today's microprocessors have many millions of gates and hundreds of millions of individual transistors.

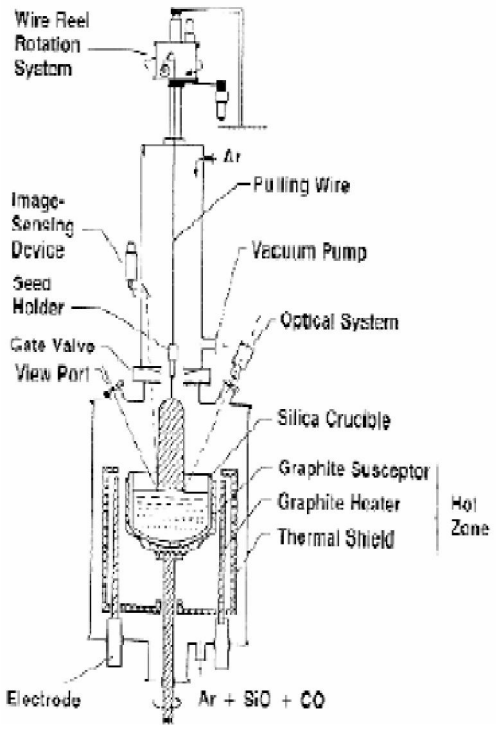
As of mid-2004, billion-transistor processors are not yet economically feasible for most uses, but they are achievable in laboratory settings, and they are clearly on the horizon as semiconductor fabrication moves from the current generation of 90 nanometer (90 nm) processes to the next 65 nm and 45 nm generations.

Fabrication process sequence

1.Silicon manifacture
2.Wafer processing
3.Lithography
4.Oxide growth and removal
5.Diffusion and ion implantation
6.Annealing
7.Silicon deposition
8.Metallization
9.Testing
10.Assembly and packaging

1. **Silicon manufacture**

Pure silicon is melted in a pot (1400º C) and a small seed containing the desired crystal orientation is inserted into molten silicon and slowly(1mm/minute) pulle out.



2. Wafer processing

The silicon crystal (in some cases also containing doping) is manufactured as a cylinder (ingot) with a diameter of 8-12 inches(1”=2.54cm).
This cylinder is carefully sawed into thin(0.50-0.75 mm thick) disks called wafers, which are later polished and marked for crystal orientation.

3.Lithography

Lithography: process used to transfer patterns to each layer of the IC

Lithography sequence steps:

Designer:Drawing the “layer” patterns on a layout editor

Silicon Foundry:Masks generation from the layer patterns in the design data base

Printing: transfer the mask pattern to the wafer surface

Process the wafer to physically pattern each layer of the IC.

(a).Photo resist application:
the surface to be patterned is
spin-coated with a light-sensitive
organic polymer called photoresist

(b)Printing (exposure):
the mask pattern is developed on the photoresist, with UV light exposure

depending on the type of
photoresist(negative or positive), the exposed or unexposed parts become resistant to certain types of solvents

(c)Development:
the soluble photo resistis chemically removed

The developed photo resistacts as a mask for patterning of underlying layers and then is removed.

4.Oxide growth and removal

Oxide can be grownfrom silicon through heating in an oxidizing atmosphere
Gate oxide, device isolation
Oxidation consumes silicon

SiO2is depositedon materials other than silicon
through reaction between gaseous silicon compounds and oxidizers
Insulation between different layers of metallization

Once the desired shape is patterned with photoresist, the etching process allows unprotected materials to be removed
Wet etching: uses chemicals
Dry or plasma etching: uses ionized gases

5 .Diffusion and ion implantation

Doping materials are added to
Change the electrical characteristics
of silicon locally through:
Diffusion: dopants deposited on silicon move through the lattice by thermal diffusion (high temperature process)
Wells
Ion implantation: highly energized donor or acceptor atoms impinge on the surface and travel below it
The patterned SiO2serves as an implantation mask
Source and Drain regions

6. Annealing

Thermal annealing is a high temperature process which:
allows doping impurities to diffuse further into the bulk
repairs lattice damage caused by the collisions with doping ions

7.Silicon deposition

Films of silicon can be added on the surface of a wafer
Epitaxy: growthof a single-crystal semiconductor film on a crystalline substate
Polysilicon: polycrystalline film with a granular structure obtained through depositionof silicon on an amorphous material
MOSFET gates

8.Metallization

Metallization: deposition of metal layers by evaporation
interconnections

9.Testing

Test that chip operates
Design errors
Manufacturing errors
A single dust particle or wafer defect kills a die
Yields from 90% to < 10%
Depends on die size, maturity of process
Test each part before shipping to customer

10.Assembly and packaging

Tapeout final layout

Fabrication

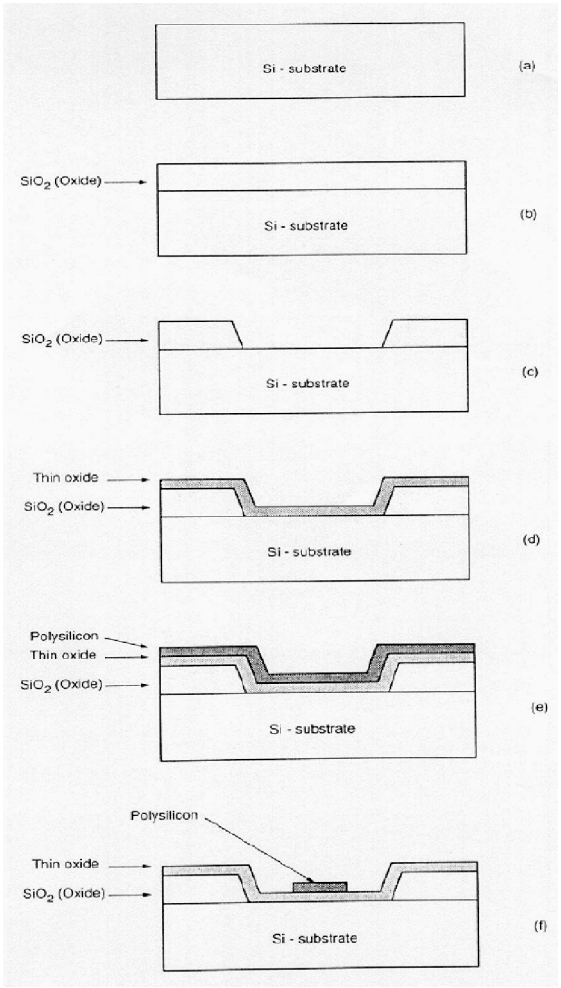
6, 8, 12” wafers

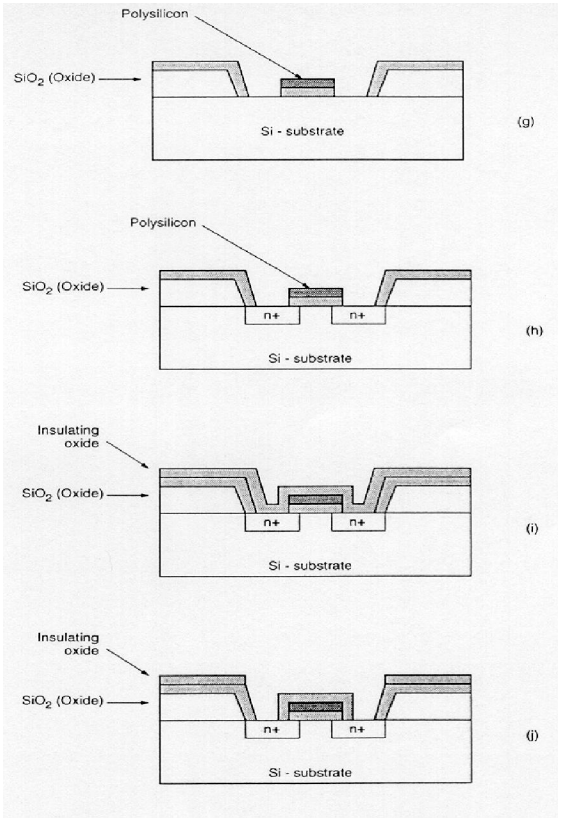
Optimized for throughput, not latency (10 weeks!)

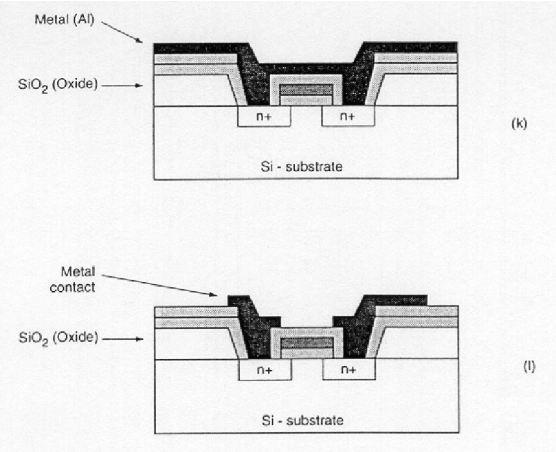
Cut into individual dice

Packaging

Bond gold wires from die I/O pads to package







Advantages

Less power

because each of the devices consumes only a tiny amount of power. In a switching circuit most of the power is consumed switching the charge on the capacitors that connect the switches to each other. In a large IC the components are so small and close together that that capacitance is much smaller, and thus less power.

Less testing.

If you built the same circuit out of discrete ICs and other components, each IC has to be tested (before you use it) for the many different ways it could be used in different applications. for 10000 ICs this is a lot of testing. In a VLSI the components are dedicated to a single use. Further, most are located in the middle of the VLSI and there is no access to them for testing. All you can test is the function the entire circuit was designed for**.**

Reliability.

Over time, we have found that the reliability of an IC is a function of how many connections it has to the outside world. So if the function is constructed with many smaller ICs connected together, then there are many connections, and the reliability is lower. The vlsi has fewer connections, and higher reliability

Limitations

Placement Issues

In order to reconfigure a new hardware, it requires having ample space to place the new hardware. The component placement issue becomes complex if the component needs to be placed near special resources like built- in memory, I/O pins or DLLs on the FPGA.

Routing Issues

Existing components has to be connected to the components newly reconfigured. The ports must be available to interface new components. The same ports must have also been used under the old configuration. To accomplish this orientation of the components should be in a workable fashion.

Timing Issues

Newly configured hardware must meet the timing requirement for the efficient operation of the circuit. Longer wires between components may affect the timing. Optimal speed should be attainable after dynamically reconfiguring the device. Over timing or under timing the new added design may yield erroneous result.

Consistency Issues

Static or dynamic reconfiguration of the device should not degrade computational

consistency of the design. This issue becomes critical when the FPGA is partially reconfigured and interfaced with existing design. Adding new components to the device by reconfigurable fabric should not erase or alter the existing design in the device. (Or memory). There should be some safe methods to store the bit stream to the memory.

Development Tools

Commercial development tools for dynamic reconfigurable computing are still under development stage. The lack of commercially available tools for the specification to implementation stages of the digital design is still a bottleneck. The available tools require enormous human intervention to implement the complete system

Conclusion

The demand for low power VLSI digital circuits in the growing area of portable communications and computing systems will continue to increase in the future. Cost and life cycle of these products will depend not only on low power synthesis techniques, but also on new DFT methods targeting power minimization during test application. This is because the traditional DFT methods are not suitable for testing low power VLSI circuits since they reduce the reliability and manufacturing yield.

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