Unlock the NoC: Transforming NoC Research with Physical Design Awareness

Christopher Batten (Cornell University)
Michael Taylor (University of Washington)

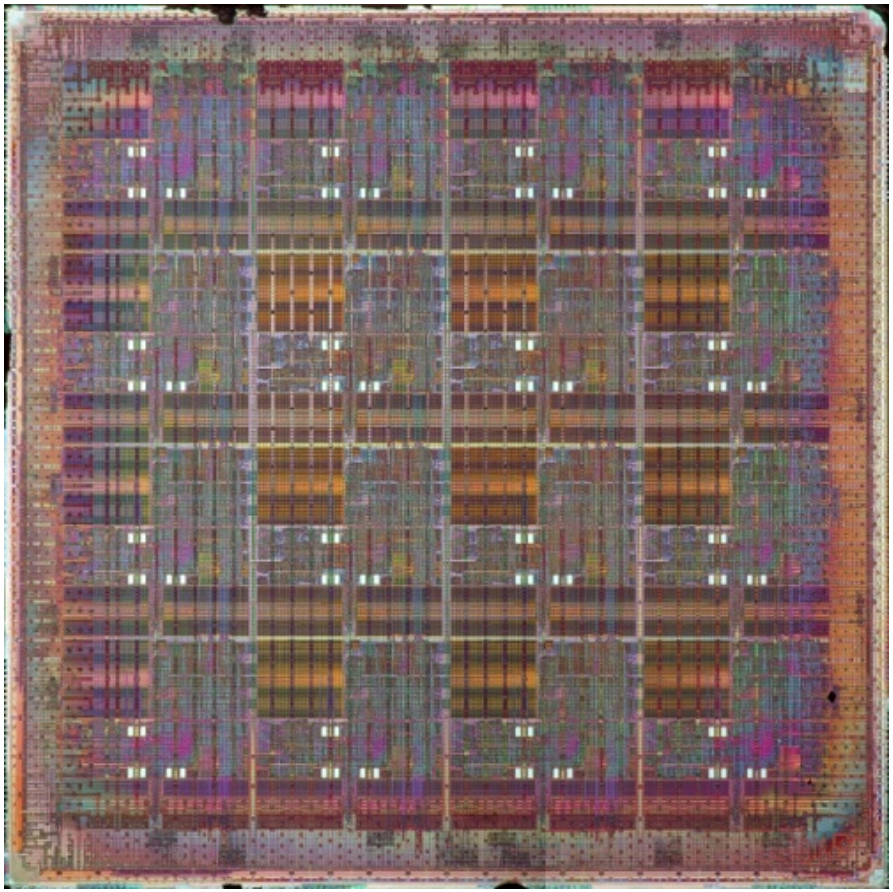
NOCS'20 Special Session

Christopher Batten
Associate Professor, Cornell University
Computer Architecture, EDA, VLSI
Tapeouts in 180/130/28/16nm
Early work on nanophotonic chip-level interconnection networks

Michael Taylor
Associate Professor, University of Washington
Computer Architecture, VLSI
Tapeouts in 180/40/28/16/12nm
Pioneered scalar-operand networks, one of the first academic works on NOCs

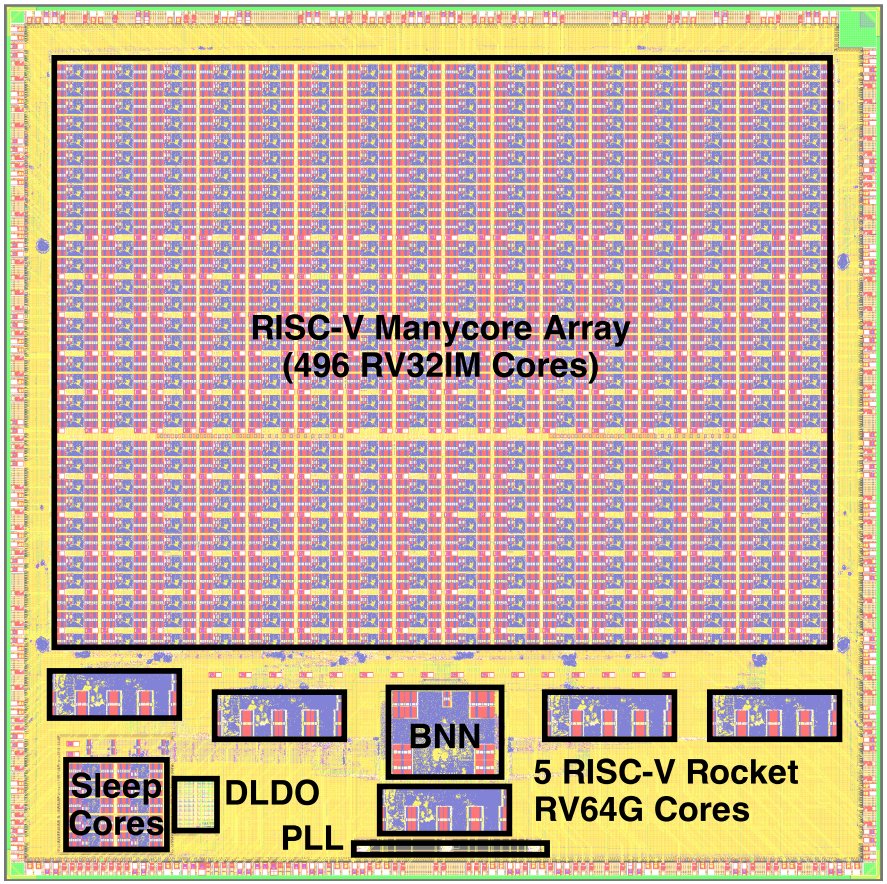
MIT RAW Processor [IEEE-Micro'02,ISSCC'03]

- 18 × 18mm in IBM 180 nm
- 16 MIPS-like cores
- 4×4 mesh network-on-chip
  - 2 statically configured NoCs for scalar operands
  - 2 dynamically routed Nocs for memory traffic
  - XY dimension ordered routing
  - Four physical networks, no VCs



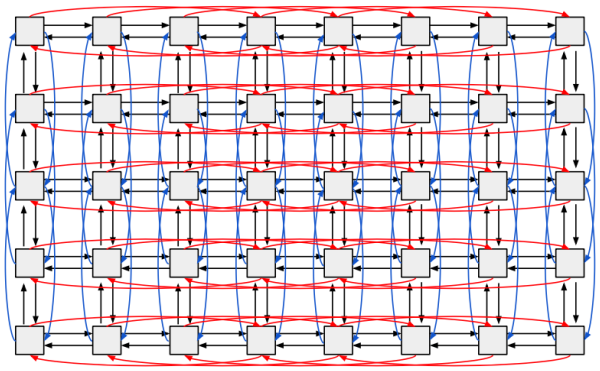
Celerity System-on-Chip [IEEE-Micro'18,VLSI'19]

- 5 × 5mm in TSMC 16 nm FFC
- 385 million transistors
- 511 RISC-V cores
  - 5 Linux-capable Rocket cores
  - 496-core tiled manycore
  - 10-core low-voltage array
- 1 BNN accelerator
- 1 synthesizable PLL
- 1 synthesizable LDO Vreg
- 3 clock domains
- 16×31 mesh network-on-chip
  - Remote-store programming
  - One-cycle router+channel latency
  - XY dimension ordered routing
  - One physical network, no VCs

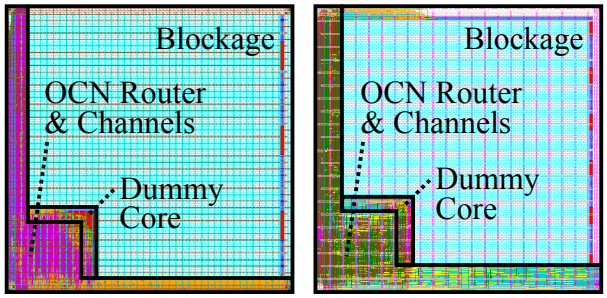


Physical Design Issues

- **Timing Closure:** Must meet both min and max timing constraints across entire chip and multiple corners
- **Silicon Utilization:** Must effectively use both active area and wiring resources without negatively impacting other design issues
- **Power Distribution:** Must ensure no static IR drop nor dI/dt voltage noise issues; carefully balance power grid vs signal routing resources
- **Hierarchical Design:** Carefully consider hard macros which can address some physical design issues while at the same time creating new challenges
- **EDA Tool Runtime:** Must facilitate an agile chip design methodology where we can spin an entire chip in less than a day
- **Signal Integrity:** Global signals must always operate robustly even in the context of voltage noise and aggressor signals
- **Custom Circuits:** Carefully consider the impact of mixing custom and standard-cell-based design methodologies



- **Ruche Networks: Wire-Maximal, No-Fuss NoCs**
  Dai Cheol Jung, Scott Davidson, Chun Zhao, Dustin Richmond, Michael Bedford Taylor (University of Washington)



- **Implementing Low-Diameter On-Chip Networks Using a Tiled Physical Design Methodology**
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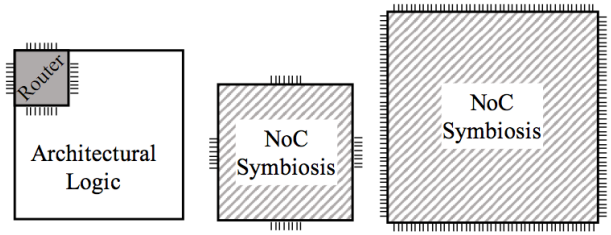
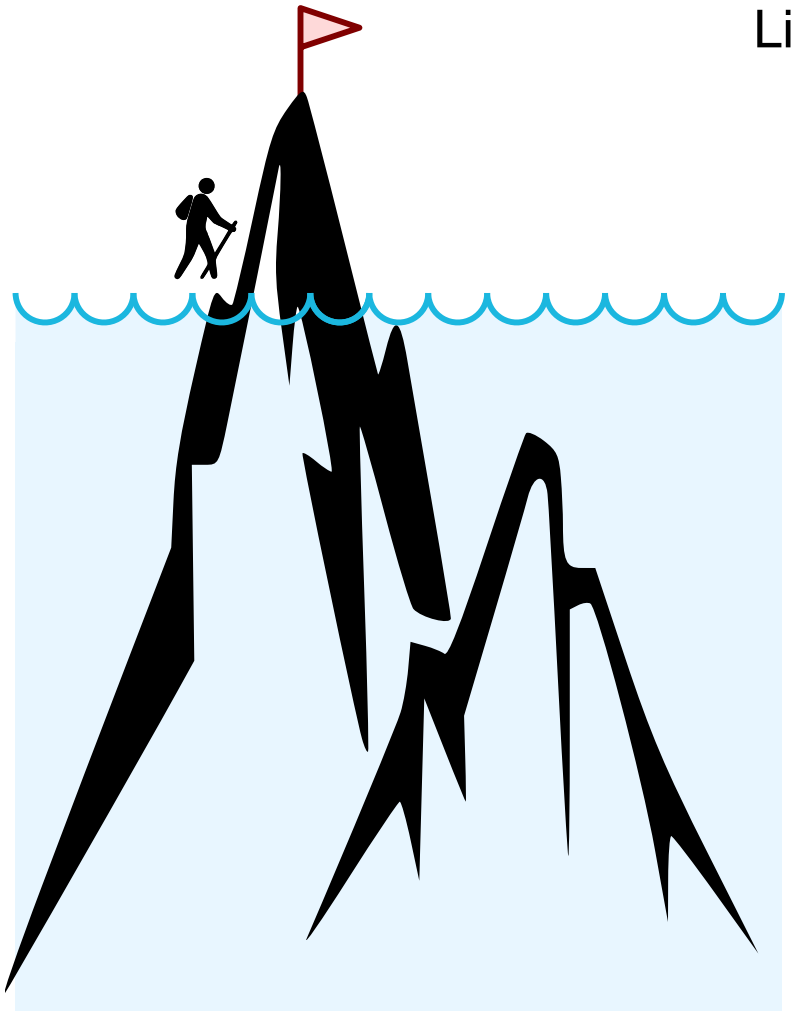


- **NoC Symbiosis**
  Daniel Petrisko, Chun Zhao, Scott Davidson, Paul Gao, Dustin Richmond, Michael Bedford Taylor (University of Washington)

Software Innovation Today



Like climbing an iceberg – much is hidden!

Your proprietary code
- Instagram
- $500K seed with 13 people → $1B

Open-source software
- Python
- Django
- Memcached
- Postgres/SQL
- Redis
- nginx
- Apache, Gnuicorn
- Linux
- GCC

"What Powers Instagram: Hundreds of Instances, Dozens of Technologies" https://goo.gl/76fWrM

Adapted from M. Taylor, “Open Source HW in 2030,” Arch 2030 Workshop @ ISCA’16

Hardware Innovation Today

Like climbing a mountain – nothing is hidden!

What you have to build

- New machine learning accelerator
- Other unrelated components, anything you cannot afford to buy or for which COTS IP does not do

Closed source

- ARM A57, A7, M4, M0
- ARM on-chip interconnect
- Standard cells, I/O pads, DDR Phy
- SRAM memory compilers
- VCS, Modelsim
- DC, ICC, Formality, Primetime
- Stratus, Innovus, Voltus
- Calibre DRC/RCX/LVS, SPICE

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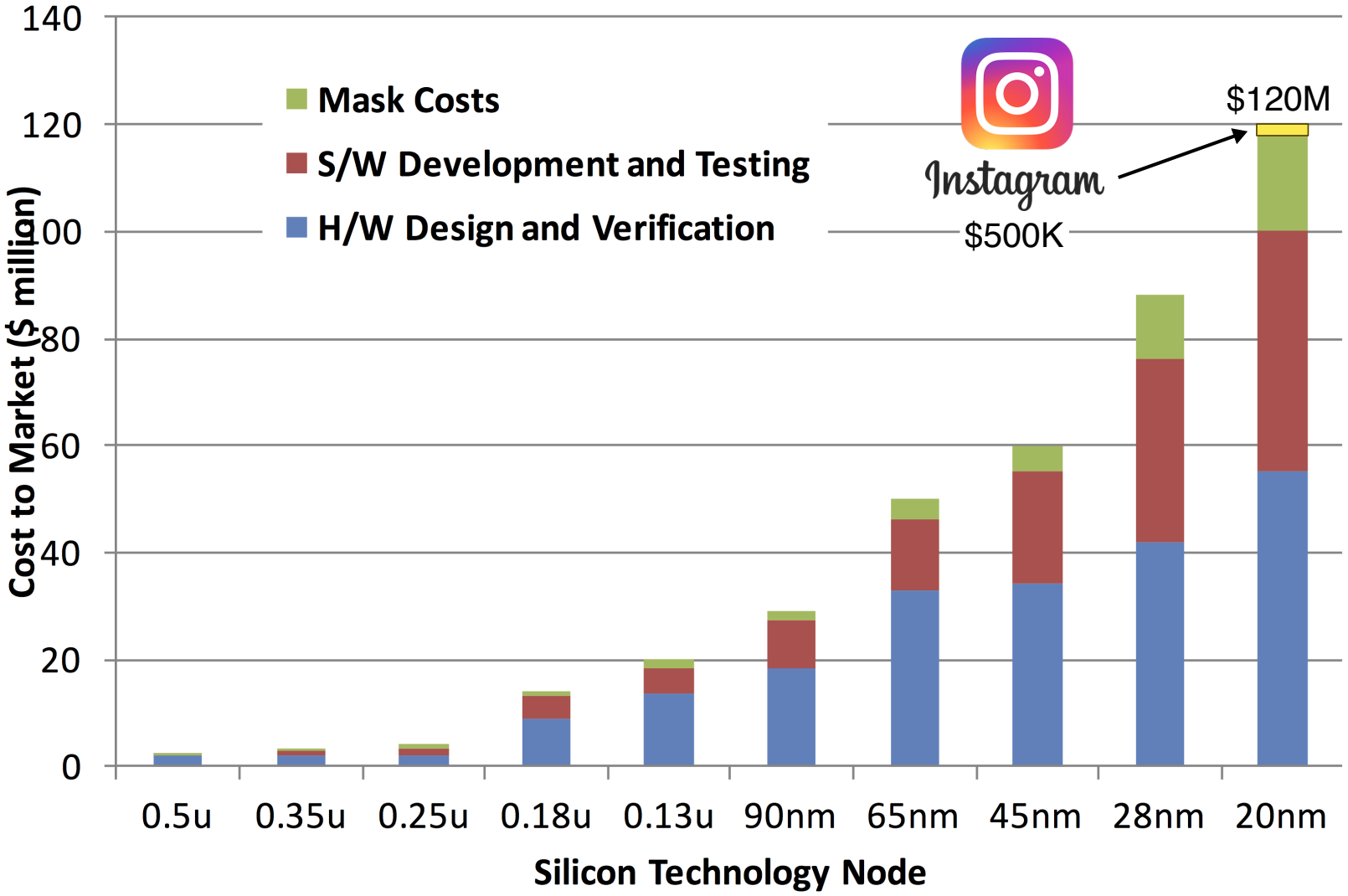
Chip Costs Are Skyrocketing



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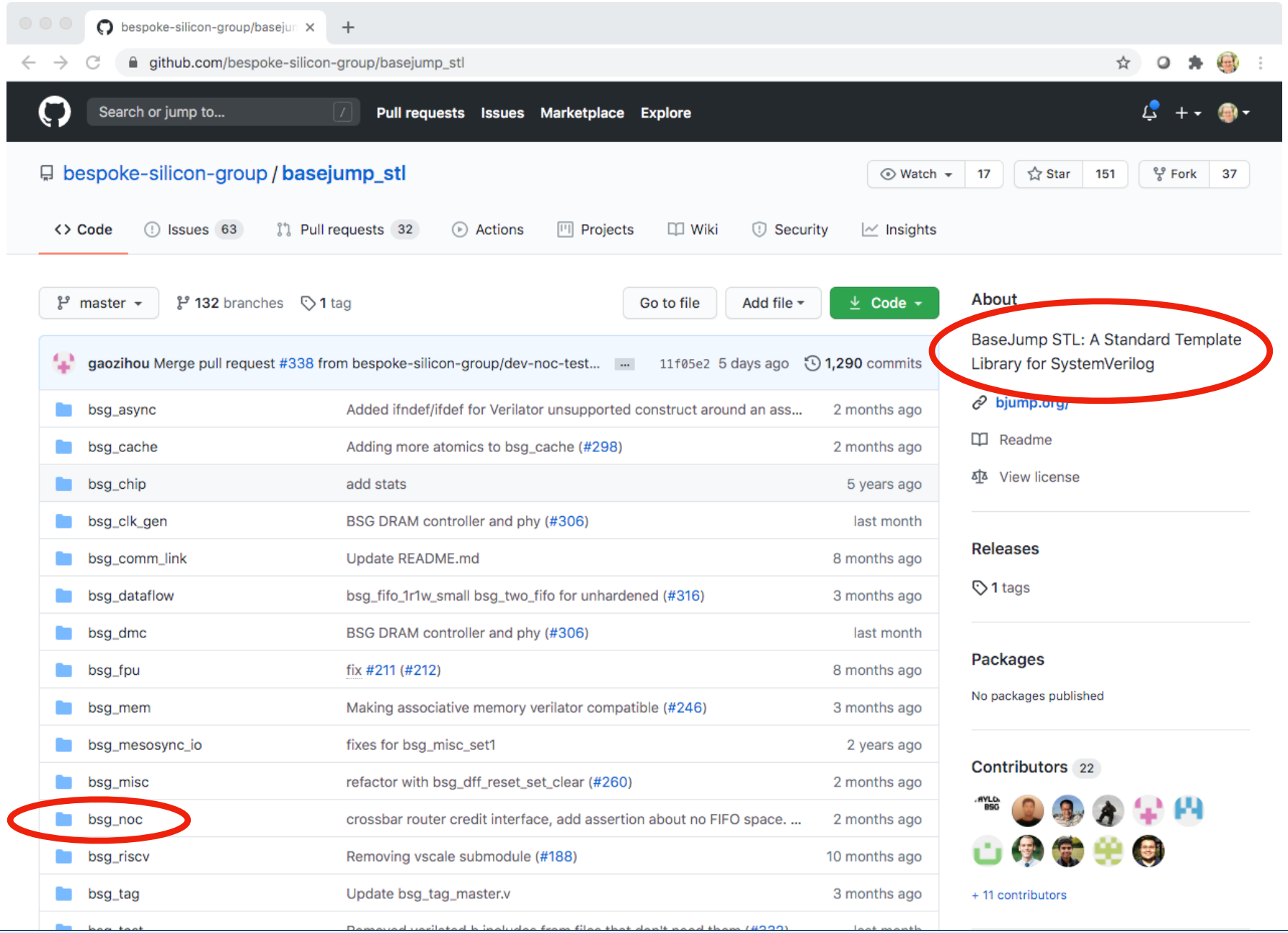
How can HW design be more like SW design?

Open-Source	Software	Hardware
high-level languages	Python, Ruby, R, Javascript, Julia	Chisel, PyMTL, PyRTL, MyHDL, JHDL, Cλash
libraries	C++ STL, Python std libs	**BaseJump, PyOCN**
systems	Linux, Apache, MySQL, memcached	Rocket, Pulp/Ariane, OpenPiton, Boom, FabScalar, MIAOW, Nyuzi
standards	POSIX	RISC-V ISA, RoCC, TileLink
tools	GCC, LLVM, CPython, MRI, PyPy, V8	Icarus Verilog, Verilator, qflow, Yosys, TimberWolf, qrouter, magic, klayout, ngspice
methodologies	agile software design	agile hardware design
cloud	IaaS, elastic computing	IaaS, elastic CAD


bespoke-silicon-group/basejur
github.com/bespoke-silicon-group/basejump_stl
Search or jump to...
Pull requests
Issues
Marketplace
Explore
bespoke-silicon-group / basejump_stl
Watch 17
Star 151
Fork 37
Code
Issues 63
Pull requests 32
Actions
Projects
Wiki
Security
Insights
master
132 branches
1 tag
Go to file
Add file
Code
gaozihou Merge pull request #338 from bespoke-silicon-group/dev-noc-test... 11f05e2 5 days ago 1,290 commits
bsg_async Added ifndef/ifdef for Verilator unsupported construct around an ass... 2 months ago
bsg_cache Adding more atomics to bsg_cache (#298) 2 months ago
bsg_chip add stats 5 years ago
bsg_clk_gen BSG DRAM controller and phy (#306) last month
bsg_comm_link Update README.md 8 months ago
bsg_dataflow bsg_fifo_1r1w_small bsg_two_fifo for unhardened (#316) 3 months ago
bsg_dmc BSG DRAM controller and phy (#306) last month
bsg_fpu fix #211 (#212) 8 months ago
bsg_mem Making associative memory verilator compatible (#246) 3 months ago
bsg_mesosync_io fixes for bsg_misc_set1 2 years ago
bsg_misc refactor with bsg_dff_reset_set_clear (#260) 2 months ago
bsg_noc crossbar router credit interface, add assertion about no FIFO space. ... 2 months ago
bsg_riscv Removing vscale submodule (#188) 10 months ago
bsg_tag Update bsg_tag_master.v 3 months ago
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BaseJump STL: A Standard Template Library for SystemVerilog
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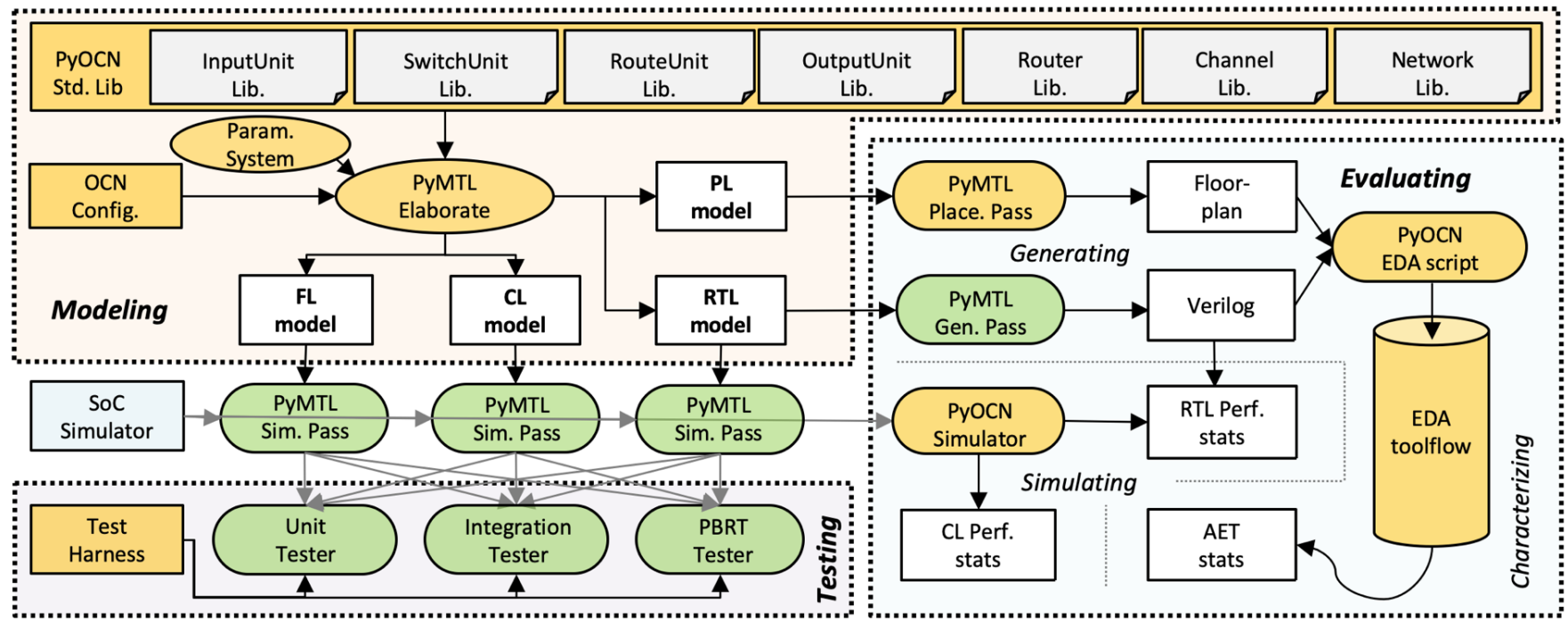
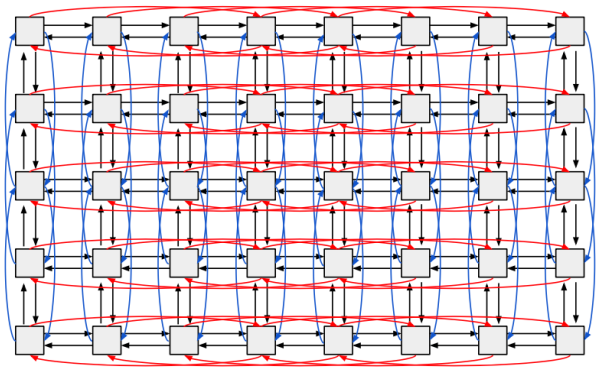
PyOCN: A Unified Framework for Modeling, Testing, and Evaluating OCNs



- Implemented using PyMTL3, a new Python modeling, generation, simulation, and verification framework [IEEE Micro'20, IEEE D&T '20]
- `https://github.com/pymtl/pymtl3-net`



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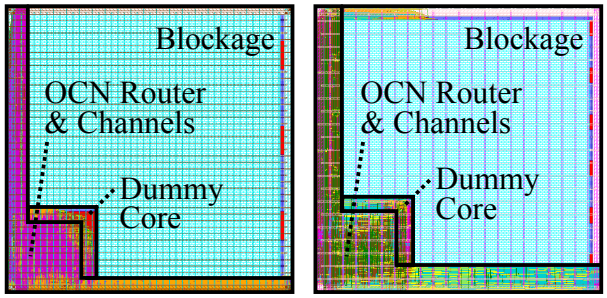

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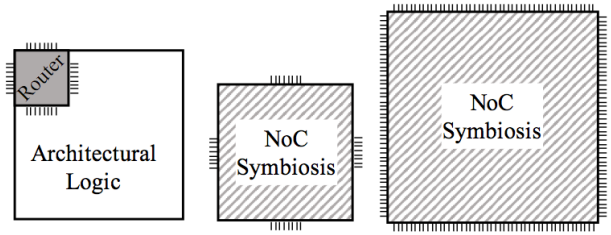

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