
Working with the PADS to Allegro Translator

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Purpose

This document helps users to translate a PADS ASCII file to an Allegro® PCB Editor file. It also covers scenarios where PCB Editor gives errors or warnings during the translation and explains how to resolve the problems. Although this document covers exhaustive scenarios where PCB Editor gives a warning or error, users can visit <https://support.cadence.com> if the issue is not resolved by the methodology described below.

Audience

Design engineers and CAD groups who intend to translate PADS ASCII data to Allegro PCB Editor. The assumption is that the user has hands on experience using Allegro PCB Editor. Familiarity with PADS Layout will be helpful.

Licensing requirement to run the translator.

The PADS translator can be run on all tiers of Allegro PCB Editor.

What is PADS Translator?

The PADS translator (`pads_in`) imports information from PADS Layout ASCII database files (`.asc`) into Allegro PCB Editor board database files (`.brd`). It is assumed that the PADS databases being translated are completed (placed and routed).

What are PADS PowerPCB and PADS Layout 2005?

These are CAD tools used to design layouts and generate fabrication files for Printed Circuit Boards.

Note: PADS (formerly PowerPCB) is now a part of Mentor Graphics.

You can visit the PADS web site: <http://www.mentor.com/products/pcb-system-design/design-flows/pads/> for more information on the above tools.

Prerequisites for running the translator

- **PADS ASCII file**. (.asc)

PADS Layout creates an ASCII database version file (.asc), which contains all information about decal, part type, part, signal (logical connectivity), route (physical connectivity), and graphics.

The component mapping from PADS ASCII file to Allegro prototypes is given below.

Pads objects	Allegro objects
<i>*TEXT*</i>	<i>Text</i>
<i>*LINES*</i>	<i>Cline or Line</i>
<i>*PART*</i>	<i>Components</i>
<i>*ROUTE*</i>	<i>Pin Cline</i>
<i>*POUR*</i>	<i>Shape</i>
<i>*VIA*</i>	<i>Via</i>
<i>*PARTDECAL*</i>	<i>Package Symbol</i>
<i>*PARTTYPE*</i>	<i>Device Type</i>
<i>LAYER DATA</i>	<i>Class/Subclass</i>
<i>*TESTPOINT*</i>	<i>Testpoint</i>

- **Options file** (.ini)

This is the PADS to Allegro PCB Editor Layer mapping file. The correctness of the Allegro PCB Editor .brd file translated from the PADS database depends on the correctness of the Copper layer mapping in the layer mapping file.

The default pads_in.ini file is located at %CDSROOT%/tools/pcb/bin. Users should make a copy of the pads_in.ini file in their Working folder and modify the same.

Steps involved in the translation

1. Create a PADS ASCII file.
2. Create an options file and map the PADS and Allegro PCB Editor layers.
3. Run the translator.
In case of any errors, the translation fails.
4. Open the log file to view the errors.
5. Correct the error either in the `.asc` or `.ini` files. At times you may need to recreate the `.asc` file.
6. Rerun the translator.
7. Open the translated `.brd` file and review all aspects (pad geometries, symbol geometries, stackup, shapes, and so on.) of the design for completeness and correctness.

Note that the translator does not guarantee 100% translation of everything. You need to edit the design that can be maintained completely within Allegro PCB Editor.

Creating a PADS ASCII Database File

The PADS job file (`.pcb`) must be converted to a PADS ASCII database (`.asc`) that the translator can read. This file contains all decal, part type, part, signal, route, and graphic data that are part of the job file. An ASCII database is self-contained and does not require any information from PADS library files.

Note: The *PADS ASCII input file* is an ASCII export of the PADS database. It should be exported directly from the PADS system and must not be hand-edited.

1. Open PADS and load the JOB database file (`.pcb`) to translate.
2. Re-pour all copper pour areas (if any).
3. Choose *Export — ASCII OUT* to display the ASCII Output form.
4. Choose the *Select All* option to output all data in the database.

Choose this option only if you want to translate the complete database.

5. Select the *PADS Layout V2005.2* format or the latest available.
6. Specify the output file name and click *OK*.

Note: -Many a times the database integrity issues in PADS ASCII file may lead to problems during import. Before creating a PADS ASCII file, run database integrity check in PADS. This can be done by using the keyboard shortcut *i*.

Working with the PADS to Allegro Translator

Creating an options file

The Options file is probably the most important piece of information needed to successfully run the translation.

Allegro is designed around the concept of named CLASSES and SUBCLASSES; Whereas PADS uses the concept of named database layers.

The Options file provides the mapping between PADS *named_database_layers* to Allegro CLASSES and SUBCLASSES.

The PADS designer could work in tandem with Allegro designer when creating the Options file. The PADS designer knows what data is kept on which layer and Allegro designer can then map the layer to the appropriate class/subclass.

Note: As mentioned earlier, if the Options file is not correctly mapped, data will be lost during translation. The `pads_in.log` file lists data that is not mapped.

The default `pads_in.ini` file is located at `%CDSROOT%/tools/pcb/bin`.

You should make a copy of the `pads_in.ini` file in your working folder and modify the same.

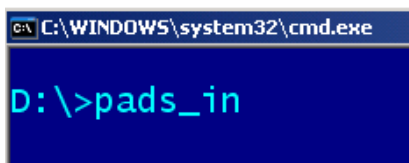
Running the translator

The PADS Layout translators can be run in the batch mode by specifying all required information on the command line, from program menu, or from the tool. All these methods call the `pads_in.exe` executable which exists in

`%CDSROOT%/tools/pcb/bin`.

- a) From DOS prompt.
From a DOS prompt (*Start — Run; cmd*)

Execute `pads_in` command

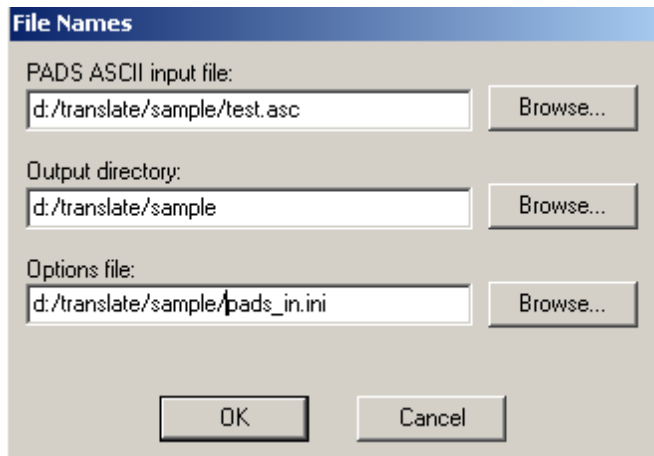


Working with the PADS to Allegro Translator

- b) From *Start — Programs — Cadence*, choose *Release xx.x — PCB Editor Utilities — PADS Translator*.



The above methods of invocation will bring up the File Names window



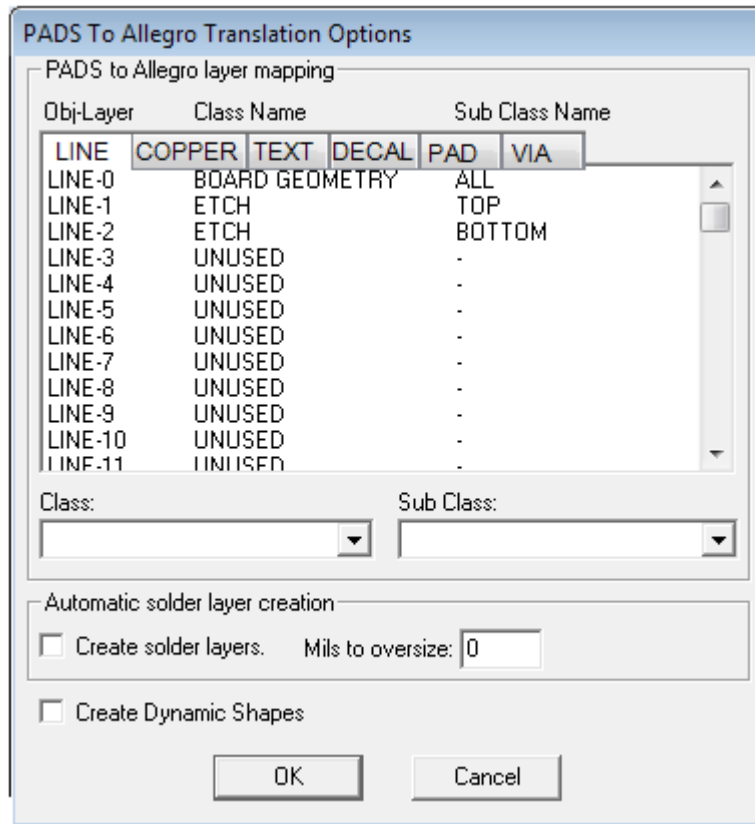
In the fields, enter the following:-

- *PADS ASCII input file:* The PADS ASCII file (.asc) created in the PADS layout tool.
- *Output directory:* Directory in which the output file needs to be created.
- *Options file:* The full path to an options. The default is the pads_in.ini in
%CDSROOT%/tools/pcb/bin

You can use the Browse button to locate the files.
Click OK after you have specified all the information.

Working with the PADS to Allegro Translator

The `pads_in` application reads the input file and determines the number of etch/conductor layers it uses. If all required program arguments are not specified, the PADS To Allegro Translation Options dialog box appears.



The window allows you to modify the `pads_in.ini` file before translation begins.

Avoid editing the default `pads_in.ini` file located at `%CDSROOT%/tools/pcb/bin`. Make a copy of the `pads_in.ini` file in the working folder and modify the same.

The PADS to Allegro Layer Mapping fields define the element-layer mappings. The list box contains all PADS objects (Lines, Copper, Text, Decals, Pads and Vias) and the name of the class and subclass to which to map the objects

Although the default mapping is done according to the `pads (.asc)` file, you can map the class / subclass name, if needed.

Each element appears once for each PADS layer, for a total of 31 entries per element. All 2D lines on PADS layer 0 map are added to the BOARD/SUBSTRATE GEOMETRY class and the subclass ALL, which is not pre-defined. Lines on PADS layer 1 map to the ETCH/CONDUCTOR class and the subclass TOP/SURFACE and so on. The translator presets all-necessary ETCH/CONDUCTOR class mappings by default, even if a previous translation created the options file. This is also true during batch translations.

Working with the PADS to Allegro Translator

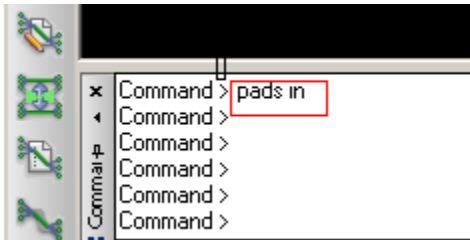
Detailed mapping is described in the section [Changing Class/subclass in layer mapping window](#)

1. In Allegro PCB Editor, either:

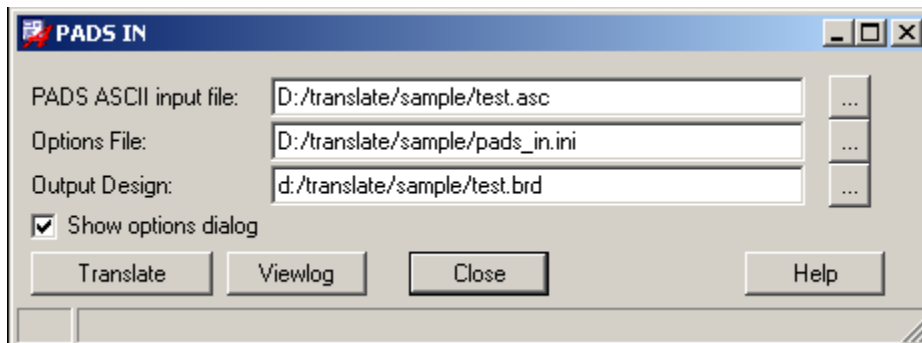
- Choose *File — Import — Cad Translators — PADS*

Or

- In the command window type, *pads in*

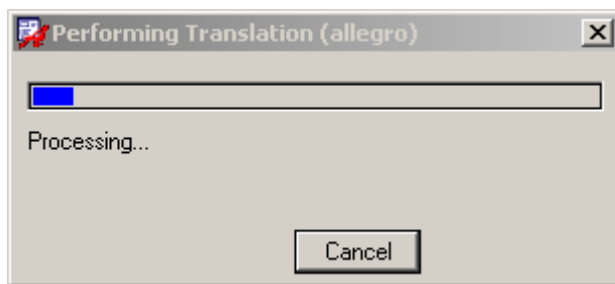


In both the cases the following translator window appears.



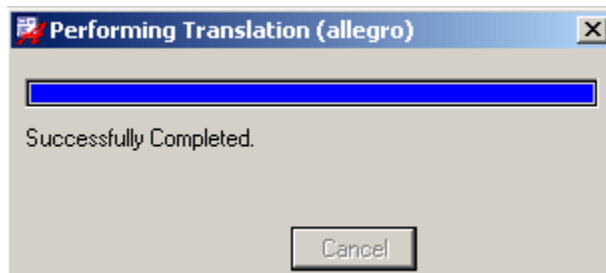
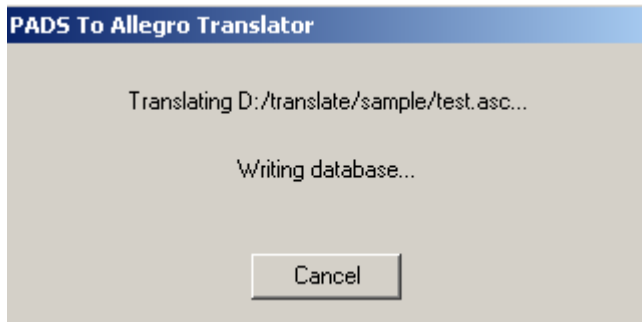
2. Select *Show options dialog* to bring up the PADS to Allegro layer mapping window. If this checkbox is not selected, the translator uses options specified in the .ini file.
3. Click *Translate* to start the translation.

A window appears displaying the progress of the translation process.



Working with the PADS to Allegro Translator

The *PADS to Allegro Translator* window appears, showing each section of the ASCII file that is getting translated.



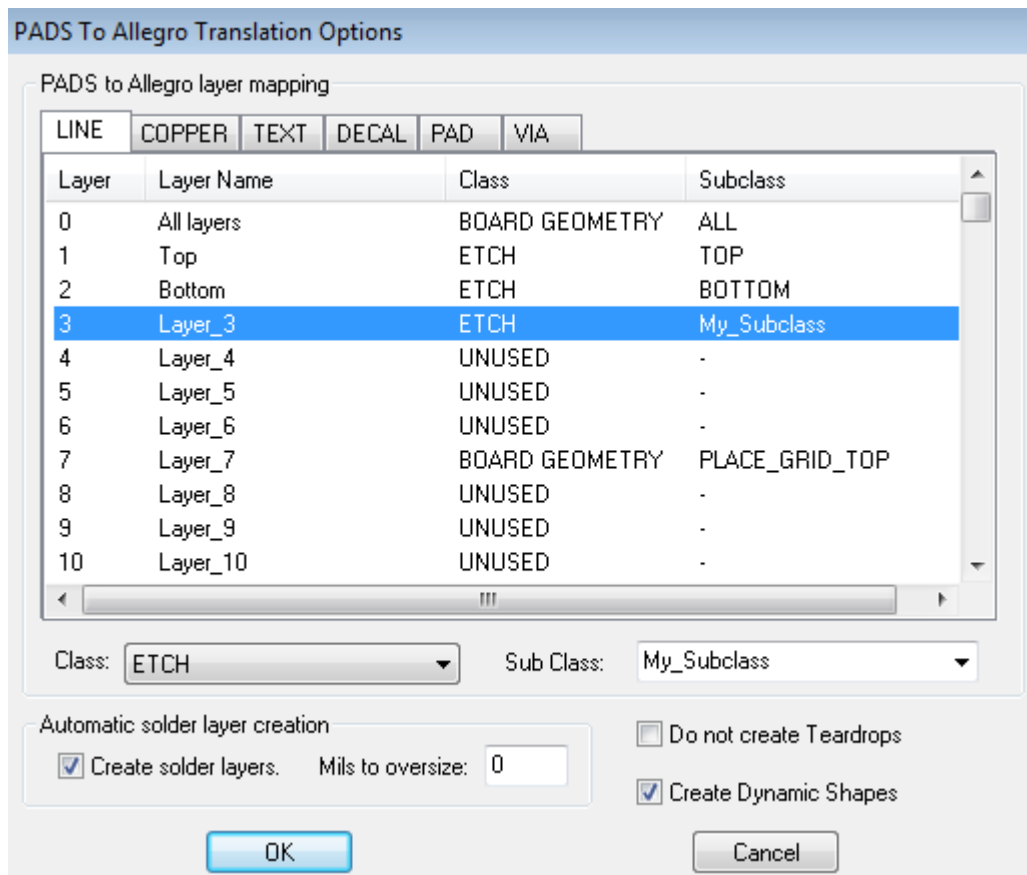
If the translation is successful, the translated .brd file is saved in the folder mentioned in the *Output Design* field.

4. Click *Viewlog* to view the log file. The file is generally created in the Working folder. If translation fails, you can view the log file to see the error and warning messages.

Changing Class/subclass in layer mapping window

When you select an element in the PADS To Allegro Translations Options window, the target class and subclass are shown in the *Class* and *Sub Class* lists.

To change the target class and subclass, select a new class or subclass from the lists. You can also type a new subclass name in the *Sub Class* field.



Note that no new subclasses can be defined for the class *PIN* or *VIA*.

Select *Create solder layers* to create solder mask and solder paste padstack layer entries and to specify the oversize radius in mils.

The solder mask pad layer entry is added to the *SOLDERMASK_TOP* subclass, and the solder paste entry is added to the *PASTEMASK_TOP* subclass. The oversized value is added to the padstack size.

For example, if the oversize is 15, a 60mil pad generates a 75mil solder mask and paste layer entry.

Selecting *Create Dynamic Shapes* creates dynamic shapes from *POUROUT* and *HATOUT* pieces from the *POUR* section.

Click *OK* to continue with the translation.

Files Generated during translation

The following files are generated in the output directory after translation is complete:

<i>pads_in.log</i>	The translator log file.
<i><name>.brd</i>	The board file where <i><name></i> is the name of the ASCII database file. For example, <i>TEST.asc</i> would produce <i>TEST.brd</i> .
<i><name>.txt</i>	The netlist create and used by the translator, where <i><name></i> is the name of the ASCII database.
<i>netin.log</i>	The log file created by the <i>netin</i> contains netlist and command used by the translator.
<i><deviceName>.txt</i>	The device file where <i>deviceName</i> is the name of a device used in the design.
<i>Devices.map</i>	The device name mapping file. This is used because PowerPCB or Pads Layout allows long device (part type) names. You can use this file as a reference to see how names were translated.
<i>Names.map</i>	The Pads name to Allegro PCB Editor name change mapping file. This file is generated whenever there is change in names while translation.
<i>techfile.log</i>	The log file created by the <i>techfile</i> command used by the translator.
<i><name>.dcf</i>	The techfile created and used by the translator, where <i><name></i> is the name of the ASCII database.

Most of these are temporary files generated for use by the translator. They remain in the output directory only for reference. The key file is the Allegro PCB Editor board (*.brd*) file, which you need to edit the design.

Verifying Database after Translation is completed

After the PADS translation finishes, load the board file into Allegro PCB editor. To create a design that can be maintained completely within the Allegro PCB editor, follow these steps:

1. Run viewlog to display the translators' log file. Examine the file for any errors or warnings. Also examine the `netin.log` file for any warnings or errors.

`Pads_in.log` file displays the unmapped layers in the log file for non-etch layer, which has data in it.

For example:

```
=====
PADS layer usage summary:
Layers 1 to 6 are route layers.
LINES:
    0 BOARD GEOMETRY - PLATING_BAR
    3             ETCH - Inner Layer 3
    24 * Not mapped!
COPPER:
TEXT:
    0 BOARD GEOMETRY - ALL
    1             ETCH - TOP
    2             ETCH - Inner Layer 2
    3             ETCH - Inner Layer 3
    4             ETCH - Inner Layer 4
    6             ETCH - BOTTOM
    19 * Not mapped!
    20 * Not mapped!
    21 * Not mapped!
    22 * Not mapped!
    23 * Not mapped!
```

In the above example, the Layer 24 has LINE data and Layer 19 has TEXT data in asc file which is not mapped to Allegro PCB editor Layers in ini file. You need to map this manually to include in the translation.

Working with the PADS to Allegro Translator

2. Choose *Display — Color/Visibility* (`color192` command) to enable the following minimum Class/SubClass:

Board Geometry/Outline

Pin, Via, DRC, and Etch/Conductor in the Stack-Up group

3. Choose *Display — Status* to check for any Unrouted/ Unconnected connections, Out of Date shapes, and DRC errors. Click *Update to Smooth* and *Update DRC* in the same dialog box.

The translator creates place bounds for all package/part symbols based on the boundaries of objects found within the PADS decal.

4. Check constraints for your design. Depending on the version of the tool you are using and the type of constraints you are setting; choose *Setup — Constraints — Constraint Manager* (`cmgr` command).
5. Choose *Tools — Database Check* (`dbdoctor` command) to verify the integrity of the design database. View the log file, and make the necessary corrections.

Constraints Support

PADS Translator also imports the constraints information from the PADS database to Allegro PCB Editor.

In PADS .asc file RULES_SECTION section and all its subsections from the .asc file are translated to Allegro PCB Editor.

Object mapping

The following table represents mapping between PADS and Allegro PCB Editor objects used in the .asc file.

PADS object	Allegro object
RULE_SET	CSet; depending on what rules are defined in PADS, it may be expanded up to 4 csets: spacing, same_net spacing, electrical and physical
NET	Net
NET_CLASS	Class
GROUP	A set of separate from to
CONNECTION	Pin pair
DIFF_PAIR	Diff_pair (see dif_pair translation section)
PAD	Pin
COPPER	Shape
TRACK	Line
BODY	Package

Working with the PADS to Allegro Translator

Constraints mapping

The following table represents mapping between PADS and Allegro constraints with their categories when translated to constraints.

Pads constraints	Allegro constraint	Allegro rule type
<i>CLEARANCE_RULE</i>		
VIA_TO_TRACK	Via to Line	Spacing
VIA_TO_VIA	Via to Via	Spacing
PAD_TO_TRACK	Pin to Line	Spacing
PAD_TO_VIA	Pin to Via	Spacing
PAD_TO_PAD	Pin to Pin	Spacing
SMD_TO_TRACK	SMD to Line	Spacing
SMD_TO_VIA	SMD to Via	Spacing
SMD_TO_PAD	SMD to Pin	Spacing
SMD_TO_SMD	SMD to SMD	Spacing
COPPER_TO_TRACK	Shape to Line	Spacing
COPPER_TO_VIA	Shape to Via	Spacing
COPPER_TO_PAD	Shape to Pin	Spacing
COPPER_TO_SMD	Shape to SMD	Spacing
COPPER_TO_COPPER	Shape to Shape	Spacing
OUTLINE_TO_TRACK	Board edge clearance	Setup -> Outlines -> Board outline
OUTLINE_TO_VIA		
OUTLINE_TO_PAD		
OUTLINE_TO_SMD		
OUTLINE_TO_COPPER		
DRILL_TO_TRACK	Hole to Line	Spacing
DRILL_TO_VIA	Hole to Via	Spacing
DRILL_TO_PAD	Hole to Pin	Spacing
DRILL_TO_SMD	Hole to SMD	Spacing
DRILL_TO_COPPER	Hole to Shape	Spacing
SAME_NET_SMD_TO_VIA	SMD to Via	Samenet Spacing
SAME_NET_VIA_TO_VIA	Via to Via	Samenet Spacing
MIN_TRACK_WIDTH	Min Line Width	Physical
MAX_TRACK_WIDTH	Max Line Width	Physical
DRILL_TO_DRILL	Hole to Hole	Spacing

Working with the PADS to Allegro Translator

BODY_TO_BODY	Package-Package	Setup -> Constraints -> DFA Constraints
HIGH_SPEED_RULE		
MIN_LENGTH	Min total etch Length	Electrical
MAX_LENGTH	Max total etch Length	Electrical
STUB_LENGTH	Wiring/Stub Length	Electrical
PARALLEL_LENGTH	Wiring/Max Parallel	Electrical
PARALLEL_GAP	Max Parallel	Electrical
MIN_DELAY	Propagation delay/Min	Electrical
MAX_DELAY	Propagation delay/Max	Electrical
MIN_IMPEDANCE	Single-line Impedance/ (target - tolerance)	Electrical
MAX_IMPEDANCE	Single-line Impedance/ (target + tolerance)	Electrical
MATCH_LENGTH_TOLERANCE	relative propagation delay	Electrical
ROUTE_RULE		
ROUTE_PRIORITY	ROUTE_PRIORITY	Property
MAX_NUMBER_OF_VIAS	Max Via count	Electrical
VALID_LAYER 1	Allow Etch	Physical
VALID_LAYER 2	Allow Etch	Physical
VALID_VIA_TYPE	vias	Physical
<i>DIFF_PAIR</i>		
MIN_LENGTH	Min total etch Length	Electrical
MAX_LENGTH	Max total etch Length	Electrical
GAP	Differential pair / Primary gap	Physical
WIDTH	Differential pair / Min line width	Physical

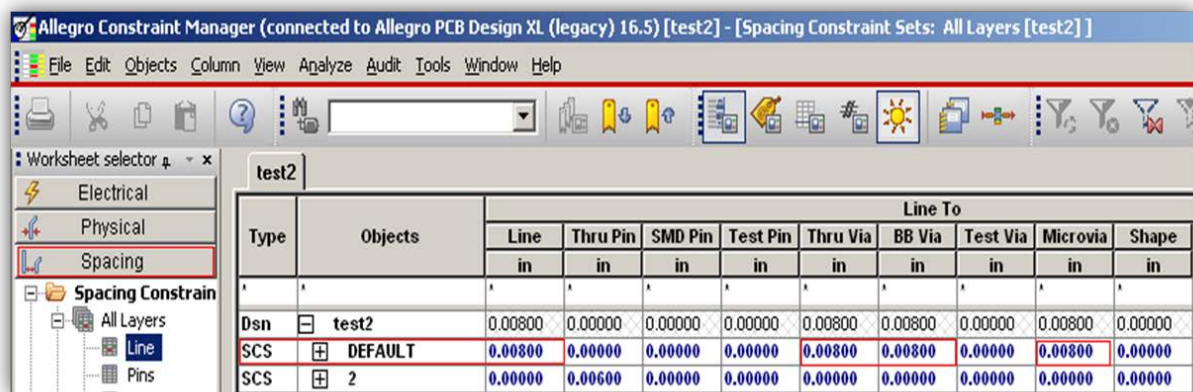
Translation of RULES_SECTION of PADS .asc to the Constraint Manager

Below is a section from the RULES_SECTION

```

RULE_SET (1)
{
  FOR :
  {
    DEFAULT :
  }
  AGAINST :
  {
    DEFAULT :
  }
  LAYER 0
  CLEARANCE_RULE :
  {
    TRACK_TO_TRACK 304800
    VIA_TO_TRACK 304800
    VIA_TO_VIA 304800
    SAME_NET_SMD_TO_VIA 228600
    MIN_TRACK_WIDTH 304800
    MAX_TRACK_WIDTH 2286000
  }
}

```



The screenshot shows the Allegro Constraint Manager window. The 'Spacing' constraint type is selected in the left sidebar. The main table displays the following data:

Type	Objects	Line To								
		Line in	Thru Pin in	SMD Pin in	Test Pin in	Thru Via in	BB Via in	Test Via in	Microvia in	Shape in
Dsn	test2	0.00800	0.00000	0.00000	0.00000	0.00800	0.00800	0.00000	0.00800	0.00000
SCS	DEFAULT	0.00800	0.00000	0.00000	0.00000	0.00800	0.00800	0.00000	0.00800	0.00000
SCS	2	0.00000	0.00600	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000

TRACK_TO_TRACK 304800 > translates to DEFAULT spacing CSet (0.008 inches)

VIA_TO_TRACK 304800 > translates to DEFAULT spacing CSet (0.008 inches)

Working with the PADS to Allegro Translator

Allegro Constraint Manager (connected to Allegro PCB Design XL (legacy) 16.5) [test2] - [Spacing Constraint Sets: All Layers [test2]]

File Edit Objects Column View Analyze Audit Tools Window Help

Worksheet selector ▾ ×

Electrical

Physical

Spacing

Spacing Constrains

All Layers

Line

Pins

Vias

Shape

Bond Finger

Hole

test2

Type	Objects	Thru Via To												
		Line	Thru Pin	SMD Pin	Test Pin	Thru Via	BB Via	Test Via	Microvia	Shape	Bond Finger	Line	Thru Pin	SI
		in	in	in	in	in	in	in	in	in	in	in	in	
Dsn	test2	0.00800	0.00000	0.00000	0.00000	0.00800	0.00800	0.00000	0.00800	0.00000	0.00000	0.00800	0.00000	0.0
SCS	DEFAULT	0.00800	0.00000	0.00000	0.00000	0.00800	0.00800	0.00000	0.00800	0.00000	0.00000	0.00800	0.00000	0.0
SCS	2	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.0
SCS	3	0.00600	0.00600	0.00600	0.00000	0.00600	0.00600	0.00000	0.00600	0.00400	0.00000	0.00600	0.00600	0.0
SCS	4	0.00800	0.00800	0.00800	0.00000	0.00800	0.00800	0.00000	0.00800	0.01500	0.00000	0.00800	0.00800	0.0
SCS	5_10	0.00800	0.00800	0.00800	0.00000	0.00800	0.00800	0.00000	0.00800	0.02000	0.00000	0.00800	0.00800	0.0

VIA_TO_VIA 304800 > translates to DEFAULT spacing CSet (0.008 inches)

Type	Objects	SMD Pin To									
		Line	Thru Pin	SMD Pin	Test Pin	Thru Via	BB Via	Test Via	Microvia	Shape	Bond F
		in	in	in	in	in	in	in	in	in	in
Dsn	test2	0.00000	0.00000	0.00000	0.00000	0.00600	0.00600	0.00000	0.00600	0.00000	0.00000
SHSC	DEFAULT	0.00000	0.00000	0.00000	0.00000	0.00600	0.00600	0.00000	0.00600	0.00000	0.00000
SHSC	2	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000
SHSC	3	0.00000	0.00000	0.00000	0.00000	0.00600	0.00600	0.00000	0.00600	0.00000	0.00000

SAME_NET_SMD_TO_VIA 228600 > translates to DEFAULT same net spacing CSet (0.006 inches)

Type	Objects	Line Width		Heck	
		Min	Max	Min Width	Max Length
		in	in	in	in
Dsn	test2	0.00800	0.06000	0.00000	0.00000
PCS	DEFAULT	0.00800	0.06000	0.00000	0.00000
PCS	2	0.00800	0.00000	0.00000	0.00000

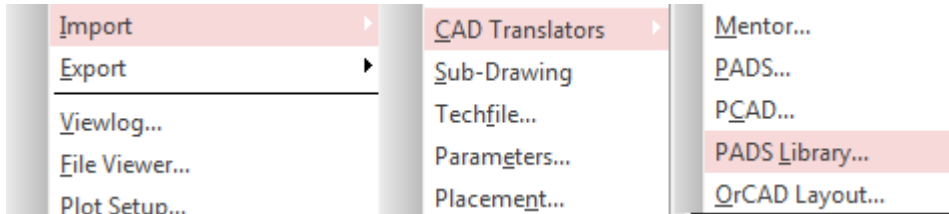
MIN_TRACK_WIDTH 304800 > translates to DEFAULT physical CSet (0.008 inches)

MAX_TRACK_WIDTH 2286000 > translates to DEFAULT physical CSet (0.06 inches)

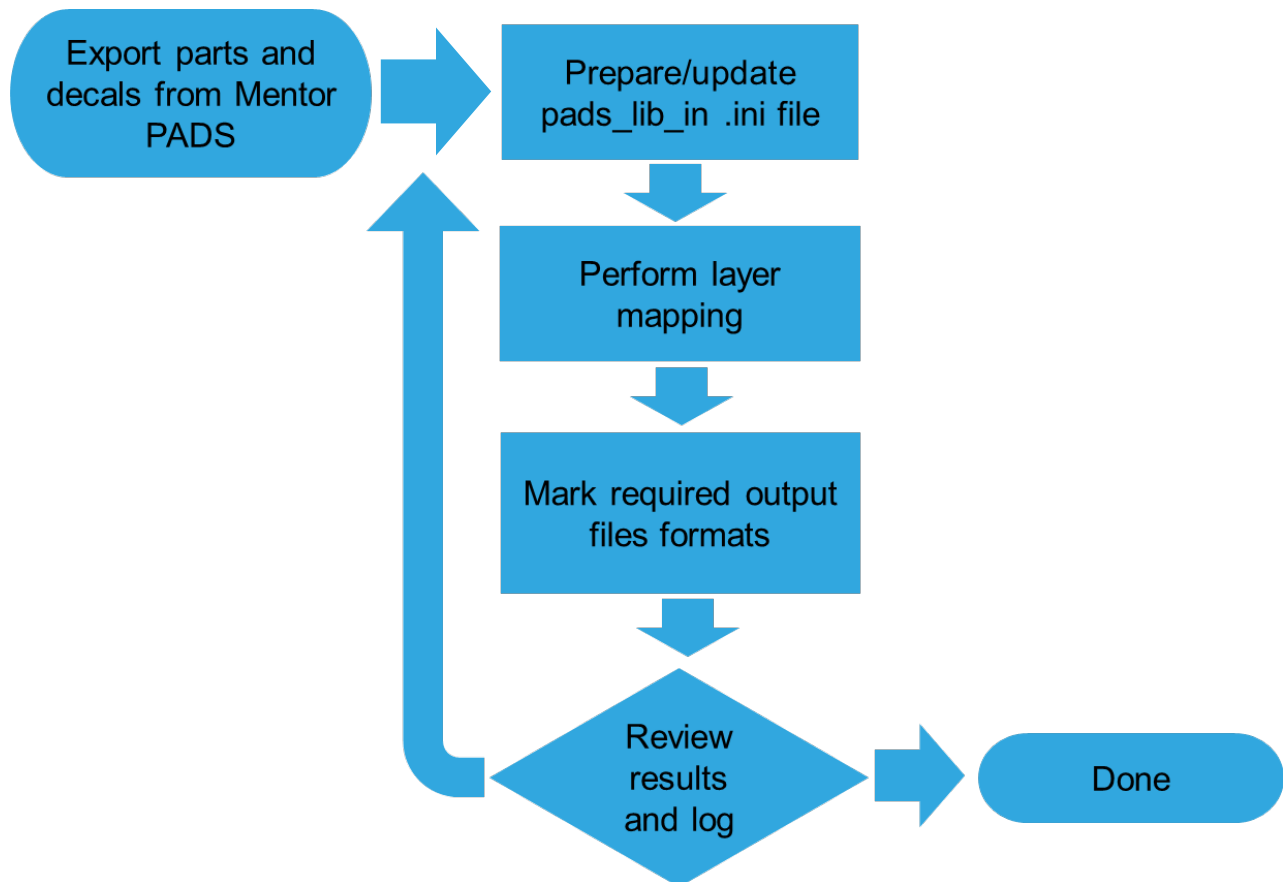
Translating PADS library

From 16.6 onwards, Allegro PCB Editor provides a translator to translate from Mentor PADS physical components library migration to Allegro PCB Editor library database.

The new utility `pads_lib_in` is added to accomplish the migration.



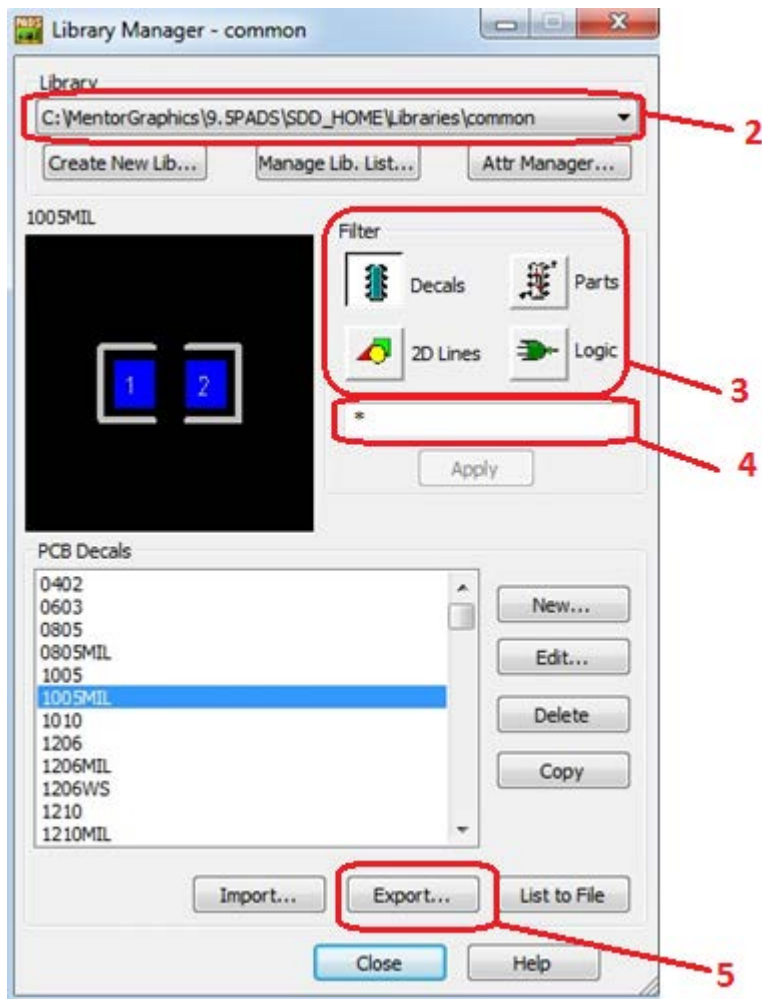
The outlined process covers translating physical component library that includes part types, decals, padstacks, and shapes.



Exporting data from Mentor PADS

Before translating library data they must be exported from PADS Library manager. The export process is following:

1. Open Library Manager by choosing *PADS Layout File — Library*.
2. Select the library for export in the top list
3. Select objects types for export: decals and parts are supported
4. Select objects to export using filter or selection methods
5. Click *Export* to export selection to file (*.d for decals, *.p for parts)



More details about library export process can be found in *PADS Layout User's Guide and Reference Manual*, "Export Library Data" section

Library data mapping

Allegro symbol data is compiled from PADS part type and PCB decal structures. Part type contains primary logical information and references to a number of PCB decals that hold physical implementation. The information is compiled and translated to an Allegro symbol.

- Part Type definition content
 - Part type header
 - Name
 - Reference to PCB decals
 - Units
 - Summary of the part content
 - Attribute information
 - Gate information
 - Signal pin information
 - Alphanumeric pins
- PCB Decal definition
 - PCB Decal header
 - Name
 - Units
 - Summary of the part content
 - Decal attributes
 - Attribute label locations
 - Piece definitions
 - Geometry definition on layers
 - Text definitions
 - Terminal definitions
 - Physical pins location and pin numbers for mapping
 - Pad-stack definitions
 - Pads shapes and layers
 - Drilling, plating, thermal information
 - Custom pad shapes definition

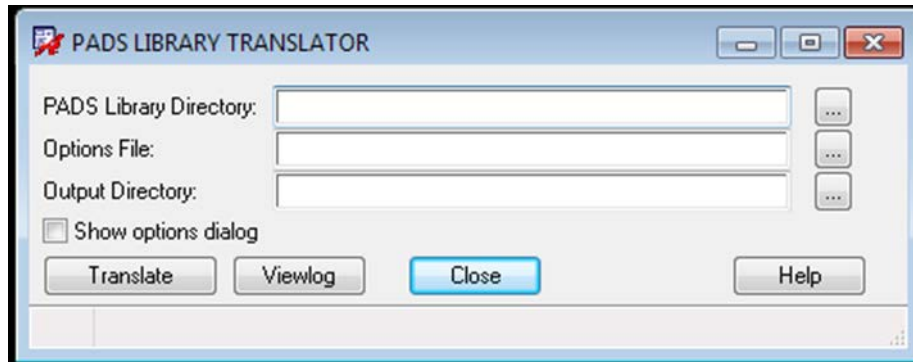
Pads_lib_in translator usage

GUI execution modes

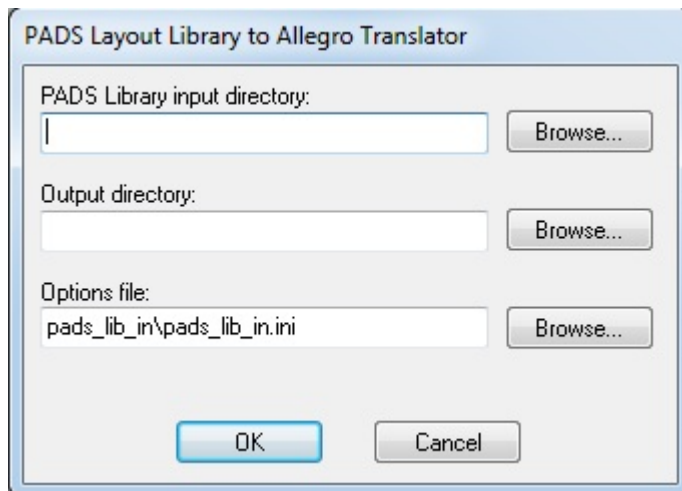
Working with the PADS to Allegro Translator

Translator UI can be executed in two ways:

- From Allegro menu *File – Import — CAD Translators – PADS Library*



- From command line by executing `pads_lib_in`



For both forms the input parameters are:

- Input directory with library part and decal files
- Output directory for resulting allegro library files
- Path to loaded/generated Options .ini file

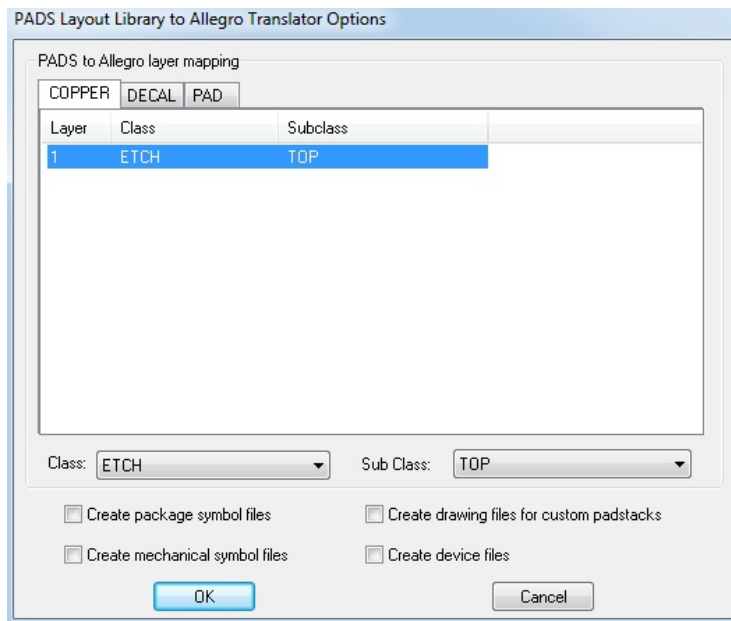
Layer mapping

When *Show option dialog* is enabled and, for standalone run, option dialog pops up and enables layer mapping. In PADS, a layer is designated by a numerical ID, in Allegro it is a class/subclass pair.

You should have clear understanding of the purpose of all layers in the library and explicitly select appropriate class/subclass pair using list boxes at the bottom of dialog. This operation should be performed for all translating object types: copper, decal and pads:

Working with the PADS to Allegro Translator

- Copper layer mapping is used to create etch items (shapes, clines) on top or bottom layer in Allegro.
- Decal layer mapping is used to create package geometry (lines, shapes).
- Pad layer mapping is used to create padstack layers and solder/paste mask.



Non-mapped layers are to be skipped from translation and appropriate objects are missed in target library.

Result files options

By default translator creates *.dra files for each translated component. The format is self-sufficient and includes all required information including padstacks. These are the options for generating other file types:

- Package symbol files (.psm) for placing symbols, .pad files are created for padstacks
- Mechanical symbol files (.bsm) for mechanical symbols (if any)
- Drawing files for padstacks, .ssm files are created for custom pad shapes, .fsm for flash symbols
- Device files (.txt) contain logic information

File generation options are saved to the .ini file and is off by default.

Translation log review

The *pads_lib_in.log* file provides useful information about translation results that can be used for adjusting the next iteration.

Structure of log file:

- PADS Library ASCII files which have been translated: part types and decals
- Created Allegro symbols
- Layer mapping summary including non-mapped layers and missed objects count
- Errors and warnings that occurred during translation
- Summary of library translation and status

Batch translation mode

For translating huge libraries, the translator can be used in batch mode.

Below is the description of available options:

- `-input <input directory name>`: Sets directory with PADS Library ASCII files
- `-output <output directory>`: Sets output directory
- `-opt <options file>`: Sets options file name
- `-psm`: Sets create package symbol files
- `-dev`: Sets create device files
- `-bsm`: Sets create mechanical symbol files
- `-custom`: Sets create drawing files for the custom padstacks

Known problem and their solutions

If you are unable to import PADS database to Allegro PCB Editor, one of the reasons can be database integrity. You can import ASCII file back in PADS PowerPCB and check if it imports successfully. If it results in error messages, try to remove any errors before proceeding further. In PADS PowerPCB, perform a database integrity check by using the keyboard shortcut `i`. After the problems are resolved, export the new ASCII file again and then try to import it into Allegro PCB Editor using *File — Import — CAD Translators — PADS*.

The same could be started with the Allegro command `pads in`.

pads_in translator translates thermal ties with a zero line width.

If `pads_in` translator translates thermal ties to positive planes with a zero line width, use the shareware SKILL program `cwidth.il` that may be downloaded from

[Working with PADS to Allegro Translator](#)

This skill program helps change all zero line widths to the desired width.

pads_in fails with error for illegal characters in ASCII file

Pads ASCII file containing illegal characters in padstack, decals which are not supported by Allegro, fail to execute in `pads_in`.

The lists of illegal characters in translations are

" \$ ~ @ # \$ % ^ & * () = ' " [] ? / < > ! \ . , ; { } ` + | "

Illegal character is replaced with the underscore (`_`) unless the name has already been used for replacement. For example, `abc(de` and `abc<de` may both be replaced with `abc_de`. To avoid duplication, the second term will be replaced with `abc0de`. If `_` leads to duplication, `0-9` will be tried instead.

The error message below indicates that there is an illegal character in Part type which is not parsed in Allegro.

```
PARSE ERROR: Part 'Q2' used an undefine PartType 'nd355anct '. Line
3918: Q2 nd355anct~~ 34921356 38647843 0.000 U
N 0 -1 0 -1 2
ERROR: Finished with errors.
```

Working with the PADS to Allegro Translator

Note that not all illegal characters are currently replaced by Allegro. The *names.map* file generated during the translation contains name change logs from pads to Allegro PCB editor.

Example:

```
# Name changes log file
# Format: <PADS name>    ->    <Allegro name>
WAFER-POGO~~WAFER-POGO    ->    WAFER-POGO WAFER-POGO
```

You may need to change the pads database to remove the illegal characters.

Pads_in fails with no error in log file

When importing a PADS design the translation runs through until it is writing the Allegro PCB Editor database. It then terminates with the error listed in the log file. There are no details indicating what the problem is and there are no clines in the translated design.

Following is written in the `pads_in.log` file:

```
ERROR: Failed while writing the Allegro database.
ERROR: Finished with errors.
```

For example, the problem in a design was the names used for the vias. The via names contained colons (:) that are not legal in Allegro PCB Editor. Replacing the colon with an underscore allowed the translation to complete without any errors.

What is character name limits for pads translation?

Currently the character name limit for pads_in translation is 30 characters. If a name is too long, the first 15 characters are retained in sequence followed by either underscore or any digit from 0 to 9, and then followed by the remaining 14 characters in sequence.

For example, if the name is

abcdefghijklmnopqrstuvwxyzabcdefghijklmnopqrstuvwxyz, it is replaced by
abcdefghijklmnop_lmnopqrstuvwxyz

The constraints in such cases cannot be translated. The log file contains the following error message.

```
ERROR: Unable to load constraints.
```

Pads_in fails with older version of PADS ASCII file.

When trying to import older versions of pads database, `pads_in` fails with the following error in the log file.

```
ERROR: Parse error on line 100.
```

```
ERROR: Finished with errors.
```

Or

```
PARSE ERROR: Unrecognized format in header line of input file.
```

The above error occurs when older versions of PADS ASCII file is given as input to `pads_in`.

The newer version of the ASCII can be exported using PADS version 5 or later by choosing *File — Export — ASCII*.

If a newer version of PADS is not available, export ASCII by changing the version string in the ASCII file.

For example, in the following:

```
!PADS-POWERPCB-V3.0-MILS! DESIGN DATABASE ASCII FILE 1.0
```

Change to the latest version available:

```
!PADS-POWERPCB-V2007.0-MILS! DESIGN DATABASE ASCII FILE 1.0
```

Note that with this method you need to verify the translated design thoroughly. Cadence recommends to output `.asc` (ASCII) file from the PADS layout software.

If you are exporting PADS ASCII (`.asc`) file from any third party translators, manually verify the General Parameters of the PCB design section in the `.asc` file.

Pads_in creates lots of Net shorting DRCs for cross hatch shape.

If the translated board has cross-hatch shapes, there are chances of getting Net shorting DRCs errors on the board.

When importing Pads database with cross-hatch shapes, the line width of the cross hatch shape is translated as 0 units. The lines extend beyond the shape and create shorts with adjacent pins and shapes.

After translation, change these shapes to solid and it can again convert back to cross hatch with desired values for cross hatching to remove net shorting errors.

Artwork fails with below error message on translated board.

While generating artwork for the translated board, the following error message is displayed because of the overlapping voids of two shapes.

```
Found at the bottom of the Artwork Control Form
```

```
Error A problem occurred - please check the logfile.
```

```
Found in the photoplot.log file:
```

```
ERROR: aborting film - Shape with first seg=(45.982 -  
19.140) [layer=BOTTOM]
```

```
has a void with extents [(38.959 -11.658) (59.635 0.372)]  
that touches
```

```
another shape with first seg=(35.306 -3.078). Manually  
resolve problem.
```

```
ERROR: aborting film - artwork will not be generated!
```

```
Error in BOTTOM--halting output. Artwork file not  
generated.
```

```
*** ERROR with BOTTOM
```

This can be resolved using the Cadence Online Solution, refer 'Related Article' section.

Summary

This application note explains the translation from PADS to Allegro PCB Editor database and its Library, It could also help in troubleshooting common translation errors.