

Kintex-7 FPGA Electrical Characteristics

Kintex™-7 FPGAs are available in -3, -2, -1, and -2L speed grades, with -3 having the highest performance. The -2L devices can operate at either of two V_{CCINT} voltages, 0.9V and 1.0V and are screened for lower maximum static power. When operated at $V_{CCINT} = 1.0V$, the speed specification of a -2L device is the same as the -2 speed grade. When operated at $V_{CCINT} = 0.9V$, the -2L performance and static and dynamic power is reduced.

Kintex-7 FPGA DC and AC characteristics are specified in commercial, extended, and industrial temperature ranges. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing

characteristics of a -1 speed grade industrial device are the same as for a -1 speed grade commercial device). However, only selected speed grades and/or devices are available in each temperature range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications.

This Kintex-7 FPGA data sheet, part of an overall set of documentation on the 7 series FPGAs, is available on the Xilinx website at www.xilinx.com/7.

All specifications are subject to change without notice.

Kintex-7 FPGA DC Characteristics

Table 1: Absolute Maximum Ratings ⁽¹⁾

Symbol	Description		Units
V_{CCINT}	Internal supply voltage relative to GND	-0.5 to 1.1	V
V_{CCAUX}	Auxiliary supply voltage relative to GND	-0.5 to 2.0	V
V_{CCAUX_IO}	Auxiliary supply voltage relative to GND	-0.5 to 2.06	V
V_{CCO}	Output drivers supply voltage relative to GND for 3.3V HR I/O banks	-0.5 to 3.6	V
	Output drivers supply voltage relative to GND for 1.8V HP I/O banks	-0.5 to 2.0	V
V_{CCBRAM}	Supply voltage for the block RAM memories	-0.5 to 1.1	V
V_{CCADC}	XADC supply relative to GNDADC	-0.5 to 2.0	V
V_{CCBATT}	Key memory battery backup supply	-0.5 to 2.0	V
V_{REF}	Input reference voltage	-0.5 to 2.0	V
V_{REFP}	XADC reference input relative to GNDADC	-0.5 to 2.0	V
$V_{IN}^{(2)}$	I/O input voltage relative to GND ⁽³⁾ (user and dedicated I/Os)	-0.5 to $V_{CCO} + 0.5$	V
V_{TS}	Voltage applied to 3-state 1.8V or below output ⁽³⁾ (user and dedicated I/Os)	-0.5 to $V_{CCO} + 0.5$	V
T_{STG}	Storage temperature (ambient)	-65 to 150	°C
T_{SOL}	Maximum soldering temperature ⁽⁴⁾	+220	°C
T_j	Maximum junction temperature ⁽⁴⁾	+125	°C

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
- The 3.3V and 1.8V I/O absolute maximum limit applied to DC and AC signals.
- For I/O operation, refer to [UG471: 7 Series FPGAs SelectIO Resources User Guide](#).
- For soldering guidelines and thermal considerations, see [UG475: 7 Series FPGA Packaging and Pinout Specification](#).

Table 2: Recommended Operating Conditions ⁽¹⁾

Symbol	Description	Min	Max	Units
V _{CCINT}	Internal supply voltage relative to GND	0.97	1.03	V
	For -2L (0.9V) devices: internal supply voltage relative to GND	0.87	0.93	V
V _{CCAUX}	Auxiliary supply voltage relative to GND	1.71	1.89	V
V _{CCAUX_IO}	Auxiliary supply voltage when set to 1.8V relative to GND	1.71	1.89	V
	Auxiliary supply voltage when set to 2.0V relative to GND	1.94	2.06	V
V _{CCO} ⁽²⁾⁽⁴⁾	Supply voltage for 3.3V HR I/O banks relative to GND	1.14	3.465	V
	Supply voltage for 1.8V HP I/O banks relative to GND	1.14	1.89	V
V _{CCBRAM}	Block RAM supply voltage	0.97	1.03	V
V _{CCBATT} ⁽³⁾	Battery voltage relative to GND	1.0	1.98	V
V _{IN}	I/O input voltage relative to GND	GND – 0.20	V _{CCO} + 0.2	V
I _{IN} ⁽⁵⁾	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	–	10	mA
T _j	Junction temperature operating range for commercial (C) temperature devices	0	85	°C
	Junction temperature operating range for extended (E) temperature devices	0	100	°C
	Junction temperature operating range for industrial (I) temperature devices	–40	100	°C

Notes:

1. All voltages are relative to ground.
2. Configuration data is retained even if V_{CCO} drops to 0V.
3. V_{CCBATT} is required only when using bitstream encryption. If battery is not used, connect V_{CCBATT} to either ground or V_{CCAUX}.
4. Includes V_{CCO} of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V.
5. A total of 100 mA per bank should not be exceeded.

Table 3: DC Characteristics Over Recommended Operating Conditions

Symbol	Description	Min	Typ ⁽¹⁾	Max	Units
V _{DRINT}	Data retention V _{CCINT} voltage (below which configuration data might be lost)	0.75	–	–	V
V _{DRI}	Data retention V _{CCAUX} voltage (below which configuration data might be lost)	1.5	–	–	V
I _{REF}	V _{REF} leakage current per pin		15		μA
I _L	Input or output leakage current per pin (sample-tested)		15		μA
C _{IN} ⁽²⁾	Die input capacitance at the pad		8		pF
I _{RPU}	Pad pull-up (when selected) @ V _{IN} = 0V, V _{CCO} = 3.3V		330		μA
	Pad pull-up (when selected) @ V _{IN} = 0V, V _{CCO} = 2.5V		250		μA
	Pad pull-up (when selected) @ V _{IN} = 0V, V _{CCO} = 1.8V		180		μA
	Pad pull-up (when selected) @ V _{IN} = 0V, V _{CCO} = 1.5V		150		μA
	Pad pull-up (when selected) @ V _{IN} = 0V, V _{CCO} = 1.2V		120		μA
I _{RPD}	Pad pull-down (when selected) @ V _{IN} = 3.3V		330		μA
	Pad pull-down (when selected) @ V _{IN} = 1.8V		180		μA
I _{BATT} ⁽³⁾	Battery supply current		150		nA
n	Temperature diode ideality factor		1.0002		–
r	Series resistance		2		Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. This measurement represents the die capacitance at the pad, not including the package.
3. Maximum value specified for worst case process at 25°C.

Static Power Consumption

Table 4: Typical Quiescent Supply Current

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
I _{CCINTQ}	Quiescent V _{CCINT} supply current	XC7K70T					mA
		XC7K160T					mA
		XC7K325T					mA
		XC7K355T					mA
		XC7K410T					mA
		XC7K420T					mA
		XC7K480T					mA
I _{CCOQ}	Quiescent V _{CCO} supply current	XC7K70T					mA
		XC7K160T					mA
		XC7K325T					mA
		XC7K355T					mA
		XC7K410T					mA
		XC7K420T					mA
		XC7K480T					mA

Table 4: Typical Quiescent Supply Current (Cont'd)

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
I _{CCAUXQ}	Quiescent V _{CCAUX} supply current	XC7K70T					mA
		XC7K160T					mA
		XC7K325T					mA
		XC7K355T					mA
		XC7K410T					mA
		XC7K420T					mA
		XC7K480T					mA
I _{CCAUX_IOQ}	Quiescent V _{CCAUX_IO} supply current	XC7K70T					mA
		XC7K160T					mA
		XC7K325T					mA
		XC7K355T					mA
		XC7K410T					mA
		XC7K420T					mA
		XC7K480T					mA
I _{CCBRAMQ}	Quiescent V _{CCBRAM} supply current	XC7K70T					mA
		XC7K160T					mA
		XC7K325T					mA
		XC7K355T					mA
		XC7K410T					mA
		XC7K420T					mA
		XC7K480T					mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j) with single-ended SelectIO resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the XPower™ Estimator (XPE) spreadsheet tool (download at <http://www.xilinx.com/power>) to calculate static power consumption for conditions other than those specified.

Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT} , V_{CCBRAM} , V_{CCAUX} , V_{CCAUX_IO} , and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCBRAM} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If V_{CCAUX} , V_{CCAUX_IO} , and V_{CCO} have the same recommended voltage levels then they can be powered by the same supply and ramped simultaneously.

For V_{CCO} voltages of 3.3V in HR I/O banks and configuration bank 0:

- The voltage difference between V_{CCO} and V_{CCAUX} must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

There are no sequencing requirements for the GTX transceiver supplies with respect to the other FPGA supply voltages.

Table 5 shows the minimum current, in addition to I_{CCO} , that are required by Kintex-7 devices for proper power-on and configuration. If the current minimums shown in Table 4 and Table 5 are met, the device powers on after all five supplies have passed through their power-on reset threshold voltages. The FPGA must not be configured until after V_{CCINT} is applied.

Once initialized and configured, use the XPower tools to estimate current drain on these supplies.

Table 5: Power-On Current for Kintex-7 Devices

Device	$I_{CCINTMIN}$	$I_{CCAUXMIN}$	I_{CCOMIN}	I_{CCAUX_IO}	I_{CCBRAM}	Units
	Typ ⁽¹⁾	Typ ⁽¹⁾	Typ ⁽¹⁾	Typ ⁽¹⁾	Typ ⁽¹⁾	
XC7K70T						mA
XC7K160T						mA
XC7K325T						mA
XC7K355T						mA
XC7K410T						mA
XC7K420T						mA
XC7K480T						mA

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. Use the XPower Estimator (XPE) spreadsheet tool (download at <http://www.xilinx.com/power>) to calculate maximum power-on currents.

Table 6: Power Supply Ramp Time

Symbol	Description	Conditions	Min	Max	Units
T_{VCCINT}	Ramp time from GND to 90% of V_{CCINT}		0.2	50	ms
T_{VCCO}	Ramp time from GND to 90% of V_{CCO}		0.2	50	ms
T_{VCCAUX}	Ramp time from GND to 90% of V_{CCAUX}		0.2	50	ms
T_{VCCAUX_IO}	Ramp time from GND to 90% of T_{VCCAUX_IO}		0.2	50	ms
$T_{VCCBRAM}$	Ramp time from GND to 90% of V_{CCBRAM}		0.2	50	ms
$T_{VCCO2VCCAUX}$	Allowed time per power cycle for $V_{CCO} - V_{CCAUX} > 2.625V$	$T_J = 100^{\circ}C^{(1)}$	–	500	ms
		$T_J = 85^{\circ}C^{(1)}$	–	800	
$T_{MGTAVCC}$	Ramp time from GND to 90% of $MGTAVCC$		0.2	50	ms
$T_{MGTAVTT}$	Ramp time from GND to 90% of $MGTAVTT$		0.2	50	ms
$T_{MGTVCCAUX}$	Ramp time from GND to 90% of $MGTVCCAUX$		0.2	50	ms

Notes:

- Based on 240,000 power cycles with nominal V_{CCO} of 3.3V or 36,500 power cycles with a worst case V_{CCO} of 3.465V.

SelectIO™ DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 7: SelectIO DC Input and Output Levels (1)(2)

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	8	-8
HSTL_I_12	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	25% V_{CCO}	75% V_{CCO}	6.3	-6.3
HSTL_I_18	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	8	-8
HSTL_II	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	16	-16
HSTL_II_18	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	16	-16
HSUL_12	-0.300	$V_{REF} - 0.120$	$V_{REF} + 0.120$	$V_{CCO} + 0.300$	$V_{REF} - 0.12$	$V_{REF} + 0.120$		
LVC MOS12	-0.300	35% V_{CCO}	65% V_{CCO}	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	Note 3	Note 3
LVC MOS15, LVDCI_15	-0.300	30% V_{CCO}	70% V_{CCO}	$V_{CCO} + 0.300$	25% V_{CCO}	75% V_{CCO}	Note 4	Note 4
LVC MOS18, LVDCI_18	-0.300	35% V_{CCO}	65% V_{CCO}	$V_{CCO} + 0.300$	0.450	$V_{CCO} - 0.450$	Note 5	Note 5
LVC MOS25	-0.300	0.700	1.700	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	Note 6	Note 6
LVC MOS33	-0.300	0.800	2.000	3.450	0.400	$V_{CCO} - 0.400$	Note 6	Note 6
LV TTL	-0.300	0.800	2.000	3.450	0.400	2.400	Note 7	Note 7
MOBILE_DDR	-0.300	20% V_{CCO}	80% V_{CCO}	$V_{CCO} + 0.300$	10% V_{CCO}	90% V_{CCO}	0.1	-0.1
PCI33_3	-0.500	30% V_{CCO}	50% V_{CCO}	$V_{CCO} + 0.500$	10% V_{CCO}	90% V_{CCO}	1.5	-0.5
SSTL12	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	$V_{REF} - 0.150$	$V_{REF} + 0.150$		
SSTL135	-0.300	$V_{REF} - 0.900$	$V_{REF} + 0.900$	$V_{CCO} + 0.300$	$V_{REF} - 0.150$	$V_{REF} + 0.150$		
SSTL135_R	-0.300	$V_{REF} - 0.900$	$V_{REF} + 0.900$	$V_{CCO} + 0.300$	$V_{REF} - 0.150$	$V_{REF} + 0.150$		
SSTL15	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	$V_{TT} - 0.175$	$V_{TT} + 0.175$	17.8	-17.8
SSTL15_R	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	$V_{TT} - 0.175$	$V_{TT} + 0.175$		
SSTL18_I	-0.300	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCO} + 0.300$	$V_{TT} - 0.470$	$V_{TT} + 0.470$	8	-8
SSTL18_II	-0.300	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCO} + 0.300$	$V_{TT} - 0.600$	$V_{TT} + 0.600$	13.4	-13.4

Notes:

1. Tested according to relevant specifications.
2. 3.3V and 2.5V standards are only supported in 3.3V I/O banks.
3. Supported drive strengths of 2, 4, 6, or 8 mA in HP I/O banks and 4, 8, or 12 mA in HR I/O banks.
4. Supported drive strengths of 2, 4, 6, 8, 12, or 16 mA in HP I/O banks and 4, 8, 12, or 16 mA in HR I/O banks.
5. Supported drive strengths of 2, 4, 6, 8, 12, or 16 mA in HP I/O banks and 4, 8, 12, 16, or 24 mA in HR I/O banks.
6. Supported drive strengths of 4, 8, 12, or 16 mA
7. Supported drive strengths of 4, 8, 12, 16, or 24 mA
8. For detailed interface specific DC voltage levels, see [UG471: 7 Series FPGAs SelectIO Resources User Guide](#).

Table 8: Differential SelectIO DC Input and Output Levels

I/O Standard	V _{ICM} ⁽¹⁾			V _{ID} ⁽²⁾			V _{OCM} ⁽³⁾			V _{OD} ⁽⁴⁾		
	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max
MINI_LVDS_25	0.300	1.200	V _{CCAUX}	0.200	0.400	0.600	1.000	1.200	1.400	0.300	0.450	0.600
PPDS_25	0.200	0.900	V _{CCAUX}	0.100	0.250	0.400	0.500	0.950	1.400	0.100	0.250	0.400
RSDS_25	0.300	0.900	1.500	0.100	0.350	0.600	1.000	1.200	1.400	0.100	0.350	0.600
TMDS_33	2.700	2.965	3.230	0.150	0.675	1.200	V _{CCO} -0.405	V _{CCO} -0.300	V _{CCO} -0.190	0.400	0.600	0.800

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q - Q̄).
3. V_{OCM} is the output common mode voltage.
4. V_{OD} is the output differential voltage (Q - Q̄).
5. LVDS_25 is specified in Table 10.
6. LVDS is specified in Table 11.

Table 9: Complementary Differential SelectIO DC Input and Output Levels

I/O Standard	V _{ICM} ⁽¹⁾			V _{ID} ⁽²⁾			V _{OCM} ⁽³⁾			V _{OD} ⁽⁴⁾			V _{OX} ⁽⁵⁾			V _{OL} ⁽⁶⁾	V _{OH} ⁽⁷⁾
	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Max	V, Min
BLVDS_25		1.250		0.100				1.250					N/A	N/A	N/A	N/A	N/A
DIFF_HSTL_I		0.750		0.100				0.750						0.750		N/A	N/A
DIFF_HSTL_I_18		0.900		0.100				0.900						0.900		N/A	N/A
DIFF_HSTL_II		0.750		0.100				0.750						0.750		N/A	N/A
DIFF_HSTL_II_18		0.900		0.100				0.900						0.900		N/A	N/A
DIFF_MOBILE_DDR		0.900		0.100				0.900						0.900		N/A	N/A
DIFF_SSTL12		0.600		0.100				0.600						0.600			
DIFF_SSTL135		0.675		0.100				0.675						0.675		(V _{CCO} /2) - 0.160	(V _{CCO} /2) + 0.160
DIFF_SSTL15		0.750		0.100				0.750						0.750		(V _{CCO} /2) - 0.175	(V _{CCO} /2) + 0.175
DIFF_SSTL18_I		0.900		0.100				0.900						0.900		N/A	N/A
DIFF_SSTL18_II		0.900		0.100				0.900						0.900		N/A	N/A

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q - Q̄).
3. V_{OCM} is the output common mode voltage.
4. V_{OD} is the output differential voltage (Q - Q̄).
5. V_{OX} is the output crossing voltage (see JEDEC specifications for SSTL)
6. V_{OL} is the single-ended low-output voltage.
7. V_{OH} is the single-ended high-output voltage.

LVDS DC Specifications (LVDS_25)

The LVDS_25 standard is available in the HR I/O banks. See [UG471: 7 Series FPGAs SelectIO Resources User Guide](#) for more information.

Table 10: LVDS_25 DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V _{CCO}	Supply Voltage		2.375	2.500	2.625	V
V _{OH}	Output High Voltage for Q and \bar{Q}	R _T = 100 Ω across Q and \bar{Q} signals	–	–	1.675	V
V _{OL}	Output Low Voltage for Q and \bar{Q}	R _T = 100 Ω across Q and \bar{Q} signals	0.825	–	–	V
V _{ODIFF}	Differential Output Voltage (Q – \bar{Q}), Q = High (\bar{Q} – Q), \bar{Q} = High	R _T = 100 Ω across Q and \bar{Q} signals	247	350	600	mV
V _{OCM}	Output Common-Mode Voltage	R _T = 100 Ω across Q and \bar{Q} signals	1.000	1.250	1.425	V
V _{IDIFF}	Differential Input Voltage (Q – \bar{Q}), Q = High (\bar{Q} – Q), \bar{Q} = High		100	350	600	mV
V _{ICM}	Input Common-Mode Voltage		0.300	1.200	1.425	V

LVDS DC Specifications (LVDS)

The LVDS standard is available in the HP I/O banks. See [UG471: 7 Series FPGAs SelectIO Resources User Guide](#) for more information.

Table 11: LVDS DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V _{CCO}	Supply Voltage		1.710	1.800	1.890	V
V _{OH}	Output High Voltage for Q and \bar{Q}	R _T = 100 Ω across Q and \bar{Q} signals	–	–	1.675	V
V _{OL}	Output Low Voltage for Q and \bar{Q}	R _T = 100 Ω across Q and \bar{Q} signals	0.825	–	–	V
V _{ODIFF}	Differential Output Voltage (Q – \bar{Q}), Q = High (\bar{Q} – Q), \bar{Q} = High	R _T = 100 Ω across Q and \bar{Q} signals	247	350	600	mV
V _{OCM}	Output Common-Mode Voltage	R _T = 100 Ω across Q and \bar{Q} signals	1.000	1.250	1.425	V
V _{IDIFF}	Differential Input Voltage (Q – \bar{Q}), Q = High (\bar{Q} – Q), \bar{Q} = High	Common-mode input voltage = 1.25V	100	350	600	mV
V _{ICM}	Input Common-Mode Voltage	Differential input voltage = ±350 mV	0.300	1.200	1.425	V

eFUSE Programming Conditions

Table 12 lists the programming conditions specifically for eFUSE. For more information, see [UG470: 7 Series FPGA Configuration User Guide](#).

Table 12: eFUSE Programming Conditions⁽¹⁾

Symbol	Description	Min	Typ	Max	Units
I _{FS}	V _{CCAUX} supply current	–	–	115	mA
t _j	Temperature range	15	–	125	°C

Notes:

1. The FPGA must not be configured during eFUSE programming.

GTX Transceiver Specifications

GTX Transceiver DC Characteristics

Table 13: Absolute Maximum Ratings for GTX Transceivers⁽¹⁾

Symbol	Description	Min	Max	Units
MGTAVCC	Analog supply voltage for the GTX transmitter and receiver circuits relative to GND	-0.5	1.1	V
MGTAVTT	Analog supply voltage for the GTX transmitter and receiver termination circuits relative to GND	-0.5	1.32	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTX transceiver column	-0.5	1.32	V
MGTVCCAUX	Auxiliary analog Quad PLL (QPLL) voltage supply for the GTX transceivers	-0.5	1.935	V
V _{IN}	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	-0.5	1.26	V
V _{MGTREFCLK}	Reference clock absolute input voltage	-0.5	1.32	V

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Table 14: Recommended Operating Conditions for GTX Transceivers (1)(2)

Symbol	Description	Min	Typ	Max	Units
MGTAVCC	Analog supply voltage for the GTX transmitter and receiver circuits relative to GND	0.97	1.0	1.03	V
MGTAVTT	Analog supply voltage for the GTX transmitter and receiver termination circuits relative to GND	1.17	1.2	1.23	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTX transceiver column	1.17	1.2	1.23	V
MGTVCCAUX	Auxiliary analog Quad PLL (QPLL) voltage supply for the transceivers	1.75	1.80	1.85	V

Notes:

- Each voltage listed requires the filter circuit described in [UG476: 7 Series FPGAs Transceiver User Guide](#).
- Voltages are specified for the temperature range of $T_j = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$.

GTX Transceiver DC Input and Output Levels

Table 15 summarizes the DC output specifications of the GTX transceivers in Kintex-7 FPGAs. Consult [UG476: 7 Series FPGAs Transceiver User Guide](#) for further details.

Table 15: GTX Transceiver DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPIN}	Differential peak-to-peak input voltage	External AC coupled		–	2000	mV
V_{IN}	Absolute input voltage	DC coupled MGTAVTT = 1.2V	–200	–	MGTAVTT	mV
V_{CMIN}	Common mode input voltage	DC coupled MGTAVTT = 1.2V	–	2/3 MGTAVTT	–	mV
DV_{PPOUT}	Differential peak-to-peak output voltage ⁽¹⁾	Transmitter output swing is set to maximum setting	–	–	1000	mV
$V_{CMOUTDC}$	DC common mode output voltage.	Equation based	$MGTAVTT - DV_{PPOUT}/4$			mV
I_{DCIN}	DC input current for receiver input pins	DC coupled MGTAVTT = 1.2V	–	–	14	mA
I_{DCOUT}	DC output current for transmitter pins	DC coupled MGTAVTT = 1.2V	–	–	14	mA
R_{IN}	Differential input resistance			100		Ω
R_{OUT}	Differential output resistance			100		Ω
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	2	12	ps
C_{EXT}	Recommended external AC coupling capacitor ⁽²⁾		–	100	–	nF

Notes:

- The output swing and preemphasis levels are programmable using the attributes discussed in [UG476: 7 Series FPGAs Transceiver User Guide](#) and can result in values lower than reported in this table.
- Other values can be used as appropriate to conform to specific protocols and standards.

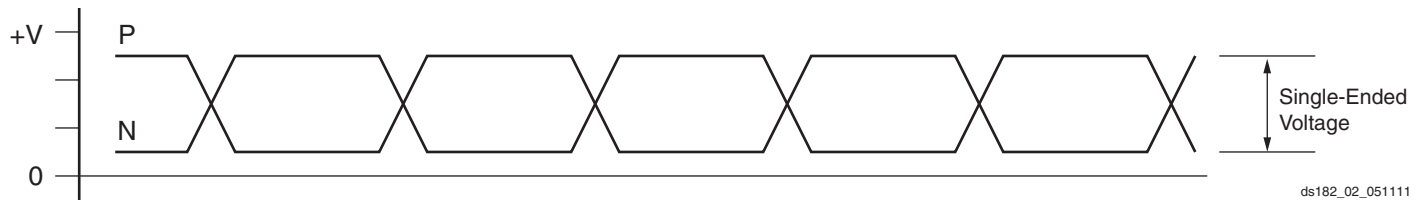


Figure 1: Single-Ended Peak-to-Peak Voltage

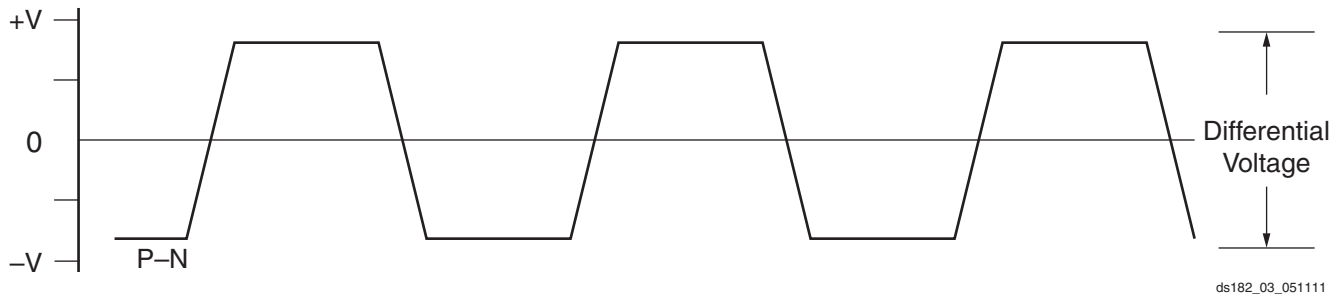


Figure 2: Differential Peak-to-Peak Voltage

Table 16 summarizes the DC specifications of the clock input of the GTX transceiver. Consult [UG476: 7 Series FPGAs Transceiver User Guide](#) for further details.

Table 16: GTX Transceiver Clock DC Input Level Specification

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	250		2000	mV
R_{IN}	Differential input resistance		100		Ω
C_{EXT}	Required external AC coupling capacitor	–	100	–	nF

GTX Transceiver Switching Characteristics

Consult [UG476: 7 Series FPGAs Transceiver User Guide](#) for further information.

Table 17: GTX Transceiver Performance

Symbol	Description	Output Divider	Speed Grade								Units
			1.0V				0.9V				
			-3		-2/-2L		-1		-2L ⁽¹⁾		
			Package Type								
			FF	FB	FF	FB	FF	FB	FF	FB	
F _{GTXMAX} ⁽²⁾	Maximum GTX transceiver data rate		12.5	6.6	10.3125	6.6	6.6	6.6	6.6	6.6	Gb/s
F _{GTXMIN} ⁽²⁾	Minimum GTX transceiver data rate		0.500	0.500	0.500	0.500	0.500	0.500	0.500	0.500	Gb/s
F _{GTXCRANGE}	CPLL line rate range	1	3.2–6.6								Gb/s
		2	1.6–3.3								Gb/s
		4	0.8–1.65								Gb/s
		8	0.5–0.825								Gb/s
		16	N/A								Gb/s
F _{GTXQRANGE1}	QPLL line rate range 1	1	5.93–8.0	5.93–6.6	5.93–8.0	5.93–6.6	5.93–6.6		5.93–6.6		Gb/s
		2	2.965–4.0		2.965–4.0		2.965–3.3		2.965–3.3		Gb/s
		4	1.4825–2.0		1.4825–2.0		1.4825–1.65		1.4825–1.65		Gb/s
		8	0.74125–1.0		0.74125–1.0		0.74125–0.825		0.74125–0.825		Gb/s
		16	N/A		N/A		N/A		N/A		Gb/s
F _{GTXQRANGE2}	QPLL line rate range 2 ⁽³⁾	1	9.8–12.5	N/A	9.8–10.3125	N/A	N/A		N/A		Gb/s
		2	4.9–6.25		4.9–5.15625		N/A		N/A		Gb/s
		4	2.45–3.125		2.45–2.578125		N/A		N/A		Gb/s
		8	1.225–1.5625		1.225–1.2890625		N/A		N/A		Gb/s
		16	0.6125–0.78125		0.6125–0.64453125		N/A		N/A		Gb/s
F _{GCPLL} RANGE	GTX transceiver CPLL frequency range		1.6–3.3		1.6–3.3		1.6–3.3		1.6–3.3		GHz
F _{GCPLL} RANGE1	GTX transceiver QPLL frequency range 1		5.93–8.0		5.93–8.0		5.93–6.6		5.93–6.6		GHz
F _{GCPLL} RANGE2	GTX transceiver QPLL frequency range 2		9.8–12.5		9.8–10.3125		N/A		N/A		GHz

Notes:

1. The -2L speed grade requires a 4-byte internal data width for operation above 5.0 Gb/s.
2. Data rates between 8.0 Gb/s and 9.8 Gb/s are not available.
3. For QPLL line rate range 2, the maximum line rate with the divider N set to 66 is 10.3125Gb/s.

Table 18: GTX Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V		0.9V		
		-3	-2/-2L	-1	-2L	
F _{GTXDRPCLK}	GTXDRPCLK maximum frequency	150	150	125	125	MHz

Table 19: GTX Transceiver Reference Clock Switching Characteristics

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F _{GCLK}	Reference clock frequency range	-3 speed grade	60	–	700	MHz
		All other speed grades	60	–	670	MHz
T _{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T _{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T _{DCREF}	Reference clock duty cycle	Transceiver PLL only	40	50	60	%
T _{LOCK}	Clock recovery frequency acquisition time	Initial PLL lock	–	–	–	ms
T _{DLOCK}	Clock recovery phase acquisition and adaptation time	After the PLL is locked to the reference clock, this is the time it takes to lock the data to the data present at the input.	–	–	–	UI

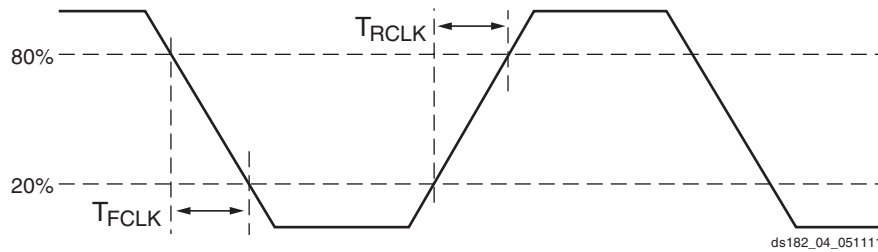


Figure 3: Reference Clock Timing Parameters

Table 20: GTX Transceiver User Clock Switching Characteristics⁽¹⁾⁽²⁾

Symbol	Description	Conditions	Speed Grade ⁽³⁾⁽⁴⁾				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
F _{TXOUT}	TXOUTCLK maximum frequency		412.5	412.5	312.5	312.5	MHz
F _{RXOUT}	RXOUTCLKT maximum frequency		412.5	412.5	312.5	312.5	MHz
F _{TXIN}	TXUSRCLK maximum frequency	16-bit data path	412.5	412.5	312.5	312.5	MHz
		32-bit data path	391	323	206.25	206.25	MHz
F _{RXIN}	RXUSRCLK maximum frequency	16-bit data path	412.5	412.5	312.5	312.5	MHz
		32-bit data path	391	323	206.25	206.25	MHz
F _{TXIN2}	TXUSRCLK2 maximum frequency	16-bit data path	412.5	412.5	312.5	312.5	MHz
		32-bit data path	391	323	206.25	206.25	MHz
		64-bit data path	196	162	103.125	103.125	MHz
F _{RXIN2}	RXUSRCLK2 maximum frequency	16-bit data path	412.5	412.5	312.5	312.5	MHz
		32-bit data path	391	323	206.25	206.25	MHz
		64-bit data path	196	162	103.125	103.125	MHz

Notes:

1. Clocking must be implemented as described in [UG476: 7 Series FPGAs Transceiver User Guide](#).
2. These frequencies are not supported for all possible transceiver configurations.
3. For speed grades -3, -2, -2L (1.0V), a 16-bit data path can only be used for speeds less than 6.6 Gb/s.
4. For speed grades -1 and -2L (0.9V), a 16-bit data path can only be used for speeds less than 5.0 Gb/s.

Table 21: GTX Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F _{GTXTX}	Serial data rate range		0.500	–	F _{GTXMAX}	Gb/s
T _{RTX}	TX Rise time	20%–80%	–	40	–	ps
T _{FTX}	TX Fall time	80%–20%	–	40	–	ps
T _{LLSKEW}	TX lane-to-lane skew ⁽¹⁾		–	–	500	ps
V _{TXOOBVDPP}	Electrical idle amplitude		–	–	15	mV
T _{TXOOBTRANSITION}	Electrical idle transition time		–	–	75	ns
T _{J12.5}	Total Jitter ⁽²⁾⁽⁴⁾	12.5 Gb/s	–	–	0.28	UI
D _{J12.5}	Deterministic Jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J11.18}	Total Jitter ⁽²⁾⁽⁴⁾	11.18 Gb/s	–	–	0.28	UI
D _{J11.18}	Deterministic Jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J10.3125}	Total Jitter ⁽²⁾⁽⁴⁾	10.3125 Gb/s	–	–	0.28	UI
D _{J10.3125}	Deterministic Jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J9.953}	Total Jitter ⁽²⁾⁽⁴⁾	9.953 Gb/s	–	–	0.28	UI
D _{J9.953}	Deterministic Jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J9.8}	Total Jitter ⁽²⁾⁽⁴⁾	9.8 Gb/s	–	–	0.28	UI
D _{J9.8}	Deterministic Jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J8.0}	Total Jitter ⁽²⁾⁽⁴⁾	8.0 Gb/s	–	–	0.33	UI
D _{J8.0}	Deterministic Jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J6.5}	Total Jitter ⁽³⁾⁽⁴⁾	6.5 Gb/s	–	–	0.33	UI
D _{J6.5}	Deterministic Jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J5.0}	Total Jitter ⁽³⁾⁽⁴⁾	5.0 Gb/s	–	–	0.33	UI
D _{J5.0}	Deterministic Jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
T _{J4.25}	Total Jitter ⁽³⁾⁽⁴⁾	4.25 Gb/s	–	–	0.33	UI
D _{J4.25}	Deterministic Jitter ⁽³⁾⁽⁴⁾		–	–	0.14	UI
T _{J3.75}	Total Jitter ⁽³⁾⁽⁴⁾	3.75 Gb/s	–	–	0.34	UI
D _{J3.75}	Deterministic Jitter ⁽³⁾⁽⁴⁾		–	–	0.16	UI
T _{J3.2}	Total Jitter ⁽³⁾⁽⁴⁾	3.20 Gb/s	–	–	0.2	UI
D _{J3.2}	Deterministic Jitter ⁽³⁾⁽⁴⁾		–	–	0.1	UI
T _{J3.2L}	Total Jitter ⁽³⁾⁽⁴⁾	3.20 Gb/s ⁽⁵⁾	–	–	0.35	UI
D _{J3.2L}	Deterministic Jitter ⁽³⁾⁽⁴⁾		–	–	0.16	UI
T _{J2.5}	Total Jitter ⁽³⁾⁽⁴⁾	2.5 Gb/s ⁽⁶⁾	–	–	0.20	UI
D _{J2.5}	Deterministic Jitter ⁽³⁾⁽⁴⁾		–	–	0.08	UI
T _{J1.25}	Total Jitter ⁽³⁾⁽⁴⁾	1.25 Gb/s ⁽⁷⁾	–	–	0.15	UI
D _{J1.25}	Deterministic Jitter ⁽³⁾⁽⁴⁾		–	–	0.06	UI
T _{J500}	Total Jitter ⁽³⁾⁽⁴⁾	500 Mb/s	–	–	0.1	UI
D _{J500}	Deterministic Jitter ⁽³⁾⁽⁴⁾		–	–	0.03	UI

Notes:

- Using same REFCLK input with TX phase alignment enabled for up to 12 consecutive transmitters (three fully populated GTX Quads).
- Using QPLL_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- Using CPLL_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- All jitter values are based on a bit-error ratio of 1e⁻¹².
- PLL frequency at 1.6 GHz and TXOUTDIV = 1.
- PLL frequency at 2.5 GHz and TXOUTDIV = 2.
- PLL frequency at 2.5 GHz and TXOUTDIV = 4.

Table 22: GTX Transceiver Receiver Switching Characteristics

Symbol	Description		Min	Typ	Max	Units
F _{GTXRX}	Serial data rate	RX oversampler not enabled	0.500	–	F _{GTXMAX}	Gb/s
T _{RXELECIDLE}	Time for RXELECIDLE to respond to loss or restoration of data		–	75	–	ns
RX _{OOBVDPP}	OOB detect threshold peak-to-peak		60	–	150	mV
RX _{SST}	Receiver spread-spectrum tracking ⁽¹⁾	Modulated @ 33 KHz	–5000	–	0	ppm
RX _{RL}	Run length (CID)	Internal AC capacitor bypassed	–	–	512	UI
RX _{PPMTOL}	Data/REFCLK PPM offset tolerance	Bit rates ≤ 6.6 Gb/s	–1250	–	1250	ppm
		Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s	–700	–	700	ppm
		Bit rates > 8.0 Gb/s	–200	–	200	ppm
SJ Jitter Tolerance⁽²⁾						
JT_SJ _{12.5}	Sinusoidal Jitter ⁽³⁾	12.5 Gb/s	0.3	–	–	UI
JT_SJ _{11.18}	Sinusoidal Jitter ⁽³⁾	11.18 Gb/s	0.3	–	–	UI
JT_SJ _{10.32}	Sinusoidal Jitter ⁽³⁾	10.32 Gb/s	0.3	–	–	UI
JT_SJ _{9.95}	Sinusoidal Jitter ⁽³⁾	9.95 Gb/s	0.3	–	–	UI
JT_SJ _{9.8}	Sinusoidal Jitter ⁽³⁾	9.8 Gb/s	0.3	–	–	UI
JT_SJ _{8.0}	Sinusoidal Jitter ⁽³⁾	8.0 Gb/s	0.44	–	–	UI
JT_SJ _{6.5}	Sinusoidal Jitter ⁽³⁾	6.5 Gb/s	0.44	–	–	UI
JT_SJ _{5.0}	Sinusoidal Jitter ⁽³⁾	5.0 Gb/s	0.44	–	–	UI
JT_SJ _{4.25}	Sinusoidal Jitter ⁽³⁾	4.25 Gb/s	0.44	–	–	UI
JT_SJ _{3.75}	Sinusoidal Jitter ⁽³⁾	3.75 Gb/s	0.44	–	–	UI
JT_SJ _{3.2}	Sinusoidal Jitter ⁽³⁾	3.2 Gb/s	0.45	–	–	UI
JT_SJ _{3.2L}	Sinusoidal Jitter ⁽³⁾	3.2 Gb/s ⁽⁴⁾	0.45	–	–	UI
JT_SJ _{2.5}	Sinusoidal Jitter ⁽³⁾	2.5 Gb/s ⁽⁵⁾	0.5	–	–	UI
JT_SJ _{1.25}	Sinusoidal Jitter ⁽³⁾	1.25 Gb/s ⁽⁶⁾	0.5	–	–	UI
JT_SJ ₅₀₀	Sinusoidal Jitter ⁽³⁾	500 Mb/s	0.4	–	–	UI
SJ Jitter Tolerance with Stressed Eye⁽²⁾						
JT_TJSE _{3.2}	Total Jitter with Stressed Eye ⁽⁷⁾	3.2 Gb/s	0.70	–	–	UI
		6.6 Gb/s	0.70	–	–	UI
JT_SJSE _{3.2}	Sinusoidal Jitter with Stressed Eye ⁽⁷⁾	3.2 Gb/s	0.1	–	–	UI
		6.6 Gb/s	0.1	–	–	UI

Notes:

- Using RXOUTDIV = 1, 2, and 4.
- All jitter values are based on a bit error ratio of 1e⁻¹².
- The frequency of the injected sinusoidal jitter is 80 MHz.
- PLL frequency at 1.6 GHz and RXOUTDIV = 1.
- PLL frequency at 2.5 GHz and RXOUTDIV = 2.
- PLL frequency at 2.5 GHz and RXOUTDIV = 4.
- Composite jitter with RX equalizer enabled. DFE disabled.

GTX Transceiver Protocol Jitter Parameters

Table 23: Gigabit Ethernet Protocol Parameters

Description	Line Rate (Mb/s)	Min	Max	Units
Gigabit Ethernet Transmitter Jitter Generation				
Total transmitter jitter (T_TJ)	1250	–	0.24	UI
Gigabit Ethernet Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	1250	0.71	–	UI

Table 24: XAUI Protocol Parameters

Description	Line Rate (Mb/s)	Min	Max	Units
XAUI Transmitter Jitter Generation				
Total transmitter jitter (T_TJ)	3125	–	0.35	UI
XAUI Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	3125	0.65	–	UI

Table 25: PCI Express Protocol Parameters

Standard	Description	Line Rate (Mb/s)	Min	Max	Units	
PCI Express Transmitter Jitter Generation						
PCI Express Gen 1	Total transmitter jitter	2500	–	0.25	UI	
PCI Express Gen 2	Total transmitter jitter	5000	–	0.25	UI	
PCI Express Gen 3	Total transmitter jitter uncorrelated	8000	–	31.25	ps	
	Deterministic transmitter jitter uncorrelated		–	12	ps	
PCI Express Receiver High Frequency Jitter Tolerance						
PCI Express Gen 1	Total receiver jitter tolerance ⁽¹⁾	2500	0.65	–	UI	
PCI Express Gen 2	Receiver inherent timing error	Common REFCLK	5000	0.40	–	UI
		Data clocked		0.34	–	UI
	Receiver inherent deterministic timing error	Common REFCLK		0.30	–	UI
		Data clocked		0.24	–	UI
PCI Express Gen 3	Receiver sinusoidal jitter tolerance	0.03 MHz–1.0 MHz	8000	1.00	–	UI
		1.0 MHz–10 MHz		Note 2	–	UI
		10 MHz–100 MHz		0.10	–	UI

Notes:

1. Sinusoidal jitter tolerance in the presence of ~3 ps RMS R_J measured at the pattern generator.
2. Between 1 MHz and 10 MHz the minimum sinusoidal jitter roll-off with a slope of 20DB/decade.

Table 26: CEI-6G and CEI-11G Protocol Parameters

Description	Line Rate (Mb/s)	Interface	Min	Max	Units
CEI-6G Transmitter Jitter Generation					
Total transmitter jitter	4976–6375	CEI-6G-SR	–	0.3	UI
		CEI-6G-LR	–	0.3	UI
CEI-6G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance	4976–6375	CEI-6G-SR	0.6	–	UI
		CEI-6G-LR	0.825	–	UI
CEI-11G Transmitter Jitter Generation					
Total transmitter jitter	9950–11200	CEI-11G-SR	–	0.3	UI
		CEI-11G-LR/MR	–	0.3	UI
CEI-11G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance	9950–11200	CEI-11G-SR	0.7	–	UI
		CEI-11G-MR	0.7	–	UI
		CEI-11G-LR	0.7	–	UI

Table 27: SFP+ Protocol Parameters

Description	Line Rate (Mb/s)	Min	Max	Units
SFP+ Transmitter Jitter Generation				
Total transmitter jitter	9953.00	–	0.28	UI
	10312.50			
	10518.75			
	11100.00			
SFP+ Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	9953.00	0.7	–	UI
	10312.50			
	10518.75			
	11100.00			

Table 28: CPRI Protocol Parameters

Description	Electrical Variant	Line Rate (Mb/s)	Min	Max	Units
CPRI Transmitter Jitter Generation					
Total transmitter jitter	LV	614.4	-	0.279	UI
		1228.8			
		2457.6			
		3072.0			
	LV-II	614.4			
		1228.8			
		2457.6			
		3072.0			
		4915.2			
		6144.0			
Deterministic jitter (T_DJ)	LV-III	All line rates	-	0.15	UI
Random jitter (T_RJ) at 10 ¹² BER	LV-III	All line rates	-	0.15	UI
CPRI Receiver Frequency Jitter Tolerance					
Total receiver jitter tolerance	LV	614.4	0.65	-	UI
		1228.8			
		2457.6			
		3072.0			
	LV-II	614.4	0.60	-	UI
		1228.8			
		2457.6			
		3072.0			
		4915.2			
		6144.0			
	LV-III	614.4	0.7	-	UI
		1228.8			
		2457.6			
		3072.0			
		4915.2			
		6144.0			
		9830.4			

Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:
<http://www.xilinx.com/technology/protocols/pciexpress.htm>

Table 29: Maximum Performance for PCI Express Designs

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
F _{PIPECLK}	Pipe clock maximum frequency	250	250	250	250	MHz
F _{USERCLK}	User clock maximum frequency	500	500	250	250	MHz
F _{USERCLK2}	User clock 2 maximum frequency	250	250	250	250	MHz
F _{DRPCLK}	DRP clock maximum frequency	250	250	250	250	MHz

XADC Specifications

Table 30: XADC Specifications

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
V _{CCADC} = 1.8V ± 5%, V _{REFP} = 1.25V, V _{REFN} = 0V, ADCCLK = 26 MHz, T _j = -40°C to 100°C, Typical values at T _j = +40°C						
ADC Accuracy⁽¹⁾						
Resolution			12	–	–	Bits
Integral Nonlinearity	INL		–	–	±2	LSBs
Differential Nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	LSBs
Offset Error		Calibrated	–	–	±4	LSBs
Gain Error		Calibrated	–	–	±0.4	%
Channel Matching		Based on two individual ADC instances with calibration enabled	–	–	10	LSBs
Sample Rate			0.1	–	1	MS/s
Signal to Noise Ratio	SNR	F _{SAMPLE} = 500KS/s, F _{IN} = 20KHz	60	–	–	dB
RMS Code Noise		External 1.25V reference	–	–	2	LSBs
		On-chip reference	–	3	–	LSBs
Total Harmonic Distortion	THD	F _{SAMPLE} = 500KS/s, F _{IN} = 20KHz	75	–	–	dB
ADC Accuracy at Extended Temperatures (-55°C to 125°C)						
Resolution			10	–	–	Bits
Integral Nonlinearity	INL		–	–	±1	LSB (at 10 bits)
Differential Nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	
Analog Inputs⁽²⁾						
ADC Input Ranges		Unipolar operation	0	–	1	V
		Bipolar operation	-0.5	–	+0.5	V
		Unipolar common mode range (FS input)	0	–	+0.5	V
		Bipolar common mode range (FS input)	+0.5	–	+0.6	V
Maximum External Channel Input Ranges		Adjacent channels set within these ranges should not corrupt measurements on adjacent channels	-0.1	–	V _{CCADC}	V
Auxiliary Channel Full Resolution Bandwidth	FRBW		250	–	–	KHz

Table 30: XADC Specifications (Cont'd)

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
On-Chip Sensors						
Temperature Sensor Error		$T_j = -40^{\circ}\text{C}$ to 100°C .	–	–	± 4	$^{\circ}\text{C}$
		$T_j = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	–	–	± 6	$^{\circ}\text{C}$
Supply Sensor Error		Measurement range of $V_{\text{CCAUX}} 1.8\text{V} \pm 5\%$ $T_j = -40^{\circ}\text{C}$ to $+100^{\circ}\text{C}$	–	–	± 1	%
		Measurement range of $V_{\text{CCAUX}} 1.8\text{V} \pm 5\%$ $T_j = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	–	–	± 2	%
Conversion Rate⁽³⁾						
Conversion Time - Continuous	t_{CONV}	Number of ADCCLK cycles	26	–	32	
Conversion Time - Event	t_{CONV}	Number of CLK cycles	–	–	21	
DRP Clock Frequency	DCLK	DRP clock frequency	8	–	250	MHz
ADC Clock Frequency	ADCCLK	Derived from DCLK	1	–	26	MHz
DCLK Duty Cycle			40	–	60	%
XADC Reference⁽⁴⁾						
External Reference	V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
On-Chip Reference		Ground V_{REFP} pin to AGND, $T_j = -40^{\circ}\text{C}$ to 100°C	1.2375	1.25	1.2625	V
Power Requirements						
Analog Power Supply	V_{CCADC}		1.71	1.8	1.89	V
Analog Supply Current	I_{CCADC}	Analog circuits in powered up state	–	–	25	mA

Notes:

- Offset and gain errors are removed by enabling the XADC automatic gain calibration feature. All values provided are with this feature enabled.
- See the ADC chapter in [UG480: 7 Series FPGAs XADC User Guide](#) for a detailed description.
- See the Timing chapter in [UG480: 7 Series FPGAs XADC User Guide](#) for a detailed description.
- Any variation in the reference voltage from the nominal $V_{\text{REFP}} = 1.25\text{V}$ and $V_{\text{REFN}} = 0\text{V}$ will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by $\pm 4\%$ is permitted. On-chip reference variation is $\pm 1\%$.

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Kintex-7 devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the [Switching Characteristics, page 25](#). In each table, the I/O bank type is either High Performance (HP) or High Range (HR).

Table 31: Networking Applications Interface Performances

Description	I/O Bank Type	Speed Grade				Units		
		1.0V		0.9V				
		-3	-2/-2L	-1	-2L			
SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8)	HR	710	710	625		Mb/s		
	HP	710	710	625		Mb/s		
DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 14)	HR	1250 ⁽²⁾	1152 ⁽³⁾	1250 ⁽²⁾	1152 ⁽³⁾	950 ⁽²⁾	800 ⁽³⁾	Mb/s
	HP	1600	1400	1250				Mb/s
SDR LVDS receiver (SFI-4.1) ⁽¹⁾	HR	710	710	625				Mb/s
	HP	710	710	625				Mb/s
DDR LVDS receiver (SPI-4.2) ⁽¹⁾	HR	1250	1250	950				Mb/s
	HP	1600	1400	1250				Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) algorithms dominate deterministic performance.
2. Some DDR LVDS transmitter frequencies are bounded by the performance of the TX interface to provide a clock with 5% DCD. The values in this column show the maximum rate that the LVDS can drive a clock at 5% DCD.
3. Some DDR LVDS transmitter frequencies are bounded by the performance of the TX interface to provide a clock with 10% DCD. The values in this column show the maximum rate that the LVDS can drive a clock at 10% DCD.

Table 32: Maximum Physical Interface (PHY) Rate for Memory Interfaces (FFG Packages)⁽¹⁾

Memory Standard	I/O Bank Type	V _{CCAUX_IO}	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
DDR3	HP	2.0V	1866		1600		Mb/s
	HP	1.8V	1600	1333	1066		Mb/s
	HR	N/A	1066	1066	800		Mb/s
DDR3L	HP	2.0V			1333		Mb/s
	HP	1.8V	1333	1066	800		Mb/s
	HR	N/A	800	800	667		Mb/s
DDR2	HP	2.0V	800	800	800		Mb/s
	HP	1.8V					
	HR	N/A					
QDR II+	HP	2.0V	550	500	450		MHz
	HP	1.8V					
	HR	N/A					
RLDRAM II	HP	2.0V	533	500	450		MHz
	HP	1.8V					
	HR	N/A					
RLDRAM III	HP	2.0V					MHz
	HP	1.8V					MHz
	HR	N/A					N/A
LPDDR2	HP	2.0V					Mb/s
	HP	1.8V					Mb/s
	HR	N/A					Mb/s

Notes:

1. Advance performance numbers pending characterization on Xilinx memory platforms designed according to the guidelines in the *7 Series FPGAs Memory Interface Solutions User Guide*.

Table 33: Maximum Physical Interface (PHY) Rate for Memory Interfaces (FBG Packages)⁽¹⁾

Memory Standard	I/O Bank Type	V _{CCAUX_IO} ⁽²⁾	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
DDR3	HP	N/A	1333	1066	800		Mb/s
	HR	N/A	1066	800	800		Mb/s
DDR3L	HP	N/A	1066	800	667		Mb/s
	HR	N/A	800	800	667		Mb/s
DDR2	HP	N/A	800	800	800		Mb/s
	HR	N/A	800	667	667		Mb/s
QDR II+	HP	N/A	550	500	450		MHz
	HR	N/A	450	400	350		MHz
RLDRAM II	HP	N/A	533	500	450		MHz
	HR	N/A					
RLDRAM III	HP	N/A					MHz
	HR	N/A					
LPDDR2	HP	N/A					Mb/s
	HR	N/A					Mb/s

Notes:

1. Advance performance numbers pending characterization on Xilinx memory platforms designed according to the guidelines in the *7 Series FPGAs Memory Interface Solutions User Guide*.
2. FBG packages do not have separate V_{CCAUX_IO} supply pins to adjust the pre-driver voltage of the HP I/O banks.

Switching Characteristics

All values represented in this data sheet are based on the advance speed specifications in ISE® software 13.4 v1.03 for the -3, -2, -2L (1.0V), -1, and -2L (0.9V) speed grades.

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device.

Table 34 correlates the current status of each Kintex-7 device on a per speed grade basis.

Table 34: Kintex-7 Device Speed Grade Designations

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC7K70T	-3, -2, -2L (1.0V), -1, -2L (0.9V)		
XC7K160T	-3, -2, -2L (1.0V), -1, -2L (0.9V)		
XC7K325T	-3, -2, -2L (1.0V), -1, -2L (0.9V)		
XC7K355T	-3, -2, -2L (1.0V), -1, -2L (0.9V)		
XC7K410T	-3, -2, -2L (1.0V), -1, -2L (0.9V)		
XC7K420T	-3, -2, -2L (1.0V), -1, -2L (0.9V)		
XC7K480T	-3, -2, -2L (1.0V), -1, -2L (0.9V)		

Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Kintex-7 devices.

Production Silicon and ISE Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

Table 35 lists the production released Kintex-7 device, speed grade, and the minimum corresponding supported speed specification version and ISE software revisions. The ISE software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 35: Kintex-7 Device Production Software and Speed Specification Release

Device	Speed Grade Designations			
	1.0V			0.9V
	-3	-2/-2L	-1	-2L
XC7K70T				
XC7K160T				
XC7K325T				
XC7K355T				
XC7K410T				
XC7K420T				
XC7K480T				

Notes:

- Blank entries indicate a device and/or speed grade in advance or preliminary status.

IOB Pad Input/Output/3-State Switching Characteristics

Table 36 (3.3V high-range IOB (HR)) and Table 37 (1.8V high-performance IOB (HP)) summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

T_{IOPi} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.

T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.

T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer.

Table 38 summarizes the value of T_{IOTPHZ} . T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state).

Table 36: 3.3V IOB High Range (HR) Switching Characteristics

I/O Standard	T_{IOPi}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V		0.9V		1.0V		0.9V		1.0V		0.9V		
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
LVTTTL_S4	1.28	1.38	1.52	1.65	5.39	5.93	6.56	5.80	5.39	5.93	6.56	5.80	ns
LVTTTL_S8	1.28	1.38	1.52	1.65	4.57	5.13	5.80	5.06	4.57	5.13	5.80	5.06	ns
LVTTTL_S12	1.28	1.38	1.52	1.65	4.57	5.13	5.80	5.06	4.57	5.13	5.80	5.06	ns
LVTTTL_S16	1.28	1.38	1.52	1.65	3.59	4.18	4.91	4.13	3.59	4.18	4.91	4.13	ns
LVTTTL_S24	1.28	1.38	1.52	1.65	3.69	4.29	5.02	4.22	3.69	4.29	5.02	4.22	ns
LVTTTL_F4	1.28	1.38	1.52	1.65	4.82	5.28	5.80	5.16	4.82	5.28	5.80	5.16	ns
LVTTTL_F8	1.28	1.38	1.52	1.65	3.78	4.36	5.07	4.27	3.78	4.36	5.07	4.27	ns
LVTTTL_F12	1.28	1.38	1.52	1.65	3.78	4.36	5.07	4.25	3.78	4.36	5.07	4.25	ns
LVTTTL_F16	1.28	1.38	1.52	1.65	2.69	3.15	3.66	3.04	2.69	3.15	3.66	3.04	ns
LVTTTL_F24	1.28	1.38	1.52	1.65	2.53	2.94	3.40	2.83	2.53	2.94	3.40	2.83	ns
LVDS_25 ⁽¹⁾	0.60	0.64	0.68	0.83	1.48	1.77	2.06	1.44	1.48	1.77	2.06	1.44	ns
MINI_LVDS_25	0.58	0.62	0.68	0.81	1.48	1.77	2.06	1.44	1.48	1.77	2.06	1.44	ns
BLVDS_25 ⁽¹⁾	0.62	0.65	0.68	0.84	1.95	2.32	2.71	2.02	1.95	2.32	2.71	2.02	ns
RSDS_25 (point to point) ⁽¹⁾	0.60	0.63	0.67	0.83	1.48	1.78	2.06	1.44	1.48	1.78	2.06	1.44	ns
PPDS_25 ⁽¹⁾	0.61	0.64	0.69	0.85	1.47	1.79	2.09	1.50	1.47	1.79	2.09	1.50	ns
TMDS_33 ⁽¹⁾	0.69	0.71	0.75	0.91	1.55	1.84	2.11	1.50	1.55	1.84	2.11	1.50	ns
PCI33_3 ⁽¹⁾	1.25	1.36	1.53	1.64	2.83	3.38	4.03	2.92	2.83	3.38	4.03	2.92	ns
HSUL_12	0.59	0.59	0.59	0.75	2.18	2.61	3.10	2.35	2.18	2.61	3.10	2.35	ns
DIFF_HSUL_12	0.55	0.56	0.58	0.75	1.95	2.34	2.77	2.05	1.95	2.34	2.77	2.05	ns
HSTL_I_S	0.58	0.59	0.61	0.77	1.67	1.99	2.31	1.68	1.67	1.99	2.31	1.68	ns
HSTL_II_S	0.58	0.59	0.61	0.77	1.28	1.61	1.96	1.24	1.28	1.61	1.96	1.24	ns
HSTL_I_18_S	0.61	0.62	0.64	0.79	1.40	1.69	1.95	1.42	1.40	1.69	1.95	1.42	ns
HSTL_II_18_S	0.61	0.62	0.64	0.79	1.29	1.61	1.92	1.24	1.29	1.61	1.92	1.24	ns
DIFF_HSTL_I_S	0.60	0.62	0.65	0.81	1.54	1.84	2.12	1.52	1.54	1.84	2.12	1.52	ns
DIFF_HSTL_II_S	0.60	0.62	0.65	0.81	1.27	1.54	1.78	1.21	1.27	1.54	1.78	1.21	ns
DIFF_HSTL_I_18_S	0.62	0.64	0.66	0.83	1.39	1.68	1.94	1.35	1.39	1.68	1.94	1.35	ns

Table 36: 3.3V IOB High Range (HR) Switching Characteristics (Cont'd)

I/O Standard	T _{IOP1}				T _{IOP0}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V		0.9V		1.0V		0.9V		1.0V		0.9V		
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
DIFF_HSTL_II_18_S	0.62	0.64	0.66	0.83	1.26	1.53	1.77	1.21	1.26	1.53	1.77	1.21	ns
HSTL_I_F	0.58	0.59	0.61	0.77	1.22	1.49	1.74	1.22	1.22	1.49	1.74	1.22	ns
HSTL_II_F	0.58	0.59	0.61	0.77	1.14	1.47	1.79	1.13	1.14	1.47	1.79	1.13	ns
HSTL_I_18_F	0.61	0.62	0.64	0.79	1.20	1.50	1.79	1.20	1.20	1.50	1.79	1.20	ns
HSTL_II_18_F	0.61	0.62	0.64	0.79	1.14	1.45	1.74	1.11	1.14	1.45	1.74	1.11	ns
DIFF_HSTL_I_F	0.60	0.62	0.65	0.81	1.20	1.48	1.73	1.15	1.20	1.48	1.73	1.15	ns
DIFF_HSTL_II_F	0.60	0.62	0.65	0.81	1.14	1.41	1.65	1.09	1.14	1.41	1.65	1.09	ns
DIFF_HSTL_I_18_F	0.62	0.64	0.66	0.83	1.20	1.47	1.72	1.14	1.20	1.47	1.72	1.14	ns
DIFF_HSTL_II_18_F	0.62	0.64	0.66	0.83	1.13	1.40	1.64	1.07	1.13	1.40	1.64	1.07	ns
LVC MOS33_S4	1.27	1.36	1.48	1.66	5.35	5.91	6.60	5.79	5.35	5.91	6.60	5.79	ns
LVC MOS33_S8	1.27	1.36	1.48	1.66	4.58	5.15	5.84	5.06	4.58	5.15	5.84	5.06	ns
LVC MOS33_S12	1.27	1.36	1.48	1.66	3.58	4.19	4.93	4.12	3.58	4.19	4.93	4.12	ns
LVC MOS33_S16	1.27	1.36	1.48	1.66	3.18	3.73	4.39	3.65	3.18	3.73	4.39	3.65	ns
LVC MOS33_F4	1.27	1.36	1.48	1.66	4.82	5.31	5.87	5.15	4.82	5.31	5.87	5.15	ns
LVC MOS33_F8	1.27	1.36	1.48	1.66	3.74	4.34	5.07	4.25	3.74	4.34	5.07	4.25	ns
LVC MOS33_F12	1.27	1.36	1.48	1.66	2.69	3.15	3.66	3.04	2.69	3.15	3.66	3.04	ns
LVC MOS33_F16	1.27	1.36	1.48	1.66	2.56	2.99	3.47	2.88	2.56	2.99	3.47	2.88	ns
LVC MOS25_S4	1.05	1.11	1.20	1.39	4.61	5.10	5.67	4.82	4.61	5.10	5.67	4.82	ns
LVC MOS25_S8	1.05	1.11	1.20	1.39	3.78	4.34	5.00	4.07	3.78	4.34	5.00	4.07	ns
LVC MOS25_S12	1.05	1.11	1.20	1.39	2.89	3.40	4.00	3.14	2.89	3.40	4.00	3.14	ns
LVC MOS25_S16	1.05	1.11	1.20	1.39	3.35	3.92	4.60	3.64	3.35	3.92	4.60	3.64	ns
LVC MOS25_F4	1.05	1.11	1.20	1.39	4.08	4.61	5.23	4.33	4.08	4.61	5.23	4.33	ns
LVC MOS25_F8	1.05	1.11	1.20	1.39	2.55	3.17	3.93	2.95	2.55	3.17	3.93	2.95	ns
LVC MOS25_F12	1.05	1.11	1.20	1.39	2.34	2.93	3.64	2.69	2.34	2.93	3.64	2.69	ns
LVC MOS25_F16	1.05	1.11	1.20	1.39	2.04	2.47	2.96	2.20	2.04	2.47	2.96	2.20	ns
LVC MOS18_S4	0.61	0.61	0.62	0.78	3.36	3.75	4.16	3.45	3.36	3.75	4.16	3.45	ns
LVC MOS18_S8	0.61	0.61	0.62	0.78	2.70	3.21	3.82	2.94	2.70	3.21	3.82	2.94	ns
LVC MOS18_S12	0.61	0.61	0.62	0.78	2.70	3.21	3.82	2.94	2.70	3.21	3.82	2.94	ns
LVC MOS18_S16	0.61	0.61	0.62	0.78	1.94	2.33	2.74	2.05	1.94	2.33	2.74	2.05	ns
LVC MOS18_S24 ⁽¹⁾	0.61	0.61	0.62	0.78	1.86	2.22	2.59	1.94	1.86	2.22	2.59	1.94	ns
LVC MOS18_F4	0.61	0.61	0.62	0.78	3.24	3.61	4.00	3.33	3.24	3.61	4.00	3.33	ns
LVC MOS18_F8	0.61	0.61	0.62	0.78	2.02	2.43	2.87	2.15	2.02	2.43	2.87	2.15	ns
LVC MOS18_F12	0.61	0.61	0.62	0.78	2.02	2.43	2.87	2.15	2.02	2.43	2.87	2.15	ns
LVC MOS18_F16	0.61	0.61	0.62	0.78	1.64	1.98	2.32	1.69	1.64	1.98	2.32	1.69	ns
LVC MOS18_F24 ⁽¹⁾	0.61	0.61	0.62	0.78	1.46	1.76	2.06	1.47	1.46	1.76	2.06	1.47	ns
LVC MOS15_S4	0.61	0.63	0.66	0.81	3.60	4.04	4.54	3.82	3.60	4.04	4.54	3.82	ns
LVC MOS15_S8	0.61	0.63	0.66	0.81	2.49	2.97	3.52	2.67	2.49	2.97	3.52	2.67	ns

Table 36: 3.3V IOB High Range (HR) Switching Characteristics (Cont'd)

I/O Standard	T _{IOP1}				T _{IOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V		0.9V		1.0V		0.9V		1.0V		0.9V		
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
LVC MOS15_S12	0.61	0.63	0.66	0.81	1.95	2.33	2.74	2.06	1.95	2.33	2.74	2.06	ns
LVC MOS15_S16	0.61	0.63	0.66	0.81	1.88	2.25	2.64	1.97	1.88	2.25	2.64	1.97	ns
LVC MOS15_F4	0.61	0.63	0.66	0.81	3.51	3.90	4.31	3.65	3.51	3.90	4.31	3.65	ns
LVC MOS15_F8	0.61	0.63	0.66	0.81	1.91	2.29	2.69	1.97	1.91	2.29	2.69	1.97	ns
LVC MOS15_F12	0.61	0.63	0.66	0.81	1.52	1.84	2.16	1.55	1.52	1.84	2.16	1.55	ns
LVC MOS15_F16	0.61	0.63	0.66	0.81	1.49	1.81	2.12	1.52	1.49	1.81	2.12	1.52	ns
LVC MOS12_S4	0.68	0.76	0.90	0.85	3.96	4.52	5.20	4.27	3.96	4.52	5.20	4.27	ns
LVC MOS12_S8	0.68	0.76	0.90	0.85	2.63	3.26	4.02	3.01	2.63	3.26	4.02	3.01	ns
LVC MOS12_S12 ⁽¹⁾	0.68	0.76	0.90	0.85	2.18	2.61	3.10	2.35	2.18	2.61	3.10	2.35	ns
LVC MOS12_F4	0.68	0.76	0.90	0.85	3.56	4.03	4.57	3.77	3.56	4.03	4.57	3.77	ns
LVC MOS12_F8	0.68	0.76	0.90	0.85	1.84	2.34	2.91	2.10	1.84	2.34	2.91	2.10	ns
LVC MOS12_F12 ⁽¹⁾	0.68	0.76	0.90	0.85	1.66	2.01	2.38	1.73	1.66	2.01	2.38	1.73	ns
SSTL135_S	0.56	0.58	0.61	0.73	1.33	1.68	2.02	1.28	1.33	1.68	2.02	1.28	ns
SSTL15_S	0.58	0.59	0.61	0.77	1.27	1.63	1.99	1.24	1.27	1.63	1.99	1.24	ns
SSTL18_I_S	0.61	0.62	0.64	0.79	1.71	2.04	2.36	1.71	1.71	2.04	2.36	1.71	ns
SSTL18_II_S	0.61	0.62	0.64	0.79	1.28	1.64	2.02	1.24	1.28	1.64	2.02	1.24	ns
DIFF_SSTL135_S	0.55	0.57	0.59	0.75	1.33	1.68	2.02	1.28	1.33	1.68	2.02	1.28	ns
DIFF_SSTL15_S	0.60	0.62	0.65	0.81	1.27	1.63	1.99	1.24	1.27	1.63	1.99	1.24	ns
DIFF_SSTL18_I_S	0.62	0.64	0.66	0.83	1.62	1.93	2.23	1.61	1.62	1.93	2.23	1.61	ns
DIFF_SSTL18_II_S	0.62	0.64	0.66	0.83	1.25	1.52	1.76	1.19	1.25	1.52	1.76	1.19	ns
SSTL135_F	0.56	0.58	0.61	0.73	1.17	1.48	1.77	1.12	1.17	1.48	1.77	1.12	ns
SSTL15_F	0.58	0.59	0.61	0.77	1.15	1.47	1.77	1.13	1.15	1.47	1.77	1.13	ns
SSTL18_I_F	0.61	0.62	0.64	0.79	1.24	1.52	1.77	1.22	1.24	1.52	1.77	1.22	ns
SSTL18_II_F	0.61	0.62	0.64	0.79	1.16	1.48	1.79	1.11	1.16	1.48	1.79	1.11	ns
DIFF_SSTL135_F	0.55	0.57	0.59	0.75	1.17	1.48	1.77	1.12	1.17	1.48	1.77	1.12	ns
DIFF_SSTL15_F	0.60	0.62	0.65	0.81	1.15	1.47	1.77	1.13	1.15	1.47	1.77	1.13	ns
DIFF_SSTL18_I_F	0.62	0.64	0.66	0.83	1.22	1.49	1.74	1.17	1.22	1.49	1.74	1.17	ns
DIFF_SSTL18_II_F	0.62	0.64	0.66	0.83	1.13	1.40	1.65	1.08	1.13	1.40	1.65	1.08	ns

Notes:

1. This I/O standard is only available in the 3.3V high-range (HR) banks.

Table 37: 1.8V IOB High Performance (HP) Switching Characteristics

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V		0.9V		1.0V		0.9V		1.0V		0.9V		
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
LVDS	0.81	0.80	0.91	1.11	1.03	1.38	1.73	1.68	1.63	2.03	2.51	1.68	ns
HSUL_12	0.76	0.73	0.82	1.05	1.79	2.13	2.53	1.72	2.39	2.79	3.31	1.72	ns
DIFF_HSUL_12	0.76	0.73	0.82	1.05	1.79	2.13	2.53	1.72	2.39	2.79	3.31	1.72	ns
HSTL_I_S	0.75	0.72	0.82	1.07	1.29	1.58	1.86	1.69	1.89	2.23	2.64	1.69	ns
HSTL_II_S	0.75	0.72	0.82	1.07	1.19	1.47	1.73	1.69	1.79	2.13	2.51	1.69	ns
HSTL_I_18_S	0.77	0.73	0.81	1.07	1.26	1.54	1.82	1.72	1.85	2.19	2.60	1.72	ns
HSTL_II_18_S	0.77	0.73	0.81	1.07	1.19	1.47	1.75	1.76	1.79	2.13	2.53	1.76	ns
HSTL_I_12_S	0.75	0.72	0.82	1.07	1.28	1.57	1.85	1.73	1.88	2.22	2.63	1.73	ns
HSTL_I_DCI_S	0.75	0.72	0.82	1.07	1.25	1.53	1.81	1.66	1.84	2.19	2.59	1.66	ns
HSTL_II_DCI_S	0.75	0.72	0.82	1.07	1.19	1.47	1.74	1.62	1.79	2.12	2.52	1.62	ns
HSTL_II_T_DCI_S	0.77	0.73	0.81	1.07	1.29	1.57	1.86	1.63	1.88	2.23	2.64	1.63	ns
HSTL_I_DCI_18_S	0.77	0.73	0.81	1.07	1.25	1.53	1.81	1.66	1.84	2.19	2.59	1.66	ns
HSTL_II_DCI_18_S	0.77	0.73	0.81	1.07	1.19	1.46	1.72	1.59	1.79	2.12	2.50	1.59	ns
HSTL_II_T_DCI_18_S	0.77	0.73	0.81	1.07	1.25	1.53	1.81	1.66	1.84	2.19	2.59	1.66	ns
DIFF_HSTL_I_S	0.81	0.80	0.91	1.11	1.29	1.58	1.86	1.69	1.89	2.23	2.64	1.69	ns
DIFF_HSTL_II_S	0.81	0.80	0.91	1.11	1.19	1.47	1.73	1.69	1.79	2.13	2.51	1.69	ns
DIFF_HSTL_I_DCI_S	0.81	0.80	0.91	1.11	1.29	1.57	1.86	1.63	1.88	2.23	2.64	1.63	ns
DIFF_HSTL_II_DCI_S	0.81	0.80	0.91	1.11	1.19	1.47	1.74	1.62	1.79	2.12	2.52	1.62	ns
DIFF_HSTL_I_18_S	0.81	0.80	0.91	1.11	1.26	1.54	1.82	1.72	1.85	2.19	2.60	1.72	ns
DIFF_HSTL_II_18_S	0.81	0.80	0.91	1.11	1.19	1.47	1.75	1.76	1.79	2.13	2.53	1.76	ns
DIFF_HSTL_I_DCI_18_S	0.81	0.80	0.91	1.11	1.25	1.53	1.81	1.66	1.84	2.19	2.59	1.66	ns
DIFF_HSTL_II_DCI_18_S	0.81	0.80	0.91	1.11	1.19	1.46	1.72	1.59	1.79	2.12	2.50	1.59	ns
DIFF_HSTL_II_T_DCI_18_S	0.81	0.80	0.91	1.11	1.25	1.53	1.81	1.66	1.84	2.19	2.59	1.66	ns
HSTL_I_F	0.75	0.72	0.82	1.07	1.16	1.44	1.70	1.69	1.76	2.09	2.48	1.69	ns
HSTL_II_F	0.75	0.72	0.82	1.07	1.11	1.38	1.63	1.69	1.71	2.04	2.41	1.69	ns
HSTL_I_18_F	0.77	0.73	0.81	1.07	1.18	1.45	1.72	1.72	1.78	2.11	2.50	1.72	ns
HSTL_II_18_F	0.77	0.73	0.81	1.07	1.12	1.39	1.64	1.76	1.72	2.05	2.42	1.76	ns
HSTL_I_12_F	0.75	0.72	0.82	1.07	1.16	1.43	1.68	1.73	1.75	2.08	2.46	1.73	ns
HSTL_I_DCI_F	0.75	0.72	0.82	1.07	1.18	1.45	1.72	1.66	1.77	2.11	2.50	1.66	ns
HSTL_II_DCI_F	0.75	0.72	0.82	1.07	1.11	1.38	1.63	1.62	1.71	2.04	2.41	1.62	ns
HSTL_II_T_DCI_F	0.77	0.73	0.81	1.07	1.16	1.44	1.70	1.63	1.76	2.10	2.48	1.63	ns
HSTL_I_DCI_18_F	0.77	0.73	0.81	1.07	1.18	1.45	1.72	1.66	1.77	2.11	2.50	1.66	ns
HSTL_II_DCI_18_F	0.77	0.73	0.81	1.07	1.12	1.39	1.64	1.59	1.71	2.04	2.42	1.59	ns
HSTL_II_T_DCI_18_F	0.77	0.73	0.81	1.07	1.18	1.45	1.72	1.66	1.77	2.11	2.50	1.66	ns
DIFF_HSTL_I_F	0.81	0.80	0.91	1.11	1.16	1.44	1.70	1.69	1.76	2.09	2.48	1.69	ns
DIFF_HSTL_II_F	0.81	0.80	0.91	1.11	1.11	1.38	1.63	1.69	1.71	2.04	2.41	1.69	ns
DIFF_HSTL_I_DCI_F	0.81	0.80	0.91	1.11	1.16	1.44	1.70	1.63	1.76	2.10	2.48	1.63	ns

Table 37: 1.8V IOB High Performance (HP) Switching Characteristics (Cont'd)

I/O Standard	T _{IOP1}				T _{IOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V		0.9V		1.0V		0.9V		1.0V		0.9V		
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
DIFF_HSTL_II_DCI_F	0.81	0.80	0.91	1.11	1.11	1.38	1.63	1.62	1.71	2.04	2.41	1.62	ns
DIFF_HSTL_I_18_F	0.81	0.80	0.91	1.11	1.18	1.45	1.72	1.72	1.78	2.11	2.50	1.72	ns
DIFF_HSTL_II_18_F	0.81	0.80	0.91	1.11	1.12	1.39	1.64	1.76	1.72	2.05	2.42	1.76	ns
DIFF_HSTL_I_DCI_18_F	0.81	0.80	0.91	1.11	1.18	1.45	1.72	1.66	1.77	2.11	2.50	1.66	ns
DIFF_HSTL_II_DCI_18_F	0.81	0.80	0.91	1.11	1.12	1.39	1.64	1.59	1.71	2.04	2.42	1.59	ns
DIFF_HSTL_II_T_DCI_18_F	0.81	0.80	0.91	1.11	1.18	1.45	1.72	1.66	1.77	2.11	2.50	1.66	ns
LVC MOS18_S2	0.57	0.58	0.59	0.72	4.09	4.58	5.33	4.86	4.69	5.24	6.11	4.86	ns
LVC MOS18_S4	0.57	0.58	0.59	0.72	2.81	3.27	3.91	3.21	3.41	3.93	4.69	3.21	ns
LVC MOS18_S6	0.57	0.58	0.59	0.72	2.28	2.68	3.20	2.64	2.87	3.34	3.98	2.64	ns
LVC MOS18_S8	0.57	0.58	0.59	0.72	2.12	2.51	3.00	2.30	2.71	3.16	3.78	2.30	ns
LVC MOS18_S12	0.57	0.58	0.59	0.72	1.84	2.21	2.65	2.16	2.44	2.87	3.43	2.16	ns
LVC MOS18_S16	0.57	0.58	0.59	0.72	1.71	2.05	2.45	2.11	2.30	2.71	3.23	2.11	ns
LVC MOS18_F2	0.57	0.58	0.59	0.72	3.64	4.17	4.96	4.59	4.24	4.83	5.74	4.59	ns
LVC MOS18_F4	0.57	0.58	0.59	0.72	2.37	2.79	3.35	3.00	2.97	3.45	4.13	3.00	ns
LVC MOS18_F6	0.57	0.58	0.59	0.72	1.94	2.30	2.73	2.47	2.53	2.96	3.51	2.47	ns
LVC MOS18_F8	0.57	0.58	0.59	0.72	1.60	2.02	2.52	2.16	2.20	2.67	3.30	2.16	ns
LVC MOS18_F12	0.57	0.58	0.59	0.72	1.40	1.70	2.01	1.96	1.99	2.35	2.79	1.96	ns
LVC MOS18_F16	0.57	0.58	0.59	0.72	1.33	1.62	1.92	1.89	1.93	2.28	2.70	1.89	ns
LVC MOS15_S2	0.60	0.60	0.72	0.85	3.69	4.19	4.93	4.10	4.29	4.85	5.71	4.10	ns
LVC MOS15_S4	0.60	0.60	0.72	0.85	2.59	3.00	3.54	3.03	3.18	3.65	4.32	3.03	ns
LVC MOS15_S6	0.60	0.60	0.72	0.85	2.38	2.81	3.36	2.52	2.98	3.46	4.14	2.52	ns
LVC MOS15_S8	0.60	0.60	0.72	0.85	2.05	2.46	2.96	2.15	2.65	3.11	3.74	2.15	ns
LVC MOS15_S12	0.60	0.60	0.72	0.85	1.91	2.27	2.71	2.07	2.51	2.93	3.49	2.07	ns
LVC MOS15_S16	0.60	0.60	0.72	0.85	1.76	2.10	2.50	1.99	2.36	2.76	3.28	1.99	ns
LVC MOS15_F2	0.60	0.60	0.72	0.85	3.52	3.98	4.66	4.10	4.12	4.64	5.44	4.10	ns
LVC MOS15_F4	0.60	0.60	0.72	0.85	2.18	2.51	2.91	2.75	2.78	3.17	3.69	2.75	ns
LVC MOS15_F6	0.60	0.60	0.72	0.85	1.61	2.04	2.56	2.22	2.20	2.69	3.35	2.22	ns
LVC MOS15_F8	0.60	0.60	0.72	0.85	1.45	1.76	2.08	2.06	2.05	2.42	2.87	2.06	ns
LVC MOS15_F12	0.60	0.60	0.72	0.85	1.35	1.64	1.93	1.92	1.94	2.29	2.71	1.92	ns
LVC MOS15_F16	0.60	0.60	0.72	0.85	1.32	1.61	1.89	1.91	1.92	2.26	2.67	1.91	ns
LVC MOS12_S2	0.65	0.65	0.77	0.95	3.52	4.10	4.95	3.68	4.12	4.75	5.73	3.68	ns
LVC MOS12_S4	0.65	0.65	0.77	0.95	2.76	3.24	3.90	2.85	3.36	3.89	4.69	2.85	ns
LVC MOS12_S6	0.65	0.65	0.77	0.95	2.19	2.63	3.19	2.29	2.79	3.28	3.97	2.29	ns
LVC MOS12_S8	0.65	0.65	0.77	0.95	2.08	2.48	2.98	2.19	2.68	3.14	3.76	2.19	ns
LVC MOS12_F2	0.65	0.65	0.77	0.95	2.98	3.44	4.10	3.24	3.58	4.10	4.88	3.24	ns
LVC MOS12_F4	0.65	0.65	0.77	0.95	2.11	2.48	2.92	2.35	2.71	3.13	3.70	2.35	ns
LVC MOS12_F6	0.65	0.65	0.77	0.95	1.47	1.81	2.18	2.06	2.06	2.46	2.96	2.06	ns

Table 37: 1.8V IOB High Performance (HP) Switching Characteristics (Cont'd)

I/O Standard	T _{IOP1}				T _{IOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V		0.9V		1.0V		0.9V		1.0V		0.9V		
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
LVC MOS12_F8	0.65	0.65	0.77	0.95	1.41	1.72	2.03	1.98	2.01	2.37	2.81	1.98	ns
LVDCI_18	0.57	0.58	0.59	0.72	2.13	2.45	2.83	2.42	2.72	3.10	3.61	2.42	ns
LVDCI_15	0.60	0.60	0.72	0.85	2.12	2.53	3.05	2.18	2.72	3.19	3.83	2.18	ns
LVDCI_DV2_18	0.57	0.58	0.59	0.72	2.13	2.45	2.82	1.97	2.72	3.10	3.60	1.97	ns
LVDCI_DV2_15	0.60	0.60	0.72	0.85	2.12	2.53	3.05	1.92	2.72	3.19	3.83	1.92	ns
HSLVDCI_18	0.75	0.72	0.82	1.07	2.13	2.45	2.83	2.42	2.72	3.10	3.61	2.42	ns
HSLVDCI_15	0.75	0.72	0.82	1.07	2.12	2.53	3.05	2.18	2.72	3.19	3.83	2.18	ns
SSTL18_I_S	0.75	0.72	0.82	1.07	1.16	1.45	1.72	1.72	1.76	2.10	2.50	1.72	ns
SSTL18_II_S	0.75	0.72	0.82	1.07	1.16	1.50	1.86	1.63	1.76	2.16	2.65	1.63	ns
SSTL18_I_DCI_S	0.75	0.72	0.82	1.07	1.06	1.36	1.65	1.64	1.66	2.01	2.43	1.64	ns
SSTL18_II_DCI_S	0.75	0.72	0.82	1.07	1.02	1.28	1.55	1.59	1.61	1.93	2.34	1.59	ns
SSTL18_II_T_DCI_S	0.75	0.72	0.82	1.07	1.06	1.36	1.65	1.64	1.66	2.01	2.43	1.64	ns
SSTL15_S	0.75	0.72	0.82	1.07	1.08	1.36	1.63	1.67	1.68	2.02	2.41	1.67	ns
SSTL15_DCI_S	0.75	0.72	0.82	1.07	1.08	1.36	1.63	1.65	1.67	2.02	2.41	1.65	ns
SSTL15_T_DCI_S	0.75	0.72	0.82	1.07	1.08	1.36	1.63	1.65	1.67	2.02	2.41	1.65	ns
SSTL135_S	0.75	0.72	0.82	1.07	1.11	1.39	1.67	1.67	1.70	2.05	2.45	1.67	ns
SSTL135_DCI_S	0.75	0.72	0.82	1.07	1.11	1.39	1.66	1.65	1.70	2.05	2.45	1.65	ns
SSTL135_T_DCI_S	0.75	0.72	0.82	1.07	1.11	1.39	1.66	1.65	1.70	2.05	2.45	1.65	ns
SSTL12_S	0.76	0.73	0.82	1.05	1.10	1.39	1.66	1.72	1.70	2.04	2.44	1.72	ns
SSTL12_DCI_S	0.76	0.73	0.82	1.05	1.17	1.47	1.75	1.72	1.76	2.12	2.53	1.72	ns
SSTL12_T_DCI_S	0.76	0.73	0.82	1.05	1.17	1.47	1.75	1.72	1.76	2.12	2.53	1.72	ns
DIFF_SSTL18_I_S	0.81	0.80	0.91	1.11	1.16	1.45	1.72	1.72	1.76	2.10	2.50	1.72	ns
DIFF_SSTL18_II_S	0.81	0.80	0.91	1.11	1.16	1.50	1.86	1.63	1.76	2.16	2.65	1.63	ns
DIFF_SSTL18_I_DCI_S	0.81	0.80	0.91	1.11	1.06	1.36	1.65	1.64	1.66	2.01	2.43	1.64	ns
DIFF_SSTL18_II_DCI_S	0.81	0.80	0.91	1.11	1.02	1.28	1.55	1.59	1.61	1.93	2.34	1.59	ns
DIFF_SSTL18_II_T_DCI_S	0.81	0.80	0.91	1.11	1.06	1.36	1.65	1.64	1.66	2.01	2.43	1.64	ns
DIFF_SSTL15_S	0.75	0.72	0.82	1.07	1.08	1.36	1.63	1.67	1.68	2.02	2.41	1.67	ns
DIFF_SSTL15_DCI_S	0.75	0.72	0.82	1.07	1.08	1.36	1.63	1.65	1.67	2.02	2.41	1.65	ns
DIFF_SSTL15_T_DCI_S	0.75	0.72	0.82	1.07	1.08	1.36	1.63	1.65	1.67	2.02	2.41	1.65	ns
DIFF_SSTL135_S	0.75	0.72	0.82	1.07	1.11	1.39	1.67	1.67	1.70	2.05	2.45	1.67	ns
DIFF_SSTL135_DCI_S	0.75	0.72	0.82	1.07	1.11	1.39	1.66	1.65	1.70	2.05	2.45	1.65	ns
DIFF_SSTL135_T_DCI_S	0.75	0.72	0.82	1.07	1.11	1.39	1.66	1.65	1.70	2.05	2.45	1.65	ns
DIFF_SSTL12_S	0.76	0.73	0.82	1.05	1.10	1.39	1.66	1.72	1.70	2.04	2.44	1.72	ns
DIFF_SSTL12_DCI_S	0.76	0.73	0.82	1.05	1.17	1.47	1.75	1.72	1.76	2.12	2.53	1.72	ns
DIFF_SSTL12_T_DCI_S	0.76	0.73	0.82	1.05	1.17	1.47	1.75	1.72	1.76	2.12	2.53	1.72	ns

Table 37: 1.8V IOB High Performance (HP) Switching Characteristics (Cont'd)

I/O Standard	T _{IOP1}				T _{IOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V		0.9V		1.0V		0.9V		1.0V		0.9V		
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
SSTL18_I_F	0.75	0.72	0.82	1.07	1.08	1.36	1.63	1.72	1.68	2.02	2.41	1.72	ns
SSTL18_II_F	0.75	0.72	0.82	1.07	0.99	1.31	1.63	1.63	1.59	1.97	2.41	1.63	ns
SSTL18_I_DCI_F	0.75	0.72	0.82	1.07	1.03	1.31	1.58	1.64	1.63	1.97	2.36	1.64	ns
SSTL18_II_DCI_F	0.75	0.72	0.82	1.07	1.03	1.31	1.58	1.59	1.63	1.97	2.36	1.59	ns
SSTL18_II_T_DCI_F	0.75	0.72	0.82	1.07	1.03	1.31	1.58	1.64	1.63	1.97	2.36	1.64	ns
SSTL15_F	0.75	0.72	0.82	1.07	1.03	1.31	1.56	1.67	1.63	1.96	2.34	1.67	ns
SSTL15_DCI_F	0.75	0.72	0.82	1.07	1.03	1.31	1.56	1.65	1.63	1.96	2.35	1.65	ns
SSTL15_T_DCI_F	0.75	0.72	0.82	1.07	1.03	1.31	1.56	1.65	1.63	1.96	2.35	1.65	ns
SSTL135_F	0.75	0.72	0.82	1.07	1.02	1.30	1.56	1.67	1.62	1.96	2.34	1.67	ns
SSTL135_DCI_F	0.75	0.72	0.82	1.07	1.03	1.30	1.56	1.65	1.62	1.96	2.34	1.65	ns
SSTL135_T_DCI_F	0.75	0.72	0.82	1.07	1.03	1.30	1.56	1.65	1.62	1.96	2.34	1.65	ns
SSTL12_F	0.76	0.73	0.82	1.05	1.02	1.30	1.56	1.72	1.62	1.95	2.34	1.72	ns
SSTL12_DCI_F	0.76	0.73	0.82	1.05	1.05	1.33	1.59	1.72	1.64	1.99	2.37	1.72	ns
SSTL12_T_DCI_F	0.76	0.73	0.82	1.05	1.05	1.33	1.59	1.72	1.64	1.99	2.37	1.72	ns
DIFF_SSTL18_I_F	0.81	0.80	0.91	1.11	1.08	1.36	1.63	1.72	1.68	2.02	2.41	1.72	ns
DIFF_SSTL18_II_F	0.81	0.80	0.91	1.11	0.99	1.31	1.63	1.63	1.59	1.97	2.41	1.63	ns
DIFF_SSTL18_I_DCI_F	0.81	0.80	0.91	1.11	1.03	1.31	1.58	1.64	1.63	1.97	2.36	1.64	ns
DIFF_SSTL18_II_DCI_F	0.81	0.80	0.91	1.11	1.03	1.31	1.58	1.59	1.63	1.97	2.36	1.59	ns
DIFF_SSTL18_II_T_DCI_F	0.81	0.80	0.91	1.11	1.03	1.31	1.58	1.64	1.63	1.97	2.36	1.64	ns
DIFF_SSTL15_F	0.75	0.72	0.82	1.07	1.03	1.31	1.56	1.67	1.63	1.96	2.34	1.67	ns
DIFF_SSTL15_DCI_F	0.75	0.72	0.82	1.07	1.03	1.31	1.56	1.65	1.63	1.96	2.35	1.65	ns
DIFF_SSTL15_T_DCI_F	0.75	0.72	0.82	1.07	1.03	1.31	1.56	1.65	1.63	1.96	2.35	1.65	ns
DIFF_SSTL135_F	0.75	0.72	0.82	1.07	1.02	1.30	1.56	1.67	1.62	1.96	2.34	1.67	ns
DIFF_SSTL135_DCI_F	0.75	0.72	0.82	1.07	1.03	1.30	1.56	1.65	1.62	1.96	2.34	1.65	ns
DIFF_SSTL135_T_DCI_F	0.75	0.72	0.82	1.07	1.03	1.30	1.56	1.65	1.62	1.96	2.34	1.65	ns
DIFF_SSTL12_F	0.76	0.73	0.82	1.05	1.02	1.30	1.56	1.72	1.62	1.95	2.34	1.72	ns
DIFF_SSTL12_DCI_F	0.76	0.73	0.82	1.05	1.05	1.33	1.59	1.72	1.64	1.99	2.37	1.72	ns
DIFF_SSTL12_T_DCI_F	0.76	0.73	0.82	1.05	1.05	1.33	1.59	1.72	1.64	1.99	2.37	1.72	ns

Notes:

1. This I/O standard is only available in the 1.8V high-performance (HP) banks.

Table 38: IOB 3-state ON Output Switching Characteristics (T_{IOTPHZ})

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T _{IOTPHZ}	T input to Pad high-impedance	1.78	1.87	2.01	2.03	ns

Input/Output Logic Switching Characteristics

Table 39: ILOGIC Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup/Hold						
T_{ICE1CK}/T_{ICKCE1}	CE1 pin Setup/Hold with respect to CLK	0.37/ 0.00	0.41/ 0.00	0.47/ 0.00	0.40/ -0.07	ns
T_{ISRCK}/T_{ICKSR}	SR pin Setup/Hold with respect to CLK	0.53/ -0.21	0.61/ -0.21	0.95/ -0.15	0.88/ -0.35	ns
$T_{IDOCKE2}/T_{IOCKDE2}$	D pin Setup/Hold with respect to CLK without Delay (HP I/O banks only)	0.01/ 0.27	0.01/ 0.29	0.01/ 0.34	0.01/ 0.41	ns
$T_{IDOCKDE2}/T_{IOCKDDE2}$	DDLY pin Setup/Hold with respect to CLK (using IDELAY) (HP I/O banks only)	0.01/ 0.27	0.02/ 0.29	0.02/ 0.34	0.01/ 0.41	ns
$T_{IDOCKE3}/T_{IOCKDE3}$	D pin Setup/Hold with respect to CLK without Delay (HR I/O banks only)	0.01/ 0.27	0.01/ 0.29	0.01/ 0.34	0.01/ 0.41	ns
$T_{IDOCKDE3}/T_{IOCKDDE3}$	DDLY pin Setup/Hold with respect to CLK (using IDELAY) (HR I/O banks only)	0.01/ 0.27	0.02/ 0.29	0.02/ 0.34	0.01/ 0.41	ns
Combinatorial						
T_{IDIE2}	D pin to O pin propagation delay, no Delay (HP I/O banks only)	0.09	0.10	0.12	0.14	ns
T_{IDIDE2}	DDLY pin to O pin propagation delay (using IDELAY) (HP I/O banks only)	0.10	0.11	0.13	0.15	ns
T_{IDIE3}	D pin to O pin propagation delay, no Delay (HR I/O banks only)	0.09	0.10	0.12	0.14	ns
T_{IDIDE3}	DDLY pin to O pin propagation delay (using IDELAY) (HR I/O banks only)	0.10	0.11	0.13	0.15	ns
Sequential Delays						
T_{IDLOE2}	D pin to Q1 pin using flip-flop as a latch without Delay (HP I/O banks only)	0.36	0.39	0.45	0.54	ns
T_{IDLDE2}	DDLY pin to Q1 pin using flip-flop as a latch (using IDELAY) (HP I/O banks only)	0.36	0.39	0.45	0.55	ns
T_{IDLOE3}	D pin to Q1 pin using flip-flop as a latch without Delay (HR I/O banks only)	0.36	0.39	0.45	0.54	ns
T_{IDLDE3}	DDLY pin to Q1 pin using flip-flop as a latch (using IDELAY) (HR I/O banks only)	0.36	0.39	0.45	0.55	ns
T_{ICKQ}	CLK to Q outputs	0.47	0.50	0.58	0.71	ns
$T_{RQ_ILOGICE2}$	SR pin to OQ/TQ out (HP I/O banks only)	0.84	0.94	1.16	1.32	ns
$T_{GSRQ_ILOGICE2}$	Global Set/Reset to Q outputs (HP I/O banks only)	7.60	7.60	10.51	11.39	ns
$T_{RQ_ILOGICE3}$	SR pin to OQ/TQ out (HR I/O banks only)	0.84	0.94	1.16	1.32	ns
$T_{GSRQ_ILOGICE3}$	Global Set/Reset to Q outputs (HR I/O banks only)	7.60	7.60	10.51	11.39	ns
Set/Reset						
$T_{RPW_ILOGICE2}$	Minimum Pulse Width, SR inputs (HP I/O banks only)	0.54	0.63	0.63	0.68	ns, Min
$T_{RPW_ILOGICE3}$	Minimum Pulse Width, SR inputs (HR I/O banks only)	0.54	0.63	0.63	0.68	ns, Min

Table 40: OLOGIC Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V		0.9V		
		-3	-2/-2L	-1	-2L	
Setup/Hold						
T_{ODCK}/T_{OOCKD}	D1/D2 pins Setup/Hold with respect to CLK	0.59/ -0.15	0.62/ -0.15	0.70/ -0.15	0.60/ -0.18	ns
$T_{OOCECK}/T_{OOCKOCE}$	OCE pin Setup/Hold with respect to CLK	0.28/ -0.09	0.40/ -0.09	0.40/ -0.09	0.21/ -0.10	ns
T_{OSRCK}/T_{OOCKSR}	SR pin Setup/Hold with respect to CLK	0.32/ 0.11	0.38/ 0.11	0.66/ 0.11	0.62/ -0.25	ns
T_{OTCK}/T_{OOCKT}	T1/T2 pins Setup/Hold with respect to CLK	0.60/ -0.15	0.64/ -0.15	0.72/ -0.15	0.60/ -0.18	ns
$T_{OTCECK}/T_{OOCKTCE}$	TCE pin Setup/Hold with respect to CLK	0.28/ -0.08	0.30/ -0.08	0.40/ -0.08	0.22/ -0.10	ns
Combinatorial						
T_{ODQ}	D1 to OQ out or T1 to TQ out	0.73	0.81	0.97	1.18	ns
Sequential Delays						
T_{OOCKQ}	CLK to OQ/TQ out	0.41	0.43	0.49	0.63	ns
$T_{RQ_OLOGICE2}$	SR pin to OQ/TQ out (HP I/O banks only)	0.63	0.70	0.83	1.12	ns
$T_{GSRQ_OLOGICE2}$	Global Set/Reset to Q outputs (HP I/O banks only)	7.60	7.60	10.51	11.39	ns
$T_{RQ_OLOGICE3}$	SR pin to OQ/TQ out (HR I/O banks only)	0.63	0.70	0.83	1.12	ns
$T_{GSRQ_OLOGICE3}$	Global Set/Reset to Q outputs (HR I/O banks only)	7.60	7.60	10.51	11.39	ns
Set/Reset						
$T_{RPW_OLOGICE2}$	Minimum Pulse Width, SR inputs (HP I/O banks only)	0.54	0.63	0.63	0.68	ns, Min
$T_{RPW_OLOGICE3}$	Minimum Pulse Width, SR inputs (HR I/O banks only)	0.54	0.63	0.63	0.68	ns, Min

Input Serializer/Deserializer Switching Characteristics

Table 41: ISERDES Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup/Hold for Control Lines						
$T_{ISCK_BITSLLIP} / T_{ISCKC_BITSLLIP}$	BITSLIP pin Setup/Hold with respect to CLKDIV	0.01/ 0.12	0.02/ 0.13	0.02/ 0.15	0.02/ 0.21	ns
$T_{ISCKC_CE} / T_{ISCKC_CE}^{(2)}$	CE pin Setup/Hold with respect to CLK (for CE1)	0.34/ -0.02	0.37/ -0.02	0.43/ -0.02	0.35/ -0.11	ns
$T_{ISCKC_CE2} / T_{ISCKC_CE2}^{(2)}$	CE pin Setup/Hold with respect to CLKDIV (for CE2)	-0.12/ 0.29	-0.12/ 0.31	-0.12/ 0.35	-0.17/ 0.40	ns
Setup/Hold for Data Lines						
$T_{ISDCK_D} / T_{ISCKD_D}$	D pin Setup/Hold with respect to CLK	-0.02/ 0.11	-0.02/ 0.12	-0.02/ 0.15	-0.04/ 0.19	ns
$T_{ISDCK_DDLly} / T_{ISCKD_DDLly}$	DDLly pin Setup/Hold with respect to CLK (using IDELAY) ⁽¹⁾	-0.02/ 0.11	-0.02/ 0.12	-0.02/ 0.15	-0.03/ 0.19	ns
$T_{ISDCK_D_DDR} / T_{ISCKD_D_DDR}$	D pin Setup/Hold with respect to CLK at DDR mode	-0.02/ 0.11	-0.02/ 0.12	-0.02/ 0.15	-0.04/ 0.19	ns
$T_{ISDCK_DDLly_DDR} / T_{ISCKD_DDLly_DDR}$	D pin Setup/Hold with respect to CLK at DDR mode (using IDELAY) ⁽¹⁾	0.11/ 0.11	0.12/ 0.12	0.15/ 0.15	0.19/ 0.19	ns
Sequential Delays						
T_{ISCKO_Q}	CLKDIV to out at Q pin	0.43	0.47	0.53	0.67	ns
Propagation Delays						
T_{ISDO_DO}	D input to DO output pin	0.18	0.19	0.22	0.14	ns

Notes:

- Recorded at 0 tap value.
- T_{ISCKC_CE2} and $T_{ISCKC_CE2}^{(2)}$ are reported as $T_{ISCKC_CE} / T_{ISCKC_CE}$ in TRACE report.

Output Serializer/Deserializer Switching Characteristics

Table 42: OSERDES Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup/Hold						
T_{OSDCK_D}/T_{OSCKD_D}	D input Setup/Hold with respect to CLKDIV	0.37/ -0.05	0.40/ -0.05	0.52/ -0.05	0.44/ -0.25	ns
$T_{OSDCK_T}/T_{OSCKD_T}^{(1)}$	T input Setup/Hold with respect to CLK	0.60/ -0.15	0.64/ -0.15	0.71/ -0.15	0.60/ -0.25	ns
$T_{OSDCK_T2}/T_{OSCKD_T2}^{(1)}$	T input Setup/Hold with respect to CLKDIV	0.27/ -0.15	0.30/ -0.15	0.34/ -0.15	0.46/ -0.25	ns
$T_{OSCKK_OCE}/T_{OSCKC_OCE}$	OCE input Setup/Hold with respect to CLK	0.28/ -0.03	0.29/ -0.03	0.39/ -0.03	0.21/ -0.15	ns
T_{OSCKK_S}	SR (Reset) input Setup with respect to CLKDIV	0.41	0.46	0.71	0.70	ns
$T_{OSCKK_TCE}/T_{OSCKC_TCE}$	TCE input Setup/Hold with respect to CLK	0.28/ -0.08	0.30/ -0.08	0.40/ -0.08	0.22/ -0.15	ns
Sequential Delays						
T_{OSCKO_OQ}	Clock to out from CLK to OQ	0.35	0.37	0.42	0.54	ns
T_{OSCKO_TQ}	Clock to out from CLK to TQ	0.41	0.43	0.49	0.63	ns
Combinatorial						
T_{OSDO_TQ}	T input to TQ Out	0.73	0.81	0.97	1.18	ns

Notes:

- T_{OSDCK_T2} and T_{OSCKD_T2} are reported as T_{OSDCK_T}/T_{OSCKD_T} in TRACE report.

Input/Output Delay Switching Characteristics

Table 43: Input/Output Delay Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
IDELAYCTRL						
T _{DLYCCO_RDY}	Reset to Ready for IDELAYCTRL	3.22	3.22	3.22	3.22	µs
F _{IDELAYCTRL_REF}	Attribute REFCLK frequency = 200.0 ⁽¹⁾	200	200	200	200	MHz
	Attribute REFCLK frequency = 300.0 ⁽¹⁾	300	300	N/A	N/A	MHz
IDELAYCTRL_REF_PRECISION	REFCLK precision	±10	±10	±10	±10	MHz
T _{IDELAYCTRL_RPW}	Minimum Reset pulse width	52.00	52.00	52.00	52.00	ns
IDELAY/ODELAY						
T _{IDELAYRESOLUTION}	IDELAY/ODELAY chain delay resolution	1/(32 x 2 x F _{REF})				ps
T _{IDELAYPAT_JIT} and T _{ODELAYPAT_JIT}	Pattern dependent period jitter in delay chain for clock pattern. ⁽²⁾	0	0	0	0	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23) ⁽³⁾	±5	±5	±5	±5	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23) ⁽⁴⁾	±9	±9	±9	±9	ps per tap
T _{IDELAY_CLK_MAX} / T _{ODELAY_CLK_MAX}	Maximum frequency of CLK input to IDELAY/ODELAY	800	800	710	800	MHz
T _{IDCCK_CE} / T _{IDCKC_CE}	CE pin Setup/Hold with respect to C for IDELAY	0.11/ 0.10	0.14/ 0.12	0.18/ 0.14	0.14/ 0.16	ns
T _{ODCCK_CE} / T _{ODCKC_CE}	CE pin Setup/Hold with respect to C for ODELAY	0.14/ 0.03	0.16/ 0.04	0.19/ 0.05	0.28/ 0.06	ns
T _{IDCCK_INC} / T _{IDCKC_INC}	INC pin Setup/Hold with respect to C for IDELAY	0.10/ 0.14	0.12/ 0.16	0.14/ 0.20	0.10/ 0.23	ns
T _{ODCCK_INC} / T _{ODCKC_INC}	INC pin Setup/Hold with respect to C for ODELAY	0.10/ 0.07	0.12/ 0.08	0.13/ 0.09	0.19/ 0.16	ns
T _{IDCCK_RST} / T _{IDCKC_RST}	RST pin Setup/Hold with respect to C for IDELAY	0.13/ 0.08	0.14/ 0.10	0.16/ 0.12	0.22/ 0.19	ns
T _{ODCCK_RST} / T _{ODCKC_RST}	RST pin Setup/Hold with respect to C for ODELAY	0.16/ 0.04	0.19/ 0.06	0.24/ 0.08	0.32/ 0.11	ns
T _{IDDO_IDATAIN}	Propagation delay through IDELAY	Note 5	Note 5	Note 5	Note 5	ps
T _{ODDO_ODATAIN}	Propagation delay through ODELAY	Note 5	Note 5	Note 5	Note 5	ps

Notes:

1. Average Tap Delay at 200 MHz = 78 ps, at 300 MHz = 52 ps.
2. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
3. When HIGH_PERFORMANCE mode is set to TRUE.
4. When HIGH_PERFORMANCE mode is set to FALSE.
5. Delay depends on IDELAY/ODELAY tap setting. See TRACE report for actual values.

I/O FIFO Switching Characteristics

Table 44: IO_FIFO Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
IO_FIFO Clock to Out Delays						
T_{OFFCKO_DO}	RDCLK to Q outputs	0.51	0.56	0.63	0.45	ns
T_{CKO_FLAGS}	Clock to IO_FIFO Flags	0.44	0.46	0.50	0.55	ns
Setup/Hold						
T_{CCK_D}/T_{CKC_D}	D inputs to WRCLK	0.43/ -0.01	0.47/ -0.01	0.53/ -0.01	0.76/ -0.05	ns
$T_{IFFCK_WREN}/T_{IFFCKC_WREN}$	WREN to WRCLK	0.39/ -0.01	0.43/ -0.01	0.50/ -0.01	0.70/ -0.05	ns
$T_{OFFCK_RDEN}/T_{OFFCKC_RDEN}$	RDEN to RDCLK	0.49/ 0.01	0.53/ 0.02	0.61/ 0.02	0.79/ -0.02	ns
Minimum Pulse Width						
$T_{PWH_IO_FIFO}$	RESET, RDCLK, WRCLK	0.81	0.92	1.08	1.29	ns
$T_{PWL_IO_FIFO}$	RESET, RDCLK, WRCLK	0.81	0.92	1.08	1.29	ns
Maximum Frequency						
F_{MAX}	RDCLK and WRCLK	533	470	400	333	MHz

CLB Switching Characteristics

Table 45: CLB Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Combinatorial Delays						
T _{ILO}	An – Dn LUT address to A	0.05	0.05	0.06	0.07	ns, Max
T _{ILO_2}	An – Dn LUT address to AMUX/CMUX	0.15	0.17	0.19	0.22	ns, Max
T _{ILO_3}	An – Dn LUT address to BMUX_A	0.24	0.27	0.30	0.37	ns, Max
T _{ITO}	An – Dn inputs to A – D Q outputs	0.58	0.65	0.74	0.91	ns, Max
T _{AXA}	AX inputs to AMUX output	0.38	0.43	0.49	0.62	ns, Max
T _{AXB}	AX inputs to BMUX output	0.40	0.45	0.52	0.66	ns, Max
T _{AXC}	AX inputs to CMUX output	0.39	0.44	0.50	0.62	ns, Max
T _{AXD}	AX inputs to DMUX output	0.43	0.47	0.52	0.67	ns, Max
T _{BXB}	BX inputs to BMUX output	0.31	0.35	0.40	0.51	ns, Max
T _{BXD}	BX inputs to DMUX output	0.38	0.42	0.47	0.62	ns, Max
T _{CXC}	CX inputs to CMUX output	0.27	0.31	0.34	0.43	ns, Max
T _{CXD}	CX inputs to DMUX output	0.33	0.37	0.41	0.54	ns, Max
T _{DXD}	DX inputs to DMUX output	0.32	0.36	0.40	0.52	ns, Max
T _{OPCYA}	An input to COUT output	0.33	0.37	0.42	0.54	ns, Max
T _{OPCYB}	Bn input to COUT output	0.31	0.35	0.39	0.52	ns, Max
T _{OPCYC}	Cn input to COUT output	0.25	0.28	0.32	0.43	ns, Max
T _{OPCYD}	Dn input to COUT output	0.25	0.28	0.32	0.41	ns, Max
T _{AXCY}	AX input to COUT output	0.29	0.32	0.36	0.47	ns, Max
T _{BXCY}	BX input to COUT output	0.25	0.28	0.31	0.42	ns, Max
T _{CXCY}	CX input to COUT output	0.20	0.22	0.25	0.34	ns, Max
T _{DXCY}	DX input to COUT output	0.19	0.21	0.24	0.32	ns, Max
T _{BYP}	CIN input to COUT output	0.05	0.06	0.06	0.08	ns, Max
T _{CINA}	CIN input to AMUX output	0.23	0.26	0.30	0.38	ns, Max
T _{CINB}	CIN input to BMUX output	0.24	0.28	0.33	0.40	ns, Max
T _{CINC}	CIN input to CMUX output	0.21	0.23	0.26	0.32	ns, Max
T _{CIND}	CIN input to DMUX output	0.24	0.26	0.28	0.35	ns, Max
Sequential Delays						
T _{CKO}	Clock to AQ – DQ outputs	0.26	0.29	0.32	0.40	ns, Max
T _{SHCKO}	Clock to AMUX – DMUX outputs	0.32	0.35	0.39	0.46	ns, Max

Table 45: CLB Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK						
T_{AS}/T_{AH}	$A_N - D_N$ input to CLK on A – D Flip Flops	0.04/ 0.13	0.05/ 0.14	0.06/ 0.15	0.06/ 0.19	ns, Min
T_{DICK}/T_{CKDI}	$A_X - D_X$ input to CLK on A – D Flip Flops	0.04/ 0.14	0.05/ 0.15	0.05/ 0.16	0.05/ 0.21	ns, Min
	$A_X - D_X$ input through MUXs and/or carry logic to CLK on A – D Flip Flops	0.36/ 0.10	0.40/ 0.11	0.46/ 0.12	0.56/ 0.15	ns, Min
$T_{CECK_CLB}/$ T_{CKCE_CLB}	CE input to CLK on A – D Flip Flops	0.19/ -0.02	0.22/ -0.02	0.25/ -0.02	0.24/ -0.02	ns, Min
T_{SRCK}/T_{CKSR}	SR input to CLK on A – D Flip Flops	0.30/ 0.03	0.33/ 0.03	0.37/ 0.03	0.48/ 0.04	ns, Min
T_{CINCK}/T_{CKCIN}	CIN input to CLK on A – D Flip Flops	0.14/ 0.13	0.16/ 0.15	0.19/ 0.16	0.22/ 0.20	ns, Min
Set/Reset						
T_{SRMIN}	SR input minimum pulse width	0.52	0.78	1.04	0.95	ns, Min
T_{RQ}	Delay from SR input to AQ – DQ flip-flops	0.38	0.41	0.46	0.59	ns, Max
T_{CEO}	Delay from CE input to AQ – DQ flip-flops	0.34	0.38	0.43	0.54	ns, Max
F_{TOG}	Toggle frequency (for export control)	1412	1286	1098	1286	MHz

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 46: CLB Distributed RAM Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Sequential Delays						
T_{SHCKO}	Clock to A – B outputs	0.68	0.75	0.85	1.08	ns, Max
T_{SHCKO_1}	Clock to AMUX – BMUX outputs	0.91	1.02	1.15	1.44	ns, Max
Setup and Hold Times Before/After Clock CLK						
T_{DS_LRAM}/T_{DH_LRAM}	A – D inputs to CLK	0.45/ 0.23	0.49/ 0.25	0.54/ 0.27	0.69/ 0.33	ns, Min
T_{AS_LRAM}/T_{AH_LRAM}	Address An inputs to clock	0.13/ 0.50	0.15/ 0.54	0.17/ 0.58	0.21/ 0.63	ns, Min
	Address An inputs through MUXs and/or carry logic to clock	0.40/ 0.16	0.45/ 0.17	0.52/ 0.19	0.63/ 0.23	ns, Min
T_{WS_LRAM}/T_{WH_LRAM}	WE input to clock	0.29/ 0.09	0.32/ 0.09	0.36/ 0.09	0.46/ 0.10	ns, Min
$T_{CECK_LRAM}/T_{CKCE_LRAM}$	CE input to CLK	0.29/ 0.09	0.33/ 0.09	0.37/ 0.09	0.47/ 0.10	ns, Min
Clock CLK						
T_{MPW}	Minimum pulse width	0.68	0.77	0.91	0.82	ns, Min
T_{MCP}	Minimum clock period	1.35	1.54	1.82	1.64	ns, Min

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time.
2. T_{SHCKO} also represents the CLK to XMUX output. Refer to TRACE report for the CLK to XMUX path.

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 47: CLB Shift Register Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Sequential Delays						
T _{REG}	Clock to A – D outputs	0.96	1.06	1.20	1.35	ns, Max
T _{REG_MUX}	Clock to AMUX – DMUX output	1.19	1.32	1.50	1.72	ns, Max
T _{REG_M31}	Clock to DMUX output via M31 output	0.89	0.98	1.10	1.20	ns, Max
Setup and Hold Times Before/After Clock CLK						
T _{WS_SHFREG} / T _{WH_SHFREG}	WE input	0.26/ 0.09	0.29/ 0.09	0.33/ 0.09	0.41/ 0.10	ns, Min
T _{CECK_SHFREG} / T _{CKCE_SHFREG}	CE input to CLK	0.27/ 0.09	0.30/ 0.09	0.33/ 0.09	0.42/ 0.10	ns, Min
T _{DS_SHFREG} / T _{DH_SHFREG}	A – D inputs to CLK	0.28/ 0.26	0.30/ 0.28	0.33/ 0.30	0.41/ 0.36	ns, Min
Clock CLK						
T _{MPW_SHFREG}	Minimum pulse width	0.55	0.65	0.78	0.70	ns, Min

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time.

Block RAM and FIFO Switching Characteristics

Table 48: Block RAM and FIFO Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Block RAM and FIFO Clock-to-Out Delays						
T _{RCKO_DO} and T _{RCKO_DO_REG} ⁽¹⁾	Clock CLK to DOUT output (without output register) ⁽²⁾⁽³⁾	1.78	1.90	2.08	2.75	ns, Max
	Clock CLK to DOUT output (with output register) ⁽⁴⁾⁽⁵⁾	0.54	0.63	0.75	0.94	ns, Max
T _{RCKO_DO_ECC} and T _{RCKO_DO_ECC_REG}	Clock CLK to DOUT output with ECC (without output register) ⁽²⁾⁽³⁾	2.35	2.71	3.26	4.49	ns, Max
	Clock CLK to DOUT output with ECC (with output register) ⁽⁴⁾⁽⁵⁾	0.62	0.69	0.80	0.94	ns, Max
T _{RCKO_DO_CASCOUT} and T _{RCKO_DO_CASCOUT_REG}	Clock CLK to DOUT output with Cascade (without output register) ⁽²⁾	2.21	2.45	2.80	3.19	ns, Max
	Clock CLK to DOUT output with Cascade (with output register) ⁽⁴⁾	0.98	1.08	1.24	1.32	ns, Max
T _{RCKO_FLAGS}	Clock CLK to FIFO flags outputs ⁽⁶⁾	0.65	0.74	0.89	0.87	ns, Max
T _{RCKO_POINTERS}	Clock CLK to FIFO pointers outputs ⁽⁷⁾	0.79	0.87	0.98	1.10	ns, Max
T _{RCKO_PARITY_ECC}	Clock CLK to ECCPARITY in ECC encode only mode	0.66	0.72	0.80	0.93	ns, Max
T _{RCKO_SDBIT_ECC} and T _{RCKO_SDBIT_ECC_REG}	Clock CLK to BITERR (without output register)	2.17	2.50	3.01	4.15	ns, Max
	Clock CLK to BITERR (with output register)	0.57	0.65	0.76	0.89	ns, Max

Table 48: Block RAM and FIFO Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T _{RCKO_RDADDR_ECC} and T _{RCKO_RDADDR_ECC_REG}	Clock CLK to RDADDR output with ECC (without output register)	0.64	0.74	0.90	0.98	ns, Max
	Clock CLK to RDADDR output with ECC (with output register)	0.71	0.79	0.92	1.10	ns, Max
Setup and Hold Times Before/After Clock CLK						
T _{RCKC_ADDRA} /T _{RCKC_ADDRA}	ADDR inputs ⁽⁸⁾	0.38/ 0.27	0.42/ 0.28	0.48/ 0.31	0.65/ 0.31	ns, Min
T _{RDCK_DI_WF_NC} / T _{RCKD_DI_WF_NC}	Data input setup/hold time when block RAM is configured in WRITE_FIRST or NO_CHANGE mode ⁽⁹⁾	0.49/ 0.51	0.55/ 0.53	0.63/ 0.57	0.78/ 0.27	ns, Min
T _{RDCK_DI_RF} /T _{RCKD_DI_RF}	Data input setup/hold time when block RAM is configured in READ_FIRST mode ⁽⁹⁾	0.17/ 0.25	0.19/ 0.29	0.21/ 0.35	0.25/ 0.27	ns, Min
T _{RDCK_DI_ECC} /T _{RCKD_DI_ECC}	DIN inputs with block RAM ECC in standard mode ⁽⁹⁾	0.42/ 0.37	0.47/ 0.39	0.53/ 0.43	0.66/ 0.31	ns, Min
T _{RDCK_DI_ECCW} /T _{RCKD_DI_ECCW}	DIN inputs with block RAM ECC encode only ⁽⁹⁾	0.79/ 0.37	0.87/ 0.39	0.99/ 0.43	1.17/ 0.31	ns, Min
T _{RDCK_DI_ECC_FIFO} / T _{RCKD_DI_ECC_FIFO}	DIN inputs with FIFO ECC in standard mode ⁽⁹⁾	0.89/ 0.47	0.98/ 0.50	1.12/ 0.54	1.32/ 0.31	ns, Min
T _{RCKC_INJECTBITERR} / T _{RCKC_INJECTBITERR}	Inject single/double bit error in ECC mode	0.49/ 0.30	0.55/ 0.31	0.63/ 0.34	0.78/ 0.24	ns, Min
T _{RCKC_EN} /T _{RCKC_EN}	Block RAM Enable (EN) input	0.30/ 0.17	0.33/ 0.18	0.38/ 0.20	0.48/ 0.22	ns, Min
T _{RCKC_REGCE} /T _{RCKC_REGCE}	CE input of output register	0.21/ 0.13	0.25/ 0.13	0.31/ 0.14	0.28/ 0.06	ns, Min
T _{RCKC_RSTREG} /T _{RCKC_RSTREG}	Synchronous RSTREG input ⁽¹⁰⁾	0.25/ 0.06	0.27/ 0.06	0.29/ 0.06	0.35/ 0.03	ns, Min
T _{RCKC_RSTRAM} /T _{RCKC_RSTRAM}	Synchronous RSTRAM input	0.27/ 0.35	0.29/ 0.37	0.31/ 0.39	0.34/ 0.18	ns, Min
T _{RCKC_WEA} /T _{RCKC_WEA}	Write Enable (WE) input (Block RAM only)	0.38/ 0.15	0.41/ 0.16	0.46/ 0.17	0.54/ 0.19	ns, Min
T _{RCKC_WREN} /T _{RCKC_WREN}	WREN FIFO inputs	0.39/ 0.25	0.39/ 0.30	0.40/ 0.37	0.65/ 0.22	ns, Min
T _{RCKC_RDEN} /T _{RCKC_RDEN}	RDEN FIFO inputs	0.36/ 0.26	0.36/ 0.30	0.37/ 0.37	0.60/ 0.12	ns, Min
Reset Delays (Flags)						
T _{RCO_RST}	Reset RST to FIFO Flags/Pointers ⁽¹¹⁾	0.76	0.83	0.93	1.06	ns, Max
Maximum Frequency						
F _{MAX_BRAM_WF_NC}	Block RAM (Write first and No change modes) When not in SDP RF mode	601	543	458	372	MHz
F _{MAX_BRAM_RF_PERFORMANCE}	Block RAM (Read first, Performance mode) When in SDP RF mode but no address overlap between port A and port B	601	543	458	372	MHz

Table 48: Block RAM and FIFO Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
F _{MAX_BRAM_RF_DELAYED_WRITE}	Block RAM (Read first, Delayed_write mode) When in SDP RF mode and there is possibility of overlap between port A and port B addresses	528	477	400	317	MHz
F _{MAX_CAS_WF_NC}	Block RAM Cascade (Write first, No change mode) When cascade but not in RF mode	551	493	408	322	MHz
F _{MAX_CAS_RF_PERFORMANCE}	Block RAM Cascade (Read first, Performance mode) When in cascade with RF mode and no possibility of address overlap/one port is disabled	551	493	408	322	MHz
F _{MAX_CAS_RF_DELAYED_WRITE}	When in cascade RF mode and there is a possibility of address overlap between port A and port B	478	427	350	267	MHz
F _{MAX_FIFO}	FIFO in all modes without ECC	601	543	458	372	MHz
F _{MAX_ECC}	Block RAM and FIFO in ECC configuration	484	430	351	254	MHz

Notes:

- TRACE will report all of these parameters as T_{RCKO_DO}.
- T_{RCKO_DOR} includes T_{RCKO_DOW}, T_{RCKO_DOPR}, and T_{RCKO_DOPW} as well as the B port equivalent timing parameters.
- These parameters also apply to synchronous FIFO with DO_REG = 0.
- T_{RCKO_DO} includes T_{RCKO_DOP} as well as the B port equivalent timing parameters.
- These parameters also apply to multirate (asynchronous) and synchronous FIFO with DO_REG = 1.
- T_{RCKO_FLAGS} includes the following parameters: T_{RCKO_AEMPTY}, T_{RCKO_AFULL}, T_{RCKO_EMPTY}, T_{RCKO_FULL}, T_{RCKO_RDERR}, T_{RCKO_WRERR}.
- T_{RCKO_POINTERS} includes both T_{RCKO_RDCOUNT} and T_{RCKO_WRCOUNT}.
- The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
- T_{RCKO_DI} includes both A and B inputs as well as the parity inputs of A and B.
- RDEN and WREN must be held Low prior to and during reset. The FIFO reset must be asserted for at least five positive clock edges of the slowest clock (WRCLK or RDCLK).
- T_{RCO_FLAGS} includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.

DSP48E1 Switching Characteristics

Table 49: DSP48E1 Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup and Hold Times of Data/Control Pins to the Input Register Clock						
$T_{\text{DSPDCK_A_AREG}}/T_{\text{DSPCKD_A_AREG}}$	A input to A register CLK	0.24/ 0.12	0.27/ 0.14	0.31/ 0.16	0.38/ 0.12	ns
$T_{\text{DSPDCK_B_BREG}}/T_{\text{DSPCKD_B_BREG}}$	B input to B register CLK	0.28/ 0.13	0.32/ 0.14	0.39/ 0.15	0.51/ 0.16	ns
$T_{\text{DSPDCK_C_CREG}}/T_{\text{DSPCKD_C_CREG}}$	C input to C register CLK	0.15/ 0.15	0.17/ 0.17	0.20/ 0.20	0.29/ 0.25	ns
$T_{\text{DSPDCK_D_DREG}}/T_{\text{DSPCKD_D_DREG}}$	D input to D register CLK	0.21/ 0.19	0.27/ 0.22	0.35/ 0.26	0.46/ 0.20	ns
$T_{\text{DSPDCK_ACIN_AREG}}/T_{\text{DSPCKD_ACIN_AREG}}$	ACIN input to A register CLK	0.21/ 0.12	0.24/ 0.14	0.27/ 0.16	0.31/ 0.12	ns
$T_{\text{DSPDCK_BCIN_BREG}}/T_{\text{DSPCKD_BCIN_BREG}}$	BCIN input to B register CLK	0.22/ 0.13	0.25/ 0.14	0.30/ 0.15	0.34/ 0.16	ns
Setup and Hold Times of Data Pins to the Pipeline Register Clock						
$T_{\text{DSPDCK_}\{A, B\}_MREG_MULT}/T_{\text{DSPCKD_B_MREG_MULT}}$	{A, B,} input to M register CLK using multiplier	2.04/ -0.01	2.34/ -0.01	2.79/ -0.01	3.66/ -0.06	ns
$T_{\text{DSPDCK_}\{A, B\}_ADREG}/T_{\text{DSPCKD_D_ADREG}}$	{A, D} input to AD register CLK	1.09/ -0.02	1.25/ -0.02	1.49/ -0.02	1.94/ -0.23	ns
Setup and Hold Times of Data/Control Pins to the Output Register Clock						
$T_{\text{DSPDCK_}\{A, B\}_PREG_MULT}/T_{\text{DSPCKD_}\{A, B\}_PREG_MULT}$	{A, B,} input to P register CLK using multiplier	3.41/ -0.24	3.90/ -0.24	4.64/ -0.24	5.89/ -0.41	ns
$T_{\text{DSPDCK_D_PREG_MULT}}/T_{\text{DSPCKD_D_PREG_MULT}}$	D input to P register CLK using multiplier	3.33/ -0.62	3.81/ -0.62	4.53/ -0.62	5.70/ -1.42	ns
$T_{\text{DSPDCK_}\{A, B\}_PREG}/T_{\text{DSPCKD_}\{A, B\}_PREG}$	A or B input to P register CLK not using multiplier	1.47/ -0.24	1.68/ -0.24	2.00/ -0.24	2.37/ -0.41	ns
$T_{\text{DSPDCK_C_PREG}}/T_{\text{DSPCKD_C_PREG}}$	C input to P register CLK not using multiplier	1.30/ -0.22	1.49/ -0.22	1.78/ -0.22	2.15/ -0.38	ns
$T_{\text{DSPDCK_PCIN_PREG}}/T_{\text{DSPCKD_PCIN_PREG}}$	PCIN input to P register CLK	1.12/ -0.13	1.28/ -0.13	1.52/ -0.13	1.81/ -0.21	ns
Setup and Hold Times of the CE Pins						
$T_{\text{DSPDCK_}\{CEA;CEB\}_AREG;BREG}/T_{\text{DSPCKD_}\{CEA;CEB\}_AREG;BREG}$	{CEA; CEB} input to {A; B} register CLK	0.30/ 0.05	0.36/ 0.06	0.44/ 0.09	0.55/ 0.09	ns
$T_{\text{DSPDCK_CEC_CREG}}/T_{\text{DSPCKD_CEC_CREG}}$	CEC input to C register CLK	0.24/ 0.08	0.29/ 0.09	0.36/ 0.11	0.42/ 0.14	ns
$T_{\text{DSPDCK_CED_DREG}}/T_{\text{DSPCKD_CED_DREG}}$	CED input to D register CLK	0.31/ -0.02	0.36/ -0.02	0.44/ -0.02	0.58/ 0.12	ns
$T_{\text{DSPDCK_CEM_MREG}}/T_{\text{DSPCKD_CEM_MREG}}$	CEM input to M register CLK	0.26/ 0.15	0.29/ 0.17	0.33/ 0.20	0.39/ 0.25	ns
$T_{\text{DSPDCK_CEP_PREG}}/T_{\text{DSPCKD_CEP_PREG}}$	CEP input to P register CLK	0.31/ 0.01	0.36/ 0.01	0.45/ 0.01	0.54/ 0.00	ns

Table 49: DSP48E1 Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup and Hold Times of the RST Pins						
$T_{D\text{SPDCK}_{\{RSTA; RSTB\}_{\{AREG; BREG\}}}$ / $T_{D\text{SPCKD}_{\{RSTA; RSTB\}_{\{AREG; BREG\}}}$	{RSTA, RSTB} input to {A, B} register CLK	0.34/ 0.10	0.39/ 0.11	0.47/ 0.13	0.53/ 0.34	ns
$T_{D\text{SPDCK}_{RSTC_CREG}}/ T_{D\text{SPCKD}_{RSTC_CREG}}$	RSTC input to C register CLK	0.06/ 0.22	0.07/ 0.24	0.08/ 0.26	0.11/ 0.09	ns
$T_{D\text{SPDCK}_{RSTD_DREG}}/ T_{D\text{SPCKD}_{RSTD_DREG}}$	RSTD input to D register CLK	0.37/ 0.06	0.42/ 0.06	0.50/ 0.07	0.57/ 0.07	ns
$T_{D\text{SPDCK}_{RSTM_MREG}}/ T_{D\text{SPCKD}_{RSTM_MREG}}$	RSTM input to M register CLK	0.18/ 0.18	0.20/ 0.21	0.23/ 0.24	0.24/ 0.29	ns
$T_{D\text{SPDCK}_{RSTP_PREG}}/ T_{D\text{SPCKD}_{RSTP_PREG}}$	RSTP input to P register CLK	0.24/ 0.01	0.26/ 0.01	0.30/ 0.01	0.37/ 0.00	ns
Combinatorial Delays from Input Pins to Output Pins						
$T_{D\text{SPDO}_{A_CARRYOUT_MULT}}$	A input to CARRYOUT output using multiplier	3.21	3.69	4.39	5.60	ns
$T_{D\text{SPDO}_{D_P_MULT}}$	D input to P output using multiplier	3.15	3.61	4.30	5.44	ns
$T_{D\text{SPDO}_{A_P}}$	A input to P output not using multiplier	1.30	1.48	1.76	2.10	ns
$T_{D\text{SPDO}_{C_P}}$	C input to P output	1.13	1.30	1.55	1.89	ns
Combinatorial Delays from Input Pins to Cascading Output Pins						
$T_{D\text{SPDO}_{\{A; B\}_{\{ACOUT; BCOUT\}}}$	{A, B} input to {ACOUT, BCOUT} output	0.47	0.53	0.63	0.73	ns
$T_{D\text{SPDO}_{\{A; B\}_{CARRYCASCOUT_MULT}}$	{A, B} input to CARRYCASCOUT output using multiplier	3.44	3.94	4.69	5.96	ns
$T_{D\text{SPDO}_{D_CARRYCASCOUT_MULT}}$	D input to CARRYCASCOUT output using multiplier	3.36	3.85	4.58	5.77	ns
$T_{D\text{SPDO}_{\{A; B\}_{CARRYCASCOUT}}$	{A, B} input to CARRYCASCOUT output not using multiplier	1.50	1.72	2.04	2.44	ns
$T_{D\text{SPDO}_{C_CARRYCASCOUT}}$	C input to CARRYCASCOUT output	1.34	1.53	1.83	2.22	ns
Combinatorial Delays from Cascading Input Pins to All Output Pins						
$T_{D\text{SPDO}_{ACIN_P_MULT}}$	ACIN input to P output using multiplier	3.09	3.55	4.24	5.42	ns
$T_{D\text{SPDO}_{ACIN_P}}$	ACIN input to P output not using multiplier	1.16	1.33	1.59	2.07	ns
$T_{D\text{SPDO}_{ACIN_ACOUT}}$	ACIN input to ACOUT output	0.32	0.37	0.45	0.53	ns
$T_{D\text{SPDO}_{ACIN_CARRYCASCOUT_MULT}}$	ACIN input to CARRYCASCOUT output using multiplier	3.30	3.79	4.52	5.76	ns
$T_{D\text{SPDO}_{ACIN_CARRYCASCOUT}}$	ACIN input to CARRYCASCOUT output not using multiplier	1.37	1.57	1.87	2.40	ns
$T_{D\text{SPDO}_{PCIN_P}}$	PCIN input to P output	0.94	1.08	1.29	1.54	ns
$T_{D\text{SPDO}_{PCIN_CARRYCASCOUT}}$	PCIN input to CARRYCASCOUT output	1.15	1.32	1.57	1.88	ns
Clock to Outs from Output Register Clock to Output Pins						
$T_{D\text{SPCKO}_{P_PREG}}$	CLK PREG to P output	0.33	0.35	0.39	0.45	ns
$T_{D\text{SPCKO}_{CARRYCASCOUT_PREG}}$	CLK PREG to CARRYCASCOUT output	0.44	0.50	0.59	0.71	ns

Table 49: DSP48E1 Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Clock to Outs from Pipeline Register Clock to Output Pins						
T _{DSPCKO_P_MREG}	CLK MREG to P output	1.42	1.64	1.96	2.31	ns
T _{DSPCKO_CARRYCASCOU_T_MREG}	CLK MREG to CARRYCASCOU_T output	1.63	1.87	2.24	2.65	ns
T _{DSPCKO_P_ADREG_MULT}	CLK ADREG to P output using multiplier	2.30	2.63	3.13	3.90	ns
T _{DSPCKO_CARRYCASCOU_ADREG_MULT}	CLK ADREG to CARRYCASCOU_T output using multiplier	2.51	2.87	3.41	4.23	ns
Clock to Outs from Input Register Clock to Output Pins						
T _{DSPCKO_P_AREG_MULT}	CLK AREG to P output using multiplier	3.34	3.83	4.55	5.80	ns
T _{DSPCKO_P_BREG}	CLK BREG to P output not using multiplier	1.39	1.59	1.88	2.24	ns
T _{DSPCKO_P_CREG}	CLK CREG to P output not using multiplier	1.43	1.64	1.95	2.38	ns
T _{DSPCKO_P_DREG_MULT}	CLK DREG to P output using multiplier	3.32	3.80	4.51	5.74	ns
Clock to Outs from Input Register Clock to Cascading Output Pins						
T _{DSPCKO_{ACOUT; BCOUT}_{AREG; BREG}}	CLK (ACOUT, BCOUT) to {A,B} register output	0.55	0.62	0.74	0.87	ns
T _{DSPCKO_CARRYCASCOU_{AREG, BREG}_MULT}	CLK (AREG, BREG) to CARRYCASCOU_T output using multiplier	3.55	4.06	4.84	6.13	ns
T _{DSPCKO_CARRYCASCOU_BREG}	CLK BREG to CARRYCASCOU_T output not using multiplier	1.60	1.82	2.16	2.58	ns
T _{DSPCKO_CARRYCASCOU_DREG_MULT}	CLK DREG to CARRYCASCOU_T output using multiplier	3.52	4.03	4.79	6.07	ns
T _{DSPCKO_CARRYCASCOU_CREG}	CLK CREG to CARRYCASCOU_T output	1.64	1.88	2.23	2.71	ns
Maximum Frequency						
F _{MAX}	With all registers used	741	650	547	429	MHz
F _{MAX_PATDET}	With pattern detector	627	549	463	365	MHz
F _{MAX_MULT_NOMREG}	Two register multiply without MREG	412	360	303	248	MHz
F _{MAX_MULT_NOMREG_PATDET}	Two register multiply without MREG with pattern detect	374	327	276	225	MHz
F _{MAX_PREADD_MULT_NOADREG}	Without ADREG	468	408	342	263	MHz
F _{MAX_PREADD_MULT_NOADREG_PATDET}	Without ADREG with pattern detect	468	408	342	263	MHz
F _{MAX_NOPIPELINEREG}	Without pipeline registers (MREG, ADREG)	306	267	225	177	MHz
F _{MAX_NOPIPELINEREG_PATDET}	Without pipeline registers (MREG, ADREG) with pattern detect	285	249	209	165	MHz

Configuration Switching Characteristics

Table 50: Configuration Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Power-up Timing Characteristics						
$T_{PL}^{(1)}$	Program latency	5	5	5	5	ms, Max
$T_{POR}^{(1)}$	Power-on reset (50ms ramp rate time)	10/50	10/50	10/50	10/50	ms, Min/Max
	Power-on reset (1ms ramp rate time)	10/35	10/35	10/35	10/35	ms, Min/Max
$T_{PROGRAM}$	Program pulse width	250	250	250	250	ns, Min
CCLK Output (Master Mode)						
T_{ICCK}	Master CCLK output delay	150	150	150	150	ns, Min
T_{MCCKL}	Master CCLK clock Low time duty cycle	40/60	40/60	40/60	40/60	%, Min/Max
T_{MCCKH}	Master CCLK clock High time duty cycle	40/60	40/60	40/60	40/60	%, Min/Max
F_{MCCK}	Master CCLK frequency	100	100	100	70	MHz, Max
	Master CCLK frequency for AES encrypted x16	50	50	50	50	MHz, Max
F_{MCCK_START}	Master CCLK frequency at start of configuration	3	3	3	3	MHz, Typ
$F_{MCCKTOL}$	Frequency tolerance, master mode with respect to nominal CCLK	±50	±50	±50	±50	%, Max
CCLK Input (Slave Modes)						
T_{SCCKL}	Slave CCLK clock minimum Low time	2.5	2.5	2.5	2.5	ns, Min
T_{SCCKH}	Slave CCLK clock minimum High time	2.5	2.5	2.5	2.5	ns, Min
F_{SCCK}	Slave CCLK frequency	100	100	100	70	MHz, Max
EMCCLK Input (Master Mode)						
T_{EMCCKL}	External master CCLK Low time	2.5	2.5	2.5	2.5	ns, Min
T_{EMCCKH}	External master CCLK High time	2.5	2.5	2.5	2.5	ns, Min
F_{EMCCK}	External master CCLK frequency	100	100	100	70	MHz, Max
Master/Slave Serial Mode Programming Switching						
T_{DCCK}/T_{CCKD}	DIN Setup/Hold	4.0/0.0	4.0/0.0	4.0/0.0	5.0/0.0	ns, Min
T_{CCO}	DOOUT clock to out	8.0	8.0	8.0	9.0	ns, Max
SelectMAP Mode Programming Switching						
T_{SMDCCK}/T_{SMCCKD}	D[31:00] Setup/Hold	4.0/0.0	4.0/0.0	4.0/0.0	4.5/0.0	ns, Min
$T_{SMCSCCK}/T_{SMCCKCS}$	CSI_B Setup/Hold	4.0/0.0	4.0/0.0	4.0/0.0	5.0/0.0	ns, Min
T_{SMWCK}/T_{SMCCKW}	RDWR_B Setup/Hold	10.0/0.0	10.0/0.0	10.0/0.0	12.0/0.0	ns, Min
$T_{SMCKCSO}$	CSO_B clock to out (330 Ω pull-up resistor required)	7.0	7.0	7.0	8.0	ns, Max
T_{SMCO}	D[31:00] clock to out in readback	8.0	8.0	8.0	10.0	ns, Max
F_{RBCK}	Readback frequency	100	100	100	70	MHz, Max

Table 50: Configuration Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Boundary-Scan Port Timing Specifications						
T_{TAPTCK}/T_{TCKTAP}	TMS and TDI Setup/Hold	3.0/2.0	3.0/2.0	3.0/2.0	3.0/2.0	ns, Min
T_{TCKTDO}	TCK falling edge to TDO output	7.0	7.0	7.0	8.5	ns, Max
F_{TCK}	TCK frequency	66	66	66	50	MHz, Max
BPI Master Flash Mode Programming Switching						
$T_{BPICCO}^{(2)}$	A[28:00], RS[1:0], FCS_B, FOE_B, FWE_B, ADV_B clock to out	8.5	8.5	8.5	10.0	ns, Max
T_{BPIDCC}/T_{BPICCD}	D[15:00] Setup/Hold	4.0/0.0	4.0/0.0	4.0/0.0	4.5/0.0	ns, Min
SPI Master Flash Mode Programming Switching						
T_{SPIDCC}/T_{SPICCD}	D[03:00] Setup/Hold	3.0/0.0	3.0/0.0	3.0/0.0	3.0/0.0	ns, Min
T_{SPICCM}	MOSI clock to out	8.0	8.0	8.0	9.0	ns, Max
T_{SPICFC}	FCS_B clock to out	8.0	8.0	8.0	9.0	ns, Max
Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK						
$T_{MMCMDCK_DADDR}/T_{MMCMCKD_DADDR}$	DADDR Setup/Hold	1.25/ 0.15	1.40/ 0.15	1.63/ 0.15	1.43/ 0.00	ns, Min
$T_{MMCMDCK_DI}/T_{MMCMCKD_DI}$	DI Setup/Hold	1.25/ 0.15	1.40/ 0.15	1.63/ 0.15	1.43/ 0.00	ns, Min
$T_{MMCMDCK_DEN}/T_{MMCMCKD_DEN}$	DEN Setup/Hold	1.76/ 0.00	1.97/ 0.00	2.29/ 0.00	2.40/ 0.00	ns, Min
$T_{MMCMDCK_DWE}/T_{MMCMCKD_DWE}$	DWE Setup/Hold	1.25/ 0.15	1.40/ 0.15	1.63/ 0.15	1.43/ 0.00	ns, Min
$T_{MMCMCKO_DO}$	CLK to out of DO ⁽³⁾	0.55	0.62	0.74	0.70	ns, Max
$T_{MMCMCKO_DRDY}$	CLK to out of DRDY	0.65	0.72	0.99	0.70	ns, Max
F_{DCK}	DCLK frequency	200	200	200	200	MHz, Max

Notes:

1. To support longer delays in configuration, use the design solutions described in [UG470: 7 Series FPGA Configuration User Guide](#).
2. Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.
3. DO will hold until next DRP operation.

Clock Buffers and Networks

Table 51: Global Clock Switching Characteristics (Including BUFCTRL)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
$T_{BCCCK_CE}/T_{BCCCK_CE}^{(1)}$	CE pins Setup/Hold	0.12/ 0.26	0.14/ 0.28	0.26/ 0.31	0.28/ 0.16	ns
$T_{BCCCK_S}/T_{BCCCK_S}^{(1)}$	S pins Setup/Hold	0.12/ 0.26	0.14/ 0.28	0.26/ 0.31	0.28/ 0.16	ns
$T_{BCCCKO_O}^{(2)}$	BUFCTRL delay from I0/I1 to O	0.08	0.10	0.12	0.13	ns
Maximum Frequency						
F_{MAX_BUFG}	Global clock tree (BUFG)	741	710	625	560	MHz

Notes:

- T_{BCCCK_CE} and T_{BCCCK_S} must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFMUX primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
- T_{BCCCKO_O} (BUFG delay from I0 to O) values are the same as T_{BCCCKO_O} values.

Table 52: Input/Output Clock Switching Characteristics (BUFIO)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T_{BIOCKO_O}	Clock to out delay from I to O	1.07	1.23	1.50	1.50	ns
Maximum Frequency						
F_{MAX_BUFIO}	I/O clock tree (BUFIO)	800	800	710	710	MHz

Table 53: Regional Clock Buffer Switching Characteristics (BUFR)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T_{BRCKO_O}	Clock to out delay from I to O	0.65	0.81	1.05	1.08	ns
$T_{BRCKO_O_BYP}$	Clock to out delay from I to O with Divide Bypass attribute set	0.32	0.38	0.52	0.57	ns
T_{BRDO_O}	Propagation delay from CLR to O	0.68	0.75	0.88	0.96	ns
Maximum Frequency						
$F_{MAX_BUFR}^{(1)}$	Regional clock tree (BUFR)	600	540	450	450	MHz

Notes:

- The maximum input frequency to the BUFR is the BUFIO F_{MAX} frequency.

Table 54: Horizontal Clock Buffer Switching Characteristics (BUFH)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T _{BHCKO_O}	BUFH delay from I to O	0.09	0.11	0.13	0.14	ns
T _{BHCKK_CE} /T _{BHCKC_CE}	CE pin Setup and Hold	0.19/ 0.16	0.23/ 0.17	0.38/ 0.21	0.32/ 0.07	ns
Maximum Frequency						
F _{MAX_BUFH}	Horizontal clock buffer (BUFH)	741	710	625	560	MHz

MMCM Switching Characteristics

Table 55: MMCM Specification

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
MMCM_F _{INMAX}	Maximum Input Clock Frequency	1066	933	800	800	MHz
MMCM_F _{INMIN}	Minimum Input Clock Frequency	10	10	10	10	MHz
MMCM_F _{INJITTER}	Maximum Input Clock Period Jitter	< 20% of clock input period or 1 ns Max				
MMCM_F _{INDUTY}	Allowable Input Duty Cycle: 10—49 MHz	25	25	25	25	%
	Allowable Input Duty Cycle: 50—199 MHz	30	30	30	30	%
	Allowable Input Duty Cycle: 200—399 MHz	35	35	35	35	%
	Allowable Input Duty Cycle: 400—499 MHz	40	40	40	40	%
	Allowable Input Duty Cycle: >500 MHz	45	45	45	45	%
MMCM_F _{MIN_PSCLK}	Minimum Dynamic Phase Shift Clock Frequency	0.01	0.01	0.01	0.01	MHz
MMCM_F _{MAX_PSCLK}	Maximum Dynamic Phase Shift Clock Frequency	550	500	450	450	MHz
MMCM_F _{VCOMIN}	Minimum MMCM VCO Frequency	600	600	600	600	MHz
MMCM_F _{VCOMAX}	Maximum MMCM VCO Frequency	1600	1440	1200	1200	MHz
MMCM_F _{BANDWIDTH}	Low MMCM Bandwidth at Typical ⁽¹⁾	1.00	1.00	1.00	1.00	MHz
	High MMCM Bandwidth at Typical ⁽¹⁾	4.00	4.00	4.00	4.00	MHz
MMCM_T _{STATPHAOFFSET}	Static Phase Offset of the MMCM Outputs ⁽²⁾	0.12	0.12	0.12	0.12	ns
MMCM_T _{OUTJITTER}	MMCM Output Jitter ⁽³⁾	Note 1				
MMCM_T _{OUTDUTY}	MMCM Output Clock Duty Cycle Precision ⁽⁴⁾	0.20	0.20	0.20	0.25	ns
MMCM_T _{LOCKMAX}	MMCM Maximum Lock Time	100	100	100	100	µs
MMCM_F _{OUTMAX}	MMCM Maximum Output Frequency	1066	933	800	800	MHz
MMCM_F _{OUTMIN}	MMCM Minimum Output Frequency ⁽⁵⁾⁽⁶⁾	4.69	4.69	4.69	4.69	MHz
MMCM_T _{EXTFDVAR}	External Clock Feedback Variation	< 20% of clock input period or 1 ns Max				
MMCM_RST _{MINPULSE}	Minimum Reset Pulse Width	5.00	5.00	5.00	5.00	ns
MMCM_F _{PFDMAX}	Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to High or Optimized	550	500	450	450	MHz
	Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to Low	300	300	300	300	MHz
MMCM_F _{PFDMIN}	Minimum Frequency at the Phase Frequency Detector	10	10	10	10	MHz
MMCM_T _{FBDELAY}	Maximum Delay in the Feedback Path	3 ns Max or one CLKIN cycle				

Table 55: MMCM Specification (Cont'd)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
MMCM Switching Characteristics Setup and Hold						
$T_{MMCM DCK_PSEN}$ / $T_{MMCM CKD_PSEN}$	Setup and Hold of Phase Shift Enable	1.04/ 0.00	1.04/ 0.00	1.04/ 0.00	1.04/ 0.00	ns
$T_{MMCM DCK_PSINCDEC}$ / $T_{MMCM CKD_PSINCDEC}$	Setup and Hold of Phase Shift Increment/Decrement	1.04/ 0.00	1.04/ 0.00	1.04/ 0.00	1.04/ 0.00	ns
$T_{MMCM CKO_PSDONE}$	Phase Shift Clock-to-Out of PSDONE	0.59	0.68	0.81	0.78	ns

Notes:

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.
6. When $CLKOUT4_CASCADE = TRUE$, $MMCM_F_{OUTMIN}$ is 0.036 MHz.

PLL Switching Characteristics

Table 56: PLL Specification

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
PLL_F_{INMAX}	Maximum Input Clock Frequency	1066	933	800	800	MHz
PLL_F_{INMIN}	Minimum Input Clock Frequency	19	19	19	19	MHz
$PLL_F_{INJITTER}$	Maximum Input Clock Period Jitter	< 20% of clock input period or 1 ns Max				
PLL_F_{INDUTY}	Allowable Input Duty Cycle: 19—49 MHz	25	25	25	25	%
	Allowable Input Duty Cycle: 50—199 MHz	30	30	30	30	%
	Allowable Input Duty Cycle: 200—399 MHz	35	35	35	35	%
	Allowable Input Duty Cycle: 400—499 MHz	40	40	40	40	%
	Allowable Input Duty Cycle: >500 MHz	45	45	45	45	%
PLL_F_{VCOMIN}	Minimum PLL VCO Frequency	800	800	800	800	MHz
PLL_F_{VCOMAX}	Maximum PLL VCO Frequency	2133	1866	1600	1600	MHz
$PLL_F_{BANDWIDTH}$	Low PLL Bandwidth at Typical ⁽¹⁾	1.00	1.00	1.00	1.00	MHz
	High PLL Bandwidth at Typical ⁽¹⁾	4.00	4.00	4.00	4.00	MHz
$PLL_T_{STATPHAOFFSET}$	Static Phase Offset of the PLL Outputs ⁽²⁾	0.12	0.12	0.12	0.12	ns
$PLL_T_{OUTJITTER}$	PLL Output Jitter ⁽³⁾	Note 1				
$PLL_T_{OUTDUTY}$	PLL Output Clock Duty Cycle Precision ⁽⁴⁾	0.20	0.20	0.20	0.25	ns
$PLL_T_{LOCKMAX}$	PLL Maximum Lock Time	100	100	100	100	μs
PLL_F_{OUTMAX}	PLL Maximum Output Frequency	1066	933	800	800	MHz
PLL_F_{OUTMIN}	PLL Minimum Output Frequency ⁽⁵⁾	6.25	6.25	6.25	6.25	MHz
$PLL_T_{EXTFDVAR}$	External Clock Feedback Variation	< 20% of clock input period or 1 ns Max				
$PLL_RST_{MINPULSE}$	Minimum Reset Pulse Width	5.00	5.00	5.00	5.00	ns

Table 56: PLL Specification (Cont'd)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
PLL_FPFDMAX	Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to High or Optimized	550	500	450	450	MHz
	Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to Low	300	300	300	300	MHz
PLL_FPFDMIN	Minimum Frequency at the Phase Frequency Detector	19	19	19	19	MHz
PLL_TFBDELAY	Maximum Delay in the Feedback Path	3 ns Max or one CLKIN cycle				
PLL Switching Characteristics Setup and Hold						
T _{PLLCKC_DEN} / T _{PLLCKC_DEN}	Setup and Hold of D enable	1.76/ 0.00	1.97/ 0.00	2.29/ 0.00	2.40/ 0.00	ns
T _{PLLCKC_DADDR} / T _{PLLCKC_DADDR}	Setup and Hold of D address	1.25/ 0.15	1.40/ 0.15	1.63/ 0.15	1.43/ 0.00	ns
T _{PLLCKC_DI} / T _{PLLCKC_DI}	Setup and Hold of D input	1.25/ 0.15	1.40/ 0.15	1.63/ 0.15	1.43/ 0.00	ns
T _{PLLCKC_DWE} / T _{PLLCKC_DWE}	Setup and Hold of D write enable	1.25/ 0.15	1.40/ 0.15	1.63/ 0.15	1.43/ 0.00	ns

Notes:

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.

Kintex-7 Device Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

Table 57: Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Near Clock Region)

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>without</i> MMCM/PLL.							
T _{ICKOFF}	Clock-capable clock input and OUTFF <i>without</i> MMCM/PLL (near clock region)	XC7K70T	6.16	7.05	8.34	7.40	ns
		XC7K160T	6.39	7.31	8.61	7.71	ns
		XC7K325T	6.81	7.78	9.16	8.26	ns
		XC7K355T	6.54	7.47	8.78	7.91	ns
		XC7K410T	6.93	7.91	9.29	8.42	ns
		XC7K420T	6.68	7.63	8.95	8.10	ns
		XC7K480T	6.98	7.96	9.35	8.50	ns

Notes:

- Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Table 58: Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Far Clock Region)

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>without</i> MMCM/PLL.							
T _{ICKOFFAR}	Clock-capable clock input and OUTFF <i>without</i> MMCM/PLL (far clock region)	XC7K70T	6.46	7.39	8.74	7.79	ns
		XC7K160T	6.98	7.97	9.41	8.49	ns
		XC7K325T	7.46	8.49	10.01	9.12	ns
		XC7K355T	7.14	8.14	9.58	8.70	ns
		XC7K410T	7.59	8.64	10.16	9.30	ns
		XC7K420T	7.58	8.62	10.15	9.28	ns
		XC7K480T	7.58	8.62	10.15	9.28	ns

Notes:

- Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Table 59: Clock-Capable Clock Input to Output Delay With MMCM

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>with</i> MMCM.							
T _{ICKOFMMCMCC}	Clock-capable clock input and OUTFF <i>with</i> MMCM	XC7K70T	1.25	1.40	1.63	2.64	ns
		XC7K160T	1.24	1.42	1.63	2.65	ns
		XC7K325T	1.25	1.44	1.64	2.67	ns
		XC7K355T	1.23	1.42	1.63	2.65	ns
		XC7K410T	1.25	1.44	1.64	2.67	ns
		XC7K420T	1.25	1.44	1.64	2.67	ns
		XC7K480T	1.25	1.44	1.64	2.67	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Table 60: Clock-Capable Clock Input to Output Delay With PLL

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>with</i> PLL.							
T _{ICKOFPLLCC}	Clock-capable clock input and OUTFF <i>with</i> PLL	XC7K70T	1.41	1.41	1.41	2.09	ns
		XC7K160T	1.42	1.42	1.42	2.13	ns
		XC7K325T	1.41	1.41	1.41	2.13	ns
		XC7K355T	1.39	1.39	1.39	2.11	ns
		XC7K410T	1.42	1.42	1.42	2.13	ns
		XC7K420T	1.39	1.39	1.39	2.13	ns
		XC7K480T	1.39	1.39	1.39	2.13	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is already included in the timing calculation.

Kintex-7 Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

Table 61: Global Clock Input Setup and Hold Without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard. ⁽¹⁾							
T_{PSFD} / T_{PHFD}	Full Delay (Legacy Delay or Default Delay) Global Clock Input and IFF ⁽²⁾ without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks	XC7K70T	3.00/ -0.70	3.00/ -0.69	3.00/ -0.46	3.20/ -0.37	ns
		XC7K160T	3.38/ -0.74	3.38/ -0.73	3.38/ -0.50	3.68/ -0.38	ns
		XC7K325T	3.17/ -0.27	3.17/ -0.21	3.17/ 0.11	2.63/ 0.23	ns
		XC7K355T	3.49/ -0.78	3.49/ -0.77	3.49/ -0.56	2.83/ 0.00	ns
		XC7K410T	3.71/ -0.70	3.71/ -0.69	3.71/ -0.45	3.41/ -0.07	ns
		XC7K420T	3.72/ -0.72	3.72/ -0.71	3.72/ -0.46	3.43/ -0.08	ns
		XC7K480T	3.64/ -0.72	3.64/ -0.71	3.64/ -0.46	3.26/ -0.08	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch
3. A Zero "0" Hold Time listing indicates no hold time or a negative hold time.

Table 62: Clock-Capable Clock Input Setup and Hold With MMCM

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard. ⁽¹⁾							
T _{PSMMCMCC} / T _{PHMMCMCC}	No Delay clock-capable clock input and IFF ⁽²⁾ with MMCM	XC7K70T	2.41/ -0.21	2.86/ -0.21	3.14/ -0.21	2.23/ -0.32	ns
		XC7K160T	2.53/ -0.22	3.00/ -0.22	3.30/ -0.22	2.41/ -0.28	ns
		XC7K325T	2.66/ -0.22	3.13/ -0.22	3.45/ -0.22	2.58/ -0.26	ns
		XC7K355T	2.53/ -0.24	2.99/ -0.24	3.28/ -0.24	2.19/ -0.39	ns
		XC7K410T	2.64/ -0.21	3.12/ -0.21	3.43/ -0.21	2.56/ -0.28	ns
		XC7K420T	2.64/ -0.23	3.12/ -0.23	3.43/ -0.23	2.36/ -0.38	ns
		XC7K480T	2.53/ -0.23	2.99/ -0.23	3.28/ -0.23	2.19/ -0.38	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 63: Clock-Capable Clock Input Setup and Hold With PLL

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
Input Setup and Hold Time Relative to Clock-Capable Clock Input Signal for SSTL15 Standard. ⁽¹⁾							
T _{PSPLLCC} / T _{PHPLLCC}	No Delay clock-capable clock input and IFF ⁽²⁾ with PLL	XC7K70T	2.82/ -0.05	3.33/ -0.05	3.73/ -0.05	2.55/ -0.73	ns
		XC7K160T	2.95/ -0.05	3.46/ -0.05	3.90/ -0.05	2.73/ -0.72	ns
		XC7K325T	3.07/ -0.05	3.60/ -0.05	4.05/ -0.05	2.90/ -0.72	ns
		XC7K355T	2.94/ -0.07	3.45/ -0.07	3.88/ -0.07	2.52/ -0.79	ns
		XC7K410T	3.06/ -0.04	3.58/ -0.04	4.03/ -0.04	2.88/ -0.72	ns
		XC7K420T	3.06/ -0.06	3.58/ -0.06	4.03/ -0.06	2.68/ -0.78	ns
		XC7K480T	2.94/ -0.06	3.45/ -0.06	3.88/ -0.06	2.52/ -0.78	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Clock Switching Characteristics

The parameters in this section provide the necessary values for calculating timing budgets for Kintex-7 FPGA clock transmitter and receiver data-valid windows.

Table 64: Duty Cycle Distortion and Clock-Tree Skew

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
T_{DCD_CLK}	Global Clock Tree Duty Cycle Distortion ⁽¹⁾	All	0.20	0.20	0.20	0.25	ns
$T_{CKSKREW}$	Global Clock Tree Skew ⁽²⁾	XC7K70T	0.16	0.17	0.19	0.21	ns
		XC7K160T	0.30	0.33	0.35	0.40	ns
		XC7K325T	0.44	0.48	0.51	0.59	ns
		XC7K355T	0.30	0.33	0.35	0.40	ns
		XC7K410T	0.44	0.48	0.51	0.59	ns
		XC7K420T	0.44	0.48	0.51	0.59	ns
		XC7K480T	0.30	0.33	0.35	0.40	ns
T_{DCD_BUFIO}	I/O clock tree duty cycle distortion	All	0.08	0.08	0.08	0.08	ns
$T_{BUFIOSKEW}$	I/O clock tree skew across one clock region	All	0.02	0.02	0.02	0.03	ns
T_{DCD_BUFR}	Regional clock tree duty cycle distortion	All	0.15	0.15	0.15	0.15	ns

Notes:

1. These parameters represent the worst-case duty cycle distortion observable at the I/O flip flops. For all I/O standards, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
2. The $T_{CKSKREW}$ value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.

Table 65: Package Skew

Symbol	Description	Device	Package	Value	Units
T _{PKGSKEW}	Package Skew ⁽¹⁾	XC7K70T	FBG484		ps
			FBG676		ps
		XC7K160T	FBG484		ps
			FBG676		ps
			FFG676		ps
		XC7K325T	FBG676	148	ps
			FFG676	160	ps
			FBG900	165	ps
			FFG900	168	ps
		XC7K355T	FFG901		ps
		XC7K410T	FBG676	171	ps
			FFG676	172	ps
			FBG900	152	ps
			FFG900	148	ps
		XC7K420T	FFG901	152	ps
			FFG1156	139	ps
XC7K480T	FFG901	152	ps		
	FFG1156	139	ps		

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest flight time to longest flight time from Pad to Ball (7.0 ps per mm).
2. Package trace length information is available for these device/package combinations. This information can be used to deskew the package.

Table 66: Sample Window

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T _{SAMP}	Sampling Error at Receiver Pins ⁽¹⁾	0.51	0.56	0.61	0.56	ns
T _{SAMP_BUFIO}	Sampling Error at Receiver Pins using BUFIO ⁽²⁾	0.30	0.35	0.40	0.35	ns

Notes:

1. This parameter indicates the total sampling error of the Kintex-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
 - CLK0 MMCM jitter
 - MMCM accuracy (phase offset)
 - MMCM phase shift resolution
 These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of the Kintex-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IDELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Table 67: Pin-to-Pin Setup/Hold and Clock-to-Out

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO						
T _{PSCS} /T _{PHCS}	Setup/Hold of I/O clock for HR I/O banks	-0.33/ 1.44	-0.33/ 1.59	-0.33/ 1.97	-0.53/ 1.78	ns
	Setup/Hold of I/O clock for HP I/O banks	-0.33/ 1.42	-0.33/ 1.57	-0.33/ 1.95	-0.43/ 1.93	ns
Pin-to-Pin Clock-to-Out Using BUFIO						
T _{ICKOFCS}	Clock-to-Out of I/O clock for HR I/O banks	6.11	7.02	8.26	7.57	ns
	Clock-to-Out of I/O clock for HP I/O banks	5.45	6.26	7.36	7.31	ns

Revision History

The following table shows the revision history for this document:

Date	Version	Description
03/01/11	1.0	Initial Xilinx release.
04/01/11	1.1	Added the XC7K355T, XC7K420T, and XC7K480T devices throughout data sheet. Added the extended temperature range discussion to page 1 . Updated V _{CCAUX_IO} in Table 2 . Edits to clarify Power-On/Off Power Supply Sequencing power sequencing discussion. Added I _{CCAUX_IO} and I _{CBBRAM} to Table 4 and Table 5 . Updated MMCM_F _{INDUTY} and added F _{INJITTER} , T _{OUTJITTER} , T _{EXTFDVAR} , and Note 3 to Table 55 . Removed the SBG324 package from Table 65 . Updated the Notice of Disclaimer .
10/04/11	1.2	Replaced -1L with -2L throughout this data sheet. Updated Min/Max values and removed Note 5 from Table 2 . Clarified Power-On/Off Power Supply Sequencing power sequencing discussion including adding T _{VCCO2VCCAUX} to Table 6 . Updated V _{ICM} in Table 10 and Table 11 . Added Note 1 to table 12. Updated Table 12 including adding Note 1 . Added Table 13 . Revised the reference clock maximum frequency (F _{GCLK}) in Table 19 . Added Table 20 . Added LVTTTL and removed SSTL135_II and SSTL15_II specifications from Table 36 . Removed HSTL_III from Table 37 . Removed the <i>I/O Standard Adjustment Measurement Methodology</i> section. Use IBIS for more accurate information and measurements. Updated T _{IDELAYPAT_JIT} in Table 43 . Added T _{AS} /T _{AH} to Table 45 . Added T _{RDCK_DI_WF_NC} /T _{RCKD_DI_WF_NC} and T _{RDCK_DI_RF} /T _{RCKD_DI_RF} to Table 48 . Completely updated Table 50 . Updated the Switching Characteristics in Table 36 , Table 37 , Table 38 , Table 39 , Table 40 , Table 41 , Table 43 through Table 55 , Table 57 through Table 64 , and Table 67 .

Date	Version	Description
11/03/11	1.3	Revised the V_{OCM} specification in Table 10 . Updated the Switching Characteristics based upon the ISE 13.3 v1.02 speed specification throughout document including Table 36 and Table 37 . Added $MMCM_T_{FBDELAY}$ while adding $MMCM_$ to the symbol names of a few specifications in Table 55 and PLL to the symbol names in Table 56 . In Table 57 through Table 63 , updated the pin-to-pin descriptions with the SSTL15 standard. Updated units in Table 66 .
02/13/12	1.4	<p>Updated summary description on page 1. In Table 2, revised V_{CCO} for the 3.3V HR I/O banks and updated T_j. Added typical values to Table 3. Updated the notes in Table 4. Added MGTAVCC, MGTAVTT, and MGTVCCAUX power supply ramp times to Table 6. Rearranged Table 7, added Mobile_DDR, HSTL_I_18, HSTL_II_18, HSUL_12, SSTL135_R, SSTL15_R, and SSTL12 and removed DIFF_SSTL135, DIFF_SSTL18_I, DIFF_SSTL18_II, DIFF_HSTL_I, and DIFF_HSTL_II. Added Table 8 and Table 9. Revised the specifications in Table 10 and Table 11. Updated the eFUSE Programming Conditions section and removed the endurance table. Added the I/O FIFO Switching Characteristics table. Revised I_{CCADC} and updated Note 1 in Table 30. Revised DDR LVDS transmitter data width in Table 31. Updated the Switching Characteristics based upon the ISE 13.4 v1.03 speed specification throughout document. Removed notes from Table 45 as they are no longer applicable. Updated specifications in Table 50. Updated Note 1 in Table 64.</p> <p>In the GTX Transceiver Specifications section: Revised V_{IN}, and added I_{DCIN} and I_{DCOUT} to Table 15. Added Note 3 to Table 17. In Table 19, revised F_{GCLK}, removed T_{PHASE}, and added T_{DLOCK}. Revised specifications and added Note 2 to Table 20. Added Table 21 and Table 22 along with GTX Transceiver Protocol Jitter Parameters in Table 23 through Table 28.</p>

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