Xilinx Products, Solutions and Technology for ADAS/AD

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Xilinx
Director: Automotive Solutions & Architects

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Xilinx Product Evolution in Automotive

2008	2010	2012	2014	2016	2018	2020	2022
FPGA		HW Programmable SoC		HW Programmable MPSoC		ADAPTIVE COMPUTE ACCELERATION PLATFORM	
SPARTAN 6		ZYNQ Z-7000		ZYNQ UltraSCALE+		XILINX VERSAL	
1 Mpixel Camera Warning (only)		2 Mpixel Camera Warning & Mitigation		4 Mpixel Camera Broader Protection & Control		8 Mpixel Camera Autonomous Drive/Park	
							
Bird's Eye View		3D Surround View		Dynamic 3D Surround		Next Gen 3D Surround w/ AI	

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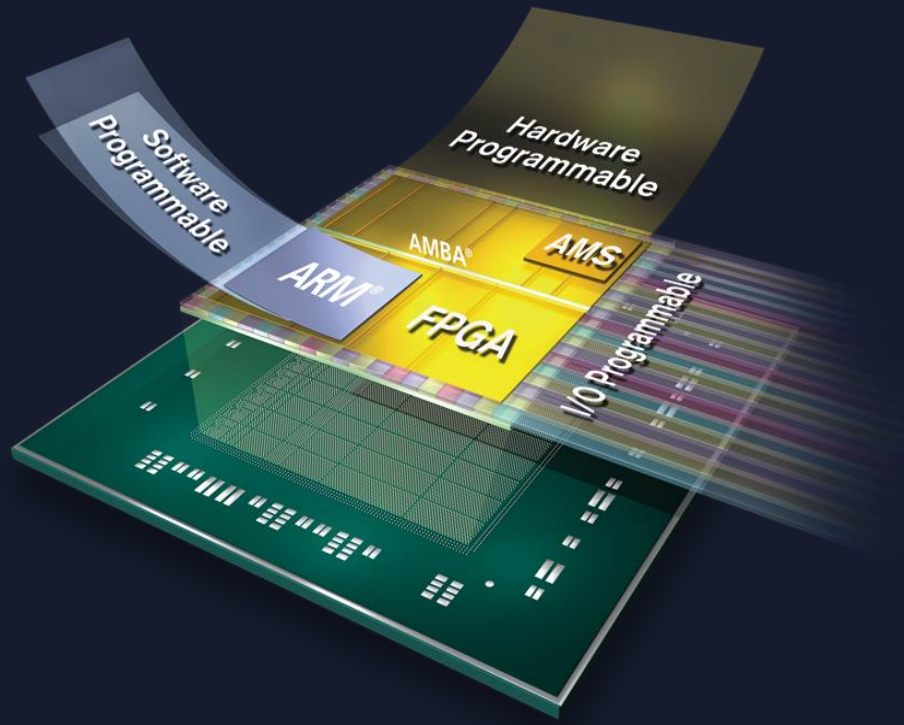
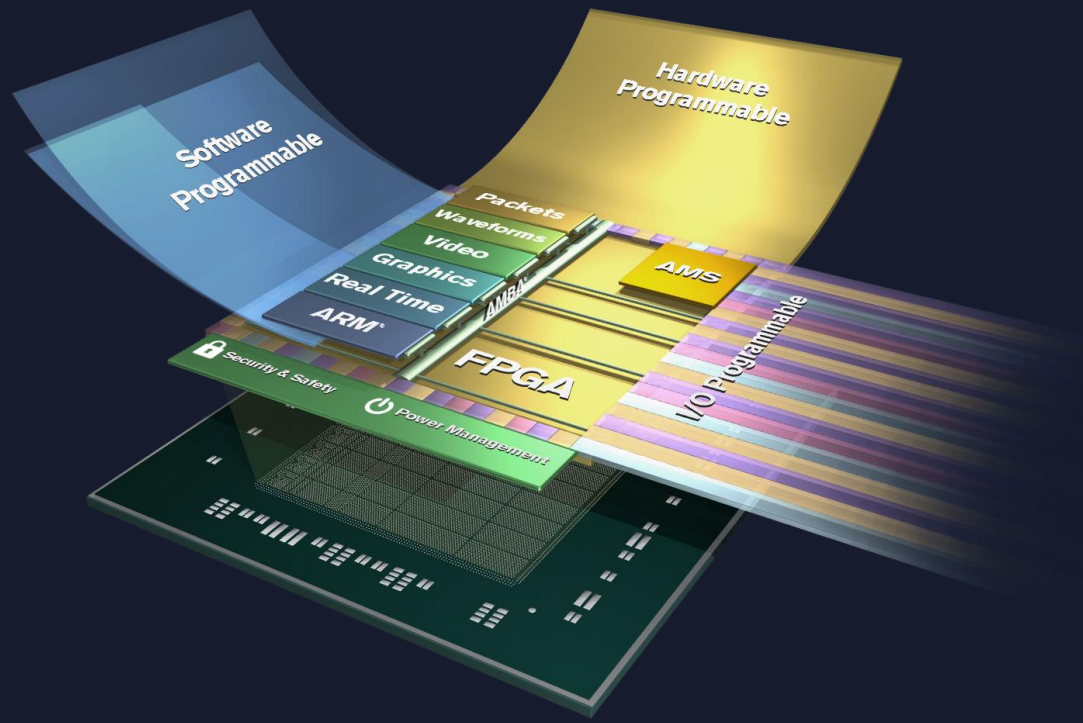
Xilinx All Programmable SoC and MPSoC

A Game Changing Technology in Automotive



ZYNQ | 28nm



ZYNQ UltraSCALE+ | 16FF+

SoC: System on Chip
MPSoC: Multi-Processor System on Chip

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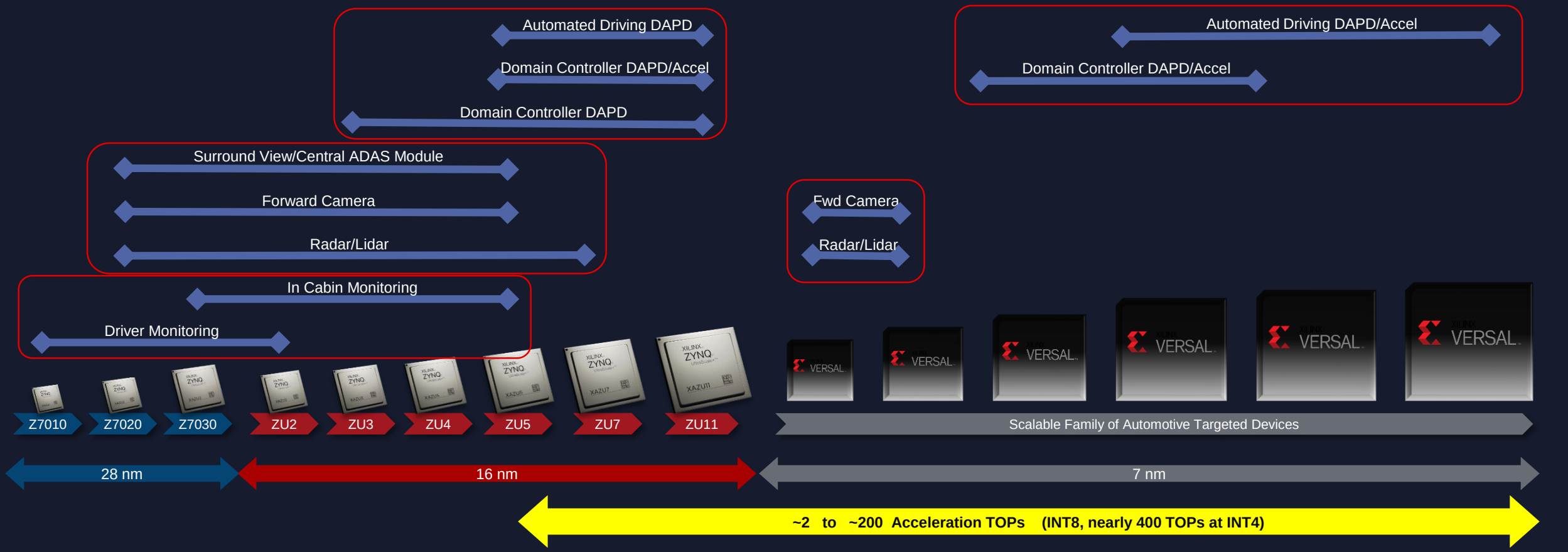
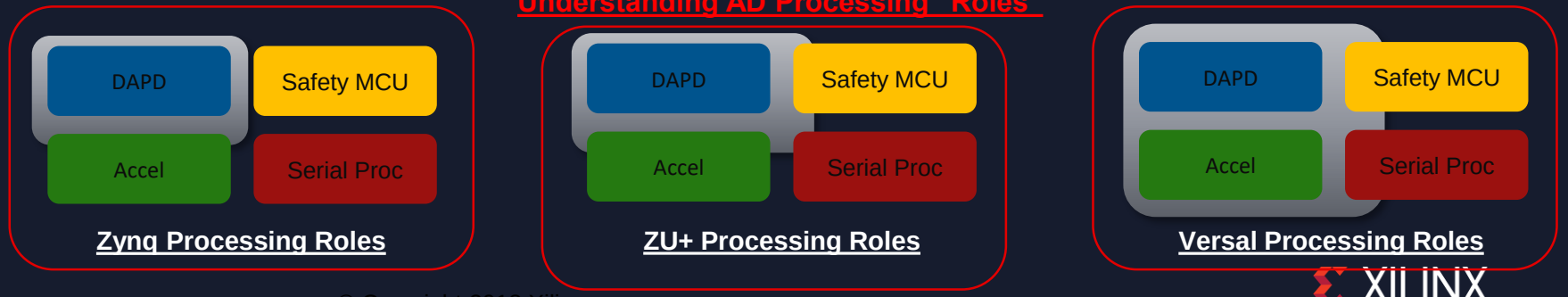
Xilinx Automotive SoC & ACAP Applications



Understanding AD Processing "Roles"

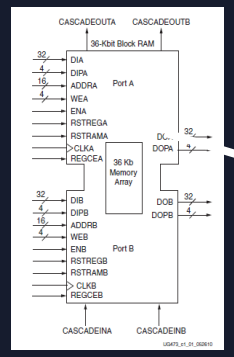


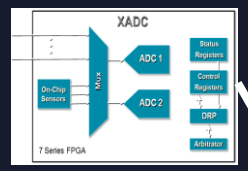
DAPD = Data Aggregation, Pre-Processing & Distribution

Accel = Compute Acceleration (e.g. CNN Processing)

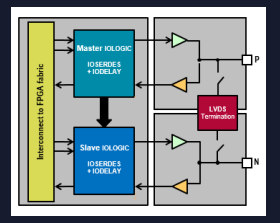
Field Programmable Gate Array Based SoC's

Block/Ultra RAMs



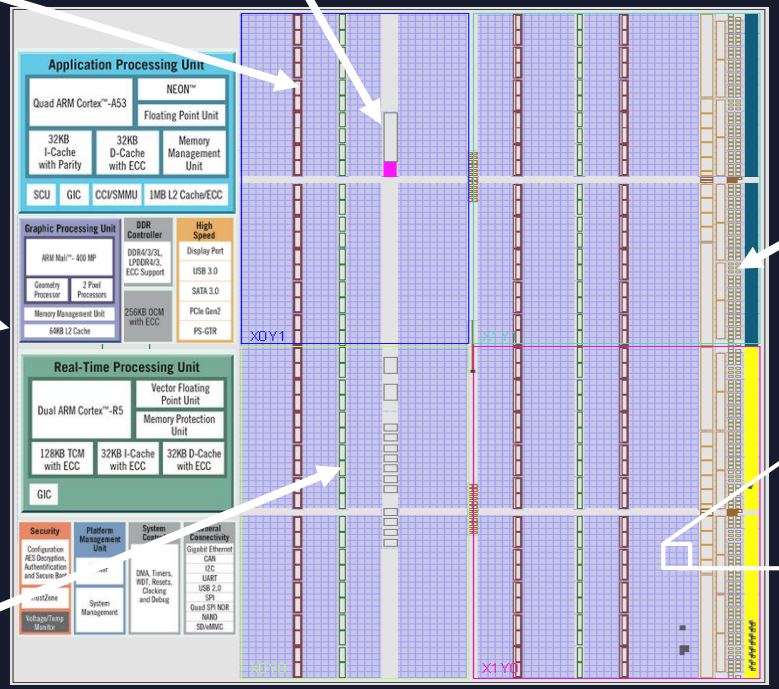


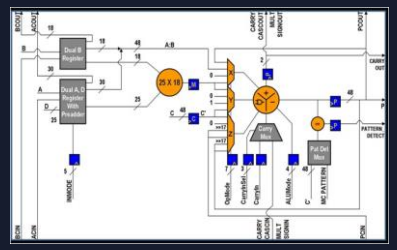
SysMon / ADCs



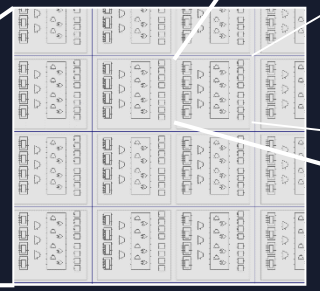
I/O Blocks

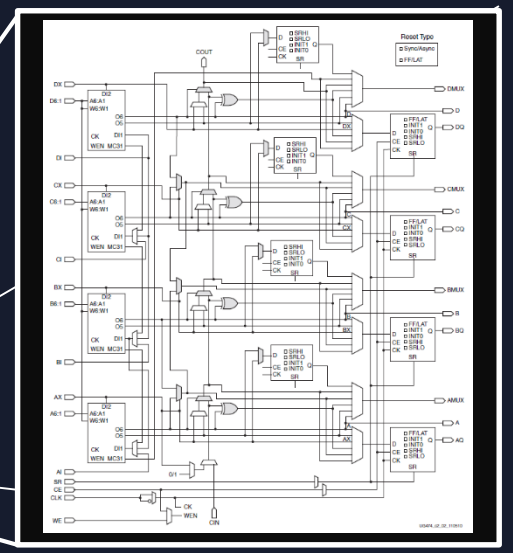
Processing System





DSP Slices





Configurable Logic Blocks

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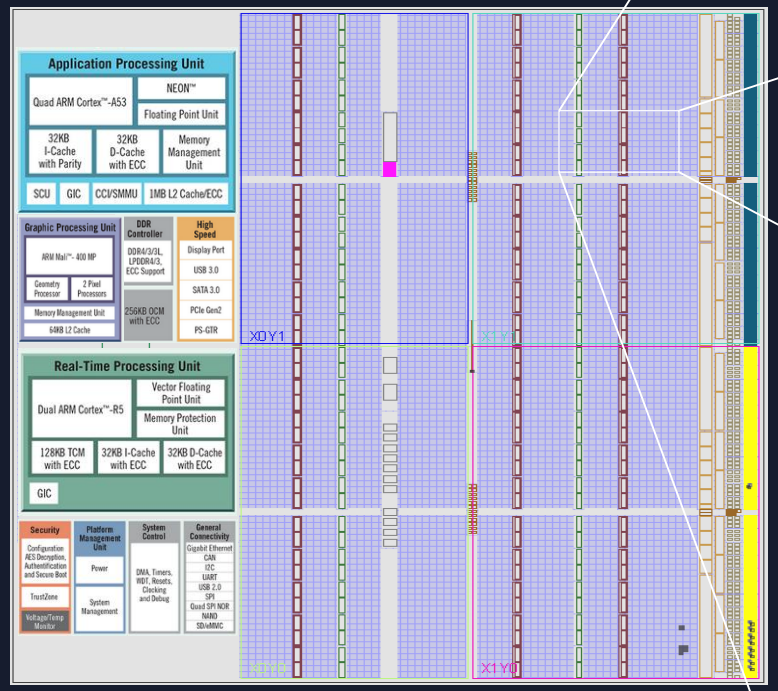
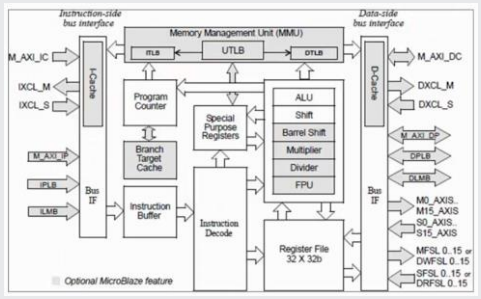
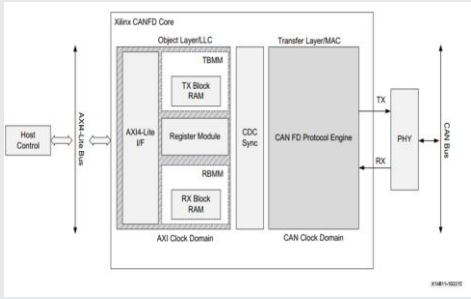
Field Programmable Gate Array Based SoC's

FPGA Fabric = Programmable Logic

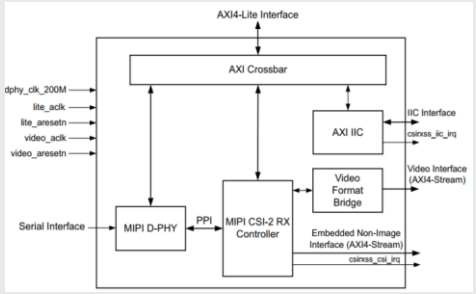




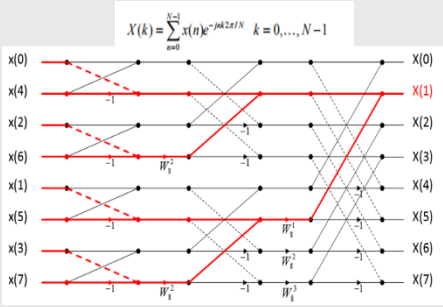
› **Common Processor Peripherals** (e.g. CAN / CAN-FD)



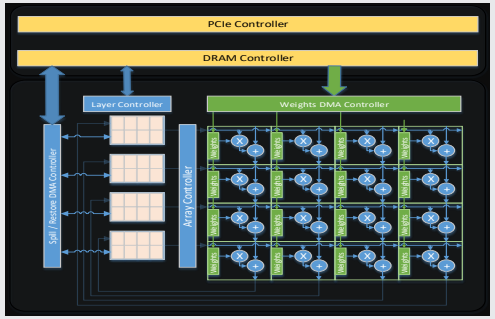
> **MicroBlaze 32-bit Soft Processor**



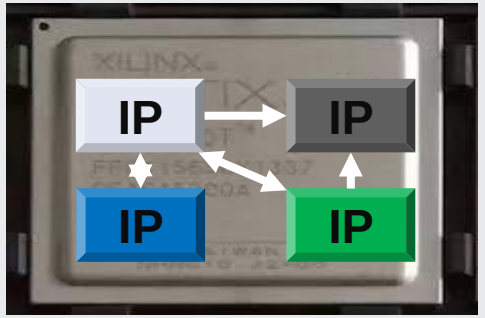
› **Application Focused Connectivity** (e.g. MIPI CSI-2 Controller and D-PHY)



› **Highly Parallelized and Customized DSP Acceleration** (e.g. FFT)



› **Inference DNN Processing Engines**



› **Unique, Differentiating User-Defined Functions or Pipelines of Functions**

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Functional Partitioning for Zynq UltraScale+

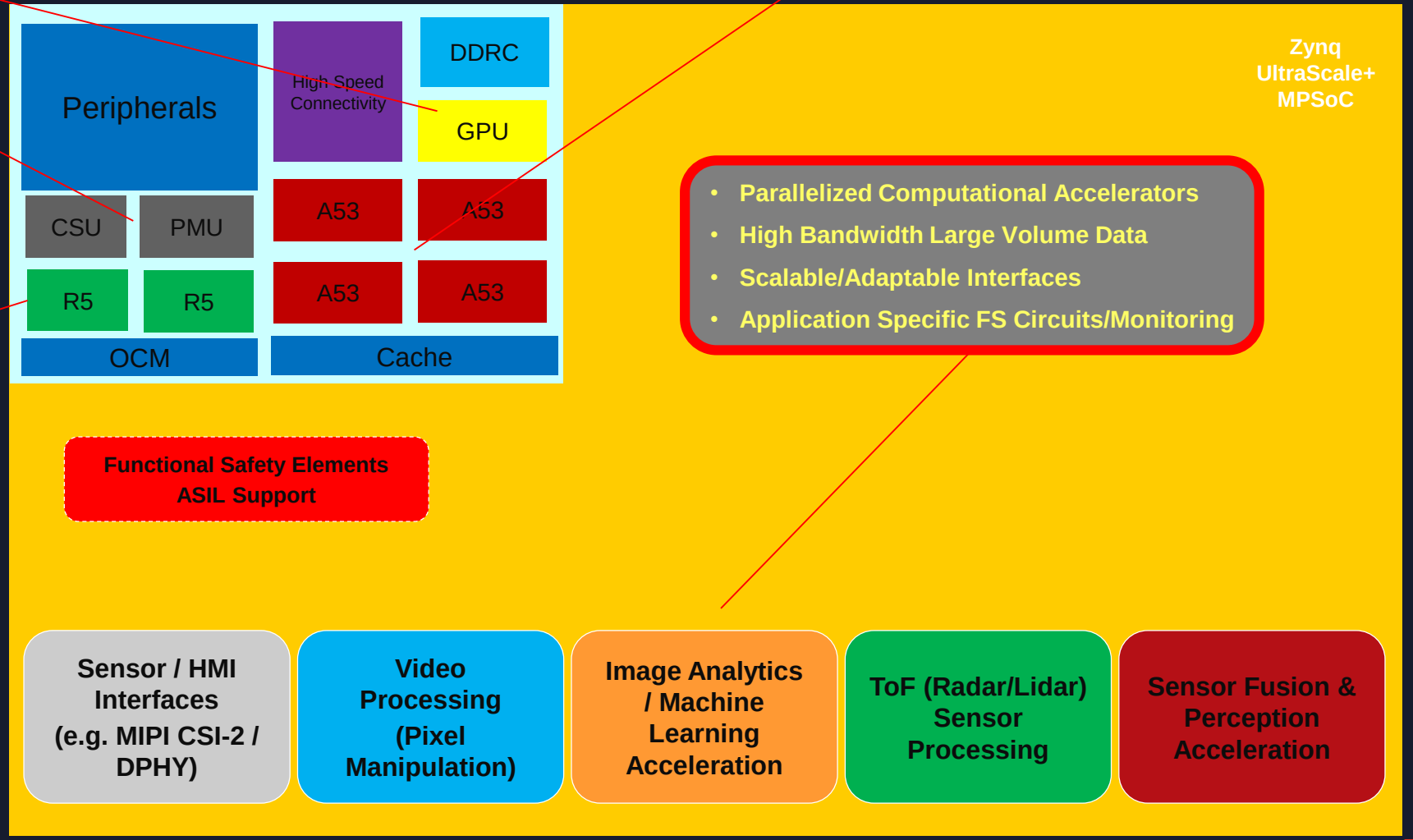
A Heterogenous Processing Platform

- Feature Application SW
- Algorithm Configuration & Control
- Object Tracking
- Environment Assessment
- Feature State Control

- HMI Graphic Overlay

- Configuration Security Unit
- Platform Management Unit

- System Control Decisions
- Diagnostics /FuncSafety
- Vehicle Comms



- Parallelized Computational Accelerators
- High Bandwidth Large Volume Data
- Scalable/Adaptable Interfaces
- Application Specific FS Circuits/Monitoring

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Versal Architecture Overview

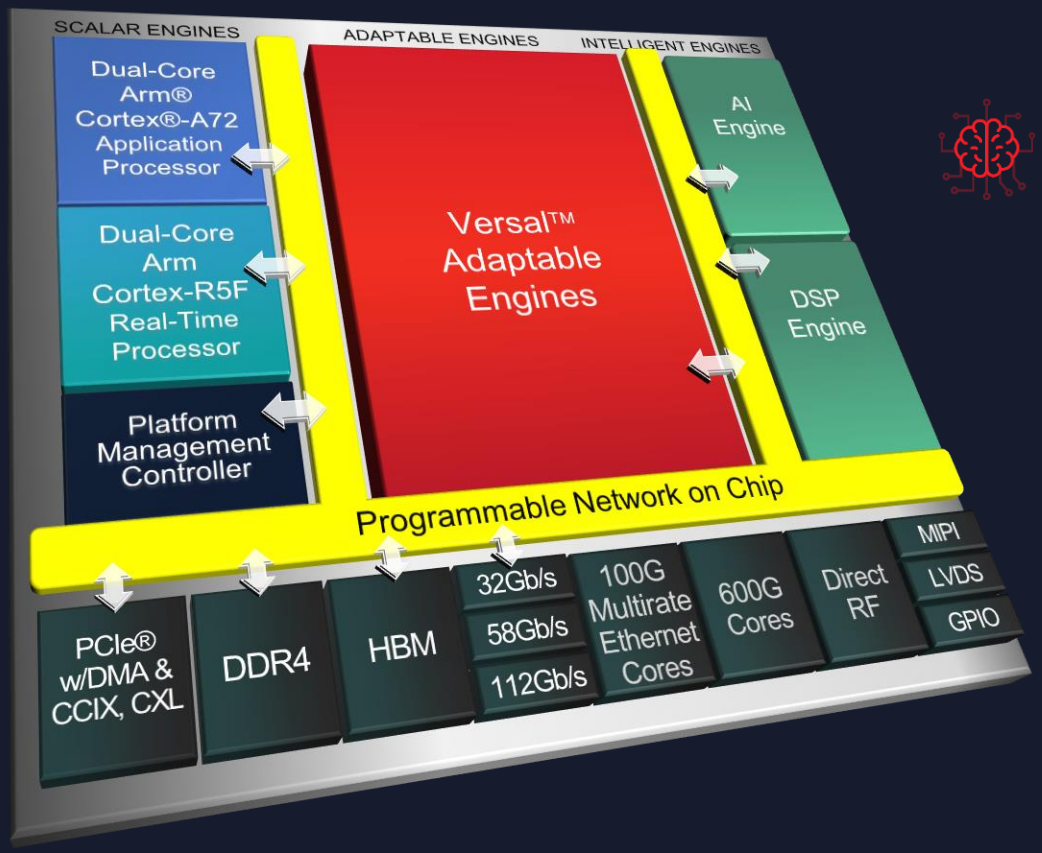
Adaptable Engines
- 2X compute density
- Voltage scaling for perf/watt

Scalar Engines
- Platform Control
- Embedded Edge Compute

PCIe Gen4/5 & CCIX
- 2X PCIe & DMA bandwidth
- Cache-coherency

DDR4 Memory
- 3200-DDR4, 4266-LPDDR4
- 2X bandwidth/pin

Transceiver Leadership
- Broad range, 1G →112G
- 58G in mainstream devices
- (32G in XA)



Intelligent Engines (DSP)
- AI Compute
- Diverse DSP Workloads

Programmable NoC
- Guaranteed Bandwidth
- Enables SW Programmability

Programmable I/O
- Any interface or sensor
- Includes 3.2Gb/s MIPI

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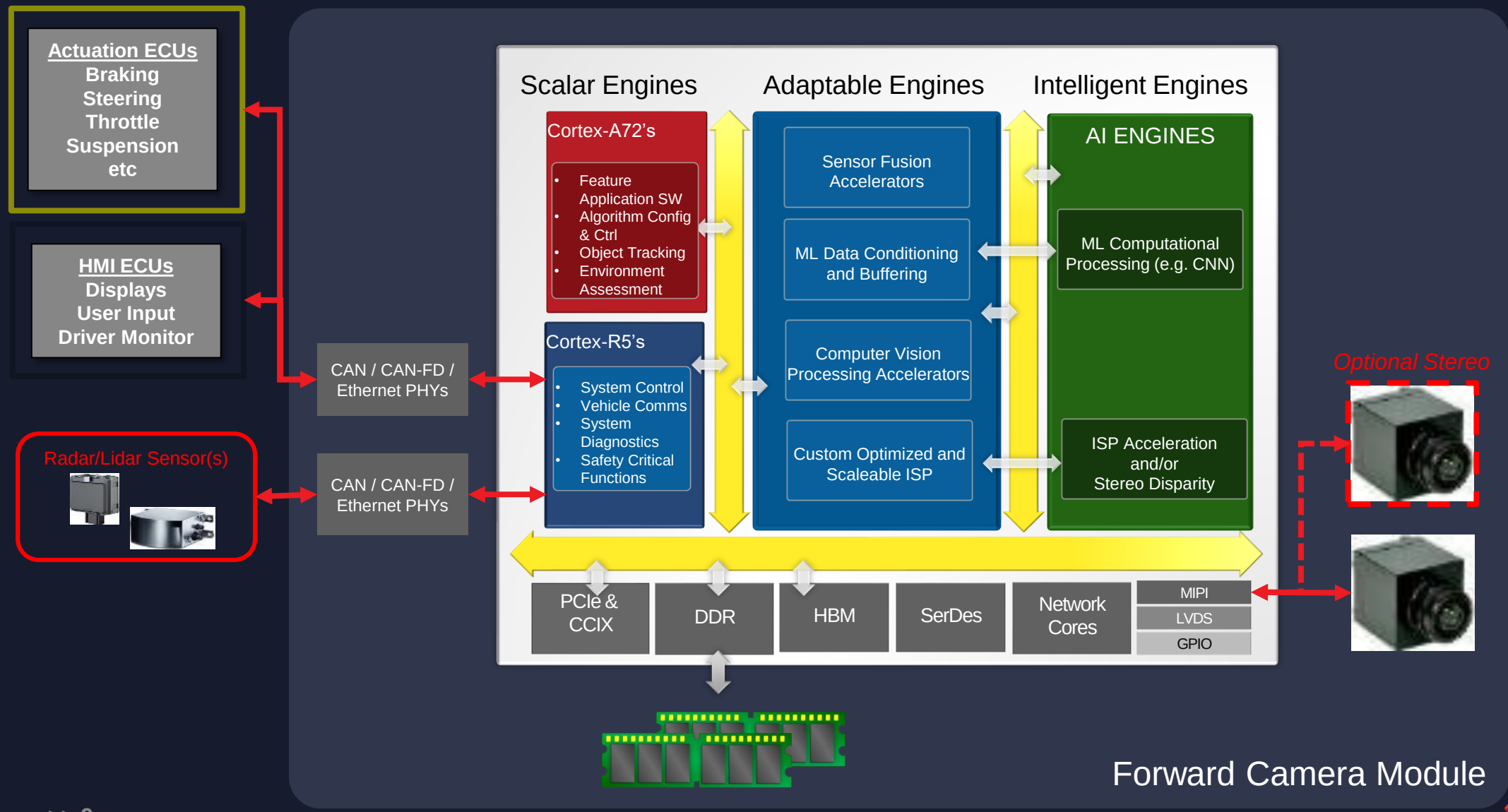
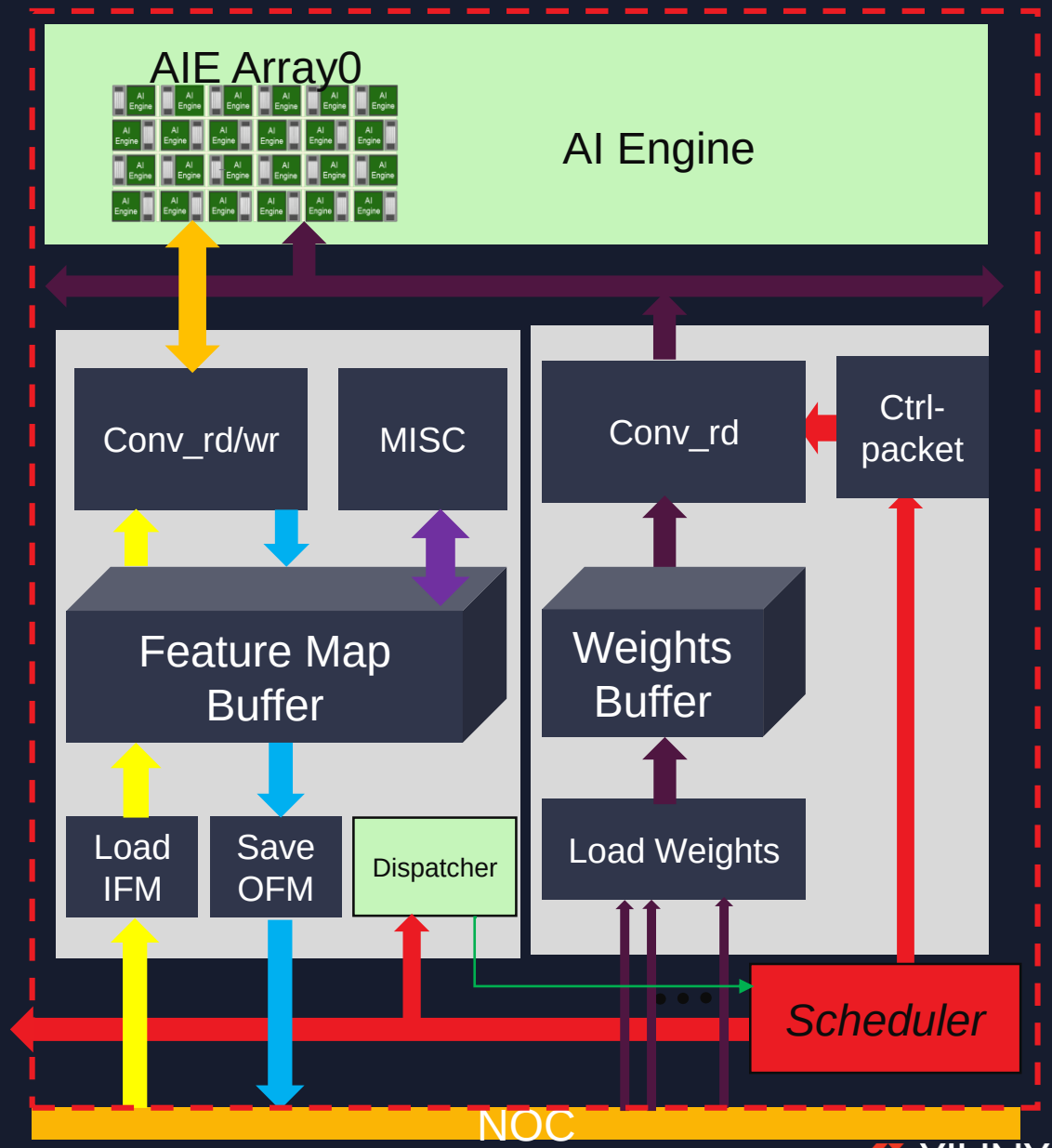
Forward-Looking Camera Partitioning Example



ML Processing on Versal

DPU Architecture Design

- **Target: Configurable/Scalable DPU**
  - **DPU = Deep-learning Processing Unit**
  - **A powerful combination of PL and AIE resources to realize optimized ML Processing**
- **AIE:** Conv engine
- **PL:** Depthwise Conv, Elementwise, Pooling, softmax and Instruction scheduler
- **Instruction:** Control the data flow between AIE and PL. Control different engines in MISC.



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Xilinx Solutions Slides

From horizontal IP to partner application specific solutions

Xilinx Radar/Lidar ML Processing

Pointpillars on Lidar Data Example

Demo specification

- Model: Pointpillars
- Framework: Pytorch
- Dataset: Kitti, 64-channel, 1~2Mpoints/sec
- 25fps (40ms latency), 1x DPU B4096 @ 300MHz on ZCU102
- General access in Vitis AI 1.3

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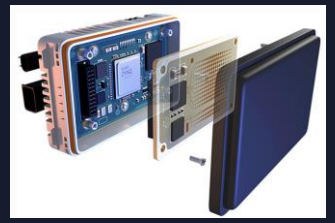
ZU+ -based 4D Radar Processor Concept

Hardware Accelerated Performance Optimized to RF Modulation and Control Strategies



DDR

Sensor Application Code

Comms, Diagnostics, Watchdog Code

Beam Element/Motor Control Integration

Processing System

- High Speed: Display Port, USB 3.0, SATA 3.0, PCIe Gen2, PS-GTR
- Application Processing Unit: Quad ARM Cortex™-A53, NEON™, Floating Point Unit, 32KB I-Cache with Parity, 32KB D-Cache with ECC, Memory Management Unit, SCU, GIC, CCI/SMMU, 1MB L2 Cache/ECC
- Graphic Processing Unit: ARM Mali™- 400 MP, Geometry Processor, 2 Pixel Processors, Memory Management Unit, 64KB L2 Cache
- DDR Controller: DDR4/3/3L, LPDDR4/3, ECC Support
- 256KB OCM with ECC
- General Connectivity: Gigabit Ethernet, CAN, I2C, UART, USB 2.0, SPI, Quad SPI NOR, NAND, SD/eMMC
- Real-Time Processing Unit: Dual ARM Cortex™-R5, Vector Floating Point Unit, Memory Protection Unit, 128KB TCM with ECC, 32KB I-Cache with ECC, 32KB D-Cache with ECC, GIC
- Security: Configuration AES Decryption, Authentification and Secure Boot, TrustZone, Voltage/Temp Monitor
- Platform Management Unit: Power, System Management
- System Control: DMA, Timers, WDT, Resets, Clocking and Debug

Programmable Logic:

System Gates, DSP, RAM

- Functional Safety Support (e.g. Cross Monitoring, Voting, Watchdog)
- RF/Sensor Control Logic/State Machine
- RF/Control Components
- Object Detection Accelerator
- Object Tracking Accelerator
- Doppler FFT

Frame Based Processing:
Pulse Integration, Detection, Range Rate, & Tracking

- Multi Channel Data Capture
- FFT Input Conditioning & Buffering
- Complex Streaming FFT
- FFT Output Conditioning & Buffering

Pulsed Based Range Processing::Streaming data from multiple antenna elements

- Digital Beamforming

Azimuth/Elevation Processing:
Phase Differencing Between Elements

RF AFE

High Speed Multi-Channel A/D Converters

MIPI

e.g. 16 receive channels

PROTECTED. CUSTOMIZED. DIFFERENTIATING, AND PRODUCT SPECIFIC IP OPPORTUNITIES

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Viewable System Processing

- From simple rear view camera
  to mirror enhancement and replacement
  to 3D surround view with flying camera
- Image Warping, Stitching (Panoramic, Bowl, other), and View Transformation in a scalable product family to cost effectively meet sensor and system performance needs
- Full development platform available from Xilinx Ecosystem Partner Xylon

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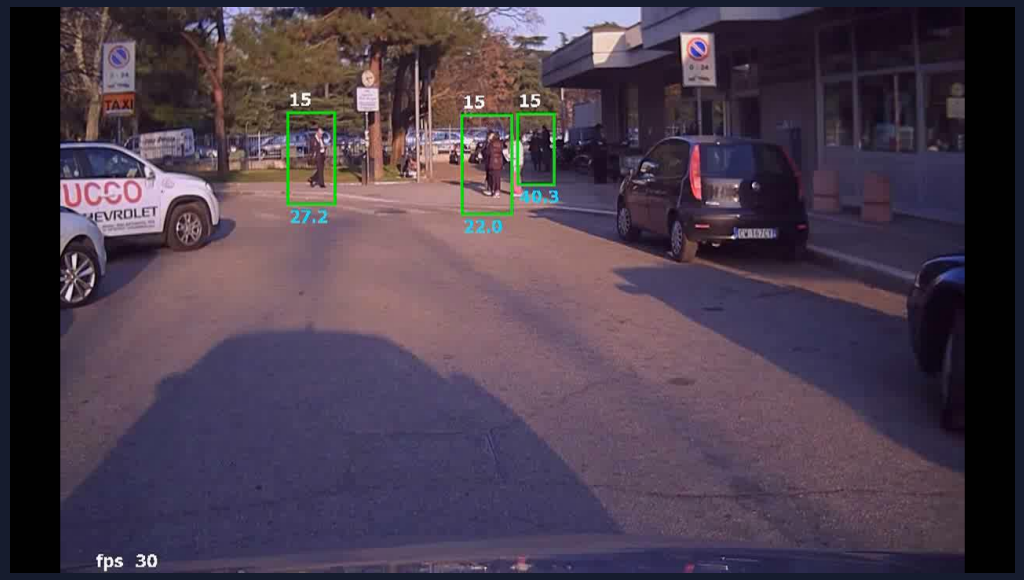
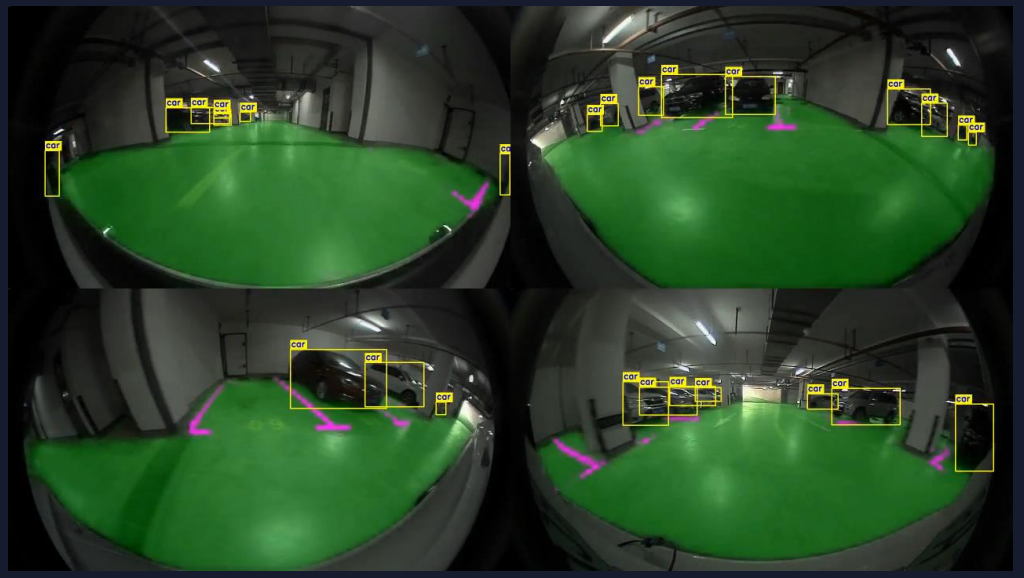
Vision Analytics Processing

- From traditional machine vision to the latest and innovative ML vision processing
- A new breed of Xilinx Ecosystem Partner





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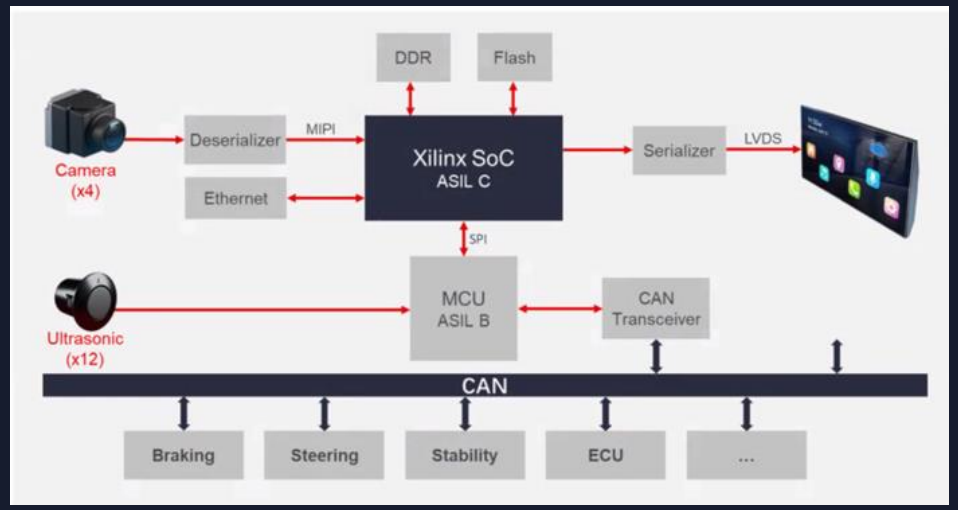
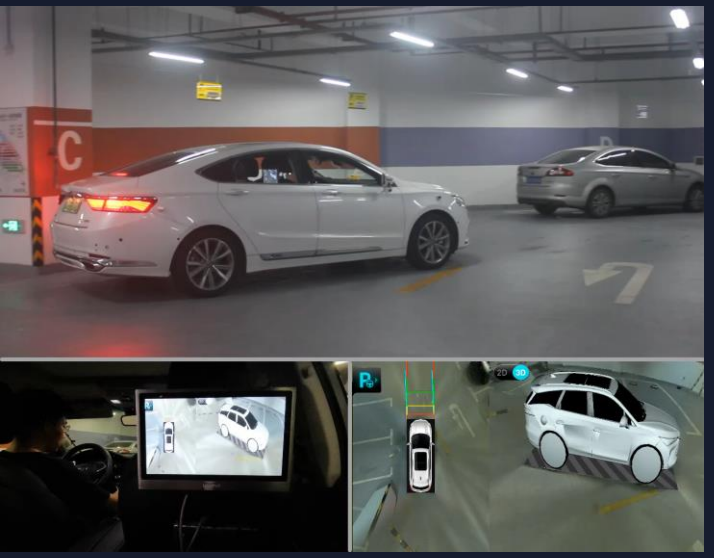
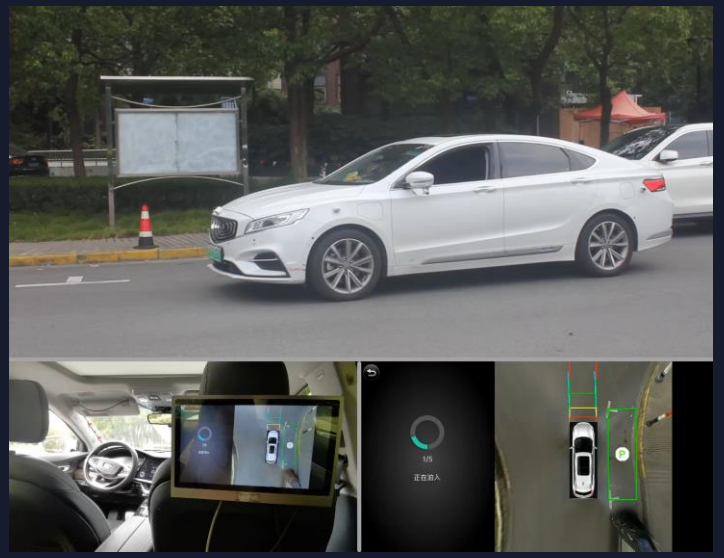
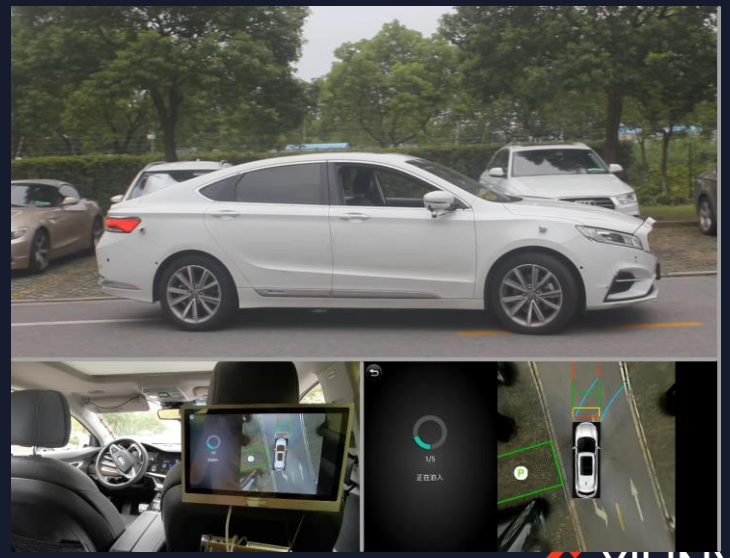
Automated Parking Functionality as Foundation for Domain Controller and other AD initiatives

- **Combining Surround View, ML Processing and Vehicle Control into an automated parking feature**









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Some Xilinx Sourced Relevant IP

- Connectivity
  - MIPI CSI, MIPI DSI, HDMI, Display Port
  - Ethernet TSN, SLVS
- Video Processing
  - Mixer, Scaler, Framebuffer, Video Controller
  - ISP – DPC, Demosaic, Gamma Correction, AWB/AE, HDR, Color Correction, Noise Reduction, etc.
  - Transformation, Image Warping and Stitching
- Image Processing
  - OpenCV Libraries – e.g. Harris Corner, Optical Flow, Stereo Disparity, , HoG/SVM, Hough Transform
- General
  - Windowing, FFT, Kalman Filter, SVD, FIR Filter, etc.

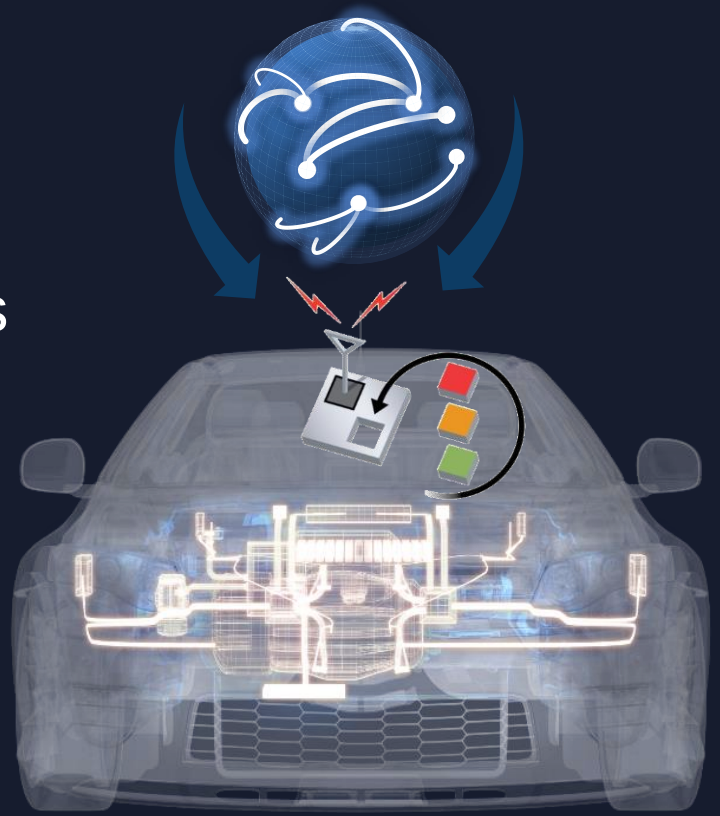
Xilinx Unique Technology Advantages

OTA HW
Dynamic Function Exchange
Functional Safety

Over-the-Air Silicon Updates (OTA)

- Over-The-Air update to enable modifications for Software AND Hardware
  - Evolve neural network implementations over time
  - Add new features or update mission critical functions
  - Future proof for emerging security threats
  - Update safety algorithms
  - Perform remediation or corrective action

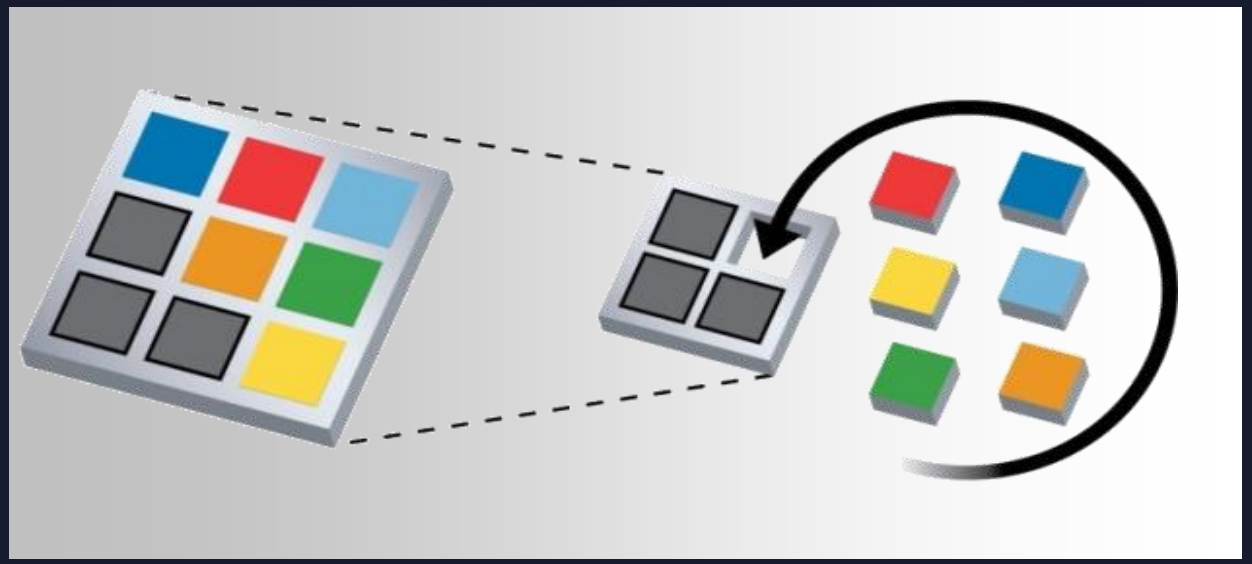
Upgrade Hardware
of Deployed Systems



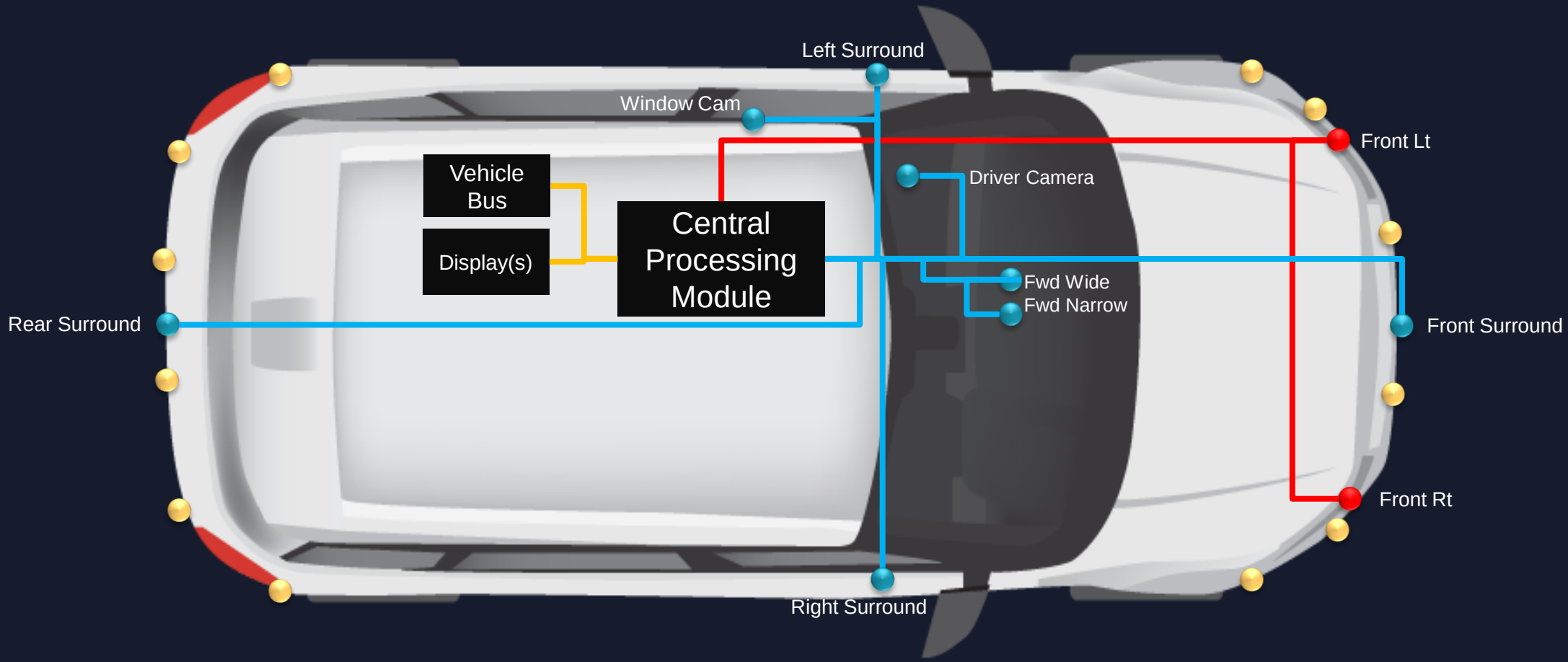
Dynamic Function eXchange (DFX)
Efficient, Low Latency Exchange of Functions

- Leverages the ability to reprogram portions of Xilinx Programmable Logic (PL) fabric while the remainder of the fabric remains fully functional

- Result is “silicon re-use” for uniquely efficient, cost-effective implementation of mutually exclusive applications



Example Multi-Feature Sensor Configuration



RADAR/LIDAR Interface

Camera Interface

Vehicle/Other Interfaces

Cameras (8)

Radar/Lidar (2)

Ultrasonics (12)

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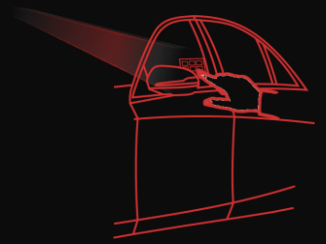
Mutually Exclusive Feature Bundles

Pre-Drive Security

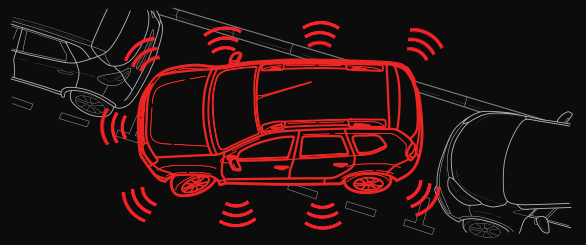


Keyless Entry

Vehicle Security

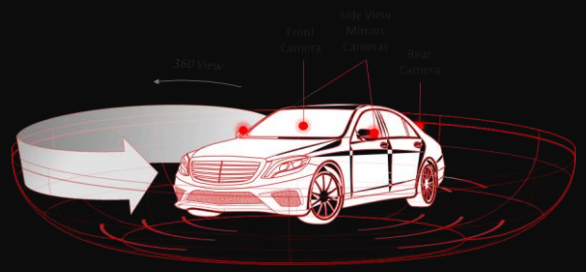
Biometric Identification

Low-Speed/Parking



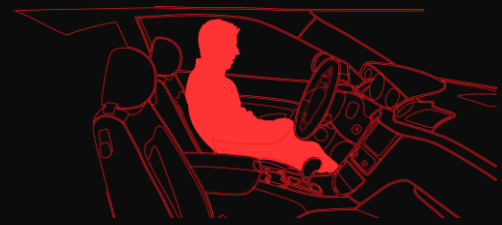
Automated Park Assist

V



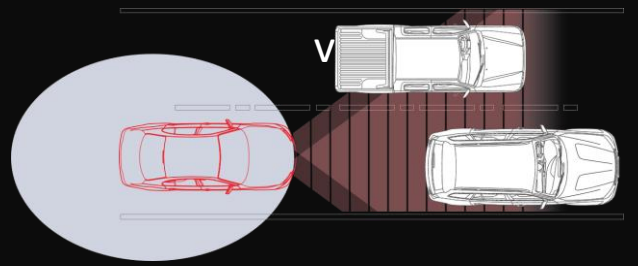
360 Degree Surround View

Highway Driving



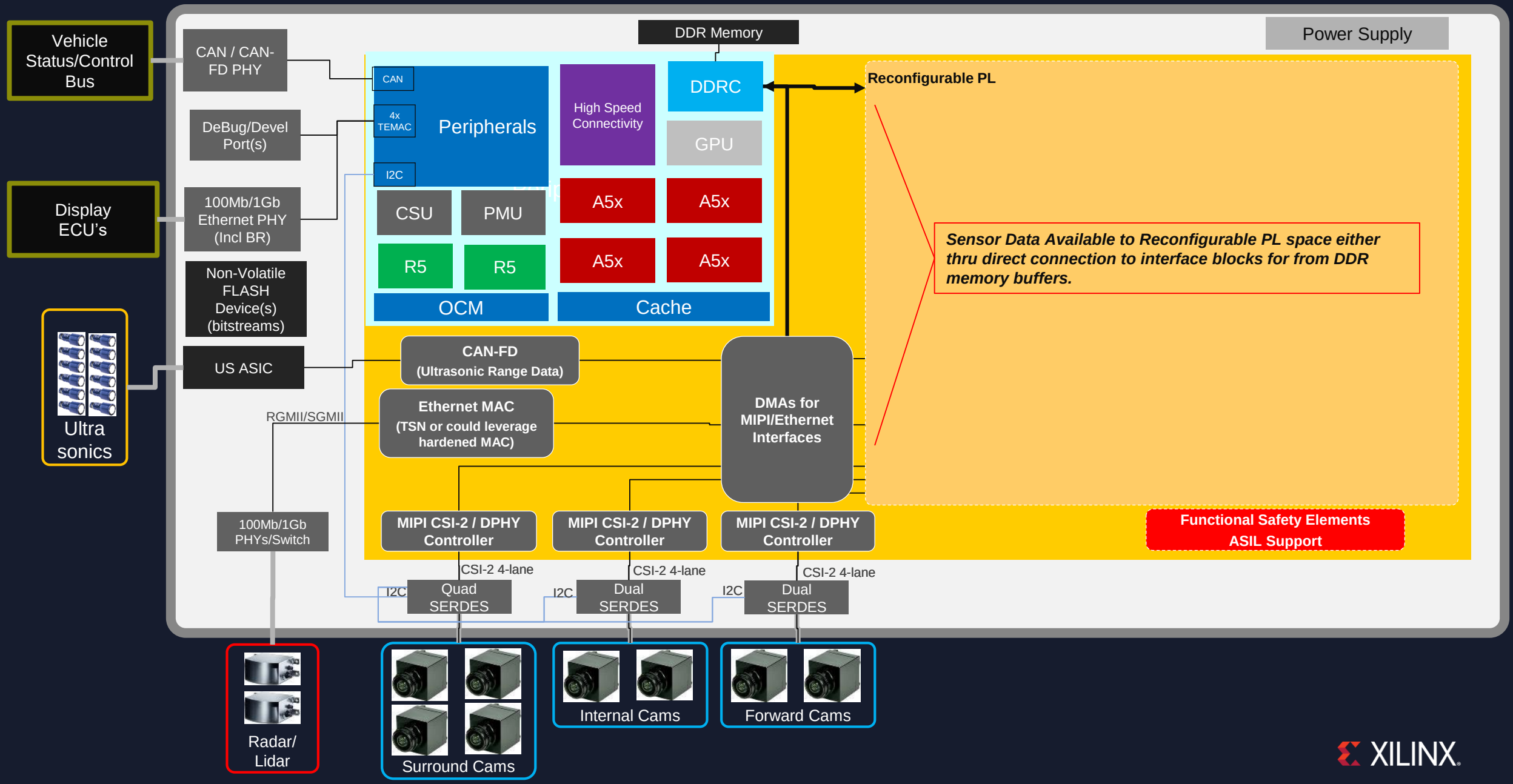
Driver Monitoring System

V



Forward Camera w/ Surround Monitor

Central Module Architecture



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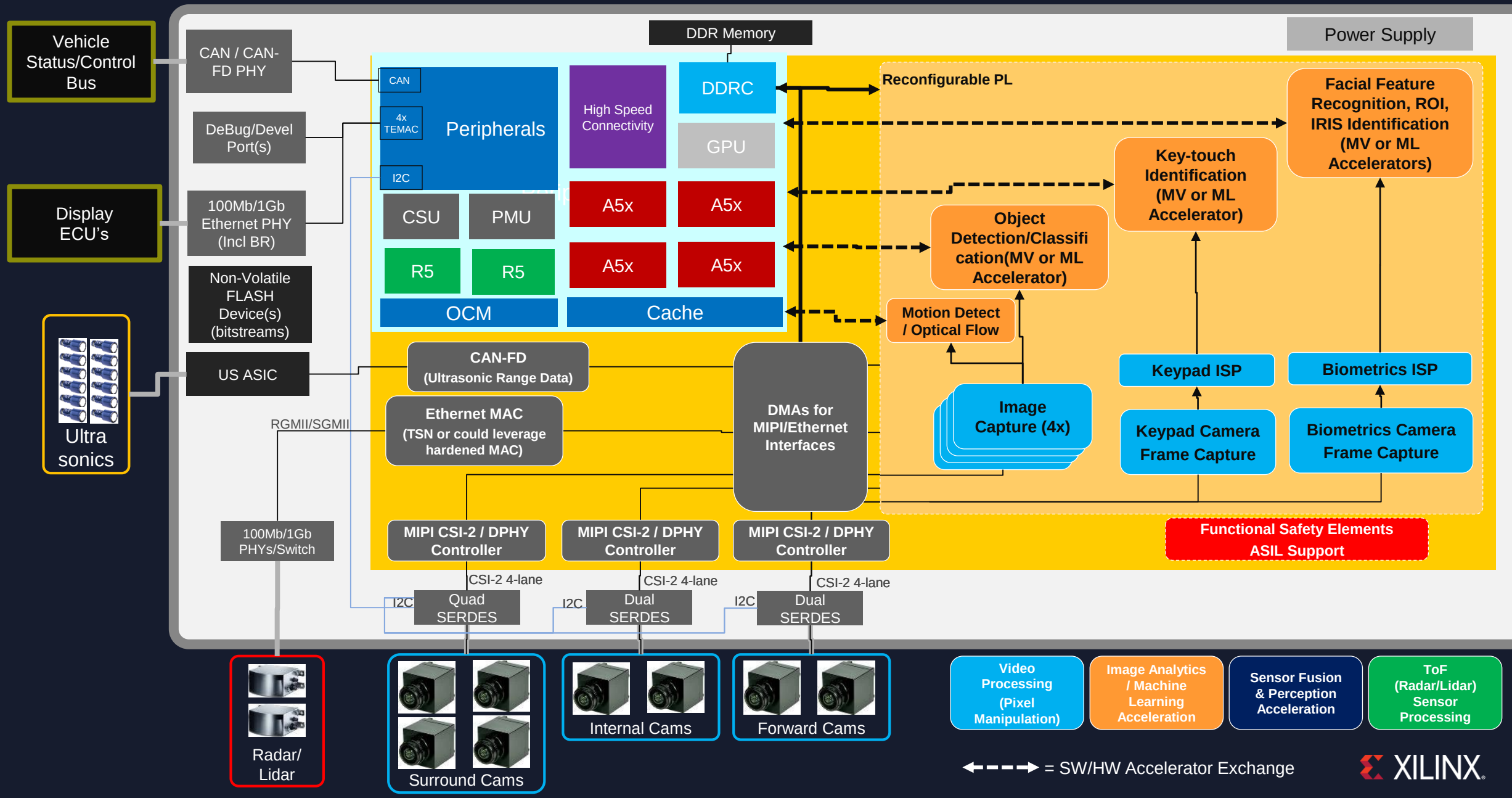
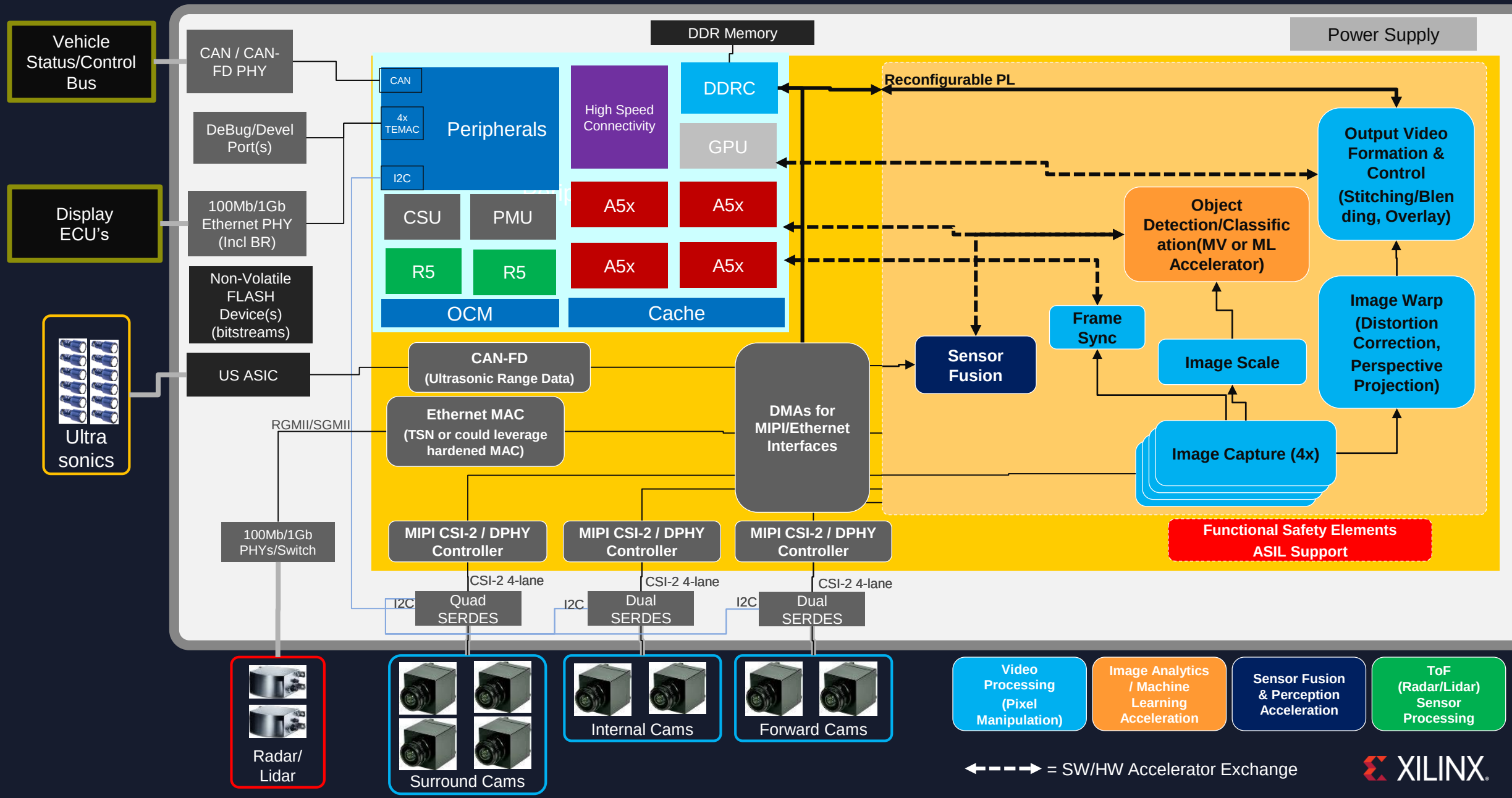
Central Module Architecture

PreDrive Security



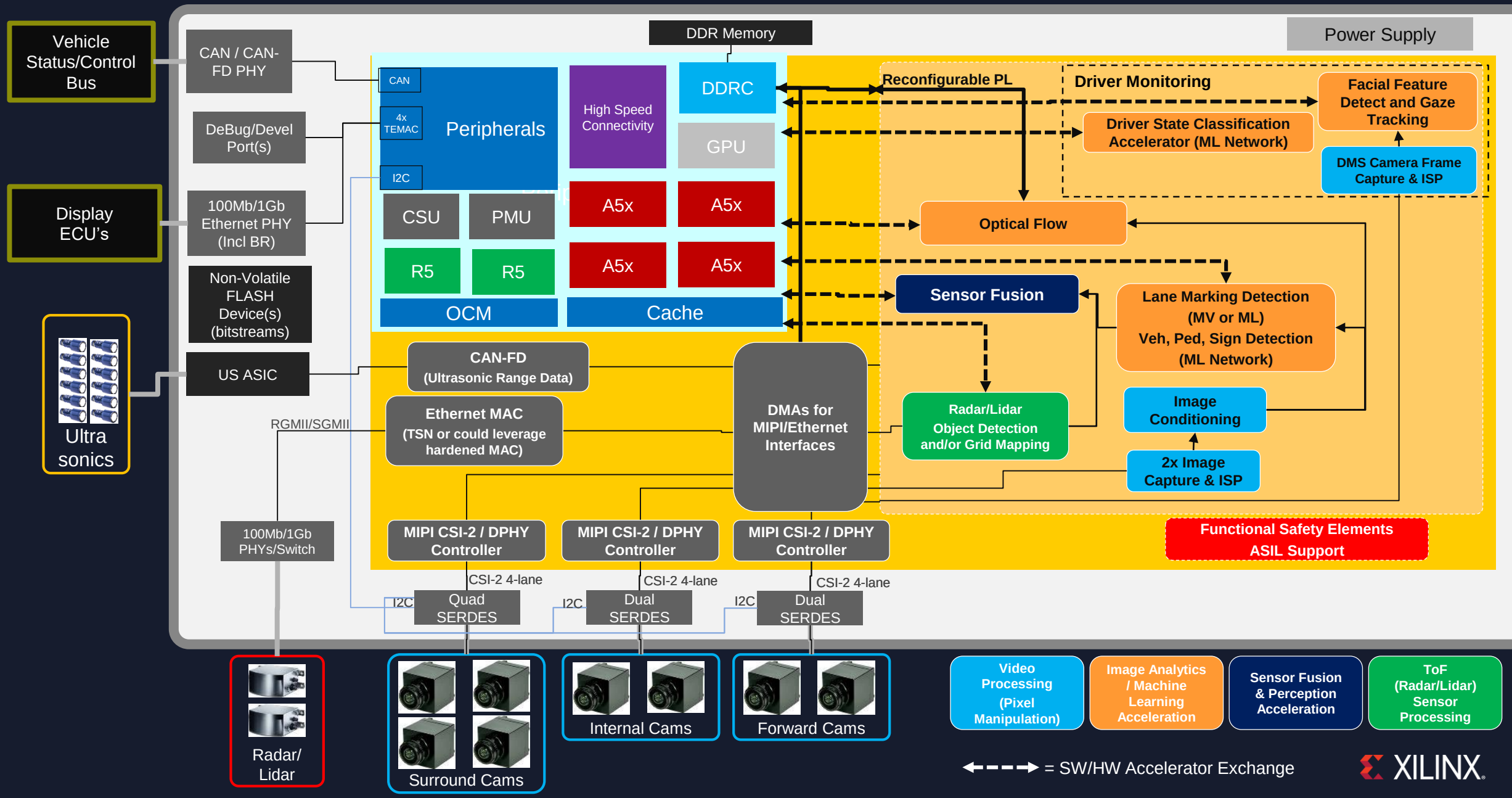
Central Module Architecture

Low Speed/Parking



Central Module Architecture

Highway Driving



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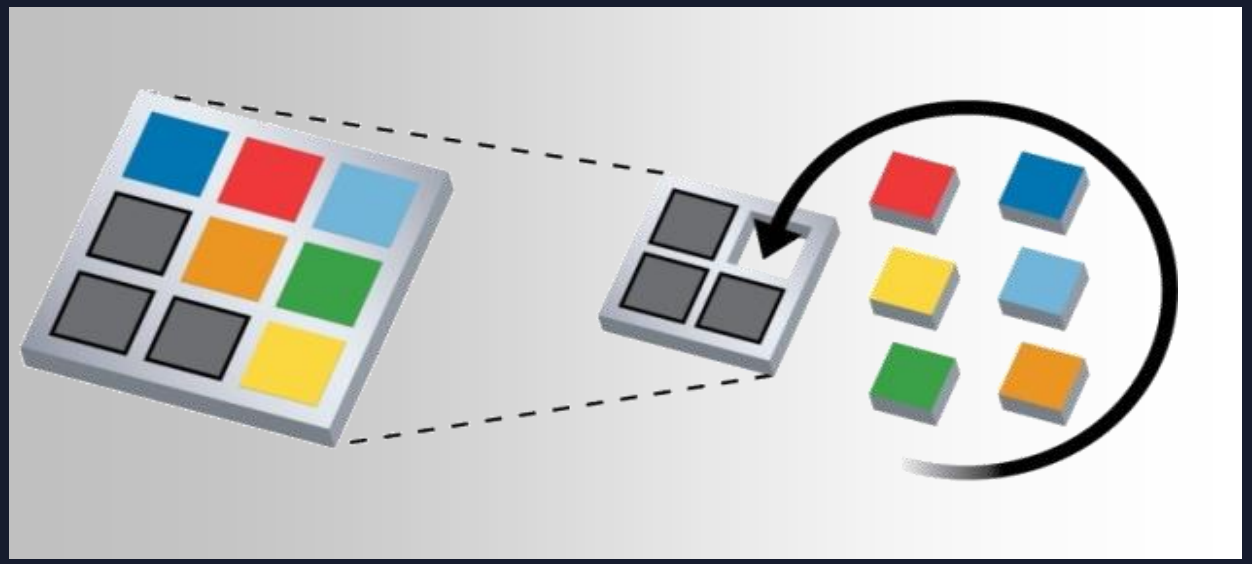
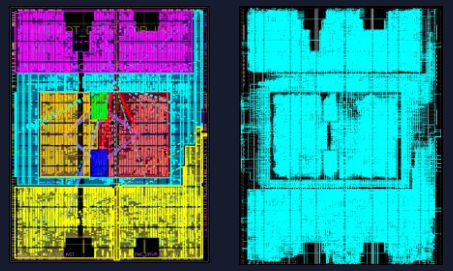
- Result is “silicon re-use” for uniquely efficient, cost-effective implementation of mutually exclusive applications

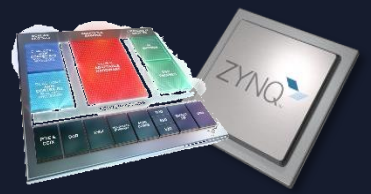
- Silicon Re-Use = Lower Density Device = Lower Cost & Power



Xilinx Functional Safety Solutions



IPs & Methodologies



SoC & FPGA

VIVADO HLx Editions

Certified Development Tools

XILINX

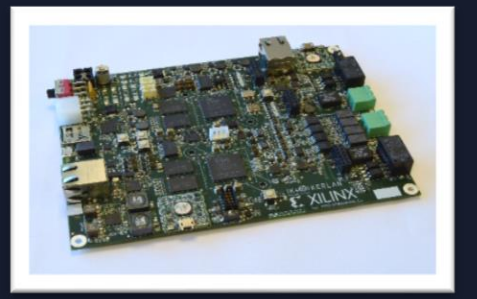
Software

exida

TÜVRheinland

TÜV SÜD

Certification Authorities



Reference Design & Ecosystem Partners

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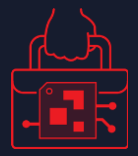
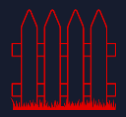
Summary

- Cost-effective & Scalable Device Families
  - Platform design for BoM scaling to various ADAS / AD Sensor and Feature Bundles



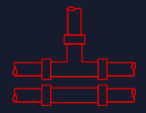
- Unique IP portability
  - IP designs migrate to / from Distributed Sensors to Centralized Modules



- Optimal Partitioning Between System Software and Hardware Accelerators
  - Integrated Sensor Data Aggregation, Compute Acceleration, and Scalar Processing

- Power Efficient, High Utilization AI / ML Inference
  - More effective use of TOPs

- Customer-owned (Proprietary) or Xilinx / Partner Licensable IP / Accelerators
  - Market Differentiation / Leadership and Fast Time to Market



- Independent (Isolated), Simultaneous, and Optimized Processing Pipelines
  - Lowest latency sensor data paths and sensor fusion

- In-field SW and HW upgradability (Unique OTA-HW)
  - Unparalleled ability to update system capabilities / performance

- Dynamic Function Exchange (processing pipelines) for Unmatched Adaptability
  - Efficiently address multi-feature systems requirements with minimized cost & power

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Thank You