Vivado Design Suite 7 Series FPGA Libraries Guide

UG953 (v 2012.2) July 25, 2012

XILINX®

Notice of Disclaimer

XILINX®

Chapter 1

Introduction

Overview

This HDL guide is part of the Vivado™ Design Suite documentation collection. A separate version of this guide is available if you prefer to work with schematics.

This guide contains the following:

- Introduction.
- A list of design elements supported in this architecture, organized by functional categories.
- Descriptions of each available primitive.

About Design Elements

This version of the Libraries Guide describes the valid design elements for 7 Series architectures including Zynq™, and includes examples of instantiation code for each element. Instantiation templates are also supplied in a separate ZIP file, which you can find on www.xilinx.com linked to this file.

Design elements are divided into the following main categories:

- **Macros :** These elements are in the UniMacro library in the tool, and are used to instantiate primitives that are complex to instantiate by just using the primitives. The synthesis tools will automatically expand the unimacros to their underlying primitives.
- **Primitives:** Xilinx components that are native to the architecture you are targeting. If you instantiate a primitive in your design, after the translation process (ngdbuild) you will end up with the exact same component in the back end. For example, if you instantiate the Virtex®-5 element known as ISERDES_NODELAY as a user primitive, after you run translate (ngdbuild) you will end up with an ISERDES_NODELAY in the back end as well. If you were using ISERDES in a Virtex-5 device, then this will automatically retarget to an ISERDES_NODELAY for Virtex-5 in the back end. Hence, this concept of a "primitive" differs from other uses of that term in this technology.

CORE Generator maintains software libraries with hundreds of functional design elements (UniMacros and primitives) for different device architectures. New functional elements are assembled with each release of development system software. In addition to a comprehensive Unified Library containing all design elements, this guide is one in a series of architecture-specific libraries.

Design Entry Methods

For each design element in this guide, Xilinx evaluates four options for using the design element, and recommends what we believe is the best solution for you. The four options are:

- **Instantiation:** This component can be instantiated directly into the design. This method is useful if you want to control the exact placement of the individual blocks.
- **Inference:** This component can be inferred by most supported synthesis tools. You should use this method if you want to have complete flexibility and portability of the code to multiple architectures. Inference also gives the tools the ability to optimize for performance, area, or power, as specified by the user to the synthesis tool.
- **Coregen & Wizards:** This component can be used through CORE Generator or other Wizards. You should use this method if you want to build large blocks of any FPGA primitive that cannot be inferred. When using this flow, you will have to re-generate your cores for each architecture that you are targeting.
- **Macro Support:** This component has a UniMacro that can be used. These components are in the UniMacro library in the Xilinx tool, and are used to instantiate primitives that are too complex to instantiate by just using the primitives. The synthesis tools will automatically expand UniMacros to their underlying primitives.

XILINX®

Chapter 2

Unimacros

Overview

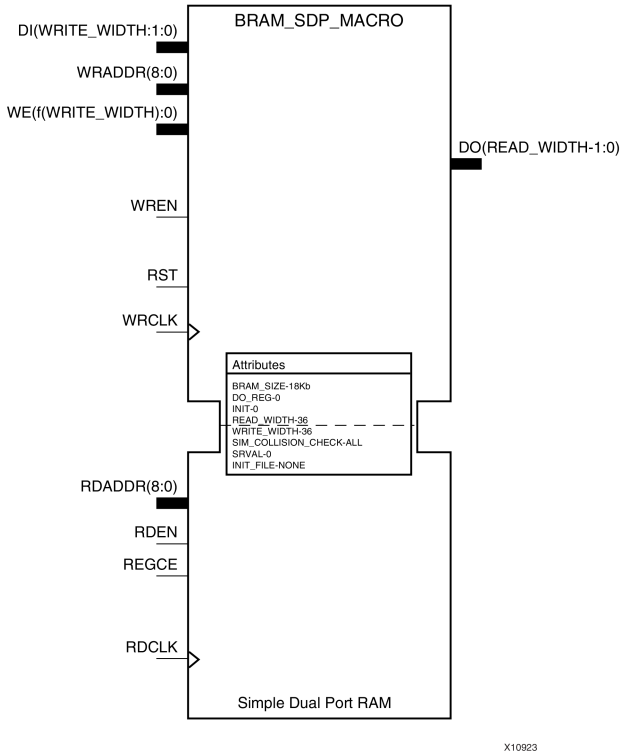
This section describes the unimacros that can be used with 7 Series architectures including Zynq™. The unimacros are organized alphabetically.

The following information is provided for each unimacro, where applicable:

- Name of element
- Brief description
- Schematic symbol
- Logic table (if any)
- Port descriptions
- Design Entry Method
- Available attributes
- Example instantiation code
- For more information

BRAM_SDP_MACRO

Macro: Simple Dual Port RAM



Introduction

7 series FPGA devices contain several block RAM memories that can be configured as general-purpose 36Kb or 18Kb RAM/ROM memories. These block RAM memories offer fast and flexible storage of large amounts of on-chip data. Both read and write operations are fully synchronous to the supplied clock(s) of the component. However, READ and WRITE ports can operate fully independently and asynchronously to each other, accessing the same memory array. Byte-enable write operations are possible, and an optional output register can be used to reduce the clock-to-out times of the RAM.

Note This element must be configured so that read and write ports have the same width.

Port Description

Name	Direction	Width (Bits)	Function
DO	Output	See Configuration Table	Data output bus addressed by RDADDR.
DI	Input	See Configuration Table	Data input bus addressed by WRADDR.
WRADDR, RDADDR	Input	See Configuration Table	Write/Read address input buses.
WE	Input	See Configuration Table	Byte-Wide Write enable.
WREN, RDEN	Input	1	Write/Read enable
SSR	Input	1	Output registers synchronous reset.
REGCE	Input	1	Output register clock enable input (valid only when DO_REG=1).
WRCLK, RDCLK	Input	1	Write/Read clock input.

Port Configuration

This unimacro is a parameterizable version of the primitive, and can be instantiated only. Use this table to correctly configure the unimacro to meet design needs.

DATA_WIDTH	BRAM_SIZE	ADDR	WE
72 - 37	36Kb	9	8
36 - 19	36Kb	10	4
	18Kb	9	
18 - 10	36Kb	11	2
	18Kb	10	
9 - 5	36Kb	12	1
	18Kb	11	
4 - 3	36Kb	13	1
	18Kb	12	
2	36Kb	14	1
	18Kb	13	
1	36Kb	15	1
	18Kb	14	

Design Entry Method

This unimacro is a parameterizable version of the primitive, and can be instantiated only. Consult the Port Configuration section to correctly configure this element to meet your design needs.

Instantiation	Yes
Inference	No
CORE Generator™ and wizards	No
Macro support	Recommended

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
BRAM_SIZE	String	"36Kb", "18Kb"	"18Kb"	Configures RAM as "36Kb" or "18Kb" memory.
DEVICE	String	"7SERIES"	"7SERIES"	Target hardware architecture.
DO_REG	Integer	0, 1	0	A value of 1 enables to the output registers to the RAM enabling quicker clock-to-out from the RAM at the expense of an added clock cycle of read latency. A value of 0 allows a read in one clock cycle but will have slower clock to out timing.
INIT	Hexadecimal	Any 72-Bit Value	All zeros	Specifies the initial value on the output after configuration.
READ_WIDTH, WRITE_WIDTH	Integer	1-72	36	Specifies the size of the DI and DO buses. The following combinations are allowed: • READ_WIDTH = WRITE_WIDTH • If asymmetric, READ_WIDTH and WRITE_WIDTH must be in the ratio of 2, or must be values allowed by the unisim (1, 2, 4, 8, 9, 16, 18, 32, 36, 64, 72)
INIT_FILE	String	String representing file name and location.	NONE	Name of the file containing initial values.

Attribute	Data Type	Allowed Values	Default	Description
SIM_COLLISION_CHECK	String	"ALL", "WARNING_ONLY", "GENERATE_X_ONLY", "NONE"	"ALL"	Allows modification of the simulation behavior if a memory collision occurs. The output is affected as follows: • "ALL" - Warning produced and affected outputs/memory location go unknown (X). • "WARNING_ONLY" - Warning produced and affected outputs/memory retain last value. • "GENERATE_X_ONLY" - No warning. However, affected outputs/memory go unknown (X). • "NONE" - No warning and affected outputs/memory retain last value. **Note** Setting this to a value other than "ALL" can allow problems in the design go unnoticed during simulation. Care should be taken when changing the value of this attribute. Please see the *Synthesis and Simulation Design Guide* for more information.
SRVAL	Hexadecimal	Any 72-Bit Value	All zeroes	Specifies the output value of on the DO port upon the assertion of the synchronous reset (RST) signal.
INIT_00 to INIT_7F	Hexadecimal	Any 256-Bit Value	All zeroes	Allows specification of the initial contents of the 16Kb or 32Kb data memory array.
INITP_00 to INITP_0F	Hexadecimal	Any 256-Bit Value	All zeroes	Allows specification of the initial contents of the 2Kb or 4Kb parity data memory array.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- BRAM_SDP_MACRO: Simple Dual Port RAM
--                 7 Series
-- Xilinx HDL Libraries Guide, version 2012.2
```

```
-- Note -  This Unimacro model assumes the port directions to be "downto".
--         Simulation of this model with "to" in the port directions could lead to erroneous results.

-----------------------------------------------------------------------
--  READ_WIDTH | BRAM_SIZE | READ Depth  | RDADDR Width |            --
-- WRITE_WIDTH |           | WRITE Depth | WRADDR Width |  WE Width  --
-- ============|===========|=============|==============|============--
--    37-72    |  "36Kb"   |      512    |     9-bit    |    8-bit   --
--    19-36    |  "36Kb"   |     1024    |    10-bit    |    4-bit   --
--    19-36    |  "18Kb"   |      512    |     9-bit    |    4-bit   --
--    10-18    |  "36Kb"   |     2048    |    11-bit    |    2-bit   --
--    10-18    |  "18Kb"   |     1024    |    10-bit    |    2-bit   --
--     5-9     |  "36Kb"   |     4096    |    12-bit    |    1-bit   --
--     5-9     |  "18Kb"   |     2048    |    11-bit    |    1-bit   --
--     3-4     |  "36Kb"   |     8192    |    13-bit    |    1-bit   --
--     3-4     |  "18Kb"   |     4096    |    12-bit    |    1-bit   --
--       2     |  "36Kb"   |    16384    |    14-bit    |    1-bit   --
--       2     |  "18Kb"   |     8192    |    13-bit    |    1-bit   --
--       1     |  "36Kb"   |    32768    |    15-bit    |    1-bit   --
--       1     |  "18Kb"   |    16384    |    14-bit    |    1-bit   --
-----------------------------------------------------------------------


BRAM_SDP_MACRO_inst : BRAM_SDP_MACRO
generic map (
   BRAM_SIZE => "18Kb", -- Target BRAM, "18Kb" or "36Kb"
   DEVICE => "7SERIES", -- Target device: "VIRTEX5", "VIRTEX6", "7SERIES", "SPARTAN6"
   WRITE_WIDTH => 0,    -- Valid values are 1-72 (37-72 only valid when BRAM_SIZE="36Kb")
   READ_WIDTH => 0,     -- Valid values are 1-72 (37-72 only valid when BRAM_SIZE="36Kb")
   DO_REG => 0, -- Optional output register (0 or 1)
   INIT_FILE => "NONE",
   SIM_COLLISION_CHECK => "ALL", -- Collision check enable "ALL", "WARNING_ONLY",
                                 -- "GENERATE_X_ONLY" or "NONE"
   SRVAL => X"0000000000000000", --  Set/Reset value for port output
   WRITE_MODE => "WRITE_FIRST", -- Specify "READ_FIRST" for same clock or synchronous clocks
                                --  Specify "WRITE_FIRST for asynchrononous clocks on ports
   INIT => X"0000000000000000", --  Initial values on output port
   -- The following INIT_xx declarations specify the initial contents of the RAM
   INIT_00 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_01 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_02 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_03 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_04 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_05 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_06 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_07 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_08 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_09 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_0A => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_0B => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_0C => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_0D => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_0E => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_0F => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_10 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_11 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_12 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_13 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_14 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_15 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_16 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_17 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_18 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_19 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_1A => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_1B => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_1C => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_1D => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_1E => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_1F => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_20 => X"0000000000000000000000000000000000000000000000000000000000000000",
```

```
INIT_21 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_22 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_23 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_24 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_25 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_26 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_27 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_28 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_29 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_2A => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_2B => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_2C => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_2D => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_2E => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_2F => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_30 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_31 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_32 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_33 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_34 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_35 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_36 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_37 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_38 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_39 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_3A => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_3B => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_3C => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_3D => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_3E => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_3F => X"0000000000000000000000000000000000000000000000000000000000000000",

-- The next set of INIT_xx are valid when configured as 36Kb
INIT_40 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_41 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_42 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_43 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_44 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_45 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_46 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_47 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_48 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_49 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_4A => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_4B => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_4C => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_4D => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_4E => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_4F => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_50 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_51 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_52 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_53 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_54 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_55 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_56 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_57 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_58 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_59 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_5A => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_5B => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_5C => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_5D => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_5E => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_5F => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_60 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_61 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_62 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_63 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_64 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_65 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_66 => X"0000000000000000000000000000000000000000000000000000000000000000",
```

```
   INIT_67 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_68 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_69 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_6A => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_6B => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_6C => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_6D => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_6E => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_6F => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_70 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_71 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_72 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_73 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_74 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_75 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_76 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_77 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_78 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_79 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_7A => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_7B => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_7C => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_7D => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_7E => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_7F => X"0000000000000000000000000000000000000000000000000000000000000000",

   -- The next set of INITP_xx are for the parity bits
   INITP_00 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_01 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_02 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_03 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_04 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_05 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_06 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_07 => X"0000000000000000000000000000000000000000000000000000000000000000",

   -- The next set of INIT_xx are valid when configured as 36Kb
   INITP_08 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_09 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_0A => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_0B => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_0C => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_0D => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_0E => X"0000000000000000000000000000000000000000000000000000000000000000",
port map (
   DO => DO,         -- Output read data port, width defined by READ_WIDTH parameter
   DI => DI,         -- Input write data port, width defined by WRITE_WIDTH parameter
   RDADDR => RDADDR, -- Input read address, width defined by read port depth
   RDCLK => RDCLK,   -- 1-bit input read clock
   RDEN => RDEN,     -- 1-bit input read port enable
   REGCE => REGCE,   -- 1-bit input read output register enable
   RST => RST,       -- 1-bit input reset
   WE => WE,         -- Input write enable, width defined by write port depth
   WRADDR => WRADDR, -- Input write address, width defined by write port depth
   WRCLK => WRCLK,   -- 1-bit input write clock
   WREN => WREN      -- 1-bit input write port enable
);
-- End of BRAM_SDP_MACRO_inst instantiation
```

Verilog Instantiation Template

```
// BRAM_SDP_MACRO: Simple Dual Port RAM
//                 7 Series
// Xilinx HDL Libraries Guide, version 2012.2

//////////////////////////////////////////////////////////////////
//  READ_WIDTH | BRAM_SIZE | READ Depth  | RDADDR Width |            //
// WRITE_WIDTH |           | WRITE Depth | WRADDR Width |  WE Width  //
// ============|===========|=============|==============|============//
//    37-72    |  "36Kb"   |      512    |     9-bit    |    8-bit   //
```

```
//    19-36    |  "36Kb"   |     1024    |    10-bit    |    4-bit   //
//    19-36    |  "18Kb"   |      512    |     9-bit    |    4-bit   //
//    10-18    |  "36Kb"   |     2048    |    11-bit    |    2-bit   //
//    10-18    |  "18Kb"   |     1024    |    10-bit    |    2-bit   //
//     5-9     |  "36Kb"   |     4096    |    12-bit    |    1-bit   //
//     5-9     |  "18Kb"   |     2048    |    11-bit    |    1-bit   //
//     3-4     |  "36Kb"   |     8192    |    13-bit    |    1-bit   //
//     3-4     |  "18Kb"   |     4096    |    12-bit    |    1-bit   //
//       2     |  "36Kb"   |    16384    |    14-bit    |    1-bit   //
//       2     |  "18Kb"   |     8192    |    13-bit    |    1-bit   //
//       1     |  "36Kb"   |    32768    |    15-bit    |    1-bit   //
//       1     |  "18Kb"   |    16384    |    14-bit    |    1-bit   //
//////////////////////////////////////////////////////////////////////

BRAM_SDP_MACRO #(
   .BRAM_SIZE("18Kb"), // Target BRAM, "18Kb" or "36Kb"
   .DEVICE("7SERIES"), // Target device: "7SERIES"
   .WRITE_WIDTH(0),    // Valid values are 1-72 (37-72 only valid when BRAM_SIZE="36Kb")
   .READ_WIDTH(0),     // Valid values are 1-72 (37-72 only valid when BRAM_SIZE="36Kb")
   .DO_REG(0),         // Optional output register (0 or 1)
   .INIT_FILE ("NONE"),
   .SIM_COLLISION_CHECK ("ALL"), // Collision check enable "ALL", "WARNING_ONLY",
                                 //   "GENERATE_X_ONLY" or "NONE"
   .SRVAL(72'h000000000000000000), // Set/Reset value forr port output
   .INIT(72'h000000000000000000),  // Initial values on output port
   .WRITE_MODE("WRITE_FIRST"),  // Specify "READ_FIRST" forr same clock or synchronous clocks
                                //   Specify "WRITE_FIRST forr asynchronous clocks on ports
   .INIT_00(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_01(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_02(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_03(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_04(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_05(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_06(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_07(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_08(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_09(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_0A(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_0B(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_0C(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_0D(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_0E(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_0F(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_10(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_11(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_12(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_13(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_14(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_15(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_16(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_17(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_18(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_19(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_1A(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_1B(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_1C(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_1D(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_1E(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_1F(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_20(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_21(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_22(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_23(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_24(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_25(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_26(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_27(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_28(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_29(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_2A(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_2B(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_2C(256'h0000000000000000000000000000000000000000000000000000000000000000),
```

```
.INIT_2D(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_2E(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_2F(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_30(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_31(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_32(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_33(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_34(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_35(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_36(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_37(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_38(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_39(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_3A(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_3B(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_3C(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_3D(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_3E(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_3F(256'h0000000000000000000000000000000000000000000000000000000000000000),

// The next set of INIT_xx are valid when configured as 36Kb
.INIT_40(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_41(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_42(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_43(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_44(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_45(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_46(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_47(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_48(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_49(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_4A(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_4B(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_4C(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_4D(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_4E(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_4F(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_50(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_51(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_52(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_53(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_54(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_55(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_56(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_57(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_58(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_59(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_5A(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_5B(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_5C(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_5D(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_5E(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_5F(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_60(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_61(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_62(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_63(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_64(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_65(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_66(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_67(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_68(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_69(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_6A(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_6B(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_6C(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_6D(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_6E(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_6F(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_70(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_71(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_72(256'h0000000000000000000000000000000000000000000000000000000000000000),
```

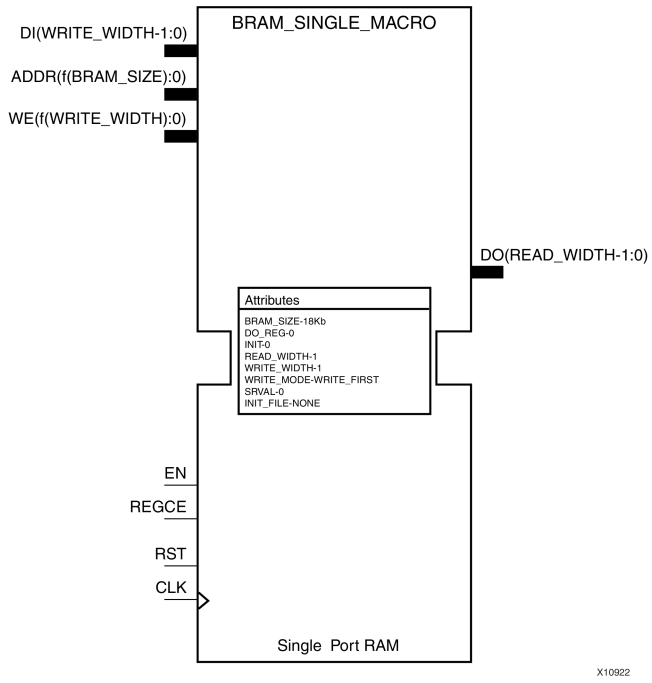
```
   .INIT_73(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_74(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_75(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_76(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_77(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_78(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_79(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_7A(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_7B(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_7C(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_7D(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_7E(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_7F(256'h0000000000000000000000000000000000000000000000000000000000000000),

   // The next set of INITP_xx are forr the parity bits
   .INITP_00(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_01(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_02(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_03(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_04(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_05(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_06(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_07(256'h0000000000000000000000000000000000000000000000000000000000000000),

   // The next set of INITP_xx are valid when configured as 36Kb
   .INITP_08(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_09(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_0A(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_0B(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_0C(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_0D(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_0E(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_0F(256'h0000000000000000000000000000000000000000000000000000000000000000)
) BRAM_SDP_MACRO_inst (
   .DO(DO),         // Output read data port, width defined by READ_WIDTH parameter
   .DI(DI),         // Input write data port, width defined by WRITE_WIDTH parameter
   .RDADDR(RDADDR), // Input read address, width defined by read port depth
   .RDCLK(RDCLK),   // 1-bit input read clock
   .RDEN(RDEN),     // 1-bit input read port enable
   .REGCE(REGCE),   // 1-bit input read output register enable
   .RST(RST),       // 1-bit input reset
   .WE(WE),         // Input write enable, width defined by write port depth
   .WRADDR(WRADDR), // Input write address, width defined by write port depth
   .WRCLK(WRCLK),   // 1-bit input write clock
   .WREN(WREN)      // 1-bit input write port enable
);

// End of BRAM_SDP_MACRO_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

BRAM_SINGLE_MACRO

Macro: Single Port RAM



Introduction

7 series FPGA devices contain several block RAM memories that can be configured as general-purpose 36Kb or 18Kb RAM/ROM memories. These single-port, block RAM memories offer fast and flexible storage of large amounts of on-chip data. Byte-enable write operations are possible, and an optional output register can be used to reduce the clock-to-out times of the RAM.

Port Description

Name	Direction	Width	Function
DO	Output	See Configuration Table below.	Data output bus addressed by ADDR.
DI	Input	See Configuration Table below.	Data input bus addressed by ADDR.
ADDR	Input	See Configuration Table below.	Address input bus.
WE	Input	See Configuration Table below.	Byte-Wide Write enable.
EN	Input	1	Write/Read enables.
RST	Input	1	Output registers synchronous reset.

Name	Direction	Width	Function
REGCE	Input	1	Output register clock enable input (valid only when DO_REG=1).
CLK	Input	1	Clock input.

Port Configuration

This unimacro is a parameterizable version of the primitive, and can be instantiated only. Use this table to correctly configure the unimacro to meet design needs.

WRITE_WIDTH	READ_WIDTH	BRAM_SIZE	ADDR	WE
72 - 37	72 - 37	36Kb	9	8
	36 - 19		10	
	18 - 10		11	
	9 - 5		12	
	4 - 3		13	
	2		14	
	1		15	
36 - 19	36 - 19	36Kb	10	4
	18-10		11	
	9 - 5		12	
	4 - 3		13	
	2		14	
	1		15	
18 - 10	36 - 19	36Kb	11	2
	18-10		11	
	9 - 5		12	
	4 - 3		13	
	2		14	
	1		15	
9 - 5	36-19	36Kb	12	1
	18-10		12	
	9 - 5		12	
	4 - 3		13	
	2		14	
	1		15	

WRITE_WIDTH	READ_WIDTH	BRAM_SIZE	ADDR	WE
4 - 3	36-19	36Kb	13	1
	18-10		13	
	9 - 5		13	
	4 - 3		13	
	2		14	
	1		15	
2	36-19	36Kb	14	1
	18-10		14	
	9 - 5		14	
	4 - 3		14	
	2		14	
	1		15	
1	36 - 19	36Kb	15	1
	18 - 10		15	
	9 - 5		15	
	3 - 4		15	
	2		15	
	1		15	
18-10	18-10	18Kb	10	2
	9 - 5		11	
	4 - 3		12	
	2		13	
	1		14	
9 - 5	18-10	18Kb	11	1
	9 - 5		11	
	4 - 3		12	
	2		13	
	1		14	

WRITE_WIDTH	READ_WIDTH	BRAM_SIZE	ADDR	WE
4 - 3	18-10	18Kb	12	1
	9 - 5		12	
	4 - 3		12	
	2		13	
	1		14	
2	18-10	18Kb	13	1
	9 - 5		13	
	4 - 3		13	
	2		13	
	1		14	
1	18-10	18Kb	14	1
	9 - 5		14	
	4 - 3		14	
	2		14	
	1		14	

Design Entry Method

This unimacro is a parameterizable version of the primitive, and can be instantiated only. Consult the Port Configuration section to correctly configure this element to meet your design needs.

Instantiation	Yes
Inference	No
CORE Generator™ and wizards	No
Macro support	Recommended

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
BRAM_SIZE	String	"36Kb", "18Kb"	"18Kb"	Configures RAM as "36Kb" or "18Kb" memory.
DEVICE	String	"7SERIES"	"7SERIES"	Target hardware architecture.
DO_REG	Integer	0, 1	0	A value of 1 enables to the output registers to the RAM enabling quicker clock-to-out from the RAM at the expense of an added clock cycle of read latency. A value of 0 allows a read in one clock cycle but will have slower clock to out timing.

Attribute	Data Type	Allowed Values	Default	Description
READ_WIDTH, WRITE_WIDTH	Integer	1 - 36	1	Specifies the size of the DI and DO buses. The following combinations are allowed: • READ_WIDTH = WRITE_WIDTH • If asymmetric, READ_WIDTH and WRITE_WIDTH must be in the ratio of 2, or must be values allowed by the unisim (1, 2, 4, 8, 9, 16, 18, 32, 36, 64, 72)
INIT_FILE	String	String representing file name and location.	None	Name of the file containing initial values.
WRITE_MODE	String	"READ_FIRST", "WRITE_FIRST", "NO_CHANGE"	"WRITE_FIRST"	Specifies write mode to the memory.
INIT	Hexadecimal	Any 72-Bit Value	All zeros	Specifies the initial value on the output after configuration.
SRVAL	Hexadecimal	Any 72-Bit Value	All zeroes	Specifies the output value of on the DO port upon the assertion of the synchronous reset (RST) signal.
INIT_00 to INIT_FF	Hexadecimal	Any 256-Bit Value	All zeroes	Allows specification of the initial contents of the 16Kb or 32Kb data memory array.
INITP_00 to INITP_0F	Hexadecimal	Any 256-Bit Value	All zeroes	Allows specification of the initial contents of the 2Kb or 4Kb parity data memory array.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- BRAM_SINGLE_MACRO: Single Port RAM
--                    7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

-- Note -  This Unimacro model assumes the port directions to be "downto".
--         Simulation of this model with "to" in the port directions could lead to erroneous results.

-----------------------------------------------------------------------
--  READ_WIDTH | BRAM_SIZE | READ Depth  | ADDR Width |            --
-- WRITE_WIDTH |           | WRITE Depth |            |  WE Width  --
-- ============|===========|=============|============|============--
--    37-72    |  "36Kb"   |      512    |    9-bit   |    8-bit   --
--    19-36    |  "36Kb"   |     1024    |   10-bit   |    4-bit   --
--    19-36    |  "18Kb"   |      512    |    9-bit   |    4-bit   --
--    10-18    |  "36Kb"   |     2048    |   11-bit   |    2-bit   --
--    10-18    |  "18Kb"   |     1024    |   10-bit   |    2-bit   --
```

```
--     5-9     |  "36Kb"   |     4096    |   12-bit   |    1-bit   --
--     5-9     |  "18Kb"   |     2048    |   11-bit   |    1-bit   --
--     3-4     |  "36Kb"   |     8192    |   13-bit   |    1-bit   --
--     3-4     |  "18Kb"   |     4096    |   12-bit   |    1-bit   --
--       2     |  "36Kb"   |    16384    |   14-bit   |    1-bit   --
--       2     |  "18Kb"   |     8192    |   13-bit   |    1-bit   --
--       1     |  "36Kb"   |    32768    |   15-bit   |    1-bit   --
--       1     |  "18Kb"   |    16384    |   14-bit   |    1-bit   --
-----------------------------------------------------------------------

BRAM_SINGLE_MACRO_inst : BRAM_SINGLE_MACRO
generic map (
   BRAM_SIZE => "18Kb", -- Target BRAM, "18Kb" or "36Kb"
   DEVICE => "7SERIES", -- Target Device: "VIRTEX5", "7SERIES", "VIRTEX6, "SPARTAN6"
   DO_REG => 0, -- Optional output register (0 or 1)
   INIT => X"000000000",    --  Initial values on output port
   INIT_FILE => "NONE",
   WRITE_WIDTH => 0,   -- Valid values are 1-72 (37-72 only valid when BRAM_SIZE="36Kb")
   READ_WIDTH => 0,   -- Valid values are 1-72 (37-72 only valid when BRAM_SIZE="36Kb")
   SRVAL => X"000000000",    -- Set/Reset value for port output
   WRITE_MODE => "WRITE_FIRST", -- "WRITE_FIRST", "READ_FIRST" or "NO_CHANGE"
   -- The following INIT_xx declarations specify the initial contents of the RAM
   INIT_00 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_01 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_02 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_03 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_04 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_05 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_06 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_07 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_08 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_09 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_0A => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_0B => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_0C => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_0D => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_0E => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_0F => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_10 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_11 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_12 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_13 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_14 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_15 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_16 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_17 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_18 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_19 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_1A => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_1B => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_1C => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_1D => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_1E => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_1F => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_20 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_21 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_22 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_23 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_24 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_25 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_26 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_27 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_28 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_29 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_2A => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_2B => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_2C => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_2D => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_2E => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_2F => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_30 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_31 => X"0000000000000000000000000000000000000000000000000000000000000000",
```

```
INIT_32 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_33 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_34 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_35 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_36 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_37 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_38 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_39 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_3A => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_3B => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_3C => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_3D => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_3E => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_3F => X"0000000000000000000000000000000000000000000000000000000000000000",

-- The next set of INIT_xx are valid when configured as 36Kb
INIT_40 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_41 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_42 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_43 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_44 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_45 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_46 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_47 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_48 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_49 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_4A => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_4B => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_4C => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_4D => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_4E => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_4F => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_50 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_51 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_52 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_53 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_54 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_55 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_56 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_57 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_58 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_59 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_5A => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_5B => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_5C => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_5D => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_5E => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_5F => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_60 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_61 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_62 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_63 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_64 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_65 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_66 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_67 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_68 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_69 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_6A => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_6B => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_6C => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_6D => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_6E => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_6F => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_70 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_71 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_72 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_73 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_74 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_75 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_76 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_77 => X"0000000000000000000000000000000000000000000000000000000000000000",
```

```
   INIT_78 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_79 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_7A => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_7B => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_7C => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_7D => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_7E => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_7F => X"0000000000000000000000000000000000000000000000000000000000000000",

   -- The next set of INITP_xx are for the parity bits
   INITP_00 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_01 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_02 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_03 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_04 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_05 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_06 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_07 => X"0000000000000000000000000000000000000000000000000000000000000000",

   -- The next set of INIT_xx are valid when configured as 36Kb
   INITP_08 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_09 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_0A => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_0B => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_0C => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_0D => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_0E => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_0F => X"0000000000000000000000000000000000000000000000000000000000000000")
port map (
   DO => DO,      -- Output data, width defined by READ_WIDTH parameter
   ADDR => ADDR,  -- Input address, width defined by read/write port depth
   CLK => CLK,    -- 1-bit input clock
   DI => DI,      -- Input data port, width defined by WRITE_WIDTH parameter
   EN => EN,      -- 1-bit input RAM enable
   REGCE => REGCE, -- 1-bit input output register enable
   RST => RST,    -- 1-bit input reset
   WE => WE       -- Input write enable, width defined by write port depth
);

-- End of BRAM_SINGLE_MACRO_inst instantiation
```

Verilog Instantiation Template

```
// BRAM_SINGLE_MACRO: Single Port RAM
//                    7 Series
// Xilinx HDL Libraries Guide, version 2012.2

//////////////////////////////////////////////////////////////////
//  READ_WIDTH | BRAM_SIZE | READ Depth  | ADDR Width |            //
// WRITE_WIDTH |           | WRITE Depth |            |  WE Width  //
// ============|===========|=============|============|============//
//    37-72    |  "36Kb"   |      512    |    9-bit   |    8-bit   //
//    19-36    |  "36Kb"   |     1024    |   10-bit   |    4-bit   //
//    19-36    |  "18Kb"   |      512    |    9-bit   |    4-bit   //
//    10-18    |  "36Kb"   |     2048    |   11-bit   |    2-bit   //
//    10-18    |  "18Kb"   |     1024    |   10-bit   |    2-bit   //
//     5-9     |  "36Kb"   |     4096    |   12-bit   |    1-bit   //
//     5-9     |  "18Kb"   |     2048    |   11-bit   |    1-bit   //
//     3-4     |  "36Kb"   |     8192    |   13-bit   |    1-bit   //
//     3-4     |  "18Kb"   |     4096    |   12-bit   |    1-bit   //
//       2     |  "36Kb"   |    16384    |   14-bit   |    1-bit   //
//       2     |  "18Kb"   |     8192    |   13-bit   |    1-bit   //
//       1     |  "36Kb"   |    32768    |   15-bit   |    1-bit   //
//       1     |  "18Kb"   |    16384    |   14-bit   |    1-bit   //
//////////////////////////////////////////////////////////////////

BRAM_SINGLE_MACRO #(
   .BRAM_SIZE("18Kb"), // Target BRAM, "18Kb" or "36Kb"
   .DEVICE("7SERIES"), // Target Device: "7SERIES"
   .DO_REG(0), // Optional output register (0 or 1)
```

```
.INIT(36'h000000000), // Initial values on output port
.INIT_FILE ("NONE"),
.WRITE_WIDTH(0), // Valid values are 1-72 (37-72 only valid when BRAM_SIZE="36Kb")
.READ_WIDTH(0),  // Valid values are 1-72 (37-72 only valid when BRAM_SIZE="36Kb")
.SRVAL(36'h000000000), // Set/Reset value forr port output
.WRITE_MODE("WRITE_FIRST"), // "WRITE_FIRST", "READ_FIRST", or "NO_CHANGE"
.INIT_00(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_01(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_02(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_03(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_04(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_05(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_06(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_07(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_08(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_09(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_0A(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_0B(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_0C(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_0D(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_0E(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_0F(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_10(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_11(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_12(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_13(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_14(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_15(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_16(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_17(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_18(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_19(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_1A(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_1B(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_1C(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_1D(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_1E(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_1F(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_20(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_21(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_22(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_23(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_24(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_25(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_26(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_27(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_28(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_29(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_2A(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_2B(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_2C(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_2D(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_2E(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_2F(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_30(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_31(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_32(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_33(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_34(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_35(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_36(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_37(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_38(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_39(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_3A(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_3B(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_3C(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_3D(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_3E(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_3F(256'h0000000000000000000000000000000000000000000000000000000000000000),

// The next set of INIT_xx are valid when configured as 36Kb
```

```
.INIT_40(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_41(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_42(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_43(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_44(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_45(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_46(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_47(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_48(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_49(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_4A(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_4B(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_4C(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_4D(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_4E(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_4F(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_50(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_51(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_52(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_53(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_54(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_55(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_56(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_57(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_58(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_59(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_5A(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_5B(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_5C(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_5D(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_5E(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_5F(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_60(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_61(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_62(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_63(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_64(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_65(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_66(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_67(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_68(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_69(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_6A(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_6B(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_6C(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_6D(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_6E(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_6F(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_70(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_71(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_72(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_73(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_74(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_75(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_76(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_77(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_78(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_79(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_7A(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_7B(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_7C(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_7D(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_7E(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_7F(256'h0000000000000000000000000000000000000000000000000000000000000000),

// The next set of INITP_xx are forr the parity bits
.INITP_00(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INITP_01(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INITP_02(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INITP_03(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INITP_04(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INITP_05(256'h0000000000000000000000000000000000000000000000000000000000000000),
```

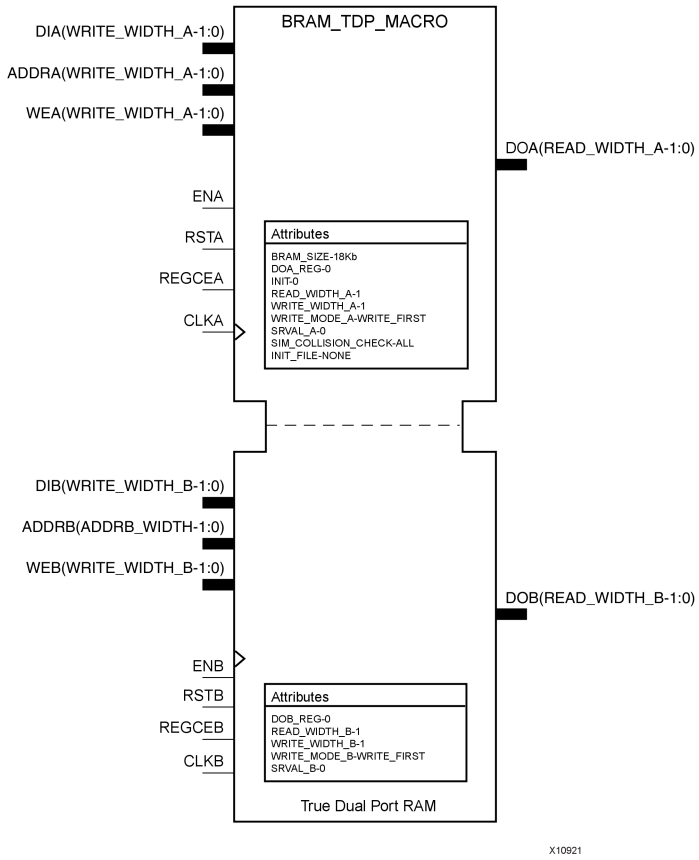
```
   .INITP_06(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_07(256'h0000000000000000000000000000000000000000000000000000000000000000),

   // The next set of INIT_xx are valid when configured as 36Kb
   .INITP_08(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_09(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_0A(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_0B(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_0C(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_0D(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_0E(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_0F(256'h0000000000000000000000000000000000000000000000000000000000000000)
) BRAM_SINGLE_MACRO_inst (
   .DO(DO),       // Output data, width defined by READ_WIDTH parameter
   .ADDR(ADDR),   // Input address, width defined by read/write port depth
   .CLK(CLK),     // 1-bit input clock
   .DI(DI),       // Input data port, width defined by WRITE_WIDTH parameter
   .EN(EN),       // 1-bit input RAM enable
   .REGCE(REGCE), // 1-bit input output register enable
   .RST(RST),     // 1-bit input reset
   .WE(WE)        // Input write enable, width defined by write port depth
);

// End of BRAM_SINGLE_MACRO_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

BRAM_TDP_MACRO

Macro: True Dual Port RAM



Introduction

7 series FPGA devices contain several block RAM memories that can be configured as general-purpose 36kb or 18kb RAM/ROM memories. These block RAM memories offer fast and flexible storage of large amounts of on-chip data. Both read and write operations are fully synchronous to the supplied clock(s) of the component. However, READ and WRITE ports can operate fully independently and asynchronous to each other, accessing the same memory array. Byte-enable write operations are possible, and an optional output register can be used to reduce the clock-to-out times of the RAM.

Port Description

Name	Direction	Width	Function
DOA	Output	See Configuration Table below.	Data output bus addressed by ADDRA.
DOB	Output	See Configuration Table below.	Data output bus addressed by ADDRB.
DIA	Input	See Configuration Table below.	Data input bus addressed by ADDRA.
DIB	Input	See Configuration Table below.	Data input bus addressed by ADDRB.
ADDRA, ADDRB	Input	See Configuration Table below.	Address input buses for Port A, B.
WEA, WEB	Input	See Configuration Table below.	Write enable for Port A, B.
ENA, ENB	Input	1	Write/Read enables for Port A, B.
RSTA, RSTB	Input	1	Output registers synchronous reset for Port A, B.
REGCEA, REGCEB	Input	1	Output register clock enable input for Port A, B (valid only when DO_REG=1).
CLKA, CLKB	Input	1	Write/Read clock input for Port A, B.

Port Configuration

This unimacro is a parameterizable version of the primitive, and can be instantiated only. Use this table to correctly configure the unimacro to meet design needs.

WRITE_WIDTH_A/B-DIA/DIB	READ_WIDTH_A/B-DOA/DOB	BRAM_SIZE	ADDRA/B	WEA/B
36 - 19	36 - 19	36Kb	10	4
	18-10		11	
	9 - 5		12	
	4 - 3		13	
	2		14	
	1		15	
18 - 10	36 - 19	36Kb	11	2
	18-10		11	
	9 - 5		12	
	4 - 3		13	
	2		14	
	1		15	

WRITE_WIDTH_A/B-DIA/DIB	READ_WIDTH_A/B-DOA/DOB	BRAM_SIZE	ADDRA/B	WEA/B
9 - 5	36-19	36Kb	12	1
	18-10		12	
	9 - 5		12	
	4 - 3		13	
	2		14	
	1		15	
4 - 3	36-19	36Kb	13	1
	18-10		13	
	9 - 5		13	
	4 - 3		13	
	2		14	
	1		15	
2	36-19	36Kb	14	1
	18-10		14	
	9 - 5		14	
	4 - 3		14	
	2		14	
	1		15	
1	36-19	36Kb	15	1
	18-10		15	
	9 - 5		15	
	4 - 3		15	
	2		15	
	1		15	
18-10	18-10	18Kb	10	2
	9 - 5		11	
	4 - 3		12	
	2		13	
	1		14	
9 - 5	18-10	18Kb	11	1
	9 - 5		11	
	4 - 3		12	
	2		13	
	1		14	

WRITE_WIDTH_A/B-DIA/DIB	READ_WIDTH_A/B-DOA/DOB	BRAM_SIZE	ADDRA/B	WEA/B
4 - 3	18-10	18Kb	12	1
	9 - 5		12	
	4 - 3		12	
	2		13	
	1		14	
2	18-10	18Kb	13	1
	9 - 5		13	
	4 - 3		13	
	2		13	
	1		14	
1	18-10	18Kb	14	1
	9 - 5		14	
	4 - 3		14	
	2		14	
	1		14	

Design Entry Method

This unimacro is a parameterizable version of the primitive, and can be instantiated only. Consult the Port Configuration section to correctly configure this element to meet your design needs.

Instantiation	Yes
Inference	No
CORE Generator™ and wizards	No
Macro support	Recommended

Available Attributes

Attribute(s)	Data Type	Allowed Values	Default	Description
BRAM_SIZE	String	"36Kb", "18Kb"	"18Kb"	Configures RAM as "36Kb" or "18Kb" memory.
DEVICE	String	"7SERIES"	"7SERIES"	Target hardware architecture.
DO_REG	Integer	0, 1	0	A value of 1 enables to the output registers to the RAM enabling quicker clock-to-out from the RAM at the expense of an added clock cycle of read latency. A value of 0 allows a read in one clock cycle but will have slower clock to out timing.
INIT	Hexa-decimal	Any 72-Bit Value	All zeros	Specifies the initial value on the output after configuration.

Attribute(s)	Data Type	Allowed Values	Default	Description
INIT_FILE	String	String representing file name and location.	NONE	Name of file containing initial values.
READ_WIDTH, WRITE_WIDTH	Integer	1 - 72	36	Specifies the size of the DI and DO buses. The following combinations are allowed: • READ_WIDTH = WRITE_WIDTH • If asymmetric, READ_WIDTH and WRITE_WIDTH must be in the ratio of 2, or must be values allowed by the unisim (1, 2, 4, 8, 9, 16, 18, 32, 36)
SIM_COLLISION_CHECK	String	"ALL", "WARNING_ONLY", "GENERATE_X_ONLY", "NONE"	"ALL"	Allows modification of the simulation behavior if a memory collision occurs. The output is affected as follows: • "ALL" - Warning produced and affected outputs/memory location go unknown (X). • "WARNING_ONLY" - Warning produced and affected outputs/memory retain last value. • "GENERATE_X_ONLY" - No warning. However, affected outputs/memory go unknown (X). • "NONE" - No warning and affected outputs/memory retain last value. **Note** Setting this to a value other than "ALL" can allow problems in the design go unnoticed during simulation. Care should be taken when changing the value of this attribute. Please see the *Synthesis and Simulation Design Guide* for more information.
SRVAL A, SRVAL_B	Hexa-decimal	Any 72-Bit Value	All zeroes	Specifies the output value of on the DO port upon the assertion of the synchronous reset (RST) signal.
INIT_00 to INIT_FF	Hexa-decimal	Any 256-Bit Value	All zeroes	Allows specification of the initial contents of the 16Kb or 32Kb data memory array.
INITP_00 to INITP_0F	Hexa-decimal	Any 256-Bit Value	All zeroes	Allows specification of the initial contents of the 2Kb or 4Kb parity data memory array.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
```

```
use UNISIM.vcomponents.all;


-- BRAM_TDP_MACRO: True Dual Port RAM
--                 7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

-- Note -  This Unimacro model assumes the port directions to be "downto".
--         Simulation of this model with "to" in the port directions could lead to erroneous results.

-----------------------------------------------------------------------
-- DATA_WIDTH_A/B | BRAM_SIZE | RAM Depth | ADDRA/B Width | WEA/B Width --
-- ===============|===========|===========|===============|=============--
--     19-36      |  "36Kb"   |    1024   |    10-bit     |    4-bit    --
--     10-18      |  "36Kb"   |    2048   |    11-bit     |    2-bit    --
--     10-18      |  "18Kb"   |    1024   |    10-bit     |    2-bit    --
--      5-9       |  "36Kb"   |    4096   |    12-bit     |    1-bit    --
--      5-9       |  "18Kb"   |    2048   |    11-bit     |    1-bit    --
--      3-4       |  "36Kb"   |    8192   |    13-bit     |    1-bit    --
--      3-4       |  "18Kb"   |    4096   |    12-bit     |    1-bit    --
--        2       |  "36Kb"   |   16384   |    14-bit     |    1-bit    --
--        2       |  "18Kb"   |    8192   |    13-bit     |    1-bit    --
--        1       |  "36Kb"   |   32768   |    15-bit     |    1-bit    --
--        1       |  "18Kb"   |   16384   |    14-bit     |    1-bit    --
-----------------------------------------------------------------------

BRAM_TDP_MACRO_inst : BRAM_TDP_MACRO
generic map (
   BRAM_SIZE => "18Kb", -- Target BRAM, "18Kb" or "36Kb"
   DEVICE => "7SERIES", -- Target Device: "VIRTEX5", "VIRTEX6", "7SERIES", "SPARTAN6"
   DOA_REG => 0, -- Optional port A output register (0 or 1)
   DOB_REG => 0, -- Optional port B output register (0 or 1)
   INIT_A => X"000000000", -- Initial values on A output port
   INIT_B => X"000000000", -- Initial values on B output port
   INIT_FILE => "NONE",
   READ_WIDTH_A => 0,   -- Valid values are 1-36 (19-36 only valid when BRAM_SIZE="36Kb")
   READ_WIDTH_B => 0,   -- Valid values are 1-36 (19-36 only valid when BRAM_SIZE="36Kb")
   SIM_COLLISION_CHECK => "ALL", -- Collision check enable "ALL", "WARNING_ONLY",
                                 -- "GENERATE_X_ONLY" or "NONE"
   SRVAL_A => X"000000000",   -- Set/Reset value for A port output
   SRVAL_B => X"000000000",   -- Set/Reset value for B port output
   WRITE_MODE_A => "WRITE_FIRST", -- "WRITE_FIRST", "READ_FIRST" or "NO_CHANGE"
   WRITE_MODE_B => "WRITE_FIRST", -- "WRITE_FIRST", "READ_FIRST" or "NO_CHANGE"
   WRITE_WIDTH_A => 0, -- Valid values are 1-36 (19-36 only valid when BRAM_SIZE="36Kb")
   WRITE_WIDTH_B => 0, -- Valid values are 1-36 (19-36 only valid when BRAM_SIZE="36Kb")
   -- The following INIT_xx declarations specify the initial contents of the RAM
   INIT_00 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_01 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_02 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_03 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_04 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_05 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_06 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_07 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_08 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_09 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_0A => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_0B => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_0C => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_0D => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_0E => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_0F => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_10 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_11 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_12 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_13 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_14 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_15 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_16 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_17 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_18 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_19 => X"0000000000000000000000000000000000000000000000000000000000000000",
```

```
INIT_1A => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_1B => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_1C => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_1D => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_1E => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_1F => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_20 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_21 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_22 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_23 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_24 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_25 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_26 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_27 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_28 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_29 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_2A => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_2B => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_2C => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_2D => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_2E => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_2F => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_30 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_31 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_32 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_33 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_34 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_35 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_36 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_37 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_38 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_39 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_3A => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_3B => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_3C => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_3D => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_3E => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_3F => X"0000000000000000000000000000000000000000000000000000000000000000",

-- The next set of INIT_xx are valid when configured as 36Kb
INIT_40 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_41 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_42 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_43 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_44 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_45 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_46 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_47 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_48 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_49 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_4A => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_4B => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_4C => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_4D => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_4E => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_4F => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_50 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_51 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_52 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_53 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_54 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_55 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_56 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_57 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_58 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_59 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_5A => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_5B => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_5C => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_5D => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_5E => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_5F => X"0000000000000000000000000000000000000000000000000000000000000000",
```

```
   INIT_60 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_61 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_62 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_63 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_64 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_65 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_66 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_67 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_68 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_69 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_6A => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_6B => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_6C => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_6D => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_6E => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_6F => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_70 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_71 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_72 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_73 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_74 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_75 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_76 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_77 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_78 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_79 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_7A => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_7B => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_7C => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_7D => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_7E => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_7F => X"0000000000000000000000000000000000000000000000000000000000000000",

   -- The next set of INITP_xx are for the parity bits
   INITP_00 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_01 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_02 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_03 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_04 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_05 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_06 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_07 => X"0000000000000000000000000000000000000000000000000000000000000000",

   -- The next set of INIT_xx are valid when configured as 36Kb
   INITP_08 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_09 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_0A => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_0B => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_0C => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_0D => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_0E => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_0F => X"0000000000000000000000000000000000000000000000000000000000000000")
port map (
   DOA => DOA,       -- Output port-A data, width defined by READ_WIDTH_A parameter
   DOB => DOB,       -- Output port-B data, width defined by READ_WIDTH_B parameter
   ADDRA => ADDRA,   -- Input port-A address, width defined by Port A depth
   ADDRB => ADDRB,   -- Input port-B address, width defined by Port B depth
   CLKA => CLKA,     -- 1-bit input port-A clock
   CLKB => CLKB,     -- 1-bit input port-B clock
   DIA => DIA,       -- Input port-A data, width defined by WRITE_WIDTH_A parameter
   DIB => DIB,       -- Input port-B data, width defined by WRITE_WIDTH_B parameter
   ENA => ENA,       -- 1-bit input port-A enable
   ENB => ENB,       -- 1-bit input port-B enable
   REGCEA => REGCEA, -- 1-bit input port-A output register enable
   REGCEB => REGCEB, -- 1-bit input port-B output register enable
   RSTA => RSTA,     -- 1-bit input port-A reset
   RSTB => RSTB,     -- 1-bit input port-B reset
   WEA => WEA,       -- Input port-A write enable, width defined by Port A depth
   WEB => WEB        -- Input port-B write enable, width defined by Port B depth
);

-- End of BRAM_TDP_MACRO_inst instantiation
```

Verilog Instantiation Template

```
// BRAM_TDP_MACRO: True Dual Port RAM
//                 7 Series
// Xilinx HDL Libraries Guide, version 2012.2

//////////////////////////////////////////////////////////////////////////
// DATA_WIDTH_A/B | BRAM_SIZE | RAM Depth | ADDRA/B Width | WEA/B Width //
// ===============|===========|===========|===============|=============//
//     19-36      |  "36Kb"   |    1024   |    10-bit     |    4-bit    //
//     10-18      |  "36Kb"   |    2048   |    11-bit     |    2-bit    //
//     10-18      |  "18Kb"   |    1024   |    10-bit     |    2-bit    //
//      5-9       |  "36Kb"   |    4096   |    12-bit     |    1-bit    //
//      5-9       |  "18Kb"   |    2048   |    11-bit     |    1-bit    //
//      3-4       |  "36Kb"   |    8192   |    13-bit     |    1-bit    //
//      3-4       |  "18Kb"   |    4096   |    12-bit     |    1-bit    //
//        2       |  "36Kb"   |   16384   |    14-bit     |    1-bit    //
//        2       |  "18Kb"   |    8192   |    13-bit     |    1-bit    //
//        1       |  "36Kb"   |   32768   |    15-bit     |    1-bit    //
//        1       |  "18Kb"   |   16384   |    14-bit     |    1-bit    //
//////////////////////////////////////////////////////////////////////////

BRAM_TDP_MACRO #(
   .BRAM_SIZE("18Kb"), // Target BRAM: "18Kb" or "36Kb"
   .DEVICE("7SERIES"), // Target device: "7SERIES"
   .DOA_REG(0),        // Optional port A output register (0 or 1)
   .DOB_REG(0),        // Optional port B output register (0 or 1)
   .INIT_A(36'h0000000),  // Initial values on port A output port
   .INIT_B(36'h00000000), // Initial values on port B output port
   .INIT_FILE ("NONE"),
   .READ_WIDTH_A (0),   // Valid values are 1-36 (19-36 only valid when BRAM_SIZE="36Kb")
   .READ_WIDTH_B (0),   // Valid values are 1-36 (19-36 only valid when BRAM_SIZE="36Kb")
   .SIM_COLLISION_CHECK ("ALL"), // Collision check enable "ALL", "WARNING_ONLY",
                                 //   "GENERATE_X_ONLY" or "NONE"
   .SRVAL_A(36'h00000000), // Set/Reset value forr port A output
   .SRVAL_B(36'h00000000), // Set/Reset value forr port B output
   .WRITE_MODE_A("WRITE_FIRST"), // "WRITE_FIRST", "READ_FIRST", or "NO_CHANGE"
   .WRITE_MODE_B("WRITE_FIRST"), // "WRITE_FIRST", "READ_FIRST", or "NO_CHANGE"
   .WRITE_WIDTH_A(0), // Valid values are 1-36 (19-36 only valid when BRAM_SIZE="36Kb")
   .WRITE_WIDTH_B(0), // Valid values are 1-36 (19-36 only valid when BRAM_SIZE="36Kb")
   .INIT_00(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_01(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_02(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_03(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_04(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_05(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_06(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_07(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_08(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_09(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_0A(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_0B(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_0C(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_0D(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_0E(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_0F(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_10(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_11(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_12(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_13(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_14(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_15(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_16(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_17(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_18(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_19(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_1A(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_1B(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_1C(256'h0000000000000000000000000000000000000000000000000000000000000000),
```

```
.INIT_1D(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_1E(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_1F(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_20(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_21(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_22(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_23(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_24(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_25(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_26(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_27(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_28(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_29(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_2A(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_2B(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_2C(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_2D(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_2E(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_2F(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_30(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_31(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_32(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_33(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_34(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_35(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_36(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_37(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_38(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_39(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_3A(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_3B(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_3C(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_3D(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_3E(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_3F(256'h0000000000000000000000000000000000000000000000000000000000000000),

// The next set of INIT_xx are valid when configured as 36Kb
.INIT_40(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_41(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_42(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_43(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_44(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_45(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_46(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_47(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_48(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_49(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_4A(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_4B(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_4C(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_4D(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_4E(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_4F(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_50(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_51(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_52(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_53(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_54(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_55(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_56(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_57(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_58(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_59(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_5A(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_5B(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_5C(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_5D(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_5E(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_5F(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_60(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_61(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_62(256'h0000000000000000000000000000000000000000000000000000000000000000),
```

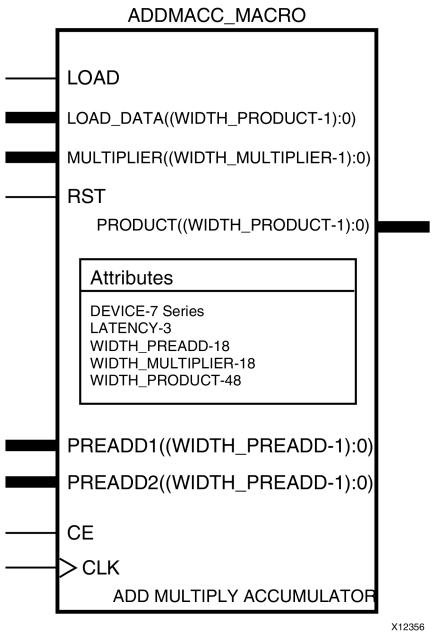
```
   .INIT_63(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_64(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_65(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_66(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_67(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_68(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_69(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_6A(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_6B(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_6C(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_6D(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_6E(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_6F(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_70(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_71(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_72(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_73(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_74(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_75(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_76(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_77(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_78(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_79(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_7A(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_7B(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_7C(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_7D(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_7E(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_7F(256'h0000000000000000000000000000000000000000000000000000000000000000),

   // The next set of INITP_xx are forr the parity bits
   .INIT_FF(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_00(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_01(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_02(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_03(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_04(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_05(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_06(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_07(256'h0000000000000000000000000000000000000000000000000000000000000000),

   // The next set of INITP_xx are valid when configured as 36Kb
   .INITP_08(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_09(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_0A(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_0B(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_0C(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_0D(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_0E(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_0F(256'h0000000000000000000000000000000000000000000000000000000000000000)
) BRAM_TDP_MACRO_inst (
   .DOA(DOA),       // Output port-A data, width defined by READ_WIDTH_A parameter
   .DOB(DOB),       // Output port-B data, width defined by READ_WIDTH_B parameter
   .ADDRA(ADDRA),   // Input port-A address, width defined by Port A depth
   .ADDRB(ADDRB),   // Input port-B address, width defined by Port B depth
   .CLKA(CLKA),     // 1-bit input port-A clock
   .CLKB(CLKB),     // 1-bit input port-B clock
   .DIA(DIA),       // Input port-A data, width defined by WRITE_WIDTH_A parameter
   .DIB(DIB),       // Input port-B data, width defined by WRITE_WIDTH_B parameter
   .ENA(ENA),       // 1-bit input port-A enable
   .ENB(ENB),       // 1-bit input port-B enable
   .REGCEA(REGCEA), // 1-bit input port-A output register enable
   .REGCEB(REGCEB), // 1-bit input port-B output register enable
   .RSTA(RSTA),     // 1-bit input port-A reset
   .RSTB(RSTB),     // 1-bit input port-B reset
   .WEA(WEA),       // Input port-A write enable, width defined by Port A depth
   .WEB(WEB)        // Input port-B write enable, width defined by Port B depth
);

// End of BRAM_TDP_MACRO_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

ADDMACC_MACRO

Macro: Adder/Multiplier/Accumulator



Introduction

ADDMACC_MACRO simplifies the instantiation of the DSP48 block when used as a pre-add, multiply accumulate function. It features parameterizable input and output widths and latency that ease the integration of DSP48 block into HDL.

Port Description

Name	Direction	Width	Function
PRODUCT	Output	Variable width, equals the value of the WIDTH_A attibute plus the value of the WIDTH_B attribute.	Primary data output.
PREADD1	Input	Variable, see WIDTH_PREADD attribute.	Preadder data input.
PREADD2	Input	Variable, see WIDTH_PREADD attribute.	Preadder data input
MULTIPLIER	Input	Variable, see WIDTH_MULTIPLIER attribute.	Multiplier data input
CARRYIN	Input	1	Carry input
CLK	Input	1	Clock
CE	Inupt	1	Clock enable

Name	Direction	Width	Function
LOAD	Input	1	Load
LOAD_DATA	Input	Variable, see WIDTH_PRODUCT attribute.	In a DSP slice, when LOAD is asserted, loads P with A*B+LOAD_DATA.
RST	Input	1	Synchronous Reset

Design Entry Method

This unimacro is a parameterizable version of the primitive, and can be instantiated only.

Instantiation	Yes
Inference	No
CORE Generator™ and wizards	No
Macro support	Recommended

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
WIDTH_PREADD	Integer	1 to 24	24	Controls the width of PREADD1 and PREADD2 inputs.
WIDTH_MULTIPLIER	Integer	1 to 18	18	Controls the width of MULTIPLIER input.
WIDTH_PRODUCT	Integer	1 to 48	48	Controls the width of MULTIPLIER output.
LATENCY	Integer	0, 1, 2, 3, 4	3	Number of pipeline registers • 1 - MREG == 1 • 2 - AREG == BREG == 1 and MREG == 1 or MREG == 1 and PREG == 1 • 3 - AREG == BREG == 1 and MREG == 1 and PREG == 1 • 4 - AREG == BREG == 2 and MREG == 1 and PREG == 1
DEVICE	String	"7SERIES"	"7SERIES"	Target hardware architecture.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- ADDMACC_MACRO: Add and Multiple Accumulate Function implemented in a DSP48E
--                7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

ADDMACC_MACRO_inst : ADDMACC_MACRO
generic map (
   DEVICE => "7SERIES",  -- Target Device: "7SERIES", "VIRTEX6", "SPARTAN6"
   LATENCY => 4,         -- Desired clock cycle latency, 1-4
   WIDTH_PREADD => 25,   -- Pre-Adder input bus width, 1-25
   WIDTH_MULTIPLIER => 18, -- Multiplier input bus width, 1-18
   WIDTH_PRODUCT => 48)    -- MACC output width, 1-48
port map (
   PRODUCT => PRODUCT,     -- MACC result output, width defined by WIDTH_PRODUCT generic
   MULTIPLIER => MULTIPLIER, -- Multiplier data input, width determined by WIDTH_MULTIPLIER generic
   PREADDER1 => PREADDER1,   -- Preadder data input, width determined by WIDTH_PREADDER generic
   PREADDER2 => PREADDER2,   -- Preadder data input, width determined by WIDTH_PREADDER generic
   CARRYIN => CARRYIN, -- 1-bit carry-in input
   CE => CE,       -- 1-bit input clock enable
   CLK => CLK,     -- 1-bit clock input
   LOAD => LOAD, -- 1-bit accumulator load input
   LOAD_DATA => LOAD_DATA, -- Accumulator load data input, width defined by WIDTH_PRODUCT generic
   RST => RST    -- 1-bit input active high synchronous reset
);
-- End of ADDMACC_MACRO_inst instantiation
```

Verilog Instantiation Template

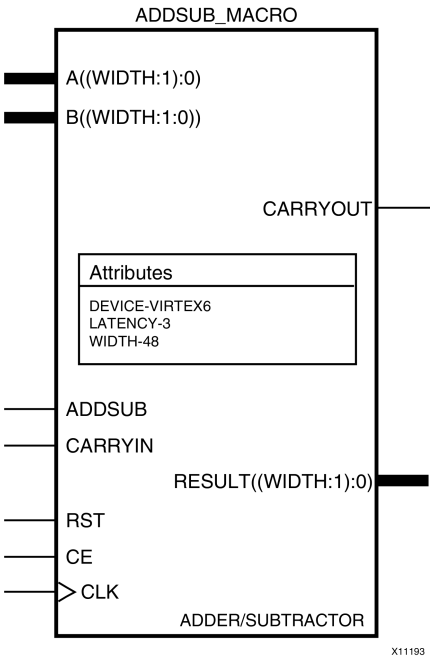
```
// ADDMACC_MACRO: Variable width & latency - Pre-Add -> Multiplier -> Accumulate
//                function implemented in a DSP48E
//                7 Series
// Xilinx HDL Libraries Guide, version 2012.2

ADDMACC_MACRO #(
   .DEVICE("7SERIES"),    // Target Device: "7SERIES"
   .LATENCY(4),           // Desired clock cycle latency, 0-4
   .WIDTH_PREADD(25),     // Pre-adder input width, 1-25
   .WIDTH_MULTIPLIER(18), // Multiplier input width, 1-18
   .WIDTH_PRODUCT(48)     // MACC output width, 1-48
) ADDMACC_MACRO_inst (
   .PRODUCT(PRODUCT),   // MACC result output, width defined by WIDTH_PRODUCT parameter
   .CARRYIN(CARRYIN),   // 1-bit carry-in input
   .CLK(CLK),           // 1-bit clock input
   .CE(CE),             // 1-bit clock enable input
   .LOAD(LOAD),         // 1-bit accumulator load input
   .LOAD_DATA(LOAD_DATA),   // Accumulator load data input, width defined by WIDTH_PRODUCT parameter
   .MULTIPLIER(MULTIPLIER), // Multiplier data input, width defined by WIDTH_MULTIPLIER parameter
   .PREADD2(PREADD2),   // Preadder data input, width defined by WIDTH_PREADD parameter
   .PREADD1(PREADD1),   // Preadder data input, width defined by WIDTH_PREADD parameter
   .RST(RST)            // 1-bit active high synchronous reset
);

// End of ADDMACC_MACRO_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

ADDSUB_MACRO

Macro: Adder/Subtractor



Introduction

ADDSUB_MACRO simplifies the instantiation of the DSP48 block when used as a simple adder/subtractor. It features parameterizable input and output widths and latency that ease the integration of the DSP48 block into HDL.

Port Description

Name	Direction	Width (Bits)	Function
CARRYOUT	Output	1	Carry Out
RESULT	Output	Variable, see WIDTH attrribute.	Data output bus addressed by RDADDR.
ADDSUB	Input	1	When high, RESULT is an addition. When low, RESULT is a subtraction.
A	Input	Variable, see WIDTH attribute.	Data input to add/sub.
B	Input	Variable, see WIDTH attribute.	Data input to add/sub
CE	Input	1	Clock Enable
CARRYIN	Input	1	Carry In
CLK	Input	1	Clock
RST	Input	1	Synchronous Reset

Design Entry Method

This unimacro is a parameterizable version of the primitive, and can be instantiated only.

Instantiation	Yes
Inference	No
CORE Generator™ and wizards	No
Macro support	Recommended

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
DEVICE	String	"7SERIES"	"7SERIES"	Target hardware architecture.
LATENCY	Integer	0, 1, 2	2	Number of pipeline registers. • 1 - PREG == 1 • 2 - AREG == BREG == CREG == PREG
WIDTH	Integer	1-48	48	A, B, and RESULT port width; internal customers can override B and RESULT port widths using other parameters
WIDTH_RESULT	Integer	1-48	48	Result port width override.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- ADDSUB_MACRO: Variable width & latency - Adder / Subtractor implemented in a DSP48E
--               7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

ADDSUB_MACRO_inst : ADDSUB_MACRO
generic map (
   DEVICE => "7SERIES", -- Target Device: "VIRTEX5", "7SERIES", "SPARTAN6"
   LATENCY => 2,        -- Desired clock cycle latency, 0-2
   WIDTH => 48)         -- Input / Output bus width, 1-48
port map (
   CARRYOUT => CARRYOUT, -- 1-bit carry-out output signal
   RESULT => RESULT,     -- Add/sub result output, width defined by WIDTH generic
   A => A,               -- Input A bus, width defined by WIDTH generic
   ADD_SUB => ADD_SUB,   -- 1-bit add/sub input, high selects add, low selects subtract
   B => B,               -- Input B bus, width defined by WIDTH generic
   CARRYIN => CARRYIN,   -- 1-bit carry-in input
   CE => CE,             -- 1-bit clock enable input
   CLK =>CLK,           -- 1-bit clock input
   RST => RST            -- 1-bit active high synchronous reset
);
-- End of ADDSUB_MACRO_inst instantiation
```

Verilog Instantiation Template

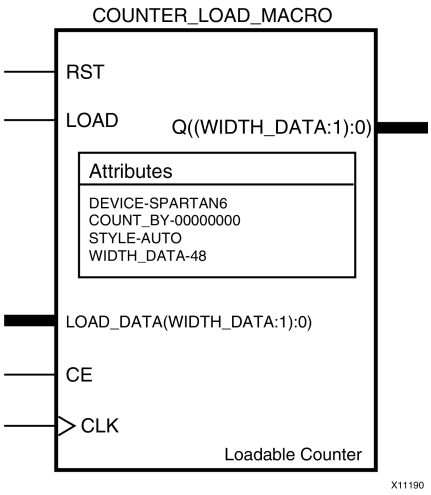
```
// ADDSUB_MACRO: Variable width & latency - Adder / Subtracter implemented in a DSP48E
//               7 Series
// Xilinx HDL Libraries Guide, version 2012.2

ADDSUB_MACRO #(
   .DEVICE("7SERIES"), // Target Device: "7SERIES"
   .LATENCY(2),        // Desired clock cycle latency, 0-2
   .WIDTH(48)          // Input / output bus width, 1-48
) ADDSUB_MACRO_inst (
   .CARRYOUT(CARRYOUT), // 1-bit carry-out output signal
   .RESULT(RESULT),     // Add/sub result output, width defined by WIDTH parameter
   .A(A),               // Input A bus, width defined by WIDTH parameter
   .ADD_SUB(ADD_SUB),   // 1-bit add/sub input, high selects add, low selects subtract
   .B(B),               // Input B bus, width defined by WIDTH parameter
   .CARRYIN(CARRYIN),   // 1-bit carry-in input
   .CE(CE),             // 1-bit clock enable input
   .CLK(CLK),           // 1-bit clock input
   .RST(RST)            // 1-bit active high synchronous reset
);

// End of ADDSUB_MACRO_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

COUNTER_LOAD_MACRO

Macro: Loadable Counter



Introduction

COUNTER_LOAD_MACRO simplifies the instantiation of the DSP48 block when used as dynamic loading up/down counter. It features parameterizable output width and count by values that ease the integration of the DSP48 block into HDL.

Port Description

Name	Direction	Width	Function
Q	Output	Variable, see WIDTH_DATA attribute.	Counter output.
CE	Input	1	Clock Enable.
CLK	Input	1	Clock.
LOAD	Input	Variable, see WIDTH_DATA attribute.	When asserted, loads the counter from LOAD_DATA (two-clock latency).
LOAD_DATA	Input	Variable, see WIDTH_DATA attribute.	In a DSP slice, asserting the LOAD pin will force this data into the P register with a latency of 2 clocks.
DIRECTION	Input	1	High for Up and Low for Down (two-clock latency)
RST	Input	1	Synchronous Reset

Design Entry Method

This unimacro is a parameterizable version of the primitive, and can be instantiated only.

Instantiation	Yes
Inference	No
CORE Generator™ and wizards	No
Macro support	Recommended

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
DEVICE	String	"7SERIES"	"7SERIES"	Target hardware architecture.
COUNT_BY	Hexa-decimal	Any 48 bit value.	000000000001	Count by *n*; takes precedence over WIDTH_DATA.
WIDTH_DATA	Integer	1-48	48	Specifies counter width.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- COUNTER_LOAD_MACRO: Loadable variable counter implemented in a DSP48E
--                     7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

COUNTER_LOAD_MACRO_inst : COUNTER_LOAD_MACRO
generic map (
   COUNT_BY => X"000000000001", -- Count by value
   DEVICE => "7SERIES",         -- Target Device: "VIRTEX5", "7SERIES", "SPARTAN6"
   WIDTH_DATA => 48)            -- Counter output bus width, 1-48
port map (
   Q => Q,                 -- Counter output, width determined by WIDTH_DATA generic
   CLK => CLK,             -- 1-bit clock input
   CE => CE,               -- 1-bit clock enable input
   DIRECTION => DIRECTION, -- 1-bit up/down count direction input, high is count up
   LOAD => LOAD,           -- 1-bit active high load input
   LOAD_DATA => LOAD_DATA, -- Counter load data, width determined by WIDTH_DATA generic
   RST => RST              -- 1-bit active high synchronous reset
);
-- End of COUNTER_LOAD_MACRO_inst instantiation
```

Verilog Instantiation Template

```
// COUNTER_LOAD_MACRO: Loadable variable counter implemented in a DSP48E
//                     7 Series
// Xilinx HDL Libraries Guide, version 2012.2

COUNTER_LOAD_MACRO #(
   .COUNT_BY(48'h000000000001), // Count by value
   .DEVICE("7SERIES"), // Target Device: "7SERIES"
   .WIDTH_DATA(48)     // Counter output bus width, 1-48
) COUNTER_LOAD_MACRO_inst (
   .Q(Q),                 // Counter output, width determined by WIDTH_DATA parameter
   .CLK(CLK),             // 1-bit clock input
   .CE(CE),               // 1-bit clock enable input
   .DIRECTION(DIRECTION), // 1-bit up/down count direction input, high is count up
   .LOAD(LOAD),           // 1-bit active high load input
```

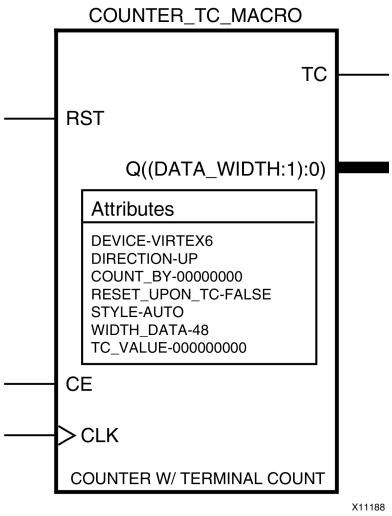
```
   .LOAD_DATA(LOAD_DATA), // Counter load data, width determined by WIDTH_DATA parameter
   .RST(RST)              // 1-bit active high synchronous reset
);

// End of COUNTER_LOAD_MACRO_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

COUNTER_TC_MACRO

Macro: Counter with Terminal Count



Introduction

COUNTER_TC_MACRO simplifies the instantiation of the DSP48 block when used as a terminal count, up/down counter. It features parameterizable output width, terminal count values, count by and count direction in order to ease the integration of DSP48 block into HDL.

Port Description

Name	Direction	Width (Bits)	Function
TC	Output	1	Terminal count goes high when TC_VALUE is reached
Q	Output	Variable, see WIDTH_DATA attribute.	Counter output
CE	Input	1	Clock Enable
CLK	Input	1	Clock
RST	Input	1	Synchronous Reset

Design Entry Method

This unimacro is a parameterizable version of the primitive, and can be instantiated only.

Instantiation	Yes
Inference	No
CORE Generator™ and wizards	No
Macro support	Recommended

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
RESET_UPON_TC	Boolean	True, False	False	Specifies whether to reset the counter upon reaching terminal count
DEVICE	String	"7SERIES"	"7SERIES"	Target hardware architecture.
DIRECTION	String	"UP", "DOWN"	"UP"	Count up versus count down.
COUNT_BY	Hexa-decimal	Any 48 bit value	000000000001	Count by *n*; takes precedence over WIDTH_DATA
TC_VALUE	Hexa-decima	Any 48 bit value	All zeros	Terminal count value.
WIDTH_DATA	Integer	1-48	48	Specifies counter width.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- COUNTER_TC_MACRO: Counter with terminal count implemented in a DSP48E
--                   7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

COUNTER_TC_MACRO_inst : COUNTER_TC_MACRO
generic map (
   COUNT_BY => X"000000000001", -- Count by value
   DEVICE => "7SERIES",         -- Target Device: "VIRTEX5", "7SERIES"
   DIRECTION => "UP",            -- Counter direction "UP" or "DOWN"
   RESET_UPON_TC => "FALSE",      -- Reset counter upon terminal count, TRUE or FALSE
   TC_VALUE => X"000000000000", -- Terminal count value
   WIDTH_DATA => 48)            -- Counter output bus width, 1-48
port map (
   Q => Q,         -- Counter output, width determined by WIDTH_DATA generic
   TC => TC,       -- 1-bit terminal count output, high = terminal count is reached
   CLK => CLK,     -- 1-bit clock input
   CE => CE,       -- 1-bit clock enable input
   RST => RST       -- 1-bit active high synchronous reset
);
-- End of COUNTER_TC_MACRO_inst instantiation
```

Verilog Instantiation Template

```
// COUNTER_TC_MACRO: Counter with terminal count implemented in a DSP48E
//                   7 Series
// Xilinx HDL Libraries Guide, version 2012.2

COUNTER_TC_MACRO #(
   .COUNT_BY(48'h000000000001), // Count by value
   .DEVICE("7SERIES"),          // Target Device: "7SERIES"
   .DIRECTION("UP"),            // Counter direction, "UP" or "DOWN"
   .RESET_UPON_TC("FALSE"), // Reset counter upon terminal count, "TRUE" or "FALSE"
   .TC_VALUE(48'h000000000000), // Terminal count value
   .WIDTH_DATA(48)              // Counter output bus width, 1-48
) COUNTER_TC_MACRO_inst (
   .Q(Q),     // Counter output bus, width determined by WIDTH_DATA parameter
   .TC(TC),   // 1-bit terminal count output, high = terminal count is reached
```

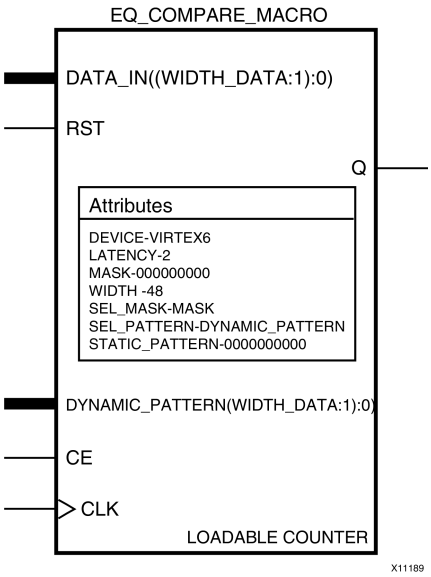
```
   .CLK(CLK), // 1-bit positive edge clock input
   .CE(CE),   // 1-bit active high clock enable input
   .RST(RST)  // 1-bit active high synchronous reset
);

// End of COUNTER_TC_MACRO_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

EQ_COMPARE_MACRO

Macro: Equality Comparator



Introduction

EQ_COMPARE_MACRO simplifies the instantiation of the DSP48 block when used as an equality comparator. It features parameterizable input and output widths, latencies, mask, and input sources that ease the integration of the DSP48 block into HDL.

Port Description

Name	Direction	Width	Function
Q	Output	1	Active High pattern detection. Detects match of DATA_IN and the selected DYNAMIC_PATTERN gated by the MASK. Result arrives on the same cycle as P.
DATA_IN	Input	Variable width, equals the value of the WIDTH attribute.	Input data to be compared.
DYNAMIC_PATTERN	Input	Variable width, equals the value of the WIDTH attribute.	Dynamic data to be compared to DATA_IN.
CLK	Input	1	Clock.
CE	Inupt	1	Clock enable.
RST	Input	1	Synchronous Reset.

Design Entry Method

This unimacro is a parameterizable version of the primitive, and can be instantiated only.

Instantiation	Yes
Inference	No
CORE Generator™ and wizards	No
Macro support	Recommended

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
DEVICE	String	"7SERIES"	"7SERIES"	Target hardware architecture.
SEL_PATTERN	Integer	1 to 24	24	Controls the width of PREADD1 and PREADD2 inputs.
MASK	Hexa-decimal	48 hex	all zeros	Mask to be used for pattern detector.
STATIC_PATTERN	Hexa-decimal	48 hex	all zeros	Pattern to be used for pattern detector.
SEL_MASK	String	"MASK", "DYNAMIC_PATTERN"	"MASK"	Selects whether to use the static MASK or the C input for the mask of the pattern detector.
WIDTH	Integer	1 to 48	48	Width of DATA_IN and DYNAMIC_PATTERN.
LATENCY	Integer	0, 1, 2, 3	2	Number of pipeline registers. • 1: QREG == 1 • 2: AREG == BREG == CREG == QREG == 1 • 3: AREG == BREG == 2 and CREG == QREG == 1

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- EQ_COMPARE_MACRO: Equality Comparator implemented in a DSP48E
--                   7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

EQ_COMPARE_MACRO_inst : EQ_COMPARE_MACRO
generic map (
   DEVICE => "7SERIES",         -- Target Device: "VIRTEX5", "7SERIES"
   LATENCY => 2,                -- Desired clock cycle latency, 0-2
   MASK => X"000000000000",     -- Select bits to be masked, must set
                                -- SEL_MASK = "MASK"
   SEL_MASK => "MASK",          -- "MASK" = use MASK generic,
                                -- "DYNAMIC_PATTERN = use DYNAMIC_PATTERN input bus
   SEL_PATTERN => "DYNAMIC_PATTERN", -- "DYNAMIC_PATTERN" = use DYNAMIC_PATTERN input bus
                                   -- "STATIC_PATTERN" = use STATIC_PATTERN generic
   STATIC_PATTERN => X"000000000000", -- Specify static pattern,
                                    -- must set SEL_PATTERN = "STATIC_PATTERN
```

```
   WIDTH => 48)            -- Comparator output bus width, 1-48
port map (
   Q => Q,         -- 1-bit output indicating a match
   CE => CE,       -- 1-bit active high input clock enable input
   CLK => CLK,     -- 1-bit positive edge clock input
   DATA_IN => DATA_IN, -- Input Data Bus, width determined by WIDTH generic
   DYNAMIC_PATTERN, => DYNAMIC_PATTERN, -- Input Dynamic Match/Mask Bus, width determined by WIDTH generic
   RST => RST       -- 1-bit input active high reset
);
-- End of EQ_COMPARE_MACRO_inst instantiation
```

Verilog Instantiation Template

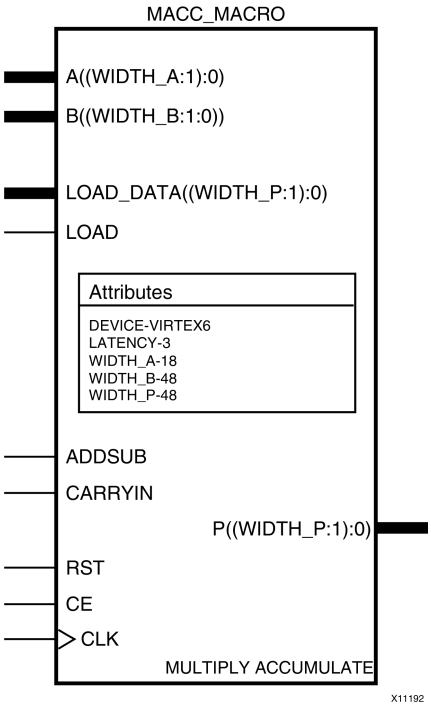
```
// EQ_COMPARE_MACRO: Equality Comparator implemented in a DSP48E
//                   7 Series
// Xilinx HDL Libraries Guide, version 2012.2

EQ_COMPARE_MACRO #(
   .DEVICE("7SERIES"),       // Target Device: "7SERIES"
   .LATENCY(2),              // Desired clock cycle latency, 0-2
   .MASK(48'h000000000000),  // Select bits to be masked, must set SEL_MASK="MASK"
   .SEL_MASK("MASK"),        // "MASK" = use MASK parameter,
                             //   "DYNAMIC_PATTERN" = use DYNAMIC_PATTERN input bus
   .SEL_PATTERN("STATIC_PATTERN"), // "STATIC_PATTERN" = use STATIC_PATTERN parameter,
                                   //   "DYNAMIC_PATTERN = use DYNAMIC_PATTERN input bus
   .STATIC_PATTERN(48'h000000000000), // Specify static pattern, must set SEL_PATTERN = "STATIC_PATTERN"
   .WIDTH(48)                // Comparator output bus width, 1-48
) EQ_COMPARE_MACRO_inst (
   .Q(Q),     // 1-bit output indicating a match
   .CE(CE),   // 1-bit active high input clock enable
   .CLK(CLK), // 1-bit positive edge clock input
   .DATA_IN(DATA_IN), // Input Data Bus, width determined by WIDTH parameter
   .DYNAMIC_PATTERN(DYNAMIC_PATTERN), // Input Dynamic Match/Mask Bus, width determined by WIDTH parameter
   .RST(RST)  // 1-bit input active high reset
);

// End of EQ_COMPARE_MACRO_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

MACC_MACRO

Macro: Multiplier/Accumulator



Introduction

MACC_MACRO simplifies the instantiation of the DSP48 block when used in simple signed multiplier/accumulator mode. It features parameterizable input and output widths and latencies that ease the integration of the DSP48 block into HDL.

Port Description

Name	Direction	Width	Function
P	Output	Variable width, equals the value of the WIDTH_A attribute plus the value of the WIDTH_B attribute.	Primary data output.
A	Input	Variable, see WIDTH_A attribute.	Multiplier data input.
B	Input	Variable, see WIDTH_B attribute.	Multiplier data input.
CARRYIN	Input	1	Carry input.
CE	Input	1	Clock enable.
CLK	Input	1	Clock.
LOAD	Inupt	1	Load.

Name	Direction	Width	Function
LOAD_DATA	Input	Variable width, equals the value of the WIDTH_A attribute plus the value of the WIDTH_B attribute.	In a DSP slice, when LOAD is asserted, loads P with A*B+LOAD_DATA.
RST	Input	1	Synchronous Reset.
ADDSUB	Input	1	High sets accumulator in addition mode; low sets accumulator in subtraction mode.

Design Entry Method

This unimacro is a parameterizable version of the primitive, and can be instantiated only.

Instantiation	Yes
Inference	No
CORE Generator™ and wizards	No
Macro support	Recommended

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
DEVICE	String	"7SERIES"	"7SERIES"	Target hardware architecture.
WIDTH_A	Integer	1 to 25	25	Controls the width of A input.
WIDTH_B	Integer	1 to 18	18	Controls the width of B input.
LATENCY	Integer	0, 1, 2, 3, 4	3	Number of pipeline registers. • 1 - MREG == 1 • 2 - AREG == BREG == 1 and MREG == 1 or MREG == 1 and PREG == 1 • 3 - AREG == BREG == 1 and MREG == 1 and PREG == 1 • 4 - AREG == BREG == 2 and MREG == 1 and PREG == 1

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- MACC_MACRO: Multiple Accumulate Function implemented in a DSP48E
--             7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

MACC_MACRO_inst : MACC_MACRO
generic map (
   DEVICE => "7SERIES",  -- Target Device: "VIRTEX5", "7SERIES", "SPARTAN6"
   LATENCY => 3,         -- Desired clock cycle latency, 1-4
   WIDTH_A => 25,        -- Multiplier A-input bus width, 1-25
   WIDTH_B => 18,        -- Multiplier B-input bus width, 1-18
   WIDTH_P => 48)        -- Accumulator output bus width, 1-48
port map (
   P => P,     -- MACC output bus, width determined by WIDTH_P generic
   A => A,     -- MACC input A bus, width determined by WIDTH_A generic
   ADDSUB => ADDSUB, -- 1-bit add/sub input, high selects add, low selects subtract
   B => B,           -- MACC input B bus, width determined by WIDTH_B generic
   CARRYIN => CARRYIN, -- 1-bit carry-in input to accumulator
   CE => CE,       -- 1-bit active high input clock enable
   CLK => CLK,     -- 1-bit positive edge clock input
   LOAD => LOAD, -- 1-bit active high input load accumulator enable
   LOAD_DATA => LOAD_DATA, -- Load accumulator input data,
                           -- width determined by WIDTH_P generic
   RST => RST    -- 1-bit input active high reset
);

-- End of MACC_MACRO_inst instantiation
```

Verilog Instantiation Template

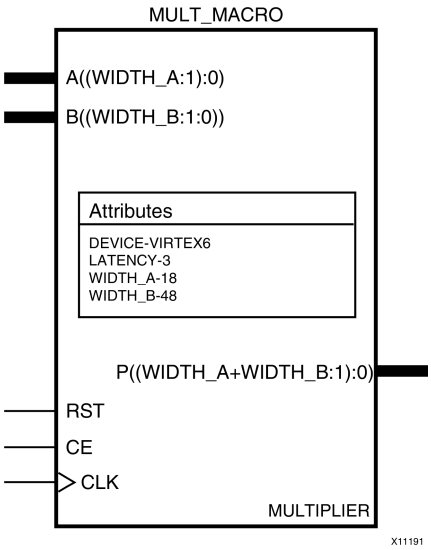
```
// MACC_MACRO: Multiply Accumulate Function implemented in a DSP48E
//             7 Series
// Xilinx HDL Libraries Guide, version 2012.2

MACC_MACRO #(
   .DEVICE("7SERIES"), // Target Device: "7SERIES"
   .LATENCY(3),        // Desired clock cycle latency, 1-4
   .WIDTH_A(25),       // Multiplier A-input bus width, 1-25
   .WIDTH_B(18),       // Multiplier B-input bus width, 1-18
   .WIDTH_P(48)        // Accumulator output bus width, 1-48
) MACC_MACRO_inst (
   .P(P),     // MACC output bus, width determined by WIDTH_P parameter
   .A(A),     // MACC input A bus, width determined by WIDTH_A parameter
   .ADDSUB(ADDSUB), // 1-bit add/sub input, high selects add, low selects subtract
   .B(B),     // MACC input B bus, width determined by WIDTH_B parameter
   .CARRYIN(CARRYIN), // 1-bit carry-in input to accumulator
   .CE(CE),     // 1-bit active high input clock enable
   .CLK(CLK),   // 1-bit positive edge clock input
   .LOAD(LOAD), // 1-bit active high input load accumulator enable
   .LOAD_DATA(LOAD_DATA), // Load accumulator input data, width determined by WIDTH_P parameter
   .RST(RST)    // 1-bit input active high reset
);

// End of MACC_MACRO_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

MULT_MACRO

Macro: Multiplier



Introduction

MULT_MACRO simplifies the instantiation of the DSP48 block when used as a simple signed multiplier. It features parameterizable input and output widths and latencies that ease the integration of the DSP48 block into HDL.

Port Description

Name	Direction	Width	Function
P	Output	Variable width, equals the value of the WIDTH_A attibute plus the value of the WIDTH_B attribute.	Primary data output.
A	Input	Variable, see WIDTH_A attribute.	Multiplier data input.
B	Input	Variable, see WIDTH_B attribute.	Multiplier data input.
CE	Input	1	Clock Enable.
CLK	Input	1	Clock.
RST	Input	1	Synchronous Reset.

Design Entry Method

This unimacro is a parameterizable version of the primitive, and can be instantiated only.

Instantiation	Yes
Inference	No
CORE Generator™ and wizards	No
Macro support	Recommended

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
DEVICE	String	"7SERIES"	"7SERIES"	Target hardware architecture.
WIDTH_A	Integer	1 to 25	25	Controls the width of A input.
WIDTH_B	Integer	1 to 18	18	Controls the width of B input.
LATENCY	Integer	0, 1, 2, 3, 4	3	Number of pipeline registers. • 1 - MREG == 1 • 2 - AREG == BREG == 1 and MREG == 1 or MREG == 1 and PREG == 1 • 3 - AREG == BREG == 1 and MREG == 1 and PREG == 1 • 4 - AREG == BREG == 2 and MREG == 1 and PREG == 1

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- MULT_MACRO: Multiply Function implemented in a DSP48E
--             7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

MULT_MACRO_inst : MULT_MACRO
generic map (
   DEVICE => "7SERIES",     -- Target Device: "VIRTEX5", "7SERIES", "SPARTAN6"
   LATENCY => 3,            -- Desired clock cycle latency, 0-4
   WIDTH_A => 18,           -- Multiplier A-input bus width, 1-25
   WIDTH_B => 18)           -- Multiplier B-input bus width, 1-18
port map (
   P => P,      -- Multiplier output bus, width determined by WIDTH_P generic
   A => A,      -- Multiplier input A bus, width determined by WIDTH_A generic
   B => B,      -- Multiplier input B bus, width determined by WIDTH_B generic
   CE => CE,    -- 1-bit active high input clock enable
   CLK => CLK,  -- 1-bit positive edge clock input
   RST => RST   -- 1-bit input active high reset
);
-- End of MULT_MACRO_inst instantiation
```

Verilog Instantiation Template

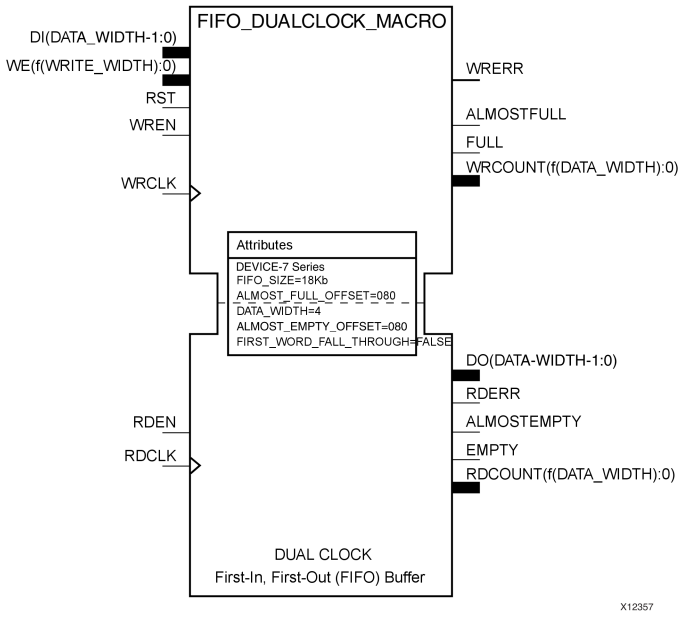
```
// MULT_MACRO: Multiply Function implemented in a DSP48E
//             7 Series
// Xilinx HDL Libraries Guide, version 2012.2

MULT_MACRO #(
   .DEVICE("7SERIES"), // Target Device: "7SERIES"
   .LATENCY(3),        // Desired clock cycle latency, 0-4
   .WIDTH_A(18),       // Multiplier A-input bus width, 1-25
   .WIDTH_B(18)        // Multiplier B-input bus width, 1-18
) MULT_MACRO_inst (
   .P(P),     // Multiplier output bus, width determined by WIDTH_P parameter
   .A(A),     // Multiplier input A bus, width determined by WIDTH_A parameter
   .B(B),     // Multiplier input B bus, width determined by WIDTH_B parameter
   .CE(CE),   // 1-bit active high input clock enable
   .CLK(CLK), // 1-bit positive edge clock input
   .RST(RST)  // 1-bit input active high reset
);

// End of MULT_MACRO_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

FIFO_DUALCLOCK_MACRO

Macro: Dual Clock First-In, First-Out (FIFO) RAM Buffer



Introduction

FPGA devices contain several block RAM memories that can be configured as general-purpose 36 Kb or 18 Kb RAM/ROM memories. Dedicated logic in the block RAM enables you to easily implement FIFOs. The FIFO can be configured as an 18 Kb or 36 Kb memory. This unimacro configures the FIFO for using independent read and writes clocks. Data is read from the FIFO on the rising edge of read clock and written to the FIFO on the rising edge of write clock.

Depending on the offset between read and write clock edges, the Empty, Almost Empty, Full and Almost Full flags can deassert one cycle later. Due to the asynchronous nature of the clocks, the simulation model only reflects the deassertion latency cycles listed in the User Guide.

Port Description

Name	Direction	Width	Function
ALMOSTEMPTY	Output	1	Almost all valid entries in FIFO have been read.
ALMOSTFULL	Output	1	Almost all entries in FIFO memory have been filled.
DO	Output	See Configuration Table below.	Data output bus addressed by ADDR.
EMPTY	Output	1	FIFO is empty.
FULL	Output	1	All entries in FIFO memory are filled.

Name	Direction	Width	Function
RDCOUNT	Output	See Configuration Table below.	FIFO data read pointer.
RDERR	Output	1	When the FIFO is empty, any additional read operation generates an error flag.
WRCOUNT	Output	See Configuration Table below.	FIFO data write pointer.
WRERR	Output	1	When the FIFO is full, any additional write operation generates an error flag.
DI	Input	See Configuration Table below.	Data input bus addressed by ADDR.
RDCLK	Input	1	Clock for Read domain operation.
RDEN	Input	1	Read Enable.
RST	Input	1	Asynchronous reset.
WRCLK	Input	1	Clock for Write domain operation.
WREN	Input	1	Write Enable.

Port Configuration

This unimacro is a parameterizable version of the primitive, and can be instantiated only. Use this table to correctly configure the unimacro to meet design needs.

DATA_WIDTH	FIFO_SIZE	WRCOUNT	RDCOUNT
72 - 37	36 Kb	9	9
36 - 19	36 Kb	10	10
	18 Kb	9	9
18 - 10	36 Kb	11	11
	18 Kb	10	10
9-5	36 Kb	12	12
	18 Kb	11	11
1-4	36 Kb	13	13
	18 Kb	12	12

Design Entry Method

This unimacro is a parameterizable version of the primitive, and can be instantiated only. Consult the Port Configuration section to correctly configure this element to meet your design needs.

Instantiation	Yes
Inference	No
CORE Generator™ and wizards	No
Macro support	Recommended

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
ALMOST_EMPTY_OFFSET	Hexadecimal	13-Bit Value	All zeros	Setting determines the difference between EMPTY and ALMOSTEMPTY conditions. Must be set using hexadecimal notation.
ALMOST_FULL_OFFSET	Hexadecimal	13-Bit Value	All zeros	Setting determines the difference between FULL and ALMOSTFULL conditions. Must be set using hexadecimal notation.
DATA_WIDTH	Integer	1 - 72	4	Width of DI/DO bus.
DEVICE	String	"7SERIES"	"7SERIES"	Target hardware architecture.
FIFO_SIZE	String	"18Kb", "36Kb"	"18Kb"	Configures the FIFO as 18 Kb or 36 Kb memory.
FIRST_WORD_FALL_THROUGH	Boolean	FALSE, TRUE	FALSE	If TRUE, the first word written into the empty FIFO appears at the FIFO output without RDEN asserted.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- FIFO_DUALCLOCK_MACRO: Dual-Clock First-In, First-Out (FIFO) RAM Buffer
--                       7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

-- Note -  This Unimacro model assumes the port directions to be "downto".
--         Simulation of this model with "to" in the port directions could lead to erroneous results.

-----------------------------------------------------------------
-- DATA_WIDTH | FIFO_SIZE | FIFO Depth | RDCOUNT/WRCOUNT Width --
-- ===========|===========|============|=======================--
--   37-72    |  "36Kb"   |     512    |         9-bit         --
--   19-36    |  "36Kb"   |    1024    |        10-bit         --
--   19-36    |  "18Kb"   |     512    |         9-bit         --
--   10-18    |  "36Kb"   |    2048    |        11-bit         --
--   10-18    |  "18Kb"   |    1024    |        10-bit         --
--    5-9     |  "36Kb"   |    4096    |        12-bit         --
--    5-9     |  "18Kb"   |    2048    |        11-bit         --
--    1-4     |  "36Kb"   |    8192    |        13-bit         --
--    1-4     |  "18Kb"   |    4096    |        12-bit         --
-----------------------------------------------------------------

FIFO_DUALCLOCK_MACRO_inst : FIFO_DUALCLOCK_MACRO
```

```
generic map (
   DEVICE => "7SERIES",            -- Target Device: "VIRTEX5", "VIRTEX6", "7SERIES"
   ALMOST_FULL_OFFSET => X"0080",  -- Sets almost full threshold
   ALMOST_EMPTY_OFFSET => X"0080", -- Sets the almost empty threshold
   DATA_WIDTH => 0,   -- Valid values are 1-72 (37-72 only valid when FIFO_SIZE="36Kb")
   FIFO_SIZE => "18Kb",            -- Target BRAM, "18Kb" or "36Kb"
   FIRST_WORD_FALL_THROUGH => FALSE) -- Sets the FIFO FWFT to TRUE or FALSE
port map (
   ALMOSTEMPTY => ALMOSTEMPTY,   -- 1-bit output almost empty
   ALMOSTFULL => ALMOSTFULL,     -- 1-bit output almost full
   DO => DO,                     -- Output data, width defined by DATA_WIDTH parameter
   EMPTY => EMPTY,               -- 1-bit output empty
   FULL => FULL,                 -- 1-bit output full
   RDCOUNT => RDCOUNT,           -- Output read count, width determined by FIFO depth
   RDERR => RDERR,               -- 1-bit output read error
   WRCOUNT => WRCOUNT,           -- Output write count, width determined by FIFO depth
   WRERR => WRERR,               -- 1-bit output write error
   DI => DI,                     -- Input data, width defined by DATA_WIDTH parameter
   RDCLK => RDCLK,               -- 1-bit input read clock
   RDEN => RDEN,                 -- 1-bit input read enable
   RST => RST,                   -- 1-bit input reset
   WRCLK => WRCLK,               -- 1-bit input write clock
   WREN => WREN                  -- 1-bit input write enable
);
-- End of FIFO_DUALCLOCK_MACRO_inst instantiation
```

Verilog Instantiation Template

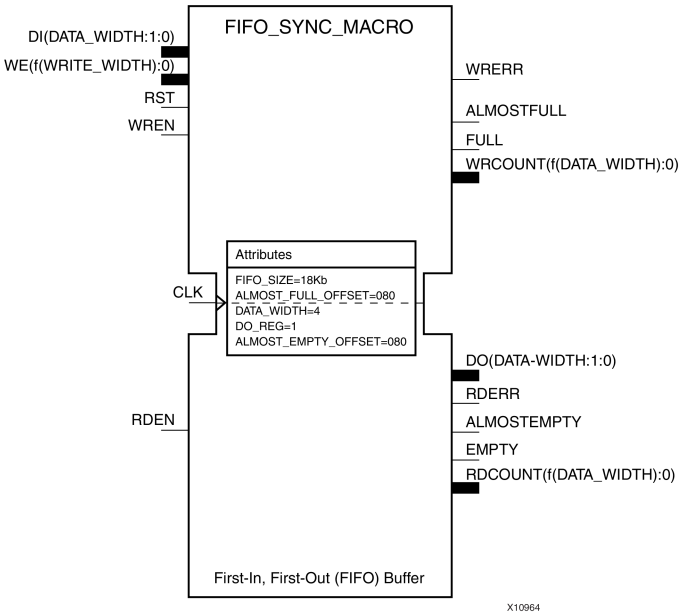
```
// FIFO_DUALCLOCK_MACRO: Dual Clock First-In, First-Out (FIfor) RAM Buffer
//                       7 Series
// Xilinx HDL Libraries Guide, version 2012.2

/////////////////////////////////////////////////////////////////
// DATA_WIDTH | FIFO_SIZE | FIfor Depth | RDCOUNT/WRCOUNT Width //
// ===========|===========|============|=======================//
//   37-72    |  "36Kb"   |     512    |         9-bit         //
//   19-36    |  "36Kb"   |    1024    |        10-bit         //
//   19-36    |  "18Kb"   |     512    |         9-bit         //
//   10-18    |  "36Kb"   |    2048    |        11-bit         //
//   10-18    |  "18Kb"   |    1024    |        10-bit         //
//    5-9     |  "36Kb"   |    4096    |        12-bit         //
//    5-9     |  "18Kb"   |    2048    |        11-bit         //
//    1-4     |  "36Kb"   |    8192    |        13-bit         //
//    1-4     |  "18Kb"   |    4096    |        12-bit         //
/////////////////////////////////////////////////////////////////

FIFO_DUALCLOCK_MACRO  #(
   .ALMOST_EMPTY_OFFSET(9'h080), // Sets the almost empty threshold
   .ALMOST_FULL_OFFSET(9'h080),  // Sets almost full threshold
   .DATA_WIDTH(0),   // Valid values are 1-72 (37-72 only valid when FIFO_SIZE="36Kb")
   .DEVICE("7SERIES"),  // Target device: "7SERIES"
   .FIFO_SIZE ("18Kb"), // Target BRAM: "18Kb" or "36Kb"
   .FIRST_WORD_FALL_THROUGH ("FALSE") // Sets the FIfor FWFT to "TRUE" or "FALSE"
) FIFO_DUALCLOCK_MACRO_inst (
   .ALMOSTEMPTY(ALMOSTEMPTY), // 1-bit output almost empty
   .ALMOSTFULL(ALMOSTFULL),   // 1-bit output almost full
   .DO(DO),                   // Output data, width defined by DATA_WIDTH parameter
   .EMPTY(EMPTY),             // 1-bit output empty
   .FULL(FULL),               // 1-bit output full
   .RDCOUNT(RDCOUNT),         // Output read count, width determined by FIfor depth
   .RDERR(RDERR),             // 1-bit output read error
   .WRCOUNT(WRCOUNT),         // Output write count, width determined by FIfor depth
   .WRERR(WRERR),             // 1-bit output write error
   .DI(DI),                   // Input data, width defined by DATA_WIDTH parameter
   .RDCLK(RDCLK),             // 1-bit input read clock
   .RDEN(RDEN),               // 1-bit input read enable
   .RST(RST),                 // 1-bit input reset
   .WRCLK(WRCLK),             // 1-bit input write clock
   .WREN(WREN)                // 1-bit input write enable
);

// End of FIFO_DUALCLOCK_MACRO_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

FIFO_SYNC_MACRO

Macro: Synchronous First-In, First-Out (FIFO) RAM Buffer



Introduction

FPGA devices contain several block RAM memories that can be configured as general-purpose 36Kb or 18Kb RAM/ROM memories. Dedicated logic in the block RAM enables you to easily implement FIFOs. The FIFO can be configured as an 18 Kb or 36 Kb memory. This unimacro configures the FIFO such that it uses one clock for reading as well as writing.

Port Description

Name	Direction	Width	Function
ALMOSTEMPTY	Output	1	Almost all valid entries in FIFO have been read.
ALMOSTFULL	Output	1	Almost all entries in FIFO memory have been filled.
DO	Output	See Configuration Table.	Data output bus addressed by ADDR.
EMPTY	Output	1	FIFO is empty.
FULL	Output	1	All entries in FIFO memory are filled.
RDCOUNT	Output	See Configuration Table below.	FIFO data read pointer.
RDERR	Output	1	When the FIFO is empty, any additional read operation generates an error flag.

Name	Direction	Width	Function
WRCOUNT	Output	See Configuration Table.	FIFO data write pointer.
WRERR	Output	1	When the FIFO is full, any additional write operation generates an error flag.
CLK	Input	1	Clock for Read/Write domain operation.
DI	Input	See Configuration Table.	Data input bus addressed by ADDR.
RDEN	Input	1	Read Enable
RST	Input	1	Asynchronous reset.
WREN	Input	1	Write Enable

Port Configuration

This unimacro is a parameterizable version of the primitive, and can be instantiated only. Use this table to correctly configure the unimacro to meet design needs.

DATA_WIDTH	FIFO_SIZE	WRCOUNT	RDCOUNT
72 - 37	36Kb	9	9
36 - 19	36Kb	10	10
	18Kb	9	9
18 - 10	36Kb	11	11
	18Kb	10	10
9-5	36Kb	12	12
	18Kb	11	11
1-4	36Kb	13	13
	18Kb	12	12

Design Entry Method

This unimacro is a parameterizable version of the primitive, and can be instantiated only. Consult the Port Configuration section to correctly configure this element to meet your design needs.

Instantiation	Yes
Inference	No
CORE Generator™ and wizards	No
Macro support	Recommended

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
ALMOST_EMPTY_OFFSET	Hexadecimal	Any 13-Bit Value	All zeros	Setting determines the difference between EMPTY and ALMOSTEMPTY conditions. Must be set using hexadecimal notation.
ALMOST_FULL_OFFSET	Hexadecimal	Any 13-Bit Value	All zeros	Setting determines the difference between FULL and ALMOSTFULL conditions. Must be set using hexadecimal notation.
DATA_WIDTH	Integer	1 - 72	4	Width of DI/DO bus.
DEVICE	String	"7SERIES"	"7SERIES"	Target hardware architecture.
DO_REG	Binary	0,1	1	DO_REG must be set to 0 for flags and data to follow a standard synchronous FIFO operation. When DO_REG is set to 1, effectively a pipeline register is added to the output of the synchronous FIFO. Data then has a one clock cycle latency. However, the clock-to-out timing is improved.
FIFO_SIZE	String	18Kb, 36Kb	18Kb	Configures FIFO as 18Kb or 36Kb memory.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- FIFO_SYNC_MACRO: Synchronous First-In, First-Out (FIFO) RAM Buffer
--                  7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

-- Note -  This Unimacro model assumes the port directions to be "downto".
--         Simulation of this model with "to" in the port directions could lead to erroneous results.

-----------------------------------------------------------------
-- DATA_WIDTH | FIFO_SIZE | FIFO Depth | RDCOUNT/WRCOUNT Width --
-- ===========|===========|============|=======================--
--   37-72    |  "36Kb"   |     512    |         9-bit         --
--   19-36    |  "36Kb"   |    1024    |        10-bit         --
--   19-36    |  "18Kb"   |     512    |         9-bit         --
--   10-18    |  "36Kb"   |    2048    |        11-bit         --
--   10-18    |  "18Kb"   |    1024    |        10-bit         --
--    5-9     |  "36Kb"   |    4096    |        12-bit         --
--    5-9     |  "18Kb"   |    2048    |        11-bit         --
--    1-4     |  "36Kb"   |    8192    |        13-bit         --
--    1-4     |  "18Kb"   |    4096    |        12-bit         --
-----------------------------------------------------------------


FIFO_SYNC_MACRO_inst : FIFO_SYNC_MACRO
generic map (
   DEVICE => "7SERIES",            -- Target Device: "VIRTEX5, "VIRTEX6", "7SERIES"
   ALMOST_FULL_OFFSET => X"0080",  -- Sets almost full threshold
   ALMOST_EMPTY_OFFSET => X"0080", -- Sets the almost empty threshold
   DATA_WIDTH => 0,   -- Valid values are 1-72 (37-72 only valid when FIFO_SIZE="36Kb")
   FIFO_SIZE => "18Kb")            -- Target BRAM, "18Kb" or "36Kb"
```

```
port map (
   ALMOSTEMPTY => ALMOSTEMPTY,   -- 1-bit output almost empty
   ALMOSTFULL => ALMOSTFULL,     -- 1-bit output almost full
   DO => DO,                     -- Output data, width defined by DATA_WIDTH parameter
   EMPTY => EMPTY,               -- 1-bit output empty
   FULL => FULL,                 -- 1-bit output full
   RDCOUNT => RDCOUNT,           -- Output read count, width determined by FIFO depth
   RDERR => RDERR,               -- 1-bit output read error
   WRCOUNT => WRCOUNT,           -- Output write count, width determined by FIFO depth
   WRERR => WRERR,               -- 1-bit output write error
   CLK => CLK,                   -- 1-bit input clock
   DI => DI,                     -- Input data, width defined by DATA_WIDTH parameter
   RDEN => RDEN,                 -- 1-bit input read enable
   RST => RST,                   -- 1-bit input reset
   WREN => WREN                  -- 1-bit input write enable
);
-- End of FIFO_SYNC_MACRO_inst instantiation
```

Verilog Instantiation Template

```
// FIFO_SYNC_MACRO: Synchronous First-In, First-Out (FIfor) RAM Buffer
//                  7 Series
// Xilinx HDL Libraries Guide, version 2012.2

//////////////////////////////////////////////////////////////////
// DATA_WIDTH | FIFO_SIZE | FIfor Depth | RDCOUNT/WRCOUNT Width //
// ===========|===========|============|======================//
//   37-72    |  "36Kb"   |     512    |         9-bit         //
//   19-36    |  "36Kb"   |    1024    |        10-bit         //
//   19-36    |  "18Kb"   |     512    |         9-bit         //
//   10-18    |  "36Kb"   |    2048    |        11-bit         //
//   10-18    |  "18Kb"   |    1024    |        10-bit         //
//    5-9     |  "36Kb"   |    4096    |        12-bit         //
//    5-9     |  "18Kb"   |    2048    |        11-bit         //
//    1-4     |  "36Kb"   |    8192    |        13-bit         //
//    1-4     |  "18Kb"   |    4096    |        12-bit         //
//////////////////////////////////////////////////////////////////

FIFO_SYNC_MACRO  #(
   .DEVICE("7SERIES"), // Target Device: "7SERIES"
   .ALMOST_EMPTY_OFFSET(9'h080), // Sets the almost empty threshold
   .ALMOST_FULL_OFFSET(9'h080),  // Sets almost full threshold
   .DATA_WIDTH(0), // Valid values are 1-72 (37-72 only valid when FIFO_SIZE="36Kb")
   .DO_REG(0),     // Optional output register (0 or 1)
   .FIFO_SIZE ("18Kb")  // Target BRAM: "18Kb" or "36Kb"
) FIFO_SYNC_MACRO_inst (
   .ALMOSTEMPTY(ALMOSTEMPTY), // 1-bit output almost empty
   .ALMOSTFULL(ALMOSTFULL),   // 1-bit output almost full
   .DO(DO),                   // Output data, width defined by DATA_WIDTH parameter
   .EMPTY(EMPTY),             // 1-bit output empty
   .FULL(FULL),               // 1-bit output full
   .RDCOUNT(RDCOUNT),         // Output read count, width determined by FIfor depth
   .RDERR(RDERR),             // 1-bit output read error
   .WRCOUNT(WRCOUNT),         // Output write count, width determined by FIfor depth
   .WRERR(WRERR),             // 1-bit output write error
   .CLK(CLK),                 // 1-bit input clock
   .DI(DI),                   // Input data, width defined by DATA_WIDTH parameter
   .RDEN(RDEN),               // 1-bit input read enable
   .RST(RST),                 // 1-bit input reset
   .WREN(WREN)                // 1-bit input write enable
 );

// End of FIFO_SYNC_MACRO_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

XILINX®

Chapter 3

Functional Categories

This section categorizes, by function, the circuit design elements described in detail later in this guide. The elements (*primitives* and *macros*) are listed in alphanumeric order under each functional category.

Advanced

Design Element	Description
GTPE2_CHANNEL	Primitive: Gigabit Transiever
GTPE2_COMMON	Primitive: Gigabit Transiever
XADC	Primitive: Dual 12-Bit 1MSPS Analog-to-Digital Converter

Arithmetic Functions

Design Element	Description
DSP48E1	Primitive: 48-bit Multi-Functional Arithmetic Block

Clock Components

Design Element	Description
BUFG	Primitive: Global Clock Simple Buffer
BUFGCE	Primitive: Global Clock Buffer with Clock Enable
BUFGCE_1	Primitive: Global Clock Buffer with Clock Enable and Output State 1
BUFGCTRL	Primitive: Global Clock Control Buffer
BUFGMUX	Primitive: Global Clock Mux Buffer
BUFGMUX_1	Primitive: Global Clock Mux Buffer with Output State 1
BUFGMUX_CTRL	Primitive: 2-to-1 Global Clock MUX Buffer
BUFH	Primitive: HROW Clock Buffer for a Single Clocking Region
BUFHCE	Primitive: HROW Clock Buffer for a Single Clocking Region with Clock Enable

Design Element	Description
BUFIO	Primitive: Local Clock Buffer for I/O
BUFMR	Primitive: Multi-Region Clock Buffer
BUFMRCE	Primitive: Multi-Region Clock Buffer with Clock Enable
BUFR	Primitive: Regional Clock Buffer for I/O and Logic Resources within a Clock Region
MMCME2_ADV	Primitive: Advanced Mixed Mode Clock Manager
MMCME2_BASE	Primitive: Base Mixed Mode Clock Manager
PLLE2_ADV	Primitive: Advanced Phase Locked Loop (PLL)
PLLE2_BASE	Primitive: Base Phase Locked Loop (PLL)

Config/BSCAN Components

Design Element	Description
BSCANE2	Primitive: Boundary-Scan User Instruction
CAPTUREE2	Primitive: Register Capture
DNA_PORT	Primitive: Device DNA Access Port
EFUSE_USR	Primitive: 32-bit non-volatile design ID
FRAME_ECCE2	Primitive: Configuration Frame Error Correction
ICAPE2	Primitive: Internal Configuration Access Port
STARTUPE2	Primitive: STARTUP Block
USR_ACCESSE2	Primitive: Configuration Data Access

I/O Components

Design Element	Description
DCIRESET	Primitive: Digitally Controlled Impedance Reset Component
IBUF	Primitive: Input Buffer
IBUF_IBUFDISABLE	Primitive: Single-ended Input Buffer with Input Disable
IBUF_INTERMDISABLE	Primitive: Single-ended Input Buffer with Input Termination Disable and Input Disable
IBUFDS	Primitive: Differential Signaling Input Buffer
IBUFDS_DIFF_OUT	Primitive: Differential Signaling Input Buffer With Differential Output
IBUFDS_DIFF_OUT _IBUFDISABLE	Primitive: Input Differential Buffer with Input Disable and Differential Output
IBUFDS_DIFF_OUT _INTERMDISABLE	Primitive: Input Differential Buffer with Input Termination Disable, Input Disable, and Differential Output
IBUFDS_IBUFDISABLE	Primitive: Input Differential Buffer with Input Path Disable
IBUFDS_INTERMDISABLE	Primitive: Input Differential Buffer with Input Termination Disable and Input Disable
IDELAYCTRL	Primitive: IDELAYE2/ODELAYE2 Tap Delay Value Control

Design Element	Description
IDELAYE2	Primitive: Input Fixed or Variable Delay Element
IN_FIFO	Primitive: Input First-In, First-Out (FIFO)
IOBUF	Primitive: Bi-Directional Buffer
IOBUF_DCIEN	Primitive: Bi-Directional Single-ended Buffer with DCI and Input Disable.
IOBUF_INTERMDISABLE	Primitive: Bi-Directional Single-ended Buffer with Input Termination Disable and Input Path Disable
IOBUFDS	Primitive: 3-State Differential Signaling I/O Buffer with Active Low Output Enable
IOBUFDS_DCIEN	Primitive: Bi-Directional Differential Buffer with DCI Enable/Disable and Input Disable
IOBUFDS_DIFF_OUT	Primitive: Differential Bi-directional Buffer with Differential Output
IOBUFDS_DIFF_OUT_DCIEN	Primitive: Bi-Directional Differential Buffer with DCI Disable, Input Disable, and Differential Output
IOBUFDS_DIFF_OUT _INTERMDISABLE	Primitive: Bi-Directional Differential Buffer with Input Termination Disable, Input Disable, and Differential Output
IOBUFDS_INTERMDISABLE	Primitive: Bi-Directional Differential Buffer with Input Termination Disable and Input Disable
ISERDESE2	Primitive: Input SERial/DESerializer with bitslip
KEEPER	Primitive: KEEPER Symbol
OBUF	Primitive: Output Buffer
OBUFDS	Primitive: Differential Signaling Output Buffer
OBUFT	Primitive: 3-State Output Buffer with Active Low Output Enable
OBUFTDS	Primitive: 3-State Output Buffer with Differential Signaling, Active-Low Output Enable
ODELAYE2	Primitive: Output Fixed or Variable Delay Element
OSERDESE2	Primitive: Output SERial/DESerializer with bitslip
OUT_FIFO	Primitive: Output First-In, First-Out (FIFO) Buffer
PHASER_IN	Primitive: Phaser in
PHASER_IN_PHY	Primitive: Phaser in phy
PHASER_OUT	Primitive: Phaser out.
PHASER_OUT_PHY	Primitive: Phaser out phy.
PHASER_REF	Primitive: Phaser out.
PHY_CONTROL	Primitive: Phaser out.
PULLDOWN	Primitive: Resistor to GND for Input Pads, Open-Drain, and 3-State Outputs
PULLUP	Primitive: Resistor to VCC for Input PADs, Open-Drain, and 3-State Outputs

RAM/ROM

Design Element	Description
FIFO18E1	Primitive: 18Kb FIFO (First-In-First-Out) Block RAM Memory
FIFO36E1	Primitive: 36Kb FIFO (First-In-First-Out) Block RAM Memory
RAM128X1D	Primitive: 128-Deep by 1-Wide Dual Port Random Access Memory (Select RAM)
RAM256X1S	Primitive: 256-Deep by 1-Wide Random Access Memory (Select RAM)
RAM32M	Primitive: 32-Deep by 8-bit Wide Multi Port Random Access Memory (Select RAM)
RAM32X1D	Primitive: 32-Deep by 1-Wide Static Dual Port Synchronous RAM
RAM32X1S	Primitive: 32-Deep by 1-Wide Static Synchronous RAM
RAM32X1S_1	Primitive: 32-Deep by 1-Wide Static Synchronous RAM with Negative-Edge Clock
RAM32X2S	Primitive: 32-Deep by 2-Wide Static Synchronous RAM
RAM64M	Primitive: 64-Deep by 4-bit Wide Multi Port Random Access Memory (Select RAM)
RAM64X1D	Primitive: 64-Deep by 1-Wide Dual Port Static Synchronous RAM
RAM64X1S	Primitive: 64-Deep by 1-Wide Static Synchronous RAM
RAM64X1S_1	Primitive: 64-Deep by 1-Wide Static Synchronous RAM with Negative-Edge Clock
RAMB18E1	Primitive: 18K-bit Configurable Synchronous Block RAM
RAMB36E1	Primitive: 36K-bit Configurable Synchronous Block RAM
ROM128X1	Primitive: 128-Deep by 1-Wide ROM
ROM256X1	Primitive: 256-Deep by 1-Wide ROM
ROM32X1	Primitive: 32-Deep by 1-Wide ROM
ROM64X1	Primitive: 64-Deep by 1-Wide ROM

Registers/Latches

Design Element	Description
FDCE	Primitive: D Flip-Flop with Clock Enable and Asynchronous Clear
FDPE	Primitive: D Flip-Flop with Clock Enable and Asynchronous Preset
FDRE	Primitive: D Flip-Flop with Clock Enable and Synchronous Reset
FDSE	Primitive: D Flip-Flop with Clock Enable and Synchronous Set
IDDR	Primitive: Input Dual Data-Rate Register
IDDR_2CLK	Primitive: Input Dual Data-Rate Register with Dual Clock Inputs
LDCE	Primitive: Transparent Data Latch with Asynchronous Clear and Gate Enable
LDPE	Primitive: Transparent Data Latch with Asynchronous Preset and Gate Enable
ODDR	Primitive: Dedicated Dual Data Rate (DDR) Output Register

Slice/CLB Primitives

Design Element	Description
CARRY4	Primitive: Fast Carry Logic with Look Ahead
CFGLUT5	Primitive: 5-input Dynamically Reconfigurable Look-Up Table (LUT)
LUT1	Primitive: 1-Bit Look-Up Table with General Output
LUT2	Primitive: 2-Bit Look-Up Table with General Output
LUT3	Primitive: 3-Bit Look-Up Table with General Output
LUT4	Primitive: 4-Bit Look-Up-Table with General Output
LUT5	Primitive: 5-Input Lookup Table with General Output
LUT6	Primitive: 6-Input Lookup Table with General Output
LUT6_2	Primitive: Six-input, 2-output, Look-Up Table
MUXF7	Primitive: 2-to-1 Look-Up Table Multiplexer with General Output
MUXF8	Primitive: 2-to-1 Look-Up Table Multiplexer with General Output
SRL16E	Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Clock Enable
SRLC32E	Primitive: 32 Clock Cycle, Variable Length Shift Register Look-Up Table (LUT) with Clock Enable

XILINX®

Chapter 4

Design Elements

Overview

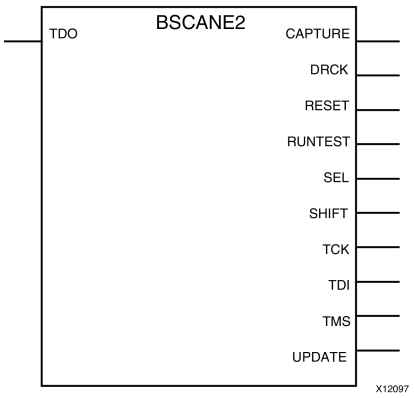
This section describes the design elements that can be used with 7 Series architectures. The design elements are organized alphabetically.

The following information is provided for each design element, where applicable:

- Name of element
- Brief description
- Schematic symbol (if any)
- Logic table (if any)
- Port descriptions
- Design Entry Method
- Available attributes (if any)
- Example instantiation code
- For more information

BSCANE2

Primitive: Boundary-Scan User Instruction



Introduction

This design element allows access to and from internal logic by the JTAG Boundary Scan logic controller. This allows for communication between the internal running design and the dedicated JTAG pins of the FPGA. Each instance of this design element will handle one JTAG USER instruction (USER1 through USER4) as set with the JTAG_CHAIN attribute. To handle all four USER instuctions, instantiate four of these elements and set the JTAG_CHAIN attribute appropriately. Note that for specific information on boundary scan for an architecture, see the Configuration User Guide for the specific device.

Port Descriptions

Port	Type	Width	Function
CAPTURE	Output	1	CAPTURE output from TAP controller.
DRCK	Output	1	Gated TCK output. When SEL is asserted, DRCK toggles when CAPTURE or SHIFT are asserted.
RESET	Output	1	Reset output for TAP controller.
RUNTEST	Output	1	Output asserted when TAP controller is in Run Test/Idle state.
SEL	Output	1	USER instruction active output.
SHIFT	Output	1	SHIFT output from TAP controller.
TCK	Output	1	Test Clock output. Fabric connection to TAP Clock pin.
TDI	Output	1	Test Data Input (TDI) output from TAP controller.
TDO	Input	1	Test Data Output (TDO) input for USER function.
TMS	Output	1	Test Mode Select output. Fabric connection to TAP.
UPDATE	Output	1	UPDATE output from TAP controller

Design Entry Method

Instantiation	Recommended
Inference	No
CORE Generator™ and wizards	No
Macro support	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
JTAG_CHAIN	DECIMAL	1, 2, 3, 4	1	Value for USER command.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- BSCANE2: Boundary-Scan User Instruction
--          7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

BSCANE2_inst : BSCANE2
generic map (
   JTAG_CHAIN => 1  -- Value for USER command.
)
port map (
   CAPTURE => CAPTURE, -- 1-bit output: CAPTURE output from TAP controller.
   DRCK => DRCK,       -- 1-bit output: Gated TCK output. When SEL is asserted, DRCK toggles when CAPTURE or
                       -- SHIFT are asserted.

   RESET => RESET,     -- 1-bit output: Reset output for TAP controller.
   RUNTEST => RUNTEST, -- 1-bit output: Output asserted when TAP controller is in Run Test/Idle state.
   SEL => SEL,         -- 1-bit output: USER instruction active output.
   SHIFT => SHIFT,     -- 1-bit output: SHIFT output from TAP controller.
   TCK => TCK,         -- 1-bit output: Test Clock output. Fabric connection to TAP Clock pin.
   TDI => TDI,         -- 1-bit output: Test Data Input (TDI) output from TAP controller.
   TMS => TMS,         -- 1-bit output: Test Mode Select output. Fabric connection to TAP.
   UPDATE => UPDATE,   -- 1-bit output: UPDATE output from TAP controller
   TDO => TDO          -- 1-bit input: Test Data Output (TDO) input for USER function.
);

-- End of BSCANE2_inst instantiation
```

Verilog Instantiation Template

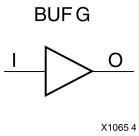
```
// BSCANE2: Boundary-Scan User Instruction
//          7 Series
// Xilinx HDL Libraries Guide, version 2012.2

BSCANE2 #(
   .JTAG_CHAIN(1)  // Value for USER command.
)
BSCANE2_inst (
   .CAPTURE(CAPTURE), // 1-bit output: CAPTURE output from TAP controller.
   .DRCK(DRCK),       // 1-bit output: Gated TCK output. When SEL is asserted, DRCK toggles when CAPTURE or
                      // SHIFT are asserted.

   .RESET(RESET),     // 1-bit output: Reset output for TAP controller.
   .RUNTEST(RUNTEST), // 1-bit output: Output asserted when TAP controller is in Run Test/Idle state.
   .SEL(SEL),         // 1-bit output: USER instruction active output.
   .SHIFT(SHIFT),     // 1-bit output: SHIFT output from TAP controller.
   .TCK(TCK),         // 1-bit output: Test Clock output. Fabric connection to TAP Clock pin.
   .TDI(TDI),         // 1-bit output: Test Data Input (TDI) output from TAP controller.
   .TMS(TMS),         // 1-bit output: Test Mode Select output. Fabric connection to TAP.
   .UPDATE(UPDATE),   // 1-bit output: UPDATE output from TAP controller
   .TDO(TDO)          // 1-bit input: Test Data Output (TDO) input for USER function.
);

// End of BSCANE2_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

BUFG

Primitive: Global Clock Simple Buffer



Introduction

This design element is a high-fanout buffer that connects signals to the global routing resources for low skew distribution of the signal. BUFGs are typically used on clock nets as well other high fanout nets like sets/resets and clock enables.

Port Descriptions

Port	Type	Width	Function
I	Input	1	Clock input
O	Output	1	Clock output

Design Entry Method

Instantiation	Yes
Inference	Recommended
CORE Generator™ and wizards	No
Macro support	No

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- BUFG: Global Clock Simple Buffer
--       7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

BUFG_inst : BUFG
port map (
   O => O, -- 1-bit output: Clock output
   I => I  -- 1-bit input: Clock input
);

-- End of BUFG_inst instantiation
```

Verilog Instantiation Template

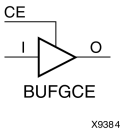
```
// BUFG: Global Clock Simple Buffer
//       7 Series
// Xilinx HDL Libraries Guide, version 2012.2

BUFG BUFG_inst (
   .O(O), // 1-bit output: Clock output
   .I(I)  // 1-bit input: Clock input
);

// End of BUFG_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

BUFGCE

Primitive: Global Clock Buffer with Clock Enable



Introduction

This design element is a global clock buffer with a single gated input. Its O output is "0" when clock enable (CE) is Low (inactive). When clock enable (CE) is High, the I input is transferred to the O output.

Logic Table

Inputs		Outputs
I	**CE**	**O**
X	0	0
I	1	I

Design Entry Method

Instantiation	Recommended
Inference	No
CORE Generator™ and wizards	No
Macro support	No

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- BUFGCE: Global Clock Buffer with Clock Enable
--         7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

BUFGCE_inst : BUFGCE
port map (
   O => O,    -- 1-bit output: Clock output
   CE => CE,  -- 1-bit input: Clock enable input for I0
   I => I     -- 1-bit input: Primary clock
);

-- End of BUFGCE_inst instantiation
```

Verilog Instantiation Template

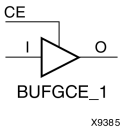
```
// BUFGCE: Global Clock Buffer with Clock Enable
//         7 Series
// Xilinx HDL Libraries Guide, version 2012.2

BUFGCE BUFGCE_inst (
   .O(O),   // 1-bit output: Clock output
   .CE(CE), // 1-bit input: Clock enable input for I0
   .I(I)    // 1-bit input: Primary clock
);

// End of BUFGCE_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

BUFGCE_1

Primitive: Global Clock Buffer with Clock Enable and Output State 1



Introduction

This design element is a global clock buffer with a single gated input. Its O output is "1" when clock enable (CE) is Low (inactive). When clock enable (CE) is High, the I input is transferred to the O output.

Logic Table

Inputs		Outputs
I	**CE**	**O**
X	0	1
I	1	I

Port Descriptions

Port	Direction	Width	Function
CE	Input	1	Clock buffer active high enable
I	Input	1	Clock input
O	Output	1	Clock output

Design Entry Method

Instantiation	Recommended
Inference	No
CORE Generator™ and wizards	No
Macro support	No

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- BUFGCE_1: Global Clock Buffer with Clock Enable and Output State 1
--           7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

BUFGCE_1_inst : BUFGCE_1
port map (
   O => O,    -- 1-bit output: Clock output
   CE => CE,  -- 1-bit input: Clock enable input for I0
   I => I     -- 1-bit input: Primary clock
);

-- End of BUFGCE_1_inst instantiation
```

Verilog Instantiation Template

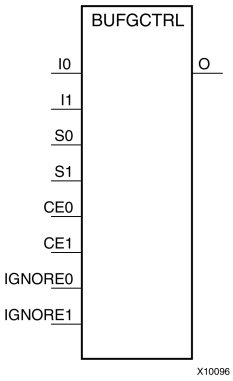
```
// BUFGCE_1: Global Clock Buffer with Clock Enable and Output State 1
//           7 Series
// Xilinx HDL Libraries Guide, version 2012.2

BUFGCE_1 BUFGCE_1_inst (
   .O(O),    // 1-bit output: Clock output
   .CE(CE), // 1-bit input: Clock enable input for I0
   .I(I)    // 1-bit input: Primary clock
);

// End of BUFGCE_1_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

BUFGCTRL

Primitive: Global Clock Control Buffer



Introduction

BUFGCTRL primitive is a 7 series global clock buffer that is designed as a synchronous/asynchronous "glitch free" 2:1 multiplexer with two clock inputs. Unlike global clock buffers that are found in previous generations of FPGAs, these clock buffers are designed with more control pins to provide a wider range of functionality and more robust input switching. BUFGCTRL is not limited to clocking applications.

Port Descriptions

Port	Type	Width	Function
CE0	Input	1	Clock enable input for the I0 clock input. A setup/hold time must be guarenteed when you are using the CE0 pin to enable this input. Failure to meet this requirement could result in a clock glitch.
CE1	Input	1	Clock enable input for the I1 clock input. A setup/hold time must be guarenteed when you are using the CE1 pin to enable this input. Failure to meet this requirement could result in a clock glitch.
IGNORE0	Input	1	Clock ignore input for I0 input. Asserting the IGNORE pin will bypass the BUFGCTRL from detecting the conditions for switching between two clock inputs. In other words, asserting IGNORE causes the MUX to switch the inputs at the instant the select pin changes. IGNORE0 causes the output to switch away from the I0 input immediately when the select pin changes, while IGNORE1 causes the output to switch away from the I1 input immediately when the select pin changes.
IGNORE1	Input	1	Clock ignore input for I1 input. Asserting the IGNORE pin will bypass the BUFGCTRL from detecting the conditions for switching between two clock inputs. In other words, asserting IGNORE causes the MUX to switch the inputs at the instant the select pin changes. IGNORE0 causes the output to switch away from the I0 input immediately when the select pin changes, while IGNORE1 causes the output to

Port	Type	Width	Function
			switch away from the I1 input immediately when the select pin changes.
I0	Input	1	Primary clock input into the BUFGCTRL enabled by the CE0 input and selected by the S0 input.
I1	Input	1	Secondary clock input into the BUFGCTRL enabled by the CE1 input and selected by the S1 input.
O	Output	1	Clock output
S0	Input	1	Clock select input for I0. The S pins represent the clock select pin for each clock input. When using the S pin as input select, there is a setup/hold time requirement. Unlike CE pins, failure to meet this requirement will not result in a clock glitch. However, it can cause the output clock to appear one clock cycle later.
S1	Input	1	Clock select input for I1. The S pins represent the clock select pin for each clock input. When using the S pin as input select, there is a setup/hold time requirement. Unlike CE pins, failure to meet this requirement will not result in a clock glitch. However, it can cause the output clock to appear one clock cycle later.

Design Entry Method

Instantiation	Recommended
Inference	No
CORE Generator™ and wizards	No
Macro support	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
INIT_OUT	DECIMAL	0, 1	0	Initializes the BUFGCTRL output to the specified value after configuration.
PRESELECT_I0	BOOLEAN	FALSE, TRUE	FALSE	If TRUE, BUFGCTRL output uses I0 input after configuration.
PRESELECT_I1	BOOLEAN	FALSE, TRUE	FALSE	If TRUE, BUFGCTRL output uses I1 input after configuration.

Note Both PRESELECT attributes might not be TRUE at the same time.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- BUFGCTRL: Global Clock Control Buffer
--           7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

BUFGCTRL_inst : BUFGCTRL
generic map (
   INIT_OUT => 0,         -- Initial value of BUFGCTRL output ($VALUES;)
   PRESELECT_I0 => FALSE, -- BUFGCTRL output uses I0 input ($VALUES;)
   PRESELECT_I1 => FALSE  -- BUFGCTRL output uses I1 input ($VALUES;)
)
port map (
   O => O,             -- 1-bit output: Clock output
   CE0 => CE0,         -- 1-bit input: Clock enable input for I0
   CE1 => CE1,         -- 1-bit input: Clock enable input for I1
   I0 => I0,           -- 1-bit input: Primary clock
   I1 => I1,           -- 1-bit input: Secondary clock
   IGNORE0 => IGNORE0, -- 1-bit input: Clock ignore input for I0
   IGNORE1 => IGNORE1, -- 1-bit input: Clock ignore input for I1
   S0 => S0,           -- 1-bit input: Clock select for I0
   S1 => S1            -- 1-bit input: Clock select for I1
);

-- End of BUFGCTRL_inst instantiation
```

Verilog Instantiation Template

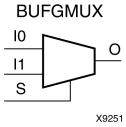
```
// BUFGCTRL: Global Clock Control Buffer
//           7 Series
// Xilinx HDL Libraries Guide, version 2012.2

BUFGCTRL #(
   .INIT_OUT(0),           // Initial value of BUFGCTRL output ($VALUES;)
   .PRESELECT_I0("FALSE"), // BUFGCTRL output uses I0 input ($VALUES;)
   .PRESELECT_I1("FALSE")  // BUFGCTRL output uses I1 input ($VALUES;)
)
BUFGCTRL_inst (
   .O(O),             // 1-bit output: Clock output
   .CE0(CE0),         // 1-bit input: Clock enable input for I0
   .CE1(CE1),         // 1-bit input: Clock enable input for I1
   .I0(I0),           // 1-bit input: Primary clock
   .I1(I1),           // 1-bit input: Secondary clock
   .IGNORE0(IGNORE0), // 1-bit input: Clock ignore input for I0
   .IGNORE1(IGNORE1), // 1-bit input: Clock ignore input for I1
   .S0(S0),           // 1-bit input: Clock select for I0
   .S1(S1)            // 1-bit input: Clock select for I1
);

// End of BUFGCTRL_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

BUFGMUX

Primitive: Global Clock Mux Buffer



Introduction

This design element is a global clock buffer, based off of the BUFGCTRL, that can select betweeen two input clocks: I0 and I1. When the select input (S) is Low, the signal on I0 is selected for output (O). When the select input (S) is High, the signal on I1 is selected for output. BUFGMUX BUFGMUX_1 are distinguished by the state the output assumes when that output switches between clocks in response to a change in its select input. BUFGMUX assumes output state 0 and BUFGMUX_1 assumes output state 1.

Logic Table

Inputs			Outputs
I0	**I1**	**S**	**O**
I0	X	0	I0
X	I1	1	I1
X	X	↑	0
X	X	↓	0

Port Descriptions

Port	Direction	Width	Function
I0	Input	1	Clock buffer input. This input is reflected on the output O when the S input is zero.
I1	Input	1	Clock buffer input. This input is reflected on the output O when the S input is one.
O	Output	1	Clock buffer output.
S	Input	1	Clock buffer select input. When low, selects I0 input and when high, the I1 input is slected

Design Entry Method

Instantiation	Recommended
Inference	No
CORE Generator™ and wizards	No
Macro support	No

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- BUFGMUX: Global Clock Mux Buffer
--          7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

BUFGMUX_inst : BUFGMUX
port map (
   O => O,    -- 1-bit output: Clock output
   I0 => I0, -- 1-bit input: Clock input (S=0)
   I1 => I1, -- 1-bit input: Clock input (S=1)
   S => S     -- 1-bit input: Clock select
);

-- End of BUFGMUX_inst instantiation
```

Verilog Instantiation Template

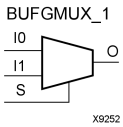
```
// BUFGMUX: Global Clock Mux Buffer
//          7 Series
// Xilinx HDL Libraries Guide, version 2012.2

BUFGMUX #(
)
BUFGMUX_inst (
   .O(O),    // 1-bit output: Clock output
   .I0(I0), // 1-bit input: Clock input (S=0)
   .I1(I1), // 1-bit input: Clock input (S=1)
   .S(S)     // 1-bit input: Clock select
);

// End of BUFGMUX_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

BUFGMUX_1

Primitive: Global Clock Mux Buffer with Output State 1



Introduction

This design element is a global clock buffer, based off of the BUFGCTRL, that can select betweeen two input clocks: I0 and I1. When the select input (S) is Low, the signal on I0 is selected for output (O). When the select input (S) is High, the signal on I1 is selected for output. BUFGMUX BUFGMUX_1 are distinguished by the state the output assumes when that output switches between clocks in response to a change in its select input. BUFGMUX assumes output state0 and BUFGMUX_1 assumes output state 1.

Logic Table

Inputs			Outputs
I0	**I1**	**S**	**O**
I0	X	0	I0
X	I1	1	I1
X	X	↑	1
X	X	↓	1

Design Entry Method

Instantiation	Recommended
Inference	No
CORE Generator™ and wizards	No
Macro support	No

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- BUFGMUX_1: Global Clock Mux Buffer with Output State 1
--            7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

BUFGMUX_1_inst : BUFGMUX_1
```

```
port map (
   O => O,    -- 1-bit output: Clock output
   I0 => I0,  -- 1-bit input: Clock input (S=0)
   I1 => I1,  -- 1-bit input: Clock input (S=1)
   S => S     -- 1-bit input: Clock select
);

-- End of BUFGMUX_1_inst instantiation
```

Verilog Instantiation Template

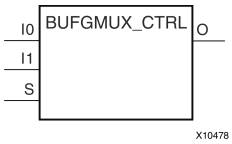
```
// BUFGMUX_1: Global Clock Mux Buffer with Output State 1
//            7 Series
// Xilinx HDL Libraries Guide, version 2012.2

BUFGMUX_1 #(
)
BUFGMUX_1_inst (
   .O(O),   // 1-bit output: Clock output
   .I0(I0), // 1-bit input: Clock input (S=0)
   .I1(I1), // 1-bit input: Clock input (S=1)
   .S(S)    // 1-bit input: Clock select
);

// End of BUFGMUX_1_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

BUFGMUX_CTRL

Primitive: 2-to-1 Global Clock MUX Buffer



Introduction

This design element is a global clock buffer with two clock inputs, one clock output, and a select line used to cleanly select between one of two clocks driving the global clocking resource. This component is based on BUFGCTRL, with some pins connected to logic High or Low. This element uses the S pin as the select pin for the 2-to-1 MUX. S can switch anytime without causing a glitch on the output clock of the buffer.

Port Descriptions

Port	Direction	Width	Function
I0	Input	1	Clock buffer input. This input is reflected on the output O when the S input is zero.
I1	Input	1	Clock buffer input. This input is reflected on the output O when the S input is one.
O	Output	1	Clock buffer output.
S	Input	1	Clock buffer select input. When low, selects I0 input and when high, the I1 input is slected

Design Entry Method

Instantiation	Recommended
Inference	No
CORE Generator™ and wizards	No
Macro support	No

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- BUFGMUX_CTRL: 2-to-1 Global Clock MUX Buffer
--               7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

BUFGMUX_CTRL_inst : BUFGMUX_CTRL
port map (
   O => O,   -- 1-bit output: Clock output
   I0 => I0, -- 1-bit input: Clock input (S=0)
   I1 => I1, -- 1-bit input: Clock input (S=1)
   S => S    -- 1-bit input: Clock select
);

-- End of BUFGMUX_CTRL_inst instantiation
```

Verilog Instantiation Template

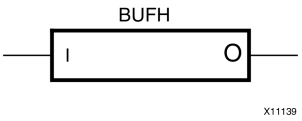
```
// BUFGMUX_CTRL: 2-to-1 Global Clock MUX Buffer
//               7 Series
// Xilinx HDL Libraries Guide, version 2012.2

BUFGMUX_CTRL BUFGMUX_CTRL_inst (
   .O(O),   // 1-bit output: Clock output
   .I0(I0), // 1-bit input: Clock input (S=0)
   .I1(I1), // 1-bit input: Clock input (S=1)
   .S(S)    // 1-bit input: Clock select
);

// End of BUFGMUX_CTRL_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

BUFH

Primitive: HROW Clock Buffer for a Single Clocking Region



Introduction

The BUFH primitive allows direct access to the clock region entry point of the global buffer (BUFG) resource. This allows access to unused portions of the global clocking network to be used as high-speed, low skew local (single clock region) routing resources. Please refer to the 7 series FPGA Clocking Resources User Guide for details for using this component.

Port Descriptions

Port	Type	Width	Function
I	Input	1	Clock input
O	Output	1	Clock output

Design Entry Method

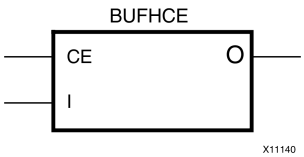
Instantiation	Yes
Inference	No
CORE Generator™ and wizards	No
Macro support	No

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

BUFHCE

Primitive: HROW Clock Buffer for a Single Clocking Region with Clock Enable



Introduction

The BUFHCE primitive allows direct access to the clock region entry point of the global buffer (BUFG) resource. This allows access to unused portions of the global clocking network to be used as high-speed, low skew local (single clock region) routing resources. Addtionaly, the CE or clock enable input allows for finer-grained control of clock enabling or gating to allow for power reduction for circuitry or portions of the design not constantly used. Please refer to the 7 series FPGA Clocking Resources User Guide for details for using this component.

Port Descriptions

Port	Type	Width	Function
CE	Input	1	Enables propagation of signal from I to O. When low, performs a glitchless transition of the output to INIT_OUT value.
I	Input	1	Clock input
O	Output	1	Clock output

Design Entry Method

Instantiation	Yes
Inference	No
CORE Generator™ and wizards	No
Macro support	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
CE_TYPE	STRING	"SYNC", "ASYNC"	"SYNC"	Sets clock enable behavior where "SYNC" allows for a glitchless transition to and from the INIT_OUT value. "ASYNC" is generally used to create a more immediate transition such as when you can expect the clock to be stopped or when using the BUFHCE for a high fanout control or data path routing instead of a clock buffer.

Attribute	Type	Allowed Values	Default	Description
INIT_OUT	DECIMAL	0, 1	0	Initial output value, also indicates stop low vs stop high behavior

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- BUFHCE: HROW Clock Buffer for a Single Clocking Region with Clock Enable
--         7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

BUFHCE_inst : BUFHCE
generic map (
   CE_TYPE => "SYNC", -- "SYNC" (glitchless switching) or "ASYNC" (immediate switch)
   INIT_OUT => 0      -- Initial output value (0-1)
)
port map (
   O => O,    -- 1-bit output: Clock output
   CE => CE, -- 1-bit input: Active high enable
   I => I     -- 1-bit input: Clock input
);

-- End of BUFHCE_inst instantiation
```

Verilog Instantiation Template

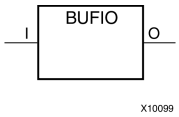
```
// BUFHCE: HROW Clock Buffer for a Single Clocking Region with Clock Enable
//         7 Series
// Xilinx HDL Libraries Guide, version 2012.2

BUFHCE #(
   .CE_TYPE("SYNC"), // "SYNC" (glitchless switching) or "ASYNC" (immediate switch)
   .INIT_OUT(0)      // Initial output value (0-1)
)
BUFHCE_inst (
   .O(O),   // 1-bit output: Clock output
   .CE(CE), // 1-bit input: Active high enable
   .I(I)    // 1-bit input: Clock input
);

// End of BUFHCE_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

BUFIO

Primitive: Local Clock Buffer for I/O



Introduction

This design element is simply a clock-in, clock-out buffer. It drives a dedicated clock net within the I/O column, independent of the global clock resources. Thus, these elements are ideally suited for source-synchronous data capture (forwarded/receiver clock distribution). They can be driven by a dedicated MRCC I/O located in the same clock region or a BUFMRCE/BUFMR component capable of clocking multiple clock regions. The BUFIO can only drive I/O components within the bank in which they exist. These elements cannot directly drive logic resources (CLB, block RAM, etc.) because the I/O clock network only reaches the I/O column.

Port Descriptions

Port	Type	Width	Function
I	Input	1	Input port to clock buffer. Connect this to an IBUFG connected to a top-level port or an associated BUFMR buffer.
O	Output	1	Output port from clock buffer. Connect this to the clock inputs to synchronous I/O components like the ISERDESE2, OSERDESE2, IDDR, ODDR or register connected directly to an I/O port (inferred or instantiated).

Design Entry Method

Instantiation	Yes
Inference	No
CORE Generator™ and wizards	No
Macro support	No

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- BUFIO: Local Clock Buffer for I/O
--        7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

BUFIO_inst : BUFIO
port map (
   O => O, -- 1-bit output: Clock output (connect to I/O clock loads).
   I => I  -- 1-bit input: Clock input (connect to an IBUFG or BUFMR).
);

-- End of BUFIO_inst instantiation
```

Verilog Instantiation Template

```
// BUFIO: Local Clock Buffer for I/O
//        7 Series
// Xilinx HDL Libraries Guide, version 2012.2

BUFIO BUFIO_inst (
   .O(O), // 1-bit output: Clock output (connect to I/O clock loads).
   .I(I)  // 1-bit input: Clock input (connect to an IBUFG or BUFMR).
);

// End of BUFIO_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

BUFMR

Primitive: Multi-Region Clock Buffer

Introduction

The BUFMR is a simple clock-in/clock-out buffer. The BUFMR replaces the multi-region/bank support of the BUFR and BUFIO available in prior Virtex architectures. There are two BUFMRs in every bank and each buffer can be driven by one specific MRCC in the same bank. The BUFMRs drive the BUFIOs and/or BUFRs in the same region/banks and in the region above and below via the I/O clocking backbone. It is not suggested to use a BUFMR when driving BUFRs using clock dividers (not in bypass) and instead use a BUFMRCE component.

Port Descriptions

Port	Direction	Width	Function
I	Input	1	BUFMR clock input pin. Connect to an IBUFG input that in turn is directly connected to a MRCC I/O port.
O	Output	1	BUFMR clock output pin. Connect to BUFIOs and/or BUFRs to be driven in adjacent regions.

Design Entry Method

Instantiation	Yes
Inference	No
CORE Generator™ and wizards	No
Macro support	No

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- BUFMR: Multi-Region Clock Buffer
--        7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

BUFMR_inst : BUFMR
port map (
   O => O, -- 1-bit output: Clock output (connect to BUFIOs/BUFRs)
   I => I  -- 1-bit input: Clock input (Connect to IBUFG)
);
```

```
-- End of BUFMR_inst instantiation
```

Verilog Instantiation Template

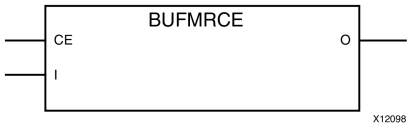
```
// BUFMR: Multi-Region Clock Buffer
//        7 Series
// Xilinx HDL Libraries Guide, version 2012.2

BUFMR BUFMR_inst (
   .O(O), // 1-bit output: Clock output (connect to BUFIOs/BUFRs)
   .I(I)  // 1-bit input: Clock input (Connect to IBUFG)
);

// End of BUFMR_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

BUFMRCE

Primitive: Multi-Region Clock Buffer with Clock Enable



Introduction

The BUFMRCE is a simple clock-in/clock-out buffer with clock with clock enable (CE). Asserting CE stops the output clock to a user specified value. The BUFMRCE replaces the multi-region/bank support of the BUFR and BUFIO available in prior Virtex architectures. There are two BUFMRCEs in every bank and each buffer can be driven by one specific MRCC in the same bank. The BUFMRCE drives the BUFIOs and/or BUFRs in the same region/banks and in the region above and below via the I/O clocking backbone. When using BUFR dividers (not in bypass), the BUFMRCE must be disabled by deasserting the CE pin, the BUFR must be reset (cleared by asserting CLR), and then the CE signal should be asserted. This sequence ensures that all BUFR output clocks are phase aligned. If the dividers within the BUFRs are not used, then this additional circuitry is not necessary. If the clock enable circuitry is not needed, a BUFMR component should be used in place of a BUFMRCE.

Port Descriptions

Port	Type	Width	Function
CE	Input	1	Active high buffer enable input. When low, output will settle to INIT_OUT value.
I	Input	1	BUFMR clock input pin. Connect to an IBUFG input that in turn is directly connected to a MRCC I/O port.
O	Output	1	BUFMR clock output pin. Connect to BUFIOs and/or BUFRs to be driven in the same and adjacent regions.

Design Entry Method

Instantiation	Yes
Inference	No
CORE Generator™ and wizards	No
Macro support	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
CE_TYPE	STRING	"SYNC", "ASYNC"	"SYNC"	Set to "SYNC" for CE to be synchronous to input I and create a glitchless output. Set to "ASYNC" for stopped clock or non-clock operation of the CE signal.
INIT_OUT	DECIMAL	0, 1	0	Initial output value, also indicates stop low vs stop high behavior

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- BUFMRCE: Multi-Region Clock Buffer with Clock Enable
--          7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

BUFMRCE_inst : BUFMRCE
generic map (
   CE_TYPE => "SYNC", -- SYNC, ASYNC
   INIT_OUT => 0      -- Initial output and stopped polarity, (0-1)
)
port map (
   O => O,    -- 1-bit output: Clock output (connect to BUFIOs/BUFRs)
   CE => CE,  -- 1-bit input: Active high buffer enable
   I => I     -- 1-bit input: Clock input (Connect to IBUFG)
);

-- End of BUFMRCE_inst instantiation
```

Verilog Instantiation Template

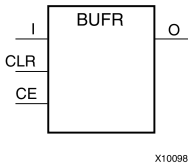
```
// BUFMRCE: Multi-Region Clock Buffer with Clock Enable
//          7 Series
// Xilinx HDL Libraries Guide, version 2012.2

BUFMRCE #(
   .CE_TYPE("SYNC"), // SYNC, ASYNC
   .INIT_OUT(0)      // Initial output and stopped polarity, (0-1)
)
BUFMRCE_inst (
   .O(O),    // 1-bit output: Clock output (connect to BUFIOs/BUFRs)
   .CE(CE), // 1-bit input: Active high buffer enable
   .I(I)     // 1-bit input: Clock input (Connect to IBUFG)
);

// End of BUFMRCE_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

BUFR

Primitive: Regional Clock Buffer for I/O and Logic Resources within a Clock Region



Introduction

The BUFR is a regional clock buffer available in 7 series devices. BUFRs drive clock signals to a dedicated clock net within a clock region, independent from the global clock tree. Each BUFR can drive the regional clock nets in the region in which it is located. Unlike BUFIOs, BUFRs can drive the I/O logic and logic resources (CLB, block RAM, etc.) in the existing clock region. BUFRs can be driven by either the output from an IBUFG, BUFMRCE, MMCM or local interconnect. In addition, BUFRs are capable of generating divided clock outputs with respect to the clock input. The divide value is an integer between one and eight. BUFRs are ideal for source-synchronous applications requiring clock domain crossing or serial-to-parallel conversion. There are two BUFRs in a typical clock region (two regional clock networks). If local clocking is needed in multiple clock regions, the BUFMRCE can drive multiple BUFRs in adjacent clock regions to further extend this clocking capability. Please refer to the BUFMRCE for more details.

Port Descriptions

Port	Type	Width	Function
CE	Input	1	Clock enable port. When asserted low, this port disables the output clock. When asserted high, the clock is propagated out the O output port. Cannot be used in "BYPASS" mode. Connect to vcc when BUFR_DIVIDE is set to "BYPASS" or if not used.
CLR	Input	1	Counter asynchronous clear for divided clock output. When asserted high, this port resets the counter used to produce the divided clock output and the output is asserted low. Cannot be used in "BYPASS" mode. Connect to gnd when BUFR_DIVIDE is set to "BYPASS" or if not used.
I	Input	1	Clock input port. This port is the clock source port for BUFR. It can be driven by an IBUFG, BUFMRCE, MMCM or local interconnect.
O	Output	1	Clock output port. This port drives the clock tracks in the clock region of the BUFR. This port connects to FPGA clocked components.

Design Entry Method

Instantiation	Yes
Inference	No
CORE Generator™ and wizards	Yes
Macro support	No

Available Attributes

Attribute	Type	Allowed_Values	Default	Description
BUFR_DIVIDE	STRING	"BYPASS", "1", "2", "3", "4", "5", "6", "7", "8"	"BYPASS"	Defines whether the output clock is a divided version of input clock.
SIM_DEVICE	STRING	7SERIES	"7SERIES"	For correct simulation behavior, this attribute must be set to "7SERIES" when targeting a 7 series device.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- BUFR: Regional Clock Buffer for I/O and Logic Resources within a Clock Region
--       7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

BUFR_inst : BUFR
generic map (
   BUFR_DIVIDE => "BYPASS", -- Values: "BYPASS, 1, 2, 3, 4, 5, 6, 7, 8"
   SIM_DEVICE => "7SERIES"  -- Must be set to "7SERIES"
)
port map (
   O => O,     -- 1-bit output: Clock output port
   CE => CE,   -- 1-bit input: Active high, clock enable (Divided modes only)
   CLR => CLR, -- 1-bit input: Active high, asynchronous clear (Divided modes only)
   I => I      -- 1-bit input: Clock buffer input driven by an IBUFG, MMCM or local interconnect
);

-- End of BUFR_inst instantiation
```

Verilog Instantiation Template

```
// BUFR: Regional Clock Buffer for I/O and Logic Resources within a Clock Region
//       7 Series
// Xilinx HDL Libraries Guide, version 2012.2

BUFR #(
   .BUFR_DIVIDE("BYPASS"), // Values: "BYPASS, 1, 2, 3, 4, 5, 6, 7, 8"
   .SIM_DEVICE("7SERIES")  // Must be set to "7SERIES"
)
BUFR_inst (
   .O(O),     // 1-bit output: Clock output port
   .CE(CE),   // 1-bit input: Active high, clock enable (Divided modes only)
   .CLR(CLR), // 1-bit input: Active high, asynchronous clear (Divided modes only)
```

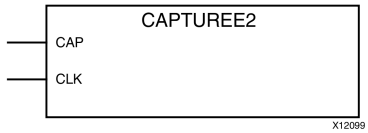
```
   .I(I)      // 1-bit input: Clock buffer input driven by an IBUFG, MMCM or local interconnect
);

// End of BUFR_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

CAPTUREE2

Primitive: Register Capture



Introduction

This element provides user control and synchronization over when and how the capture register (flip-flop and latch) information task is requested. The readback function is provided through dedicated configuration port instructions. However, without this element, the readback data is synchronized to the configuration clock. Only register (flip-flop and latch) states can be captured. Although LUT RAM, SRL, and block RAM states are readback, they cannot be captured. An asserted high CAP signal indicates that the registers in the device are to be captured at the next Low-to-High clock transition. By default, data is captured after every trigger when transition on CLK while CAP is asserted. To limit the readback operation to a single data capture, add the ONESHOT=TRUE attribute to this element.

Port Descriptions

Port	Type	Width	Function
CAP	Input	1	Capture Input
CLK	Input	1	Clock Input

Design Entry Method

Instantiation	Recommended
Inference	No
CORE Generator™ and wizards	No
Macro support	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
ONESHOT	STRING	"TRUE", "FALSE"	"TRUE"	Specifies the procedure for performing single readback per CAP trigger.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- CAPTUREE2: Register Capture
--            7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

CAPTUREE2_inst : CAPTUREE2
generic map (
   ONESHOT => "TRUE"  -- Specifies the procedure for performing single readback per CAP trigger.
)
port map (
   CAP => CAP, -- 1-bit input: Capture Input
   CLK => CLK  -- 1-bit input: Clock Input
);

-- End of CAPTUREE2_inst instantiation
```

Verilog Instantiation Template

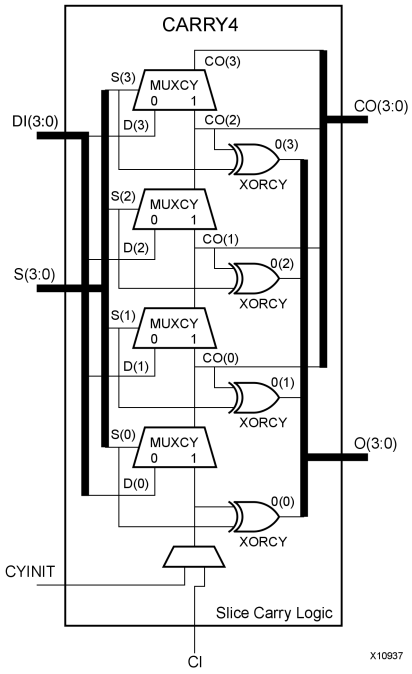
```
// CAPTUREE2: Register Capture
//            7 Series
// Xilinx HDL Libraries Guide, version 2012.2

CAPTUREE2 #(
   .ONESHOT("TRUE")  // Specifies the procedure for performing single readback per CAP trigger.
)
CAPTUREE2_inst (
   .CAP(CAP), // 1-bit input: Capture Input
   .CLK(CLK)  // 1-bit input: Clock Input
);

// End of CAPTUREE2_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

CARRY4

Primitive: Fast Carry Logic with Look Ahead



Introduction

This circuit design represents the fast carry logic for a slice. The carry chain consists of a series of four MUXes and four XORs that connect to the other logic (LUTs) in the slice via dedicated routes to form more complex functions. The fast carry logic is useful for building arithmetic functions like adders, counters, subtractors and add/subs, as well as such other logic functions as wide comparators, address decoders, and some logic gates (specifically, AND and OR).

Port Descriptions

Port	Direction	Width	Function
O	Output	4	Carry chain XOR general data out
CO	Output	4	Carry-out of each stage of the carry chain
DI	Input	4	Carry-MUX data input
S	Input	4	Carry-MUX select line
CYINIT	Input	1	Carry-in initialization input
CI	Input	1	Carry cascade input

Design Entry Method

Instantiation	Yes
Inference	Recommended
CORE Generator™ and wizards	No
Macro support	No

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- CARRY4: Fast Carry Logic Component
--         7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

CARRY4_inst : CARRY4
port map (
   CO => CO,         -- 4-bit carry out
   O => O,           -- 4-bit carry chain XOR data out
   CI => CI,         -- 1-bit carry cascade input
   CYINIT => CYINIT, -- 1-bit carry initialization
   DI => DI,         -- 4-bit carry-MUX data in
   S => S            -- 4-bit carry-MUX select input
);

-- End of CARRY4_inst instantiation
```

Verilog Instantiation Template

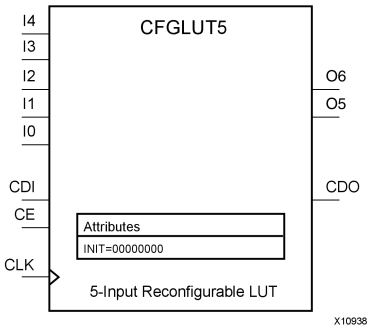
```
// CARRY4: Fast Carry Logic Component
//         7 Series
// Xilinx HDL Libraries Guide, version 2012.2

CARRY4 CARRY4_inst (
   .CO(CO),         // 4-bit carry out
   .O(O),           // 4-bit carry chain XOR data out
   .CI(CI),         // 1-bit carry cascade input
   .CYINIT(CYINIT), // 1-bit carry initialization
   .DI(DI),         // 4-bit carry-MUX data in
   .S(S)            // 4-bit carry-MUX select input
);

// End of CARRY4_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

CFGLUT5

Primitive: 5-input Dynamically Reconfigurable Look-Up Table (LUT)



Introduction

This element is a runtime, dynamically reconfigurable, 5-input look-up table (LUT) that enables the changing of the logical function of the LUT during circuit operation. Using the CDI pin, a new INIT value can be synchronously shifted in serially to change the logical function. The O6 output pin produces the logical output function, based on the current INIT value loaded into the LUT and the currently selected I0-I4 input pins. Optionally, you can use the O5 output in combination with the O6 output to create two individual 4-input functions sharing the same inputs or a 5-input function and a 4-input function that uses a subset of the 5-input logic (see tables below). This component occupies one of the four LUT6 components within a Slice-M.

To cascade this element, connect the CDO pin from each element to the CDI input of the next element. This will allow a single serial chain of data (32-bits per LUT) to reconfigure multiple LUTs.

Port Descriptions

Port	Direction	Width	Function
O6	Output	1	5-LUT output
O5	Output	1	4-LUT output
I0, I1, I2, I3, I4	Input	1	LUT inputs
CDO	Output	1	Reconfiguration data cascaded output (optionally connect to the CDI input of a subsequent LUT)
CDI	Input	1	Reconfiguration data serial input
CLK	Input	1	Reconfiguration clock
CE	Input	1	Active high reconfiguration clock enable

Design Entry Method

Instantiation	Recommended
Inference	No
CORE Generator™ and wizards	No
Macro support	No

- Connect the CLK input to the clock source used to supply the reconfiguration data.
- Connect the CDI input to the source of the reconfiguration data.
- Connect the CE pin to the active high logic if you need to enable/disable LUT reconfiguration.
- Connect the I4-I0 pins to the source inputs to the logic equation. The logic function is output on O6 and O5.
- To cascade this element, connect the CDO pin from each element to the CDI input of the next element to allow a single serial chain of data to reconfigure multiple LUTs.

The INIT attribute should be placed on this design element to specify the initial logical function of the LUT. A new INIT can be loaded into the LUT any time during circuit operation by shifting in 32-bits per LUT in the chain, representing the new INIT value. Disregard the O6 and O5 output data until all 32-bits of new INIT data has been clocked into the LUT. The logical function of the LUT changes as new INIT data is shifted into it. Data should be shifted in MSB (INIT[31]) first and LSB (INIT[0]) last.

In order to understand the O6 and O5 logical value based on the current INIT, see the table below:

I4 I3 I2 I1 I0	O6 Value	O5 Value
1 1 1 1 1	INIT[31]	INIT[15]
1 1 1 1 0	INIT[30]	INIT[14]
. . .	. . .	. . .
1 0 0 0 1	INIT[17]	INIT[1]
1 0 0 0 0	INIT[16]	INIT[0]
0 1 1 1 1	INIT[15]	INIT[15]
0 1 1 1 0	INIT[14]	INIT[14]
. . .	. . .	. . .
0 0 0 0 1	INIT[1]	INIT[1]
0 0 0 0 0	INIT[0]	INIT[0]

For instance, the INIT value of FFFF8000 would represent the following logical equations:

- O6 = I4 or (I3 and I2 and I1 and I0)
- O5 = I3 and I2 and I1 and I0

To use these elements as two, 4-input LUTs with the same inputs but different functions, tie the I4 signal to a logical one. The INIT[31:16] values apply to the logical values of the O6 output and INIT [15:0] apply to the logical values of the O5 output.

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 32-bit Value	All zeros	Specifies the initial logical expression of this element.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- CFGLUT5: Reconfigurable 5-input LUT (Mapped to SliceM LUT6)
--          7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

CFGLUT5_inst : CFGLUT5
generic map (
   INT => X"00000000")
port map (
   CDO => CDO, -- Reconfiguration cascade output
   O5 => O5,   -- 4-LUT output
   O6 => O6,   -- 5-LUT output
   CDI => CDI, -- Reconfiguration data input
   CE => CE,   -- Reconfiguration enable input
   CLK => CLK, -- Clock input
   I0 => I0,   -- Logic data input
   I1 => I1,   -- Logic data input
   I2 => I2,   -- Logic data input
   I3 => I3,   -- Logic data input
   I4 => I4    -- Logic data input
);

-- End of CFGLUT5_inst instantiation
```

Verilog Instantiation Template

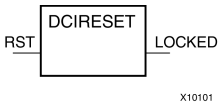
```
// CFGLUT5: Reconfigurable 5-input LUT  (Mapped to a SliceM LUT6)
//          7 Series
// Xilinx HDL Libraries Guide, version 2012.2

CFGLUT5 #(
   .INIT(32'h00000000) // Specify initial LUT contents
) CFGLUT5_inst (
   .CDO(CDO), // Reconfiguration cascade output
   .O5(O5),   // 4-LUT output
   .O6(O6),   // 5-LUT output
   .CDI(CDI), // Reconfiguration data input
   .CE(CE),   // Reconfiguration enable input
   .CLK(CLK), // Clock input
   .I0(I0),   // Logic data input
   .I1(I1),   // Logic data input
   .I2(I2),   // Logic data input
   .I3(I3),   // Logic data input
   .I4(I4)    // Logic data input
);

// End of CFGLUT5_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

DCIRESET

Primitive: Digitally Controlled Impedance Reset Component



Introduction

This design element is used to reset the Digitally Controlled Impedance (DCI) state machine after configuration has been completed. By toggling the RST input to the DCIRESET primitive while the device is operating, the DCI state-machine is reset and both phases of impedance adjustment proceed in succession. All I/Os using DCI will be unavailable until the LOCKED output from the DCIRESET block is asserted

Port Descriptions

Port	Type	Width	Function
LOCKED	Output	1	DCI state-machine LOCK status output. When low, DCI I/O impedance is being calibrated and DCI I/Os are unavailable. Upon a low-to-high assertion, DCI I/Os are available for use.
RST	Input	1	Active-high asynchronous reset input to DCI state-machine. After RST is asserted, I/Os utilizing DCI will be unavailable until LOCKED is asserted.

Design Entry Method

Instantiation	Yes
Inference	No
CORE Generator™ and wizards	No
Macro support	No

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- DCIRESET: Digitally Controlled Impedance Reset Component
--           7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

DCIRESET_inst : DCIRESET
```

```
port map (
   LOCKED => LOCKED, -- 1-bit output: LOCK status output
   RST => RST        -- 1-bit input: Active-high asynchronous reset input
);

-- End of DCIRESET_inst instantiation
```

Verilog Instantiation Template

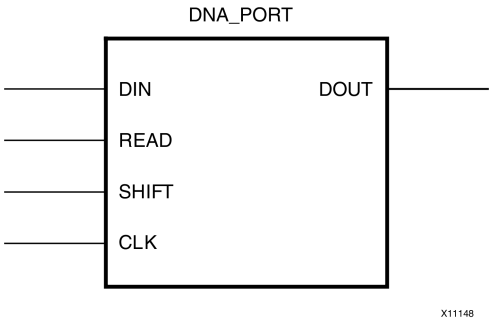
```
// DCIRESET: Digitally Controlled Impedance Reset Component
//           7 Series
// Xilinx HDL Libraries Guide, version 2012.2

DCIRESET DCIRESET_inst (
   .LOCKED(LOCKED), // 1-bit output: LOCK status output
   .RST(RST)        // 1-bit input: Active-high asynchronous reset input
);

// End of DCIRESET_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

DNA_PORT

Primitive: Device DNA Access Port



Introduction

The DNA_PORT allows access to a dedicated shift register that can be loaded with the Device DNA data bits (factory-programmed, read-only unique ID) for a given 7 series device. In addition to shifting out the DNA data bits, this component allows for the inclusion of supplemental bits of your data, or allows for the DNA data to rollover (repeat DNA data after initial data has been shifted out). This component is primarily used in conjunction with other circuitry to build added copy protection for the FPGA bitstream from possible theft. Connect all inputs and outputs to the design to ensure proper operation. To access the Device DNA data, you must first load the shift register by setting the active high READ signal for one clock cycle. After the shift register is loaded, the data can be synchronously shifted out by enabling the active high SHIFT input and capturing the data out the DOUT output port. Additional data can be appended to the end of the 57-bit shift register by connecting the appropriate logic to the DIN port. If DNA data rollover is desired, connect the DOUT port directly to the DIN port to allow for the same data to be shifted out after completing the 57-bit shift operation. If no additional data is necessary, the DIN port can be tied to a logic zero. The attribute SIM_DNA_VALUE can be optionally set to allow for simulation of a possible DNA data sequence. By default, the Device DNA data bits are all zeros in the simulation model.

Port Descriptions

Port	Type	Width	Function
CLK	Input	1	Clock input.
DIN	Input	1	User data input pin.
DOUT	Output	1	DNA output data.
READ	Input	1	Active high load DNA, active low read input.
SHIFT	Input	1	Active high shift enable input.

Design Entry Method

Instantiation	Recommended
Inference	No
CORE Generator™ and wizards	No
Macro support	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
SIM_DNA _VALUE	HEX	57'h0000000000000000 to 57'h1ffffffffffffff	57'h0000000000000000	Specifies a sample 57-bit DNA value for simulation

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- DNA_PORT: Device DNA Access Port
--           7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

DNA_PORT_inst : DNA_PORT
generic map (
   SIM_DNA_VALUE => X"000000000000000"  -- Specifies a sample 57-bit DNA value for simulation
)
port map (
   DOUT => DOUT,   -- 1-bit output: DNA output data.
   CLK => CLK,     -- 1-bit input: Clock input.
   DIN => DIN,     -- 1-bit input: User data input pin.
   READ => READ,   -- 1-bit input: Active high load DNA, active low read input.
   SHIFT => SHIFT  -- 1-bit input: Active high shift enable input.
);

-- End of DNA_PORT_inst instantiation
```

Verilog Instantiation Template

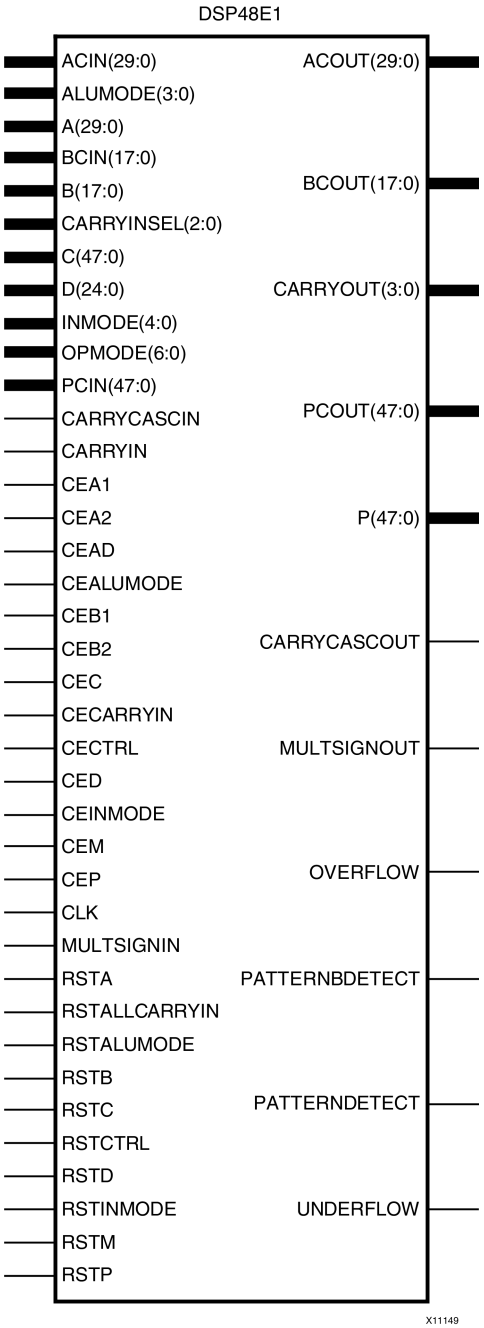
```
// DNA_PORT: Device DNA Access Port
//           7 Series
// Xilinx HDL Libraries Guide, version 2012.2

DNA_PORT #(
   .SIM_DNA_VALUE(57'h000000000000000)  // Specifies a sample 57-bit DNA value for simulation
)
DNA_PORT_inst (
   .DOUT(DOUT),   // 1-bit output: DNA output data.
   .CLK(CLK),     // 1-bit input: Clock input.
   .DIN(DIN),     // 1-bit input: User data input pin.
   .READ(READ),   // 1-bit input: Active high load DNA, active low read input.
   .SHIFT(SHIFT)  // 1-bit input: Active high shift enable input.
);

// End of DNA_PORT_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

DSP48E1

Primitive: 48-bit Multi-Functional Arithmetic Block



Introduction

This design element is a versatile, scalable, hard IP block within 7 series devices that allows for the creation of compact, high-speed, arithmetic-intensive operations, such as those seen for many DSP algorithms. Some of the functions capable within the block include multiplication, addition, subtraction, accumulation, shifting, logical operations and pattern detection.

Port Descriptions

Port	Type	Width	Function
A<29:0>	Input	30	Data input for preadder, multiplier, adder/subtractor/accumulator, ALU or concatenation operations. When used with the multiplier or preadder, 25 bits of data (A[24:0]) is used and upper bits (A[29:25]) are unused and may be tied to ground. When using the internal adder/subctractor/accumulator or ALU circuit, all 30 bits are used (A[29:0]). When used in concatenation mode, all 30 bits are used and this constitutes the MSB (upper) bits of the concatenated vector.
ACIN<29:0>	Input	30	Cascaded data input from ACOUT of previous DSP48E1 slice (muxed with A). If not used, tie port to all zeros.
ACOUT<29:0>	Output	30	Cascaded data output to ACIN of next DSP48E1 slice. If not used, leave unconnected.
ALUMODE<3:0>	Input	4	Controls the selection of the logic function in the DSP48E1 slice.
B<17:0>	Input	18	The B input of the multiplier. B[17:0] are the least significant bits (LSBs) of the A:B concatenated input to the second-stage adder/subtracter or logic function.
BCIN<17:0>	Input	18	Cascaded data input from BCOUT of previous DSP48E1 slice (muxed with B). If not used, tie port to all zeros.
BCOUT<17:0>	Output	18	Cascaded data output to BCIN of next DSP48E1 slice. If not used, leave unconnected.
C<47:0>	Input	48	Data input to the second-stage adder/subtracter, pattern detector, or logic function.
CARRYCASCIN	Input	1	Cascaded carry input from CARRYCASCOUT of previous DSP48E1 slice.
CARRYCASCOUT	Output	1	Cascaded carry output to CARRYCASCIN of next DSP48E1 slice. This signal is internally fed back into the CARRYINSEL multiplexer input of the same DSP48E1 slice.
CARRYIN	Input	1	Carry input from the FPGA logic.

Port	Type	Width	Function
CARRYINSEL< 2:0>	Input	3	Selects the carry source: • 0 1 1 - PCIN[47] - Rounding PCIN (round towards zero) • 1 0 0 - CARRYCASCOUT - For larger add/sub/acc (sequential operation via internal feedback). Must select with PREG=1 • 1 0 1 - ~P[47] - Rounding P (round towards infinity). Must select with PREG=1 • 1 1 0 - A[24] - XNOR B[17] Rounding A x B • 1 1 1 - P[47] - For rounding P (round towards zero). Must select with PREG=1
CARRYOUT<3: 0>	Output	4	4-bit carry output from each 12-bit field of the accumulate/adder/logic unit. Normal 48-bit operation uses only CARRYOUT3. SIMD operation can use four carry out bits (CARRYOUT[3:0]).
CEAD	Input	1	Active high, clock enable for the pre-adder output AD pipeline register. Tie to logic one if not used and ADREG=1. Tie to logic zero if ADREG=0.
CEALUMODE	Input	1	Active High, clock enable for ALUMODE (control inputs) registers (ALUMODEREG=1). Tie to logic one if not used.
CEA1	Input	1	Active high, clock enable for the first A (input) register. This port is only used if AREG=2 or INMODE0 = 1. Tie to logic one if not used and AREG=2. Tie to logic zero if AREG=0 or 1. When two registers are used, this is the first sequentially. When Dynamic AB Access is used, this clock enable is applied for INMODE[0]=1.
CEA2	Input	1	Active high, clock enable for the second A (input) register. This port is only used if AREG=1 or 2. Tie to logic one if not used and AREG=1 or 2. Tie to logic zero if AREG=0. When two registers are used, this is the second sequentially. When one register is used (AREG=1), CEA2 is the clock enable.
CEB1	Input	1	Active high, Clock enable for the first B (input) register. This port is only used if BREG=2 or INMODE4=1. Tie to logic one if not used and BREG=2. Tie to logic zero if BREG=0 or 1. When two registers are used, this is the first sequentially. When Dynamic AB Access is used, this clock enable is applied for INMODE[4]=1.
CEB2	Input	1	Active high, clock enable for the second B (input) register. This port is only used if BREG=1 or 2. Tie to logic one if not used and BREG=1 or 2. Tie to logic zero if BREG=0. When two registers are used, this is the second sequentially. When one register isused (BREG=1), CEB2 is the clock enable.
CEC	Input	1	Active High, Clock enable for the C (input) register (CREG=1). Tie to logic one if not used.
CECARRYIN	Input	1	Active high, clock enable for the CARRYIN (input from fabric) register (CARRYINREG=1). Tie to logic one if not used.
CECTRL	Input	1	Active high, clock enable for the OPMODE and CARRYINSEL (control inputs) registers (OPMODEREG=1 or CARRYINSELREG=1). Tie to logic one if not used.

Port	Type	Width	Function
CED	Input	1	Active high, Clock enable for the D (input) registers (DREG=1). Tie to logic one if not used.
CEINMODE	Input	1	Active high, clock enable for the INMODE control input registers (INMODEREG=1). Tie to logic one if not used.
CEM	Input	1	Active high, Clock enable for the post-multiply M (pipeline) register and the internal multiply round CARRYIN register (MREG=1). Tie to logic one if not used.
CEP	Input	1	Active high, clock enable for the P (output) register (PREG=1). Tie to logic one if not used.
CLK	Input	1	This port is the DSP48E1 input clock, common to all internal registers and flip-flops.
D<24:0>	Input	25	25-bit data input to the pre-adder or alternative input to the multiplier. The pre-adder implements D + A as determined by the INMODE3 signal.
INMODE<4:0>	Input	5	These five control bits select the functionality of the pre-adder, the A, B, and D inputs, and the input registers. These bits should be tied to all zeroes if not used.
MULTSIGNIN	Input	1	Sign of the multiplied result from the previous DSP48E1 slice for MACC extension. Either connect to the MULTSIGNOUT of another DSP block or tie to ground if not used.
MULTSIGNOUT	Output	1	Sign of the multiplied result cascaded to the next DSP48E1 slice for MACC extension. Either connect to the MULTSIGNIN of another DSP block or tie to ground if not used.
OPMODE<6:0>	Input	7	Controls the input to the X, Y, and Z multiplexers in the DSP48E1 slice dictating the operation or function of the DSP slice.
OVERFLOW	Output	1	Active high Overflow indicator when used with the appropriate setting of the pattern detector and PREG=1.
P<47:0>	Output	48	Data output from second stage adder/subtracter or logic function.
PATTERNBDET ECT	Output	1	Active high match indicator between P[47:0] and the pattern bar.
PATTERNDETE CT	Output	1	Active high Match indicator between P[47:0] and the pattern gated by the MASK. Result arrives on the same cycle as P.
PCIN<47:0>	Input	48	Cascaded data input from PCOUT of previous DSP48E1 slice to adder. If used, connect to PCOUT of upstream cascaded DSP slice. If not used, tie port to all zeros.
PCOUT<47:0>	Output	48	Cascaded data output to PCIN of next DSP48E1 slice. If used, connect to PCIN of downstream cascaded DSP slice. If not used, leave unconnected.
RSTA	Input	1	Active high, synchronous Reset for both A (input) registers (AREG=1 or 2). Tie to logic zero if not used.
RSTALLCARRY IN	Input	1	Active high, synchronous reset for the Carry (internal path) and the CARRYIN registers (CARRYINREG=1). Tie to logic zero if not used.

Port	Type	Width	Function
RSTALUMODE	Input	1	Active high, synchronous Reset for ALUMODE (control inputs) registers (ALUMODEREG=1). Tie to logic zero if not used.
RSTB	Input	1	Active high, synchronous Reset for both B (input) registers (BREG=1 or 2). Tie to logic zero if not used.
RSTC	Input	1	Active high, synchronous reset for the C (input) registers (CREG=1). Tie to logic zero if not used.
RSTCTRL	Input	1	Active High, synchronous reset for OPMODE and CARRYINSEL (control inputs) registers (OPMODEREG=1 and/or CARRYINSELREG=1). Tie to logic zero if not used.
RSTD	Input	1	Active high, synchronous reset for the D (input) register and for the pre-adder (output) AD pipeline register (DREG=1 and/or ADREG=1). Tie to logic zero if not used.
RSTINMODE	Input	1	Active high, synchronous reset for the INMODE (control input) registers (INMODEREG=1). Tie to logic zero if not used.
RSTM	Input	1	Active high, synchronous reset for the M (pipeline) registers (MREG=1). Tie to logic zero if not used.
RSTP	Input	1	Active high, synchronous reset for the P (output) registers (PREG=1). Tie to logic zero if not used.
UNDERFLOW	Output	1	Active high underflow indicator when used with the appropriate setting of the pattern detector and PREG=1.

Design Entry Method

Instantiation	Yes
Inference	Recommended
CORE Generator™ and wizards	Yes
Macro support	Yes

Available Attributes

Attribute	Type	Allowed Values	Default	Description
ACASCREG	DECIMAL	1, 0, 2	1	In conjunction with AREG, selects the number of A input registers on the A cascade path, ACOUT. This attribute must be equal to or one less than the AREG value: AREG=0: ACASCREG must be 0 AREG=1: ACASCREG must be 1 AREG=2: ACASCREG can be 1 or 2
ADREG	DECIMAL	1, 0	1	Selects the number of AD pipeline registers. Set to 1 to use the AD pipeline registers.
A_INPUT	STRING	"DIRECT", "CASCADE"	"DIRECT"	Selects the input to the A port between parallel input ("DIRECT") or the cascaded input from the previous slice ("CASCADE").

Attribute	Type	Allowed Values	Default	Description
ALUMODEREG	DECIMAL	1, 0	1	Selects the number of ALUMODE input registers. Set to 1 to register the ALUMODE inputs.
AREG	DECIMAL	1, 0, 2	1	Selects the number of A input pipeline registers.
AUTORESET _PATDET	STRING	"NO_RESET", "RESET_MATCH", "RESET_NOT_MATCH"	"NO_RESET"	Automatically resets the P Register (accumulated value or counter value) on the next clock cycle, if a pattern detect event has occurred on this clock cycle. The "RESET_MATCH" and "RESET_NOT_MATCH" settings distinguish between whether the DSP48E1 slice should cause an auto reset of the P Register on the next cycle: - if the pattern is matched or - whenever the pattern is not matched on the current cycle but was matched on the previous clock cycle.
BCASCREG	DECIMAL	1, 0, 2	1	In conjunction with BREG, selects the number of B input registers on the B cascade path, BCOUT. This attribute must be equal to or one less than the BREG value: BREG=0: BCASCREG must be 0 BREG=1: BCASCREG must be 1 BREG=2: BCASCREG can be 1 or 2
B_INPUT	STRING	"DIRECT", "CASCADE"	"DIRECT"	Selects the input to the B port between parallel input ("DIRECT") or the cascaded input from the previous slice ("CASCADE").
BREG	DECIMAL	1, 0, 2	1	Selects the number of B input registers.
CARRYINREG	DECIMAL	1, 0	1	Selects the number of CARRYIN input registers. Set to 1 to register the CARRYIN inputs.
CARRYINSELR EG	DECIMAL	1, 0	1	Selects the number of CARRYINSEL input registers. Set to 1 to register the CARRYINSEL inputs.
CREG	DECIMAL	1, 0	1	Selects the number of C input registers. Set to 1 to register the C inputs.
DREG	DECIMAL	1, 0	1	Selects the number of D input registers. Set to 1 to register the D inputs.
INMODEREG	DECIMAL	1, 0	1	Selects the number of INMODE input registers. Set to 1 to register the INMODE inputs.
MASK	HEX	48'h000000000000 to 48'hffffffffffff	48'h3fffffffffff	This 48-bit value is used to mask out certain bits during a pattern detection. When a MASK bit is set to 1, the corresponding pattern bit is ignored. When a MASK bit is set to 0, the pattern bit is compared.
MREG	DECIMAL	1, 0	1	Selects the number of multiplier output (M) pipeline register stages. Set to 1 to use the M pipeline registers.

Attribute	Type	Allowed Values	Default	Description
OPMODEREG	DECIMAL	1, 0	1	Selects the number of OPMODE input registers. Set to 1 to register the OPMODE inputs.
PATTERN	HEX	48'h000000000000 to 48'hffffffffffff	48'h000000000000	This 48-bit value is used in the pattern detector.
PREG	DECIMAL	1, 0	1	Selects the number of P output registers. Set to 1 to register the P outputs. The registered outputs will include CARRYOUT, CARRYCASCOUT, MULTSIGNOUT, PATTERNB_DETECT, PATTERN_DETECT, and PCOUT.
SEL_MASK	STRING	"MASK", "C", "ROUNDING_MODE1", "ROUNDING_MODE2"	"MASK"	Selects the mask to be used for the pattern detector. The C and MASK settings are for standard uses of the pattern detector (counter, overflow detection, etc.). ROUNDING_MODE1 (Cbar left shifted by 1) and ROUNDING_MODE2 (C-bar left shifted by 2) select special masks based off of the optionally registered C port. These rounding modes can be used to implement convergent rounding in the DSP48E1 slice using the pattern detector.
SEL_PATTERN	STRING	"PATTERN", "C"	"PATTERN"	Selects the input source for the pattern field. The input source can either be a 48-bit dynamic C input or a 48-bit static PATTERN attribute field.
USE_DPORT	BOOLEAN	FALSE, TRUE	FALSE	Determines whether the pre-adder and the D Port are used or not.
USE_MULT	STRING	"MULTIPLY", "DYNAMIC", "NONE"	"MULTIPLY"	Selects usage of the multiplier. Set to "NONE" to save power when using only the Adder/Logic Unit. The "DYNAMIC" setting indicates that the user is switching between A*B and A:B operations on the fly and therefore needs to get the worst-case timing of the two paths.
USE_PATTERN_DETECT	STRING	"NO_PATDET", "PATDET"	"NO_PATDET"	Selects whether the pattern detector and related features are used ("PATDET") or not used ("NO_PATDET"). This attribute is used for speed specification and Simulation Model purposes only.
USE_SIMD	STRING	"ONE48", "FOUR12", "TWO24"	"ONE48"	Selects the mode of operation for the adder/subtracter. The attribute setting can be one 48-bit adder mode ("ONE48"), two 24- bit adder mode ("TWO24"), or four 12-bit adder mode ("FOUR12"). Selecting "ONE48" mode is compatible with Virtex-5 DSP48 operation and is not actually a true SIMD mode. Typical Multiply-Add operations are supported when the mode is set to "ONE48". When either "TWO24" or "FOUR12" mode is selected, the multiplier must not be used, and USE_MULT must be set to "NONE".

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- DSP48E1: 48-bit Multi-Functional Arithmetic Block
--          7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

DSP48E1_inst : DSP48E1
generic map (
   -- Feature Control Attributes: Data Path Selection
   A_INPUT => "DIRECT",               -- Selects A input source, "DIRECT" (A port) or "CASCADE" (ACIN port)
   B_INPUT => "DIRECT",               -- Selects B input source, "DIRECT" (B port) or "CASCADE" (BCIN port)
   USE_DPORT => FALSE,                -- Select D port usage (TRUE or FALSE)
   USE_MULT => "MULTIPLY",            -- Select multiplier usage ("MULTIPLY", "DYNAMIC", or "NONE")
   -- Pattern Detector Attributes: Pattern Detection Configuration
   AUTORESET_PATDET => "NO_RESET",    -- "NO_RESET", "RESET_MATCH", "RESET_NOT_MATCH"
   MASK => X"3fffffffffff",           -- 48-bit mask value for pattern detect (1=ignore)
   PATTERN => X"000000000000",        -- 48-bit pattern match for pattern detect
   SEL_MASK => "MASK",                -- "C", "MASK", "ROUNDING_MODE1", "ROUNDING_MODE2"
   SEL_PATTERN => "PATTERN",          -- Select pattern value ("PATTERN" or "C")
   USE_PATTERN_DETECT => "NO_PATDET", -- Enable pattern detect ("PATDET" or "NO_PATDET")
   -- Register Control Attributes: Pipeline Register Configuration
   ACASCREG => 1,                     -- Number of pipeline stages between A/ACIN and ACOUT (0, 1 or 2)
   ADREG => 1,                        -- Number of pipeline stages for pre-adder (0 or 1)
   ALUMODEREG => 1,                   -- Number of pipeline stages for ALUMODE (0 or 1)
   AREG => 1,                         -- Number of pipeline stages for A (0, 1 or 2)
   BCASCREG => 1,                     -- Number of pipeline stages between B/BCIN and BCOUT (0, 1 or 2)
   BREG => 1,                         -- Number of pipeline stages for B (0, 1 or 2)
   CARRYINREG => 1,                   -- Number of pipeline stages for CARRYIN (0 or 1)
   CARRYINSELREG => 1,                -- Number of pipeline stages for CARRYINSEL (0 or 1)
   CREG => 1,                         -- Number of pipeline stages for C (0 or 1)
   DREG => 1,                         -- Number of pipeline stages for D (0 or 1)
   INMODEREG => 1,                    -- Number of pipeline stages for INMODE (0 or 1)
   MREG => 1,                         -- Number of multiplier pipeline stages (0 or 1)
   OPMODEREG => 1,                    -- Number of pipeline stages for OPMODE (0 or 1)
   PREG => 1,                         -- Number of pipeline stages for P (0 or 1)
   USE_SIMD => "ONE48"                -- SIMD selection ("ONE48", "TWO24", "FOUR12")
)
port map (
   -- Cascade: 30-bit (each) output: Cascade Ports
   ACOUT => ACOUT,                    -- 30-bit output: A port cascade output
   BCOUT => BCOUT,                    -- 18-bit output: B port cascade output
   CARRYCASCOUT => CARRYCASCOUT,      -- 1-bit output: Cascade carry output
   MULTSIGNOUT => MULTSIGNOUT,        -- 1-bit output: Multiplier sign cascade output
   PCOUT => PCOUT,                    -- 48-bit output: Cascade output
   -- Control: 1-bit (each) output: Control Inputs/Status Bits
   OVERFLOW => OVERFLOW,              -- 1-bit output: Overflow in add/acc output
   PATTERNBDETECT => PATTERNBDETECT,  -- 1-bit output: Pattern bar detect output
   PATTERNDETECT => PATTERNDETECT,    -- 1-bit output: Pattern detect output
   UNDERFLOW => UNDERFLOW,            -- 1-bit output: Underflow in add/acc output
   -- Data: 4-bit (each) output: Data Ports
   CARRYOUT => CARRYOUT,              -- 4-bit output: Carry output
   P => P,                            -- 48-bit output: Primary data output
   -- Cascade: 30-bit (each) input: Cascade Ports
   ACIN => ACIN,                      -- 30-bit input: A cascade data input
   BCIN => BCIN,                      -- 18-bit input: B cascade input
   CARRYCASCIN => CARRYCASCIN,        -- 1-bit input: Cascade carry input
   MULTSIGNIN => MULTSIGNIN,          -- 1-bit input: Multiplier sign input
   PCIN => PCIN,                      -- 48-bit input: P cascade input
   -- Control: 4-bit (each) input: Control Inputs/Status Bits
   ALUMODE => ALUMODE,                -- 4-bit input: ALU control input
   CARRYINSEL => CARRYINSEL,          -- 3-bit input: Carry select input
   CEINMODE => CEINMODE,              -- 1-bit input: Clock enable input for INMODEREG
   CLK => CLK,                        -- 1-bit input: Clock input
   INMODE => INMODE,                  -- 5-bit input: INMODE control input
   OPMODE => OPMODE,                  -- 7-bit input: Operation mode input
```

```
   RSTINMODE => RSTINMODE,           -- 1-bit input: Reset input for INMODEREG
   -- Data: 30-bit (each) input: Data Ports
   A => A,                           -- 30-bit input: A data input
   B => B,                           -- 18-bit input: B data input
   C => C,                           -- 48-bit input: C data input
   CARRYIN => CARRYIN,               -- 1-bit input: Carry input signal
   D => D,                           -- 25-bit input: D data input
   -- Reset/Clock Enable: 1-bit (each) input: Reset/Clock Enable Inputs
   CEA1 => CEA1,                     -- 1-bit input: Clock enable input for 1st stage AREG
   CEA2 => CEA2,                     -- 1-bit input: Clock enable input for 2nd stage AREG
   CEAD => CEAD,                     -- 1-bit input: Clock enable input for ADREG
   CEALUMODE => CEALUMODE,           -- 1-bit input: Clock enable input for ALUMODERE
   CEB1 => CEB1,                     -- 1-bit input: Clock enable input for 1st stage BREG
   CEB2 => CEB2,                     -- 1-bit input: Clock enable input for 2nd stage BREG
   CEC => CEC,                       -- 1-bit input: Clock enable input for CREG
   CECARRYIN => CECARRYIN,           -- 1-bit input: Clock enable input for CARRYINREG
   CECTRL => CECTRL,                 -- 1-bit input: Clock enable input for OPMODEREG and CARRYINSELREG
   CED => CED,                       -- 1-bit input: Clock enable input for DREG
   CEM => CEM,                       -- 1-bit input: Clock enable input for MREG
   CEP => CEP,                       -- 1-bit input: Clock enable input for PREG
   RSTA => RSTA,                     -- 1-bit input: Reset input for AREG
   RSTALLCARRYIN => RSTALLCARRYIN,   -- 1-bit input: Reset input for CARRYINREG
   RSTALUMODE => RSTALUMODE,         -- 1-bit input: Reset input for ALUMODEREG
   RSTB => RSTB,                     -- 1-bit input: Reset input for BREG
   RSTC => RSTC,                     -- 1-bit input: Reset input for CREG
   RSTCTRL => RSTCTRL,               -- 1-bit input: Reset input for OPMODEREG and CARRYINSELREG
   RSTD => RSTD,                     -- 1-bit input: Reset input for DREG and ADREG
   RSTM => RSTM,                     -- 1-bit input: Reset input for MREG
   RSTP => RSTP                      -- 1-bit input: Reset input for PREG
);

-- End of DSP48E1_inst instantiation
```

Verilog Instantiation Template

```
// DSP48E1: 48-bit Multi-Functional Arithmetic Block
//          7 Series
// Xilinx HDL Libraries Guide, version 2012.2

DSP48E1 #(
   // Feature Control Attributes: Data Path Selection
   .A_INPUT("DIRECT"),               // Selects A input source, "DIRECT" (A port) or "CASCADE" (ACIN port)
   .B_INPUT("DIRECT"),               // Selects B input source, "DIRECT" (B port) or "CASCADE" (BCIN port)
   .USE_DPORT("FALSE"),              // Select D port usage (TRUE or FALSE)
   .USE_MULT("MULTIPLY"),            // Select multiplier usage ("MULTIPLY", "DYNAMIC", or "NONE")
   // Pattern Detector Attributes: Pattern Detection Configuration
   .AUTORESET_PATDET("NO_RESET"),    // "NO_RESET", "RESET_MATCH", "RESET_NOT_MATCH"
   .MASK(48'h3fffffffffff),          // 48-bit mask value for pattern detect (1=ignore)
   .PATTERN(48'h000000000000),       // 48-bit pattern match for pattern detect
   .SEL_MASK("MASK"),                // "C", "MASK", "ROUNDING_MODE1", "ROUNDING_MODE2"
   .SEL_PATTERN("PATTERN"),          // Select pattern value ("PATTERN" or "C")
   .USE_PATTERN_DETECT("NO_PATDET"), // Enable pattern detect ("PATDET" or "NO_PATDET")
   // Register Control Attributes: Pipeline Register Configuration
   .ACASCREG(1),                     // Number of pipeline stages between A/ACIN and ACOUT (0, 1 or 2)
   .ADREG(1),                        // Number of pipeline stages for pre-adder (0 or 1)
   .ALUMODEREG(1),                   // Number of pipeline stages for ALUMODE (0 or 1)
   .AREG(1),                         // Number of pipeline stages for A (0, 1 or 2)
   .BCASCREG(1),                     // Number of pipeline stages between B/BCIN and BCOUT (0, 1 or 2)
   .BREG(1),                         // Number of pipeline stages for B (0, 1 or 2)
   .CARRYINREG(1),                   // Number of pipeline stages for CARRYIN (0 or 1)
   .CARRYINSELREG(1),                // Number of pipeline stages for CARRYINSEL (0 or 1)
   .CREG(1),                         // Number of pipeline stages for C (0 or 1)
   .DREG(1),                         // Number of pipeline stages for D (0 or 1)
   .INMODEREG(1),                    // Number of pipeline stages for INMODE (0 or 1)
   .MREG(1),                         // Number of multiplier pipeline stages (0 or 1)
   .OPMODEREG(1),                    // Number of pipeline stages for OPMODE (0 or 1)
   .PREG(1),                         // Number of pipeline stages for P (0 or 1)
   .USE_SIMD("ONE48")                // SIMD selection ("ONE48", "TWO24", "FOUR12")
)
DSP48E1_inst (
```

```
   // Cascade: 30-bit (each) output: Cascade Ports
   .ACOUT(ACOUT),                   // 30-bit output: A port cascade output
   .BCOUT(BCOUT),                   // 18-bit output: B port cascade output
   .CARRYCASCOUT(CARRYCASCOUT),     // 1-bit output: Cascade carry output
   .MULTSIGNOUT(MULTSIGNOUT),       // 1-bit output: Multiplier sign cascade output
   .PCOUT(PCOUT),                   // 48-bit output: Cascade output
   // Control: 1-bit (each) output: Control Inputs/Status Bits
   .OVERFLOW(OVERFLOW),             // 1-bit output: Overflow in add/acc output
   .PATTERNBDETECT(PATTERNBDETECT), // 1-bit output: Pattern bar detect output
   .PATTERNDETECT(PATTERNDETECT),   // 1-bit output: Pattern detect output
   .UNDERFLOW(UNDERFLOW),           // 1-bit output: Underflow in add/acc output
   // Data: 4-bit (each) output: Data Ports
   .CARRYOUT(CARRYOUT),             // 4-bit output: Carry output
   .P(P),                           // 48-bit output: Primary data output
   // Cascade: 30-bit (each) input: Cascade Ports
   .ACIN(ACIN),                     // 30-bit input: A cascade data input
   .BCIN(BCIN),                     // 18-bit input: B cascade input
   .CARRYCASCIN(CARRYCASCIN),       // 1-bit input: Cascade carry input
   .MULTSIGNIN(MULTSIGNIN),         // 1-bit input: Multiplier sign input
   .PCIN(PCIN),                     // 48-bit input: P cascade input
   // Control: 4-bit (each) input: Control Inputs/Status Bits
   .ALUMODE(ALUMODE),               // 4-bit input: ALU control input
   .CARRYINSEL(CARRYINSEL),         // 3-bit input: Carry select input
   .CEINMODE(CEINMODE),             // 1-bit input: Clock enable input for INMODEREG
   .CLK(CLK),                       // 1-bit input: Clock input
   .INMODE(INMODE),                 // 5-bit input: INMODE control input
   .OPMODE(OPMODE),                 // 7-bit input: Operation mode input
   .RSTINMODE(RSTINMODE),           // 1-bit input: Reset input for INMODEREG
   // Data: 30-bit (each) input: Data Ports
   .A(A),                           // 30-bit input: A data input
   .B(B),                           // 18-bit input: B data input
   .C(C),                           // 48-bit input: C data input
   .CARRYIN(CARRYIN),               // 1-bit input: Carry input signal
   .D(D),                           // 25-bit input: D data input
   // Reset/Clock Enable: 1-bit (each) input: Reset/Clock Enable Inputs
   .CEA1(CEA1),                     // 1-bit input: Clock enable input for 1st stage AREG
   .CEA2(CEA2),                     // 1-bit input: Clock enable input for 2nd stage AREG
   .CEAD(CEAD),                     // 1-bit input: Clock enable input for ADREG
   .CEALUMODE(CEALUMODE),           // 1-bit input: Clock enable input for ALUMODERE
   .CEB1(CEB1),                     // 1-bit input: Clock enable input for 1st stage BREG
   .CEB2(CEB2),                     // 1-bit input: Clock enable input for 2nd stage BREG
   .CEC(CEC),                       // 1-bit input: Clock enable input for CREG
   .CECARRYIN(CECARRYIN),           // 1-bit input: Clock enable input for CARRYINREG
   .CECTRL(CECTRL),                 // 1-bit input: Clock enable input for OPMODEREG and CARRYINSELREG
   .CED(CED),                       // 1-bit input: Clock enable input for DREG
   .CEM(CEM),                       // 1-bit input: Clock enable input for MREG
   .CEP(CEP),                       // 1-bit input: Clock enable input for PREG
   .RSTA(RSTA),                     // 1-bit input: Reset input for AREG
   .RSTALLCARRYIN(RSTALLCARRYIN),   // 1-bit input: Reset input for CARRYINREG
   .RSTALUMODE(RSTALUMODE),         // 1-bit input: Reset input for ALUMODEREG
   .RSTB(RSTB),                     // 1-bit input: Reset input for BREG
   .RSTC(RSTC),                     // 1-bit input: Reset input for CREG
   .RSTCTRL(RSTCTRL),               // 1-bit input: Reset input for OPMODEREG and CARRYINSELREG
   .RSTD(RSTD),                     // 1-bit input: Reset input for DREG and ADREG
   .RSTM(RSTM),                     // 1-bit input: Reset input for MREG
   .RSTP(RSTP)                      // 1-bit input: Reset input for PREG
);

// End of DSP48E1_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

EFUSE_USR

Primitive: 32-bit non-volatile design ID

Introduction

Provides internal access to the 32 non-volatile, user-programmable eFUSE bits

Port Descriptions

Port	Type	Width	Function
EFUSEUSR<31 :0>	Output	32	User eFUSE register value output

Design Entry Method

Instantiation	Recommended
Inference	No
CORE Generator™ and wizards	No
Macro support	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
SIM_EFUSE _VALUE	HEX	32'h00000000 to 32'hffffffff	32'h00000000	Value of the 32-bit non-volatile value used in simulation

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- EFUSE_USR: 32-bit non-volatile design ID
--            7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

EFUSE_USR_inst : EFUSE_USR
generic map (
   SIM_EFUSE_VALUE => X"00000000"  -- Value of the 32-bit non-volatile value used in simulation
)
port map (
   EFUSEUSR => EFUSEUSR  -- 32-bit output: User eFUSE register value output
);
```

```
-- End of EFUSE_USR_inst instantiation
```

Verilog Instantiation Template

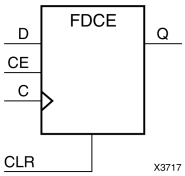
```
// EFUSE_USR: 32-bit non-volatile design ID
//            7 Series
// Xilinx HDL Libraries Guide, version 2012.2

EFUSE_USR #(
   .SIM_EFUSE_VALUE(32'h00000000)  // Value of the 32-bit non-volatile value used in simulation
)
EFUSE_USR_inst (
   .EFUSEUSR(EFUSEUSR)  // 32-bit output: User eFUSE register value output
);

// End of EFUSE_USR_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

FDCE

Primitive: D Flip-Flop with Clock Enable and Asynchronous Clear



Introduction

This design element is a single D-type flip-flop with clock enable and asynchronous clear. When clock enable (CE) is High and asynchronous clear (CLR) is Low, the data on the data input (D) of this design element is transferred to the corresponding data output (Q) during the Low-to-High clock (C) transition. When CLR is High, it overrides all other inputs and resets the data output (Q) Low. When CE is Low, clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_E2 symbol.

Logic Table

Inputs				Outputs
CLR	**CE**	**D**	**C**	**Q**
1	X	X	X	0
0	0	X	X	No Change
0	1	D	↑	D

Design Entry Method

Instantiation	Yes
Inference	Recommended
CORE Generator™ and wizards	No
Macro support	No

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	1, 0	0	Sets the initial value of Q output after configuration.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- FDCE: Single Data Rate D Flip-Flop with Asynchronous Clear and
--       Clock Enable (posedge clk).
--       7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

FDCE_inst : FDCE
generic map (
   INIT => '0') -- Initial value of register ('0' or '1')
port map (
   Q => Q,      -- Data output
   C => C,      -- Clock input
   CE => CE,    -- Clock enable input
   CLR => CLR,  -- Asynchronous clear input
   D => D       -- Data input
);

-- End of FDCE_inst instantiation
```

Verilog Instantiation Template

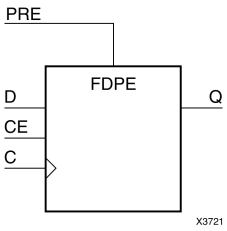
```
// FDCE: Single Data Rate D Flip-Flop with Asynchronous Clear and
//       Clock Enable (posedge clk).
//       7 Series
// Xilinx HDL Libraries Guide, version 2012.2

FDCE #(
   .INIT(1'b0) // Initial value of register (1'b0 or 1'b1)
) FDCE_inst (
   .Q(Q),      // 1-bit Data output
   .C(C),      // 1-bit Clock input
   .CE(CE),    // 1-bit Clock enable input
   .CLR(CLR),  // 1-bit Asynchronous clear input
   .D(D)       // 1-bit Data input
);

// End of FDCE_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

FDPE

Primitive: D Flip-Flop with Clock Enable and Asynchronous Preset



Introduction

This design element is a single D-type flip-flop with data (D), clock enable (CE), and asynchronous preset (PRE) inputs and data output (Q). The asynchronous PRE, when High, overrides all other inputs and sets the (Q) output High. Data on the (D) input is loaded into the flip-flop when PRE is Low and CE is High on the Low-to-High clock (C) transition. When CE is Low, the clock transitions are ignored.

For FPGA devices, this flip-flop is asynchronously preset, output High, when power is applied. Power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_E2 symbol.

Logic Table

Inputs				Outputs
PRE	**CE**	**D**	**C**	**Q**
1	X	X	X	1
0	0	X	X	No Change
0	1	D	↑	D

Design Entry Method

Instantiation	Yes
Inference	Recommended
CORE Generator™ and wizards	No
Macro support	No

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- FDPE: Single Data Rate D Flip-Flop with Asynchronous Preset and
--       Clock Enable (posedge clk).
--       7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

FDPE_inst : FDPE
generic map (
   INIT => '0') -- Initial value of register ('0' or '1')
port map (
   Q => Q,      -- Data output
   C => C,      -- Clock input
   CE => CE,    -- Clock enable input
   PRE => PRE,  -- Asynchronous preset input
   D => D       -- Data input
);

-- End of FDPE_inst instantiation
```

Verilog Instantiation Template

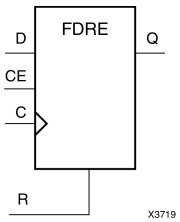
```
// FDPE: Single Data Rate D Flip-Flop with Asynchronous Preset and
//       Clock Enable (posedge clk).
//       7 Series
// Xilinx HDL Libraries Guide, version 2012.2

FDPE #(
   .INIT(1'b0) // Initial value of register (1'b0 or 1'b1)
) FDPE_inst (
   .Q(Q),      // 1-bit Data output
   .C(C),      // 1-bit Clock input
   .CE(CE),    // 1-bit Clock enable input
   .PRE(PRE),  // 1-bit Asynchronous preset input
   .D(D)       // 1-bit Data input
);

// End of FDPE_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

FDRE

Primitive: D Flip-Flop with Clock Enable and Synchronous Reset



Introduction

This design element is a single D-type flip-flop with data (D), clock enable (CE), and synchronous reset (R) inputs and data output (Q). The synchronous reset (R) input, when High, overrides all other inputs and resets the (Q) output Low on the Low-to-High clock (C) transition. The data on the (D) input is loaded into the flip-flop when R is Low and CE is High during the Low-to-High clock transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_E2 symbol.

Logic Table

Inputs				Outputs
R	**CE**	**D**	**C**	**Q**
1	X	X	↑	0
0	0	X	X	No Change
0	1	D	↑	D

Design Entry Method

Instantiation	Yes
Inference	Recommended
CORE Generator™ and wizards	No
Macro support	No

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- FDRE: Single Data Rate D Flip-Flop with Synchronous Reset and
--       Clock Enable (posedge clk).
--       7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

FDRE_inst : FDRE
generic map (
   INIT => '0') -- Initial value of register ('0' or '1')
port map (
   Q => Q,      -- Data output
   C => C,      -- Clock input
   CE => CE,    -- Clock enable input
   R => R,      -- Synchronous reset input
   D => D       -- Data input
);

-- End of FDRE_inst instantiation
```

Verilog Instantiation Template

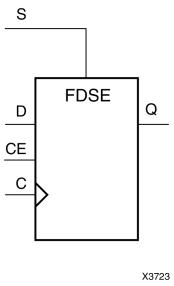
```
// FDRE: Single Data Rate D Flip-Flop with Synchronous Reset and
//       Clock Enable (posedge clk).
//       7 Series
// Xilinx HDL Libraries Guide, version 2012.2

FDRE #(
   .INIT(1'b0) // Initial value of register (1'b0 or 1'b1)
) FDRE_inst (
   .Q(Q),      // 1-bit Data output
   .C(C),      // 1-bit Clock input
   .CE(CE),    // 1-bit Clock enable input
   .R(R),      // 1-bit Synchronous reset input
   .D(D)       // 1-bit Data input
);

// End of FDRE_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

FDSE

Primitive: D Flip-Flop with Clock Enable and Synchronous Set



Introduction

FDSE is a single D-type flip-flop with data (D), clock enable (CE), and synchronous set (S) inputs and data output (Q). The synchronous set (S) input, when High, overrides the clock enable (CE) input and sets the Q output High during the Low-to-High clock (C) transition. The data on the D input is loaded into the flip-flop when S is Low and CE is High during the Low-to-High clock (C) transition.

For FPGA devices, this flip-flop is asynchronously preset, output High, when power is applied. Power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_E2 symbol.

Logic Table

Inputs				Outputs
S	**CE**	**D**	**C**	**Q**
1	X	X	↑	1
0	0	X	X	No Change
0	1	D	↑	D

Design Entry Method

Instantiation	Yes
Inference	Recommended
CORE Generator™ and wizards	No
Macro support	No

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- FDSE: Single Data Rate D Flip-Flop with Synchronous Set and
--       Clock Enable (posedge clk).
--       7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

FDSE_inst : FDSE
generic map (
   INIT => '0') -- Initial value of register ('0' or '1')
port map (
   Q => Q,      -- Data output
   C => C,      -- Clock input
   CE => CE,    -- Clock enable input
   S => S,      -- Synchronous Set input
   D => D       -- Data input
);

-- End of FDSE_inst instantiation
```

Verilog Instantiation Template

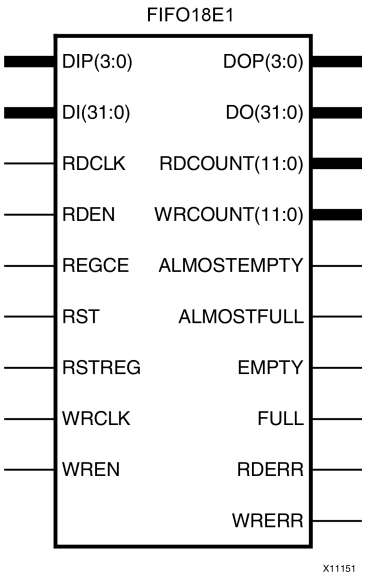
```
// FDSE: Single Data Rate D Flip-Flop with Synchronous Set and
//       Clock Enable (posedge clk).
//       7 Series
// Xilinx HDL Libraries Guide, version 2012.2

FDSE #(
   .INIT(1'b0) // Initial value of register (1'b0 or 1'b1)
) FDSE_inst (
   .Q(Q),      // 1-bit Data output
   .C(C),      // 1-bit Clock input
   .CE(CE),    // 1-bit Clock enable input
   .S(S),      // 1-bit Synchronous set input
   .D(D)       // 1-bit Data input
);

// End of FDSE_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

FIFO18E1

Primitive: 18Kb FIFO (First-In-First-Out) Block RAM Memory



Introduction

7 series devices contain several block RAM memories, each of which can be separately configured as a FIFO, an automatic error-correction RAM, or as a general-purpose 36KB or 18KB RAM/ROM memory. These Block RAM memories offer fast and flexible storage of large amounts of on-chip data. The FIFO18E1 uses the FIFO control logic and the 18KB Block RAM. This primitive can be used in a 4-bit wide by 4K deep, 9-bit wide by 2K deep, 18-bit wide by 1K deep, or a 36-bit wide by 512 deep configuration. The primitive can be configured in either synchronous or dual-clock (asynchronous) mode, with all associated FIFO flags and status signals.

When using the dual-clock mode with independent clocks, depending on the offset between read and write clock edges, the Empty, Almost Empty, Full and Almost Full flags can deassert one cycle later. Due to the asynchronous nature of the clocks the simulation model only reflects the deassertion latency cycles listed in the User Guide.

Note For a 36-bit wide by 512 deep FIFO, the "FIFO18_36" mode must be used. For deeper or wider configurations of the FIFO, the FIFO36E1 can be used. If error-correction circuitry is desired, the FIFO36E1 with "FIFO36_72" mode must be used.

Port Descriptions

Port	Type	Width	Function
ALMOSTEMPTY	Output	1	Programmable flag to indicate the FIFO is almost empty. The ALMOST_EMPTY_OFFSET attribute specifies the threshold where this flag is triggered relative to full/empty.
ALMOSTFULL	Output	1	Programmable flag to indicate that the FIFO is almost full. The ALMOST_FULL_OFFSET attribute specifies the threshold where this flag is triggered relative to full/empty.
DI<31:0>	Input	32	FIFO data input bus.
DIP<3:0>	Input	4	FIFO parity data input bus.
DO<31:0>	Output	32	FIFO data output bus.
DOP<3:0>	Output	4	FIFO parity data output bus.
EMPTY	Output	1	Active high logic to indicate that the FIFO is currently empty.
FULL	Output	1	Active high logic indicates that the FIFO is full.
RDCLK	Input	1	Rising edge read clock.
RDCOUNT<11: 0>	Output	12	Read count.
RDEN	Input	1	Active high FIFO read enable.
RDERR	Output	1	Read error occurred.
REGCE	Input	1	Output register clock enable for pipelined synchronous FIFO. DO_REG must be set to 1 if using this enable.
RST	Input	1	Active high (FIFO logic) asynchronous reset (for dual-clock FIFO), synchronous reset (for synchronous FIFO). Must be held for a minimum of 5 WRCLK/RDCLK cycles.
RSTREG	Input	1	Output register synchronous set/reset. DO_REG must be set to 1 if using this reset.
WRCLK	Input	1	Rising edge write clock.
WRCOUNT<11: 0>	Output	12	Write count.
WREN	Input	1	Active high FIFO write enable.
WRERR	Output	1	Write error occurred. When the FIFO is full, any additional write operation generates an error flag. Synchronous with WRCLK.

Design Entry Method

Instantiation	Yes
Inference	No
CORE Generator™ and wizards	Yes
Macro support	Recommended

Available Attributes

Attribute	Type	Allowed Values	Default	Description
ALMOST_EMPTY _OFFSET	HEX	13'h0000 to 13'h1fff	13'h0080	Specifies the amount of data contents in the RAM to trigger the ALMOST_EMPTY flag.
ALMOST_FULL _OFFSET	HEX	13'h0000 to 13'h1fff	13'h0080	Specifies the amount of data contents in the RAM to trigger the ALMOST_FULL flag.
DATA_WIDTH	DECIMAL	4, 9, 18, 36	4	Specifies the desired data width for the FIFO. **Note** If set to 36, FIFO_MODE must be set to FIFO18_36.
DO_REG	DECIMAL	1, 0	1	Data pipeline register for EN_SYN.
EN_SYN	BOOLEAN	FALSE, TRUE	FALSE	EN_SYN denotes whether the FIFO is operating in either dual-clock (two independent clocks) or synchronous (a single clock) mode. Dual-clock must use DO_REG=1.
FIFO_MODE	STRING	"FIFO18", "FIFO18_36"	"FIFO18"	Selects "FIFO18" or "FIFO18_36" mode. If set to "FIFO18_36", DATA_WIDTH must be set to 36.
FIRST_WORD _FALL_THROUGH	BOOLEAN	FALSE, TRUE	FALSE	If TRUE, the first write to the FIFO will appear on DO without a first RDEN assertion.
INIT	HEX	36 bit HEX	36'h000000000	Specifies the initial value on the DO output after configuration.
SIM_DEVICE	STRING	7SERIES	"7SERIES"	Must be set to "7SERIES" in order to exhibit proper simulation behavior under all conditions.
SRVAL	HEX	36 bit HEX	36'h000000000	Specifies the output value of the FIFO upon assertion of the synchronous reset (RSTREG) signal. Only valid for DO_REG=1.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- FIFO18E1: 18Kb FIFO (First-In-First-Out) Block RAM Memory
--           7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

FIFO18E1_inst : FIFO18E1
generic map (
   ALMOST_EMPTY_OFFSET => X"0080",    -- Sets the almost empty threshold
   ALMOST_FULL_OFFSET => X"0080",     -- Sets almost full threshold
   DATA_WIDTH => 4,                   -- Sets data width to 4-36
   DO_REG => 1,                       -- Enable output register (1-0) Must be 1 if EN_SYN = FALSE
```

```
   EN_SYN => FALSE,                  -- Specifies FIFO as dual-clock (FALSE) or Synchronous (TRUE)
   FIFO_MODE => "FIFO18",            -- Sets mode to FIFO18 or FIFO18_36
   FIRST_WORD_FALL_THROUGH => FALSE, -- Sets the FIFO FWFT to FALSE, TRUE
   INIT => X"000000000",             -- Initial values on output port
   SIM_DEVICE => "7SERIES",          -- Must be set to "7SERIES" for simulation behavior
   SRVAL => X"000000000"             -- Set/Reset value for output port
)
port map (
   -- Read Data: 32-bit (each) output: Read output data
   DO => DO,                     -- 32-bit output: Data output
   DOP => DOP,                   -- 4-bit output: Parity data output
   -- Status: 1-bit (each) output: Flags and other FIFO status outputs
   ALMOSTEMPTY => ALMOSTEMPTY, -- 1-bit output: Almost empty flag
   ALMOSTFULL => ALMOSTFULL,   -- 1-bit output: Almost full flag
   EMPTY => EMPTY,             -- 1-bit output: Empty flag
   FULL => FULL,               -- 1-bit output: Full flag
   RDCOUNT => RDCOUNT,         -- 12-bit output: Read count
   RDERR => RDERR,             -- 1-bit output: Read error
   WRCOUNT => WRCOUNT,         -- 12-bit output: Write count
   WRERR => WRERR,             -- 1-bit output: Write error
   -- Read Control Signals: 1-bit (each) input: Read clock, enable and reset input signals
   RDCLK => RDCLK,             -- 1-bit input: Read clock
   RDEN => RDEN,               -- 1-bit input: Read enable
   REGCE => REGCE,             -- 1-bit input: Clock enable
   RST => RST,                 -- 1-bit input: Asynchronous Reset
   RSTREG => RSTREG,           -- 1-bit input: Output register set/reset
   -- Write Control Signals: 1-bit (each) input: Write clock and enable input signals
   WRCLK => WRCLK,             -- 1-bit input: Write clock
   WREN => WREN,               -- 1-bit input: Write enable
   -- Write Data: 32-bit (each) input: Write input data
   DI => DI,                   -- 32-bit input: Data input
   DIP => DIP                  -- 4-bit input: Parity input
);

-- End of FIFO18E1_inst instantiation
```

Verilog Instantiation Template

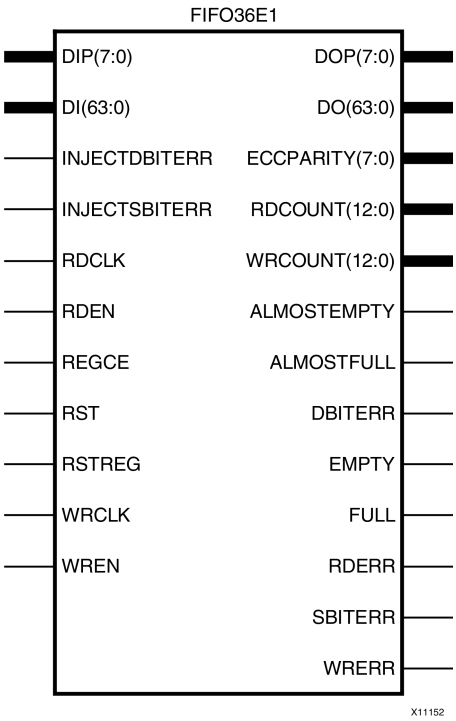
```
// FIFO18E1: 18Kb FIFO (First-In-First-Out) Block RAM Memory
//           7 Series
// Xilinx HDL Libraries Guide, version 2012.2

FIFO18E1 #(
   .ALMOST_EMPTY_OFFSET(13'h0080),    // Sets the almost empty threshold
   .ALMOST_FULL_OFFSET(13'h0080),     // Sets almost full threshold
   .DATA_WIDTH(4),                    // Sets data width to 4-36
   .DO_REG(1),                        // Enable output register (1-0) Must be 1 if EN_SYN = FALSE
   .EN_SYN("FALSE"),                  // Specifies FIFO as dual-clock (FALSE) or Synchronous (TRUE)
   .FIFO_MODE("FIFO18"),              // Sets mode to FIFO18 or FIFO18_36
   .FIRST_WORD_FALL_THROUGH("FALSE"), // Sets the FIFO FWFT to FALSE, TRUE
   .INIT(36'h000000000),              // Initial values on output port
   .SIM_DEVICE("7SERIES"),            // Must be set to "7SERIES" for simulation behavior
   .SRVAL(36'h000000000)              // Set/Reset value for output port
)
FIFO18E1_inst (
   // Read Data: 32-bit (each) output: Read output data
   .DO(DO),                   // 32-bit output: Data output
   .DOP(DOP),                 // 4-bit output: Parity data output
   // Status: 1-bit (each) output: Flags and other FIFO status outputs
   .ALMOSTEMPTY(ALMOSTEMPTY), // 1-bit output: Almost empty flag
   .ALMOSTFULL(ALMOSTFULL),   // 1-bit output: Almost full flag
   .EMPTY(EMPTY),             // 1-bit output: Empty flag
   .FULL(FULL),               // 1-bit output: Full flag
   .RDCOUNT(RDCOUNT),         // 12-bit output: Read count
   .RDERR(RDERR),             // 1-bit output: Read error
   .WRCOUNT(WRCOUNT),         // 12-bit output: Write count
   .WRERR(WRERR),             // 1-bit output: Write error
   // Read Control Signals: 1-bit (each) input: Read clock, enable and reset input signals
   .RDCLK(RDCLK),             // 1-bit input: Read clock
   .RDEN(RDEN),               // 1-bit input: Read enable
   .REGCE(REGCE),             // 1-bit input: Clock enable
   .RST(RST),                 // 1-bit input: Asynchronous Reset
   .RSTREG(RSTREG),           // 1-bit input: Output register set/reset
   // Write Control Signals: 1-bit (each) input: Write clock and enable input signals
   .WRCLK(WRCLK),             // 1-bit input: Write clock
   .WREN(WREN),               // 1-bit input: Write enable
   // Write Data: 32-bit (each) input: Write input data
   .DI(DI),                   // 32-bit input: Data input
   .DIP(DIP)                  // 4-bit input: Parity input
);

// End of FIFO18E1_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

FIFO36E1

Primitive: 36Kb FIFO (First-In-First-Out) Block RAM Memory



Introduction

7 series devices contain several block RAM memories that can be configured as FIFOs, automatic error-correction RAM, or general-purpose 36KB or 18KB RAM/ROM memories. These Block RAM memories offer fast and flexible storage of large amounts of on-chip data. The FIFO36E1 allows access to the Block RAM in the 36KB FIFO configurations. This component can be configured and used as a 4-bit wide by 8K deep, 9-bit by 4K deep, 18-bit by 2K deep, 36-bit wide by 1K deep, or 72-bit wide by 512 deep synchronous or dual-clock (asynchronous) FIFO RAM with all associated FIFO flags. When using the dual-clock mode with independent clocks, depending on the offset between read and write clock edges, the Empty, Almost Empty, Full and Almost Full flags can deassert one cycle later. Due to the asynchronous nature of the clocks the simulation model only reflects the deassertion latency cycles listed in the User Guide.
Note For a 72-bit wide by 512 deep FIFO, the "FIFO36_72" mode must be used. For smaller configurations of the FIFO, the FIFO18E1 can be used. If error-correction circuitry is desired, the "FIFO36_72" mode must be used.

Port Descriptions

Port	Type	Width	Function
ALMOSTEMPTY	Output	1	Programmable flag to indicate the FIFO is almost empty. The ALMOST_EMPTY_OFFSET attribute specifies where to trigger this flag.
ALMOSTFULL	Output	1	Programmable flag to indicate the FIFO is almost full. The ALMOST_FULL_OFFSET attribute specifies where to trigger this flag.
DBITERR	Output	1	Status output from ECC function to indicate a double bit error was detected. EN_ECC_READ needs to be TRUE in order to use this functionality.
DI<63:0>	Input	64	FIFO data input bus.
DIP<7:0>	Input	8	FIFO parity data input bus.
DO<63:0>	Output	64	FIFO data output bus.
DOP<7:0>	Output	8	FIFO parity data output bus.
ECCPARITY<7 :0>	Output	8	8-bit data generated by the ECC encoder used by the ECC decoder for memory error detection and correction.
EMPTY	Output	1	Active high logic to indicate that the FIFO is currently empty.
FULL	Output	1	Active high logic indicates that the FIFO is full.
INJECTDBITE RR	Input	1	Inject a double bit error if ECC feature is used.
INJECTSBITE RR	Input	1	Inject a single bit error if ECC feature is used.
RDCLK	Input	1	Rising edge read clock.
RDCOUNT<12: 0>	Output	13	Read count.
RDEN	Input	1	Active high FIFO read enable.
RDERR	Output	1	Read error occurred.
REGCE	Input	1	Output register clock enable for pipelined synchronous FIFO. DO_REG must be 1 to use this enable.
RST	Input	1	Active high (FIFO logic) asynchronous reset (for dual-clock FIFO), synchronous reset (synchronous FIFO) for 5 CLK cycles.
RSTREG	Input	1	Output register synchronous set/reset. DO_REG must be 1 to use this reset.
SBITERR	Output	1	Status output from ECC function to indicate a single bit error was detected. EN_ECC_READ needs to be TRUE in order to use this functionality.
WRCLK	Input	1	Write clock and enable input signals
WRCOUNT<12: 0>	Output	13	Write count.
WREN	Input	1	Active high FIFO write enable.
WRERR	Output	1	Write error occurred. When the FIFO is full, any additional write operation generates an error flag. Synchronous with WRCLK.

Design Entry Method

Instantiation	Yes
Inference	No
CORE Generator™ and wizards	Yes
Macro support	Recommended

Available Attributes

Attribute	Type	Allowed Values	Default	Description
ALMOST_EMPTY _OFFSET	HEX	13'h0000 to 13'h1fff	13'h0080	Specifies the amount of data contents in the RAM to trigger the ALMOST_EMPTY flag.
ALMOST_FULL _OFFSET	HEX	13'h0000 to 13'h1fff	13'h0080	Specifies the amount of data contents in the RAM to trigger the ALMOST_FULL flag.
DATA_WIDTH	DECIMAL	4, 9, 18, 36, 72	4	Specifies the desired data width for the FIFO. For data widths of 72, FIFO_MODE must be set to "FIFO36_72"
DO_REG	DECIMAL	1, 0	1	Enable output register to the FIFO for improved clock-to-out timing at the expense of added read latency (one pipeline delay). DO_REG must be 1 when EN_SYN is set to FALSE.
EN_ECC_READ	BOOLEAN	FALSE, TRUE	FALSE	Enable the ECC decoder circuitry.
EN_ECC_WRITE	BOOLEAN	FALSE, TRUE	FALSE	Enable the ECC encoder circuitry.
EN_SYN	BOOLEAN	FALSE, TRUE	FALSE	When FALSE, specifies the FIFO to be used in asynchronous mode (two independent clock) or when TRUE in synchronous (a single clock) operation.
FIFO_MODE	STRING	"FIFO36", "FIFO36_72"	"FIFO36"	Selects regular "FIFO36" or the wide "FIFO36_72" mode. If set to "FIFO36_72", the DATA_WIDTH attribute has to be 72.
FIRST_WORD _FALL_THROUGH	BOOLEAN	FALSE, TRUE	FALSE	If TRUE, the first write to the FIFO will appear on DO without an RDEN assertion.
INIT	HEX	72 bit HEX	72'h000000000000000000	Specifies the initial value on the DO output after configuration.
SIM_DEVICE	STRING	7SERIES	"7SERIES"	Must be set to "7SERIES" in order to exhibit proper simulation behavior under all conditions.
SRVAL	HEX	72 bit HEX	72'h000000000000000000	Specifies the output value of the FIFO upon assertion of the synchronous reset (RSTREG) signal. Only valid for DO_REG=1.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- FIFO36E1: 36Kb FIFO (First-In-First-Out) Block RAM Memory
--           7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

FIFO36E1_inst : FIFO36E1
generic map (
   ALMOST_EMPTY_OFFSET => X"0080",   -- Sets the almost empty threshold
   ALMOST_FULL_OFFSET => X"0080",    -- Sets almost full threshold
   DATA_WIDTH => 4,                  -- Sets data width to 4-72
   DO_REG => 1,                      -- Enable output register (1-0) Must be 1 if EN_SYN = FALSE
   EN_ECC_READ => FALSE,             -- Enable ECC decoder, FALSE, TRUE
   EN_ECC_WRITE => FALSE,            -- Enable ECC encoder, FALSE, TRUE
   EN_SYN => FALSE,                  -- Specifies FIFO as Asynchronous (FALSE) or Synchronous (TRUE)
   FIFO_MODE => "FIFO36",            -- Sets mode to "FIFO36" or "FIFO36_72"
   FIRST_WORD_FALL_THROUGH => FALSE, -- Sets the FIFO FWFT to &VALUES
   INIT => X"000000000000000000",    -- Initial values on output port
   SIM_DEVICE => "7SERIES",          -- Must be set to "7SERIES" for simulation behavior
   SRVAL => X"000000000000000000"    -- Set/Reset value for output port
)
port map (
   -- ECC Signals: 1-bit (each) output: Error Correction Circuitry ports
   DBITERR => DBITERR,             -- 1-bit output: Double bit error status
   ECCPARITY => ECCPARITY,         -- 8-bit output: Generated error correction parity
   SBITERR => SBITERR,             -- 1-bit output: Single bit error status
   -- Read Data: 64-bit (each) output: Read output data
   DO => DO,                       -- 64-bit output: Data output
   DOP => DOP,                     -- 8-bit output: Parity data output
   -- Status: 1-bit (each) output: Flags and other FIFO status outputs
   ALMOSTEMPTY => ALMOSTEMPTY,     -- 1-bit output: Almost empty flag
   ALMOSTFULL => ALMOSTFULL,       -- 1-bit output: Almost full flag
   EMPTY => EMPTY,                 -- 1-bit output: Empty flag
   FULL => FULL,                   -- 1-bit output: Full flag
   RDCOUNT => RDCOUNT,             -- 13-bit output: Read count
   RDERR => RDERR,                 -- 1-bit output: Read error
   WRCOUNT => WRCOUNT,             -- 13-bit output: Write count
   WRERR => WRERR,                 -- 1-bit output: Write error
   -- ECC Signals: 1-bit (each) input: Error Correction Circuitry ports
   INJECTDBITERR => INJECTDBITERR, -- 1-bit input: Inject a double bit error input
   INJECTSBITERR => INJECTSBITERR,
   -- Read Control Signals: 1-bit (each) input: Read clock, enable and reset input signals
   RDCLK => RDCLK,                 -- 1-bit input: Read clock
   RDEN => RDEN,                   -- 1-bit input: Read enable
   REGCE => REGCE,                 -- 1-bit input: Clock enable
   RST => RST,                     -- 1-bit input: Reset
   RSTREG => RSTREG,               -- 1-bit input: Output register set/reset
   -- Write Control Signals: 1-bit (each) input: Write clock and enable input signals
   WRCLK => WRCLK,                 -- 1-bit input: Rising edge write clock.
   WREN => WREN,                   -- 1-bit input: Write enable
   -- Write Data: 64-bit (each) input: Write input data
   DI => DI,                       -- 64-bit input: Data input
   DIP => DIP                      -- 8-bit input: Parity input
);

-- End of FIFO36E1_inst instantiation
```

Verilog Instantiation Template

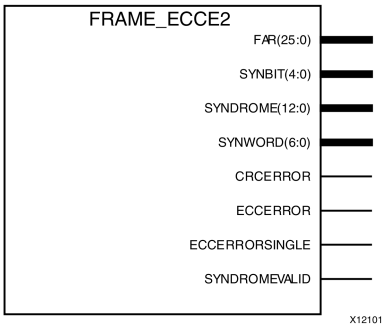
```
// FIFO36E1: 36Kb FIFO (First-In-First-Out) Block RAM Memory
//           7 Series
// Xilinx HDL Libraries Guide, version 2012.2

FIFO36E1 #(
   .ALMOST_EMPTY_OFFSET(13'h0080),    // Sets the almost empty threshold
   .ALMOST_FULL_OFFSET(13'h0080),     // Sets almost full threshold
   .DATA_WIDTH(4),                    // Sets data width to 4-72
   .DO_REG(1),                        // Enable output register (1-0) Must be 1 if EN_SYN = FALSE
   .EN_ECC_READ("FALSE"),             // Enable ECC decoder, FALSE, TRUE
   .EN_ECC_WRITE("FALSE"),            // Enable ECC encoder, FALSE, TRUE
   .EN_SYN("FALSE"),                  // Specifies FIFO as Asynchronous (FALSE) or Synchronous (TRUE)
   .FIFO_MODE("FIFO36"),              // Sets mode to "FIFO36" or "FIFO36_72"
   .FIRST_WORD_FALL_THROUGH("FALSE"), // Sets the FIFO FWFT to &VALUES
   .INIT(72'h000000000000000000),     // Initial values on output port
   .SIM_DEVICE("7SERIES"),            // Must be set to "7SERIES" for simulation behavior
   .SRVAL(72'h000000000000000000)     // Set/Reset value for output port
)
FIFO36E1_inst (
   // ECC Signals: 1-bit (each) output: Error Correction Circuitry ports
   .DBITERR(DBITERR),             // 1-bit output: Double bit error status
   .ECCPARITY(ECCPARITY),         // 8-bit output: Generated error correction parity
   .SBITERR(SBITERR),             // 1-bit output: Single bit error status
   // Read Data: 64-bit (each) output: Read output data
   .DO(DO),                       // 64-bit output: Data output
   .DOP(DOP),                     // 8-bit output: Parity data output
   // Status: 1-bit (each) output: Flags and other FIFO status outputs
   .ALMOSTEMPTY(ALMOSTEMPTY),     // 1-bit output: Almost empty flag
   .ALMOSTFULL(ALMOSTFULL),       // 1-bit output: Almost full flag
   .EMPTY(EMPTY),                 // 1-bit output: Empty flag
   .FULL(FULL),                   // 1-bit output: Full flag
   .RDCOUNT(RDCOUNT),             // 13-bit output: Read count
   .RDERR(RDERR),                 // 1-bit output: Read error
   .WRCOUNT(WRCOUNT),             // 13-bit output: Write count
   .WRERR(WRERR),                 // 1-bit output: Write error
   // ECC Signals: 1-bit (each) input: Error Correction Circuitry ports
   .INJECTDBITERR(INJECTDBITERR), // 1-bit input: Inject a double bit error input
   .INJECTSBITERR(INJECTSBITERR),
   // Read Control Signals: 1-bit (each) input: Read clock, enable and reset input signals
   .RDCLK(RDCLK),                 // 1-bit input: Read clock
   .RDEN(RDEN),                   // 1-bit input: Read enable
   .REGCE(REGCE),                 // 1-bit input: Clock enable
   .RST(RST),                     // 1-bit input: Reset
   .RSTREG(RSTREG),               // 1-bit input: Output register set/reset
   // Write Control Signals: 1-bit (each) input: Write clock and enable input signals
   .WRCLK(WRCLK),                 // 1-bit input: Rising edge write clock.
   .WREN(WREN),                   // 1-bit input: Write enable
   // Write Data: 64-bit (each) input: Write input data
   .DI(DI),                       // 64-bit input: Data input
   .DIP(DIP)                      // 8-bit input: Parity input
);

// End of FIFO36E1_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

FRAME_ECCE2

Primitive: Configuration Frame Error Correction



Introduction

This design element enables the dedicated, built-in Error Correction Code (ECC) for the configuration memory of the FPGA. This element contains outputs that allow monitoring of the status of the ECC circuitry and the status of the readback CRC circuitry.

Port Descriptions

Port	Type	Width	Function
CRCERROR	Output	1	Output indicating a CRC error.
ECCERROR	Output	1	Output indicating an ECC error.
ECCERRORSIN GLE	Output	1	Output Indicating single-bit Frame ECC error detected.
FAR<25:0>	Output	26	Frame Address Register Value output.
SYNBIT<4:0>	Output	5	Output bit address of error.
SYNDROME<12 :0>	Output	13	Output location of erroneous bit.
SYNDROMEVAL ID	Output	1	Frame ECC output indicating the SYNDROME output is valid.
SYNWORD<6:0>	Output	7	Word output in the frame where an ECC error has been detected.

Design Entry Method

Instantiation	Recommended
Inference	No
CORE Generator™ and wizards	No
Macro support	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
FARSRC	STRING	"EFAR", "FAR"	"EFAR"	Determines if the output of FAR[25:0] configuration register points to the FAR or EFAR. Sets configuration option register bit CTL0[7].
FRAME_RBT_IN_FILENAME	STRING	"0", "bit", "STRING"	"NONE"	This file is output by the ICAP_E2 model and it contains Frame Data information for the Raw Bitstream (RBT) file. The FRAME_ECCE2 model will parse this file, calculate ECC and output any error conditions.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- FRAME_ECCE2: Configuration Frame Error Correction
--              7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

FRAME_ECCE2_inst : FRAME_ECCE2
generic map (
   FARSRC => "EFAR",                -- Determines if the output of FAR[25:0] configuration register points
                                    -- to the FAR or EFAR. Sets configuration option register bit CTL0[7].
   FRAME_RBT_IN_FILENAME => "NONE"  -- This file is output by the ICAP_E2 model and it contains Frame Data
                                    -- information for the Raw Bitstream (RBT) file. The FRAME_ECCE2 model
                                    -- will parse this file, calculate ECC and output any error conditions.
)
port map (
   CRCERROR => CRCERROR,             -- 1-bit output: Output indicating a CRC error.
   ECCERROR => ECCERROR,             -- 1-bit output: Output indicating an ECC error.
   ECCERRORSINGLE => ECCERRORSINGLE, -- 1-bit output: Output Indicating single-bit Frame ECC error detected.
   FAR => FAR,                       -- 26-bit output: Frame Address Register Value output.
   SYNBIT => SYNBIT,                 -- 5-bit output: Output bit address of error.
   SYNDROME => SYNDROME,             -- 13-bit output: Output location of erroneous bit.
   SYNDROMEVALID => SYNDROMEVALID,   -- 1-bit output: Frame ECC output indicating the SYNDROME output is
                                     -- valid.

   SYNWORD => SYNWORD                -- 7-bit output: Word output in the frame where an ECC error has been
                                     -- detected.

);

-- End of FRAME_ECCE2_inst instantiation
```

Verilog Instantiation Template

```
// FRAME_ECCE2: Configuration Frame Error Correction
//              7 Series
// Xilinx HDL Libraries Guide, version 2012.2

FRAME_ECCE2 #(
   .FARSRC("EFAR"),                // Determines if the output of FAR[25:0] configuration register points to
                                   // the FAR or EFAR. Sets configuration option register bit CTL0[7].
   .FRAME_RBT_IN_FILENAME("NONE")  // This file is output by the ICAP_E2 model and it contains Frame Data
                                   // information for the Raw Bitstream (RBT) file. The FRAME_ECCE2 model
                                   // will parse this file, calculate ECC and output any error conditions.
)
FRAME_ECCE2_inst (
   .CRCERROR(CRCERROR),             // 1-bit output: Output indicating a CRC error.
   .ECCERROR(ECCERROR),             // 1-bit output: Output indicating an ECC error.
   .ECCERRORSINGLE(ECCERRORSINGLE), // 1-bit output: Output Indicating single-bit Frame ECC error detected.
   .FAR(FAR),                       // 26-bit output: Frame Address Register Value output.
   .SYNBIT(SYNBIT),                 // 5-bit output: Output bit address of error.
   .SYNDROME(SYNDROME),             // 13-bit output: Output location of erroneous bit.
   .SYNDROMEVALID(SYNDROMEVALID),   // 1-bit output: Frame ECC output indicating the SYNDROME output is
                                    // valid.

   .SYNWORD(SYNWORD)                // 7-bit output: Word output in the frame where an ECC error has been
                                    // detected.

);

// End of FRAME_ECCE2_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

GTPE2_CHANNEL

Primitive: Gigabit Transiever

Introduction

GTPE2 is a gigabit transceiver component for 7 series devices. It is not intended for direct instantiation. Use the Xilinx CORE Generator to properly configure and use this component. For additional details, see the 7 series FPGAs Transceivers User Guide.

Design Entry Method

Instantiation	No
Inference	No
CORE Generator™ and wizards	Yes
Macro support	No

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

GTPE2_COMMON

Primitive: Gigabit Transiever

Introduction

GTPE2 is a gigabit transceiver component for 7 series devices. It is not intended for direct instantiation. Use the Xilinx CORE Generator to properly configure and use this component. For additional details, see the 7 series FPGAs Transceivers User Guide.

Design Entry Method

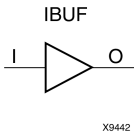
Instantiation	No
Inference	No
CORE Generator™ and wizards	Yes
Macro support	No

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

IBUF

Primitive: Input Buffer



Introduction

This design element is automatically inserted (inferred) by the synthesis tool to any signal directly connected to a top-level input or in-out port of the design. You should generally let the synthesis tool infer this buffer. However, it can be instantiated into the design if required. In order to do so, connect the input port (I) directly to the associated top-level input or in-out port, and connect the output port (O) to the logic sourced by that port. Modify any necessary generic maps (VHDL) or named parameter value assignment (Verilog) in order to change the default behavior of the component.

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Buffer output
I	Input	1	Buffer input

Design Entry Method

Instantiation	Yes
Inference	Recommended
CORE Generator™ and wizards	No
Macro support	No

In general, this element is inferred by the synthesis tool for any specified top-level input port to the design. It is generally not necessary to specify them in the source code. However, if desired, they be manually instantiated by either copying the instantiation code from the appropriate Libraries Guide HDL template and pasting it into the top-level entity/module of your code. It is recommended to always put all I/O components on the top-level of the design to help facilitate hierarchical design methods. Connect the I port directly to the top-level input port of the design and the O port to the logic in which this input is to source. Specify the desired generic/defparam values in order to configure the proper behavior of the buffer.

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
IBUF_LOW_PWR	Boolean	TRUE, FALSE	TRUE	When set to TRUE, allows for reduced power when using differential or referenced (requiring V_{REF}) input standards like LVDS or HSTL. A setting of FALSE demands more power but delivers higher performance characteristics. Consult the 7 Series FPGA SelectIO Resources User Guide for details.
IOSTANDARD	String	See Data Sheet.	"DEFAULT"	Assigns an I/O standard to the element.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- IBUF: Single-ended Input Buffer
--       7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

IBUF_inst : IBUF
generic map (
   IBUF_LOW_PWR => TRUE, -- Low power (TRUE) vs. performance (FALSE) setting for referenced I/O standards
   IOSTANDARD => "DEFAULT")
port map (
   O => O,     -- Buffer output
   I => I      -- Buffer input (connect directly to top-level port)
);

-- End of IBUF_inst instantiation
```

Verilog Instantiation Template

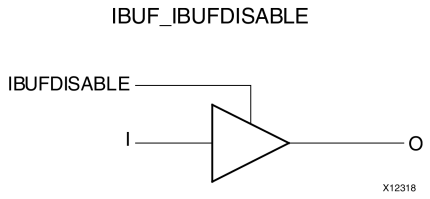
```
// IBUF: Single-ended Input Buffer
//       7 Series
// Xilinx HDL Libraries Guide, version 2012.2

IBUF #(
   .IBUF_LOW_PWR("TRUE"),  // Low power (TRUE) vs. performance (FALSE) setting for referenced I/O standards
   .IOSTANDARD("DEFAULT")  // Specify the input I/O standard
) IBUF_inst (
   .O(O),     // Buffer output
   .I(I)      // Buffer input (connect directly to top-level port)
);

// End of IBUF_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

IBUF_IBUFDISABLE

Primitive: Single-ended Input Buffer with Input Disable



Introduction

This design element is an input buffer used to connect internal logic to an external pin. This element includes an input path disable as an additional power saving feature when the I/O is not used for a sustained amount of time.

Port Descriptions

Port	Direction	Width	Function
I	Input	1	Input port connection. Connect directly to top-level port in the design.
IBUFDISABLE	Input	1	Disables input path through the buffer and forces to a logic high when USE_IBUFDISABLE is set to "TRUE" and this signal is asserted high. If USE_IBUFDISABLE is set to "FALSE" this input is ignored and should be tied to ground. This feature is generally used to reduce power at times when the I/O is idle for a period of time.
O	Output	1	Buffer output representing the input path to the device.

Design Entry Method

Instantiation	Yes
Inference	No
CORE Generator™ and wizards	Yes
Macro support	No

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
IBUF_LOW_PWR	String	"TRUE", "FALSE"	"TRUE"	Allows a trade off of lower power consumption versus highest performance when referenced I/O standards are used.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
USE_IBUFDISABLE	String	"TRUE", "FALSE"	"TRUE"	Enables or disables the feature of IBUFDISABLE.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- IBUF_IBUFDISABLE: Single-ended Input Buffer with Disable
--                   7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

IBUF_IBUFDISABLE_inst : IBUF_IBUFDISABLE
generic map (
   IBUF_LOW_PWR => "TRUE", -- Low power (TRUE) vs. performance (FALSE) setting for referenced I/O standards
   IOSTANDARD => "DEFAULT", -- Specify the input I/O standard
   USE_IBUFDISABLE => "TRUE") -- Set to "TRUE" to enable IBUFDISABLE feature
port map (
   O => O,      -- Buffer output
   I => I,      -- Buffer input (connect directly to top-level port)
   IBUFDISABLE => IBUFDISABLE -- Buffer disable input, low=disable
);

-- End of IBUF_IBUFDISABLE_inst instantiation
```

Verilog Instantiation Template

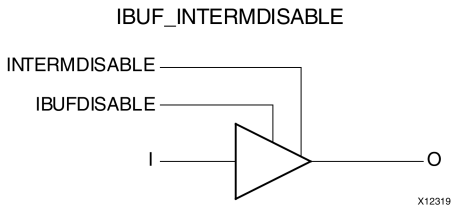
```
// IBUF_IBUFDISABLE: Single-ended Input Buffer with Disable
//                   7 Series
// Xilinx HDL Libraries Guide, version 2012.2

IBUF_IBUFDISABLE #(
   .IBUF_LOW_PWR("TRUE"),   // Low power ("TRUE") vs. perforrmance ("FALSE") forr referenced I/O standards
   .IOSTANDARD("DEFAULT"),  // Specify the input I/O standard
   .USE_IBUFDISABLE("TRUE") // Set to "TRUE" to enable IBUFDISABLE feature
) IBUF_IBUFDISABLE_inst (
   .O(O),                    // Buffer output
   .I(I),                    // Buffer input (connect directly to top-level port)
   .IBUFDISABLE(IBUFDISABLE) // Buffer disable input, low=disable
);

// End of IBUF_IBUFDISABLE_inst instantiation
```

For More Information

- See the *7 series FPGA SelectIO Resources User Guide (UG471)*.
- See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

IBUF_INTERMDISABLE

Primitive: Single-ended Input Buffer with Input Termination Disable and Input Disable



Introduction

This design element is an input buffer used to connect internal logic to an external pin. This element includes an input termination (INTERM) enable/disable as well as an input path disable as additional power saving features when the I/O is not being used for a sustained amount of time.

Port Descriptions

Port	Direction	Width	Function
I	Input	1	Input port connection. Connect directly to top-level port in the design.
IBUFDISABLE	Input	1	Disables input path through the buffer and forces to a logic high when USE_IBUFDISABLE is set to "TRUE" and this signal is asserted high. If USE_IBUFDISABLE is set to "FALSE" this input is ignored and should be tied to ground. This feature is generally used to reduce power at times when the I/O is idle for a period of time.
INTERMDISABLE	Input	1	Disables input termination. This feature is generally used to reduce power at times when the I/O is idle.
O	Output	1	Buffer output representing the input path to the device.

Design Entry Method

Instantiation	Yes
Inference	No
CORE Generator™ and wizards	Yes
Macro support	No

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
IBUF_LOW_PWR	String	"TRUE", "FALSE"	"TRUE"	Allows a trade off of lower power consumption vs. highest performance when referenced I/O standards are used.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
USE_IBUFDISABLE	String	"TRUE", "FALSE"	"TRUE"	Enables or disables the feature of IBUFDISABLE.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- IBUF_INTERMDISABLE: Single-ended Input Buffer with Termination Input Disable
--                     May only be placed in High Range (HR) Banks
--                     7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

IBUF_INTERMDISABLE_inst : IBUF_INTERMDISABLE
generic map (
   IBUF_LOW_PWR => "TRUE", -- Low power (TRUE) vs. performance (FALSE) setting for referenced I/O standards
   IOSTANDARD => "DEFAULT", -- Specify the input I/O standard
   USE_IBUFDISABLE => "TRUE") -- Set to "TRUE" to enable IBUFDISABLE feature
port map (
   O => O,      -- Buffer output
   I => I,      -- Buffer input (connect directly to top-level port)
   INTERMDISABLE => INTERMDISABLE, -- Input Termination Disable
   IBUFDISABLE => IBUFDISABLE -- Buffer disable input, low=disable
);

-- End of IBUF_INTERMDISABLE_inst instantiation
```

Verilog Instantiation Template

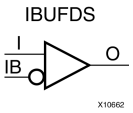
```
// IBUF_INTERMDISABLE: Single-ended Input Buffer with Termination Input Disable
//                     May only be placed in High Range (HR) Banks
//                     7 Series
// Xilinx HDL Libraries Guide, version 2012.2

IBUF_INTERMDISABLE #(
   .IBUF_LOW_PWR("TRUE"),   // Low power ("TRUE") vs. performance ("FALSE") forr referenced I/O standards
   .IOSTANDARD("DEFAULT"),  // Specify the input I/O standard
   .USE_IBUFDISABLE("TRUE") // Set to "TRUE" to enable IBUFDISABLE feature
) IBUF_INTERMDISABLE_inst (
   .O(O),                    // Buffer output
   .I(I),                    // Buffer input (connect directly to top-level port)
   .IBUFDISABLE(IBUFDISABLE),    // Buffer disable input, low=disable
   .INTERMDISABLE(INTERMDISABLE) // Input Termination Disable
);

// End of IBUF_INTERMDISABLE_inst instantiation
```

For More Information

- See the *7 series FPGA SelectIO Resources User Guide (UG471)*.
- See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

IBUFDS

Primitive: Differential Signaling Input Buffer



Introduction

This design element is an input buffer that supports low-voltage, differential signaling. In IBUFDS, a design level interface signal is represented as two distinct ports (I and IB), one deemed the "master" and the other the "slave." The master and the slave are opposite phases of the same logical signal (for example, MYNET_P and MYNET_N). Optionally, a programmable differential termination feature is available to help improve signal integrity and reduce external components.

Logic Table

Inputs		Outputs
I	**IB**	**O**
0	0	No Change
0	1	0
1	0	1
1	1	No Change

Port Descriptions

Port	Direction	Width	Function
I	Input	1	Diff_p Buffer Input
IB	Input	1	Diff_n Buffer Input
O	Output	1	Buffer Output

Design Entry Method

Instantiation	Recommended
Inference	No
CORE Generator™ and wizards	No
Macro support	No

Put all I/O components on the top-level of the design to help facilitate hierarchical design methods. Connect the I port directly to the top-level "master" input port of the design, the IB port to the top-level "slave" input port, and the O port to the logic in which this input is to source. Specify the desired generic/defparam values in order to configure the proper behavior of the buffer.

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
DIFF_TERM	Boolean	TRUE, FALSE	FALSE	The differential termination attribute is designed for the 7 Series FPGA supported differential input I/O standards. It is used to turn the built-in differential termination on (TRUE) or off (FALSE).
IBUF_LOW_PWR	Boolean	TRUE, FALSE	TRUE	When set to TRUE, allows for reduced power when using differential or referenced (requiring V_{REF}) input standards like LVDS or HSTL. A setting of FALSE demands more power but delivers higher performance characteristics. Consult the 7 Series FPGA SelectIO Resources User Guide for details.
IOSTANDARD	String	See Data Sheet.	"DEFAULT"	Assigns an I/O standard to the element.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- IBUFDS: Differential Input Buffer
--         7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

IBUFDS_inst : IBUFDS
generic map (
   DIFF_TERM => FALSE, -- Differential Termination
   IBUF_LOW_PWR => TRUE, -- Low power (TRUE) vs. performance (FALSE) setting for referenced I/O standards
   IOSTANDARD => "DEFAULT")
port map (
   O => O,  -- Buffer output
   I => I,  -- Diff_p buffer input (connect directly to top-level port)
   IB => IB -- Diff_n buffer input (connect directly to top-level port)
);

-- End of IBUFDS_inst instantiation
```

Verilog Instantiation Template

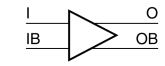
```
// IBUFDS: Differential Input Buffer
//         7 Series
// Xilinx HDL Libraries Guide, version 2012.2

IBUFDS #(
   .DIFF_TERM("FALSE"),       // Differential Termination
   .IBUF_LOW_PWR("TRUE"),     // Low power="TRUE", Highest perforrmance="FALSE"
   .IOSTANDARD("DEFAULT")     // Specify the input I/O standard
) IBUFDS_inst (
   .O(O),  // Buffer output
   .I(I),  // Diff_p buffer input (connect directly to top-level port)
   .IB(IB) // Diff_n buffer input (connect directly to top-level port)
);

// End of IBUFDS_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

IBUFDS_DIFF_OUT

Primitive: Differential Signaling Input Buffer With Differential Output



IBUFDS_DIFF_OUT

X10107

Introduction

This design element is an input buffer that supports differential signaling. In IBUFDS_DIFF_OUT, a design level interface signal is represented as two distinct ports (I and IB), one deemed the "master" and the other the "slave." The master and the slave are opposite phases of the same logical signal (for example, MYNET_P and MYNET_N). The IBUFDS_DIFF_OUT differs from the IBUFDS in that it allows internal access to both phases of the differential signal. Optionally, a programmable differential termination feature is available to help improve signal integrity and reduce external components.

Logic Table

Inputs		Outputs	
I	**IB**	**O**	**OB**
0	0	No Change	No Change
0	1	0	1
1	0	1	0
1	1	No Change	No Change

Port Descriptions

Port	Direction	Width	Function
I	Input	1	Diff_p Buffer Input (connect to top-level port in the design).
IB	Input	1	Diff_n Buffer Input (connect to top-level port in the design).
O	Output	1	Diff_p Buffer Output.
OB	Output	1	Diff_n Buffer Output.

Design Entry Method

Instantiation	Recommended
Inference	No
CORE Generator™ and wizards	No
Macro support	No

It is suggested to put all I/O components on the top-level of the design to help facilitate hierarchical design methods. Connect the I port directly to the top-level "master" input port of the design, the IB port to the top-level "slave" input port, and the O and OB ports to the logic in which this input is to source. Specify the desired generic/parameter values in order to configure the proper behavior of the buffer.

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
DIFF_TERM	Boolean	TRUE, FALSE	FALSE	The differential termination attribute is designed for the 7 Series FPGA supported differential input I/O standards. It is used to turn the built-in differential termination on (TRUE) or off (FALSE).
IBUF_LOW_PWR	Boolean	TRUE, FALSE	TRUE	When set to TRUE, allows for reduced power when using differential or referenced (requiring V_{REF}) input standards like LVDS or HSTL. A setting of FALSE demands more power but delivers higher performance characteristics. Consult the 7 Series FPGA SelectIO Resources User Guide for details.
IOSTANDARD	String	See Data Sheet.	"DEFAULT"	Assigns an I/O standard to the element.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- IBUFDS_DIFF_OUT: Differential Input Buffer with Differential Output
--                  7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

IBUFDS_DIFF_OUT_inst : IBUFDS_DIFF_OUT
generic map (
   DIFF_TERM => FALSE, -- Differential Termination
   IBUF_LOW_PWR => TRUE, -- Low power (TRUE) vs. performance (FALSE) setting for referenced I/O standards
   IOSTANDARD => "DEFAULT", -- Specify the input I/O standard
   USE_IBUFDISABLE => "TRUE"
port map (
   O => O,      -- Buffer diff_p output
   OB => OB,    -- Buffer diff_n output
   I => I,  -- Diff_p buffer input (connect directly to top-level port)
   IB => IB -- Diff_n buffer input (connect directly to top-level port)
);
```

```
-- End of IBUFDS_DIFF_OUT_inst instantiation
```

Verilog Instantiation Template

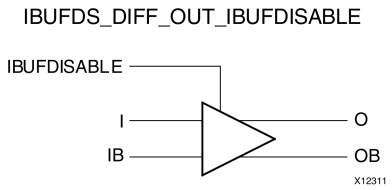
```
// IBUFDS_DIFF_OUT: Differential Input Buffer with Differential Output
//                  7 Series
// Xilinx HDL Libraries Guide, version 2012.2

IBUFDS_DIFF_OUT #(
   .DIFF_TERM("FALSE"),   // Differential Termination, "TRUE"/"FALSE"
   .IBUF_LOW_PWR("TRUE"), // Low power="TRUE", Highest performrmance="FALSE"
   .IOSTANDARD("DEFAULT") // Specify the input I/O standard
) IBUFDS_DIFF_OUT_inst (
   .O(O),   // Buffer diff_p output
   .OB(OB), // Buffer diff_n output
   .I(I),   // Diff_p buffer input (connect directly to top-level port)
   .IB(IB)  // Diff_n buffer input (connect directly to top-level port)
);

// End of IBUFDS_DIFF_OUT_inst instantiation
```

For More Information

- See the *7 series FPGA SelectIO Resources User Guide (UG471)*.
- See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

IBUFDS_DIFF_OUT_IBUFDISABLE

Primitive: Input Differential Buffer with Input Disable and Differential Output



Introduction

This design element is a differential input buffer used to connect internal logic to an external bidirectional pin. This element includes an input path disable as an additional power saving feature when the input is idle for a sustained time. The IOBUFDS_DIFF_OUT_IBUFDISABLE differs from the IOBUFDS_IBUFDISABLE in that it allows internal access to both phases of the differential signal.

Port Descriptions

Port	Direction	Width	Function
I	Input	1	Input p-side port connection. Connect directly to top-level port in the design.
IB	Input	1	Input n-side port connection. Connect directly to top-level port in the design.
IBUFDISABLE	Input	1	Disables input path through the buffer and forces to a logic high when USE_IBUFDISABLE is set to "TRUE" and this signal is asserted high. If USE_IBUFDISABLE is set to "FALSE" this input is ignored and should be tied to ground. This feature is generally used to reduce power at times when the I/O is idle for a period of time.
O	Output	1	Buffer p-side output representing the input path to the device.
OB	Output	1	Buffer n-side output representing the input path to the device.

Design Entry Method

Instantiation	Yes
Inference	No
CORE Generator™ and wizards	Yes
Macro support	No

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
DIFF_TERM	String	"TRUE", "FALSE"	"FALSE"	Enable the built-in differential termination.
IBUF_LOW_PWR	String	"TRUE", "FALSE"	"TRUE"	Allows a trade off of lower power consumption vs. highest performance when referenced I/O standards are used.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
USE_IBUFDISABLE	String	"TRUE", "FALSE"	"TRUE"	Enables or disables the feature of IBUFDISABLE.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- IBUFDS_DIFF_OUT_IBUFDISABLE: Differential Input Buffer with Differential Output w/ Disable
--                              7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

IBUFDS_DIFF_OUT_IBUFDISABLE_inst : IBUFDS_DIFF_OUT_IBUFDISABLE
generic map (
   DIFF_TERM => "FALSE", -- Differential Termination
   IBUF_LOW_PWR => "TRUE", -- Low power "TRUE" vs. performance "FALSE" setting for referenced I/O standards
   IOSTANDARD => "DEFAULT", -- Specify the input I/O standard
   USE_IBUFDISABLE => "TRUE") -- Set to "TRUE" to enable IBUFDISABLE feature
port map (
   O => O,     -- Buffer diff_p output
   OB => OB,   -- Buffer diff_n output
   I => I,  -- Diff_p buffer input (connect directly to top-level port)
   IB => IB, -- Diff_n buffer input (connect directly to top-level port)
   IBUFDISABLE => IBUFDISABLE -- Buffer disable input, low=disable
);

-- End of IBUFDS_DIFF_OUT_IBUFDISABLE_inst instantiation
```

Verilog Instantiation Template

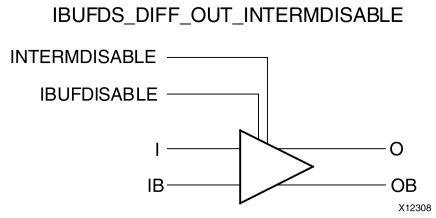
```
// IBUFDS_DIFF_OUT_IBUFDISABLE: Differential Input Buffer with Differential Output with Input Disable
//                              7 Series
// Xilinx HDL Libraries Guide, version 2012.2

IBUFDS_DIFF_OUT_IBUFDISABLE #(
   .DIFF_TERM("FALSE"),     // Differential Termination, "TRUE"/"FALSE"
   .IBUF_LOW_PWR("TRUE"),   // Low power="TRUE", Highest performrmance="FALSE"
   .IOSTANDARD("DEFAULT"),  // Specify the input I/O standard
   .USE_IBUFDISABLE("TRUE") // Set to "TRUE" to enable IBUFDISABLE feature
) IBUFDS_DIFF_OUT_IBUFDISABLE_inst (
   .O(O),   // Buffer diff_p output
   .OB(OB), // Buffer diff_n output
   .I(I),   // Diff_p buffer input (connect directly to top-level port)
   .IB(IB), // Diff_n buffer input (connect directly to top-level port)
   .IBUFDISABLE(IBUFDISABLE)  // Buffer disable input, low=disable
);

// End of IBUFDS_DIFF_OUT_IBUFDISABLE_inst instantiation
```

For More Information

- See the *7 series FPGA SelectIO Resources User Guide (UG471)*.
- See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

IBUFDS_DIFF_OUT_INTERMDISABLE

Primitive: Input Differential Buffer with Input Termination Disable, Input Disable, and Differential Output



Introduction

This design element is a differential input buffer used to connect internal logic to an external bidirectional pin. This element includes an uncalibrated input termination (INTERM) disable as well as input path disable as additional power saving features when the I/O is idle for a sustained time. The IOBUFDS_DIFF_OUT_INTERMDISABLE differs from the IOBUFDS_INTERMDISABLE in that it allows internal access to both phases of the differential signal. This element may only be placed in High Range (HR) banks in the 7 series devices.

Port Descriptions

Port	Direction	Width	Function
I	Input	1	Input p-side port connection. Connect directly to top-level port in the design.
IB	Input	1	Input n-side port connection. Connect directly to top-level port in the design.
IBUFDISABLE	Input	1	Disables input path through the buffer and forces to a logic high when USE_IBUFDISABLE is set to "TRUE" and this signal is asserted high. If USE_IBUFDISABLE is set to "FALSE" this input is ignored and should be tied to ground. This feature is generally used to reduce power at times when the I/O is idle.
INTERMDISABLE	Input	1	Disables input termination. This feature is generally used to reduce power at times when the I/O is idle.
O	Output	1	Buffer p-side output representing the input path to the device.
OB	Output	1	Buffer n-side output representing the input path to the device.

Design Entry Method

Instantiation	Yes
Inference	No
CORE Generator™ and wizards	Yes
Macro support	No

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
DIFF_TERM	String	"TRUE", "FALSE"	"FALSE"	Enable the built-in differential termination.
IBUF_LOW_PWR	String	"TRUE", "FALSE"	"TRUE"	Allows a trade off of lower power consumption vs. highest performance when referenced I/O standards are used.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
USE_IBUFDISABLE	String	"TRUE", "FALSE"	"TRUE"	Enables or disables the feature of IBUFDISABLE.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- IBUFDS_DIFF_OUT_INTERMDISABLE: Differential Input Buffer with Differential Output w/ Disable
--                                7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

IBUFDS_DIFF_OUT_INTERMDISABLE_inst : IBUFDS_DIFF_OUT_INTERMDISABLE
generic map (
   DIFF_TERM => "FALSE", -- Differential Termination
   IBUF_LOW_PWR => "TRUE", -- Low power "TRUE" vs. performance "FALSE" setting for referenced I/O standards
   IOSTANDARD => "DEFAULT", -- Specify the input I/O standard
   USE_IBUFDISABLE => "TRUE") -- Set to "TRUE" to enable IBUFDISABLE feature
port map (
   O => O,     -- Buffer diff_p output
   OB => OB,   -- Buffer diff_n output
   I => I,  -- Diff_p buffer input (connect directly to top-level port)
   IB => IB, -- Diff_n buffer input (connect directly to top-level port)
   IBUFDISABLE => IBUFDISABLE, -- Buffer disable input, low=disable
   INTERMDISABLE => INTERMDISABLE -- Input termination disable
);

-- End of IBUFDS_DIFF_OUT_INTERMDISABLE_inst instantiation
```

Verilog Instantiation Template

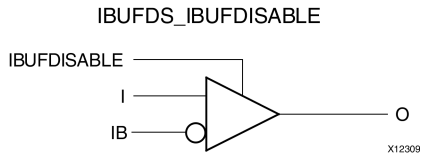
```
// IBUFDS_DIFF_OUT_INTERMDISABLE: Differential Input Buffer with Differential Output with Input Termination Disable
//                                May only be placed in High Range (HR) Banks
//                                7 Series
// Xilinx HDL Libraries Guide, version 2012.2

IBUFDS_DIFF_OUT_INTERMDISABLE  #(
   .DIFF_TERM("FALSE"),     // Differential Termination, "TRUE"/"FALSE"
   .IBUF_LOW_PWR("TRUE"),   // Low power="TRUE", Highest performrmance="FALSE"
   .IOSTANDARD("DEFAULT"),  // Specify the input I/O standard
   .USE_IBUFDISABLE("TRUE") // Set to "TRUE" to enable IBUFDISABLE feature
) IBUFDS_DIFF_OUT_INTERMDISABLE_inst (
   .O(O),   // Buffer diff_p output
   .OB(OB), // Buffer diff_n output
   .I(I),   // Diff_p buffer input (connect directly to top-level port)
   .IB(IB), // Diff_n buffer input (connect directly to top-level port)
   .IBUFDISABLE(IBUFDISABLE),    // Buffer disable input, low=disable
   .INTERMDISABLE(INTERMDISABLE) // Input Termination Disable
);

// End of IBUFDS_DIFF_OUT_INTERMDISABLE_inst instantiation
```

For More Information

- See the *7 series FPGA SelectIO Resources User Guide (UG471)*.
- See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

IBUFDS_IBUFDISABLE

Primitive: Input Differential Buffer with Input Path Disable



Introduction

This design element is an input differential buffer used to connect internal logic to an external bidirectional pin. This element includes an input path disable as an additional power saving feature when the I/O is either is an unused state for a sustained amount of time.

Port Descriptions

Port	Direction	Width	Function
I	Input	1	Input p-side port connection. Connect directly to top-level port in the design.
IB	Input	1	Input n-side port connection. Connect directly to top-level port in the design.
IBUFDISABLE	Input	1	Disables input path through the buffer and forces to a logic high when USE_IBUFDISABLE is set to "TRUE" and this signal is asserted high. If USE_IBUFDISABLE is set to "FALSE" this input is ignored and should be tied to ground. This feature is generally used to reduce power at times when the I/O is idle.
O	Output	1	Buffer output representing the input path to the device.

Design Entry Method

Instantiation	Yes
Inference	No
CORE Generator™ and wizards	Yes
Macro support	No

Put all I/O components on the top-level of the design to help facilitate hierarchical design methods. Connect the I port directly to the top-level "master" input port of the design, the IB port to the top-level "slave" input port, and the O port to the logic in which this input is to source. Specify the desired generic/defparam values in order to configure the proper behavior of the buffer.

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
DIFF_TERM	String	"TRUE", "FALSE"	"FALSE"	Enable the built-in differential termination.
IBUF_LOW_PWR	String	"TRUE", "FALSE"	"TRUE"	Allows a trade off of lower power consumption vs. highest performance when referenced I/O standards are used.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
USE_IBUFDISABLE	String	"TRUE", "FALSE"	"TRUE"	Enables or disables the feature of IBUFDISABLE.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- IBUFDS_IBUFDISABLE: Differential Input Buffer w/ Disable
--                     7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

IBUFDS_IBUFDISABLE_inst : IBUFDS_IBUFDISABLE
generic map (
   DIFF_TERM => "FALSE", -- Differential Termination
   IBUF_LOW_PWR => "TRUE", -- Low power (TRUE) vs. performance (FALSE) setting for referenced I/O standards
   IOSTANDARD => "DEFAULT" -- Specify the input I/O standard
   USE_IBUFDISABLE => "TRUE") -- Set to "TRUE" to enable IBUFDISABLE feature
port map (
   O => O,  -- Buffer output
   I => I,  -- Diff_p buffer input (connect directly to top-level port)
   IB => IB, -- Diff_n buffer input (connect directly to top-level port)
   IBUFDISABLE => IBUFDISABLE -- Buffer disable input, low=disable
);

-- End of IBUFDS_IBUFDISABLE_inst instantiation
```

Verilog Instantiation Template

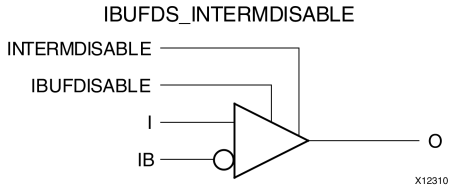
```
// IBUFDS_IBUFDISABLE: Differential Input Buffer with Input Disable
//                     7 Series
// Xilinx HDL Libraries Guide, version 2012.2

IBUFDS_IBUFDISABLE #(
   .DIFF_TERM("FALSE"),      // Differential Termination
   .IBUF_LOW_PWR("TRUE"),    // Low power="TRUE", Highest performrmance="FALSE"
   .IOSTANDARD("DEFAULT"),   // Specify the input I/O standard
   .USE_IBUFDISABLE("TRUE")  // Set to "TRUE" to enable IBUFDISABLE feature
) IBUFDS_IBUFDISABLE_inst (
   .O(O),   // Buffer output
   .I(I),   // Diff_p buffer input (connect directly to top-level port)
   .IB(IB), // Diff_n buffer input (connect directly to top-level port)
   .IBUFDISABLE(IBUFDISABLE) // Buffer disable input, low=disable
);

// End of IBUFDS_IBUFDISABLE_inst instantiation
```

For More Information

- See the *7 series FPGA SelectIO Resources User Guide (UG471)*.
- See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

IBUFDS_INTERMDISABLE

Primitive: Input Differential Buffer with Input Termination Disable and Input Disable



Introduction

This design element is an input differential buffer used to connect internal logic to an external bidirectional pin. This element includes an uncalibrated input termination (INTERM) disable as well as input path disable as additional power saving features when the input is idle for a sustained amount of time. This element may only be placed in High Range (HR) banks in the 7 series devices.

Port Descriptions

Port	Direction	Width	Function
I	Input	1	Input p-side port connection. Connect directly to top-level port in the design.
IB	Input	1	Input n-side port connection. Connect directly to top-level port in the design.
IBUFDISABLE	Input	1	Disables input path through the buffer and forces to a logic high when USE_IBUFDISABLE is set to "TRUE" and this signal is asserted high. If USE_IBUFDISABLE is set to "FALSE" this input is ignored and should be tied to ground. This feature is generally used to reduce power at times when the I/O is idle.
INTERMDISABLE	Input	1	Disables input termination. This feature is generally used to reduce power at times when the I/O is idle.

Port	Direction	Width	Function
O	Output	1	Buffer output representing the input path to the device.

Design Entry Method

Instantiation	Yes
Inference	No
CORE Generator™ and wizards	Yes
Macro support	No

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
DIFF_TERM	String	"TRUE", "FALSE"	"FALSE"	Enable the built-in differential termination.
IBUF_LOW_PWR	String	"TRUE", "FALSE"	"TRUE"	Allows a trade off of lower power consumption versus. highest performance when referenced I/O standards are used.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
USE_IBUFDISABLE	String	"TRUE", "FALSE"	"TRUE"	Enables or disables the IBUFDISABLE feature. Generally used when it is not desirable to disable the input path in order to allow a read during write operation.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- IBUFDS_INTERMDISABLE: Differential Input Buffer with Input Termination Disable
--                       May only be placed in High Range (HR) Banks
--                       7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

IBUFDS_INTERMDISABLE_inst : IBUFDS_INTERMDISABLE
generic map (
   DIFF_TERM => "FALSE", -- Differential Termination
   IBUF_LOW_PWR => "TRUE", -- Low power (TRUE) vs. performance (FALSE) setting for referenced I/O standards
   IOSTANDARD => "DEFAULT" -- Specify the input I/O standard
   USE_IBUFDISABLE => "TRUE") -- Set to "TRUE" to enable IBUFDISABLE feature
port map (
   O => O,  -- Buffer output
   I => I,  -- Diff_p buffer input (connect directly to top-level port)
   IB => IB, -- Diff_n buffer input (connect directly to top-level port)
   IBUFDISABLE => IBUFDISABLE, -- Buffer disable input, low=disable
   INTERMDISALE => INTERMDISABLE -- Input termination disable
```

```
);

-- End of IBUFDS_IBUFDISABLE_inst instantiation
```

Verilog Instantiation Template

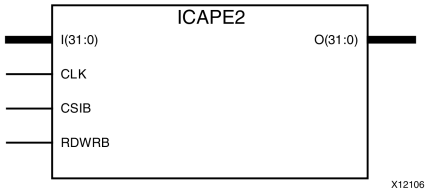
```
// IBUFDS_INTERMDISABLE: Differential Input Buffer with Input Termination Disable
//                       May only be placed in High Range (HR) Banks
//                       7 Series
// Xilinx HDL Libraries Guide, version 2012.2

IBUFDS_INTERMDISABLE #(
   .DIFF_TERM("FALSE"),      // Differential Termination
   .IBUF_LOW_PWR("TRUE"),    // Low power="TRUE", Highest performrmance="FALSE"
   .IOSTANDARD("DEFAULT"),   // Specify the input I/O standard
   .USE_IBUFDISABLE("TRUE")  // Set to "TRUE" to enable IBUFDISABLE feature
) IBUFDS_INTERMDISABLE_inst (
   .O(O),   // Buffer output
   .I(I),   // Diff_p buffer input (connect directly to top-level port)
   .IB(IB), // Diff_n buffer input (connect directly to top-level port)
   .IBUFDISABLE(IBUFDISABLE),    // Buffer disable input, low=disable
   .INTERMDISABLE(INTERMDISABLE) // Input Termination Disable
);

// End of IBUFDS_INTERMDISABLE_inst instantiation
```

For More Information

- See the *7 series FPGA SelectIO Resources User Guide (UG471)*.
- See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

ICAPE2

Primitive: Internal Configuration Access Port



Introduction

This design element gives you access to the configuration functions of the FPGA from the FPGA fabric. Using this component, commands and data can be written to and read from the configuration logic of the FPGA array. Since the improper use of this function can have a negative effect on the functionality and reliability of the FPGA, you should not use this element unless you are very familiar with its capabilities.

Port Descriptions

Port	Type	Width	Function
CLK	Input	1	Clock Input
CSIB	Input	1	Active-Low ICAP Enable
I<31:0>	Input	32	Configuration data input bus
O<31:0>	Output	32	Configuration data output bus
RDWRB	Input	1	Read/Write Select input

Design Entry Method

Instantiation	Recommended
Inference	No
CORE Generator™ and wizards	No
Macro support	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
DEVICE_ID	HEX	32'h03651093, 32'h036A2093, 32'h036A4093, 32'h036A6093, 32'h036BF093, 32'h036B1093, 32'h036B3093, 32'h036C2093, 32'h036C4093, 32'h036C6093, 32'h036DF093, 32'h036D1093, 32'h036D3093, 32'h036D5093, 32'h036D9093, 32'h0362C093, 32'h0362D093, 32'h0363B093, 32'h0364C093, 32'h0371F093, 32'h0372C093, 32'h0377F093, 32'h03627093, 32'h03628093, 32'h03631093, 32'h03636093, 32'h03642093, 32'h03647093, 32'h03656093, 32'h03667093, 32'h03671093, 32'h03676093, 32'h03680093, 32'h03681093, 32'h03682093, 32'h03687093, 32'h03691093, 32'h03692093, 32'h03696093, 32'h03702093, 32'h03704093, 32'h03711093, 32'h03722093, 32'h03727093, 32'h03731093, 32'h03747093, 32'h03751093, 32'h03752093, 32'h03762093, 32'h03771093, 32'h03782093	0'h3651093	Specifies the pre-programmed Device ID value to be used for simulation purposes.
ICAP_WIDTH	STRING	"X32", "X8", "X16"	"X32"	Specifies the input and output data width.
SIM_CFG_FILE_NAME	STRING	"0", "bit", "STRING"	"NONE"	Specifies the Raw Bitstream (RBT) file to be parsed by the simulation model.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- ICAPE2: Internal Configuration Access Port
--         7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

ICAPE2_inst : ICAPE2
generic map (
   DEVICE_ID => X"3651093",     -- Specifies the pre-programmed Device ID value to be used for simulation
                                -- purposes.
   ICAP_WIDTH => "X32",         -- Specifies the input and output data width.
   SIM_CFG_FILE_NAME => "NONE"  -- Specifies the Raw Bitstream (RBT) file to be parsed by the simulation
                                -- model.
)
port map (
   O => O,         -- 32-bit output: Configuration data output bus
   CLK => CLK,     -- 1-bit input: Clock Input
   CSIB => CSIB,   -- 1-bit input: Active-Low ICAP Enable
   I => I,         -- 32-bit input: Configuration data input bus
   RDWRB => RDWRB  -- 1-bit input: Read/Write Select input
);

-- End of ICAPE2_inst instantiation
```

Verilog Instantiation Template

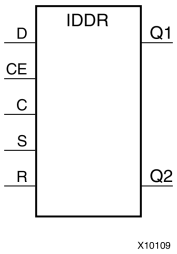
```
// ICAPE2: Internal Configuration Access Port
//         7 Series
// Xilinx HDL Libraries Guide, version 2012.2

ICAPE2 #(
   .DEVICE_ID(0'h3651093),     // Specifies the pre-programmed Device ID value to be used for simulation
                               // purposes.
   .ICAP_WIDTH("X32"),         // Specifies the input and output data width.
   .SIM_CFG_FILE_NAME("NONE")  // Specifies the Raw Bitstream (RBT) file to be parsed by the simulation
                               // model.
)
ICAPE2_inst (
   .O(O),         // 32-bit output: Configuration data output bus
   .CLK(CLK),     // 1-bit input: Clock Input
   .CSIB(CSIB),   // 1-bit input: Active-Low ICAP Enable
   .I(I),         // 32-bit input: Configuration data input bus
   .RDWRB(RDWRB)  // 1-bit input: Read/Write Select input
);

// End of ICAPE2_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

IDDR

Primitive: Input Dual Data-Rate Register



Introduction

This design element is a dedicated input register designed to receive external dual data rate (DDR) signals into Xilinx® FPGAs. The IDDR is available with modes that present the data to the FPGA fabric at the time and clock edge they are captured, or on the same clock edge. This feature allows you to avoid additional timing complexities and resource usage.

- **OPPOSITE_EDGE mode:** Data is recovered in the classic DDR methodology. Given a DDR data and clock at pin D and C respectively, Q1 changes after every positive edge of clock C, and Q2 changes after every negative edge of clock C.
- **SAME_EDGE mode:** Data is still recovered by opposite edges of clock C. However, an extra register has been placed in front of the negative edge data register. This extra register is clocked with positive clock edge of clock signal C. As a result, DDR data is now presented into the FPGA fabric at the same clock edge. However, because of this feature, the data pair appears to be "separated." Q1 and Q2 no longer have pair 1 and 2. Instead, the first pair presented is Pair 1 and DONT_CARE, followed by Pair 2 and 3 at the next clock cycle.
- **SAME_EDGE_PIPELINED mode:** Recovers data in a similar fashion as the SAME_EDGE mode. In order to avoid the "separated" effect of the SAME_EDGE mode, an extra register has been placed in front of the positive edge data register. A data pair now appears at the Q1 and Q2 pin at the same time. However, using this mode costs you an additional cycle of latency for Q1 and Q2 signals to change.

IDDR also works with the SelectIO™ features, such as the IODELAYE2.

Note For high speed interfaces, the IDDR_2CLK component can be used to specify two independent clocks to capture the data. Use this component when the performance requirements of the IDDR are not adequate, since the IDDR_2CLK requires more clocking resources and can imply placement restrictions that are not necessary when using the IDDR component.

Port Descriptions

Port	Direction	Width	Function
Q1 - Q2	Output	1	These pins are the IDDR output that connects to the FPGA fabric. Q1 is the first data pair and Q2 is the second data pair.
C	Input	1	Clock input pin.
CE	Input	1	When asserted Low, this port disables the output clock at port O.
D	Input	1	This pin is where the DDR data is presented into the IDDR module. This pin connects to a top-level input or bi-directional port, and IODELAY configured for an input delay or to an appropriate input or bidirectional buffer.
R	Input	1	Active high reset forcing Q1 and Q2 to a logic zero. Can be synchronous or asynchronous based on the SRTYPE attribute.
S	Input	1	Active high reset forcing Q1 and Q2 to a logic one. Can be synchronous or asynchronous based on the SRTYPE attribute.

Design Entry Method

Instantiation	Recommended
Inference	No
CORE Generator™ and wizards	Yes
Macro support	No

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
DDR_CLK_EDGE	String	"OPPOSITE_EDGE", "SAME_EDGE", "SAME_EDGE_ PIPELINED"	"OPPOSITE_ EDGE"	Sets the IDDR mode of operation with respect to clock edge.
INIT_Q1	Binary	0, 1	0	Initial value on the Q1 pin after configuration startup or when GSR is asserted.
INIT_Q2	Binary	0, 1	0	Initial value on the Q2 pin after configuration startup or when GSR is asserted.
SRTYPE	String	"SYNC" or "ASYNC"	"SYNC"	Set/reset type selection. "SYNC" specifies the behavior of the reset (R) and set (S) pins to be synchronous to the positive edge of the C clock pin. "ASYNC" specifies an asynchronous set/reset function.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- IDDR: Double Data Rate Input Register with Set, Reset
--       and Clock Enable.
--       7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

IDDR_inst : IDDR
generic map (
   DDR_CLK_EDGE => "OPPOSITE_EDGE", -- "OPPOSITE_EDGE", "SAME_EDGE"
                                    -- or "SAME_EDGE_PIPELINED"
   INIT_Q1 => '0', -- Initial value of Q1: '0' or '1'
   INIT_Q2 => '0', -- Initial value of Q2: '0' or '1'
   SRTYPE => "SYNC") -- Set/Reset type: "SYNC" or "ASYNC"
port map (
   Q1 => Q1, -- 1-bit output for positive edge of clock
   Q2 => Q2, -- 1-bit output for negative edge of clock
   C => C,   -- 1-bit clock input
   CE => CE, -- 1-bit clock enable input
   D => D,   -- 1-bit DDR data input
   R => R,   -- 1-bit reset
   S => S    -- 1-bit set
   );

-- End of IDDR_inst instantiation
```

Verilog Instantiation Template

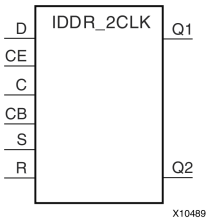
```
// IDDR: Input Double Data Rate Input Register with Set, Reset
//       and Clock Enable.
//       7 Series
// Xilinx HDL Libraries Guide, version 2012.2

IDDR #(
   .DDR_CLK_EDGE("OPPOSITE_EDGE"), // "OPPOSITE_EDGE", "SAME_EDGE"
                                   //    or "SAME_EDGE_PIPELINED"
   .INIT_Q1(1'b0), // Initial value of Q1: 1'b0 or 1'b1
   .INIT_Q2(1'b0), // Initial value of Q2: 1'b0 or 1'b1
   .SRTYPE("SYNC") // Set/Reset type: "SYNC" or "ASYNC"
) IDDR_inst (
   .Q1(Q1), // 1-bit output forr positive edge of clock
   .Q2(Q2), // 1-bit output forr negative edge of clock
   .C(C),   // 1-bit clock input
   .CE(CE), // 1-bit clock enable input
   .D(D),   // 1-bit DDR data input
   .R(R),   // 1-bit reset
   .S(S)    // 1-bit set
);

// End of IDDR_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

IDDR_2CLK

Primitive: Input Dual Data-Rate Register with Dual Clock Inputs



Introduction

This design element is a dedicated input register designed to receive external dual data rate (DDR) signals into Xilinx® FPGAs. You should only use the IDDR_2CLK for very high speed interfaces, since it requires more clocking resources, more power, and can imply certain placement restrictions that are not necessary when using the IDDR component. The IDDR component is also easier to use, uses fewer resources, and has fewer restrictions, though it cannot operate at the same high I/O speeds. The IDDR_2CLK is available with modes that present the data to the FPGA fabric at the time and clock edge they are captured, or on the same clock edge. This feature allows designers to avoid additional timing complexities and resource usage.

- **OPPOSITE_EDGE mode:** Data is presented in the classic DDR methodology. Given a DDR data and clock at pin D and C respectively, Q1 changes after every positive edge of clock C, and Q2 changes after every positive edge of clock CB.
- **SAME_EDGE mode:** Data is still presented by positive edges of each clock. However, an extra register has been placed in front of the CB clocked data register. This extra register is clocked with positive clock edge of clock signal C. As a result, DDR data is now presented into the FPGA fabric at the positive edge of clock C. However, because of this feature, the data pair appears to be "separated." Q1 and Q2 no longer have pair 1 and 2. Instead, the first pair presented is Pair 1 and DON'T CARE, followed by Pair 2 and 3 at the next clock cycle.
- **SAME_EDGE_PIPELINED mode:** Presents data in a similar fashion as the SAME_EDGE mode. In order to avoid the "separated" effect of the SAME_EDGE mode, an extra register has been placed in front of the C clocked data register. A data pair now appears at the Q1 and Q2 pin at the same time during the positive edge of C. However, using this mode requires an additional cycle of latency for Q1 and Q2 signals to change.

IDDR also works with SelectIO™ features, such as the IODELAYE2.

Port Descriptions

Port	Direction	Width	Function
Q1 : Q2	Output	1	These pins are the IDDR output that connects to the FPGA fabric. Q1 is the first data pair and Q2 is the second data pair.
C	Input	1	Primary clock input pin used to capture the positive edge data.
CB	Input	1	Secondary clock input pin (typically 180 degrees out of phase with the primary clock) used to capture the negative edge data.
CE	Input	1	When asserted Low, this port disables the output clock at port O.
D	Input	1	This pin is where the DDR data is presented into the IDDR module. This pin connects to a top-level input or bi-directional port, and IODELAY configured for an input delay or to an appropriate input or bidirectional buffer.
R	Input	1	Active high reset forcing Q1 and Q2 to a logic zero. Can be synchronous or asynchronous based on the SRTYPE attribute.
S	Input	1	Active high reset forcing Q1 and Q2 to a logic one. Can be synchronous or asynchronous based on the SRTYPE attribute.

Design Entry Method

Instantiation	Recommended
Inference	No
CORE Generator™ and wizards	No
Macro support	No

- Connect the C pin to the appropriate clock source, representing the positive clock edge and CB to the clock source representing the negative clock edge.
- Connect the D pin to the top-level input, or bidirectional port, an IODELAY, or an instantiated input or bidirectional buffer.
- The Q1 and Q2 pins should be connected to the appropriate data sources.
- CE should be tied high when not used, or connected to the appropriate clock enable logic.
- R and S pins should be tied low, if not used, or to the appropriate set or reset generation logic.
- Set all attributes to the component to represent the desired behavior.
- Always instantiate this component in pairs with the same clocking, and to LOC those to the appropriate P and N I/O pair in order not to sacrifice possible I/O resources.
- Always instantiate this component in the top-level hierarchy of your design, along with any other instantiated I/O components for the design. This helps facilitate hierarchical design flows/practices.

- To minimize CLK skew, both CLK and CLKB should come from global routing (MMCM) and not from the local inversion. MMCM de-skews these clocks whereas the local inversion adds skew.

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
DDR_CLK_EDGE	String	"OPPOSITE_EDGE", "SAME_EDGE" "SAME_EDGE_ PIPELINED"	"OPPOSITE_ EDGE"	DDR clock mode recovery mode selection. See Introduction for more explanation.
INIT_Q1	Binary	0, 1	0	Initial value on the Q1 pin after configuration startup or when GSR is asserted.
INIT_Q2	Binary	0, 1	0	Initial value on the Q2 pin after configuration startup or when GSR is asserted.
SRTYPE	String	"SYNC" or "ASYNC"	"SYNC"	Set/reset type selection. SYNC" specifies the behavior of the reset (R) and set (S) pins to be synchronous to the positive edge of the C clock pin. "ASYNC" specifies an asynchronous set/reset function.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- IDDR_2CLK: Dual-Clock, Input Double Data Rate Input Register with
--            Set, Reset and Clock Enable.
--            7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

IDDR_2CLK_inst : IDDR_2CLK
generic map (
   DDR_CLK_EDGE => "OPPOSITE_EDGE", -- "OPPOSITE_EDGE", "SAME_EDGE"
                                    -- or "SAME_EDGE_PIPELINED"
   INIT_Q1 => '0', -- Initial value of Q1: '0' or '1'
   INIT_Q2 => '0', -- Initial value of Q2: '0' or '1'
   SRTYPE => "SYNC") -- Set/Reset type: "SYNC" or "ASYNC"
port map (
   Q1 => Q1, -- 1-bit output for positive edge of clock
   Q2 => Q2, -- 1-bit output for negative edge of clock
   C => C,   -- 1-bit primary clock input
   CB => CB, -- 1-bit secondary clock input
   CE => CE, -- 1-bit clock enable input
   D => D,   -- 1-bit DDR data input
   R => R,   -- 1-bit reset
   S => S    -- 1-bit set
   );

-- End of IDDR_2CLK_inst instantiation
```

Verilog Instantiation Template

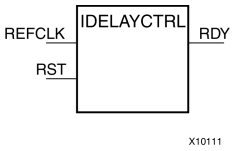
```
// IDDR_2CLK: Dual-Clock, Input Double Data Rate Input Register with
//            Set, Reset and Clock Enable.
//            7 Series
// Xilinx HDL Libraries Guide, version 2012.2

IDDR_2CLK #(
   .DDR_CLK_EDGE("OPPOSITE_EDGE"), // "OPPOSITE_EDGE", "SAME_EDGE"
                                   //    or "SAME_EDGE_PIPELINED"
   .INIT_Q1(1'b0), // Initial value of Q1: 1'b0 or 1'b1
   .INIT_Q2(1'b0), // Initial value of Q2: 1'b0 or 1'b1
   .SRTYPE("SYNC") // Set/Reset type: "SYNC" or "ASYNC"
) IDDR_2CLK_inst (
   .Q1(Q1), // 1-bit output forr positive edge of clock
   .Q2(Q2), // 1-bit output forr negative edge of clock
   .C(C),   // 1-bit primary clock input
   .CB(CB), // 1-bit secondary clock input
   .CE(CE), // 1-bit clock enable input
   .D(D),   // 1-bit DDR data input
   .R(R),   // 1-bit reset
   .S(S)    // 1-bit set
);

// End of IDDR_2CLK_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

IDELAYCTRL

Primitive: IDELAYE2/ODELAYE2 Tap Delay Value Control



Introduction

At least one of these design elements must be instantiated when using the IDELAYE2 or ODELAYE2. The IDELAYCTRL module provides a reference clock input that allows internal circuitry to derrive a voltage bias, independent of PVT (process, voltage, and temperature) variations, in order to define precise delay tap values for the associated IDELAYE2 and ODELAYE2 components. It is highly suggested to use the IODELAY_GROUP attribute in conjuction with the instantiation of this component in order to distiguish which IDELAYCTRL is associated with which IDELAYE2 and ODELAYE2s. See the Constraints Guide for more details on IODELAY_GROUP.

Port Descriptions

Port	Type	Width	Function
RDY	Output	1	The ready (RDY) signal indicates when the IDELAYE2 and ODELAYE2 modules in the specific region are calibrated. The RDY signal is deasserted if REFCLK is held High or Low for one clock period or more. If RDY is deasserted Low, the IDELAYCTRL module must be reset. If not needed, RDY to be unconnected/ignored.
REFCLK	Input	1	Time reference to IDELAYCTRL to calibrate all IDELAYE2 and ODELAYE2 modules in the same region. REFCLK can be supplied directly from a user-supplied source or the MMCME2/PLLE2 and must be routed on a global clock buffer.
RST	Input	1	Active-High asynchronous reset. To ensure proper IDELAYE2 and ODELAYE2 operation, IDELAYCTRL must be reset after configuration and the REFCLK signal is stable. A reset pulse width Tidelayctrl_rpw is required.

RST (Module reset): Resets the IDELAYCTRL circuitry. The RST signal is an active-high asynchronous reset. To reset the IDELAYCTRL, assert it High for at least 50 ns.

REFCLK (Reference Clock): Provides a voltage bias, independent of process, voltage, and temperature variations, to the tap-delay lines in the IOBs. The frequency of REFCLK must be 200 MHz to guarantee the tap-delay value specified in the applicable data sheet.

RDY (Ready Output): Indicates the validity of the reference clock input, REFCLK. When REFCLK disappears (i.e., REFCLK is held High or Low for one clock period or more), the RDY signal is deasserted.

Design Entry Method

Instantiation	Yes
Inference	No
CORE Generator™ and wizards	Yes
Macro support	No

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- IDELAYCTRL: IDELAYE2/ODELAYE2 Tap Delay Value Control
--             7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

IDELAYCTRL_inst : IDELAYCTRL
port map (
   RDY => RDY,       -- 1-bit output: Ready output
   REFCLK => REFCLK, -- 1-bit input: Reference clock input
   RST => RST        -- 1-bit input: Active high reset input
);

-- End of IDELAYCTRL_inst instantiation
```

Verilog Instantiation Template

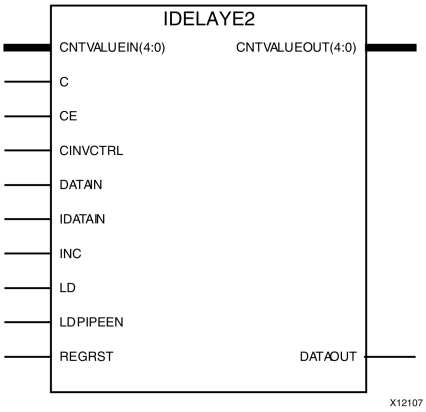
```
// IDELAYCTRL: IDELAYE2/ODELAYE2 Tap Delay Value Control
//             7 Series
// Xilinx HDL Libraries Guide, version 2012.2

(* IODELAY_GROUP = <iodelay_group_name> *) // Specifies group name for associated IDELAYs/ODELAYs and IDELAYCTRL

IDELAYCTRL IDELAYCTRL_inst (
   .RDY(RDY),       // 1-bit output: Ready output
   .REFCLK(REFCLK), // 1-bit input: Reference clock input
   .RST(RST)        // 1-bit input: Active high reset input
);

// End of IDELAYCTRL_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

IDELAYE2

Primitive: Input Fixed or Variable Delay Element



Introduction

Every I/O block contains a programmable absolute delay element called IDELAYE2. The IDELAYE2 can be connected to an input register/ISERDESE1 or driven directly into FPGA logic. The IDELAYE2 is a 31-tap, wraparound, delay element with a calibrated tap resolution. Refer to the 7 series FPGA Data Sheet for delay values. The IDELAYE2 allows incoming signals to be delayed on an individual basis. The tap delay resolution is varied by selecting an IDELAYCTRL reference clock from the range specified in the 7 series FPGA Data Sheet.

Port Descriptions

Port	Type	Width	Function
C	Input	1	All control inputs to IDELAYE2 primitive (RST, CE, and INC) are synchronous to the clock input (C). A clock must be connected to this port when IDELAYE2 is configured in "VARIABLE", "VAR_LOAD" or "VAR_LOAD_PIPE" mode. C can be locally inverted, and must be supplied by a global or regional clock buffer. This clock should be connected to the same clock in the SelectIO logic resources (when using ISERDESE2 and OSERDESE2, C is connected to CLKDIV).
CE	Input	1	Active high enable increment/decrement function
CINVCTRL	Input	1	The CINVCTRL pin is used for dynamically switching the polarity of C pin. This is for use in applications when glitches are not an issue. When switching the polarity, do not use the IDELAYE2 control pins for two clock cycles.
CNTVALUEIN<4:0>	Input	5	Counter value from FPGA logic for dynamically loadable tap value input.
CNTVALUEOUT<4:0>	Output	5	The CNTVALUEOUT pins are used for reporting the dynamically switching value of the delay element. CNTVALUEOUT is only available when IDELAYE2 is in "VAR_LOAD" or "VAR_LOAD_PIPE" mode.

Port	Type	Width	Function
DATAIN	Input	1	The DATAIN input is directly driven by the FPGA logic providing a logic accessible delay line. The data is driven back into the FPGA logic through the DATAOUT port with a delay set by the IDELAY_VALUE. DATAIN can be locally inverted. The data cannot be driven to an I/O.
DATAOUT	Output	1	Delayed data from either the IDATAIN or DATAIN input paths. DATAOUT connects to an ISERDESE2, input register or FPGA logic.
IDATAIN	Input	1	The IDATAIN input is driven by its associated I/O. The data can be driven to either an ISERDESE1 or input register block, directly into the FPGA logic, or to both through the DATAOUT port with a delay set by the IDELAY_VALUE.
INC	Input	1	Increment/decrement number of tap delays
LD	Input	1	Load IDELAY_VALUE to the counter.
LDPIPEEN	Input	1	Enable PIPELINE register to load data from LD pins.
REGRST	Input	1	When in "VARIABLE" mode, resets the delay element to a value set by the IDELAY_VALUE. If this attribute is not specified, a value of zero is assumed. The RST signal is an active-high reset and is synchronous to the input clock signal (C). When in "VAR_LOAD" or "VAR_LOAD_PIPE" mode, the IDELAYE2 reset signal resets the delay element to a value set by the CNTVALUEIN. The value present at CNTVALUEIN will be the new tap value. As a results of this functionality the IDELAY_VALUE is ignored.

Design Entry Method

Instantiation	Yes
Inference	No
CORE Generator™ and wizards	Yes
Macro support	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
CINVCTRL_SEL	STRING	"FALSE", "TRUE"	"FALSE"	Enables the CINVCTRL_SEL pin to dynamically switch the polarity of the C pin.
DELAY_SRC	STRING	"IDATAIN", "DATAIN"	"IDATAIN"	Select the delay source input to the IDELAYE2 • "IDATAIN": IDELAYE2 chain input is IDATAIN • "DATAIN" : IDELAYE2 chain input is DATAIN

Attribute	Type	Allowed Values	Default	Description
HIGH _PERFORMANCE_MODE	STRING	"FALSE", "TRUE"	"FALSE"	When TRUE, this attribute reduces the output jitter. When FALSE, power consumption is reduced. The difference in power consumption is quantified in the Xilinx Power Estimator tool.
IDELAY_TYPE	STRING	"FIXED", "VARIABLE", "VAR_LOAD", "VAR_LOAD_PIPE"	"FIXED"	Sets the type of tap delay line. • "FIXED" - Sets a static delay value. • "VARIABLE" - Dynamically adjust (incement/decrement) delay value. • "VAR_LOAD" - Dynamically loads tap values. • "VAR_LOAD_PIPE" - Pipelined dynamically loadable tap values.
IDELAY_VALUE	DECIMAL	0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31	0	Specifies the fixed number of delay taps in fixed mode or the initial starting number of taps in "VARIABLE" mode (input path). When IDELAY_TYPE is set to "VAR_LOAD" or "VAR_LOAD_PIPE" mode, this value is ignored.
PIPE_SEL	STRING	"FALSE", "TRUE"	"FALSE"	Select pipelined mode.
REFCLK _FREQUENCY	1 significant digit FLOAT	190.0 to 210.0 and 290.0 to 310.0	200.0	Sets the tap value (in MHz) used by the timing analyzer for static timing analysis and functional/timing simulation. The frequency of REFCLK must be within the given datasheet range to guarantee the tap-delay value and performance.
SIGNAL _PATTERN	STRING	"DATA", "CLOCK"	"DATA"	Causes the timing analyzer to account for the appropriate amount of delay-chain jitter in the data or clock path.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- IDELAYE2: Input Fixed or Variable Delay Element
--           7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

IDELAYE2_inst : IDELAYE2
```

```
generic map (
   CINVCTRL_SEL => "FALSE",          -- Enable dynamic clock inversion (FALSE, TRUE)
   DELAY_SRC => "IDATAIN",           -- Delay input (IDATAIN, DATAIN)
   HIGH_PERFORMANCE_MODE => "FALSE", -- Reduced jitter ("TRUE"), Reduced power ("FALSE")
   IDELAY_TYPE => "FIXED",           -- FIXED, VARIABLE, VAR_LOAD, VAR_LOAD_PIPE
   IDELAY_VALUE => 0,                -- Input delay tap setting (0-31)
   PIPE_SEL => "FALSE",              -- Select pipelined mode, FALSE, TRUE
   REFCLK_FREQUENCY => 200.0,        -- IDELAYCTRL clock input frequency in MHz (190.0-210.0).
   SIGNAL_PATTERN => "DATA"          -- DATA, CLOCK input signal
)
port map (
   CNTVALUEOUT => CNTVALUEOUT, -- 5-bit output: Counter value output
   DATAOUT => DATAOUT,         -- 1-bit output: Delayed data output
   C => C,                     -- 1-bit input: Clock input
   CE => CE,                   -- 1-bit input: Active high enable increment/decrement input
   CINVCTRL => CINVCTRL,       -- 1-bit input: Dynamic clock inversion input
   CNTVALUEIN => CNTVALUEIN,   -- 5-bit input: Counter value input
   DATAIN => DATAIN,           -- 1-bit input: Internal delay data input
   IDATAIN => IDATAIN,         -- 1-bit input: Data input from the I/O
   INC => INC,                 -- 1-bit input: Increment / Decrement tap delay input
   LD => LD,                   -- 1-bit input: Load IDELAY_VALUE input
   LDPIPEEN => LDPIPEEN,       -- 1-bit input: Enable PIPELINE register to load data input
   REGRST => REGRST            -- 1-bit input: Active-high reset tap-delay input
);

-- End of IDELAYE2_inst instantiation
```

Verilog Instantiation Template

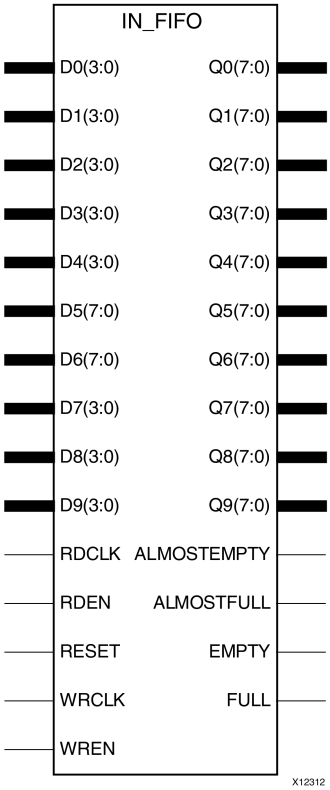
```
// IDELAYE2: Input Fixed or Variable Delay Element
//           7 Series
// Xilinx HDL Libraries Guide, version 2012.2

(* IODELAY_GROUP = <iodelay_group_name> *) // Specifies group name for associated IDELAYs/ODELAYs and IDELAYCTRL

IDELAYE2 #(
   .CINVCTRL_SEL("FALSE"),          // Enable dynamic clock inversion (FALSE, TRUE)
   .DELAY_SRC("IDATAIN"),           // Delay input (IDATAIN, DATAIN)
   .HIGH_PERFORMANCE_MODE("FALSE"), // Reduced jitter ("TRUE"), Reduced power ("FALSE")
   .IDELAY_TYPE("FIXED"),           // FIXED, VARIABLE, VAR_LOAD, VAR_LOAD_PIPE
   .IDELAY_VALUE(0),                // Input delay tap setting (0-31)
   .PIPE_SEL("FALSE"),              // Select pipelined mode, FALSE, TRUE
   .REFCLK_FREQUENCY(200.0),        // IDELAYCTRL clock input frequency in MHz (190.0-210.0).
   .SIGNAL_PATTERN("DATA")          // DATA, CLOCK input signal
)
IDELAYE2_inst (
   .CNTVALUEOUT(CNTVALUEOUT), // 5-bit output: Counter value output
   .DATAOUT(DATAOUT),         // 1-bit output: Delayed data output
   .C(C),                     // 1-bit input: Clock input
   .CE(CE),                   // 1-bit input: Active high enable increment/decrement input
   .CINVCTRL(CINVCTRL),       // 1-bit input: Dynamic clock inversion input
   .CNTVALUEIN(CNTVALUEIN),   // 5-bit input: Counter value input
   .DATAIN(DATAIN),           // 1-bit input: Internal delay data input
   .IDATAIN(IDATAIN),         // 1-bit input: Data input from the I/O
   .INC(INC),                 // 1-bit input: Increment / Decrement tap delay input
   .LD(LD),                   // 1-bit input: Load IDELAY_VALUE input
   .LDPIPEEN(LDPIPEEN),       // 1-bit input: Enable PIPELINE register to load data input
   .REGRST(REGRST)            // 1-bit input: Active-high reset tap-delay input
);

// End of IDELAYE2_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

IN_FIFO

Primitive: Input First-In, First-Out (FIFO)



Introduction

The Input FIFO is a new resource located next to the I/O. This dedicated hardware is designed to help transition the data from the input port, input register, IDDR or ISERDES to the fabric. It has two basic modes the first is a 4x4 mode where the data coming into the FIFO goes out at the same rate. The second mode is a 4x8 mode where the data coming out is de-serialized by a factor of 2. In other words in 4x8 mode 4 bits go to the IN_FIFO and 8 bits come out. Features of this component include:

- Array dimensions: 80 wide, 8 deep (4x8 mode); 40 wide, 8 deep (4x4 mode)
- Empty and Full flags
- Programmable Almost Empty and Almost Full flags

Port Descriptions

Port	Type	Width	Function
ALMOSTEMPTY	Output	1	Active high output flag indicating the FIFO is almost empty. The threshold of the almost empty flag is set by the ALMOST_EMPTY_VALUE attribute.
ALMOSTFULL	Output	1	Active high output flag indicating the FIFO is almost full. The threshold of the almost empty flag is set by the ALMOST_FULL_VALUE attribute.
D0<3:0>	Input	4	Channel 0 input bus.
D1<3:0>	Input	4	Channel 1 input bus.
D2<3:0>	Input	4	Channel 2 input bus.
D3<3:0>	Input	4	Channel 3 input bus.
D4<3:0>	Input	4	Channel 4 input bus.
D5<7:0>	Input	8	Channel 5 input bus.
D6<7:0>	Input	8	Channel 6 input bus.
D7<3:0>	Input	4	Channel 7 input bus.
D8<3:0>	Input	4	Channel 8 input bus.
D9<3:0>	Input	4	Channel 9 input bus.
EMPTY	Output	1	Active high output flag indicating the FIFO is empty.
FULL	Output	1	Active high output flag indicating the FIFO is full.
Q0<7:0>	Output	8	Channel 0 input bus.
Q1<7:0>	Output	8	Channel 1 output bus.
Q2<7:0>	Output	8	Channel 2 output bus.
Q3<7:0>	Output	8	Channel 3 output bus.
Q4<7:0>	Output	8	Channel 4 output bus.
Q5<7:0>	Output	8	Channel 5 output bus.
Q6<7:0>	Output	8	Channel 6 output bus.
Q7<7:0>	Output	8	Channel 7 output bus.
Q8<7:0>	Output	8	Channel 8 output bus.
Q9<7:0>	Output	8	Channel 9 output bus.
RDCLK	Input	1	Read clock.
RDEN	Input	1	Active high read enable.
RESET	Input	1	Active low, asynchrnous reset.
WRCLK	Input	1	Write clock.
WREN	Input	1	Active high write enable.

Design Entry Method

Instantiation	Yes
Inference	No
CORE Generator™ and wizards	No
Macro support	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
ALMOST_EMPTY_VALUE	DECIMAL	1, 2	1	Specifies the number of entries left before asserting the ALMOSTEMPTY output signal.
ALMOST_FULL_VALUE	DECIMAL	1, 2	1	Specifies the number of entries left before asserting the ALMOSTFULL output signal.
ARRAY_MODE	STRING	"ARRAY_MODE_4_X_8", "ARRAY_MODE_4_X_4"	"ARRAY_MODE_4_X_8"	Specifies deserializer mode: • "ARRAY_MODE_8_X_8" - Eight bits in, eight bits out • "ARRAY_MODE_4_X_8" - Four bits in, eight bits out
SYNCHRONOUS_MODE	STRING	"FALSE"	"FALSE"	Specify whether the RDCLK and WRCLK are synchrnous to each other.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- IN_FIFO: Input First-In, First-Out (FIFO)
--          7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

IN_FIFO_inst : IN_FIFO
generic map (
   ALMOST_EMPTY_VALUE => 1,          -- Almost empty offset (1-2)
   ALMOST_FULL_VALUE => 1,           -- Almost full offset (1-2)
   ARRAY_MODE => "ARRAY_MODE_4_X_8", -- ARRAY_MODE_4_X_8, ARRAY_MODE_4_X_4
   SYNCHRONOUS_MODE => "FALSE"       -- Clock synchronous (FALSE)
)
port map (
   -- FIFO Status Flags: 1-bit (each) output: Flags and other FIFO status outputs
   ALMOSTEMPTY => ALMOSTEMPTY, -- 1-bit output: Almost empty
   ALMOSTFULL => ALMOSTFULL,   -- 1-bit output: Almost full
   EMPTY => EMPTY,             -- 1-bit output: Empty
   FULL => FULL,               -- 1-bit output: Full
   -- Q0-Q9: 8-bit (each) output: FIFO Outputs
   Q0 => Q0,                   -- 8-bit output: Channel 0
   Q1 => Q1,                   -- 8-bit output: Channel 1
```

```
   Q2 => Q2,                    -- 8-bit output: Channel 2
   Q3 => Q3,                    -- 8-bit output: Channel 3
   Q4 => Q4,                    -- 8-bit output: Channel 4
   Q5 => Q5,                    -- 8-bit output: Channel 5
   Q6 => Q6,                    -- 8-bit output: Channel 6
   Q7 => Q7,                    -- 8-bit output: Channel 7
   Q8 => Q8,                    -- 8-bit output: Channel 8
   Q9 => Q9,                    -- 8-bit output: Channel 9
   -- D0-D9: 4-bit (each) input: FIFO inputs
   D0 => D0,                    -- 4-bit input: Channel 0
   D1 => D1,                    -- 4-bit input: Channel 1
   D2 => D2,                    -- 4-bit input: Channel 2
   D3 => D3,                    -- 4-bit input: Channel 3
   D4 => D4,                    -- 4-bit input: Channel 4
   D5 => D5,                    -- 8-bit input: Channel 5
   D6 => D6,                    -- 8-bit input: Channel 6
   D7 => D7,                    -- 4-bit input: Channel 7
   D8 => D8,                    -- 4-bit input: Channel 8
   D9 => D9,                    -- 4-bit input: Channel 9
   -- FIFO Control Signals: 1-bit (each) input: Clocks, Resets and Enables
   RDCLK => RDCLK,              -- 1-bit input: Read clock
   RDEN => RDEN,                -- 1-bit input: Read enable
   RESET => RESET,              -- 1-bit input: Reset
   WRCLK => WRCLK,              -- 1-bit input: Write clock
   WREN => WREN                 -- 1-bit input: Write enable
);

-- End of IN_FIFO_inst instantiation
```

Verilog Instantiation Template

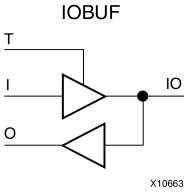
```
// IN_FIFO: Input First-In, First-Out (FIFO)
//          7 Series
// Xilinx HDL Libraries Guide, version 2012.2

IN_FIFO #(
   .ALMOST_EMPTY_VALUE(1),          // Almost empty offset (1-2)
   .ALMOST_FULL_VALUE(1),           // Almost full offset (1-2)
   .ARRAY_MODE("ARRAY_MODE_4_X_8"), // ARRAY_MODE_4_X_8, ARRAY_MODE_4_X_4
   .SYNCHRONOUS_MODE("FALSE")       // Clock synchronous (FALSE)
)
IN_FIFO_inst (
   // FIFO Status Flags: 1-bit (each) output: Flags and other FIFO status outputs
   .ALMOSTEMPTY(ALMOSTEMPTY), // 1-bit output: Almost empty
   .ALMOSTFULL(ALMOSTFULL),   // 1-bit output: Almost full
   .EMPTY(EMPTY),             // 1-bit output: Empty
   .FULL(FULL),               // 1-bit output: Full
   // Q0-Q9: 8-bit (each) output: FIFO Outputs
   .Q0(Q0),                   // 8-bit output: Channel 0
   .Q1(Q1),                   // 8-bit output: Channel 1
   .Q2(Q2),                   // 8-bit output: Channel 2
   .Q3(Q3),                   // 8-bit output: Channel 3
   .Q4(Q4),                   // 8-bit output: Channel 4
   .Q5(Q5),                   // 8-bit output: Channel 5
   .Q6(Q6),                   // 8-bit output: Channel 6
   .Q7(Q7),                   // 8-bit output: Channel 7
   .Q8(Q8),                   // 8-bit output: Channel 8
   .Q9(Q9),                   // 8-bit output: Channel 9
   // D0-D9: 4-bit (each) input: FIFO inputs
   .D0(D0),                   // 4-bit input: Channel 0
   .D1(D1),                   // 4-bit input: Channel 1
   .D2(D2),                   // 4-bit input: Channel 2
   .D3(D3),                   // 4-bit input: Channel 3
   .D4(D4),                   // 4-bit input: Channel 4
   .D5(D5),                   // 8-bit input: Channel 5
   .D6(D6),                   // 8-bit input: Channel 6
   .D7(D7),                   // 4-bit input: Channel 7
   .D8(D8),                   // 4-bit input: Channel 8
   .D9(D9),                   // 4-bit input: Channel 9
   // FIFO Control Signals: 1-bit (each) input: Clocks, Resets and Enables
   .RDCLK(RDCLK),             // 1-bit input: Read clock
   .RDEN(RDEN),               // 1-bit input: Read enable
   .RESET(RESET),             // 1-bit input: Reset
   .WRCLK(WRCLK),             // 1-bit input: Write clock
   .WREN(WREN)                // 1-bit input: Write enable
);

// End of IN_FIFO_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

IOBUF

Primitive: Bi-Directional Buffer



Introduction

The design element is a bidirectional single-ended I/O Buffer used to connect internal logic to an external bidirectional pin.

Logic Table

Inputs		Bidirectional	Outputs
T	**I**	**IO**	**O**
1	X	Z	IO
0	1	1	1
0	0	0	0

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Buffer output
IO	In/out	1	Buffer In/out
I	Input	1	Buffer input
T	Input	1	3-State enable input

Design Entry Method

Instantiation	Yes
Inference	Recommended
CORE Generator™ and wizards	No
Macro support	No

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
DRIVE	Integer	2, 4, 6, 8, 12, 16, 24	12	Selects output drive strength (mA) for the SelectIO™ buffers that use the LVTTL, LVCMOS12, LVCMOS15, LVCMOS18, LVCMOS25, or LVCMOS33 interface I/O standard.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
SLEW	String	"SLOW", "FAST"	"SLOW"	Sets the output rise and fall time.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- IOBUF: Single-ended Bi-directional Buffer
--        7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

IOBUF_inst : IOBUF
generic map (
   DRIVE => 12,
   IOSTANDARD => "DEFAULT",
   SLEW => "SLOW")
port map (
   O => O,     -- Buffer output
   IO => IO,   -- Buffer inout port (connect directly to top-level port)
   I => I,     -- Buffer input
   T => T      -- 3-state enable input, high=input, low=output
);

-- End of IOBUF_inst instantiation
```

Verilog Instantiation Template

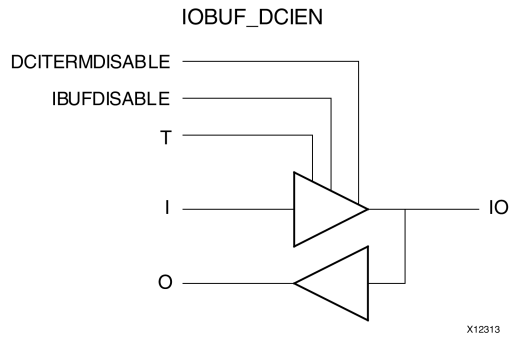
```
// IOBUF: Single-ended Bi-directional Buffer
//        All devices
// Xilinx HDL Libraries Guide, version 2012.2

IOBUF #(
   .DRIVE(12), // Specify the output drive strength
   .IBUF_LOW_PWR("TRUE"),  // Low Power - "TRUE", High Perforrmance = "FALSE"
   .IOSTANDARD("DEFAULT"), // Specify the I/O standard
   .SLEW("SLOW") // Specify the output slew rate
) IOBUF_inst (
   .O(O),     // Buffer output
   .IO(IO),   // Buffer inout port (connect directly to top-level port)
   .I(I),     // Buffer input
   .T(T)      // 3-state enable input, high=input, low=output
);

// End of IOBUF_inst instantiation
```

For More Information

- See the *7 series FPGA SelectIO Resources User Guide (UG471)*.
- See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

IOBUF_DCIEN

Primitive: Bi-Directional Single-ended Buffer with DCI and Input Disable.



Introduction

This design element is a bidirectional single ended I/O buffer used to connect internal logic to an external bidirectional pin. This element includes Digitally Controlled Impedance (DCI) termination enable/disable as well as input path disable as additional power saving features when the I/O is either in an unused state or being used as an output for a sustained amount of time. This element may only be placed in High Performance (HP) banks in the 7 series devices.

Port Descriptions

Port	Direction	Width	Function
IO	In/out	1	Bi-directional port connection. Connect directly to top-level port in the design.
I	Input	1	Buffer input representing the output path to the device.
IBUFDISABLE	Input	1	Disables input path. When this signal is asserted HIGH and the attribute USE_IBUFDISABLE is set to "TRUE", the input path through the input buffer is disabled and forced to a logic HIGH. If USE_IBUFDISABLE is set to "FALSE" this input is ignored and should be tied to ground. This feature is generally used to reduce power at times when the I/O is either idle or during sustained write (output) conditions.
DCITERMDISABLE	Input	1	Disables DCI termination. When this signal is asserted HIGH, DCI termination is disabled. This feature is generally used to reduce power at times when the I/O is either idle or during sustained write (output) conditions.
T	Input	1	Sets the I/O in a high impedance 3-state mode when the I/O is being used for a read (input) operation. The T pin also affects the IBUFDISABLE function when USE_IBUFDISABLE = "TRUE".
O	Output	1	Buffer output representing the input path to the device.

Design Entry Method

Instantiation	Yes
Inference	No
CORE Generator™ and wizards	Yes
Macro support	No

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
DRIVE	Integer	2, 4, 6, 8, 12, 16, 24	12	Selects output drive strength (mA) for the SelectIO™ buffers.
IBUF_LOW_PWR	String	"TRUE", "FALSE"	"TRUE"	Allows a trade off of lower power consumption vs. highest performance.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
SLEW	String	"SLOW", "FAST",	"SLOW"	Sets the output rise and fall time. See the Data Sheet for recommendations of the best setting for this attribute.
USE_IBUFDISABLE	String	"TRUE", "FALSE"	"TRUE"	Enables or disables the feature of IBUFDISABLE. Set to FALSE when it is not desirable to have the T pin disable input path to allow a read during write operation. When set to TRUE deasserting T (IO used as output) or asserting IBUFDISABLE will disable the input path through the buffer and forces to a logic high.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- IOBUF_DCIEN: Single-ended Bi-directional Buffer with Digital Controlled Impedance (DCI)
--              and Input path enable/disable
--              May only be placed in High Performance (HP) Banks
--              7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

IOBUF_DCIEN_inst : IOBUF_DCIEN
generic map (
   DRIVE => 12,
   IOSTANDARD => "DEFAULT",
   IBUF_LOW_PWR => "TRUE",
   SLEW => "SLOW")
port map (
   O => O,     -- Buffer output
```

```
   IO => IO,   -- Buffer inout port (connect directly to top-level port)
   DCITERMDISABLE => DCITERMDISABLE, -- DCI Termination enable input
   I => I,     -- Buffer input
   IBUFDISABLE => IBUFDISABLE, -- Input disable input, low=disable
   T => T      -- 3-state enable input, high=input, low=output
);

-- End of IOBUF_DCIEN_inst instantiation
```

Verilog Instantiation Template

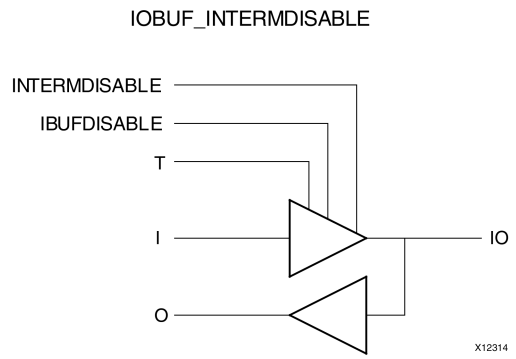
```
// IOBUF_DCIEN: Single-ended Bi-directional Buffer with Digital Controlled Impedance (DCI)
//              and Input path enable/disable
//              May only be placed in High Performrmance (HP) Banks
//              7 Series
// Xilinx HDL Libraries Guide, version 2012.2

IOBUF_DCIEN #(
   .DRIVE(12), // Specify the output drive strength
   .IBUF_LOW_PWR("TRUE"),  // Low Power - "TRUE", High Performrmance = "FALSE"
   .IOSTANDARD("DEFAULT"), // Specify the I/O standard
   .SLEW("SLOW"),          // Specify the output slew rate
   .USE_IBUFDISABLE("TRUE") // Use IBUFDISABLE function, "TRUE" or "FALSE"
) IOBUF_DCIEN_inst (
   .O(O),     // Buffer output
   .IO(IO),   // Buffer inout port (connect directly to top-level port)
   .DCITERMDISABLE(DCITERMDISABLE), // DCI Termination enable input
   .I(I),     // Buffer input
   .IBUFDISABLE(IBUFDISABLE), // Input disable input, low=disable
   .T(T)      // 3-state enable input, high=input, low=output
);

// End of IOBUF_DCIEN_inst instantiation
```

For More Information

- See the *7 series FPGA SelectIO Resources User Guide (UG471)*.
- See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

IOBUF_INTERMDISABLE

Primitive: Bi-Directional Single-ended Buffer with Input Termination Disable and Input Path Disable



Introduction

The design element is a bidirectional single-ended I/O Buffer used to connect internal logic to an external bidirectional pin. This element include uncalibrated input termination (INTERM) disable as well as input path disable as additional power saving features when the I/O is either is an unused state or being used as an output for several clock cycles. This element may only be placed in High Range (HR) banks in the 7 series devices.

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Buffer output representing the input path to the device.
IO	In/out	1	Bi-directional port connection. Connect directly to top-level port in the design.
I	Input	1	Buffer input representing the output path to the device.
IBUFDISABLE	Input	1	Disables input path through the buffer and forces to a logic high when USE_IBUFDISABLE is set to "TRUE". If USE_IBUFDISABLE is set to "FALSE" this input is ignored and should be tied to ground. This feature is generally used to reduce power at times when the I/O is either idle or during sustained write (output) conditions.
INTERMDISABLE	Input	1	Disables input termination. This feature is generally used to reduce power at times when the I/O is either idle or during sustained write (output) conditions.

Port	Direction	Width	Function
T	Input	1	Sets the I/O in a high impedance 3-state mode when the I/O is being used for a read (input) operation. The T pin also affects the IBUFDISABLE function when USE_IBUFDISABLE = "TRUE". The T pin also disables INTERM when in a write (output) mode.

Design Entry Method

Instantiation	Yes
Inference	No
CORE Generator™ and wizards	Yes
Macro support	No

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
DRIVE	Integer	2, 4, 6, 8, 12, 16, 24	12	Selects output drive strength (mA) for the SelectIO™ buffers.
IBUF_LOW_PWR	String	"TRUE", "FALSE"	"TRUE"	Allows a trade off of lower power consumption vs. highest performance.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
SLEW	String	"SLOW", "FAST"	"SLOW"	Sets the output rise and fall time. See the Data Sheet for recommendations of the best setting for this attribute.
USE_IBUFDISABLE	String	"TRUE", "FALSE"	"TRUE"	Enables or disables the feature of IBUFDISABLE. Generally used when it is not desirable to have the T pin disable input path to allow a read during write operation.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- IOBUF_INTERMDISABLE: Single-ended Bi-directional Buffer with Input Termination
--                      and Input path enable/disable
--                      May only be placed in High Range (HR) Banks
--                      7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

IOBUF_INTERMDISABLE_inst : IOBUF_INTERMDISABLE
```

```
generic map (
   DRIVE => 12,
   IOSTANDARD => "DEFAULT", -- Specify the I/O standard
   IBUF_LOW_PWR => "TRUE", -- Low Power - "TRUE", High Performance = "FALSE"
   USE_IBUFDISABLE => "TRUE", -- Use IBUFDISABLE function "TRUE" or "FALSE"
   SLEW => "SLOW")
port map (
   O => O,     -- Buffer output
   IO => IO,   -- Buffer inout port (connect directly to top-level port)
   DCITERMDISABLE => DCITERMDISABLE, -- DCI Termination enable input
   I => I,     -- Buffer input
   IBUFDISABLE => IBUFDISABLE, -- Input disable input, low=disable
   INTERMDISABLE => INTERMDISABLE, -- Input termination disable input
   T => T      -- 3-state enable input, high=input, low=output
);

-- End of IOBUF_INTERMDISABLE_inst instantiation
```

Verilog Instantiation Template

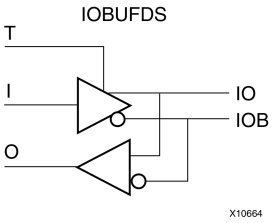
```
// IOBUF_INTERMDISABLE: Single-ended Bi-directional Buffer with Input Termination
//                      and Input path enable/disable
//                      May only be placed in High Range (HR) Banks
//                      7 Series
// Xilinx HDL Libraries Guide, version 2012.2

IOBUF_INTERMDISABLE #(
   .DRIVE(12), // Specify the output drive strength
   .IBUF_LOW_PWR("TRUE"),  // Low Power - "TRUE", High Performrmance = "FALSE"
   .IOSTANDARD("DEFAULT"), // Specify the I/O standard
   .SLEW("SLOW"),          // Specify the output slew rate
   .USE_IBUFDISABLE("TRUE") // Use IBUFDISABLE function, "TRUE" or "FALSE"
) IOBUF_INTERMDISABLE_inst (
   .O(O),     // Buffer output
   .IO(IO),   // Buffer inout port (connect directly to top-level port)
   .I(I),     // Buffer input
   .IBUFDISABLE(IBUFDISABLE), // Input disable input, low=disable
   .INTERMDISABLE(INTERMDISABLE), // Input termination disable input
   .T(T)      // 3-state enable input, high=input, low=output
);

// End of IOBUF_INTERMDISABLE_inst instantiation
```

For More Information

- See the *7 series FPGA SelectIO Resources User Guide (UG471)*.
- See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

IOBUFDS

Primitive: 3-State Differential Signaling I/O Buffer with Active Low Output Enable



Introduction

The design element is a bidirectional buffer that supports low-voltage, differential signaling. For the IOBUFDS, a design level interface signal is represented as two distinct ports (IO and IOB), one deemed the "master" and the other the "slave." The master and the slave are opposite phases of the same logical signal (for example, MYNET_P and MYNET_N). Optionally, a programmable differential termination feature is available to help improve signal integrity and reduce external components. Also available is a programmable delay is to assist in the capturing of incoming data to the device.

Logic Table

Inputs		Bidirectional		Outputs
I	**T**	**IO**	**IOB**	**O**
X	1	Z	Z	No Change
0	0	0	1	0
I	0	1	0	1

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Buffer output
IO	In/out	1	Diff_p In/out
IOB	In/out	1	Diff_n In/out
I	Input	1	Buffer input
T	Input	1	3-state enable input

Design Entry Method

Instantiation	Recommended
Inference	No
CORE Generator™ and wizards	No
Macro support	No

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
DIFF_TERM	Boolean	TRUE, FALSE	FALSE	The differential termination attribute is designed for the 7 Series FPGA supported differential input I/O standards. It is used to turn the built-in differential termination on (TRUE) or off (FALSE).
IBUF_LOW_PWR	Boolean	TRUE, FALSE	TRUE	When set to TRUE, allows for reduced power when using differential or referenced (requiring V_{REF}) input standards like LVDS or HSTL. A setting of FALSE demands more power but delivers higher performance characteristics. Consult the 7 Series FPGA SelectIO Resources User Guide for details.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
SLEW	String	"SLOW" or "FAST"	"SLOW"	Specifies the slew rate of the output driver. Consult the product Data Sheet for recommendations of the best setting for this attribute.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- IOBUFDS: Differential Bi-directional Buffer
--          7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

IOBUFDS_inst : IOBUFDS
generic map (
   DIFF_TERM => FALSE, -- Differential Termination (TRUE/FALSE)
   IBUF_LOW_PWR => TRUE, -- Low Power = TRUE, High Performance = FALSE
   IOSTANDARD => "BLVDS_25", -- Specify the I/O standard
   SLEW => "SLOW")       -- Specify the output slew rate
port map (
   O => O,     -- Buffer output
   IO => IO,   -- Diff_p inout (connect directly to top-level port)
```

```
   IOB => IOB, -- Diff_n inout (connect directly to top-level port)
   I => I,     -- Buffer input
   T => T      -- 3-state enable input, high=input, low=output
);

-- End of IOBUFDS_inst instantiation
```

Verilog Instantiation Template

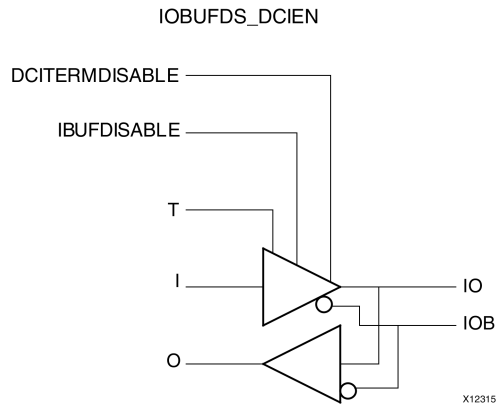
```
// IOBUFDS: Differential Bi-directional Buffer
//          7 Series
// Xilinx HDL Libraries Guide, version 2012.2

IOBUFDS #(
   .DIFF_TERM("FALSE"),     // Differential Termination ("TRUE"/"FALSE")
   .IBUF_LOW_PWR("TRUE"),   // Low Power - "TRUE", High Performmance = "FALSE"
   .IOSTANDARD("BLVDS_25"), // Specify the I/O standard
   .SLEW("SLOW")            // Specify the output slew rate
) IOBUFDS_inst (
   .O(O),     // Buffer output
   .IO(IO),   // Diff_p inout (connect directly to top-level port)
   .IOB(IOB), // Diff_n inout (connect directly to top-level port)
   .I(I),     // Buffer input
   .T(T)      // 3-state enable input, high=input, low=output
);

// End of IOBUFDS_inst instantiation
```

For More Information

- See the *7 series FPGA SelectIO Resources User Guide (UG471)*.
- See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

IOBUFDS_DCIEN

Primitive: Bi-Directional Differential Buffer with DCI Enable/Disable and Input Disable



Introduction

This design element is a bidirectional differential I/O buffer used to connect internal logic to an external bidirectional pin. This element includes Digitally Controlled Impedance (DCI) termination enable/disable as well as input path disable as additional power saving features when the I/O is either in an unused state or being used as an output for a sustained amount of time. This element may only be placed in High Performance (HP) banks in the 7 series devices.

Port Descriptions

Port	Direction	Width	Function
IO	In/out	1	Bi-directional p-side port connection. Connect directly to top-level port in the design.
IOB	In/out	1	Bi-directional p-side port connection. Connect directly to top-level port in the design.
I	Input	1	Buffer input representing the output path to the device.
IBUFDISABLE	Input	1	Disables input path. When this signal is asserted HIGH and the attribute USE_IBUFDISABLE is set to "TRUE", the input path through the input buffer is disabled and forced to a logic HIGH.. If USE_IBUFDISABLE is set to "FALSE" this input is ignored and should be tied to ground. This feature is generally used to reduce power at times when the I/O is either idle or during sustained write (output) conditions.
DCITERMDISABLE	Input	1	Disables DCI termination. When this signal is asserted HIGH, DCI termination is disabled. This feature is generally used to reduce power

Port	Direction	Width	Function
			at times when the I/O is either idle or during sustained write (output) conditions.
T	Input	1	Sets the I/O in a high impedance 3-state mode when the I/O is being used for a read (input) operation. The T pin also affects the IBUFDISABLE function when USE_IBUFDISABLE = "TRUE".
O	Output	1	Buffer output representing the input path to the device.

Design Entry Method

Instantiation	Yes
Inference	No
CORE Generator™ and wizards	Yes
Macro support	No

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
DIFF_TERM	String	"TRUE", "FALSE"	"FALSE"	Enable the built-in differential termination.
IBUF_LOW_PWR	String	"TRUE", "FALSE"	"TRUE"	Allows a trade off of lower power consumption vs. highest performance.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
SLEW	String	"SLOW", "FAST",	"SLOW"	Sets the output rise and fall time. See the Data Sheet for recommendations of the best setting for this attribute.
USE_IBUFDISABLE	String	"TRUE", "FALSE"	"TRUE"	Enables or disables the feature of IBUFDISABLE. Set to FALSE when it is not desirable to have the T pin disable input path to allow a read during write operation. When set to TRUE deasserting T (IO used as output) or asserting IBUFDISABLE will disable the input path through the buffer and forces to a logic high.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- IOBUFDS_DCIEN: Differential Bi-directional Buffer with Digital Controlled Impedance (DCI)
--                and Input path enable/disable
--                May only be placed in High Performance (HP) Banks
--                7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

IOBUFDS_DCIEN_inst : IOBUFDS_DCIEN
generic map (
   DIFF_TERM => "FALSE", -- Differential termination (TRUE/FALSE)
   IBUF_LOW_PWR => "TRUE", -- Low Power - TRUE, HIGH Performance = FALSE
   IOSTANDARD => "BLVDS_25", -- Specify the I/O standard
   SLEW => "SLOW",   -- Specify the output slew rate
   USE_IBUFDISABLE => "TRUE") -- Use IBUFDISABLE function "TRUE" or "FALSE"
port map (
   O => O,     -- Buffer output
   IO => IO,   -- Diff_p inout (connect directly to top-level port)
   IOB => IOB, -- Diff_n inout (connect directly to top-level port)
   DCITERMDISABLE => DCITERMDISABLE, -- DCI Termination enable input
   I => I,     -- Buffer input
   IBUFDISABLE => IBUFDISABLE, -- Input disable input, low=disable
   T => T      -- 3-state enable input, high=input, low=output
);

-- End of IOBUFDS_DCIEN_inst instantiation
```

Verilog Instantiation Template

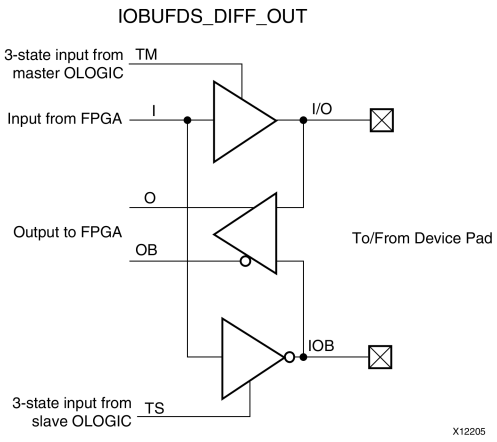
```
// IOBUFDS_DCIEN: Differential Bi-directional Buffer with Digital Controlled Impedance (DCI)
//                and Input path enable/disable
//                May only be placed in High Performrmance (HP) Banks
//                7 Series
// Xilinx HDL Libraries Guide, version 2012.2

IOBUFDS_DCIEN #(
   .DIFF_TERM("FALSE"),     // Differential Termination ("TRUE"/"FALSE")
   .IBUF_LOW_PWR("TRUE"),   // Low Power - "TRUE", High Performrmance = "FALSE"
   .IOSTANDARD("BLVDS_25"), // Specify the I/O standard
   .SLEW("SLOW"),           // Specify the output slew rate
   .USE_IBUFDISABLE("TRUE") // Use IBUFDISABLE function, "TRUE" or "FALSE"
) IOBUFDS_DCIEN_inst (
   .O(O),     // Buffer output
   .IO(IO),   // Diff_p inout (connect directly to top-level port)
   .IOB(IOB), // Diff_n inout (connect directly to top-level port)
   .DCITERMDISABLE(DCITERMDISABLE), // DCI Termination enable input
   .I(I),                           // Buffer input
   .IBUFDISABLE(IBUFDISABLE),       // Input disable input, low=disable
   .T(T)      // 3-state enable input, high=input, low=output
);

// End of IOBUFDS_DCIEN_inst instantiation
```

For More Information

- See the *7 series FPGA SelectIO Resources User Guide (UG471)*.
- See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

IOBUFDS_DIFF_OUT

Primitive: Differential Bi-directional Buffer with Differential Output



Introduction

This design element is a bidirectional buffer that supports low-voltage, differential signaling. For the IOBUFDS_DIFF_OUT, a design level interface signal is represented as two distinct ports (IO and IOB), one deemed the "master" and the other the "slave." The master and the slave are opposite phases of the same logical signal (for example, MYNET_P and MYNET_N). The IOBUFDS_DIFF_OUT differs from the IOBUFDS in that it allows internal access to both phases of the differential signal. Optionally, a programmable differential termination feature is available to help improve signal integrity and reduce external components.

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Buffer p-side output
OB	Output	1	Buffer n-side output
IO	In/out	1	Diff_p In/out (connect directly to top-level port)
IOB	In/out	1	Diff_n In/out (connect directly to top-level port)
I	Input	1	Buffer input
TM	Input	1	3-state enable input from master OLOGIC, high=input, low=output
TS	Input	1	3-state enable input from slave OLOGIC, high=input, low=output

Design Entry Method

Instantiation	Recommended
Inference	No
CORE Generator™ and wizards	No
Macro support	No

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
DIFF_TERM	Boolean	TRUE, FALSE	FALSE	The differential termination attribute is designed for the 7 Series FPGA supported differential input I/O standards. It is used to turn the built-in, 100?, differential termination on (TRUE) or off (FALSE).
IBUF_LOW_PWR	Boolean	TRUE, FALSE	TRUE	When set to TRUE, allows for reduced power when using differential or referenced (requiring V_{REF}) input standards like LVDS or HSTL. A setting of FALSE demands more power but delivers higher performance characteristics. Consult the 7 Series FPGA SelectIO Resources User Guide for details.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- IOBUFDS_DIFF_OUT: Differential Bi-directional Buffer with Differential Output
--                   7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

IOBUFDS_DIFF_OUT_inst : IOBUFDS_DIFF_OUT
generic map (
   DIFF_TERM => FALSE, -- Differential Termination (TRUE/FALSE)
   IBUF_LOW_PWR => TRUE, -- Low Power - TRUE, High Performance = FALSE
   IOSTANDARD => "BLVDS_25") -- Specify the I/O standard
port map (
   O => O,     -- Buffer p-side output
   OB => OB,   -- Buffer n-side output
   IO => IO,   -- Diff_p inout (connect directly to top-level port)
   IOB => IOB, -- Diff_n inout (connect directly to top-level port)
   I => I,     -- Buffer input
   TM => TM,   -- 3-state enable input, high=input, low=output
   TS => TS    -- 3-state enable input, high=output, low=input
);
```

```
-- End of IOBUFDS_DIFF_OUT_inst instantiation
```

Verilog Instantiation Template

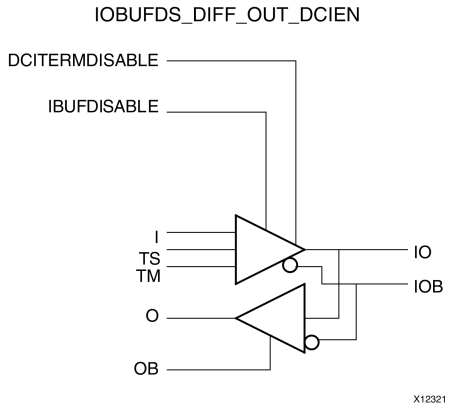
```
// IOBUFDS_DIFF_OUT: Differential Bi-directional Buffer with Differential Output
//                   7 Series
// Xilinx HDL Libraries Guide, version 2012.2

IOBUFDS_DIFF_OUT #(
   .DIFF_TERM("FALSE"),    // Differential Termination ("TRUE"/"FALSE")
   .IBUF_LOW_PWR("TRUE"),  // Low Power - "TRUE", High Performmance = "FALSE"
   .IOSTANDARD("BLVDS_25") // Specify the I/O standard
) IOBUFDS_DIFF_OUT_inst (
   .O(O),     // Buffer p-side output
   .OB(OB),   // Buffer n-side output
   .IO(IO),   // Diff_p inout (connect directly to top-level port)
   .IOB(IOB), // Diff_n inout (connect directly to top-level port)
   .I(I),     // Buffer input
   .TM(TM),   // 3-state enable input, high=input, low=output
   .TS(TS)    // 3-state enable input, high=output, low=input
);

// End of IOBUFDS_DIFF_OUT_inst instantiation
```

For More Information

- See the *7 series FPGA SelectIO Resources User Guide (UG471)*.
- See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

IOBUFDS_DIFF_OUT_DCIEN

Primitive: Bi-Directional Differential Buffer with DCI Disable, Input Disable, and Differential Output



Introduction

This design element is a bidirectional differential I/O buffer used to connect internal logic to an external bidirectional pin. This element includes Digitally Controlled Impedance (DCI) termination enable/ disable as well as input path disable as additional power saving features when the I/O is either is an unused state or being used as an output for a sustained amount of time. The IOBUFDS_DIFF_OUT_DCIEN differs from the IOBUFDS_DCIEN in that it allows internal access to both phases of the differential signal. This element may only be placed in High Performance (HP) banks in the 7 series devices.

Port Descriptions

Port	Direction	Width	Function
IO	In/out	1	Bi-directional p-side port connection. Connect directly to top-level port in the design.
IOB	In/out	1	Bi-directional n-side port connection. Connect directly to top-level port in the design.
I	Input	1	Buffer input representing the output path to the device.
IBUFDISABLE	Input	1	Disables input path. When this signal is asserted HIGH and the attribute USE_IBUFDISABLE is set to "TRUE", the input path through the input buffer is disabled and forced to a logic HIGH.. If USE_IBUFDISABLE is set to "FALSE" this input is ignored and should be tied to ground. This feature is generally used to reduce power at times when the I/O is either idle or during sustained write (output) conditions.

Port	Direction	Width	Function
DCITERMDISABLE	Input	1	Disables DCI termination. When this signal is asserted HIGH, DCI termination is disabled. This feature is generally used to reduce power at times when the I/O is either idle or during sustained write (output) conditions.
TM	Input	1	P-side or master side of the high impedance 3-state mode when the I/O is being used for a read (input) operation. The TM pin also affects the IBUFDISABLE function when USE_IBUFDISABLE = "TRUE".
TS	Input	1	N-side or slave side of the high impedance 3-state mode when the I/O is being used for a read (input) operation. The TM pin also affects the IBUFDISABLE function when USE_IBUFDISABLE = "TRUE".
O	Output	1	Buffer p-side output representing the input path to the device.
OB	Output	1	Buffer n-side output representing the input path to the device.

Design Entry Method

Instantiation	Yes
Inference	No
CORE Generator™ and wizards	Yes
Macro support	No

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
DIFF_TERM	String	"TRUE", "FALSE"	"FALSE"	Enable the built-in differential termination.
IBUF_LOW_PWR	String	"TRUE", "FALSE"	"TRUE"	Allows a trade off of lower power consumption vs highest performance.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
USE_IBUFDISABLE	String	"TRUE", "FALSE"	"TRUE"	Enables or disables the feature of IBUFDISABLE. Set to FALSE when it is not desirable to have the T pin disable input path to allow a read during write operation. When set to TRUE deasserting T (IO used as output) or asserting IBUFDISABLE will disable the input path through the buffer and forces to a logic high.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- IOBUFDS_DIFF_OUT_DCIEN: Differential Bi-directional Buffer with Differential Output,
--                         Digital Controlled Impedance (DCI)and Input path enable/disable
--                         May only be placed in High Performance (HP) Banks
--                         7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

IOBUFDS_DIFF_OUT_DCIEN_inst : IOBUFDS_DIFF_OUT_DCIEN
generic map (
   DIFF_TERM => "FALSE", -- Differential Termination (TRUE/FALSE)
   IBUF_LOW_PWR => "TRUE", -- Low Power - TRUE, High Performance = FALSE
   IOSTANDARD => "BLVDS_25", -- Specify the I/O standard
   USE_IBUFDISABLE => "TRUE") -- Use IBUFDISABLE function, "TRUE" or "FALSE"
port map (
   O => O,     -- Buffer p-side output
   OB => OB,   -- Buffer n-side output
   IO => IO,   -- Diff_p inout (connect directly to top-level port)
   IOB => IOB, -- Diff_n inout (connect directly to top-level port)
   DCITERMDISABLE => DCITERMDISABLE, -- DCI Termination enable input
   I => I,     -- Buffer input
   IBUFTERMDISABLE => IBUFTERMDISABLE, -- input disable input, low=disable
   TM => TM,   -- 3-state enable input, high=input, low=output
   TS => TS    -- 3-state enable input, high=output, low=input
);

-- End of IOBUFDS_DIFF_OUT_DCIEN_inst instantiation
```

Verilog Instantiation Template

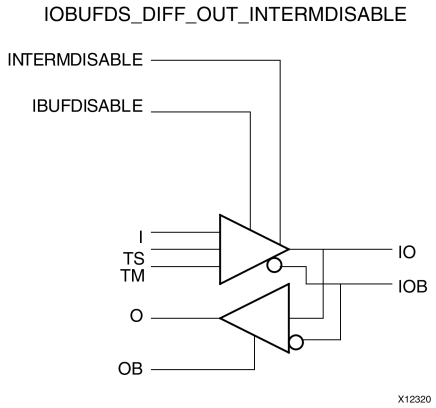
```
// IOBUFDS_DIFF_OUT_DCIEN: Differential Bi-directional Buffer with Differential Output,
//                         Digital Controlled Impedance (DCI)and Input path enable/disable
//                         May only be placed in High Performrmance (HP) Banks
//                         7 Series
// Xilinx HDL Libraries Guide, version 2012.2

IOBUFDS_DIFF_OUT_DCIEN #(
   .DIFF_TERM("FALSE"),     // Differential Termination ("TRUE"/"FALSE")
   .IBUF_LOW_PWR("TRUE"),   // Low Power - "TRUE", High Performrmance = "FALSE"
   .IOSTANDARD("BLVDS_25"), // Specify the I/O standard
   .USE_IBUFDISABLE("TRUE") // Use IBUFDISABLE function, "TRUE" or "FALSE"
) IOBUFDS_DIFF_OUT_DCIEN_inst (
   .O(O),     // Buffer p-side output
   .OB(OB),   // Buffer n-side output
   .IO(IO),   // Diff_p inout (connect directly to top-level port)
   .IOB(IOB), // Diff_n inout (connect directly to top-level port)
   .DCITERMDISABLE(DCITERMDISABLE), //  DCI Termination enable input
   .I(I),                           // Buffer input
   .IBUFDISABLE(IBUFDISABLE),       // Input disable input, low=disable
   .TM(TM),   // 3-state enable input, high=input, low=output
   .TS(TS)    // 3-state enable input, high=output, low=input
);

// End of IOBUFDS_DIFF_OUT_DCIEN_inst instantiation
```

For More Information

- See the *7 series FPGA SelectIO Resources User Guide (UG471)*.
- See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

IOBUFDS_DIFF_OUT_INTERMDISABLE

Primitive: Bi-Directional Differential Buffer with Input Termination Disable, Input Disable, and Differential Output



Introduction

This design element is a bidirectional differential I/O Buffer used to connect internal logic to an external bidirectional pin. This element includes an uncalibrated input termination (INTERM) disable as well as input path disable as additional power saving features when the I/O is either is an unused state or being used as an output for several clock cycles. The IOBUFDS_DIFF_OUT_INTERMDISABLE differs from the IOBUFDS_INTERMDISABLE in that it allows internal access to both phases of the differential signal. This element may only be placed in High Range (HR) banks in the 7 series devices.

Port Descriptions

Port	Direction	Width	Function
IO	In/out	1	Bi-directional p-side port connection. Connect directly to top-level port in the design.
IOB	In/out	1	Bi-directional n-side port connection. Connect directly to top-level port in the design.
I	Input	1	Buffer input representing the output path to the device.
IBUFDISABLE	Input	1	Disables input path through the buffer and forces to a logic high when USE_IBUFDISABLE is set to "TRUE". If USE_IBUFDISABLE is set to "FALSE" this input is ignored and should be tied to ground. This feature is generally used to reduce power at times when the I/O is either idle or during sustained write (output) conditions.
INTERMDISABLE	Input	1	Disables input termination. This feature is generally used to reduce power at times when the I/O

Port	Direction	Width	Function
			is either idle or during sustained write (output) conditions.
TM	Input	1	P-side or master side of the high impedance 3-state mode when the I/O is being used for a read (input) operation. The TM pin also affects the IBUFDISABLE function when USE_IBUFDISABLE = "TRUE", and disables INTERM when in a write (output) mode.
TS	Input	1	N-side or slave side of the high impedance 3-state mode when the I/O is being used for a read (input) operation. The TS pin also affects the IBUFDISABLE function when USE_IBUFDISABLE = "TRUE", and disables INTERM when in a write (output) mode.
O	Output	1	Buffer p-side output representing the input path to the device.
OB	Output	1	Buffer n-side output representing the input path to the device.

Design Entry Method

Instantiation	Yes
Inference	No
CORE Generator™ and wizards	Yes
Macro support	No

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
DIFF_TERM	String	"TRUE", "FALSE"	"FALSE"	Enable the built-in differential termination.
IBUF_LOW_PWR	String	"TRUE", "FALSE"	"TRUE"	Allows a trade off of lower power consumption vs. highest performance when referenced I/O standards are used.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
USE_IBUFDISABLE	String	"TRUE", "FALSE"	"TRUE"	Enables or disables the feature of IBUFDISABLE. Generally used when it is not desirable to have the T pin disable input path to allow a read during write operation.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- IOBUFDS_DIFF_OUT_INTERMDISABLE:  Differential Global Clock Buffer with Differential Output
--                                  Input Termination and Input Path Disable
--                                  May only be placed in High Range (HR) Banks
--                                  7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

IOBUFDS_DIFF_OUT_INTERMDISABLE_inst : IOBUFDS_DIFF_OUT_INTERMDISABLE
generic map (
   DIFF_TERM => "FALSE", -- Differential Termination (TRUE/FALSE)
   IBUF_LOW_PWR => "TRUE", -- Low Power - TRUE, High Performance = FALSE
   IOSTANDARD => "BLVDS_25", -- Specify the I/O standard
   USE_IBUFDISABLE => "TRUE") -- Use IBUFDISABLE function, "TRUE" or "FALSE"
port map (
   O => O,     -- Buffer p-side output
   OB => OB,   -- Buffer n-side output
   IO => IO,   -- Diff_p inout (connect directly to top-level port)
   IOB => IOB, -- Diff_n inout (connect directly to top-level port)
   DCITERMDISABLE => DCITERMDISABLE, -- DCI Termination enable input
   I => I,     -- Buffer input
   IBUFDISABLE => IBUFDISABLE, -- input disable input, low=disable
   INTERMDISABLE => INTERMDISABLE, -- Input termination disable input
   TM => TM,   -- 3-state enable input, high=input, low=output
   TS => TS    -- 3-state enable input, high=output, low=input
);

-- End of IOBUFDS_DIFF_OUT_INTERMDISABLE_inst instantiation
```

Verilog Instantiation Template

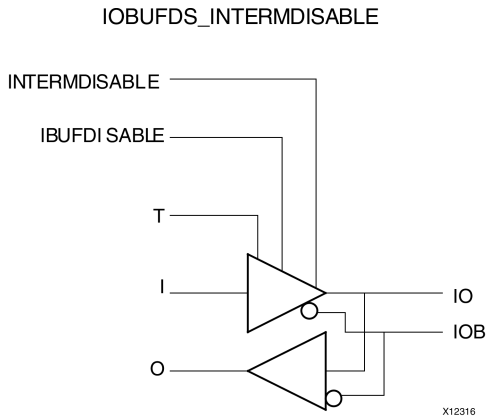
```
// IOBUFDS_DIFF_OUT_INTERMDISABLE: Differential Global Clock Buffer with Differential Output
//                                 Input Termination and Input Path Disable
//                                 May only be placed in High Range (HR) Banks
//                                 7 Series
// Xilinx HDL Libraries Guide, version 2012.2

IOBUFDS_DIFF_OUT_INTERMDISABLE #(
   .DIFF_TERM("FALSE"),     // Differential Termination, "TRUE"/"FALSE"
   .IBUF_LOW_PWR("TRUE"),   // Low power="TRUE", Highest performrmance="FALSE"
   .IOSTANDARD("DEFAULT"),  // Specify the input I/O standard
   .USE_IBUFDISABLE("TRUE") // Set to "TRUE" to enable IBUFDISABLE feature
) IOBUFDS_DIFF_OUT_INTERMDISABLE_inst (
   .O(O),     // Buffer p-side output
   .OB(OB),   // Buffer n-side output
   .IO(IO),   // Diff_p inout (connect directly to top-level port)
   .IOB(IOB), // Diff_n inout (connect directly to top-level port)
   .I(I),     // Buffer input
   .INTERMDISABLE(INTERMDISABLE), //  Input termination disable input
   .IBUFDISABLE(IBUFDISABLE),     // Input disable input, low=disable
   .TM(TM),   // 3-state enable input, high=input, low=output
   .TS(TS)    // 3-state enable input, high=output, low=input
);

// End of IOBUFDS_DIFF_OUT_INTERMDISABLE_inst instantiation
```

For More Information

- See the *7 series FPGA SelectIO Resources User Guide (UG471)*.
- See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

IOBUFDS_INTERMDISABLE

Primitive: Bi-Directional Differential Buffer with Input Termination Disable and Input Disable



Introduction

This design element is a bidirectional differential I/O buffer used to connect internal logic to an external bidirectional pin. This element includes an uncalibrated input termination (INTERM) disable as well as an input path disable as additional power saving features when the I/O is either is an unused state or being used as an output for a sustained amount of time. This element may only be placed in High Range (HR) banks in 7 series devices.

Port Descriptions

Port	Direction	Width	Function
IO	In/out	1	Bi-directional p-side port connection. Connect directly to top-level port in the design.
IOB	In/out	1	Bi-directional n-side port connection. Connect directly to top-level port in the design.
I	Input	1	Buffer input representing the output path to the device.
IBUFDISABLE	Input	1	Disables input path through the buffer and forces to a logic high when USE_IBUFDISABLE is set to "TRUE". If USE_IBUFDISABLE is set to "FALSE" this input is ignored and should be tied to ground. This feature is generally used to reduce power at times when the I/O is either idle or during sustained write (output) conditions.
INTERMDISABLE	Input	1	Disables input termination. This feature is generally used to reduce power at times when the I/O is either idle or during sustained write (output) conditions.

T	Input	1	Sets the I/O in a high impedance 3-state mode when the I/O is being used for a read (input) operation. The T pin also affects the IBUFDISABLE function when USE_IBUFDISABLE = "TRUE". The T pin also disables INTERM when in a write (output) mode.
O	Output	1	Buffer output representing the input path to the device.

Design Entry Method

Instantiation	Yes
Inference	No
CORE Generator™ and wizards	Yes
Macro support	No

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
DIFF_TERM	String	"TRUE", "FALSE"	"FALSE"	Enable the built-in differential termination.
IBUF_LOW_PWR	String	"TRUE", "FALSE"	"TRUE"	Allows a trade off of lower power consumption vs. highest performance when referenced I/O standards are used.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
SLEW	String	"SLOW" or "FAST"	"SLOW"	Sets the output rise and fall time. See the Data Sheet for recommendations of the best setting for this attribute.
USE_IBUFDISABLE	String	"TRUE", "FALSE"	"TRUE"	Enables or disables the feature of IBUFDISABLE. Generally used when it is not desirable to have the T pin disable input path to allow a read during write operation.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;

-- IOBUFDS_INTERMDISABLE: Differential Bi-directional Buffer with Input Termination
--                        and Input path enable/disable
--                        May only be placed in High Range (HR) Banks
--                        7 Series
-- Xilinx HDL Libraries Guide, version 2012.2
```

```
IOBUFDS_INTERMDISABLE_inst : IOBUFDS_INTERMDISABLE
generic map (
   DIFF_TERM => "FALSE", -- Differential termination (TRUE/FALSE)
   IBUF_LOW_PWR => "TRUE", -- Low Power - TRUE, HIGH Performance = FALSE
   IOSTANDARD => "BLVDS_25", -- Specify the I/O standard
   SLEW => "SLOW",   -- Specify the output slew rate
   USE_IBUFDISABLE => "TRUE") -- Use IBUFDISABLE function "TRUE" or "FALSE"
port map (
   O => O,     -- Buffer output
   IO => IO,   -- Diff_p inout (connect directly to top-level port)
   IOB => IOB, -- Diff_n inout (connect directly to top-level port)
   DCITERMDISABLE => DCITERMDISABLE, -- DCI Termination enable input
   I => I,     -- Buffer input
   IBUFDISABLE => IBUFDISABLE, -- Input disable input, low=disable
   INTERMDISABLE => INTERMDISABLE, -- Input termination disable input
   T => T      -- 3-state enable input, high=input, low=output
);

-- End of IOBUFDS_INTERMDISABLE_inst instantiation
```

Verilog Instantiation Template

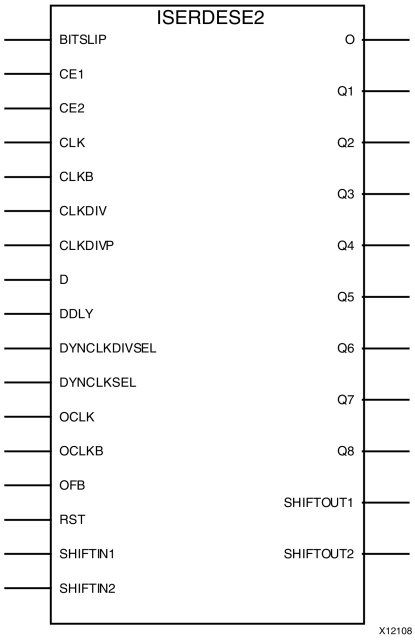
```
// IOBUFDS_INTERMDISABLE: Differential Bi-directional Buffer with Input Termination
//                        and Input path enable/disable
//                        May only be placed in High Range (HR) Banks
//                        7 Series
// Xilinx HDL Libraries Guide, version 2012.2

IOBUFDS_INTERMDISABLE #(
   .DIFF_TERM("FALSE"),     // Differential Termination ("TRUE"/"FALSE")
   .IBUF_LOW_PWR("TRUE"),   // Low Power - "TRUE", High Perforrmance = "FALSE"
   .IOSTANDARD("BLVDS_25"), // Specify the I/O standard
   .SLEW("SLOW"),           // Specify the output slew rate
   .USE_IBUFDISABLE("TRUE") // Use IBUFDISABLE function, "TRUE" or "FALSE"
) IOBUFDS_INTERMDISABLE_inst (
   .O(O),     // Buffer output
   .IO(IO),   // Diff_p inout (connect directly to top-level port)
   .IOB(IOB), // Diff_n inout (connect directly to top-level port)
   .I(I),     // Buffer input
   .IBUFDISABLE(IBUFDISABLE),     // Input disable input, low=disable
   .INTERMDISABLE(INTERMDISABLE), // Input termination disable input
   .T(T)      // 3-state enable input, high=input, low=output
);

// End of IOBUFDS_INTERMDISABLE_inst instantiation
```

For More Information

- See the *7 series FPGA SelectIO Resources User Guide (UG471)*.
- See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

ISERDESE2

Primitive: Input SERial/DESerializer with bitslip



Introduction

The ISERDESE2 in 7 series FPGAs is a dedicated serial-to-parallel converter with specific clocking and logic features designed to facilitate the implementation of high-speed source-synchronous applications. The ISERDESE2 avoids the additional timing complexities encountered when designing deserializers in the FPGA fabric. ISERDESE2 features include:

- Dedicated Deserializer/Serial-to-Parallel Converter, which enables high-speed data transfer without requiring the FPGA fabric to match the input data frequency. This converter supports both single data rate (SDR) and double data rate (DDR) modes. In SDR mode, the serial-to-parallel converter creates a 2-, 3-, 4-, 5-, 6-, 7-, or 8-bit wide parallel word. In DDR mode, the serial-to-parallel converter creates a 4-, 6-, 8-, 10-, or 14-bit-wide parallel word.
- Bitslip Submodule, which lets designers reorder the sequence of the parallel data stream going into the FPGA fabric. This can be used for training source-synchronous interfaces that include a training pattern.
- Dedicated Support for Strobe-based Memory Interfaces, including the OCLK input pin, to handle the strobe-to-FPGA clock domain crossover entirely within the ISERDESE2 block. This allows for higher performance and a simplified implementation.
- Dedicated Support for Networking Interfaces
- Dedicated Support for Memory Interfaces

Port Descriptions

Port	Type	Width	Function
BITSLIP	Input	1	The BITSLIP pin performs a Bitslip operation synchronous to CLKDIV when asserted (active High). Subsequently, the data seen on the Q1 to Q8 output ports will shift, as in a barrel-shifter operation, one position every time Bitslip is invoked (DDR operation is different from SDR).
CE1, CE2	Input	1	Each ISERDESE2 block contains an input clock enable module. When NUM_CE = 1, the CE2 input is not used, and the CE1 input is an active high clock enable connected directly to the input registers in the ISERDESE2. When NUM_CE = 2, the CE1 and CE2 inputs are both used, with CE1 enabling the ISERDESE2 for half of a CLKDIV cycle, and CE2 enabling the ISERDESE2 for the other half. The clock enable module functions as a 2:1 serial-to-parallel converter, clocked by CLKDIV. The clock enable module is needed specifically for bidirectional memory interfaces when ISERDESE2 is configured for 1:4 deserialization in DDR mode. When the attribute NUM_CE = 2, the clock enable module is enabled and both CE1 and CE2 ports are available. When NUM_CE = 1, only CE1 is available and functions as a regular clock enable.
CLK	Input	1	The high-speed clock input (CLK) is used to clock in the input serial data stream.
CLKB	Input	1	The high-speed secondary clock input (CLKB) is used to clock in the input serial data stream. In any mode other than "MEMORY_QDR", connect CLKB to an inverted version of CLK. In "MEMORY_QDR" mode CLKB should be connected to a unique, phase shifted clock.
CLKDIV	Input	1	The divided clock input (CLKDIV) is typically a divided version of CLK (depending on the width of the implemented deserialization). It drives the output of the serial-to-parallel converter, the Bitslip submodule, and the CE module.
CLKDIVP	Input	1	Only supported in MIG. Sourced by PHASER_IN divided CLK in MEMORY_DDR3 mode. All other modes connect to ground.
D	Input	1	The serial input data port (D) is the serial (high-speed) data input port of the ISERDESE2. This port works in conjunction only with the 7 series FPGA I/O resource.
DDLY	Input	1	The serial input data port (DDLY) is the serial (high-speed) data input port of the ISERDESE2. This port works in conjunction only with the 7 series FPGA IDELAYE2 resource.
DYNCLKDIVSEL	Input	1	Dynamically select CLKDIV inversion.
DYNCLKSEL	Input	1	Dynamically select CLK and CLKB inversion.
O	Output	1	The combinatorial output port (O) is an unregistered output of the ISERDESE2 module. This output can come directly from the data input (D), or from the data input (DDLY) via the IDELAYE2.

Port	Type	Width	Function
OCLK	Input	1	The OCLK clock input synchronizes data transfer in strobe-based memory interfaces. The OCLK clock is only used when INTERFACE_TYPE is set to "MEMORY". The OCLK clock input is used to transfer strobe-based memory data onto a free-running clock domain. OCLK is a free-running FPGA clock at the same frequency as the strobe on the CLK input. The timing of the domain transfer is set by the user by adjusting the delay of the strobe signal to the CLK input (e.g., using IDELAY). Examples of setting the timing of this domain transfer are given in the Memory Interface Generator (MIG). When INTERFACE_TYPE is "NETWORKING", this port is unused and should be connected to GND.
OCLKB	Input	1	The OCLK clock input synchronizes data transfer in strobe-based memory interfaces. The OCLKB clock is only used when INTERFACE_TYPE is set to "MEMORY".
OFB	Input	1	The serial input data port (OFB) is the serial (high-speed) data input port of the ISERDESE2. This port works in conjunction only with the 7 series FPGA OSERDESE2 port OFB.
Q1 - Q8	Output	1	The output ports Q1 to Q8 are the registered outputs of the ISERDESE2 module. One ISERDESE2 block can support up to eight bits (i.e., a 1:8 deserialization). Bit widths greater than eight (up to 14) can be supported using Width Expansion. The first data bit received appears on the highest order Q output. The bit ordering at the input of an OSERDESE2 is the opposite of the bit ordering at the output of an ISERDESE2 block. For example, the least significant bit A of the word FEDCBA is placed at the D1 input of an OSERDESE2, but the same bit A emerges from the ISERDESE2 block at the Q8 output. In other words, D1 is the least significant input to the OSERDESE2, while Q8 is the least significant output of the ISERDESE2 block. When width expansion is used, D1 of the master OSERDESE1 is the least significant input, while Q7 of the slave ISERDESE2 block is the least significant output.
RST	Input	1	The reset input causes the outputs of all data flip-flops in the CLK and CLKDIV domains to be driven low asynchronously. ISERDESE2 circuits running in the CLK domain where timing is critical use an internal, dedicated circuit to retime the RST input to produce a reset signal synchronous to the CLK domain. Similarly, there is a dedicated circuit to retime the RST input to produce a reset signal synchronous to the CLKDIV domain. Because the ISERDESE2 is driven into reset asynchronously but comes out of reset synchronously it must be treated as a synchronous reset to the CLKDIV time domain and have a minimum pulse of one CLKDIV cycle. When building an interface consisting of multiple ISERDESE2 ports, all ISERDESE2 ports in the interface must be synchronized. The internal retiming of the RST input is designed so that all ISERDESE2 blocks that receive the same reset pulse come out of reset synchronized with one another.
SHIFTIN1-SHIFTIN2	Input	1	If SERDES_MODE="SLAVE", connect SHIFTIN1/2 to the master ISERDESE2 SHIFTOUT1/2 outputs. Otherwise, leave SHIFTOUT1/2 unconnected and/or SHIFTIN1/2 grounded.
SHIFTOUT1-SHIFTOUT2	Output	1	If SERDES_MODE="MASTER" and two ISERDESE2s are to be cascaded, connect SHIFTOUT1/2 to the slave ISERDESE2 SHIFTIN1/2 inputs.

Design Entry Method

Instantiation	Yes
Inference	No
CORE Generator™ and wizards	Yes
Macro support	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
DATA_RATE	STRING	"DDR", "SDR"	"DDR"	The DATA_RATE attribute defines whether the incoming data stream is processed as single data rate (SDR) or double data rate (DDR).
DATA_WIDTH	DECIMAL	4, 2, 3, 5, 6, 7, 8, 10, 14	4	Defines the width of the serial-to-parallel converter. The legal value depends on the DATA_RATE attribute (SDR or DDR). • If DATA_RATE = DDR, value is limited to 4, 6, 8, 10 or 14. • If DATA_RATE = SDR, value is limited to 2, 3, 4, 5, 6, 7, or 8.
DYN_CLKDIV_INV_EN	STRING	"FALSE", "TRUE"	"FALSE"	Enables DYNCLKDIVINVSEL inversion when TRUE and disables HDL inversions on CLKDIV pin.
DYN_CLK_INV_EN	STRING	"FALSE", "TRUE"	"FALSE"	Enables DYNCLKINVSEL inversion when TRUE and disables HDL inversions on CLK and CLKB pins.
INIT_Q1, INIT_Q2, INIT_Q3, INIT_Q4	BINARY	1'b0 to 1'b1	1'b0	Defines the initial value on the Q1 through Q4 outputs after configuration.
INTERFACE_TYPE	STRING	"MEMORY", "MEMORY_DDR3", "MEMORY_QDR", "NETWORKING", "OVERSAMPLE"	"MEMORY"	Specifies mode of operation for the ISERDESE2. For details on each mode, please refer to the 7 series FPGA SelectIO Resources User Guide.

Attribute	Type	Allowed Values	Default	Description
IOBDELAY	STRING	"NONE", "BOTH", "IBUF", "IFD"	"NONE"	Defines input sources for ISERDESE2 module. The D and DDLY pins are dedicated inputs to the ISERDESE2. The D input is a direct connection to the I/O. The DDLY pin is a direct connection to the IODELAYE2. This allows the user to either have a delayed or non-delayed version of the input to the registered (Q1- Q6) or combinatorial path (O) output. The attribute IOBDELAY determines the input applied the output. • "NONE" - O => D | Q1-Q6 => D • "IBUF" - O => DDLY | Q1-Q6 => D • "IFD" - O => D | Q1-Q6 => DDLY • "BOTH" - O => DDLY | Q1-Q6 => DDLY
NUM_CE	DECIMAL	2, 1	2	The NUM_CE attribute defines the number of clock enables (CE1 and CE2) used.
OFB_USED	STRING	"FALSE", "TRUE"	"FALSE"	Enables the path from the OLOGIC, OSERDES OFB pin to the ISERDES OFB pin. Disables the use of the D input pin.
SERDES_MODE	STRING	"MASTER", "SLAVE"	"MASTER"	The SERDES_MODE attribute defines whether the ISERDESE2 module is a master or slave when using width expansion. Set to "MASTER" when not using width explansion.
SRVAL_Q1, SRVAL_Q2, SRVAL_Q3, SRVAL_Q4	BINARY	1'b0 to 1'b1	1'b0	Defines the value (set or reset) of Q1 through Q4 outputs when the SR pin is invoked.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- ISERDESE2: Input SERial/DESerializer with bitslip
--            7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

ISERDESE2_inst : ISERDESE2
generic map (
   DATA_RATE => "DDR",           -- DDR, SDR
```

```
   DATA_WIDTH => 4,              -- Parallel data width (2-8,10,14)
   DYN_CLKDIV_INV_EN => "FALSE", -- Enable DYNCLKDIVINVSEL inversion (FALSE, TRUE)
   DYN_CLK_INV_EN => "FALSE",    -- Enable DYNCLKINVSEL inversion (FALSE, TRUE)
   -- INIT_Q1 - INIT_Q4: Initial value on the Q outputs (0/1)
   INIT_Q1 => '0',
   INIT_Q2 => '0',
   INIT_Q3 => '0',
   INIT_Q4 => '0',
   INTERFACE_TYPE => "MEMORY",   -- MEMORY, MEMORY_DDR3, MEMORY_QDR, NETWORKING, OVERSAMPLE
   IOBDELAY => "NONE",           -- NONE, BOTH, IBUF, IFD
   NUM_CE => 2,                  -- Number of clock enables (1,2)
   OFB_USED => "FALSE",          -- Select OFB path (FALSE, TRUE)
   SERDES_MODE => "MASTER",      -- MASTER, SLAVE
   -- SRVAL_Q1 - SRVAL_Q4: Q output values when SR is used (0/1)
   SRVAL_Q1 => '0',
   SRVAL_Q2 => '0',
   SRVAL_Q3 => '0',
   SRVAL_Q4 => '0'
)
port map (
   O => O,                       -- 1-bit output: Combinatorial output
   -- Q1 - Q8: 1-bit (each) output: Registered data outputs
   Q1 => Q1,
   Q2 => Q2,
   Q3 => Q3,
   Q4 => Q4,
   Q5 => Q5,
   Q6 => Q6,
   Q7 => Q7,
   Q8 => Q8,
   -- SHIFTOUT1-SHIFTOUT2: 1-bit (each) output: Data width expansion output ports
   SHIFTOUT1 => SHIFTOUT1,
   SHIFTOUT2 => SHIFTOUT2,
   BITSLIP => BITSLIP,           -- 1-bit input: The BITSLIP pin performs a Bitslip operation synchronous to
                                 -- CLKDIV when asserted (active High). Subsequently, the data seen on the
                                 -- Q1 to Q8 output ports will shift, as in a barrel-shifter operation, one
                                 -- position every time Bitslip is invoked (DDR operation is different from
                                 -- SDR).

   -- CE1, CE2: 1-bit (each) input: Data register clock enable inputs
   CE1 => CE1,
   CE2 => CE2,
   CLKDIVP => CLKDIVP,           -- 1-bit input: TBD
   -- Clocks: 1-bit (each) input: ISERDESE2 clock input ports
   CLK => CLK,                   -- 1-bit input: High-speed clock
   CLKB => CLKB,                 -- 1-bit input: High-speed secondary clock
   CLKDIV => CLKDIV,             -- 1-bit input: Divided clock
   OCLK => OCLK,                 -- 1-bit input: High speed output clock used when INTERFACE_TYPE="MEMORY"
   -- Dynamic Clock Inversions: 1-bit (each) input: Dynamic clock inversion pins to switch clock polarity
   DYNCLKDIVSEL => DYNCLKDIVSEL, -- 1-bit input: Dynamic CLKDIV inversion
   DYNCLKSEL => DYNCLKSEL,       -- 1-bit input: Dynamic CLK/CLKB inversion
   -- Input Data: 1-bit (each) input: ISERDESE2 data input ports
   D => D,                       -- 1-bit input: Data input
   DDLY => DDLY,                 -- 1-bit input: Serial data from IDELAYE2
   OFB => OFB,                   -- 1-bit input: Data feedback from OSERDESE2
   OCLKB => OCLKB,               -- 1-bit input: High speed negative edge output clock
   RST => RST,                   -- 1-bit input: Active high asynchronous reset
   -- SHIFTIN1-SHIFTIN2: 1-bit (each) input: Data width expansion input ports
   SHIFTIN1 => SHIFTIN1,
   SHIFTIN2 => SHIFTIN2
);

-- End of ISERDESE2_inst instantiation
```

Verilog Instantiation Template

```
// ISERDESE2: Input SERial/DESerializer with bitslip
//            7 Series
// Xilinx HDL Libraries Guide, version 2012.2
```

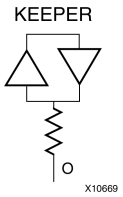
```
ISERDESE2 #(
   .DATA_RATE("DDR"),           // DDR, SDR
   .DATA_WIDTH(4),              // Parallel data width (2-8,10,14)
   .DYN_CLKDIV_INV_EN("FALSE"), // Enable DYNCLKDIVINVSEL inversion (FALSE, TRUE)
   .DYN_CLK_INV_EN("FALSE"),    // Enable DYNCLKINVSEL inversion (FALSE, TRUE)
   // INIT_Q1 - INIT_Q4: Initial value on the Q outputs (0/1)
   .INIT_Q1(1'b0),
   .INIT_Q2(1'b0),
   .INIT_Q3(1'b0),
   .INIT_Q4(1'b0),
   .INTERFACE_TYPE("MEMORY"),   // MEMORY, MEMORY_DDR3, MEMORY_QDR, NETWORKING, OVERSAMPLE
   .IOBDELAY("NONE"),           // NONE, BOTH, IBUF, IFD
   .NUM_CE(2),                  // Number of clock enables (1,2)
   .OFB_USED("FALSE"),          // Select OFB path (FALSE, TRUE)
   .SERDES_MODE("MASTER"),      // MASTER, SLAVE
   // SRVAL_Q1 - SRVAL_Q4: Q output values when SR is used (0/1)
   .SRVAL_Q1(1'b0),
   .SRVAL_Q2(1'b0),
   .SRVAL_Q3(1'b0),
   .SRVAL_Q4(1'b0)
)
ISERDESE2_inst (
   .O(O),                       // 1-bit output: Combinatorial output
   // Q1 - Q8: 1-bit (each) output: Registered data outputs
   .Q1(Q1),
   .Q2(Q2),
   .Q3(Q3),
   .Q4(Q4),
   .Q5(Q5),
   .Q6(Q6),
   .Q7(Q7),
   .Q8(Q8),
   // SHIFTOUT1-SHIFTOUT2: 1-bit (each) output: Data width expansion output ports
   .SHIFTOUT1(SHIFTOUT1),
   .SHIFTOUT2(SHIFTOUT2),
   .BITSLIP(BITSLIP),           // 1-bit input: The BITSLIP pin performs a Bitslip operation synchronous to
                                // CLKDIV when asserted (active High). Subsequently, the data seen on the Q1
                                // to Q8 output ports will shift, as in a barrel-shifter operation, one
                                // position every time Bitslip is invoked (DDR operation is different from
                                // SDR).

   // CE1, CE2: 1-bit (each) input: Data register clock enable inputs
   .CE1(CE1),
   .CE2(CE2),
   .CLKDIVP(CLKDIVP),           // 1-bit input: TBD
   // Clocks: 1-bit (each) input: ISERDESE2 clock input ports
   .CLK(CLK),                   // 1-bit input: High-speed clock
   .CLKB(CLKB),                 // 1-bit input: High-speed secondary clock
   .CLKDIV(CLKDIV),             // 1-bit input: Divided clock
   .OCLK(OCLK),                 // 1-bit input: High speed output clock used when INTERFACE_TYPE="MEMORY"
   // Dynamic Clock Inversions: 1-bit (each) input: Dynamic clock inversion pins to switch clock polarity
   .DYNCLKDIVSEL(DYNCLKDIVSEL), // 1-bit input: Dynamic CLKDIV inversion
   .DYNCLKSEL(DYNCLKSEL),       // 1-bit input: Dynamic CLK/CLKB inversion
   // Input Data: 1-bit (each) input: ISERDESE2 data input ports
   .D(D),                       // 1-bit input: Data input
   .DDLY(DDLY),                 // 1-bit input: Serial data from IDELAYE2
   .OFB(OFB),                   // 1-bit input: Data feedback from OSERDESE2
   .OCLKB(OCLKB),               // 1-bit input: High speed negative edge output clock
   .RST(RST),                   // 1-bit input: Active high asynchronous reset
   // SHIFTIN1-SHIFTIN2: 1-bit (each) input: Data width expansion input ports
   .SHIFTIN1(SHIFTIN1),
   .SHIFTIN2(SHIFTIN2)
);

// End of ISERDESE2_inst instantiation
```

For More Information

- See the *7 series FPGA SelectIO Resources User Guide (UG471)*.
- See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

KEEPER

Primitive: KEEPER Symbol



Introduction

The design element is a weak keeper element that retains the value of the net connected to its bidirectional O pin. For example, if a logic 1 is being driven onto the net, KEEPER drives a weak/resistive 1 onto the net. If the net driver is then 3-stated, KEEPER continues to drive a weak/resistive 1 onto the net.

Port Descriptions

Name	Direction	Width	Function
O	Output	1-Bit	Keeper output

Design Entry Method

Instantiation	Yes
Inference	No
CORE Generator™ and wizards	No
Macro support	No

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- KEEPER: I/O Buffer Weak Keeper
--         7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

KEEPER_inst : KEEPER
port map (
   O => O     -- Keeper output (connect directly to top-level port)
);

-- End of KEEPER_inst instantiation
```

Verilog Instantiation Template

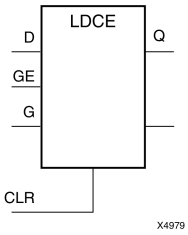
```
// KEEPER: I/O Buffer Weak Keeper
//         7 Series
// Xilinx HDL Libraries Guide, version 2012.2

KEEPER KEEPER_inst (
   .O(O)     // Keeper output (connect directly to top-level port)
);

// End of KEEPER_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

LDCE

Primitive: Transparent Data Latch with Asynchronous Clear and Gate Enable



Introduction

This design element is a transparent data latch with asynchronous clear and gate enable. When the asynchronous clear input (CLR) is High, it overrides the other inputs and resets the data (Q) output Low. Q reflects the data (D) input while the gate (G) input and gate enable (GE) are High and CLR is Low. If (GE) is Low, data on (D) cannot be latched. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) or (GE) remains low.

This latch is asynchronously cleared, outputs Low, when power is applied. Power-on conditions are simulated when global set/reset (GSR) is active.

Logic Table

Inputs				Outputs
CLR	**GE**	**G**	**D**	**Q**
1	X	X	X	0
0	0	X	X	No Change
0	1	1	D	D
0	1	0	X	No Change
0	1	↓	D	D

Design Entry Method

Instantiation	Yes
Inference	Recommended
CORE Generator™ and wizards	No
Macro support	No

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- LDCE: Transparent latch with Asynchronous Reset and
--        Gate Enable.
--        7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

LDCE_inst : LDCE
generic map (
   INIT => '0') -- Initial value of latch ('0' or '1')
port map (
   Q => Q,      -- Data output
   CLR => CLR,  -- Asynchronous clear/reset input
   D => D,      -- Data input
   G => G,      -- Gate input
   GE => GE     -- Gate enable input
);

-- End of LDCE_inst instantiation
```

Verilog Instantiation Template

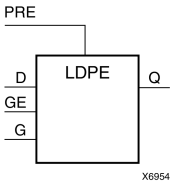
```
// LDCE:  Transparent latch with Asynchronous Reset and Gate Enable.
//        7 Series
// Xilinx HDL Libraries Guide, version 2012.2

LDCE #(
   .INIT(1'b0) // Initial value of latch (1'b0 or 1'b1)
) LDCE_inst (
   .Q(Q),      // Data output
   .CLR(CLR),  // Asynchronous clear/reset input
   .D(D),      // Data input
   .G(G),      // Gate input
   .GE(GE)     // Gate enable input
);

// End of LDCE_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

LDPE

Primitive: Transparent Data Latch with Asynchronous Preset and Gate Enable



Introduction

This design element is a transparent data latch with asynchronous preset and gate enable. When the asynchronous preset (PRE) is High, it overrides the other input and presets the data (Q) output High. Q reflects the data (D) input while the gate (G) input and gate enable (GE) are High. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) or (GE) remains Low.

This latch is asynchronously preset, output High, when power is applied. Power-on conditions are simulated when global set/reset (GSR) is active.

Logic Table

Inputs				Outputs
PRE	**GE**	**G**	**D**	**Q**
1	X	X	X	1
0	0	X	X	No Change
0	1	1	D	D
0	1	0	X	No Change
0	1	↓	D	D

Design Entry Method

Instantiation	Yes
Inference	Recommended
CORE Generator™ and wizards	No
Macro support	No

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Specifies the initial value upon power-up or the assertion of GSR for the (Q) port.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- LDPE:  Transparent latch with Asynchronous Set and
--        Gate Enable.
--        7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

LDPE_inst : LDPE
generic map (
   INIT => '0') -- Initial value of latch ('0' or '1')
port map (
   Q => Q,      -- Data output
   CLR => CLR,  -- Asynchronous preset/set input
   D => D,      -- Data input
   G => G,      -- Gate input
   GE => GE     -- Gate enable input
);

-- End of LDPE_inst instantiation
```

Verilog Instantiation Template

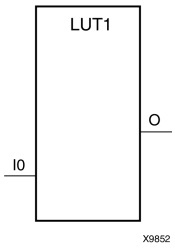
```
// LDPE:  Transparent latch with Asynchronous Preset and Gate Enable.
//        7 Series
// Xilinx HDL Libraries Guide, version 2012.2

LDPE #(
   .INIT(1'b1) // Initial value of latch (1'b0 or 1'b1)
) LDPE_inst (
   .Q(Q),      // Data output
   .PRE(PRE),  // Asynchronous preset/set input
   .D(D),      // Data input
   .G(G),      // Gate input
   .GE(GE)     // Gate enable input
);

// End of LDPE_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

LUT1

Primitive: 1-Bit Look-Up Table with General Output



Introduction

This design element is a 1-bit look-up table (LUT) with general output (O).

An INIT attribute with an appropriate number of hexadecimal digits for the number of inputs must be attached to the LUT to specify its function. This element provides a look-up table version of a buffer or inverter. These elements are the basic building blocks. Multiple variants of LUTs accommodate additional types of outputs that can be used by different timing models for more accurate pre-layout timing estimation.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method: A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method: Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs	Outputs
I0	**O**
0	INIT[0]
1	INIT[1]
INIT = Binary number assigned to the INIT attribute	

Design Entry Method

Instantiation	Yes
Inference	Recommended
CORE Generator™ and wizards	No
Macro support	No

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 2-Bit Value	All zeros	Initializes look-up tables.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- LUT1: 1-input Look-Up Table with general output
--       7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

LUT1_inst : LUT1
generic map (
   INIT => "00")
port map (
   O => O,    -- LUT general output
   I0 => I0  -- LUT input
);

-- End of LUT1_inst instantiation
```

Verilog Instantiation Template

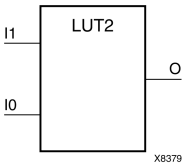
```
// LUT1: 1-input Look-Up Table with general output (Mapped to a LUT6)
//       7 Series
// Xilinx HDL Libraries Guide, version 2012.2

LUT1 #(
   .INIT(2'b00)  // Specify LUT Contents
) LUT1_inst (
   .O(O),   // LUT general output
   .I0(I0)  // LUT input
);

// End of LUT1_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

LUT2

Primitive: 2-Bit Look-Up Table with General Output



Introduction

This design element is a 2-bit look-up table (LUT) with general output (O).

An INIT attribute with an appropriate number of hexadecimal digits for the number of inputs must be attached to the LUT to specify its function. This element provides a look-up table version of a buffer or inverter. These elements are the basic building blocks. Multiple variants of LUTs accommodate additional types of outputs that can be used by different timing models for more accurate pre-layout timing estimation.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method: A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method: Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs		Outputs
I1	**I0**	**O**
0	0	INIT[0]
0	1	INIT[1]
1	0	INIT[2]
1	1	INIT[3]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute		

Design Entry Method

Instantiation	Yes
Inference	Recommended
CORE Generator™ and wizards	No
Macro support	No

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 4-Bit Value	All zeros	Initializes look-up tables.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- LUT2: 2-input Look-Up Table with general output
--       7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

LUT2_inst : LUT2
generic map (
   INIT => X"0")
port map (
   O => O,   -- LUT general output
   I0 => I0, -- LUT input
   I1 => I1  -- LUT input
);

-- End of LUT2_inst instantiation
```

Verilog Instantiation Template

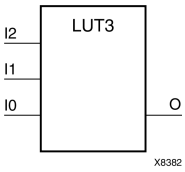
```
// LUT2: 2-input Look-Up Table with general output (Mapped to a LUT6)
//       7 Series
// Xilinx HDL Libraries Guide, version 2012.2

LUT2 #(
   .INIT(4'h0)  // Specify LUT Contents
) LUT2_inst (
   .O(O),   // LUT general output
   .I0(I0), // LUT input
   .I1(I1)  // LUT input
);

// End of LUT2_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

LUT3

Primitive: 3-Bit Look-Up Table with General Output



Introduction

This design element is a 3-bit look-up table (LUT) with general output (O). A mandatory INIT attribute, with an appropriate number of hexadecimal digits for the number of inputs, must be attached to the LUT to specify its function.

An INIT attribute with an appropriate number of hexadecimal digits for the number of inputs must be attached to the LUT to specify its function. This element provides a look-up table version of a buffer or inverter. These elements are the basic building blocks. Multiple variants of LUTs accommodate additional types of outputs that can be used by different timing models for more accurate pre-layout timing estimation.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method: A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method: Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs			Outputs
I2	**I1**	**I0**	**O**
0	0	0	INIT[0]
0	0	1	INIT[1]
0	1	0	INIT[2]
0	1	1	INIT[3]
1	0	0	INIT[4]
1	0	1	INIT[5]

Inputs			Outputs
I2	**I1**	**I0**	**O**
1	1	0	INIT[6]
1	1	1	INIT[7]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute			

Design Entry Method

Instantiation	Yes
Inference	Recommended
CORE Generator™ and wizards	No
Macro support	No

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 8-Bit Value	All zeros	Initializes look-up tables.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- LUT3: 3-input Look-Up Table with general output (Mapped to a LUT6)
--       7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

LUT3_inst : LUT3
generic map (
   INIT => X"00")
port map (
   O => O,   -- LUT general output
   I0 => I0, -- LUT input
   I1 => I1, -- LUT input
   I2 => I2  -- LUT input
);

-- End of LUT3_inst instantiation
```

Verilog Instantiation Template

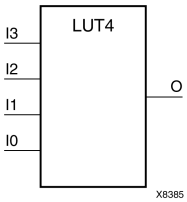
```
// LUT3: 3-input Look-Up Table with general output (Mapped to a LUT6)
//       7 Series
// Xilinx HDL Libraries Guide, version 2012.2

LUT3 #(
   .INIT(8'h00)  // Specify LUT Contents
) LUT3_inst (
   .O(O),   // LUT general output
   .I0(I0), // LUT input
   .I1(I1), // LUT input
   .I2(I2)  // LUT input
);

// End of LUT3_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

LUT4

Primitive: 4-Bit Look-Up-Table with General Output



Introduction

This design element is a 4-bit look-up table (LUT) with general output (O).

An INIT attribute with an appropriate number of hexadecimal digits for the number of inputs must be attached to the LUT to specify its function. This element provides a look-up table version of a buffer or inverter. These elements are the basic building blocks. Multiple variants of LUTs accommodate additional types of outputs that can be used by different timing models for more accurate pre-layout timing estimation.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method: A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method: Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs				Outputs
I3	**I2**	**I1**	**I0**	**O**
0	0	0	0	INIT[0]
0	0	0	1	INIT[1]
0	0	1	0	INIT[2]
0	0	1	1	INIT[3]
0	1	0	0	INIT[4]
0	1	0	1	INIT[5]
0	1	1	0	INIT[6]

Inputs				Outputs
I3	**I2**	**I1**	**I0**	**O**
0	1	1	1	INIT[7]
1	0	0	0	INIT[8]
1	0	0	1	INIT[9]
1	0	1	0	INIT[10]
1	0	1	1	INIT[11]
1	1	0	0	INIT[12]
1	1	0	1	INIT[13]
1	1	1	0	INIT[14]
1	1	1	1	INIT[15]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute				

Design Entry Method

Instantiation	Yes
Inference	Recommended
CORE Generator™ and wizards	No
Macro support	No

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Initializes look-up tables.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- LUT4: 4-input Look-Up Table with general output
--       7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

LUT4_inst : LUT4
generic map (
   INIT => X"0000")
port map (
   O => O,    -- LUT general output
   I0 => I0, -- LUT input
   I1 => I1, -- LUT input
   I2 => I2, -- LUT input
   I3 => I3  -- LUT input
);

-- End of LUT4_inst instantiation
```

Verilog Instantiation Template

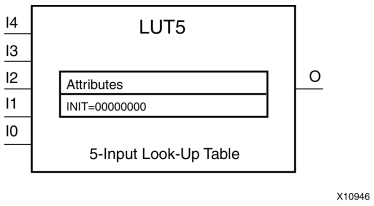
```
// LUT4: 4-input Look-Up Table with general output (Mapped to a LUT6)
//       7 Series
// Xilinx HDL Libraries Guide, version 2012.2

LUT4 #(
   .INIT(16'h0000)  // Specify LUT Contents
) LUT4_inst (
   .O(O),   // LUT general output
   .I0(I0), // LUT input
   .I1(I1), // LUT input
   .I2(I2), // LUT input
   .I3(I3)  // LUT input
);

// End of LUT4_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

LUT5

Primitive: 5-Input Lookup Table with General Output



Introduction

This design element is a 5-input, 1-output look-up table (LUT) that can either act as an asynchronous 32-bit ROM (with 5-bit addressing) or implement any 5-input logic function. LUTs are the basic logic building blocks and are used to implement most logic functions of the design. One LUT5 is packed into a LUT6 within a slice, or two LUT5s can be packed into a single LUT6 with some restrictions. The functionality of the LUT5, LUT5_L and LUT5_D is the same. However, the LUT5_L and LUT5_D allow the additional specification to connect the LUT5 output signal to an internal slice or CLB connection using the LO output. The LUT5_L specifies that the only connections from the LUT5 will be within a slice or CLB, while the LUT5_D allows the specification to connect the output of the LUT to both inter-slice/CLB logic and external logic as well. The LUT5 does not state any specific output connections and should be used in all cases except where internal slice or CLB signal connections must be implicitly specified.

An INIT attribute consisting of a 32-bit hexadecimal value must be specified to indicate the LUTs logical function. The INIT value is calculated by assigning a 1 to the corresponding INIT bit value when the associated inputs are applied. For instance, a Verilog INIT value of 32'h80000000 (X"80000000" for VHDL) makes the output zero unless all of the inputs are one (a 5-input AND gate). A Verilog INIT value of 32'hfffffffe (X"FFFFFFFE" for VHDL) makes the output one unless all zeros are on the inputs (a 5-input OR gate).

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method: A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method: Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs					Outputs
I4	I3	I2	I1	I0	LO
0	0	0	0	0	INIT[0]
0	0	0	0	1	INIT[1]
0	0	0	1	0	INIT[2]
0	0	0	1	1	INIT[3]
0	0	1	0	0	INIT[4]
0	0	1	0	1	INIT[5]
0	0	1	1	0	INIT[6]
0	0	1	1	1	INIT[7]
0	1	0	0	0	INIT[8]
0	1	0	0	1	INIT[9]
0	1	0	1	0	INIT[10]
0	1	0	1	1	INIT[11]
0	1	1	0	0	INIT[12]
0	1	1	0	1	INIT[13]
0	1	1	1	0	INIT[14]
0	1	1	1	1	INIT[15]
1	0	0	0	0	INIT[16]
1	0	0	0	1	INIT[17]
1	0	0	1	0	INIT[18]
1	0	0	1	1	INIT[19]
1	0	1	0	0	INIT[20]
1	0	1	0	1	INIT[21]
1	0	1	1	0	INIT[22]
1	0	1	1	1	INIT[23]
1	1	0	0	0	INIT[24]
1	1	0	0	1	INIT[25]
1	1	0	1	0	INIT[26]
1	1	0	1	1	INIT[27]
1	1	1	0	0	INIT[28]
1	1	1	0	1	INIT[29]
1	1	1	1	0	INIT[30]
1	1	1	1	1	INIT[31]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute					

Port Description

Name	Direction	Width	Function
O	Output	1	5-LUT output
I0, I1, I2, I3, I4	Input	1	LUT inputs

Design Entry Method

Instantiation	Yes
Inference	Recommended
CORE Generator™ and wizards	No
Macro support	No

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 32-Bit Value	All zeros	Specifies the logic value for the look-up tables.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- LUT5: 5-input Look-Up Table with general output (Mapped to SliceM LUT6)
--       7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

LUT5_inst : LUT5
generic map (
   INIT => X"00000000") -- Specify LUT Contents
port map (
   O => O,  -- LUT general output
   I0 => I0,    -- LUT input
   I1 => I1,    -- LUT input
   I2 => I2,    -- LUT input
   I3 => I3,    -- LUT input
   I4 => I4     -- LUT input
);

-- End of LUT5_inst instantiation
```

Verilog Instantiation Template

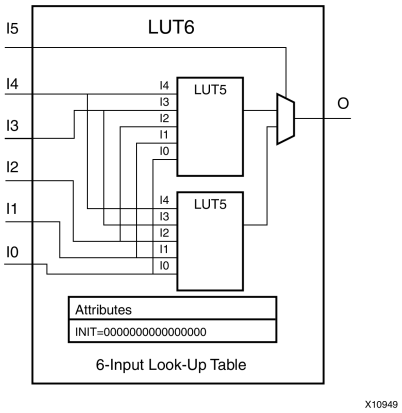
```
// LUT5: 5-input Look-Up Table with general output (Mapped to a LUT6)
//       7 Series
// Xilinx HDL Libraries Guide, version 2012.2

LUT5 #(
   .INIT(32'h00000000)  // Specify LUT Contents
) LUT5_inst (
   .O(O),   // LUT general output
   .I0(I0), // LUT input
   .I1(I1), // LUT input
   .I2(I2), // LUT input
   .I3(I3), // LUT input
   .I4(I4)  // LUT input
);

// End of LUT5_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

LUT6

Primitive: 6-Input Lookup Table with General Output



Introduction

This design element is a 6-input, 1-output look-up table (LUT) that can either act as an asynchronous 64-bit ROM (with 6-bit addressing) or implement any 6-input logic function. LUTs are the basic logic building blocks and are used to implement most logic functions of the design. A LUT6 is mapped to one of the four look-up tables in the slice. The functionality of the LUT6, LUT6_L and LUT6_D is the same. However, the LUT6_L and LUT6_D allow the additional specification to connect the LUT6 output signal to an internal slice, or CLB connection, using the LO output. The LUT6_L specifies that the only connections from the LUT6 will be within a slice, or CLB, while the LUT6_D allows the specification to connect the output of the LUT to both inter-slice/CLB logic and external logic as well. The LUT6 does not state any specific output connections and should be used in all cases except where internal slice or CLB signal connections must be implicitly specified.

An INIT attribute consisting of a 64-bit Hexadecimal value must be specified to indicate the LUTs logical function. The INIT value is calculated by assigning a 1 to corresponding INIT bit value when the associated inputs are applied. For instance, a Verilog INIT value of 64'h8000000000000000 (X"8000000000000000" for VHDL) makes the output zero unless all of the inputs are one (a 6-input AND gate). A Verilog INIT value of 64'hfffffffffffffffe (X"FFFFFFFFFFFFFFFE" for VHDL) makes the output one unless all zeros are on the inputs (a 6-input OR gate).

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method: A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method: Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs						Outputs
I5	I4	I3	I2	I1	I0	O
0	0	0	0	0	0	INIT[0]
0	0	0	0	0	1	INIT[1]
0	0	0	0	1	0	INIT[2]
0	0	0	0	1	1	INIT[3]
0	0	0	1	0	0	INIT[4]
0	0	0	1	0	1	INIT[5]
0	0	0	1	1	0	INIT[6]
0	0	0	1	1	1	INIT[7]
0	0	1	0	0	0	INIT[8]
0	0	1	0	0	1	INIT[9]
0	0	1	0	1	0	INIT[10]
0	0	1	0	1	1	INIT[11]
0	0	1	1	0	0	INIT[12]
0	0	1	1	0	1	INIT[13]
0	0	1	1	1	0	INIT[14]
0	0	1	1	1	1	INIT[15]
0	1	0	0	0	0	INIT[16]
0	1	0	0	0	1	INIT[17]
0	1	0	0	1	0	INIT[18]
0	1	0	0	1	1	INIT[19]
0	1	0	1	0	0	INIT[20]
0	1	0	1	0	1	INIT[21]
0	1	0	1	1	0	INIT[22]
0	1	0	1	1	1	INIT[23]
0	1	1	0	0	0	INIT[24]
0	1	1	0	0	1	INIT[25]
0	1	1	0	1	0	INIT[26]
0	1	1	0	1	1	INIT[27]
0	1	1	1	0	0	INIT[28]
0	1	1	1	0	1	INIT[29]

Inputs						Outputs
I5	I4	I3	I2	I1	I0	O
0	1	1	1	1	0	INIT[30]
0	1	1	1	1	1	INIT[31]
1	0	0	0	0	0	INIT[32]
1	0	0	0	0	1	INIT[33]
1	0	0	0	1	0	INIT[34]
1	0	0	0	1	1	INIT[35]
1	0	0	1	0	0	INIT[36]
1	0	0	1	0	1	INIT[37]
1	0	0	1	1	0	INIT[38]
1	0	0	1	1	1	INIT[39]
1	0	1	0	0	0	INIT[40]
1	0	1	0	0	1	INIT[41]
1	0	1	0	1	0	INIT[42]
1	0	1	0	1	1	INIT[43]
1	0	1	1	0	0	INIT[44]
1	0	1	1	0	1	INIT[45]
1	0	1	1	1	0	INIT[46]
1	0	1	1	1	1	INIT[47]
1	1	0	0	0	0	INIT[48]
1	1	0	0	0	1	INIT[49]
1	1	0	0	1	0	INIT[50]
1	1	0	0	1	1	INIT[51]
1	1	0	1	0	0	INIT[52]
1	1	0	1	0	1	INIT[53]
1	1	0	1	1	0	INIT[54]
1	1	0	1	1	1	INIT[55]
1	1	1	0	0	0	INIT[56]
1	1	1	0	0	1	INIT[57]
1	1	1	0	1	0	INIT[58]
1	1	1	0	1	1	INIT[59]
1	1	1	1	0	0	INIT[60]
1	1	1	1	0	1	INIT[61]
1	1	1	1	1	0	INIT[62]
1	1	1	1	1	1	INIT[63]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute						

Port Description

Name	Direction	Width	Function
O	Output	1	6/5-LUT output
I0, I1, I2, I3, I4, I5	Input	1	LUT inputs

Design Entry Method

Instantiation	Yes
Inference	Recommended
CORE Generator™ and wizards	No
Macro support	No

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 64-Bit Value	All zeros	Specifies the logic value for the look-up tables.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- LUT6: 6-input Look-Up Table with general output
--       7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

LUT6_inst : LUT6
generic map (
   INIT => X"0000000000000000") -- Specify LUT Contents
port map (
   O => O,  -- LUT general output
   I0 => I0,    -- LUT input
   I1 => I1,    -- LUT input
   I2 => I2,    -- LUT input
   I3 => I3,    -- LUT input
   I4 => I4,    -- LUT input
   I5 => I5     -- LUT input
);

-- End of LUT6_inst instantiation
```

Verilog Instantiation Template

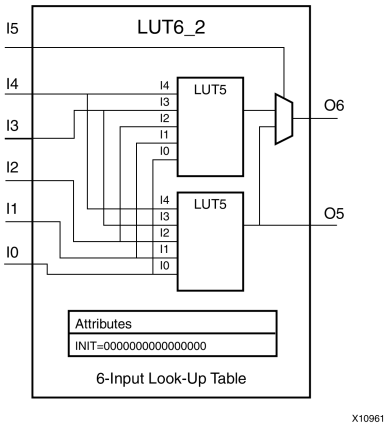
```
// LUT6: 6-input Look-Up Table with general output
//       7 Series
// Xilinx HDL Libraries Guide, version 2012.2

LUT6 #(
   .INIT(64'h0000000000000000)  // Specify LUT Contents
) LUT6_inst (
   .O(O),   // LUT general output
   .I0(I0), // LUT input
   .I1(I1), // LUT input
   .I2(I2), // LUT input
   .I3(I3), // LUT input
   .I4(I4), // LUT input
   .I5(I5)  // LUT input
);

// End of LUT6_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

LUT6_2

Primitive: Six-input, 2-output, Look-Up Table



Introduction

This design element is a 6-input, 2-output look-up table (LUT) that can either act as a dual asynchronous 32-bit ROM (with 5-bit addressing), implement any two 5-input logic functions with shared inputs, or implement a 6-input logic function and a 5-input logic function with shared inputs and shared logic values. LUTs are the basic logic building blocks and are used to implement most logic functions of the design. A LUT6_2 will be mapped to one of the four look-up tables in the slice.

An INIT attribute consisting of a 64-bit hexadecimal value must be specified to indicate the LUTs logical function. The INIT value is calculated by assigning a 1 to corresponding INIT bit value when the associated inputs are applied. For instance, a Verilog INIT value of 64'hfffffffffffffffe (X"FFFFFFFFFFFFFFFE" for VHDL) makes the O6 output 1 unless all zeros are on the inputs and the O5 output a 1, or unless I[4:0] are all zeroes (a 5-input and 6-input OR gate). The lower half (bits 31:0) of the INIT values apply to the logic function of the O5 output.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method: A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method: Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs						Outputs	
I5	I4	I3	I2	I1	I0	O5	O6
0	0	0	0	0	0	INIT[0]	INIT[0]
0	0	0	0	0	1	INIT[1]	INIT[1]
0	0	0	0	1	0	INIT[2]	INIT[2]
0	0	0	0	1	1	INIT[3]	INIT[3]
0	0	0	1	0	0	INIT[4]	INIT[4]
0	0	0	1	0	1	INIT[5]	INIT[5]
0	0	0	1	1	0	INIT[6]	INIT[6]
0	0	0	1	1	1	INIT[7]	INIT[7]
0	0	1	0	0	0	INIT[8]	INIT[8]
0	0	1	0	0	1	INIT[9]	INIT[9]
0	0	1	0	1	0	INIT[10]	INIT[10]
0	0	1	0	1	1	INIT[11]	INIT[11]
0	0	1	1	0	0	INIT[12]	INIT[12]
0	0	1	1	0	1	INIT[13]	INIT[13]
0	0	1	1	1	0	INIT[14]	INIT[14]
0	0	1	1	1	1	INIT[15]	INIT[15]
0	1	0	0	0	0	INIT[16]	INIT[16]
0	1	0	0	0	1	INIT[17]	INIT[17]
0	1	0	0	1	0	INIT[18]	INIT[18]
0	1	0	0	1	1	INIT[19]	INIT[19]
0	1	0	1	0	0	INIT[20]	INIT[20]
0	1	0	1	0	1	INIT[21]	INIT[21]
0	1	0	1	1	0	INIT[22]	INIT[22]
0	1	0	1	1	1	INIT[23]	INIT[23]
0	1	1	0	0	0	INIT[24]	INIT[24]
0	1	1	0	0	1	INIT[25]	INIT[25]
0	1	1	0	1	0	INIT[26]	INIT[26]
0	1	1	0	1	1	INIT[27]	INIT[27]
0	1	1	1	0	0	INIT[28]	INIT[28]
0	1	1	1	0	1	INIT[29]	INIT[29]
0	1	1	1	1	0	INIT[30]	INIT[30]
0	1	1	1	1	1	INIT[31]	INIT[31]
1	0	0	0	0	0	INIT[0]	INIT[32]
1	0	0	0	0	1	INIT[1]	INIT[33]

Inputs						Outputs	
1	0	0	0	1	0	INIT[2]	INIT[34]
1	0	0	0	1	1	INIT[3]	INIT[35]
1	0	0	1	0	0	INIT[4]	INIT[36]
1	0	0	1	0	1	INIT[5]	INIT[37]
1	0	0	1	1	0	INIT[6]	INIT[38]
1	0	0	1	1	1	INIT[7]	INIT[39]
1	0	1	0	0	0	INIT[8]	INIT[40]
1	0	1	0	0	1	INIT[9]	INIT[41]
1	0	1	0	1	0	INIT[10]	INIT[42]
1	0	1	0	1	1	INIT[11]	INIT[43]
1	0	1	1	0	0	INIT[12]	INIT[44]
1	0	1	1	0	1	INIT[13]	INIT[45]
1	0	1	1	1	0	INIT[14]	INIT[46]
1	0	1	1	1	1	INIT[15]	INIT[47]
1	1	0	0	0	0	INIT[16]	INIT[48]
1	1	0	0	0	1	INIT[17]	INIT[49]
1	1	0	0	1	0	INIT[18]	INIT[50]
1	1	0	0	1	1	INIT[19]	INIT[51]
1	1	0	1	0	0	INIT[20]	INIT[52]
1	1	0	1	0	1	INIT[21]	INIT[53]
1	1	0	1	1	0	INIT[22]	INIT[54]
1	1	0	1	1	1	INIT[23]	INIT[55]
1	1	1	0	0	0	INIT[24]	INIT[56]
1	1	1	0	0	1	INIT[25]	INIT[57]
1	1	1	0	1	0	INIT[26]	INIT[58]
1	1	1	0	1	1	INIT[27]	INIT[59]
1	1	1	1	0	0	INIT[28]	INIT[60]
1	1	1	1	0	1	INIT[29]	INIT[61]
1	1	1	1	1	0	INIT[30]	INIT[62]
1	1	1	1	1	1	INIT[31]	INIT[63]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute							

Port Descriptions

Port	Direction	Width	Function
O6	Output	1	6/5-LUT output
O5	Output	1	5-LUT output
I0, I1, I2, I3, I4, I5	Input	1	LUT inputs

Design Entry Method

Instantiation	Yes
Inference	Recommended
CORE Generator™ and wizards	No
Macro support	No

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 64-Bit Value	All zeros	Specifies the LUT5/6 output function.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- LUT6_2: 6-input  2 output Look-Up Table
--         7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

LUT6_2_inst : LUT6_2
generic map (
   INIT => X"0000000000000000") -- Specify LUT Contents
port map (
   O6 => O6,  -- 6/5-LUT output (1-bit)
   O5 => O5,  -- 5-LUT output (1-bit)
   I0 => I0,   -- LUT input (1-bit)
   I1 => I1,   -- LUT input (1-bit)
   I2 => I2,   -- LUT input (1-bit)
   I3 => I3,   -- LUT input (1-bit)
   I4 => I4,   -- LUT input (1-bit)
   I5 => I5    -- LUT input (1-bit)
);

-- End of LUT6_2_inst instantiation
```

Verilog Instantiation Template

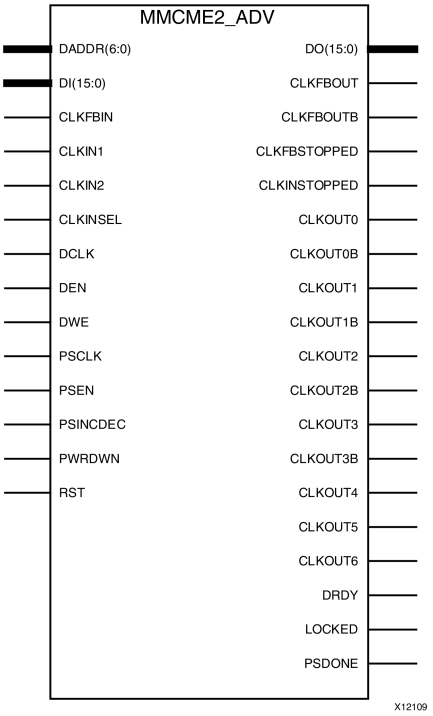
```
// LUT6_2: 6-input, 2 output Look-Up Table
//         7 Series
// Xilinx HDL Libraries Guide, version 2012.2

LUT6_2 #(
   .INIT(64'h0000000000000000) // Specify LUT Contents
) LUT6_2_inst (
   .O6(O6), // 1-bit LUT6 output
   .O5(O5), // 1-bit lower LUT5 output
   .I0(I0), // 1-bit LUT input
   .I1(I1), // 1-bit LUT input
   .I2(I2), // 1-bit LUT input
   .I3(I3), // 1-bit LUT input
   .I4(I4), // 1-bit LUT input
   .I5(I5)  // 1-bit LUT input (fast MUX select only available to O6 output)
);

// End of LUT6_2_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

MMCME2_ADV

Primitive: Advanced Mixed Mode Clock Manager



Introduction

The MMCME2 is a mixed signal block designed to support frequency synthesis, clock network deskew, and jitter reduction. The clock outputs can each have an individual divide, phase shift and duty cycle based on the same VCO frequency. Additionally, the MMCME2 supports dynamic phase shifting and fractional divides.

Port Descriptions

Port	Type	Width	Function
CLKFBIN	Input	1	Feedback clock pin to the MMCM
CLKFBOUT	Output	1	Dedicated MMCM Feedback clock output
CLKFBOUTB	Output	1	Inverted CLKFBOUT
CLKFBSTOPPED	Output	1	Status pin indicating that the feedback clock has stopped.
CLKINSEL	Input	1	Signal controls the state of the input MUX, High = CLKIN1, Low = CLKIN2.
CLKINSTOPPED	Output	1	Status pin indicating that the input clock has stopped.
CLKIN1	Input	1	Primary clock input.

Port	Type	Width	Function
CLKIN2	Input	1	Secondary clock input to dynamically switch the MMCM reference clock.
CLKOUT0	Output	1	CLKOUT0 output
CLKOUT0B	Output	1	Inverted CLKOUT0 output
CLKOUT1	Output	1	CLKOUT1 output
CLKOUT1B	Output	1	Inverted CLKOUT1 output
CLKOUT2	Output	1	CLKOUT2 output
CLKOUT2B	Output	1	Inverted CLKOUT2 output
CLKOUT3	Output	1	CLKOUT3 output
CLKOUT3B	Output	1	Inverted CLKOUT3 output
CLKOUT4	Output	1	CLKOUT4 output
CLKOUT5	Output	1	CLKOUT5 output
CLKOUT6	Output	1	CLKOUT6 output
DADDR<6:0>	Input	7	The dynamic reconfiguration address (DADDR) input bus provides a reconfiguration address for the dynamic reconfiguration. When not used, all bits must be assigned zeros.
DCLK	Input	1	The DCLK signal is the reference clock for the dynamic reconfiguration port.
DEN	Input	1	The dynamic reconfiguration enable (DEN) provides the enable control signal to access the dynamic reconfiguration feature. When the dynamic reconfiguration feature is not used, DEN must be tied Low.
DI<15:0>	Input	16	The dynamic reconfiguration data input (DI) bus provides reconfiguration data. When not used, all bits must be set to zero.
DO<15:0>	Output	16	The dynamic reconfiguration output bus provides MMCM data output when using dynamic reconfiguration.
DRDY	Output	1	The dynamic reconfiguration ready output (DRDY) provides the response to the DEN signal for the MMCMs dynamic reconfiguration feature.
DWE	Input	1	The dynamic reconfiguration write enable (DWE) input pin provides the write enable control signal to write the DI data into the DADDR address. When not used, it must be tied Low.
LOCKED	Output	1	An output from the MMCM that indicates when the MMCM has achieved phase alignment within a predefined window and frequency matching within a predefined PPM range. The MMCM automatically locks after power on, no extra reset is required. LOCKED will be deasserted if the input clock stops or the phase alignment is violated (e.g., input clock phase shift). The MMCM automatically reacquires lock after LOCKED is deasserted.
PSCLK	Input	1	Phase shift clock.
PSDONE	Output	1	Phase shift done.
PSEN	Input	1	Phase shift enable

Port	Type	Width	Function
PSINCDEC	Input	1	Phase shift increment/decrement control.
PWRDWN	Input	1	Powers down instantiated but unused MMCMs.
RST	Input	1	Asynchronous reset signal. The MMCM will synchronously re-enable itself when this signal is released (i.e., MMCM re-enabled). A reset is required when the input clock conditions change (e.g., frequency).

Design Entry Method

Instantiation	Yes
Inference	No
CORE Generator™ and wizards	Recommended
Macro support	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
BANDWIDTH	STRING	"OPTIMIZED", "HIGH", "LOW"	"OPTIMIZED"	Specifies the MMCM programming algorithm affecting the jitter, phase margin and other characteristics of the MMCM.
CLKFBOUT_MULT_F	3 significant digit FLOAT	2.000 to 64.000	5.000	Specifies the amount to multiply all CLKOUT clock outputs if a different frequency is desired. This number, in combination with the associated CLKOUT#_DIVIDE value and DIVCLK_DIVIDE value, will determine the output frequency.
CLKFBOUT_PHASE	3 significant digit FLOAT	-360.000 to 360.000	0.000	Specifies the phase offset in degrees of the clock feedback output. Shifting the feedback clock results in a negative phase shift of all output clocks to the MMCM.
CLKIN1_PERIOD, CLKIN2_PERIOD	FLOAT(nS)	0.000 to 100.000	0.000	Specifies the input period in ns to the MMCM CLKIN inputs. Resolution is down to the ps. For exmaple a value of 33.333 would indicate a 30 MHz input clock. This information is mandatory and must be supplied. CLKIN1_PERIOD relates to the input period on the CLKIN1 input while CLKIN2_PERIOD relates to the input clock period on the CLKIN2 input.

Attribute	Type	Allowed Values	Default	Description
CLKOUT1 _DIVIDE, CLKOUT2 _DIVIDE, CLKOUT3 _DIVIDE, CLKOUT4 _DIVIDE, CLKOUT5 _DIVIDE, CLKOUT6 _DIVIDE	DECIMAL	1 to 128	1	Specifies the amount to divide the associated CLKOUT clock output if a different frequency is desired. This number in combination with the CLKFBOUT_MULT_F and DIVCLK_DIVIDE values will determine the output frequency.
CLKOUT0 _DIVIDE_F	3 significant digit FLOAT	1.000 to 128.000	1.000	Specifies the amount to divide the associated CLKOUT clock output if a different frequency is desired. This number in combination with the CLKFBOUT_MULT_F and DIVCLK_DIVIDE values will determine the output frequency.
CLKOUT0_DUTY _CYCLE to CLKOUT6_DUTY _CYCLE	3 significant digit FLOAT	0.001 to 0.999	0.500	Specifies the Duty Cycle of the associated CLKOUT clock output in percentage (i.e., 0.50 will generate a 50% duty cycle).
CLKOUT0 _PHASE to CLKOUT6 _PHASE	3 significant digit FLOAT	-360.000 to 360.000	0.000	Specifies the phase offset in degrees of the clock feedback output. Shifting the feedback clock results in a negative phase shift of all output clocks to the MMCM.
CLKOUT4 _CASCADE	BOOLEAN	FALSE, TRUE	FALSE	Cascades the output divider (counter) into the input of the CLKOUT4 divider for an output clock divider that is greater than 128.
COMPENSATION	STRING	"ZHOLD", "BUF_IN", "EXTERNAL", "INTERNAL"	"ZHOLD"	Clock input compensation. Should be set to ZHOLD. Defines how the MMCM feedback is configured. • "ZHOLD" - MMCM is configured to provide a negative hold time at the I/O registers. • "INTERNAL" - MMCM is using its own internal feedback path so no delay is being compensated. • "EXTERNAL" - a network external to the FPGA is being compensated. • "BUF_IN" - configuration does not match with the other compensation modes and no delay will be compensated. This is the case if a clock

Attribute	Type	Allowed Values	Default	Description
				input is driven by a BUFG/BUFH/BUFR/GT.
DIVCLK _DIVIDE	DECIMAL	1 to 106	1	Specifies the division ratio for all output clocks with respect to the input clock. Effectively divides the CLKIN going into the PFD.
REF_JITTER1, REF_JITTER2	3 significant digit FLOAT	0.000 to 0.999	0.010	Allows specification of the expected jitter on the CLKIN inputs in order to better optimize MMCM performance. A bandwidth setting of OPTIMIZED will attempt to choose the best parameter for input clocking when unknown. If known, then the value provided should be specified in terms of the UI percentage (the maximum peak to peak value) of the expected jitter on the input clock. REF_JITTER1 relates to the input jitter on CLKIN1 while REF_JITTER2 relates to the input jitter on CLKIN2.
SS_EN	STRING	"FALSE", "TRUE"	"FALSE"	Enables the spread spectrum feature for the MMCM. Used in conjunction with SS_MODE and SS_MOD_PERIOD attributes.
SS_MOD _PERIOD	DECIMAL(nS)	4000 to 40000	10000	Specifies the spread spectrum modulation period (ns).
SS_MODE	STRING	"CENTER_HIGH", "CENTER_LOW", "DOWN_HIGH", "DOWN_LOW"	"CENTER_HIGH"	Controls the spread spectrum frequency deviation and the spread type.
STARTUP_WAIT	BOOLEAN	FALSE, TRUE	FALSE	Delays configuration DONE signal from asserting until MMCM is locked.
CLKFBOUT_USE _FINE_PS to CLKOUT6_USE _FINE_PS	BOOLEAN	FALSE, TRUE	FALSE	Counter variable fine phase shift enable.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- MMCME2_ADV: Advanced Mixed Mode Clock Manager
--             7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

MMCME2_ADV_inst : MMCME2_ADV
generic map (
   BANDWIDTH => "OPTIMIZED",      -- Jitter programming (OPTIMIZED, HIGH, LOW)
```

```
   CLKFBOUT_MULT_F => 5.0,        -- Multiply value for all CLKOUT (2.000-64.000).
   CLKFBOUT_PHASE => 0.0,         -- Phase offset in degrees of CLKFB (-360.000-360.000).
   -- CLKIN_PERIOD: Input clock period in ns to ps resolution (i.e. 33.333 is 30 MHz).
   CLKIN1_PERIOD => 0.0,
   CLKIN2_PERIOD => 0.0,
   -- CLKOUT0_DIVIDE - CLKOUT6_DIVIDE: Divide amount for CLKOUT (1-128)
   CLKOUT1_DIVIDE => 1,
   CLKOUT2_DIVIDE => 1,
   CLKOUT3_DIVIDE => 1,
   CLKOUT4_DIVIDE => 1,
   CLKOUT5_DIVIDE => 1,
   CLKOUT6_DIVIDE => 1,
   CLKOUT0_DIVIDE_F => 1.0,       -- Divide amount for CLKOUT0 (1.000-128.000).
   -- CLKOUT0_DUTY_CYCLE - CLKOUT6_DUTY_CYCLE: Duty cycle for CLKOUT outputs (0.01-0.99).
   CLKOUT0_DUTY_CYCLE => 0.5,
   CLKOUT1_DUTY_CYCLE => 0.5,
   CLKOUT2_DUTY_CYCLE => 0.5,
   CLKOUT3_DUTY_CYCLE => 0.5,
   CLKOUT4_DUTY_CYCLE => 0.5,
   CLKOUT5_DUTY_CYCLE => 0.5,
   CLKOUT6_DUTY_CYCLE => 0.5,
   -- CLKOUT0_PHASE - CLKOUT6_PHASE: Phase offset for CLKOUT outputs (-360.000-360.000).
   CLKOUT0_PHASE => 0.0,
   CLKOUT1_PHASE => 0.0,
   CLKOUT2_PHASE => 0.0,
   CLKOUT3_PHASE => 0.0,
   CLKOUT4_PHASE => 0.0,
   CLKOUT5_PHASE => 0.0,
   CLKOUT6_PHASE => 0.0,
   CLKOUT4_CASCADE => FALSE,      -- Cascade CLKOUT4 counter with CLKOUT6 (FALSE, TRUE)
   COMPENSATION => "ZHOLD",       -- ZHOLD, BUF_IN, EXTERNAL, INTERNAL
   DIVCLK_DIVIDE => 1,            -- Master division value (1-106)
   -- REF_JITTER: Reference input jitter in UI (0.000-0.999).
   REF_JITTER1 => 0.0,
   REF_JITTER2 => 0.0,
   STARTUP_WAIT => FALSE,         -- Delays DONE until MMCM is locked (FALSE, TRUE)
   -- Spread Spectrum: Spread Spectrum Attributes
   SS_EN => "FALSE",              -- Enables spread spectrum (FALSE, TRUE)
   SS_MODE => "CENTER_HIGH",      -- CENTER_HIGH, CENTER_LOW, DOWN_HIGH, DOWN_LOW
   SS_MOD_PERIOD => 10000,        -- Spread spectrum modulation period (ns) (VALUES)
   -- USE_FINE_PS: Fine phase shift enable (TRUE/FALSE)
   CLKFBOUT_USE_FINE_PS => FALSE,
   CLKOUT0_USE_FINE_PS => FALSE,
   CLKOUT1_USE_FINE_PS => FALSE,
   CLKOUT2_USE_FINE_PS => FALSE,
   CLKOUT3_USE_FINE_PS => FALSE,
   CLKOUT4_USE_FINE_PS => FALSE,
   CLKOUT5_USE_FINE_PS => FALSE,
   CLKOUT6_USE_FINE_PS => FALSE
)
port map (
   -- Clock Outputs: 1-bit (each) output: User configurable clock outputs
   CLKOUT0 => CLKOUT0,            -- 1-bit output: CLKOUT0
   CLKOUT0B => CLKOUT0B,          -- 1-bit output: Inverted CLKOUT0
   CLKOUT1 => CLKOUT1,            -- 1-bit output: CLKOUT1
   CLKOUT1B => CLKOUT1B,          -- 1-bit output: Inverted CLKOUT1
   CLKOUT2 => CLKOUT2,            -- 1-bit output: CLKOUT2
   CLKOUT2B => CLKOUT2B,          -- 1-bit output: Inverted CLKOUT2
   CLKOUT3 => CLKOUT3,            -- 1-bit output: CLKOUT3
   CLKOUT3B => CLKOUT3B,          -- 1-bit output: Inverted CLKOUT3
   CLKOUT4 => CLKOUT4,            -- 1-bit output: CLKOUT4
   CLKOUT5 => CLKOUT5,            -- 1-bit output: CLKOUT5
   CLKOUT6 => CLKOUT6,            -- 1-bit output: CLKOUT6
   -- DRP Ports: 16-bit (each) output: Dynamic reconfiguration ports
   DO => DO,                      -- 16-bit output: DRP data
   DRDY => DRDY,                  -- 1-bit output: DRP ready
   -- Dynamic Phase Shift Ports: 1-bit (each) output: Ports used for dynamic phase shifting of the outputs
   PSDONE => PSDONE,              -- 1-bit output: Phase shift done
   -- Feedback Clocks: 1-bit (each) output: Clock feedback ports
   CLKFBOUT => CLKFBOUT,          -- 1-bit output: Feedback clock
   CLKFBOUTB => CLKFBOUTB,        -- 1-bit output: Inverted CLKFBOUT
   -- Status Ports: 1-bit (each) output: MMCM status ports
```

```
   CLKFBSTOPPED => CLKFBSTOPPED, -- 1-bit output: Feedback clock stopped
   CLKINSTOPPED => CLKINSTOPPED, -- 1-bit output: Input clock stopped
   LOCKED => LOCKED,             -- 1-bit output: LOCK
   -- Clock Inputs: 1-bit (each) input: Clock inputs
   CLKIN1 => CLKIN1,             -- 1-bit input: Primary clock
   CLKIN2 => CLKIN2,             -- 1-bit input: Secondary clock
   -- Control Ports: 1-bit (each) input: MMCM control ports
   CLKINSEL => CLKINSEL,         -- 1-bit input: Clock select, High=CLKIN1 Low=CLKIN2
   PWRDWN => PWRDWN,             -- 1-bit input: Power-down
   RST => RST,                   -- 1-bit input: Reset
   -- DRP Ports: 7-bit (each) input: Dynamic reconfiguration ports
   DADDR => DADDR,               -- 7-bit input: DRP address
   DCLK => DCLK,                 -- 1-bit input: DRP clock
   DEN => DEN,                   -- 1-bit input: DRP enable
   DI => DI,                     -- 16-bit input: DRP data
   DWE => DWE,                   -- 1-bit input: DRP write enable
   -- Dynamic Phase Shift Ports: 1-bit (each) input: Ports used for dynamic phase shifting of the outputs
   PSCLK => PSCLK,               -- 1-bit input: Phase shift clock
   PSEN => PSEN,                 -- 1-bit input: Phase shift enable
   PSINCDEC => PSINCDEC,         -- 1-bit input: Phase shift increment/decrement
   -- Feedback Clocks: 1-bit (each) input: Clock feedback ports
   CLKFBIN => CLKFBIN            -- 1-bit input: Feedback clock
);

-- End of MMCME2_ADV_inst instantiation
```

Verilog Instantiation Template

```
// MMCME2_ADV: Advanced Mixed Mode Clock Manager
//             7 Series
// Xilinx HDL Libraries Guide, version 2012.2

MMCME2_ADV #(
   .BANDWIDTH("OPTIMIZED"),        // Jitter programming (OPTIMIZED, HIGH, LOW)
   .CLKFBOUT_MULT_F(5.0),          // Multiply value for all CLKOUT (2.000-64.000).
   .CLKFBOUT_PHASE(0.0),           // Phase offset in degrees of CLKFB (-360.000-360.000).
   // CLKIN_PERIOD: Input clock period in ns to ps resolution (i.e. 33.333 is 30 MHz).
   .CLKIN1_PERIOD(0.0),
   .CLKIN2_PERIOD(0.0),
   // CLKOUT0_DIVIDE - CLKOUT6_DIVIDE: Divide amount for CLKOUT (1-128)
   .CLKOUT1_DIVIDE(1),
   .CLKOUT2_DIVIDE(1),
   .CLKOUT3_DIVIDE(1),
   .CLKOUT4_DIVIDE(1),
   .CLKOUT5_DIVIDE(1),
   .CLKOUT6_DIVIDE(1),
   .CLKOUT0_DIVIDE_F(1.0),         // Divide amount for CLKOUT0 (1.000-128.000).
   // CLKOUT0_DUTY_CYCLE - CLKOUT6_DUTY_CYCLE: Duty cycle for CLKOUT outputs (0.01-0.99).
   .CLKOUT0_DUTY_CYCLE(0.5),
   .CLKOUT1_DUTY_CYCLE(0.5),
   .CLKOUT2_DUTY_CYCLE(0.5),
   .CLKOUT3_DUTY_CYCLE(0.5),
   .CLKOUT4_DUTY_CYCLE(0.5),
   .CLKOUT5_DUTY_CYCLE(0.5),
   .CLKOUT6_DUTY_CYCLE(0.5),
   // CLKOUT0_PHASE - CLKOUT6_PHASE: Phase offset for CLKOUT outputs (-360.000-360.000).
   .CLKOUT0_PHASE(0.0),
   .CLKOUT1_PHASE(0.0),
   .CLKOUT2_PHASE(0.0),
   .CLKOUT3_PHASE(0.0),
   .CLKOUT4_PHASE(0.0),
   .CLKOUT5_PHASE(0.0),
   .CLKOUT6_PHASE(0.0),
   .CLKOUT4_CASCADE("FALSE"),      // Cascade CLKOUT4 counter with CLKOUT6 (FALSE, TRUE)
   .COMPENSATION("ZHOLD"),         // ZHOLD, BUF_IN, EXTERNAL, INTERNAL
   .DIVCLK_DIVIDE(1),              // Master division value (1-106)
   // REF_JITTER: Reference input jitter in UI (0.000-0.999).
   .REF_JITTER1(0.0),
   .REF_JITTER2(0.0),
   .STARTUP_WAIT("FALSE"),         // Delays DONE until MMCM is locked (FALSE, TRUE)
```

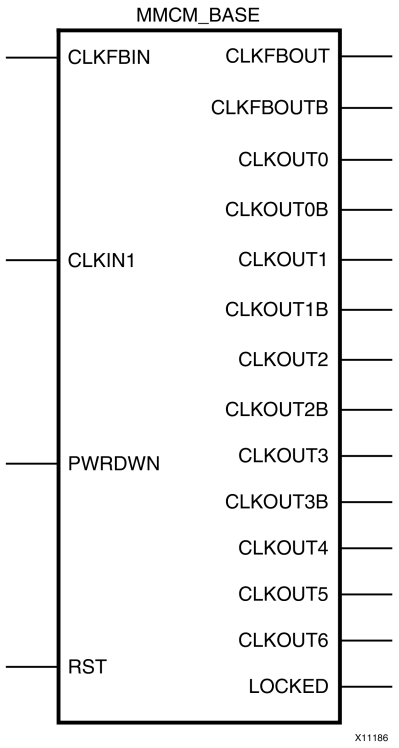
```
   // Spread Spectrum: Spread Spectrum Attributes
   .SS_EN("FALSE"),                // Enables spread spectrum (FALSE, TRUE)
   .SS_MODE("CENTER_HIGH"),        // CENTER_HIGH, CENTER_LOW, DOWN_HIGH, DOWN_LOW
   .SS_MOD_PERIOD(10000),          // Spread spectrum modulation period (ns) (VALUES)
   // USE_FINE_PS: Fine phase shift enable (TRUE/FALSE)
   .CLKFBOUT_USE_FINE_PS("FALSE"),
   .CLKOUT0_USE_FINE_PS("FALSE"),
   .CLKOUT1_USE_FINE_PS("FALSE"),
   .CLKOUT2_USE_FINE_PS("FALSE"),
   .CLKOUT3_USE_FINE_PS("FALSE"),
   .CLKOUT4_USE_FINE_PS("FALSE"),
   .CLKOUT5_USE_FINE_PS("FALSE"),
   .CLKOUT6_USE_FINE_PS("FALSE")
)
MMCME2_ADV_inst (
   // Clock Outputs: 1-bit (each) output: User configurable clock outputs
   .CLKOUT0(CLKOUT0),            // 1-bit output: CLKOUT0
   .CLKOUT0B(CLKOUT0B),          // 1-bit output: Inverted CLKOUT0
   .CLKOUT1(CLKOUT1),            // 1-bit output: CLKOUT1
   .CLKOUT1B(CLKOUT1B),          // 1-bit output: Inverted CLKOUT1
   .CLKOUT2(CLKOUT2),            // 1-bit output: CLKOUT2
   .CLKOUT2B(CLKOUT2B),          // 1-bit output: Inverted CLKOUT2
   .CLKOUT3(CLKOUT3),            // 1-bit output: CLKOUT3
   .CLKOUT3B(CLKOUT3B),          // 1-bit output: Inverted CLKOUT3
   .CLKOUT4(CLKOUT4),            // 1-bit output: CLKOUT4
   .CLKOUT5(CLKOUT5),            // 1-bit output: CLKOUT5
   .CLKOUT6(CLKOUT6),            // 1-bit output: CLKOUT6
   // DRP Ports: 16-bit (each) output: Dynamic reconfiguration ports
   .DO(DO),                      // 16-bit output: DRP data
   .DRDY(DRDY),                  // 1-bit output: DRP ready
   // Dynamic Phase Shift Ports: 1-bit (each) output: Ports used for dynamic phase shifting of the outputs
   .PSDONE(PSDONE),              // 1-bit output: Phase shift done
   // Feedback Clocks: 1-bit (each) output: Clock feedback ports
   .CLKFBOUT(CLKFBOUT),          // 1-bit output: Feedback clock
   .CLKFBOUTB(CLKFBOUTB),        // 1-bit output: Inverted CLKFBOUT
   // Status Ports: 1-bit (each) output: MMCM status ports
   .CLKFBSTOPPED(CLKFBSTOPPED), // 1-bit output: Feedback clock stopped
   .CLKINSTOPPED(CLKINSTOPPED), // 1-bit output: Input clock stopped
   .LOCKED(LOCKED),              // 1-bit output: LOCK
   // Clock Inputs: 1-bit (each) input: Clock inputs
   .CLKIN1(CLKIN1),              // 1-bit input: Primary clock
   .CLKIN2(CLKIN2),              // 1-bit input: Secondary clock
   // Control Ports: 1-bit (each) input: MMCM control ports
   .CLKINSEL(CLKINSEL),          // 1-bit input: Clock select, High=CLKIN1 Low=CLKIN2
   .PWRDWN(PWRDWN),              // 1-bit input: Power-down
   .RST(RST),                    // 1-bit input: Reset
   // DRP Ports: 7-bit (each) input: Dynamic reconfiguration ports
   .DADDR(DADDR),                // 7-bit input: DRP address
   .DCLK(DCLK),                  // 1-bit input: DRP clock
   .DEN(DEN),                    // 1-bit input: DRP enable
   .DI(DI),                      // 16-bit input: DRP data
   .DWE(DWE),                    // 1-bit input: DRP write enable
   // Dynamic Phase Shift Ports: 1-bit (each) input: Ports used for dynamic phase shifting of the outputs
   .PSCLK(PSCLK),                // 1-bit input: Phase shift clock
   .PSEN(PSEN),                  // 1-bit input: Phase shift enable
   .PSINCDEC(PSINCDEC),          // 1-bit input: Phase shift increment/decrement
   // Feedback Clocks: 1-bit (each) input: Clock feedback ports
   .CLKFBIN(CLKFBIN)             // 1-bit input: Feedback clock
);

// End of MMCME2_ADV_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

MMCME2_BASE

Primitive: Base Mixed Mode Clock Manager



Introduction

The MMCME2 is a mixed signal block designed to support frequency synthesis, clock network deskew, and jitter reduction. The clock outputs can each have an individual divide, phase shift and duty cycle based on the same VCO frequency. Additionally, the MMCME2 supports dynamic phase shifting and fractional divides.

Port Descriptions

Port	Type	Width	Function
CLKFBIN	Input	1	Feedback clock pin to the MMCM
CLKFBOUT	Output	1	Dedicated MMCM Feedback clock output
CLKFBOUTB	Output	1	Inverted CLKFBOUT output
CLKOUT0	Output	1	CLKOUT0 output
CLKOUT0B	Output	1	Inverted CLKOUT0 output
CLKOUT1	Output	1	CLKOUT1 output
CLKOUT1B	Output	1	Inverted CLKOUT1 output

Port	Type	Width	Function
CLKOUT2	Output	1	CLKOUT2 output
CLKOUT2B	Output	1	Inverted CLKOUT2 output
CLKOUT3	Output	1	CLKOUT3 output
CLKOUT3B	Output	1	Inverted CLKOUT3 output
CLKOUT4	Output	1	CLKOUT4 output
CLKOUT5	Output	1	CLKOUT5 output
CLKOUT6	Output	1	CLKOUT6 output
Clock Inputs	Input	1	General clock input.
PWRDWN	Input	1	Powers down instantiated but unused MMCMs.
RST	Input	1	Asynchronous reset signal. The MMCM will synchronously re-enable itself when this signal is released (i.e., MMCM re-enabled). A reset is required when the input clock conditions change (e.g., frequency).
Status Ports	Output	1	An output from the MMCM that indicates when the MMCM has achieved phase alignment within a predefined window and frequency matching within a predefined PPM range. The MMCM automatically locks after power on, no extra reset is required. LOCKED will be deasserted if the input clock stops or the phase alignment is violated (e.g., input clock phase shift). The MMCM automatically reacquires lock after LOCKED is deasserted.

Design Entry Method

Instantiation	Yes
Inference	No
CORE Generator™ and wizards	Recommended
Macro support	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
BANDWIDTH	STRING	"OPTIMIZED", "HIGH", "LOW"	"OPTIMIZED"	Specifies the MMCM programming algorithm affecting the jitter, phase margin and other characteristics of the MMCM.
CLKFBOUT_MULT _F	3 significant digit FLOAT	2.000 to 64.000	5.000	Specifies the amount to multiply all CLKOUT clock outputs if a different frequency is desired. This number, in combination with the associated CLKOUT#_DIVIDE value and DIVCLK_DIVIDE value, will determine the output frequency.

Attribute	Type	Allowed Values	Default	Description
CLKFBOUT _PHASE	3 significant digit FLOAT	-360.000 to 360.000	0.000	Specifies the phase offset in degrees of the clock feedback output. Shifting the feedback clock results in a negative phase shift of all output clocks to the MMCM.
CLKIN1 _PERIOD	FLOAT(nS)	0.000 to 100.000	0.000	Specifies the input period in ns to the MMCM CLKIN1 input. Resolution is down to the ps (3 decimal places). For example, a value of 33.333 would indicate a 30 MHz input clock. This information is mandatory and must be supplied.
CLKOUT1 _DIVIDE, CLKOUT2 _DIVIDE, CLKOUT3 _DIVIDE, CLKOUT4 _DIVIDE, CLKOUT5 _DIVIDE, CLKOUT6 _DIVIDE	DECIMAL	1 to 128	1	Specifies the amount to divide the associated CLKOUT clock output if a different frequency is desired. This number in combination with the CLKFBOUT_MULT_F and DIVCLK_DIVIDE values will determine the output frequency.
CLKOUT0 _DIVIDE_F	3 significant digit FLOAT	1.000 to 128.000	1.000	Specifies the amount to divide the associated CLKOUT clock output if a different frequency is desired. This number in combination with the CLKFBOUT_MULT_F and DIVCLK_DIVIDE values will determine the output frequency.
CLKOUT0_DUTY _CYCLE to CLKOUT6_DUTY _CYCLE	3 significant digit FLOAT	0.001 to 0.999	0.500	Specifies the Duty Cycle of the associated CLKOUT clock output in percentage (i.e., 0.50 will generate a 50% duty cycle).
CLKOUT0 _PHASE to CLKOUT6 _PHASE	3 significant digit FLOAT	-360.000 to 360.000	0.000	Specifies the phase offset in degrees of the clock feedback output. Shifting the feedback clock results in a negative phase shift of all output clocks to the MMCM.
CLKOUT4 _CASCADE	BOOLEAN	FALSE, TRUE	FALSE	Cascades the output divider (counter) CLKOUT6 into the input of the CLKOUT4 divider for an output clock divider that is greater than 128.
DIVCLK _DIVIDE	DECIMAL	1 to 106	1	Specifies the division ratio for all output clocks with respect to the input clock. Effectively divides the CLKIN going into the PFD.

Attribute	Type	Allowed Values	Default	Description
REF_JITTER1	3 significant digit FLOAT	0.000 to 0.999	0.010	Allows specification of the expected jitter on CLKIN1 in order to better optimize MMCM performance. A bandwidth setting of OPTIMIZED will attempt to choose the best parameter for input clocking when unknown. If known, then the value provided should be specified in terms of the UI percentage (the maximum peak to peak value) of the expected jitter on the input clock.
STARTUP_WAIT	BOOLEAN	FALSE, TRUE	FALSE	Delays configuration DONE signal from asserting until MMCM is locked.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- MMCME2_BASE: Base Mixed Mode Clock Manager
--              7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

MMCME2_BASE_inst : MMCME2_BASE
generic map (
   BANDWIDTH => "OPTIMIZED",  -- Jitter programming (OPTIMIZED, HIGH, LOW)
   CLKFBOUT_MULT_F => 5.0,    -- Multiply value for all CLKOUT (2.000-64.000).
   CLKFBOUT_PHASE => 0.0,     -- Phase offset in degrees of CLKFB (-360.000-360.000).
   CLKIN1_PERIOD => 0.0,      -- Input clock period in ns to ps resolution (i.e. 33.333 is 30 MHz).
   -- CLKOUT0_DIVIDE - CLKOUT6_DIVIDE: Divide amount for each CLKOUT (1-128)
   CLKOUT1_DIVIDE => 1,
   CLKOUT2_DIVIDE => 1,
   CLKOUT3_DIVIDE => 1,
   CLKOUT4_DIVIDE => 1,
   CLKOUT5_DIVIDE => 1,
   CLKOUT6_DIVIDE => 1,
   CLKOUT0_DIVIDE_F => 1.0,   -- Divide amount for CLKOUT0 (1.000-128.000).
   -- CLKOUT0_DUTY_CYCLE - CLKOUT6_DUTY_CYCLE: Duty cycle for each CLKOUT (0.01-0.99).
   CLKOUT0_DUTY_CYCLE => 0.5,
   CLKOUT1_DUTY_CYCLE => 0.5,
   CLKOUT2_DUTY_CYCLE => 0.5,
   CLKOUT3_DUTY_CYCLE => 0.5,
   CLKOUT4_DUTY_CYCLE => 0.5,
   CLKOUT5_DUTY_CYCLE => 0.5,
   CLKOUT6_DUTY_CYCLE => 0.5,
   -- CLKOUT0_PHASE - CLKOUT6_PHASE: Phase offset for each CLKOUT (-360.000-360.000).
   CLKOUT0_PHASE => 0.0,
   CLKOUT1_PHASE => 0.0,
   CLKOUT2_PHASE => 0.0,
   CLKOUT3_PHASE => 0.0,
   CLKOUT4_PHASE => 0.0,
   CLKOUT5_PHASE => 0.0,
   CLKOUT6_PHASE => 0.0,
   CLKOUT4_CASCADE => FALSE,  -- Cascade CLKOUT4 counter with CLKOUT6 (FALSE, TRUE)
   DIVCLK_DIVIDE => 1,        -- Master division value (1-106)
   REF_JITTER1 => 0.0,        -- Reference input jitter in UI (0.000-0.999).
   STARTUP_WAIT => FALSE      -- Delays DONE until MMCM is locked (FALSE, TRUE)
)
port map (
   -- Clock Outputs: 1-bit (each) output: User configurable clock outputs
```

```
   CLKOUT0 => CLKOUT0,      -- 1-bit output: CLKOUT0
   CLKOUT0B => CLKOUT0B,    -- 1-bit output: Inverted CLKOUT0
   CLKOUT1 => CLKOUT1,      -- 1-bit output: CLKOUT1
   CLKOUT1B => CLKOUT1B,    -- 1-bit output: Inverted CLKOUT1
   CLKOUT2 => CLKOUT2,      -- 1-bit output: CLKOUT2
   CLKOUT2B => CLKOUT2B,    -- 1-bit output: Inverted CLKOUT2
   CLKOUT3 => CLKOUT3,      -- 1-bit output: CLKOUT3
   CLKOUT3B => CLKOUT3B,    -- 1-bit output: Inverted CLKOUT3
   CLKOUT4 => CLKOUT4,      -- 1-bit output: CLKOUT4
   CLKOUT5 => CLKOUT5,      -- 1-bit output: CLKOUT5
   CLKOUT6 => CLKOUT6,      -- 1-bit output: CLKOUT6
   -- Feedback Clocks: 1-bit (each) output: Clock feedback ports
   CLKFBOUT => CLKFBOUT,    -- 1-bit output: Feedback clock
   CLKFBOUTB => CLKFBOUTB, -- 1-bit output: Inverted CLKFBOUT
   -- Status Ports: 1-bit (each) output: MMCM status ports
   LOCKED => LOCKED,        -- 1-bit output: LOCK
   -- Clock Inputs: 1-bit (each) input: Clock input
   CLKIN1 => CLKIN1,        -- 1-bit input: Clock
   -- Control Ports: 1-bit (each) input: MMCM control ports
   PWRDWN => PWRDWN,        -- 1-bit input: Power-down
   RST => RST,              -- 1-bit input: Reset
   -- Feedback Clocks: 1-bit (each) input: Clock feedback ports
   CLKFBIN => CLKFBIN       -- 1-bit input: Feedback clock
);

-- End of MMCME2_BASE_inst instantiation
```

Verilog Instantiation Template

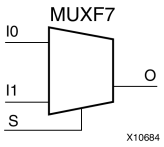
```
// MMCME2_BASE: Base Mixed Mode Clock Manager
//              7 Series
// Xilinx HDL Libraries Guide, version 2012.2

MMCME2_BASE #(
   .BANDWIDTH("OPTIMIZED"),   // Jitter programming (OPTIMIZED, HIGH, LOW)
   .CLKFBOUT_MULT_F(5.0),     // Multiply value for all CLKOUT (2.000-64.000).
   .CLKFBOUT_PHASE(0.0),      // Phase offset in degrees of CLKFB (-360.000-360.000).
   .CLKIN1_PERIOD(0.0),       // Input clock period in ns to ps resolution (i.e. 33.333 is 30 MHz).
   // CLKOUT0_DIVIDE - CLKOUT6_DIVIDE: Divide amount for each CLKOUT (1-128)
   .CLKOUT1_DIVIDE(1),
   .CLKOUT2_DIVIDE(1),
   .CLKOUT3_DIVIDE(1),
   .CLKOUT4_DIVIDE(1),
   .CLKOUT5_DIVIDE(1),
   .CLKOUT6_DIVIDE(1),
   .CLKOUT0_DIVIDE_F(1.0),    // Divide amount for CLKOUT0 (1.000-128.000).
   // CLKOUT0_DUTY_CYCLE - CLKOUT6_DUTY_CYCLE: Duty cycle for each CLKOUT (0.01-0.99).
   .CLKOUT0_DUTY_CYCLE(0.5),
   .CLKOUT1_DUTY_CYCLE(0.5),
   .CLKOUT2_DUTY_CYCLE(0.5),
   .CLKOUT3_DUTY_CYCLE(0.5),
   .CLKOUT4_DUTY_CYCLE(0.5),
   .CLKOUT5_DUTY_CYCLE(0.5),
   .CLKOUT6_DUTY_CYCLE(0.5),
   // CLKOUT0_PHASE - CLKOUT6_PHASE: Phase offset for each CLKOUT (-360.000-360.000).
   .CLKOUT0_PHASE(0.0),
   .CLKOUT1_PHASE(0.0),
   .CLKOUT2_PHASE(0.0),
   .CLKOUT3_PHASE(0.0),
   .CLKOUT4_PHASE(0.0),
   .CLKOUT5_PHASE(0.0),
   .CLKOUT6_PHASE(0.0),
   .CLKOUT4_CASCADE("FALSE"), // Cascade CLKOUT4 counter with CLKOUT6 (FALSE, TRUE)
   .DIVCLK_DIVIDE(1),         // Master division value (1-106)
   .REF_JITTER1(0.0),         // Reference input jitter in UI (0.000-0.999).
   .STARTUP_WAIT("FALSE")     // Delays DONE until MMCM is locked (FALSE, TRUE)
)
MMCME2_BASE_inst (
   // Clock Outputs: 1-bit (each) output: User configurable clock outputs
   .CLKOUT0(CLKOUT0),     // 1-bit output: CLKOUT0
   .CLKOUT0B(CLKOUT0B),   // 1-bit output: Inverted CLKOUT0
   .CLKOUT1(CLKOUT1),     // 1-bit output: CLKOUT1
   .CLKOUT1B(CLKOUT1B),   // 1-bit output: Inverted CLKOUT1
   .CLKOUT2(CLKOUT2),     // 1-bit output: CLKOUT2
   .CLKOUT2B(CLKOUT2B),   // 1-bit output: Inverted CLKOUT2
   .CLKOUT3(CLKOUT3),     // 1-bit output: CLKOUT3
   .CLKOUT3B(CLKOUT3B),   // 1-bit output: Inverted CLKOUT3
   .CLKOUT4(CLKOUT4),     // 1-bit output: CLKOUT4
   .CLKOUT5(CLKOUT5),     // 1-bit output: CLKOUT5
   .CLKOUT6(CLKOUT6),     // 1-bit output: CLKOUT6
   // Feedback Clocks: 1-bit (each) output: Clock feedback ports
   .CLKFBOUT(CLKFBOUT),   // 1-bit output: Feedback clock
   .CLKFBOUTB(CLKFBOUTB), // 1-bit output: Inverted CLKFBOUT
   // Status Ports: 1-bit (each) output: MMCM status ports
   .LOCKED(LOCKED),       // 1-bit output: LOCK
   // Clock Inputs: 1-bit (each) input: Clock input
   .CLKIN1(CLKIN1),       // 1-bit input: Clock
   // Control Ports: 1-bit (each) input: MMCM control ports
   .PWRDWN(PWRDWN),       // 1-bit input: Power-down
   .RST(RST),             // 1-bit input: Reset
   // Feedback Clocks: 1-bit (each) input: Clock feedback ports
   .CLKFBIN(CLKFBIN)      // 1-bit input: Feedback clock
);

// End of MMCME2_BASE_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

MUXF7

Primitive: 2-to-1 Look-Up Table Multiplexer with General Output



Introduction

This design element is a two input multiplexer which, in combination with two LUT6 elements will let you create any 7-input function, an 8-to-1 multiplexer, or other logic functions up to 12-bits wide. Local outputs of the LUT6 element are connected to the I0 and I1 inputs of the MUXF7. The S input is driven from any internal net. When Low, S selects I0. When High, S selects I1.

The O output is a general interconnect.

The variants, "MUXF7_D" and "MUXF7_L", provide additional types of outputs that can be used by different timing models for more accurate pre-layout timing estimation.

Logic Table

Inputs			Outputs
S	**I0**	**I1**	**O**
0	I0	X	I0
1	X	I1	I1
X	0	0	0
X	1	1	1

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Output of MUX to general routing.
I0	Input	1	Input (tie to LUT6 LO out).
I1	Input	1	Input (tie to LUT6 LO out).
S	Input	1	Input select to MUX.

Design Entry Method

Instantiation	Yes
Inference	Recommended
CORE Generator™ and wizards	No
Macro support	No

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- MUXF7: CLB MUX to tie two LUT6's together with general output
--        7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

MUXF7_inst : MUXF7
port map (
   O => O,     -- Output of MUX to general routing
   I0 => I0,   -- Input (tie to LUT6 O6 pin)
   I1 => I1,   -- Input (tie to LUT6 O6 pin)
   S => S      -- Input select to MUX
);

-- End of MUXF7_inst instantiation
```

Verilog Instantiation Template

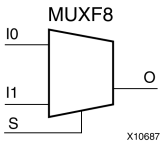
```
// MUXF7: CLB MUX to tie two LUT6's together with general output
//        7 Series
// Xilinx HDL Libraries Guide, version 2012.2

MUXF7 MUXF7_inst (
   .O(O),     // Output of MUX to general routing
   .I0(I0),   // Input (tie to LUT6 O6 pin)
   .I1(I1),   // Input (tie to LUT6 O6 pin)
   .S(S)      // Input select to MUX
);

// End of MUXF7_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

MUXF8

Primitive: 2-to-1 Look-Up Table Multiplexer with General Output



Introduction

This design element is a two input multiplexer which, in combination with two MUXF7 multiplexers and their four associated LUT6 elements, will let you create any 8-input function, a 16-to-1 multiplexer, or other logic functions up to 24-bits wide. Local outputs of MUXF7 are connected to the I0 and I1 inputs of the MUXF8. The S input is driven from any internal net. When Low, S selects I0. When High, S selects I1.

The O output is a general interconnect.

The variants, "MUXF8_D" and "MUXF8_L", provide additional types of outputs that can be used by different timing models for more accurate pre-layout timing estimation.

Logic Table

Inputs			Outputs
S	**I0**	**I1**	**O**
0	I0	X	I0
1	X	I1	I1
X	0	0	0
X	1	1	1

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Output of MUX to general routing
I0	Input	1	Input (tie to MUXF7 LO out)
I1	Input	1	Input (tie to MUXF7 LO out)
S	Input	1	Input select to MUX

Design Entry Method

Instantiation	Yes
Inference	Recommended
CORE Generator™ and wizards	No
Macro support	No

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- MUXF8: CLB MUX to tie two MUXF7's together with general output
--        7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

MUXF8_inst : MUXF8
port map (
   O => O,     -- Output of MUX to general routing
   I0 => I0,   -- Input (tie to MUXF7 L/LO out)
   I1 => I1,   -- Input (tie to MUXF7 L/LO out)
   S => S      -- Input select to MUX
);

-- End of MUXF8_inst instantiation
```

Verilog Instantiation Template

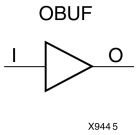
```
// MUXF8: CLB MUX to tie two MUXF7's together with general output
//        7 Series
// Xilinx HDL Libraries Guide, version 2012.2

MUXF8 MUXF8_inst (
   .O(O),     // Output of MUX to general routing
   .I0(I0),   // Input (tie to MUXF7 L/LO out)
   .I1(I1),   // Input (tie to MUXF7 L/LO out)
   .S(S)      // Input select to MUX
);

// End of MUXF8_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OBUF

Primitive: Output Buffer



Introduction

This design element is a simple output buffer used to drive output signals to the FPGA device pins that do not need to be 3-stated (constantly driven). Either an OBUF, OBUFT, OBUFDS, or OBUFTDS must be connected to every output port in the design.

This element isolates the internal circuit and provides drive current for signals leaving a chip. It exists in input/output blocks (IOB). Its output (O) is connected to an OPAD or an IOPAD. The interface standard used by this element is LVCMOS18. Also, this element has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints.

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Output of OBUF to be connected directly to top-level output port.
I	Input	1	Input of OBUF. Connect to the logic driving the output port.

Design Entry Method

Instantiation	Yes
Inference	Recommended
CORE Generator™ and wizards	No
Macro support	No

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
DRIVE	Integer	2, 4, 6, 8, 12, 16, 24	12	Specifies the output current drive strength of the I/O. It is suggested that you set this to the lowest setting tolerable for the design drive and timing requirements.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.

Attribute	Data Type	Allowed Values	Default	Description
SLEW	String	"SLOW" or "FAST"	"SLOW"	Specifies the slew rate of the output driver. Consult the product Data Sheet for recommendations of the best setting for this attribute.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- OBUF: Single-ended Output Buffer
--       7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

OBUF_inst : OBUF
generic map (
   DRIVE => 12,
   IOSTANDARD => "DEFAULT",
   SLEW => "SLOW")
port map (
   O => O,     -- Buffer output (connect directly to top-level port)
   I => I      -- Buffer input
);

-- End of OBUF_inst instantiation
```

Verilog Instantiation Template

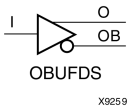
```
// OBUF: Single-ended Output Buffer
//       7 Series
// Xilinx HDL Libraries Guide, version 2012.2

OBUF #(
   .DRIVE(12),   // Specify the output drive strength
   .IOSTANDARD("DEFAULT"), // Specify the output I/O standard
   .SLEW("SLOW") // Specify the output slew rate
) OBUF_inst (
   .O(O),     // Buffer output (connect directly to top-level port)
   .I(I)      // Buffer input
);

// End of OBUF_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OBUFDS

Primitive: Differential Signaling Output Buffer



Introduction

This design element is a single output buffer that supports low-voltage, differential signaling. OBUFDS isolates the internal circuit and provides drive current for signals leaving the chip. Its output is represented as two distinct ports (O and OB), one deemed the "master" and the other the "slave." The master and the slave are opposite phases of the same logical signal (for example, MYNET and MYNETB).

Logic Table

Inputs	Outputs	
I	**O**	**OB**
0	0	1
1	1	0

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Diff_p output (connect directly to top level port)
OB	Output	1	Diff_n output (connect directly to top level port)
I	Input	1	Buffer input

Design Entry Method

Instantiation	Recommended
Inference	No
CORE Generator™ and wizards	No
Macro support	No

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
SLEW	String	"SLOW" or "FAST"	"SLOW"	Specifies the slew rate of the output driver. Consult the product Data Sheet for recommendations of the best setting for this attribute.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- OBUFDS: Differential Output Buffer
--         7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

OBUFDS_inst : OBUFDS
generic map (
   IOSTANDARD => "DEFAULT", -- Specify the output I/O standard
   SLEW => "SLOW")          -- Specify the output slew rate
port map (
   O => O,     -- Diff_p output (connect directly to top-level port)
   OB => OB,   -- Diff_n output (connect directly to top-level port)
   I => I      -- Buffer input
);

-- End of OBUFDS_inst instantiation
```

Verilog Instantiation Template

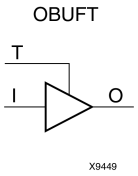
```
// OBUFDS: Differential Output Buffer
//         7 Series
// Xilinx HDL Libraries Guide, version 2012.2

OBUFDS #(
   .IOSTANDARD("DEFAULT"), // Specify the output I/O standard
   .SLEW("SLOW")           // Specify the output slew rate
) OBUFDS_inst (
   .O(O),     // Diff_p output (connect directly to top-level port)
   .OB(OB),   // Diff_n output (connect directly to top-level port)
   .I(I)      // Buffer input
);

// End of OBUFDS_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OBUFT

Primitive: 3-State Output Buffer with Active Low Output Enable



Introduction

This design element is a single, 3-state output buffer with input I, output O, and active-Low output enables (T). This element uses the LVCMOS18 standard and has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints.

When T is Low, data on the inputs of the buffers is transferred to the corresponding outputs. When T is High, the output is high impedance (off or Z state). OBUFTs are generally used when a single-ended output is needed with a 3-state capability, such as the case when building bidirectional I/O.

Logic Table

Inputs		Outputs
T	**I**	**O**
1	X	Z
0	1	1
0	0	0

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Buffer output (connect directly to top-level port)
I	Input	1	Buffer input
T	Input	1	3-state enable input

Design Entry Method

Instantiation	Yes
Inference	Recommended
CORE Generator™ and wizards	No
Macro support	No

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
DRIVE	Integer	2, 4, 6, 8, 12, 16, 24	12	Specifies the output current drive strength of the I/O. It is suggested that you set this to the lowest setting tolerable for the design drive and timing requirements.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
SLEW	String	"SLOW" or "FAST"	"SLOW"	Specifies the slew rate of the output driver. See the Data Sheet for recommendations of the best setting for this attribute.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- OBUFT: Single-ended 3-state Output Buffer
--        7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

OBUFT_inst : OBUFT
generic map (
   DRIVE => 12,
   IOSTANDARD => "DEFAULT",
   SLEW => "SLOW")
port map (
   O => O,     -- Buffer output (connect directly to top-level port)
   I => I,     -- Buffer input
   T => T      -- 3-state enable input
);

-- End of OBUFT_inst instantiation
```

Verilog Instantiation Template

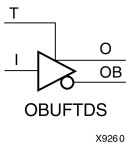
```
// OBUFT: Single-ended 3-state Output Buffer
//        All devices
// Xilinx HDL Libraries Guide, version 2012.2

OBUFT #(
   .DRIVE(12),   // Specify the output drive strength
   .IOSTANDARD("DEFAULT"), // Specify the output I/O standard
   .SLEW("SLOW") // Specify the output slew rate
) OBUFT_inst (
   .O(O),     // Buffer output (connect directly to top-level port)
   .I(I),     // Buffer input
   .T(T)      // 3-state enable input
);

  // End of OBUFT_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OBUFTDS

Primitive: 3-State Output Buffer with Differential Signaling, Active-Low Output Enable



Introduction

This design element is an output buffer that supports low-voltage, differential signaling. For the OBUFTDS, a design level interface signal is represented as two distinct ports (O and OB), one deemed the "master" and the other the "slave." The master and the slave are opposite phases of the same logical signal (for example, MYNET_P and MYNET_N).

Logic Table

Inputs		Outputs	
I	**T**	**O**	**OB**
X	1	Z	Z
0	0	0	1
1	0	1	0

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Diff_p output (connect directly to top level port)
OB	Output	1	Diff_n output (connect directly to top level port)
I	Input	1	Buffer input
T	Input	1	3-state enable input

Design Entry Method

Instantiation	Recommended
Inference	No
CORE Generator™ and wizards	No
Macro support	No

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
SLEW	String	"SLOW" or "FAST"	"SLOW"	Specifies the slew rate of the output driver. Consult the product Data Sheet for recommendations of the best setting for this attribute.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- OBUFTDS: Differential 3-state Output Buffer
--          7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

OBUFTDS_inst : OBUFTDS
generic map (
   IOSTANDARD => "DEFAULT")
port map (
   O => O,     -- Diff_p output (connect directly to top-level port)
   OB => OB,   -- Diff_n output (connect directly to top-level port)
   I => I,     -- Buffer input
   T => T      -- 3-state enable input
);

-- End of OBUFTDS_inst instantiation
```

Verilog Instantiation Template

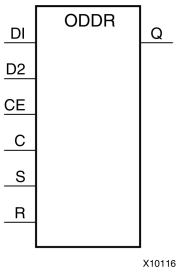
```
// OBUFTDS: Differential 3-state Output Buffer
//          7 Series
// Xilinx HDL Libraries Guide, version 2012.2

OBUFTDS #(
   .IOSTANDARD("DEFAULT"), // Specify the output I/O standard
   .SLEW("SLOW")           // Specify the output slew rate
) OBUFTDS_inst (
   .O(O),     // Diff_p output (connect directly to top-level port)
   .OB(OB),   // Diff_n output (connect directly to top-level port)
   .I(I),     // Buffer input
   .T(T)      // 3-state enable input
);

// End of OBUFTDS_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

ODDR

Primitive: Dedicated Dual Data Rate (DDR) Output Register



Introduction

This design element is a dedicated output register for use in transmitting dual data rate (DDR) signals from FPGA devices. The ODDR interface with the FPGA fabric is not limited to opposite clock edges. It can be configured to present date from the FPGA fabric at the same clock edge. This feature allows designers to avoid additional timing complexities and CLB usage. The ODDR also works with SelectIO™ features.

ODDR Modes

This element has two modes of operation. These modes are set by the DDR_CLK_EDGE attribute.

- **OPPOSITE_EDGE mode:** The data transmit interface uses classic DDR methodology. Given a data and clock at pin D1-2 and C respectively, D1 is sampled at every positive edge of clock C and D2 is sampled at every negative edge of clock C. Q changes every clock edge.
- **SAME_EDGE mode:** Data is still transmitted at the output of the ODDR by opposite edges of clock C. However, the two inputs to the ODDR are clocked with a positive clock edge of clock signal C and an extra register is clocked with a negative clock edge of clock signal C. Using this feature, DDR data can now be presented into the ODDR at the same clock edge.

Port Descriptions

Port	Direction	Width	Function
Q	Output	1	Data Output (DDR) - The ODDR output that connects to the IOB pad.
C	Input	1	Clock Input - The C pin represents the clock input pin.
CE	Input	1	Clock Enable Input - When asserted High, this port enables the clock input on port C.
D1 : D2	Input	1 (each)	Data Input - This pin is where the DDR data is presented into the ODDR module.
R	Input	1	Reset - Depends on how SRTYPE is set.
S	Input	1	Set - Active High asynchronous set pin. This pin can also be Synchronous depending on the SRTYPE attribute.

Design Entry Method

Instantiation	Recommended
Inference	No
CORE Generator™ and wizards	No
Macro support	No

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
DDR_CLK_EDGE	String	"OPPOSITE_EDGE", "SAME_EDGE"	"OPPOSITE_EDGE"	DDR clock mode recovery mode selection.
INIT	Integer	0, 1	1	Q initialization value.
SRTYPE	String	"SYNC", "ASYNC"	"SYNC"	Set/Reset type selection.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- ODDR: Output Double Data Rate Output Register with Set, Reset
--       and Clock Enable.
--       7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

ODDR_inst : ODDR
generic map(
   DDR_CLK_EDGE => "OPPOSITE_EDGE", -- "OPPOSITE_EDGE" or "SAME_EDGE"
   INIT => '0',   -- Initial value for Q port ('1' or '0')
   SRTYPE => "SYNC") -- Reset Type ("ASYNC" or "SYNC")
port map (
   Q => Q,   -- 1-bit DDR output
   C => C,    -- 1-bit clock input
   CE => CE,  -- 1-bit clock enable input
   D1 => D1,  -- 1-bit data input (positive edge)
   D2 => D2,  -- 1-bit data input (negative edge)
   R => R,    -- 1-bit reset input
   S => S     -- 1-bit set input
);

-- End of ODDR_inst instantiation
```

Verilog Instantiation Template

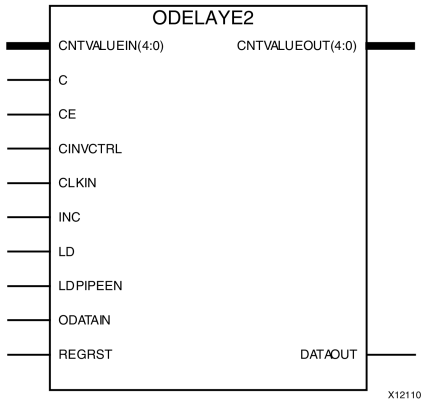
```
// ODDR: Output Double Data Rate Output Register with Set, Reset
//       and Clock Enable.
//       7 Series
// Xilinx HDL Libraries Guide, version 2012.2

ODDR #(
   .DDR_CLK_EDGE("OPPOSITE_EDGE"), // "OPPOSITE_EDGE" or "SAME_EDGE"
   .INIT(1'b0),    // Initial value of Q: 1'b0 or 1'b1
   .SRTYPE("SYNC") // Set/Reset type: "SYNC" or "ASYNC"
) ODDR_inst (
   .Q(Q),   // 1-bit DDR output
   .C(C),   // 1-bit clock input
   .CE(CE), // 1-bit clock enable input
   .D1(D1), // 1-bit data input (positive edge)
   .D2(D2), // 1-bit data input (negative edge)
   .R(R),   // 1-bit reset
   .S(S)    // 1-bit set
);

// End of ODDR_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

ODELAYE2

Primitive: Output Fixed or Variable Delay Element



Introduction

This design element can be used to provide a fixed delay or an adjustable delay to the output path of the 7 series FPGA. This delay can be useful for the purpose of external data alignment, external phase offset and simultaneous switching noise (SSN) mitigation, as well as allowing for the tracking of external data alignment over process, temperature, and voltage (PVT). When used in conjunction with the IDELAYCTRL component circuitry, can provide precise time increments of delay. When used in variable mode, the output path can be adjusted for increasing and decreasing amounts of delay. The ODELAYE2 is not available on the High Range (HR) banks in the 7 series devices.

Port Descriptions

Port	Type	Width	Function
C	Input	1	All control inputs to ODELAYE2 primitive (CNTVALUEIN, RST, CE, LD, LDPIPEEN and INC) are synchronous to the clock input (C). A clock must be connected to this port when the ODELAYE2 is configured in "VARIABLE", "VAR_LOAD" or "VAR_LOAD_PIPE" mode. C can be locally inverted, and must be supplied by a global or regional clock buffer. This clock should be connected to the same clock in the SelectIO logic resources (when using OSERDESE2, C is connected to CLKDIV). If the ODELAYE2 is configured as "FIXED", connect this port to gnd.
CE	Input	1	Active high enable increment/decrement function. If the ODELAYE2 is configured as "FIXED", connect this port to gnd.
CINVCTRL	Input	1	The CINVCTRL pin is used for dynamically switching the polarity of C pin. This is for use in applications when glitches are not an issue. When switching the polarity, do not use the ODELAYE2 control pins for two clock cycles. If the ODELAYE2 is configured as "FIXED", connect this port to gnd.
CLKIN	Input	1	Delayed Clock input into the ODELAYE2.

Port	Type	Width	Function
CNTVALUEIN<4:0>	Input	5	Counter value from FPGA logic for dynamically loadable tap value input when configigured in "VAR_LOAD" or "VAR_LOAD_PIPE" modes. If the ODELAYE2 is configured as "FIXED" or "VARIABLE", connect this port to gnd.
CNTVALUEOUT <4:0>	Output	5	The CNTVALUEOUT pins are used for reporting the dynamically switching value of the delay element. CNTVALUEOUT is only available when ODELAYE2 is in "VAR_LOAD" or "VAR_LOAD_PIPE" mode.
DATAOUT	Output	1	Delayed data/clock from either the CLKIN or ODATAIN ports. DATAOUT connects to an I/O port in the case of data or back to the clocking structure in the case of a clock..
INC	Input	1	The increment/decrement is controlled by the enable signal (CE). This interface is only available when ODELAYE2 is in VARIABLE, VAR_LOAD, or VAR_LOAD_PIPE mode.
LD	Input	1	Load initial value or loaded value to the counter.
LDPIPEEN	Input	1	Enable PIPELINE register to load data from LD pins.
ODATAIN	Input	1	The ODATAIN input is the output data to be delayed driven by the OSERDESE2 or output register.
REGRST	Input	1	The REGRST signal is an active-high reset and is synchronous to the input clock signal (C). When asserted, the tap value reverts to a zero state unless LDPIPEEN is also assreted in which case the tap value results in the value on the CNTVALUEIN port.

Design Entry Method

Instantiation	Yes
Inference	No
CORE Generator™ and wizards	Yes
Macro support	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
CINVCTRL_SEL	STRING	"FALSE", "TRUE"	"FALSE"	Enables the CINVCTRL_SEL pin to dynamically switch the polarity of the C pin.
DELAY_SRC	STRING	"ODATAIN", "CLKIN"	"ODATAIN"	Select the data input source: • "ODATAIN": ODELAYE2 chain input is ODATAIN • "CLKIN": ODELAYE2 chain input is CLKIN

Attribute	Type	Allowed Values	Default	Description
HIGH _PERFORMANCE_MODE	STRING	"FALSE", "TRUE"	"FALSE"	When TRUE, this attribute reduces the output jitter. When FALSE, power consumption is reduced. The difference in power consumption is quantified in the Xilinx Power Estimator tool.
ODELAY_TYPE	STRING	"FIXED", "VARIABLE", "VAR_LOAD", "VAR_LOAD_PIPE"	"FIXED"	Sets the type of tap delay line. • "FIXED": Sets a static delay value • "VARIABLE": Dynamically adjust (incement/decrement) delay value • "VAR_LOAD": Dynamically loads tap values • "VAR_LOAD_PIPE": Pipelined dynamically loadable tap values
ODELAY_VALUE	DECIMAL	0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31	0	Specifies the fixed number of delay taps in fixed mode or the initial starting number of taps in "VARIABLE" mode (output path). When IDELAY_TYPE is set to "VAR_LOAD" or "VAR_LOAD_PIPE" mode, this value is ignored.
PIPE_SEL	STRING	"FALSE", "TRUE"	"FALSE"	Select pipelined mode.
REFCLK _FREQUENCY	1 significant digit FLOAT	190.0 to 210.0 and 290.0 to 310.0	200.0	Sets the tap value (in MHz) used by the Timing Analyzer for static timing analysis and functional/timing simulation. The frequency of REFCLK must be within the given datasheet range to guarantee the tap-delay value and performance.
SIGNAL _PATTERN	STRING	"DATA", "CLOCK"	"DATA"	Causes timing analysis to account for the appropriate amount of delay-chain jitter when presented with either a "DATA" pattern with irregular transitions or a "CLOCK" pattern with a regular rise/fall pattern.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- ODELAYE2: Output Fixed or Variable Delay Element
--           7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

ODELAYE2_inst : ODELAYE2
generic map (
   CINVCTRL_SEL => "FALSE",          -- Enable dynamic clock inversion (FALSE, TRUE)
   DELAY_SRC => "ODATAIN",           -- Delay input (ODATAIN, CLKIN)
   HIGH_PERFORMANCE_MODE => "FALSE", -- Reduced jitter ("TRUE"), Reduced power ("FALSE")
   ODELAY_TYPE => "FIXED",           -- FIXED, VARIABLE, VAR_LOAD, VAR_LOAD_PIPE
   ODELAY_VALUE => 0,                -- Output delay tap setting (0-31)
   PIPE_SEL => "FALSE",              -- Select pipelined mode, FALSE, TRUE
   REFCLK_FREQUENCY => 200.0,        -- IDELAYCTRL clock input frequency in MHz (190.0-210.0).
   SIGNAL_PATTERN => "DATA"          -- DATA, CLOCK input signal
)
port map (
   CNTVALUEOUT => CNTVALUEOUT, -- 5-bit output: Counter value output
   DATAOUT => DATAOUT,         -- 1-bit output: Delayed data/clock output
   C => C,                     -- 1-bit input: Clock input
   CE => CE,                   -- 1-bit input: Active high enable increment/decrement input
   CINVCTRL => CINVCTRL,       -- 1-bit input: Dynamic clock inversion input
   CLKIN => CLKIN,             -- 1-bit input: Clock delay input
   CNTVALUEIN => CNTVALUEIN,   -- 5-bit input: Counter value input
   INC => INC,                 -- 1-bit input: Increment / Decrement tap delay input
   LD => LD,                   -- 1-bit input: Loads ODELAY_VALUE tap delay in VARIABLE mode, in VAR_LOAD or
                               -- VAR_LOAD_PIPE mode, loads the value of CNTVALUEIN

   LDPIPEEN => LDPIPEEN,       -- 1-bit input: Enables the pipeline register to load data
   ODATAIN => ODATAIN,         -- 1-bit input: Output delay data input
   REGRST => REGRST            -- 1-bit input: Active-high reset tap-delay input
);

-- End of ODELAYE2_inst instantiation
```

Verilog Instantiation Template

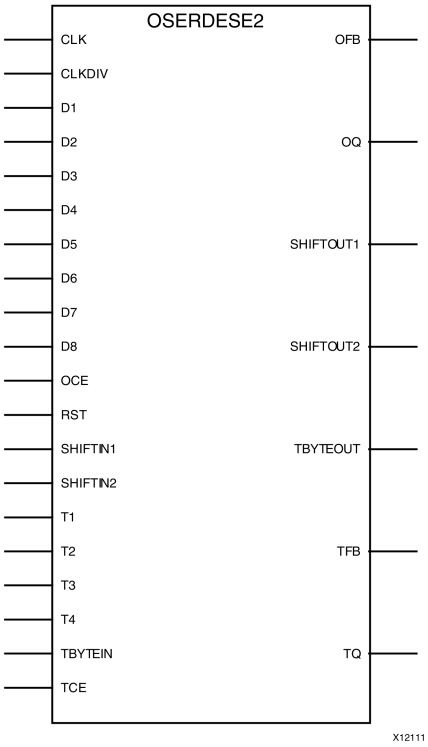
```
// ODELAYE2: Output Fixed or Variable Delay Element
//           7 Series
// Xilinx HDL Libraries Guide, version 2012.2

(* IODELAY_GROUP = <iodelay_group_name> *) // Specifies group name for associated IDELAYs/ODELAYs and IDELAYCTRL

ODELAYE2 #(
   .CINVCTRL_SEL("FALSE"),          // Enable dynamic clock inversion (FALSE, TRUE)
   .DELAY_SRC("ODATAIN"),           // Delay input (ODATAIN, CLKIN)
   .HIGH_PERFORMANCE_MODE("FALSE"), // Reduced jitter ("TRUE"), Reduced power ("FALSE")
   .ODELAY_TYPE("FIXED"),           // FIXED, VARIABLE, VAR_LOAD, VAR_LOAD_PIPE
   .ODELAY_VALUE(0),                // Output delay tap setting (0-31)
   .PIPE_SEL("FALSE"),              // Select pipelined mode, FALSE, TRUE
   .REFCLK_FREQUENCY(200.0),        // IDELAYCTRL clock input frequency in MHz (190.0-210.0).
   .SIGNAL_PATTERN("DATA")          // DATA, CLOCK input signal
)
ODELAYE2_inst (
   .CNTVALUEOUT(CNTVALUEOUT), // 5-bit output: Counter value output
   .DATAOUT(DATAOUT),         // 1-bit output: Delayed data/clock output
   .C(C),                     // 1-bit input: Clock input
   .CE(CE),                   // 1-bit input: Active high enable increment/decrement input
   .CINVCTRL(CINVCTRL),       // 1-bit input: Dynamic clock inversion input
   .CLKIN(CLKIN),             // 1-bit input: Clock delay input
   .CNTVALUEIN(CNTVALUEIN),   // 5-bit input: Counter value input
   .INC(INC),                 // 1-bit input: Increment / Decrement tap delay input
   .LD(LD),                   // 1-bit input: Loads ODELAY_VALUE tap delay in VARIABLE mode, in VAR_LOAD or
                              // VAR_LOAD_PIPE mode, loads the value of CNTVALUEIN

   .LDPIPEEN(LDPIPEEN),       // 1-bit input: Enables the pipeline register to load data
   .ODATAIN(ODATAIN),         // 1-bit input: Output delay data input
   .REGRST(REGRST)            // 1-bit input: Active-high reset tap-delay input
);

// End of ODELAYE2_inst instantiation
```

For More Information

- See the *7 series FPGA SelectIO Resources User Guide (UG471)*.
- See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OSERDESE2

Primitive: Output SERial/DESerializer with bitslip



Introduction

The OSERDES in 7 series devices is a dedicated parallel-to-serial converter with specific clocking and logic resources designed to facilitate the implementation of high-speed source-synchronous interfaces. Every OSERDES module includes a dedicated serializer for data and 3-state control. Both data and 3-state serializers can be configured in single data rate (SDR) and double data rate (DDR) mode. Data serialization can be up to 8:1 (10:1 or 14:1 if using OSERDES Width Expansion). 3-state serialization can be up to 4:1.

Port Descriptions

Port	Type	Width	Function
CLK	Input	1	This high speed clock input drives the serial side of the parallel-to-serial converters.
CLKDIV	Input	1	This divided high-speed clock input drives the parallel side of the parallel-to-serial converters. This clock is the divided version of the clock connected to the CLK port.

Port	Type	Width	Function
D1 - D8	Input	1	All incoming parallel data enters the OSERDES module through ports D1 to D8. These ports are connected to the FPGA fabric, and can be configured from two to eight bits (i.e., a 8:1 serialization). Bit widths greater than six (up to 14) can be supported by using a second OSERDES in SLAVE mode.
OCE	Input	1	OCE is an active High clock enable for the data path.
OFB	Output	1	The output feedback port (OFB) is the serial (high-speed) data output port of the OSERDESE2.
OQ	Output	1	The OQ port is the data output port of the OSERDES module. Data at the input port D1 will appear first at OQ. This port connects the output of the data parallel-to-serial converter to the data input of the IOB. This port can not drive the ODELAYE2; the OFB pin must be used.
RST	Input	1	The reset input causes the outputs of all data flip-flops in the CLK and CLKDIV domains to be driven Low asynchronously. OSERDES circuits running in the CLK domain where timing is critical use an internal, dedicated circuit to retime the RST input to produce a reset signal synchronous to the CLK domain. Similarly, there is a dedicated circuit to retime the RST input to produce a reset signal synchronous to the CLKDIV domain. Because there are OSERDES circuits that retime the RST input, the user is only required to provide a reset pulse to the RST input that meets timing on the CLKDIV frequency domain (synchronous to CLKDIV). Therefore, RST should be driven High for a minimum of one CLKDIV cycle. When building an interface consisting of multiple OSERDES ports, all OSERDES ports must be synchronized. The internal retiming of the RST input is designed so that all OSERDES blocks that receive the same reset pulse come out of reset synchronized with one another.
SHIFTIN1 / SHIFTIN2	Input	1	Cascade Input for data input expansion. Connect to SHIFTOUT1/2 of slave.
SHIFTOUT1 / SHIFTOUT2	Output	1	Cascade out for data input expansion. Connect to SHIFTIN1/2 of master.
TBYTEIN	Input	1	Byte group tristate input from source
TBYTEOUT	Output	1	Byte group tristate output to IOB
TCE	Input	1	TCE is an active High clock enable for the 3-state control path.
TFB	Output	1	This port is the 3-state control output of the OSERDES module sent to the ODELAYE2. When used, this port connects the output of the 3-state parallel-to-serial converter to the control/3-state input of the ODELAYE2.
TQ	Output	1	This port is the 3-state control output of the OSERDES module. When used, this port connects the output of the 3-state parallel-to-serial converter to the control/3-state input of the IOB.
T1 - T4	Input	1	All parallel 3-state signals enter the OSERDES module through ports T1 to T4. The ports are connected to the FPGA fabric, and can be configured as one, two, or four bits.

Design Entry Method

Instantiation	Yes
Inference	No
CORE Generator™ and wizards	Yes
Macro support	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
DATA_RATE_OQ	STRING	"DDR", "SDR"	"DDR"	The DATA_RATE_OQ attribute defines whether data is processed as single data rate (SDR) or double data rate (DDR).
DATA_RATE_TQ	STRING	"DDR", "BUF", "SDR"	"DDR"	The DATA_RATE_TQ attribute defines whether 3-state control is to be processed as single data rate (SDR) or double data rate (DDR).
DATA_WIDTH	DECIMAL	4, 2, 3, 5, 6, 7, 8, 10, 14	4	The DATA_WIDTH attribute defines the parallel data input width of the parallel-to-serial converter. The possible values for this attribute depend on the DATA_RATE_OQ attribute. When DATA_RATE_OQ is set to SDR, the possible values for the DATA_WIDTH attribute are 2, 3, 4, 5, 6, 7, and 8. When DATA_RATE_OQ is set to DDR, the possible values for the DATA_WIDTH attribute are 4, 6, 8, 10 and 14. When the DATA_WIDTH is set to widths larger than eight, a pair of OSERDES must be configured into a master-slave configuration.
INIT_OQ	BINARY	1'b0 to 1'b1	1'b0	Defines the initial value of OQ output.
INIT_TQ	BINARY	1'b0 to 1'b1	1'b0	Defines the initial value of TQ output.
SERDES_MODE	STRING	"MASTER", "SLAVE"	"MASTER"	The SERDES_MODE attribute defines whether the OSERDES module is a master or slave when using width expansion.
SRVAL_OQ	BINARY	1'b0 to 1'b1	1'b0	Defines the value of OQ outputs when the SR is invoked.
SRVAL_TQ	BINARY	1'b0 to 1'b1	1'b0	Defines the value of YQ outputs when the SR is invoked.

Attribute	Type	Allowed Values	Default	Description
TBYTE_CTL	STRING	"FALSE", "TRUE"	"FALSE"	Enable Tristate BYTE operation for DDR3 mode. This allows the tristate signal to take value from one of the tristate outputs which is acting as a source.
TBYTE_SRC	STRING	"FALSE", "TRUE"	"FALSE"	Enable OSERDES to act as a source for Tristate Byte operation in DDR3 mode.
TRISTATE_WIDTH	DECIMAL	4, 1	4	The TRISTATE_WIDTH attribute defines the parallel 3-state input width of the 3-state control parallel-to-serial converter. The possible values for this attribute depend on the DATA_RATE_TQ attribute. When DATA_RATE_TQ is set to SDR or BUF, the TRISTATE_WIDTH attribute can only be set to 1. When DATA_RATE_TQ is set to DDR, the possible values for the TRISTATE_WIDTH attribute is 4. TRISTATE_WIDTH cannot be set to widths larger than 4. When a DATA_WIDTH is larger than four, set the TRISTATE_WIDTH to 1.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- OSERDESE2: Output SERial/DESerializer with bitslip
--            7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

OSERDESE2_inst : OSERDESE2
generic map (
   DATA_RATE_OQ => "DDR",   -- DDR, SDR
   DATA_RATE_TQ => "DDR",   -- DDR, BUF, SDR
   DATA_WIDTH => 4,         -- Parallel data width (2-8,10,14)
   INIT_OQ => '0',          -- Initial value of OQ output (1'b0,1'b1)
   INIT_TQ => '0',          -- Initial value of TQ output (1'b0,1'b1)
   SERDES_MODE => "MASTER", -- MASTER, SLAVE
   SRVAL_OQ => '0',         -- OQ output value when SR is used (1'b0,1'b1)
   SRVAL_TQ => '0',         -- TQ output value when SR is used (1'b0,1'b1)
   TBYTE_CTL => "FALSE",    -- Enable tristate byte operation (FALSE, TRUE)
   TBYTE_SRC => "FALSE",    -- Tristate byte source (FALSE, TRUE)
   TRISTATE_WIDTH => 4      -- 3-state converter width (1,4)
)
port map (
   OFB => OFB,             -- 1-bit output: Feedback path for data
   OQ => OQ,               -- 1-bit output: Data path output
   -- SHIFTOUT1 / SHIFTOUT2: 1-bit (each) output: Data output expansion (1-bit each)
   SHIFTOUT1 => SHIFTOUT1,
   SHIFTOUT2 => SHIFTOUT2,
   TBYTEOUT => TBYTEOUT,   -- 1-bit output: Byte group tristate
   TFB => TFB,             -- 1-bit output: 3-state control
   TQ => TQ,               -- 1-bit output: 3-state control
```

```
   CLK => CLK,             -- 1-bit input: High speed clock
   CLKDIV => CLKDIV,       -- 1-bit input: Divided clock
   -- D1 - D8: 1-bit (each) input: Parallel data inputs (1-bit each)
   D1 => D1,
   D2 => D2,
   D3 => D3,
   D4 => D4,
   D5 => D5,
   D6 => D6,
   D7 => D7,
   D8 => D8,
   OCE => OCE,             -- 1-bit input: Output data clock enable
   RST => RST,             -- 1-bit input: Reset
   -- SHIFTIN1 / SHIFTIN2: 1-bit (each) input: Data input expansion (1-bit each)
   SHIFTIN1 => SHIFTIN1,
   SHIFTIN2 => SHIFTIN2,
   -- T1 - T4: 1-bit (each) input: Parallel 3-state inputs
   T1 => T1,
   T2 => T2,
   T3 => T3,
   T4 => T4,
   TBYTEIN => TBYTEIN,     -- 1-bit input: Byte group tristate
   TCE => TCE              -- 1-bit input: 3-state clock enable
);

-- End of OSERDESE2_inst instantiation
```

Verilog Instantiation Template

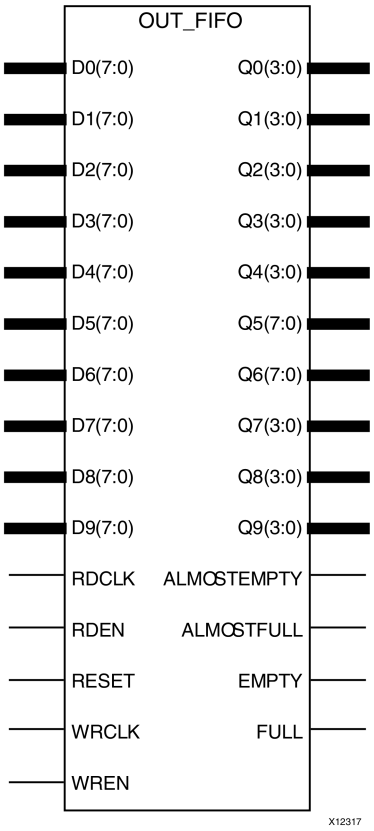
```
// OSERDESE2: Output SERial/DESerializer with bitslip
//            7 Series
// Xilinx HDL Libraries Guide, version 2012.2

OSERDESE2 #(
   .DATA_RATE_OQ("DDR"),   // DDR, SDR
   .DATA_RATE_TQ("DDR"),   // DDR, BUF, SDR
   .DATA_WIDTH(4),         // Parallel data width (2-8,10,14)
   .INIT_OQ(1'b0),         // Initial value of OQ output (1'b0,1'b1)
   .INIT_TQ(1'b0),         // Initial value of TQ output (1'b0,1'b1)
   .SERDES_MODE("MASTER"), // MASTER, SLAVE
   .SRVAL_OQ(1'b0),        // OQ output value when SR is used (1'b0,1'b1)
   .SRVAL_TQ(1'b0),        // TQ output value when SR is used (1'b0,1'b1)
   .TBYTE_CTL("FALSE"),    // Enable tristate byte operation (FALSE, TRUE)
   .TBYTE_SRC("FALSE"),    // Tristate byte source (FALSE, TRUE)
   .TRISTATE_WIDTH(4)      // 3-state converter width (1,4)
)
OSERDESE2_inst (
   .OFB(OFB),             // 1-bit output: Feedback path for data
   .OQ(OQ),               // 1-bit output: Data path output
   // SHIFTOUT1 / SHIFTOUT2: 1-bit (each) output: Data output expansion (1-bit each)
   .SHIFTOUT1(SHIFTOUT1),
   .SHIFTOUT2(SHIFTOUT2),
   .TBYTEOUT(TBYTEOUT),   // 1-bit output: Byte group tristate
   .TFB(TFB),             // 1-bit output: 3-state control
   .TQ(TQ),               // 1-bit output: 3-state control
   .CLK(CLK),             // 1-bit input: High speed clock
   .CLKDIV(CLKDIV),       // 1-bit input: Divided clock
   // D1 - D8: 1-bit (each) input: Parallel data inputs (1-bit each)
   .D1(D1),
   .D2(D2),
   .D3(D3),
   .D4(D4),
   .D5(D5),
   .D6(D6),
   .D7(D7),
   .D8(D8),
   .OCE(OCE),             // 1-bit input: Output data clock enable
   .RST(RST),             // 1-bit input: Reset
   // SHIFTIN1 / SHIFTIN2: 1-bit (each) input: Data input expansion (1-bit each)
   .SHIFTIN1(SHIFTIN1),
   .SHIFTIN2(SHIFTIN2),
   // T1 - T4: 1-bit (each) input: Parallel 3-state inputs
   .T1(T1),
   .T2(T2),
   .T3(T3),
   .T4(T4),
   .TBYTEIN(TBYTEIN),     // 1-bit input: Byte group tristate
   .TCE(TCE)              // 1-bit input: 3-state clock enable
);

// End of OSERDESE2_inst instantiation
```

For More Information

- See the *7 series FPGA SelectIO Resources User Guide (UG471)*.
- See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OUT_FIFO

Primitive: Output First-In, First-Out (FIFO) Buffer



The Output FIFO is a new resource located next to the I/O. This dedicated hardware is designed to help transition the data from fabric to the I/O, ODDR or OSERDES. It has two basic modes the first is a 4x4 mode where the data coming into the FIFO goes out at the same rate. The second mode is a 8x4 mode where the data coming out is serialized by a factor of 2. In other words in 8x4 mode 8 bits go to the OUT_FIFO and 4 bits come out.

The Output FIFO is a new resource located next to the I/O. This dedicated hardware is designed to help transition the data from fabric to the I/O, ODDR or OSERDES. It has two basic modes the first is a 4x4 mode where the data coming into the FIFO goes out at the same rate. The second mode is a 8x4 mode where the data coming out is serialized by a factor of 2. In other words in 8x4 mode 8 bits go to the OUT_FIFO and 4 bits come out. Features of this component include:

- Array dimensions: 80 wide, 8 deep (8x4 mode); 40 wide, 8 deep (4x4 mode)
- Empty and Full flags
- Programmable Almost Empty and Almost Full flags

Port Descriptions

Port	Type	Width	Function
ALMOSTEMPTY	Output	1	Active high output flag indicating the FIFO is almost empty. The threshold of the almost empty flag is set by the ALMOST_EMPTY_VALUE attribute.
ALMOSTFULL	Output	1	Active high output flag indicating the FIFO is almost full. The threshold of the almost empty flag is set by the ALMOST_FULL_VALUE attribute.
D0<7:0>	Input	8	Channel 0 input bus.
D1<7:0>	Input	8	Channel 1 input bus.
D2<7:0>	Input	8	Channel 2 input bus.
D3<7:0>	Input	8	Channel 3 input bus.
D4<7:0>	Input	8	Channel 4 input bus.
D5<7:0>	Input	8	Channel 5 input bus.
D6<7:0>	Input	8	Channel 6 input bus.
D7<7:0>	Input	8	Channel 7 input bus.
D8<7:0>	Input	8	Channel 8 input bus.
D9<7:0>	Input	8	Channel 9 input bus.
EMPTY	Output	1	Active high output flag indicating the FIFO is empty.
FULL	Output	1	Active high output flag indicating the FIFO is full.
Q0<3:0>	Output	4	Channel 0 output bus.
Q1<3:0>	Output	4	Channel 1 output bus.
Q2<3:0>	Output	4	Channel 2 output bus.
Q3<3:0>	Output	4	Channel 3 output bus.
Q4<3:0>	Output	4	Channel 4 output bus.
Q5<7:0>	Output	8	Channel 5 output bus.
Q6<7:0>	Output	8	Channel 6 output bus.
Q7<3:0>	Output	4	Channel 7 output bus.
Q8<3:0>	Output	4	Channel 8 output bus.
Q9<3:0>	Output	4	Channel 9 output bus.
RDCLK	Input	1	Read clock
RDEN	Input	1	Active high read enable
RESET	Input	1	Active high asynchrnous reset
WRCLK	Input	1	Write clock
WREN	Input	1	Active high write enable

Design Entry Method

Instantiation	Yes
Inference	No
CORE Generator™ and wizards	Yes
Macro support	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
ALMOST_EMPTY _VALUE	DECIMAL	1, 2	1	Specifies the number of entries left before asserting the ALMOSTEMPTY output signal.
ALMOST_FULL _VALUE	DECIMAL	1, 2	1	Specifies the number of entries left before asserting the ALMOSTFULL output signal.
ARRAY_MODE	STRING	"ARRAY_MODE_8_X_4", "ARRAY_MODE_4_X_4"	"ARRAY_MODE_8_X_4"	Specifies serializer mode: • "ARRAY_MODE_4_X_4" - four bits in, four bits out • "ARRAY_MODE_4_X_8" - Four bits in, eight bits out
OUTPUT _DISABLE	STRING	"FALSE", "TRUE"	"FALSE"	Disable output.
SYNCHRONOUS _MODE	STRING	"FALSE"	"FALSE"	Must always be set to false.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- OUT_FIFO: Output First-In, First-Out (FIFO) Buffer
--           7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

OUT_FIFO_inst : OUT_FIFO
generic map (
   ALMOST_EMPTY_VALUE => 1,          -- Almost empty offset (1-2)
   ALMOST_FULL_VALUE => 1,           -- Almost full offset (1-2)
   ARRAY_MODE => "ARRAY_MODE_8_X_4", -- ARRAY_MODE_8_X_4, ARRAY_MODE_4_X_4
   OUTPUT_DISABLE => "FALSE",        -- Disable output (FALSE, TRUE)
   SYNCHRONOUS_MODE => "FALSE"       -- Must always be set to false.
)
port map (
   -- FIFO Status Flags: 1-bit (each) output: Flags and other FIFO status outputs
   ALMOSTEMPTY => ALMOSTEMPTY, -- 1-bit output: Almost empty flag
   ALMOSTFULL => ALMOSTFULL,   -- 1-bit output: Almost full flag
   EMPTY => EMPTY,             -- 1-bit output: Empty flag
   FULL => FULL,               -- 1-bit output: Full flag
   -- Q0-Q9: 4-bit (each) output: FIFO Outputs
```

```
   Q0 => Q0,                   -- 4-bit output: Channel 0 output bus
   Q1 => Q1,                   -- 4-bit output: Channel 1 output bus
   Q2 => Q2,                   -- 4-bit output: Channel 2 output bus
   Q3 => Q3,                   -- 4-bit output: Channel 3 output bus
   Q4 => Q4,                   -- 4-bit output: Channel 4 output bus
   Q5 => Q5,                   -- 8-bit output: Channel 5 output bus
   Q6 => Q6,                   -- 8-bit output: Channel 6 output bus
   Q7 => Q7,                   -- 4-bit output: Channel 7 output bus
   Q8 => Q8,                   -- 4-bit output: Channel 8 output bus
   Q9 => Q9,                   -- 4-bit output: Channel 9 output bus
   -- D0-D9: 8-bit (each) input: FIFO inputs
   D0 => D0,                   -- 8-bit input: Channel 0 input bus
   D1 => D1,                   -- 8-bit input: Channel 1 input bus
   D2 => D2,                   -- 8-bit input: Channel 2 input bus
   D3 => D3,                   -- 8-bit input: Channel 3 input bus
   D4 => D4,                   -- 8-bit input: Channel 4 input bus
   D5 => D5,                   -- 8-bit input: Channel 5 input bus
   D6 => D6,                   -- 8-bit input: Channel 6 input bus
   D7 => D7,                   -- 8-bit input: Channel 7 input bus
   D8 => D8,                   -- 8-bit input: Channel 8 input bus
   D9 => D9,                   -- 8-bit input: Channel 9 input bus
   -- FIFO Control Signals: 1-bit (each) input: Clocks, Resets and Enables
   RDCLK => RDCLK,             -- 1-bit input: Read clock
   RDEN => RDEN,               -- 1-bit input: Read enable
   RESET => RESET,             -- 1-bit input: Active high reset
   WRCLK => WRCLK,             -- 1-bit input: Write clock
   WREN => WREN                -- 1-bit input: Write enable
);

-- End of OUT_FIFO_inst instantiation
```

Verilog Instantiation Template

```
// OUT_FIFO: Output First-In, First-Out (FIFO) Buffer
//           7 Series
// Xilinx HDL Libraries Guide, version 2012.2

OUT_FIFO #(
   .ALMOST_EMPTY_VALUE(1),          // Almost empty offset (1-2)
   .ALMOST_FULL_VALUE(1),           // Almost full offset (1-2)
   .ARRAY_MODE("ARRAY_MODE_8_X_4"), // ARRAY_MODE_8_X_4, ARRAY_MODE_4_X_4
   .OUTPUT_DISABLE("FALSE"),        // Disable output (FALSE, TRUE)
   .SYNCHRONOUS_MODE("FALSE")       // Must always be set to false.
)
OUT_FIFO_inst (
   // FIFO Status Flags: 1-bit (each) output: Flags and other FIFO status outputs
   .ALMOSTEMPTY(ALMOSTEMPTY), // 1-bit output: Almost empty flag
   .ALMOSTFULL(ALMOSTFULL),   // 1-bit output: Almost full flag
   .EMPTY(EMPTY),             // 1-bit output: Empty flag
   .FULL(FULL),               // 1-bit output: Full flag
   // Q0-Q9: 4-bit (each) output: FIFO Outputs
   .Q0(Q0),                   // 4-bit output: Channel 0 output bus
   .Q1(Q1),                   // 4-bit output: Channel 1 output bus
   .Q2(Q2),                   // 4-bit output: Channel 2 output bus
   .Q3(Q3),                   // 4-bit output: Channel 3 output bus
   .Q4(Q4),                   // 4-bit output: Channel 4 output bus
   .Q5(Q5),                   // 8-bit output: Channel 5 output bus
   .Q6(Q6),                   // 8-bit output: Channel 6 output bus
   .Q7(Q7),                   // 4-bit output: Channel 7 output bus
   .Q8(Q8),                   // 4-bit output: Channel 8 output bus
   .Q9(Q9),                   // 4-bit output: Channel 9 output bus
   // D0-D9: 8-bit (each) input: FIFO inputs
   .D0(D0),                   // 8-bit input: Channel 0 input bus
   .D1(D1),                   // 8-bit input: Channel 1 input bus
   .D2(D2),                   // 8-bit input: Channel 2 input bus
   .D3(D3),                   // 8-bit input: Channel 3 input bus
   .D4(D4),                   // 8-bit input: Channel 4 input bus
   .D5(D5),                   // 8-bit input: Channel 5 input bus
   .D6(D6),                   // 8-bit input: Channel 6 input bus
   .D7(D7),                   // 8-bit input: Channel 7 input bus
   .D8(D8),                   // 8-bit input: Channel 8 input bus
   .D9(D9),                   // 8-bit input: Channel 9 input bus
   // FIFO Control Signals: 1-bit (each) input: Clocks, Resets and Enables
   .RDCLK(RDCLK),             // 1-bit input: Read clock
   .RDEN(RDEN),               // 1-bit input: Read enable
   .RESET(RESET),             // 1-bit input: Active high reset
   .WRCLK(WRCLK),             // 1-bit input: Write clock
   .WREN(WREN)                // 1-bit input: Write enable
);

// End of OUT_FIFO_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

PHASER_IN

Primitive: Phaser in

Introduction

PHASER_IN is designed to work with other PHASER elements to handle data alignment and capture for high-speed memory interfaces. Its only intended use is by the Memory Interface Generator (MIG) and is not intended to be instantiated, used or modified outside of Xilinx generated IP.

Design Entry Method

Instantiation	No
Inference	No
CORE Generator™ and wizards	Yes
Macro support	No

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

PHASER_IN_PHY

Primitive: Phaser in phy

Introduction

PHASER_IN_PHY is designed to work with other PHASER elements to handle data alignment and capture for high-speed memory interfaces. Its only intended use is by the Memory Interface Generator(MIG) and is not intended to be instantiated, used or modified outside of Xilinx generated IP.

Design Entry Method

Instantiation	No
Inference	No
CORE Generator™ and wizards	Yes
Macro support	No

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

PHASER_OUT

Primitive: Phaser out.

Introduction

PHASER_OUT is designed to work with other PHASER elements to handle data alignment and capture for high-speed memory interfaces. Its only intended use is by the Memory Interface Generator (MIG) and is not intended to be instantiated, used or modified outside of Xilinx generated IP.

Design Entry Method

Instantiation	No
Inference	No
CORE Generator™ and wizards	Yes
Macro support	No

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

PHASER_OUT_PHY

Primitive: Phaser out phy.

Introduction

PHASER_OUT_PHY is designed to work with other PHASER elements to handle data alignment and capture for high-speed memory interfaces. Its only intended use is by the Memory Interface Generator (MIG) and is not intended to be instantiated, used or modified outside of Xilinx generated IP.

Design Entry Method

Instantiation	No
Inference	No
CORE Generator™ and wizards	Yes
Macro support	No

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

PHASER_REF

Primitive: Phaser out.

Introduction

PHASER_REF is designed to work with other PHASER elements to handle data alignment and capture for high-speed memory interfaces. Its only intended use is by the Memory Interface Generator (MIG) and is not intended to be instantiated, used or modified outside of Xilinx generated IP.

Design Entry Method

Instantiation	No
Inference	No
CORE Generator™ and wizards	Yes
Macro support	No

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

PHY_CONTROL

Primitive: Phaser out.

Introduction

PHY_CONTROL is designed to work with other PHASER elements to handle data alignment and capture for high-speed memory interfaces. Its only intended use is by the Memory Interface Generator (MIG) and is not intended to be instantiated, used or modified outside of Xilinx generated IP.

Design Entry Method

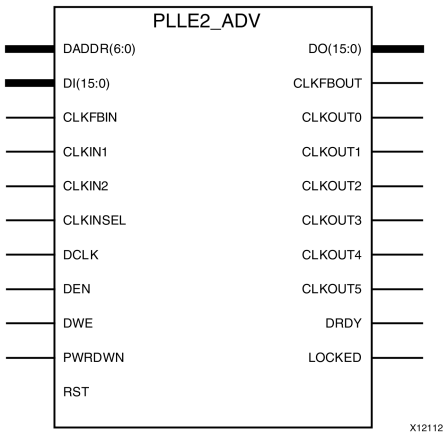
Instantiation	No
Inference	No
CORE Generator™ and wizards	Yes
Macro support	No

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

PLLE2_ADV

Primitive: Advanced Phase Locked Loop (PLL)



Introduction

The PLLE2 is a mixed signal block designed to support frequency synthesis, clock network deskew, and jitter reduction. The clock outputs can each have an individual divide, phase shift and duty cycle based on the same VCO frequency. The PLLE2 complements the MMCM by supporting higher speed clocking while the MMCM has more features to handle most general clocking needs. The PLLE2_BASE is intended for most uses of this PLL component while the PLLE2_ADV is intended for use when clock switch-over or dynamic reconfiguration is required.

Port Descriptions

Port	Type	Width	Function
CLKFBIN	Input	1	Feedback clock pin to the PLL
CLKFBOUT	Output	1	Dedicated PLL Feedback clock output
CLKINSEL	Input	1	Signal controls the state of the input MUX, High = CLKIN1, Low = CLKIN2.
CLKIN1	Input	1	Primary clock input.
CLKIN2	Input	1	Secondary clock input.
CLKOUT0	Output	1	CLKOUT0 output
CLKOUT1	Output	1	CLKOUT1 output
CLKOUT2	Output	1	CLKOUT2 output
CLKOUT3	Output	1	CLKOUT3 output
CLKOUT4	Output	1	CLKOUT4 output
CLKOUT5	Output	1	CLKOUT5 output
DADDR<6:0>	Input	7	The dynamic reconfiguration address (DADDR) input bus provides a reconfiguration address for the dynamic reconfiguration. When not used, all bits must be assigned zeros.

Port	Type	Width	Function
DCLK	Input	1	The DCLK signal is the reference clock for the dynamic reconfiguration port.
DEN	Input	1	The dynamic reconfiguration enable (DEN) provides the enable control signal to access the dynamic reconfiguration feature. When the dynamic reconfiguration feature is not used, DEN must be tied Low.
DI<15:0>	Input	16	The dynamic reconfiguration data input (DI) bus provides reconfiguration data. When not used, all bits must be set to zero.
DO<15:0>	Output	16	The dynamic reconfiguration output bus provides PLL data output when using dynamic reconfiguration.
DRDY	Output	1	The dynamic reconfiguration ready output (DRDY) provides the response to the DEN signal for the PLLs dynamic reconfiguration feature.
DWE	Input	1	The dynamic reconfiguration write enable (DWE) input pin provides the write enable control signal to write the DI data into the DADDR address. When not used, it must be tied Low.
PWRDWN	Input	1	Powers down instantiated but unused PLLs.
RST	Input	1	The RST signal is an asynchronous reset for the PLL. The PLL will synchronously re-enable itself when this signal is released and go through a new phase alignment and lock cycle. A reset is required when the input clock conditions change (e.g., frequency).
Status Ports	Output	1	An output from the PLL that indicates when the PLL has achieved phase alignment within a predefined window and frequency matching within a predefined PPM range. The PLL automatically locks after power on, no extra reset is required. LOCKED will be deasserted if the input clock stops or the phase alignment is violated (e.g., input clock phase shift). The PLL automatically reacquires lock after LOCKED is deasserted.

Design Entry Method

Instantiation	Yes
Inference	No
CORE Generator™ and wizards	Yes
Macro support	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
BANDWIDTH	STRING	"OPTIMIZED", "HIGH", "LOW"	"OPTIMIZED"	Specifies the PLLE2 programming algorithm affecting the jitter, phase margin and other characteristics of the PLLE2.
CLKFBOUT _MULT	DECIMAL	2 to 64	5	Specifies the amount to multiply all CLKOUT clock outputs if a different frequency is desired. This number, in combination with the associated CLKOUT#_DIVIDE value and DIVCLK_DIVIDE value, will determine the output frequency.
CLKFBOUT _PHASE	3 significant digit FLOAT	-360.000 to 360.000	0.000	Specifies the phase offset in degrees of the clock feedback output. Shifting the feedback clock results in a negative phase shift of all output clocks to the PLL.
CLKIN1 _PERIOD, CLKIN2 _PERIOD	FLOAT(nS)	0.000 to 52.631	0.000	Specifies the input period in ns to the PLLE2 CLKIN inputs. Resolution is down to the ps. For example a value of 33.333 would indicate a 30 MHz input clock. This information is mandatory and must be supplied. CLKIN1_PERIOD relates to the input period on the CLKIN1 input while CLKIN2_PERIOD relates to the input clock period on the CLKIN2 input.
CLKOUT0 _DIVIDE, CLKOUT1 _DIVIDE, CLKOUT2 _DIVIDE, CLKOUT3 _DIVIDE, CLKOUT4 _DIVIDE, CLKOUT5 _DIVIDE	DECIMAL	1 to 128	1	Specifies the amount to divide the associated CLKOUT clock output if a different frequency is desired. This number in combination with the CLKFBOUT_MULT and DIVCLK_DIVIDE values will determine the output frequency.
CLKOUT0_DUTY _CYCLE, CLKOUT1_DUTY _CYCLE, CLKOUT2_DUTY _CYCLE, CLKOUT3_DUTY _CYCLE, CLKOUT4_DUTY _CYCLE, CLKOUT5_DUTY _CYCLE	3 significant digit FLOAT	0.001 to 0.999	0.500	Specifies the Duty Cycle of the associated CLKOUT clock output in percentage (i.e., 0.500 will generate a 50% duty cycle).

Attribute	Type	Allowed Values	Default	Description
CLKOUT0 _PHASE, CLKOUT1 _PHASE, CLKOUT2 _PHASE, CLKOUT3 _PHASE, CLKOUT4 _PHASE, CLKOUT5 _PHASE	3 significant digit FLOAT	-360.000 to 360.000	0.000	Specifies the phase offset in degrees of the clock feedback output. Shifting the feedback clock results in a negative phase shift of all output clocks to the PLL.
COMPENSATION	STRING	"ZHOLD", "BUF_IN", "EXTERNAL", "INTERNAL"	"ZHOLD"	Clock input compensation. Suggested to be set to "ZHOLD". Defines how the PLL feedback is configured. • "ZHOLD" - PLL is configured to provide a negative hold time at the I/O registers. • "INTERNAL" - PLL is using its own internal feedback path so no delay is being compensated. • "EXTERNAL" - a network external to the FPGA is being compensated. • "BUF_IN" - the configuration does not match with the other compensation modes and no delay will be compensated.
DIVCLK _DIVIDE	DECIMAL	1 to 56	1	Specifies the division ratio for all output clocks with respect to the input clock. Effectively divides the CLKIN going into the PFD.
REF_JITTER1, REF_JITTER2	3 significant digit FLOAT	0.000 to 0.999	0.010	Allows specification of the expected jitter on the CLKIN inputs in order to better optimize PLL performance. A bandwidth setting of OPTIMIZED will attempt to choose the best parameter for input clocking when unknown. If known, then the value provided should be specified in terms of the UI percentage (the maximum peak to peak value) of the expected jitter on the input clock. REF_JITTER1 relates to the input jitter on CLKIN1 while REF_JITTER2 relates to the input jitter on CLKIN2.
STARTUP_WAIT	STRING	"FALSE", "TRUE"	"FALSE"	When "TRUE", wait for the PLLE2(s) that have this attribute

Attribute	Type	Allowed Values	Default	Description
				attached to them will delay DONE from going high until a LOCK is achieved.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- PLLE2_ADV: Advanced Phase Locked Loop (PLL)
--            7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

PLLE2_ADV_inst : PLLE2_ADV
generic map (
   BANDWIDTH => "OPTIMIZED",  -- OPTIMIZED, HIGH, LOW
   CLKFBOUT_MULT => 5,        -- Multiply value for all CLKOUT, (2-64)
   CLKFBOUT_PHASE => 0.0,     -- Phase offset in degrees of CLKFB, (-360.000-360.000).
   -- CLKIN_PERIOD: Input clock period in nS to ps resolution (i.e. 33.333 is 30 MHz).
   CLKIN1_PERIOD => 0.0,
   CLKIN2_PERIOD => 0.0,
   -- CLKOUT0_DIVIDE - CLKOUT5_DIVIDE: Divide amount for CLKOUT (1-128)
   CLKOUT0_DIVIDE => 1,
   CLKOUT1_DIVIDE => 1,
   CLKOUT2_DIVIDE => 1,
   CLKOUT3_DIVIDE => 1,
   CLKOUT4_DIVIDE => 1,
   CLKOUT5_DIVIDE => 1,
   -- CLKOUT0_DUTY_CYCLE - CLKOUT5_DUTY_CYCLE: Duty cycle for CLKOUT outputs (0.001-0.999).
   CLKOUT0_DUTY_CYCLE => 0.5,
   CLKOUT1_DUTY_CYCLE => 0.5,
   CLKOUT2_DUTY_CYCLE => 0.5,
   CLKOUT3_DUTY_CYCLE => 0.5,
   CLKOUT4_DUTY_CYCLE => 0.5,
   CLKOUT5_DUTY_CYCLE => 0.5,
   -- CLKOUT0_PHASE - CLKOUT5_PHASE: Phase offset for CLKOUT outputs (-360.000-360.000).
   CLKOUT0_PHASE => 0.0,
   CLKOUT1_PHASE => 0.0,
   CLKOUT2_PHASE => 0.0,
   CLKOUT3_PHASE => 0.0,
   CLKOUT4_PHASE => 0.0,
   CLKOUT5_PHASE => 0.0,
   COMPENSATION => "ZHOLD",   -- ZHOLD, BUF_IN, EXTERNAL, INTERNAL
   DIVCLK_DIVIDE => 1,        -- Master division value (1-56)
   -- REF_JITTER: Reference input jitter in UI (0.000-0.999).
   REF_JITTER1 => 0.0,
   REF_JITTER2 => 0.0,
   STARTUP_WAIT => "FALSE"    -- Delay DONE until PLL Locks, ("TRUE"/"FALSE")
)
port map (
   -- Clock Outputs: 1-bit (each) output: User configurable clock outputs
   CLKOUT0 => CLKOUT0,   -- 1-bit output: CLKOUT0
   CLKOUT1 => CLKOUT1,   -- 1-bit output: CLKOUT1
   CLKOUT2 => CLKOUT2,   -- 1-bit output: CLKOUT2
   CLKOUT3 => CLKOUT3,   -- 1-bit output: CLKOUT3
   CLKOUT4 => CLKOUT4,   -- 1-bit output: CLKOUT4
   CLKOUT5 => CLKOUT5,   -- 1-bit output: CLKOUT5
   -- DRP Ports: 16-bit (each) output: Dynamic reconfiguration ports
   DO => DO,             -- 16-bit output: DRP data
   DRDY => DRDY,         -- 1-bit output: DRP ready
   -- Feedback Clocks: 1-bit (each) output: Clock feedback ports
   CLKFBOUT => CLKFBOUT, -- 1-bit output: Feedback clock
   -- Status Ports: 1-bit (each) output: PLL status ports
```

```
   LOCKED => LOCKED,     -- 1-bit output: LOCK
   -- Clock Inputs: 1-bit (each) input: Clock inputs
   CLKIN1 => CLKIN1,     -- 1-bit input: Primary clock
   CLKIN2 => CLKIN2,     -- 1-bit input: Secondary clock
   -- Control Ports: 1-bit (each) input: PLL control ports
   CLKINSEL => CLKINSEL, -- 1-bit input: Clock select, High=CLKIN1 Low=CLKIN2
   PWRDWN => PWRDWN,     -- 1-bit input: Power-down
   RST => RST,           -- 1-bit input: Reset
   -- DRP Ports: 7-bit (each) input: Dynamic reconfiguration ports
   DADDR => DADDR,       -- 7-bit input: DRP address
   DCLK => DCLK,         -- 1-bit input: DRP clock
   DEN => DEN,           -- 1-bit input: DRP enable
   DI => DI,             -- 16-bit input: DRP data
   DWE => DWE,           -- 1-bit input: DRP write enable
   -- Feedback Clocks: 1-bit (each) input: Clock feedback ports
   CLKFBIN => CLKFBIN    -- 1-bit input: Feedback clock
);

-- End of PLLE2_ADV_inst instantiation
```

Verilog Instantiation Template

```
// PLLE2_ADV: Advanced Phase Locked Loop (PLL)
//            7 Series
// Xilinx HDL Libraries Guide, version 2012.2

PLLE2_ADV #(
   .BANDWIDTH("OPTIMIZED"),  // OPTIMIZED, HIGH, LOW
   .CLKFBOUT_MULT(5),        // Multiply value for all CLKOUT, (2-64)
   .CLKFBOUT_PHASE(0.0),     // Phase offset in degrees of CLKFB, (-360.000-360.000).
   // CLKIN_PERIOD: Input clock period in nS to ps resolution (i.e. 33.333 is 30 MHz).
   .CLKIN1_PERIOD(0.0),
   .CLKIN2_PERIOD(0.0),
   // CLKOUT0_DIVIDE - CLKOUT5_DIVIDE: Divide amount for CLKOUT (1-128)
   .CLKOUT0_DIVIDE(1),
   .CLKOUT1_DIVIDE(1),
   .CLKOUT2_DIVIDE(1),
   .CLKOUT3_DIVIDE(1),
   .CLKOUT4_DIVIDE(1),
   .CLKOUT5_DIVIDE(1),
   // CLKOUT0_DUTY_CYCLE - CLKOUT5_DUTY_CYCLE: Duty cycle for CLKOUT outputs (0.001-0.999).
   .CLKOUT0_DUTY_CYCLE(0.5),
   .CLKOUT1_DUTY_CYCLE(0.5),
   .CLKOUT2_DUTY_CYCLE(0.5),
   .CLKOUT3_DUTY_CYCLE(0.5),
   .CLKOUT4_DUTY_CYCLE(0.5),
   .CLKOUT5_DUTY_CYCLE(0.5),
   // CLKOUT0_PHASE - CLKOUT5_PHASE: Phase offset for CLKOUT outputs (-360.000-360.000).
   .CLKOUT0_PHASE(0.0),
   .CLKOUT1_PHASE(0.0),
   .CLKOUT2_PHASE(0.0),
   .CLKOUT3_PHASE(0.0),
   .CLKOUT4_PHASE(0.0),
   .CLKOUT5_PHASE(0.0),
   .COMPENSATION("ZHOLD"),   // ZHOLD, BUF_IN, EXTERNAL, INTERNAL
   .DIVCLK_DIVIDE(1),        // Master division value (1-56)
   // REF_JITTER: Reference input jitter in UI (0.000-0.999).
   .REF_JITTER1(0.0),
   .REF_JITTER2(0.0),
   .STARTUP_WAIT("FALSE")    // Delay DONE until PLL Locks, ("TRUE"/"FALSE")
)
PLLE2_ADV_inst (
   // Clock Outputs: 1-bit (each) output: User configurable clock outputs
   .CLKOUT0(CLKOUT0),   // 1-bit output: CLKOUT0
   .CLKOUT1(CLKOUT1),   // 1-bit output: CLKOUT1
   .CLKOUT2(CLKOUT2),   // 1-bit output: CLKOUT2
   .CLKOUT3(CLKOUT3),   // 1-bit output: CLKOUT3
   .CLKOUT4(CLKOUT4),   // 1-bit output: CLKOUT4
   .CLKOUT5(CLKOUT5),   // 1-bit output: CLKOUT5
   // DRP Ports: 16-bit (each) output: Dynamic reconfiguration ports
```

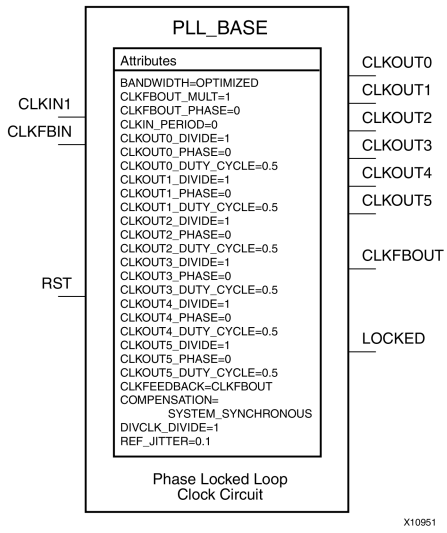
```
   .DO(DO),              // 16-bit output: DRP data
   .DRDY(DRDY),          // 1-bit output: DRP ready
   // Feedback Clocks: 1-bit (each) output: Clock feedback ports
   .CLKFBOUT(CLKFBOUT), // 1-bit output: Feedback clock
   // Status Ports: 1-bit (each) output: PLL status ports
   .LOCKED(LOCKED),     // 1-bit output: LOCK
   // Clock Inputs: 1-bit (each) input: Clock inputs
   .CLKIN1(CLKIN1),     // 1-bit input: Primary clock
   .CLKIN2(CLKIN2),     // 1-bit input: Secondary clock
   // Control Ports: 1-bit (each) input: PLL control ports
   .CLKINSEL(CLKINSEL), // 1-bit input: Clock select, High=CLKIN1 Low=CLKIN2
   .PWRDWN(PWRDWN),     // 1-bit input: Power-down
   .RST(RST),           // 1-bit input: Reset
   // DRP Ports: 7-bit (each) input: Dynamic reconfiguration ports
   .DADDR(DADDR),       // 7-bit input: DRP address
   .DCLK(DCLK),         // 1-bit input: DRP clock
   .DEN(DEN),           // 1-bit input: DRP enable
   .DI(DI),             // 16-bit input: DRP data
   .DWE(DWE),           // 1-bit input: DRP write enable
   // Feedback Clocks: 1-bit (each) input: Clock feedback ports
   .CLKFBIN(CLKFBIN)    // 1-bit input: Feedback clock
);

// End of PLLE2_ADV_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

PLLE2_BASE

Primitive: Base Phase Locked Loop (PLL)



Introduction

The PLLE2 is a mixed signal block designed to support frequency synthesis, clock network deskew, and jitter reduction. The clock outputs can each have an individual divide, phase shift and duty cycle based on the same VCO frequency. The PLLE2 complements the MMCM by supporting higher speed clocking while the MMCM has more features to handle most general clocking needs. The PLLE2_BASE is intended for most uses of this PLL component while the PLLE2_ADV is intended for use when clock switch-over or dynamic reconfiguration is required.

Port Descriptions

Port	Direction	Width	Function
CLKFBIN	Input	1	Feedback clock pin to the PLL
CLKFBOUT	Output	1	Dedicated PLL Feedback clock output
Clock Input	Input	1	General clock input.
Clock Outpu ts	Output	1	User configurable clock outputs that can be divided versions of the VCO phase outputs (user controllable) from 1 (bypassed) to 128. The output clocks are phase aligned to each other (unless phase shifted) and aligned to the input clock with a proper feedback configuration. .
PWRDWN	Input	1	Powers down instantiated but unused PLLs.
RST	Input	1	The RST signal is an asynchronous reset for the PLL. The PLL will synchronously re-enable itself when this signal is released and go through a new phase alignment and lock

Port	Direction	Width	Function
			cycle. A reset is required when the input clock conditions change (e.g., frequency).
Status Port	Output	1	An output from the PLL that indicates when the PLL has achieved phase alignment within a predefined window and frequency matching within a predefined PPM range. The PLL automatically locks after power on, no extra reset is required. LOCKED will be deasserted if the input clock stops or the phase alignment is violated (e.g., input clock phase shift). The PLL automatically reacquires lock after LOCKED is deasserted.

Design Entry Method

Instantiation	Yes
Inference	No
CORE Generator™ and wizards	Yes
Macro support	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
BANDWIDTH	STRING	"OPTIMIZED", "HIGH", "LOW"	"OPTIMIZED"	Specifies the PLLE2 programming algorithm affecting the jitter, phase margin and other characteristics of the PLLE2.
CLKFBOUT _MULT	DECIMAL	2 to 64	5	Specifies the amount to multiply all CLKOUT clock outputs if a different frequency is desired. This number, in combination with the associated CLKOUT#_DIVIDE value and DIVCLK_DIVIDE value, will determine the output frequency.
CLKFBOUT _PHASE	3 significant digit FLOAT	-360.000 to 360.000	0.000	Specifies the phase offset in degrees of the clock feedback output. Shifting the feedback clock results in a negative phase shift of all output clocks to the PLL.
CLKIN1 _PERIOD	FLOAT(nS)	0.000 to 52.631	0.000	Specifies the input period in ns to the PLL CLKIN1 input. Resolution is down to the ps (3 decimal places). For exmaple a value of 33.333 would indicate a 30 MHz input clock. This information is mandatory and must be supplied.

Attribute	Type	Allowed Values	Default	Description
CLKOUT0 _DIVIDE, CLKOUT1 _DIVIDE, CLKOUT2 _DIVIDE, CLKOUT3 _DIVIDE, CLKOUT4 _DIVIDE, CLKOUT5 _DIVIDE	DECIMAL	1 to 128	1	Specifies the amount to divide the associated CLKOUT clock output if a different frequency is desired. This number in combination with the CLKFBOUT_MULT and DIVCLK_DIVIDE values will determine the output frequency.
CLKOUT0_DUTY _CYCLE, CLKOUT1_DUTY _CYCLE, CLKOUT2_DUTY _CYCLE, CLKOUT3_DUTY _CYCLE, CLKOUT4_DUTY _CYCLE, CLKOUT5_DUTY _CYCLE	3 significant digit FLOAT	0.001 to 0.999	0.500	Specifies the Duty Cycle of the associated CLKOUT clock output in percentage (i.e., 0.500 will generate a 50% duty cycle).
CLKOUT0 _PHASE, CLKOUT1 _PHASE, CLKOUT2 _PHASE, CLKOUT3 _PHASE, CLKOUT4 _PHASE, CLKOUT5 _PHASE	3 significant digit FLOAT	-360.000 to 360.000	0.000	Specifies the phase offset in degrees of the clock feedback output. Shifting the feedback clock results in a negative phase shift of all output clocks to the PLL.
DIVCLK _DIVIDE	DECIMAL	1 to 56	1	Specifies the division ratio for all output clocks with respect to the input clock. Effectively divides the CLKIN going into the PFD.
REF_JITTER1	3 significant digit FLOAT	0.000 to 0.999	0.010	Allows specification of the expected jitter on CLKIN1 in order to better optimize PLL performance. A bandwidth setting of OPTIMIZED will attempt to choose the best parameter for input clocking when unknown. If known, then the value provided should be specified in terms of the UI percentage (the maximum peak to peak value) of the expected jitter on the input clock.
STARTUP_WAIT	STRING	"FALSE", "TRUE"	"FALSE"	When "TRUE", wait for the PLLE2(s) that have this attribute attached to them will delay DONE from going high until a LOCK is achieved.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- PLLE2_BASE: Base Phase Locked Loop (PLL)
--             7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

PLLE2_BASE_inst : PLLE2_BASE
generic map (
   BANDWIDTH => "OPTIMIZED",  -- OPTIMIZED, HIGH, LOW
   CLKFBOUT_MULT => 5,        -- Multiply value for all CLKOUT, (2-64)
   CLKFBOUT_PHASE => 0.0,     -- Phase offset in degrees of CLKFB, (-360.000-360.000).
   CLKIN1_PERIOD => 0.0,      -- Input clock period in ns to ps resolution (i.e. 33.333 is 30 MHz).
   -- CLKOUT0_DIVIDE - CLKOUT5_DIVIDE: Divide amount for each CLKOUT (1-128)
   CLKOUT0_DIVIDE => 1,
   CLKOUT1_DIVIDE => 1,
   CLKOUT2_DIVIDE => 1,
   CLKOUT3_DIVIDE => 1,
   CLKOUT4_DIVIDE => 1,
   CLKOUT5_DIVIDE => 1,
   -- CLKOUT0_DUTY_CYCLE - CLKOUT5_DUTY_CYCLE: Duty cycle for each CLKOUT (0.001-0.999).
   CLKOUT0_DUTY_CYCLE => 0.5,
   CLKOUT1_DUTY_CYCLE => 0.5,
   CLKOUT2_DUTY_CYCLE => 0.5,
   CLKOUT3_DUTY_CYCLE => 0.5,
   CLKOUT4_DUTY_CYCLE => 0.5,
   CLKOUT5_DUTY_CYCLE => 0.5,
   -- CLKOUT0_PHASE - CLKOUT5_PHASE: Phase offset for each CLKOUT (-360.000-360.000).
   CLKOUT0_PHASE => 0.0,
   CLKOUT1_PHASE => 0.0,
   CLKOUT2_PHASE => 0.0,
   CLKOUT3_PHASE => 0.0,
   CLKOUT4_PHASE => 0.0,
   CLKOUT5_PHASE => 0.0,
   DIVCLK_DIVIDE => 1,        -- Master division value, (1-56)
   REF_JITTER1 => 0.0,        -- Reference input jitter in UI, (0.000-0.999).
   STARTUP_WAIT => "FALSE"    -- Delay DONE until PLL Locks, ("TRUE"/"FALSE")
)
port map (
   -- Clock Outputs: 1-bit (each) output: User configurable clock outputs
   CLKOUT0 => CLKOUT0,
   CLKOUT1 => CLKOUT1,
   CLKOUT2 => CLKOUT2,
   CLKOUT3 => CLKOUT3,
   CLKOUT4 => CLKOUT4,
   CLKOUT5 => CLKOUT5,
   -- Feedback Clocks: 1-bit (each) output: Clock feedback ports
   CLKFBOUT => CLKFBOUT, -- 1-bit output: Feedback clock
   -- Status Port: 1-bit (each) output: PLL status ports
   LOCKED => LOCKED,     -- 1-bit output: LOCK
   -- Clock Input: 1-bit (each) input: Clock input
   CLKIN1 => CLKIN1,     -- 1-bit input: Input clock
   -- Control Ports: 1-bit (each) input: PLL control ports
   PWRDWN => PWRDWN,     -- 1-bit input: Power-down
   RST => RST,           -- 1-bit input: Reset
   -- Feedback Clocks: 1-bit (each) input: Clock feedback ports
   CLKFBIN => CLKFBIN    -- 1-bit input: Feedback clock
);

-- End of PLLE2_BASE_inst instantiation
```

Verilog Instantiation Template

```
// PLLE2_BASE: Base Phase Locked Loop (PLL)
//             7 Series
// Xilinx HDL Libraries Guide, version 2012.2

PLLE2_BASE #(
   .BANDWIDTH("OPTIMIZED"),  // OPTIMIZED, HIGH, LOW
   .CLKFBOUT_MULT(5),        // Multiply value for all CLKOUT, (2-64)
   .CLKFBOUT_PHASE(0.0),     // Phase offset in degrees of CLKFB, (-360.000-360.000).
   .CLKIN1_PERIOD(0.0),      // Input clock period in ns to ps resolution (i.e. 33.333 is 30 MHz).
   // CLKOUT0_DIVIDE - CLKOUT5_DIVIDE: Divide amount for each CLKOUT (1-128)
   .CLKOUT0_DIVIDE(1),
   .CLKOUT1_DIVIDE(1),
   .CLKOUT2_DIVIDE(1),
   .CLKOUT3_DIVIDE(1),
   .CLKOUT4_DIVIDE(1),
   .CLKOUT5_DIVIDE(1),
   // CLKOUT0_DUTY_CYCLE - CLKOUT5_DUTY_CYCLE: Duty cycle for each CLKOUT (0.001-0.999).
   .CLKOUT0_DUTY_CYCLE(0.5),
   .CLKOUT1_DUTY_CYCLE(0.5),
   .CLKOUT2_DUTY_CYCLE(0.5),
   .CLKOUT3_DUTY_CYCLE(0.5),
   .CLKOUT4_DUTY_CYCLE(0.5),
   .CLKOUT5_DUTY_CYCLE(0.5),
   // CLKOUT0_PHASE - CLKOUT5_PHASE: Phase offset for each CLKOUT (-360.000-360.000).
   .CLKOUT0_PHASE(0.0),
   .CLKOUT1_PHASE(0.0),
   .CLKOUT2_PHASE(0.0),
   .CLKOUT3_PHASE(0.0),
   .CLKOUT4_PHASE(0.0),
   .CLKOUT5_PHASE(0.0),
   .DIVCLK_DIVIDE(1),        // Master division value, (1-56)
   .REF_JITTER1(0.0),        // Reference input jitter in UI, (0.000-0.999).
   .STARTUP_WAIT("FALSE")    // Delay DONE until PLL Locks, ("TRUE"/"FALSE")
)
PLLE2_BASE_inst (
   // Clock Outputs: 1-bit (each) output: User configurable clock outputs
   .CLKOUT0(CLKOUT0),
   .CLKOUT1(CLKOUT1),
   .CLKOUT2(CLKOUT2),
   .CLKOUT3(CLKOUT3),
   .CLKOUT4(CLKOUT4),
   .CLKOUT5(CLKOUT5),
   // Feedback Clocks: 1-bit (each) output: Clock feedback ports
   .CLKFBOUT(CLKFBOUT), // 1-bit output: Feedback clock
   // Status Port: 1-bit (each) output: PLL status ports
   .LOCKED(LOCKED),     // 1-bit output: LOCK
   // Clock Input: 1-bit (each) input: Clock input
   .CLKIN1(CLKIN1),     // 1-bit input: Input clock
   // Control Ports: 1-bit (each) input: PLL control ports
   .PWRDWN(PWRDWN),     // 1-bit input: Power-down
   .RST(RST),           // 1-bit input: Reset
   // Feedback Clocks: 1-bit (each) input: Clock feedback ports
   .CLKFBIN(CLKFBIN)    // 1-bit input: Feedback clock
);

// End of PLLE2_BASE_inst instantiation
```

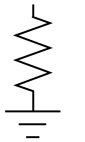
For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

PULLDOWN

Primitive: Resistor to GND for Input Pads, Open-Drain, and 3-State Outputs

PULLDOWN



Introduction

This resistor element is connected to input, output, or bidirectional pads to guarantee a logic Low level for nodes that might float.

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Pulldown output (connect directly to top level port)

Design Entry Method

Instantiation	Yes
Inference	No
CORE Generator™ and wizards	No
Macro support	No

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- PULLDOWN: I/O Buffer Weak Pull-down
--           7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

PULLDOWN_inst : PULLDOWN
port map (
   O => O     -- Pulldown output (connect directly to top-level port)
);

-- End of PULLDOWN_inst instantiation
```

Verilog Instantiation Template

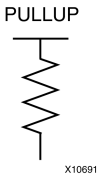
```
// PULLDOWN: I/O Buffer Weak Pull-down
//           7 Series
// Xilinx HDL Libraries Guide, version 2012.2

PULLDOWN PULLDOWN_inst (
   .O(O)     // Pulldown output (connect directly to top-level port)
);

// End of PULLDOWN_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

PULLUP

Primitive: Resistor to VCC for Input PADs, Open-Drain, and 3-State Outputs



Introduction

This design element allows for an input, 3-state output or bi-directional port to be driven to a weak high value when not being driven by an internal or external source. This element establishes a High logic level for open-drain elements and macros when all the drivers are off.

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Pullup output (connect directly to top level port)

Design Entry Method

Instantiation	Yes
Inference	No
CORE Generator™ and wizards	No
Macro support	No

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- PULLUP: I/O Buffer Weak Pull-up
--         7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

PULLUP_inst : PULLUP
port map (
   O => O     -- Pullup output (connect directly to top-level port)
);

-- End of PULLUP_inst instantiation
```

Verilog Instantiation Template

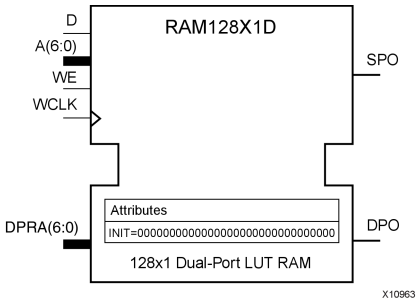
```
// PULLUP: I/O Buffer Weak Pull-up
//         7 Series
// Xilinx HDL Libraries Guide, version 2012.2

PULLUP PULLUP_inst (
   .O(O)     // Pullup output (connect directly to top-level port)
);

// End of PULLUP_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

RAM128X1D

Primitive: 128-Deep by 1-Wide Dual Port Random Access Memory (Select RAM)



Introduction

This design element is a 128-bit deep by 1-bit wide random access memory and has a read/write port that writes the value on the D input data pin when the write enable (WE) is high to the location specified by the A address bus. This happens shortly after the rising edge of the WCLK and that same value is reflected in the data output SPO. When WE is low, an asynchronous read is initiated in which the contents of the memory location specified by the A address bus is output asynchronously to the SPO output. The read port can perform asynchronous read access of the memory by changing the value of the address bus DPRA, and by outputing that value to the DPO data output.

Port Descriptions

Port	Direction	Width	Function
SPO	Output	1	Read/Write port data output addressed by A
DPO	Output	1	Read port data output addressed by DPRA
D	Input	1	Write data input addressed by A
A	Input	7	Read/Write port address bus
DPRA	Input	7	Read port address bus
WE	Input	1	Write Enable
WCLK	Input	1	Write clock (reads are asynchronous)

If instantiated, the following connections should be made to this component:

- Tie the WCLK input to the desired clock source, the D input to the data source to be stored and the DPO output to an FDCE D input or other appropriate data destination.
- Optionally, the SPO output can also be connected to the appropriate data destination or else left unconnected.
- The WE clock enable pin should be connected to the proper write enable source in the design.
- The 7-bit A bus should be connected to the source for the read/write addressing and the 7-bit DPRA bus should be connected to the appropriate read address connections.
- An optional INIT attribute consisting of a 128-bit Hexadecimal value can be specified to indicate the initial contents of the RAM.

If left unspecified, the initial contents default to all zeros.

Design Entry Method

Instantiation	Yes
Inference	Recommended
CORE Generator™ and wizards	No
Macro support	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 128-Bit Value	All zeros	Specifies the initial contents of the RAM.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- RAM128X1D: 128-deep by 1-wide positive edge write, asynchronous read
--            dual-port distributed LUT RAM (Mapped to two SliceM LUT6s)
--            7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

RAM128X1D_inst : RAM128X1D
generic map (
   INIT => X"00000000000000000000000000000000")
port map (
   DPO => DPO,     -- Read/Write port 1-bit output
   SPO => SPO,     -- Read port 1-bit output
   A => A,         -- Read/Write port 7-bit address input
   D => D,         -- RAM data input
   DPRA => DPRA,   -- Read port 7-bit address input
   WCLK => WCLK,   -- Write clock input
   WE => WE        -- RAM data input
);
```

```
-- End of RAM128X1D_inst instantiation
```

Verilog Instantiation Template

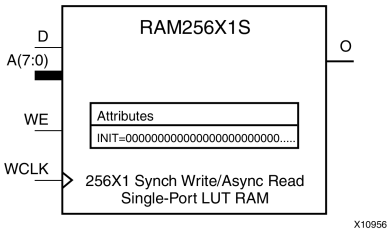
```
// RAM128X1D: 128-deep by 1-wide positive edge write, asynchronous read  (Mapped to two SliceM LUT6s)
//            dual-port distributed LUT RAM
//            7 Series
// Xilinx HDL Libraries Guide, version 2012.2

RAM128X1D #(
   .INIT(128'h00000000000000000000000000000000)
) RAM128X1D_inst (
   .DPO(DPO),   // Read port 1-bit output
   .SPO(SPO),   // Readw/rite port 1-bit output
   .A(A),       // Readw/rite port 7-bit address input
   .D(D),       // RAM data input
   .DPRA(DPRA), // Read port 7-bit address input
   .WCLK(WCLK), // Write clock input
   .WE(WE)      // Write enable input
);

// End of RAM128X1D_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

RAM256X1S

Primitive: 256-Deep by 1-Wide Random Access Memory (Select RAM)



Introduction

This design element is a 256-bit deep by 1-bit wide random access memory with synchronous write and asynchronous read capability. This RAM is implemented using the LUT resources of the device (also known as Select RAM), and does not consume any of the block RAM resources of the device. If a synchronous read capability is preferred, a register can be attached to the output and placed in the same slice as long as the same clock is used for both the RAM and the register. The RAM256X1S has an active-High write enable, WE, so that when that signal is High, and a rising edge occurs on the WCLK pin, a write is performed recording the value of the D input data pin into the memory array. The output O displays the contents of the memory location addressed by A, regardless of the WE value. When a write is performed, the output is updated to the new value shortly after the write completes.

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Read/Write port data output addressed by A
D	Input	1	Write data input addressed by A
A	Input	8	Read/Write port address bus
WE	Input	1	Write Enable
WCLK	Input	1	Write clock (reads are asynchronous)

Design Entry Method

Instantiation	Yes
Inference	Recommended
CORE Generator™ and wizards	No
Macro support	No

If instantiated, the following connections should be made to this component:

- Tie the WCLK input to the desired clock source, the D input to the data source to be stored, and the O output to an FDCE D input or other appropriate data destination.
- The WE clock enable pin should be connected to the proper write enable source in the design.
- The 8-bit A bus should be connected to the source for the read/write.
- An optional INIT attribute consisting of a 256-bit Hexadecimal value can be specified to indicate the initial contents of the RAM.

If left unspecified, the initial contents default to all zeros.

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 256-Bit Value	All zeros	Specifies the initial contents of the RAM.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- RAM256X1S: 256-deep by 1-wide positive edge write, asynchronous read
--            single-port distributed LUT RAM (Mapped to four SliceM LUT6s)
--            7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

RAM256X1S_inst : RAM256X1S
generic map (
   INIT => X"0000000000000000000000000000000000000000000000000000000000000000")
port map (
   O => O,  -- Read/Write port 1-bit output
   A => A,  -- Read/Write port 8-bit address input
   D => D,  -- RAM data input
   WCLK => WCLK,  -- Write clock input
   WE => WE -- Write enable input
);

-- End of RAM256X1S_inst instantiation
```

Verilog Instantiation Template

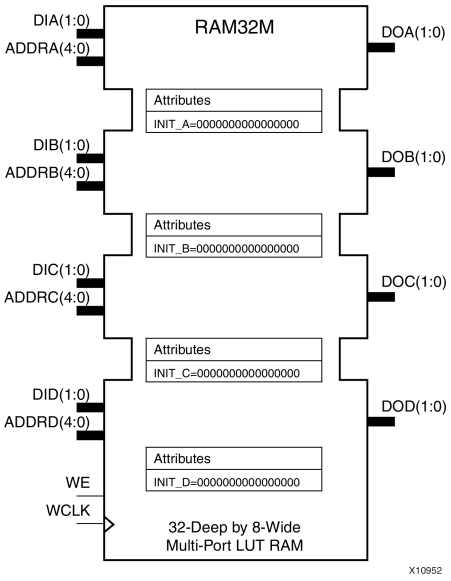
```
// RAM256X1S: 256-deep by 1-wide positive edge write, asynchronous read  (Mapped to forur SliceM LUT6s)
//            single-port distributed LUT RAM
//            7 Series
// Xilinx HDL Libraries Guide, version 2012.2

RAM256X1S #(
   .INIT(256'h0000000000000000000000000000000000000000000000000000000000000000)
) RAM256X1S_inst (
   .O(O),       // Readw/rite port 1-bit output
   .A(A),       // Readw/rite port 8-bit address input
   .WE(WE),     // Write enable input
   .WCLK(WCLK), // Write clock input
   .D(D)        // RAM data input
);

// End of RAM256X1S_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

RAM32M

Primitive: 32-Deep by 8-bit Wide Multi Port Random Access Memory (Select RAM)



Introduction

This design element is a 32-bit deep by 8-bit wide, multi-port, random access memory with synchronous write and asynchronous independent, 2-bit, wide-read capability. This RAM is implemented using the LUT resources of the device known as SelectRAM™, and does not consume any of the Block RAM resources of the device. The RAM32M is implemented in a single slice and consists of one 8-bit write, 2-bit read port and three separate 2-bit read ports from the same memory, which allows for byte-wide write and independent 2-bit read access RAM.

- If the DIA, DIB, DIC, and DID inputs are all tied to the same data inputs, the RAM can become a 1 read/write port, 3 independent read port, 32x2 quad port memory.
- If DID is grounded, DOD is not used.
- If ADDRA, ADDRB, and ADDRC are tied to the same address, the RAM becomes a 32x6 simple dual port RAM.
- If ADDRD is tied to ADDRA, ADDRB, and ADDRC, then the RAM is a 32x8 single port RAM.

There are several other possible configurations for this RAM.

Port Descriptions

Port	Direction	Width	Function
DOA	Output	2	Read port data outputs addressed by ADDRA
DOB	Output	2	Read port data outputs addressed by ADDRB
DOC	Output	2	Read port data outputs addressed by ADDRC
DOD	Output	2	Read/Write port data outputs addressed by ADDRD
DIA	Input	2	Write data inputs addressed by ADDRD (read output is addressed by ADDRA)
DIB	Input	2	Write data inputs addressed by ADDRD (read output is addressed by ADDRB)
DIC	Input	2	Write data inputs addressed by ADDRD (read output is addressed by ADDRC)
DID	Input	2	Write data inputs addressed by ADDRD
ADDRA	Input	5	Read address bus A
ADDRB	Input	5	Read address bus B
ADDRC	Input	5	Read address bus C
ADDRD	Input	5	8-bit data write port, 2-bit data read port address bus D
WE	Input	1	Write Enable
WCLK	Input	1	Write clock (reads are asynchronous)

Design Entry Method

Instantiation	Yes
Inference	Recommended
CORE Generator™ and wizards	No
Macro support	No

This element can be inferred by some synthesis tools by describing a RAM with a synchronous write and asynchronous read capability. Consult your synthesis tool documentation for details on RAM inference capabilities and coding examples. You should instantiate this component if you have a need to implicitly specify the RAM function, or if you need to manually place or relationally place the component. If a synchronous read capability is desired, the outputs can be connected to an FDRSE (FDCPE if asynchronous reset is needed) in order to improve the output timing of the function. However, this is not necessary for the proper operation of the RAM. If you want to have the data clocked on the negative edge of a clock, an inverter can be described on the clock input to this component. This inverter will be absorbed into the block giving the ability to write to the RAM on falling clock edges.

If instantiated, the following connections should be made to this component:

- Connect the WCLK input to the desired clock source, the DIA, DIB, DIC
- Connect the DIA, DIB, DIC, and DID inputs to the data source to be stored
- Connect the DOA, DOB, DOC, and DOD outputs to an FDCE D input or other appropriate data destination, or leave unconnected if not used
- Connect the WE clock enable pin to the proper write enable source in the design
- Connect the ADDRD bus to the source for the read/write addressing
- Connect the ADDRA, ADDRB, and ADDRC buses to the appropriate read address connections

The optional INIT_A, INIT_B, INIT_C and INIT_D attributes let you specify the initial memory contents of each port using a 64-bit hexadecimal value. The INIT value correlates to the RAM addressing by the following equation: ADDRy[z] = INIT_y[2*z+1:2*z]. For instance, if the RAM ADDRC port is addressed to 00001, then the INIT_C[3:2] values would be the initial values shown on the DOC port before the first write occurs at that address. If left unspecified, the initial contents will be all zeros.

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
INIT_A	Hexadecimal	Any 64-Bit Value	All zeros	Specifies the initial contents of the RAM on port A.
INIT_B	Hexadecimal	Any 64-Bit Value	All zeros	Specifies the initial contents of the RAM on port B.
INIT_C	Hexadecimal	Any 64-Bit Value	All zeros	Specifies the initial contents of the RAM on port C.
INIT_D	Hexadecimal	Any 64-Bit Value	All zeros	Specifies the initial contents of the RAM on port D.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- RAM32M: 32-deep by 8-wide Multi Port LUT RAM (Mapped to four SliceM LUT6s)
--         7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

RAM32M_inst : RAM32M
generic map (
   INIT_A => X"0000000000000000",   -- Initial contents of A port
   INIT_B => X"0000000000000000",   -- Initial contents of B port
   INIT_C => X"0000000000000000",   -- Initial contents of C port
   INIT_D => X"0000000000000000")   -- Initial contents of D port
port map (
   DOA => DOA, -- Read port A 2-bit output
   DOB => DOB, -- Read port B 2-bit output
   DOC => DOC, -- Read port C 2-bit output
   DOD => DOD, -- Read/Write port D 2-bit output
   ADDRA => ADDRA,   -- Read port A 5-bit address input
   ADDRB => ADDRB,   -- Read port B 5-bit address input
```

```
   ADDRC => ADDRC,   -- Read port C 5-bit address input
   ADDRD => ADDRD,   -- Read/Write port D 5-bit address input
   DIA => DIA, -- RAM 2-bit data write input addressed by ADDRD,
               -- read addressed by ADDRA
   DIB => DIB, -- RAM 2-bit data write input addressed by ADDRD,
               -- read addressed by ADDRB
   DIC => DIC, -- RAM 2-bit data write input addressed by ADDRD,
               -- read addressed by ADDRC
   DID => DID, -- RAM 2-bit data write input addressed by ADDRD,
               -- read addressed by ADDRD
   WCLK => WCLK,  -- Write clock input
   WE => WE       -- Write enable input
);
-- End of RAM32M_inst instantiation
```

Verilog Instantiation Template

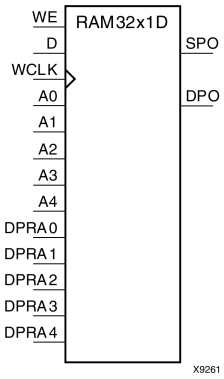
```
// RAM32M: 32-deep by 8-wide Multi Port LUT RAM (Mapped to forur SliceM LUT6s)
//         7 Series
// Xilinx HDL Libraries Guide, version 2012.2

RAM32M #(
   .INIT_A(64'h0000000000000000), // Initial contents of A Port
   .INIT_B(64'h0000000000000000), // Initial contents of B Port
   .INIT_C(64'h0000000000000000), // Initial contents of C Port
   .INIT_D(64'h0000000000000000)  // Initial contents of D Port
) RAM32M_inst (
   .DOA(DOA),     // Read port A 2-bit output
   .DOB(DOB),     // Read port B 2-bit output
   .DOC(DOC),     // Read port C 2-bit output
   .DOD(DOD),     // Readw/rite port D 2-bit output
   .ADDRA(ADDRA), // Read port A 5-bit address input
   .ADDRB(ADDRB), // Read port B 5-bit address input
   .ADDRC(ADDRC), // Read port C 5-bit address input
   .ADDRD(ADDRD), // Readw/rite port D 5-bit address input
   .DIA(DIA),     // RAM 2-bit data write input addressed by ADDRD,
                  //   read addressed by ADDRA
   .DIB(DIB),     // RAM 2-bit data write input addressed by ADDRD,
                  //   read addressed by ADDRB
   .DIC(DIC),     // RAM 2-bit data write input addressed by ADDRD,
                  //   read addressed by ADDRC
   .DID(DID),     // RAM 2-bit data write input addressed by ADDRD,
                  //   read addressed by ADDRD
   .WCLK(WCLK),   // Write clock input
   .WE(WE)        // Write enable input
);

// End of RAM32M_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

RAM32X1D

Primitive: 32-Deep by 1-Wide Static Dual Port Synchronous RAM



Introduction

The design element is a 32-word by 1-bit static dual port random access memory with synchronous write capability. The device has two separate address ports: the read address (DPRA4:DPRA0) and the write address (A4:A0). These two address ports are completely asynchronous. The read address controls the location of the data driven out of the output pin (DPO), and the write address controls the destination of a valid write transaction. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data input (D) into the word selected by the 5-bit write address. For predictable performance, write address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block. You can initialize RAM32X1D during configuration using the INIT attribute. Mode selection is shown in the following logic table.

The SPO output reflects the data in the memory cell addressed by A4:A0. The DPO output reflects the data in the memory cell addressed by DPRA4:DPRA0. The write process is not affected by the address on the read address port.

Logic Table

Inputs			Outputs	
WE (Mode)	**WCLK**	**D**	**SPO**	**DPO**
0 (read)	X	X	data_a	data_d
1 (read)	0	X	data_a	data_d
1 (read)	1	X	data_a	data_d
1 (write)	↑	D	D	data_d
1 (read)	↓	X	data_a	data_d

Design Entry Method

Instantiation	Yes
Inference	Recommended
CORE Generator™ and wizards	No
Macro support	No

Available Attributes

Attribute	Data Type	Allowed Values	Default	Descriptions
INIT	Hexadecimal	Any 32-Bit Value	All Zeros	Initializes ROMs, RAMs, registers, and look-up tables.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- RAM32X1D: 32 x 1 positive edge write, asynchronous read
--              dual-port distributed RAM (Mapped to SliceM LUT6)
--              7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

RAM32X1D_inst : RAM32X1D
generic map (
   INIT => X"00000000") -- Initial contents of RAM
port map (
   DPO => DPO,     -- Read-only 1-bit data output
   SPO => SPO,     -- R/W 1-bit data output
   A0 => A0,       -- R/W address[0] input bit
   A1 => A1,       -- R/W address[1] input bit
   A2 => A2,       -- R/W address[2] input bit
   A3 => A3,       -- R/W address[3] input bit
   A4 => A4,       -- R/W address[4] input bit
   D => D,         -- Write 1-bit data input
   DPRA0 => DPRA0, -- Read-only address[0] input bit
   DPRA1 => DPRA1, -- Read-only address[1] input bit
   DPRA2 => DPRA2, -- Read-only address[2] input bit
   DPRA3 => DPRA3, -- Read-only address[3] input bit
   DPRA4 => DPRA4, -- Read-only address[4] input bit
   WCLK => WCLK,   -- Write clock input
   WE => WE        -- Write enable input
);

-- End of RAM32X1D_inst instantiation
```

Verilog Instantiation Template

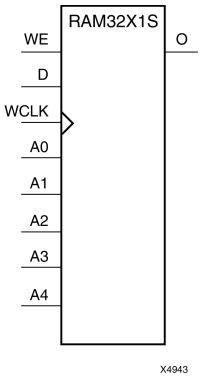
```
// RAM32X1D: 32 x 1 positive edge write, asynchronous read dual-port distributed RAM (Mapped to a SliceM LUT6
//           7 Series
// Xilinx HDL Libraries Guide, version 2012.2

RAM32X1D #(
   .INIT(32'h00000000) // Initial contents of RAM
) RAM32X1D_inst (
   .DPO(DPO),     // Read-only 1-bit data output
   .SPO(SPO),     // Rw/ 1-bit data output
   .A0(A0),       // Rw/ address[0] input bit
   .A1(A1),       // Rw/ address[1] input bit
   .A2(A2),       // Rw/ address[2] input bit
   .A3(A3),       // Rw/ address[3] input bit
   .A4(A4),       // Rw/ address[4] input bit
   .D(D),         // Write 1-bit data input
   .DPRA0(DPRA0), // Read-only address[0] input bit
   .DPRA1(DPRA1), // Read-only address[1] input bit
   .DPRA2(DPRA2), // Read-only address[2] input bit
   .DPRA3(DPRA3), // Read-only address[3] input bit
   .DPRA4(DPRA4), // Read-only address[4] input bit
   .WCLK(WCLK),   // Write clock input
   .WE(WE)        // Write enable input
);

// End of RAM32X1D_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

RAM32X1S

Primitive: 32-Deep by 1-Wide Static Synchronous RAM



Introduction

The design element is a 32-word by 1-bit static random access memory with synchronous write capability. When the write enable is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When (WE) is High, any positive transition on (WCLK) loads the data on the data input (D) into the word selected by the 5-bit address (A4-A0). For predictable performance, address and data inputs must be stable before a Low-to-High (WCLK) transition. This RAM block assumes an active-High (WCLK). However, (WCLK) can be active-High or active-Low. Any inverter placed on the (WCLK) input net is absorbed into the block.

The signal output on the data output pin (O) is the data that is stored in the RAM at the location defined by the values on the address pins. You can initialize RAM32X1S during configuration using the INIT attribute.

Logic Table

Inputs			Outputs
WE (Mode)	**WCLK**	**D**	**O**
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↑	D	D
1 (read)	↓	X	Data

Design Entry Method

Instantiation	Yes
Inference	Recommended
CORE Generator™ and wizards	No
Macro support	No

Available Attributes

Attribute	Data Type	Allowed Values	Default	Descriptions
INIT	Hexadecimal	Any 32-Bit Value	All zeros	Specifies initial contents of the RAM.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- RAM32X1S: 32 x 1 posedge write distributed (LUT) RAM (Mapped to SliceM LUT6)
--           7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

RAM32X1S_inst : RAM32X1S
generic map (
   INIT => X"00000000")
port map (
   O => O,       -- RAM output
   A0 => A0,     -- RAM address[0] input
   A1 => A1,     -- RAM address[1] input
   A2 => A2,     -- RAM address[2] input
   A3 => A3,     -- RAM address[3] input
   A4 => A4,     -- RAM address[4] input
   D => D,       -- RAM data input
   WCLK => WCLK, -- Write clock input
   WE => WE      -- Write enable input
);

-- End of RAM32X1S_inst instantiation
```

Verilog Instantiation Template

```
// RAM32X1S: 32 x 1 posedge write distributed (LUT) RAM (Mapped to a SliceM LUT6)
//           7 Series
// Xilinx HDL Libraries Guide, version 2012.2

RAM32X1S #(
   .INIT(32'h00000000)  // Initial contents of RAM
) RAM32X1S_inst (
   .O(O),       // RAM output
   .A0(A0),     // RAM address[0] input
   .A1(A1),     // RAM address[1] input
   .A2(A2),     // RAM address[2] input
   .A3(A3),     // RAM address[3] input
   .A4(A4),     // RAM address[4] input
   .D(D),       // RAM data input
   .WCLK(WCLK), // Write clock input
   .WE(WE)      // Write enable input
```

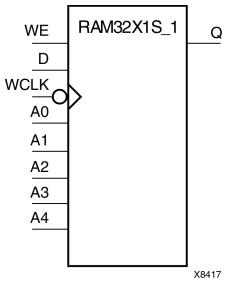
```
);
// End of RAM32X1S_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

RAM32X1S_1

Primitive: 32-Deep by 1-Wide Static Synchronous RAM with Negative-Edge Clock



Introduction

The design element is a 32-word by 1-bit static random access memory with synchronous write capability. When the write enable is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When (WE) is High, any negative transition on (WCLK) loads the data on the data input (D) into the word selected by the 5-bit address (A4:A0). For predictable performance, address and data inputs must be stable before a High-to-Low (WCLK) transition. This RAM block assumes an active-Low (WCLK). However, (WCLK) can be active-High or active-Low. Any inverter placed on the (WCLK) input net is absorbed into the block.

The signal output on the data output pin (O) is the data that is stored in the RAM at the location defined by the values on the address pins. You can initialize RAM32X1S_1 during configuration using the INIT attribute.

Logic Table

Inputs			Outputs
WE (Mode)	**WCLK**	**D**	**O**
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↓	D	D
1 (read)	↑	X	Data
Data = word addressed by bits A4:A0			

Design Entry Method

Instantiation	Yes
Inference	Recommended
CORE Generator™ and wizards	No
Macro support	No

Available Attributes

Attribute	Data Type	Allowed Values	Default	Descriptions
INIT	Hexadecimal	Any 32-Bit Value	0	Initializes RAMs, registers, and look-up tables.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- RAM32X1S_1: 32 x 1 negedge write distributed (LUT) RAM (Mapped to SliceM LUT6)
--             7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

RAM32X1S_1_inst : RAM32X1S_1
generic map (
   INIT => X"00000000")
port map (
   O => O,       -- RAM output
   A0 => A0,     -- RAM address[0] input
   A1 => A1,     -- RAM address[1] input
   A2 => A2,     -- RAM address[2] input
   A3 => A3,     -- RAM address[3] input
   A4 => A4,     -- RAM address[4] input
   D => D,       -- RAM data input
   WCLK => WCLK, -- Write clock input
   WE => WE      -- Write enable input
);

-- End of RAM32X1S_1_inst instantiation
```

Verilog Instantiation Template

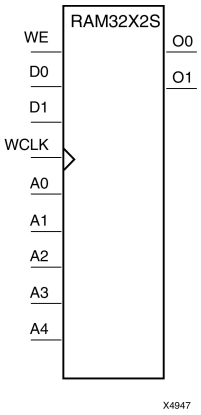
```
// RAM32X1S_1: 32 x 1 negedge write distributed (LUT) RAM (Mapped to a SliceM LUT6)
//             7 Series
// Xilinx HDL Libraries Guide, version 2012.2

RAM32X1S_1 #(
   .INIT(32'h00000000)  // Initial contents of RAM
)RAM32X1S_1_inst (
   .O(O),       // RAM output
   .A0(A0),     // RAM address[0] input
   .A1(A1),     // RAM address[1] input
   .A2(A2),     // RAM address[2] input
   .A3(A3),     // RAM address[3] input
   .A4(A4),     // RAM address[4] input
   .D(D),       // RAM data input
   .WCLK(WCLK), // Write clock input
   .WE(WE)      // Write enable input
);

// End of RAM32X1S_1_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

RAM32X2S

Primitive: 32-Deep by 2-Wide Static Synchronous RAM



Introduction

The design element is a 32-word by 2-bit static random access memory with synchronous write capability. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When (WE) is High, any positive transition on (WCLK) loads the data on the data input (D1-D0) into the word selected by the 5-bit address (A4-A0). For predictable performance, address and data inputs must be stable before a Low-to-High (WCLK) transition. This RAM block assumes an active-High (WCLK). However, (WCLK) can be active-High or active-Low. Any inverter placed on the (WCLK) input net is absorbed into the block. The signal output on the data output pins (O1-O0) is the data that is stored in the RAM at the location defined by the values on the address pins.

You can use the INIT_00 and INIT_01 properties to specify the initial contents of RAM32X2S.

Logic Table

Inputs			Outputs
WE (Mode)	**WCLK**	**D**	**O0-O1**
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↑	D1:D0	D1:D0
1 (read)	↓	X	Data
Data = word addressed by bits A4:A0			

Design Entry Method

Instantiation	Yes
Inference	Recommended
CORE Generator™ and wizards	No
Macro support	No

Available Attributes

Attribute	Data Type	Allowed Values	Default	Descriptions
INIT_00	Hexadecimal	Any 32-Bit Value	All zeros	INIT for bit 0 of RAM.
INIT_01	Hexadecimal	Any 32-Bit Value	All zeros	INIT for bit 1 of RAM.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- RAM32X2S: 32 x 2 posedge write distributed (LUT) RAM (Mapped to SliceM LUT6)
--           7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

RAM32X2S_inst : RAM32X2S
generic map (
   INIT_00 => X"00000000", --  INIT for bit 0 of RAM
   INIT_01 => X"00000000") --  INIT for bit 1 of RAM
port map (
   O0 => O0,     -- RAM data[0] output
   O1 => O1,     -- RAM data[1] output
   A0 => A0,     -- RAM address[0] input
   A1 => A1,     -- RAM address[1] input
   A2 => A2,     -- RAM address[2] input
   A3 => A3,     -- RAM address[3] input
   A4 => A4,     -- RAM address[4] input
   D0 => D0,     -- RAM data[0] input
   D1 => D1,     -- RAM data[1] input
   WCLK => WCLK, -- Write clock input
   WE => WE      -- Write enable input
);

-- End of RAM32X2S_inst instantiation
```

Verilog Instantiation Template

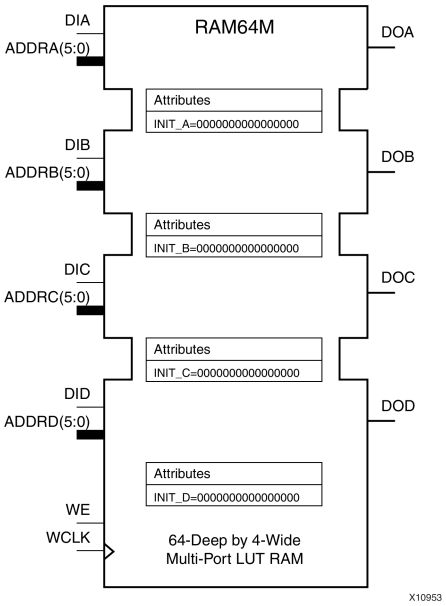
```
// RAM32X2S: 32 x 2 posedge write distributed (LUT) RAM (Mapped to a SliceM LUT6)
//           7 Series
// Xilinx HDL Libraries Guide, version 2012.2

RAM32X2S #(
   .INIT_00(32'h00000000), // INIT forr bit 0 of RAM
   .INIT_01(32'h00000000)  // INIT forr bit 1 of RAM
) RAM32X2S_inst (
   .O0(O0),     // RAM data[0] output
   .O1(O1),     // RAM data[1] output
   .A0(A0),     // RAM address[0] input
   .A1(A1),     // RAM address[1] input
   .A2(A2),     // RAM address[2] input
   .A3(A3),     // RAM address[3] input
   .A4(A4),     // RAM address[4] input
   .D0(D0),     // RAM data[0] input
   .D1(D1),     // RAM data[1] input
   .WCLK(WCLK), // Write clock input
   .WE(WE)      // Write enable input
);

// End of RAM32X2S_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

RAM64M

Primitive: 64-Deep by 4-bit Wide Multi Port Random Access Memory (Select RAM)



Introduction

This design element is a 64-bit deep by 4-bit wide, multi-port, random access memory with synchronous write and asynchronous independent bit wide read capability. This RAM is implemented using the LUT resources of the device (also known as SelectRAM™) and does not consume any of the block RAM resources of the device. The RAM64M component is implemented in a single slice, and consists of one 4-bit write, 1-bit read port, and three separate 1-bit read ports from the same memory allowing for 4-bit write and independent bit read access RAM.

- If the DIA, DIB, DIC, and DID inputs are all tied to the same data inputs, the RAM can become a 1 read/write port, 3 independent read port 64x1 quad port memory.
- If DID is grounded, DOD is not used.
- If ADDRA, ADDRB, and ADDRC are tied to the same address, the RAM becomes a 64x3 simple dual port RAM.
- If ADDRD is tied to ADDRA, ADDRB, and ADDRC, the RAM is a 64x4 single port RAM.

There are several other possible configurations for this RAM.

Port Descriptions

Port	Direction	Width	Function
DOA	Output	1	Read port data outputs addressed by ADDRA
DOB	Output	1	Read port data outputs addressed by ADDRB
DOC	Output	1	Read port data outputs addressed by ADDRC
DOD	Output	1	Read/Write port data outputs addressed by ADDRD
DIA	Input	1	Write data inputs addressed by ADDRD (read output is addressed by ADDRA)
DIB	Input	1	Write data inputs addressed by ADDRD (read output is addressed by ADDRB)
DIC	Input	1	Write data inputs addressed by ADDRD (read output is addressed by ADDRC)
DID	Input	1	Write data inputs addressed by ADDRD
ADDRA	Input	6	Read address bus A
ADDRB	Input	6	Read address bus B
ADDRC	Input	6	Read address bus C
ADDRD	Input	6	4-bit data write port, 1-bit data read port address bus D
WE	Input	1	Write Enable
WCLK	Input	1	Write clock (reads are asynchronous)

Design Entry Method

Instantiation	Yes
Inference	Recommended
CORE Generator™ and wizards	No
Macro support	No

This element can be inferred by some synthesis tools by describing a RAM with a synchronous write and asynchronous read capability. Consult your synthesis tool documentation for details on RAM inference capabilities and coding examples. Xilinx suggests that you instantiate this component if you have a need to implicitly specify the RAM function, or if you need to manually place or relationally place the component. If a synchronous read capability is desired, the outputs can be connected to an FDRE (FDCE if asynchronous reset is needed) in order to improve the output timing of the function. However, this is not necessary for the proper operation of the RAM. If you want to have the data clocked on the negative edge of a clock, an inverter can be described on the clock input to this component. This inverter will be absorbed into the block giving the ability to write to the RAM on falling clock edges.

If instantiated, the following connections should be made to this component:

- Connect the WCLK input to the desired clock source, the DIA, DIB, DIC
- Connect the DIA, DIB, DIC, and DID inputs to the data source to be stored
- Connect the DOA, DOB, DOC, and DOD outputs to an FDCE D input or other appropriate data destination, or leave unconnected if not used
- Connect the WE clock enable pin to the proper write enable source in the design
- Connect the ADDRD bus to the source for the read/write addressing
- Connect the ADDRA, ADDRB, and ADDRC buses to the appropriate read address connections

The optional INIT_A, INIT_B, INIT_C and INIT_D attributes let you specify the initial memory contents of each port using a 64-bit hexadecimal value. The INIT value correlates to the RAM addressing by the following equation: ADDRy[z] = INIT_y[z]. For instance, if the RAM ADDRC port is addressed to 00001, then the INIT_C[1] values would be the initial values shown on the DOC port before the first write occurs at that address. If left unspecified, the initial contents will default to all zeros.

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
INIT_A	Hexadecimal	Any 64-Bit Value	All zero	Specifies the initial contents of the RAM on port A.
INIT_B	Hexadecimal	Any 64-Bit Value	All zero	Specifies the initial contents of the RAM on port B.
INIT_C	Hexadecimal	Any 64-Bit Value	All zero	Specifies the initial contents of the RAM on port C.
INIT_D	Hexadecimal	Any 64-Bit Value	All zero	Specifies the initial contents of the RAM on port D.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- RAM64M: 64-deep by 4-wide Multi Port LUT RAM (Mapped to four SliceM LUT6s)
--         7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

RAM64M_inst : RAM64M
generic map (
   INIT_A => X"0000000000000000",   -- Initial contents of A port
   INIT_B => X"0000000000000000",   -- Initial contents of B port
   INIT_C => X"0000000000000000",   -- Initial contents of C port
   INIT_D => X"0000000000000000")    -- Initial contents of D port
port map (
   DOA => DOA, -- Read port A 1-bit output
   DOB => DOB, -- Read port B 1-bit output
   DOC => DOC, -- Read port C 1-bit output
   DOD => DOD, -- Read/Write port D 1-bit output
```

```
   ADDRA => ADDRA,   -- Read port A 6-bit address input
   ADDRB => ADDRB,   -- Read port B 6-bit address input
   ADDRC => ADDRC,   -- Read port C 6-bit address input
   ADDRD => ADDRD,   -- Read/Write port D 6-bit address input
   DIA => DIA, -- RAM 1-bit data write input addressed by ADDRD,
               -- read addressed by ADDRA
   DIB => DIB, -- RAM 1-bit data write input addressed by ADDRD,
               -- read addressed by ADDRB
   DIC => DIC, -- RAM 1-bit data write input addressed by ADDRD,
               -- read addressed by ADDRC
   DID => DID, -- RAM 1-bit data write input addressed by ADDRD,
               -- read addressed by ADDRD
   WCLK => WCLK,  -- Write clock input
   WE => WE       -- Write enable input
);
-- End of RAM64M_inst instantiation
```

Verilog Instantiation Template

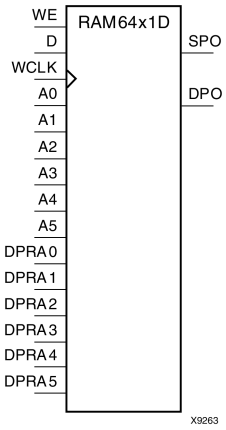
```
// RAM64M: 64-deep by 4-wide Multi Port LUT RAM (Mapped to forur SliceM LUT6s)
//         7 Series
// Xilinx HDL Libraries Guide, version 2012.2

RAM64M #(
   .INIT_A(64'h0000000000000000), // Initial contents of A Port
   .INIT_B(64'h0000000000000000), // Initial contents of B Port
   .INIT_C(64'h0000000000000000), // Initial contents of C Port
   .INIT_D(64'h0000000000000000)  // Initial contents of D Port
) RAM64M_inst (
   .DOA(DOA),     // Read port A 1-bit output
   .DOB(DOB),     // Read port B 1-bit output
   .DOC(DOC),     // Read port C 1-bit output
   .DOD(DOD),     // Readw/rite port D 1-bit output
   .DIA(DIA),     // RAM 1-bit data write input addressed by ADDRD,
                  //   read addressed by ADDRA
   .DIB(DIB),     // RAM 1-bit data write input addressed by ADDRD,
                  //   read addressed by ADDRB
   .DIC(DIC),     // RAM 1-bit data write input addressed by ADDRD,
                  //   read addressed by ADDRC
   .DID(DID),     // RAM 1-bit data write input addressed by ADDRD,
                  //   read addressed by ADDRD
   .ADDRA(ADDRA), // Read port A 6-bit address input
   .ADDRB(ADDRB), // Read port B 6-bit address input
   .ADDRC(ADDRC), // Read port C 6-bit address input
   .ADDRD(ADDRD), // Readw/rite port D 6-bit address input
   .WE(WE),       // Write enable input
   .WCLK(WCLK)    // Write clock input
);

// End of RAM64M_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

RAM64X1D

Primitive: 64-Deep by 1-Wide Dual Port Static Synchronous RAM



Introduction

This design element is a 64-word by 1-bit static dual port random access memory with synchronous write capability. The device has two separate address ports: the read address (DPRA5:DPRA0) and the write address (A5:A0). These two address ports are completely asynchronous. The read address controls the location of the data driven out of the output pin (DPO), and the write address controls the destination of a valid write transaction. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected.

When WE is High, any positive transition on WCLK loads the data on the data input (D) into the word selected by the 6-bit (A0:A5) write address. For predictable performance, write address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The SPO output reflects the data in the memory cell addressed by A5:A0. The DPO output reflects the data in the memory cell addressed by DPRA5:DPRA0.

Note The write process is not affected by the address on the read address port.

Logic Table

Inputs			Outputs	
WE (mode)	**WCLK**	**D**	**SPO**	**DPO**
0 (read)	X	X	data_a	data_d
1 (read)	0	X	data_a	data_d
1 (read)	1	X	data_a	data_d
1 (write)	↑	D	D	data_d
1 (read)	↓	X	data_a	data_d

Inputs			Outputs	
WE (mode)	**WCLK**	**D**	**SPO**	**DPO**
data_a = word addressed by bits A5:A0 data_d = word addressed by bits DPRA5:DPRA0				

Design Entry Method

Instantiation	Yes
Inference	Recommended
CORE Generator™ and wizards	No
Macro support	No

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 64-Bit Value	All zeros	Initializes RAMs, registers, and look-up tables.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- RAM64X1D: 64 x 1 negative edge write, asynchronous read
--           dual-port distributed RAM (Mapped to SliceM LUT6)
--           7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

RAM64X1D_1_inst : RAM64X1D_1
generic map (
   INIT => X"0000000000000000") -- Initial contents of RAM
port map (
   DPO => DPO,     -- Read-only 1-bit data output
   SPO => SPO,     -- R/W 1-bit data output
   A0 => A0,       -- R/W address[0] input bit
   A1 => A1,       -- R/W address[1] input bit
   A2 => A2,       -- R/W address[2] input bit
   A3 => A3,       -- R/W address[3] input bit
   A4 => A4,       -- R/W address[4] input bit
   A5 => A5,       -- R/W address[5] input bit
   D => D,         -- Write 1-bit data input
   DPRA0 => DPRA0, -- Read-only address[0] input bit
   DPRA1 => DPRA1, -- Read-only address[1] input bit
   DPRA2 => DPRA2, -- Read-only address[2] input bit
   DPRA3 => DPRA3, -- Read-only address[3] input bit
   DPRA4 => DPRA4, -- Read-only address[4] input bit
   DPRA5 => DPRA5, -- Read-only address[5] input bit
   WCLK => WCLK,   -- Write clock input
   WE => WE        -- Write enable input
);

-- End of RAM64X1D_1_inst instantiation
```

Verilog Instantiation Template

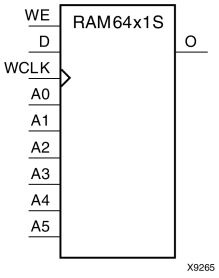
```
// RAM64X1D: 64 x 1 positive edge write, asynchronous read dual-port distributed RAM (Mapped to a SliceM LUT6
//           7 Series
// Xilinx HDL Libraries Guide, version 2012.2

RAM64X1D #(
   .INIT(64'h0000000000000000) // Initial contents of RAM
) RAM64X1D_inst (
   .DPO(DPO),     // Read-only 1-bit data output
   .SPO(SPO),     // Rw/ 1-bit data output
   .A0(A0),       // Rw/ address[0] input bit
   .A1(A1),       // Rw/ address[1] input bit
   .A2(A2),       // Rw/ address[2] input bit
   .A3(A3),       // Rw/ address[3] input bit
   .A4(A4),       // Rw/ address[4] input bit
   .A5(A5),       // Rw/ address[5] input bit
   .D(D),         // Write 1-bit data input
   .DPRA0(DPRA0), // Read-only address[0] input bit
   .DPRA1(DPRA1), // Read-only address[1] input bit
   .DPRA2(DPRA2), // Read-only address[2] input bit
   .DPRA3(DPRA3), // Read-only address[3] input bit
   .DPRA4(DPRA4), // Read-only address[4] input bit
   .DPRA5(DPRA5), // Read-only address[5] input bit
   .WCLK(WCLK),   // Write clock input
   .WE(WE)        // Write enable input
);

// End of RAM64X1D_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

RAM64X1S

Primitive: 64-Deep by 1-Wide Static Synchronous RAM



Introduction

This design element is a 64-word by 1-bit static random access memory (RAM) with synchronous write capability. When the write enable is set Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is set High, any positive transition on WCLK loads the data on the data input (D) into the word selected by the 6-bit address (A5:A0). This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pin (O) is the data that is stored in the RAM at the location defined by the values on the address pins.

You can initialize this element during configuration using the INIT attribute.

Logic Table

Mode selection is shown in the following logic table

Inputs			Outputs
WE (mode)	**WCLK**	**D**	**O**
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↑	D	D
1 (read)	↓	X	Data
Data = word addressed by bits A5:A0			

Design Entry Method

Instantiation	Yes
Inference	Recommended
CORE Generator™ and wizards	No
Macro support	No

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 64-Bit Value	All zeros	Initializes ROMs, RAMs, registers, and look-up tables.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- RAM64X1S: 64 x 1 positive edge write, asynchronous read single-port distributed RAM (Mapped to SliceM LUT6
--           7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

RAM64X1S_inst : RAM64X1S
generic map (
   INIT => X"0000000000000000")
port map (
   O => O,         -- 1-bit data output
   A0 => A0,       -- Address[0] input bit
   A1 => A1,       -- Address[1] input bit
   A2 => A2,       -- Address[2] input bit
   A3 => A3,       -- Address[3] input bit
   A4 => A4,       -- Address[4] input bit
   A5 => A5,       -- Address[5] input bit
   D => D,         -- 1-bit data input
   WCLK => WCLK,   -- Write clock input
   WE => WE        -- Write enable input
);

-- End of RAM64X1S_inst instantiation
```

Verilog Instantiation Template

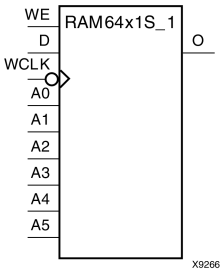
```
// RAM64X1S: 64 x 1 positive edge write, asynchronous read single-port distributed RAM (Mapped to a SliceM LUT6)
//           7 Series
// Xilinx HDL Libraries Guide, version 2012.2

RAM64X1S #(
   .INIT(64'h0000000000000000) // Initial contents of RAM
) RAM64X1S_inst (
   .O(O),         // 1-bit data output
   .A0(A0),       // Address[0] input bit
   .A1(A1),       // Address[1] input bit
   .A2(A2),       // Address[2] input bit
   .A3(A3),       // Address[3] input bit
   .A4(A4),       // Address[4] input bit
   .A5(A5),       // Address[5] input bit
   .D(D),         // 1-bit data input
   .WCLK(WCLK),   // Write clock input
   .WE(WE)        // Write enable input
);

// End of RAM64X1S_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

RAM64X1S_1

Primitive: 64-Deep by 1-Wide Static Synchronous RAM with Negative-Edge Clock



Introduction

This design element is a 64-word by 1-bit static random access memory with synchronous write capability. When the write enable is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When (WE) is High, any negative transition on (WCLK) loads the data on the data input (D) into the word selected by the 6-bit address (A5:A0). For predictable performance, address and data inputs must be stable before a High-to-Low (WCLK) transition. This RAM block assumes an active-Low (WCLK). However, (WCLK) can be active-High or active-Low. Any inverter placed on the (WCLK) input net is absorbed into the block.

The signal output on the data output pin (O) is the data that is stored in the RAM at the location defined by the values on the address pins.

You can initialize this element during configuration using the INIT attribute.

Logic Table

Inputs			Outputs
WE (mode)	**WCLK**	**D**	**O**
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↓	D	D
1 (read)	↑	X	Data
Data = word addressed by bits A5:A0			

Design Entry Method

Instantiation	Yes
Inference	Recommended
CORE Generator™ and wizards	No
Macro support	No

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 64-Bit Value	All zeros	Initializes ROMs, RAMs, registers, and look-up tables.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- RAM64X1S_1: 64 x 1 negative edge write, asynchronous read single-port distributed RAM (Mapped to SliceM LUT6)
--             7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

RAM64X1S_1_inst : RAM64X1S_1
generic map (
   INIT => X"0000000000000000")
port map (
   O => O,         -- 1-bit data output
   A0 => A0,       -- Address[0] input bit
   A1 => A1,       -- Address[1] input bit
   A2 => A2,       -- Address[2] input bit
   A3 => A3,       -- Address[3] input bit
   A4 => A4,       -- Address[4] input bit
   A5 => A5,       -- Address[5] input bit
   D => D,         -- 1-bit data input
   WCLK => WCLK,   -- Write clock input
   WE => WE        -- Write enable input
);

-- End of RAM64X1S_1_inst instantiation
```

Verilog Instantiation Template

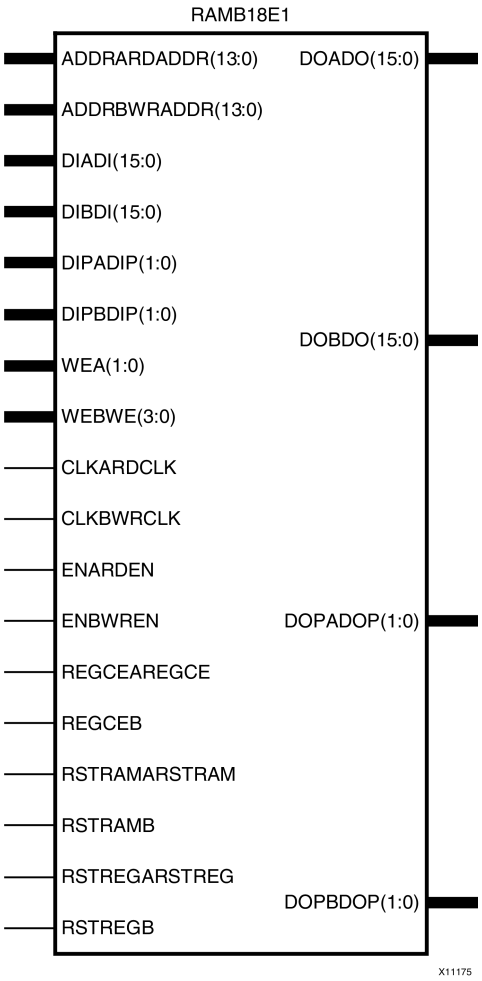
```
// RAM64X1S_1: 64 x 1 negative edge write, asynchronous read single-port distributed RAM (Mapped to a SliceM LUT6)
//             7 Series
// Xilinx HDL Libraries Guide, version 2012.2

RAM64X1S_1 #(
   .INIT(64'h0000000000000000) // Initial contents of RAM
) RAM64X1S_1_inst (
   .O(O),         // 1-bit data output
   .A0(A0),       // Address[0] input bit
   .A1(A1),       // Address[1] input bit
   .A2(A2),       // Address[2] input bit
   .A3(A3),       // Address[3] input bit
   .A4(A4),       // Address[4] input bit
   .A5(A5),       // Address[5] input bit
   .D(D),         // 1-bit data input
   .WCLK(WCLK),   // Write clock input
   .WE(WE)        // Write enable input
);

// End of RAM64X1S_1_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

RAMB18E1

Primitive: 18K-bit Configurable Synchronous Block RAM



Introduction

7 series devices contain several block RAM memories that can be configured as FIFOs, automatic error correction RAM, or general-purpose 36KB or 18KB RAM/ROM memories. These block RAM memories offer fast and flexible storage of large amounts of on-chip data. The RAMB18E1 allows access to the block RAM in the 18KB configuration. This element can be configured and used as a 1-bit wide by 16K deep to an 18-bit wide by 1024-bit deep true dual port RAM. This element can also be configured as a 36-bit wide by 512 deep simple dual port RAM. Both read and write operations are fully synchronous to the supplied clock(s) to the component. However, the READ and WRITE ports can operate fully independent and asynchronous to each other, accessing the same memory array. When configured in the wider data width modes, byte-enable write operations are possible, and an optional output register can be used to reduce the clock-to-out times of the RAM.

Port Descriptions

Port	Type	Width	Function
ADDRARDADDR <13:0>	Input	14	Port A address input bus/Read address input bus.
ADDRBWRADDR <13:0>	Input	14	Port B address input bus/Write address input bus.
CLKARDCLK	Input	1	Rising edge port A clock input/Read clock input.
CLKBWRCLK	Input	1	Rising edge port B clock input/Write clock input.
DIADI<15:0>	Input	16	Port A data input bus/Data input bus addressed by WRADDR. When RAM_MODE="SDP", DIADI is the logical DI<15:0>.
DIBDI<15:0>	Input	16	Port B data input bus/Data input bus addressed by WRADDR. When RAM_MODE="SDP", DIBDI is the logical DI<31:16>.
DIPADIP<1:0>	Input	2	Port A parity data input bus/Data parity input bus addressed by WRADDR. When RAM_MODE="SDP", DIPADIP is the logical DIP<1:0>.
DIPBDIP<1:0>	Input	2	Port B parity data input bus/Data parity input bus addressed by WRADDR. When RAM_MODE="SDP", DIPBDIP is the logical DIP<3:2>.
DOADO<15:0>	Output	16	Port A data output bus/Data output bus addressed by RDADDR. When RAM_MODE="SDP", DOADO is the logical DO<15:0>.
DOBDO<15:0>	Output	16	Port B data output bus/Data output bus addressed by RDADDR. When RAM_MODE="SDP", DOBDO is the logical DO<31:16>.
DOPADOP<1:0>	Output	2	Port A parity data output bus/Data parity output bus addressed by RDADDR. When RAM_MODE="SDP", DOPADOP is the logical DOP<1:0>.
DOPBDOP<1:0>	Output	2	Port B parity data output bus/Data parity output bus addressed by RDADDR. When RAM_MODE="SDP", DOPBDOP is the logical DOP<3:2>.
ENARDEN	Input	1	Port A RAM enable/Read enable.
ENBWREN	Input	1	Port B RAM enable/Write enable.
REGCEAREGCE	Input	1	Port A output register clock enable input/Output register clock enable input (valid only when DOA_REG=1).
REGCEB	Input	1	Port B output register clock enable (valid only when DOB_REG=1 and RAM_MODE="TDP").
RSTRAMARSTR AM	Input	1	Synchronous data latch set/reset to value indicated by SRVAL_A. RSTRAMARSTRAM sets/resets the BRAM data output latch when DO_REG=0 or 1. If DO_REG=1 there is a cycle of latency between the internal data latch node that is reset by RSTRAMARSTRAM and the DO output of the BRAM. This signal resets port A RAM output when RAM_MODE="TDP" and the entire RAM output when RAM_MODE="SDP".

Port	Type	Width	Function
RSTRAMB	Input	1	Synchronous data latch set/reset to value indicated by SRVAL_B. RSTRAMB sets/resets the BRAM data output latch when DO_REG=0 or 1. If DO_REG=1 there is a cycle of latency between the internal data latch node that is reset by RSTRAMB and the DO output of the BRAM. Not used when RAM_MODE="SDP".
RSTREGARSTR EG	Input	1	Synchronous output register set/reset to value indicated by SRVAL_A. RSTREGARSTREG sets/resets the output register when DO_REG=1. RSTREG_PRIORITY_A determines if this signal gets priority over REGCEAREGCE. This signal resets port A output when RAM_MODE="TDP" and the entire output port when RAM_MODE="SDP".
RSTREGB	Input	1	Synchronous output register set/reset to value indicated by SRVAL_B. RSTREGB sets/resets the output register when DO_REG=1. RSTREG_PRIORITY_B determines if this signal gets priority over REGCEB. Not used when RAM_MODE="SDP".
WEA<1:0>	Input	2	Port A byte-wide write enable. Not used when RAM_MODE="SDP". See User Guide for WEA mapping for different port widths.
WEBWE<3:0>	Input	4	Port B byte-wide write enable/Write enable. See User Guide for WEBWE mapping for different port widths.

Design Entry Method

Instantiation	Yes
Inference	Recommended
CORE Generator™ and wizards	Yes
Macro support	Yes

Available Attributes

Attribute	Type	Allowed Values	Default	Description
RDADDR _COLLISION_HWCONFIG	STRING	"DELAYED_WRITE", "PERFORMANCE"	"DELAYED_WRITE"	When set to "PERFORMANCE" allows for higher clock performance (frequency) in READ_FIRST mode. If using the same clock on both ports of the RAM with "PERFORMANCE" mode, the address overlap collision rules apply where in "DELAYED_WRITE" mode, you can safely use the BRAM without incurring collisions.
SIM_COLLISION _CHECK	STRING	"ALL", "GENERATE_X_ONLY", "NONE", "WARNING_ONLY"	"ALL"	Allows modification of the simulation behavior so that if a memory collision occurs. • "ALL" = warning produced and affected

Attribute	Type	Allowed Values	Default	Description
				outputs/memory location go unknown (X) • "WARNING_ONLY" = warning produced and affected outputs/memory retain last value • "GENERATE_X_ONLY" = no warning however affected outputs/memory go unknown (X) • "NONE" = no warning and affected outputs/memory retain last value Setting this to a value other than ALL can allow problems in the design go unnoticed during simulation. Care should be taken when changing the value of this attribute.
DOA_REG, DOB_REG	DECIMAL	0, 1	0	A value of 1 enables the output registers to the RAM enabling quicker clock-to-out from the RAM at the expense of an added clock cycle of read latency. A value of 0 allows a read in one clock cycle but will result in slower clock-to-out timing. Applies to port A/B in TDP mode and up to 18 lower bits (including parity bits) in SDP mode.
INIT_A, INIT_B	HEX	18 bit HEX	18'h00000	Specifies the initial value on the port output after configuration. Applies to Port A/B in TDP mode and up to 18 lower bits (including parity bits) in SDP mode.
INIT_00 to INIT_3F	HEX	Any 256-bit HEX value	All zeros	Allows specification of the initial contents of the 16KB data memory array.
INIT_FILE	STRING	File name	None	File name of file used to specify initial RAM contents.
INITP_00 to INITP_07	HEX	Any 256-bit HEX value	All zeros	Allows specification of the initial contents of the 2KB parity data memory array.
RAM_MODE	STRING	"TDP", "SDP"	"TDP"	Selects simple dual port (SDP) or true dual port (TDP) mode.

Attribute	Type	Allowed Values	Default	Description
READ_WIDTH_A	DECIMAL	0, 1, 2, 4, 9, 18, 36, 72	0	Specifies the desired data width for a read on Port A, including parity bits. This value must be 0 if the Port A is not used. Otherwise, it should be set to the desired port width. In "SDP" mode, this is the read width including parity bits.
READ_WIDTH_B	DECIMAL	0, 1, 2, 4, 9, 18	0	Specifies the desired data width for a read on Port B including parity bits. This value must be 0 if the Port B is not used. Otherwise, it should be set to the desired port width. Not used for "SDP" mode.
RSTREG _PRIORITY_A, RSTREG _PRIORITY_B	STRING	"RSTREG", "REGCE"	"RSTREG"	Selects register priority for RSTREG or REGCE. Applies to port A/B in TDP mode and up to 18 lower bits (including parity bits) in SDP mode.
SIM_DEVICE	STRING	7SERIES	"7SERIES"	Must be set to "7SERIES" in order to exhibit proper simulation behavior under all conditions.
SRVAL_A, SRVAL_B	HEX	18 bit HEX	18'h00000	Specifies the output value of the RAM upon assertion of the synchronous reset (RSTREG) signal.
WRITE_MODE_A, WRITE_MODE_B	STRING	"WRITE_FIRST", "NO_CHANGE", "READ_FIRST"	"WRITE_FIRST"	Specifies output behavior of the port being written to. • "WRITE_FIRST" = written value appears on output port of the RAM • "READ_FIRST" = previous RAM contents for that memory location appear on the output port • "NO_CHANGE" = previous value on the output port remains the same. When RAM_MODE="SDP", WRITE_MODE can not be set to "NO_CHANGE". For simple dual port implementations, you should generally set this attribute to "READ_FIRST" if using the same clock on both ports and to set it to "WRITE_FIRST" if using different clocks. This generally yields an improved collision or address overlap behavior when using the BRAM in this configuration.

Attribute	Type	Allowed Values	Default	Description
WRITE_WIDTH_A	DECIMAL	0, 1, 2, 4, 9, 18	0	Specifies the desired data width for a write to Port A including parity bits. This value must be 0 if the port is not used. Otherwise should be set to the desired write width. Not used in SDP mode.
WRITE_WIDTH_B	DECIMAL	0, 1, 2, 4, 9, 18, 36, 72	0	Specifies the desired data width for a write to Port B including parity bits. This value must be 0 if the port is not used. Otherwise should be set to the desired write width. In SDP mode, this is the write width including parity bits.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- RAMB18E1: 18K-bit Configurable Synchronous Block RAM
--           7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

RAMB18E1_inst : RAMB18E1
generic map (
   -- Address Collision Mode: "PERFORMANCE" or "DELAYED_WRITE"
   RDADDR_COLLISION_HWCONFIG => "DELAYED_WRITE",
   -- Collision check: Values ("ALL", "WARNING_ONLY", "GENERATE_X_ONLY" or "NONE")
   SIM_COLLISION_CHECK => "ALL",
   -- DOA_REG, DOB_REG: Optional output register (0 or 1)
   DOA_REG => 0,
   DOB_REG => 0,
   -- INITP_00 to INITP_07: Initial contents of parity memory array
   INITP_00 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_01 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_02 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_03 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_04 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_05 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_06 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_07 => X"0000000000000000000000000000000000000000000000000000000000000000",
   -- INIT_00 to INIT_3F: Initial contents of data memory array
   INIT_00 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_01 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_02 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_03 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_04 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_05 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_06 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_07 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_08 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_09 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_0A => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_0B => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_0C => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_0D => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_0E => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_0F => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_10 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_11 => X"0000000000000000000000000000000000000000000000000000000000000000",
```

```
   INIT_12 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_13 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_14 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_15 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_16 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_17 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_18 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_19 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_1A => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_1B => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_1C => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_1D => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_1E => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_1F => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_20 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_21 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_22 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_23 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_24 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_25 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_26 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_27 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_28 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_29 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_2A => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_2B => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_2C => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_2D => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_2E => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_2F => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_30 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_31 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_32 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_33 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_34 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_35 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_36 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_37 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_38 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_39 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_3A => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_3B => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_3C => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_3D => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_3E => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_3F => X"0000000000000000000000000000000000000000000000000000000000000000",
   -- INIT_A, INIT_B: Initial values on output ports
   INIT_A => X"00000",
   INIT_B => X"00000",
   -- Initialization File: RAM initialization file
   INIT_FILE => "NONE",
   -- RAM Mode: "SDP" or "TDP"
   RAM_MODE => "TDP",
   -- READ_WIDTH_A/B, WRITE_WIDTH_A/B: Read/write width per port
   READ_WIDTH_A => 0,                                                              -- 0-72
   READ_WIDTH_B => 0,                                                              -- 0-18
   WRITE_WIDTH_A => 0,                                                             -- 0-18
   WRITE_WIDTH_B => 0,                                                             -- 0-72
   -- RSTREG_PRIORITY_A, RSTREG_PRIORITY_B: Reset or enable priority ("RSTREG" or "REGCE")
   RSTREG_PRIORITY_A => "RSTREG",
   RSTREG_PRIORITY_B => "RSTREG",
   -- SRVAL_A, SRVAL_B: Set/reset value for output
   SRVAL_A => X"00000",
   SRVAL_B => X"00000",
   -- Simulation Device: Must be set to "7SERIES" for simulation behavior
   SIM_DEVICE => "7SERIES",
   -- WriteMode: Value on output upon a write ("WRITE_FIRST", "READ_FIRST", or "NO_CHANGE")
   WRITE_MODE_A => "WRITE_FIRST",
   WRITE_MODE_B => "WRITE_FIRST"
)
port map (
   -- Port A Data: 16-bit (each) output: Port A data
```

```
   DOADO => DOADO,                 -- 16-bit output: A port data/LSB data
   DOPADOP => DOPADOP,             -- 2-bit output: A port parity/LSB parity
   -- Port B Data: 16-bit (each) output: Port B data
   DOBDO => DOBDO,                 -- 16-bit output: B port data/MSB data
   DOPBDOP => DOPBDOP,             -- 2-bit output: B port parity/MSB parity
   -- Port A Address/Control Signals: 14-bit (each) input: Port A address and control signals (read port
   -- when RAM_MODE="SDP")
   ADDRARDADDR => ADDRARDADDR,     -- 14-bit input: A port address/Read address
   CLKARDCLK => CLKARDCLK,         -- 1-bit input: A port clock/Read clock
   ENARDEN => ENARDEN,             -- 1-bit input: A port enable/Read enable
   REGCEAREGCE => REGCEAREGCE,     -- 1-bit input: A port register enable/Register enable
   RSTRAMARSTRAM => RSTRAMARSTRAM, -- 1-bit input: A port set/reset
   RSTREGARSTREG => RSTREGARSTREG, -- 1-bit input: A port register set/reset
   WEA => WEA,                     -- 2-bit input: A port write enable
   -- Port A Data: 16-bit (each) input: Port A data
   DIADI => DIADI,                 -- 16-bit input: A port data/LSB data
   DIPADIP => DIPADIP,             -- 2-bit input: A port parity/LSB parity
   -- Port B Address/Control Signals: 14-bit (each) input: Port B address and control signals (write port
   -- when RAM_MODE="SDP")
   ADDRBWRADDR => ADDRBWRADDR,     -- 14-bit input: B port address/Write address
   CLKBWRCLK => CLKBWRCLK,         -- 1-bit input: B port clock/Write clock
   ENBWREN => ENBWREN,             -- 1-bit input: B port enable/Write enable
   REGCEB => REGCEB,               -- 1-bit input: B port register enable
   RSTRAMB => RSTRAMB,             -- 1-bit input: B port set/reset
   RSTREGB => RSTREGB,             -- 1-bit input: B port register set/reset
   WEBWE => WEBWE,                 -- 4-bit input: B port write enable/Write enable
   -- Port B Data: 16-bit (each) input: Port B data
   DIBDI => DIBDI,                 -- 16-bit input: B port data/MSB data
   DIPBDIP => DIPBDIP              -- 2-bit input: B port parity/MSB parity
);

-- End of RAMB18E1_inst instantiation
```

Verilog Instantiation Template

```
// RAMB18E1: 18K-bit Configurable Synchronous Block RAM
//           7 Series
// Xilinx HDL Libraries Guide, version 2012.2

RAMB18E1 #(
   // Address Collision Mode: "PERFORMANCE" or "DELAYED_WRITE"
   .RDADDR_COLLISION_HWCONFIG("DELAYED_WRITE"),
   // Collision check: Values ("ALL", "WARNING_ONLY", "GENERATE_X_ONLY" or "NONE")
   .SIM_COLLISION_CHECK("ALL"),
   // DOA_REG, DOB_REG: Optional output register (0 or 1)
   .DOA_REG(0),
   .DOB_REG(0),
   // INITP_00 to INITP_07: Initial contents of parity memory array
   .INITP_00(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_01(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_02(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_03(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_04(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_05(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_06(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_07(256'h0000000000000000000000000000000000000000000000000000000000000000),
   // INIT_00 to INIT_3F: Initial contents of data memory array
   .INIT_00(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_01(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_02(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_03(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_04(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_05(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_06(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_07(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_08(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_09(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_0A(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_0B(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_0C(256'h0000000000000000000000000000000000000000000000000000000000000000),
```

```
.INIT_0D(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_0E(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_0F(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_10(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_11(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_12(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_13(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_14(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_15(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_16(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_17(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_18(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_19(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_1A(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_1B(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_1C(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_1D(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_1E(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_1F(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_20(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_21(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_22(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_23(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_24(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_25(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_26(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_27(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_28(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_29(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_2A(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_2B(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_2C(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_2D(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_2E(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_2F(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_30(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_31(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_32(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_33(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_34(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_35(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_36(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_37(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_38(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_39(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_3A(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_3B(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_3C(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_3D(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_3E(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_3F(256'h0000000000000000000000000000000000000000000000000000000000000000),
// INIT_A, INIT_B: Initial values on output ports
.INIT_A(18'h00000),
.INIT_B(18'h00000),
// Initialization File: RAM initialization file
.INIT_FILE("NONE"),
// RAM Mode: "SDP" or "TDP"
.RAM_MODE("TDP"),
// READ_WIDTH_A/B, WRITE_WIDTH_A/B: Read/write width per port
.READ_WIDTH_A(0),                                                                    // 0-72
.READ_WIDTH_B(0),                                                                    // 0-18
.WRITE_WIDTH_A(0),                                                                   // 0-18
.WRITE_WIDTH_B(0),                                                                   // 0-72
// RSTREG_PRIORITY_A, RSTREG_PRIORITY_B: Reset or enable priority ("RSTREG" or "REGCE")
.RSTREG_PRIORITY_A("RSTREG"),
.RSTREG_PRIORITY_B("RSTREG"),
// SRVAL_A, SRVAL_B: Set/reset value for output
.SRVAL_A(18'h00000),
.SRVAL_B(18'h00000),
// Simulation Device: Must be set to "7SERIES" for simulation behavior
.SIM_DEVICE("7SERIES"),
// WriteMode: Value on output upon a write ("WRITE_FIRST", "READ_FIRST", or "NO_CHANGE")
```

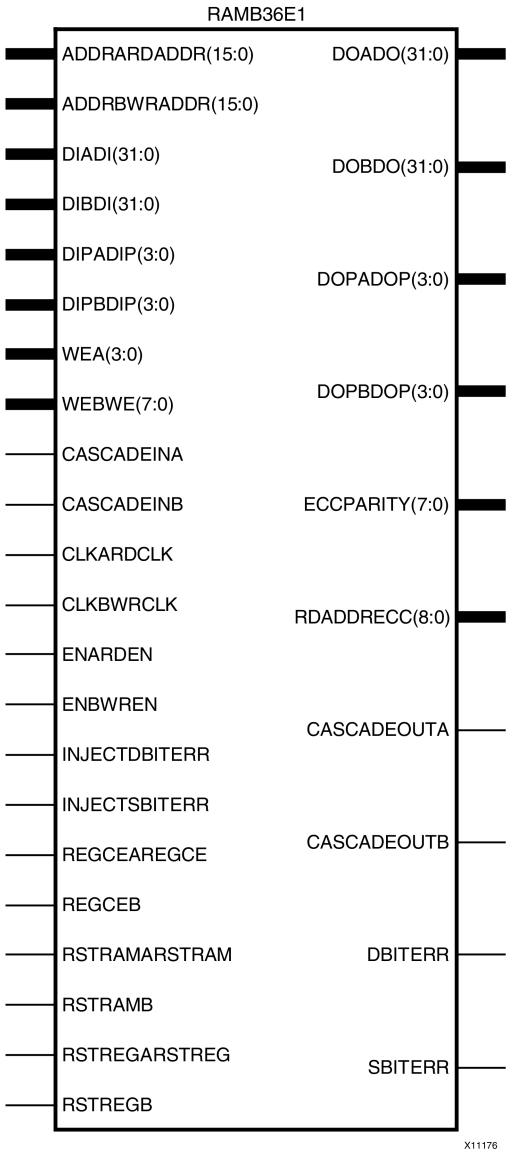
```
   .WRITE_MODE_A("WRITE_FIRST"),
   .WRITE_MODE_B("WRITE_FIRST")
)
RAMB18E1_inst (
   // Port A Data: 16-bit (each) output: Port A data
   .DOADO(DOADO),                 // 16-bit output: A port data/LSB data
   .DOPADOP(DOPADOP),             // 2-bit output: A port parity/LSB parity
   // Port B Data: 16-bit (each) output: Port B data
   .DOBDO(DOBDO),                 // 16-bit output: B port data/MSB data
   .DOPBDOP(DOPBDOP),             // 2-bit output: B port parity/MSB parity
   // Port A Address/Control Signals: 14-bit (each) input: Port A address and control signals (read port
   // when RAM_MODE="SDP")
   .ADDRARDADDR(ADDRARDADDR),     // 14-bit input: A port address/Read address
   .CLKARDCLK(CLKARDCLK),         // 1-bit input: A port clock/Read clock
   .ENARDEN(ENARDEN),             // 1-bit input: A port enable/Read enable
   .REGCEAREGCE(REGCEAREGCE),     // 1-bit input: A port register enable/Register enable
   .RSTRAMARSTRAM(RSTRAMARSTRAM), // 1-bit input: A port set/reset
   .RSTREGARSTREG(RSTREGARSTREG), // 1-bit input: A port register set/reset
   .WEA(WEA),                     // 2-bit input: A port write enable
   // Port A Data: 16-bit (each) input: Port A data
   .DIADI(DIADI),                 // 16-bit input: A port data/LSB data
   .DIPADIP(DIPADIP),             // 2-bit input: A port parity/LSB parity
   // Port B Address/Control Signals: 14-bit (each) input: Port B address and control signals (write port
   // when RAM_MODE="SDP")
   .ADDRBWRADDR(ADDRBWRADDR),     // 14-bit input: B port address/Write address
   .CLKBWRCLK(CLKBWRCLK),         // 1-bit input: B port clock/Write clock
   .ENBWREN(ENBWREN),             // 1-bit input: B port enable/Write enable
   .REGCEB(REGCEB),               // 1-bit input: B port register enable
   .RSTRAMB(RSTRAMB),             // 1-bit input: B port set/reset
   .RSTREGB(RSTREGB),             // 1-bit input: B port register set/reset
   .WEBWE(WEBWE),                 // 4-bit input: B port write enable/Write enable
   // Port B Data: 16-bit (each) input: Port B data
   .DIBDI(DIBDI),                 // 16-bit input: B port data/MSB data
   .DIPBDIP(DIPBDIP)              // 2-bit input: B port parity/MSB parity
);

// End of RAMB18E1_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

RAMB36E1

Primitive: 36K-bit Configurable Synchronous Block RAM



Introduction

7 series devices contain several block RAM memories that can be configured as FIFOs, automatic error correction RAM, or general-purpose 36KB or 18KB RAM/ROM memories. These block RAM memories offer fast and flexible storage of large amounts of on-chip data. The RAMB36E1 allows access to the block RAM in the 36KB configuration. This element can be cascaded to create a larger ram. This element can be configured and used as a 1-bit wide by 32K deep to a 36-bit wide by 1K deep true dual port RAM. This element can also be configured as a 72-bit wide by 512 deep simple dual port RAM. Both read and write operations are fully synchronous to the supplied clock(s) to the component. However, the READ and WRITE ports can operate fully independent and asynchronous to each other, accessing the same memory array. When configured in the wider data width modes, byte-enable write operations are possible, and an optional output register can be used to reduce the clock-to-out times of the RAM. Error detection and correction circuitry can also be enabled to uncover and rectify possible memory corruptions.

Port Descriptions

Port	Type	Width	Function
ADDRARDADDR <15:0>	Input	16	Port A address input bus/Read address input bus.
ADDRBWRADDR <15:0>	Input	16	Port B address input bus/Write address input bus.
CASCADEINA	Input	1	Port A cascade input. Never use when RAM_MODE="SDP".
CASCADEINB	Input	1	Port B cascade input. Never use when RAM_MODE="SDP".
CASCADEOUTA	Output	1	Port A cascade output. Never use when RAM_MODE="SDP".
CASCADEOUTB	Output	1	Port B cascade output. Never use when RAM_MODE="SDP".
CLKARDCLK	Input	1	Rising edge port A clock input/Read clock input.
CLKBWRCLK	Input	1	Rising edge port B clock input/Write clock input.
DBITERR	Output	1	Status output from ECC function to indicate a double bit error was detected. EN_ECC_READ needs to be TRUE in order to use this functionality. Not used when RAM_MODE="TDP".
DIADI<31:0>	Input	32	Port A data input bus/Data input bus addressed by WRADDR. When RAM_MODE="SDP", DIADI is the logical DI<31:0>.
DIBDI<31:0>	Input	32	Port B data input bus/Data input bus addressed by WRADDR. When RAM_MODE="SDP", DIBDI is the logical DI<63:32>.
DIPADIP<3:0>	Input	4	Port A parity data input bus/Data parity input bus addressed by WRADDR. When RAM_MODE="SDP", DIPADIP is the logical DIP<3:0>.
DIPBDIP<3:0>	Input	4	Port B parity data input bus/Data parity input bus addressed by WRADDR. When RAM_MODE="SDP", DIPBDIP is the logical DIP<7:4>.

Port	Type	Width	Function
DOADO<31:0>	Output	32	Port A data output bus/Data output bus addressed by RDADDR. When RAM_MODE="SDP", DOADO is the logical DO<31:0>.
DOBDO<31:0>	Output	32	Port B data output bus/Data output bus addressed by RDADDR. When RAM_MODE="SDP", DOBDO is the logical DO<63:32>.
DOPADOP<3:0>	Output	4	Port A parity data output bus/Data parity output bus addressed by RDADDR. When RAM_MODE="SDP", DOPADOP is the logical DOP<3:0>.
DOPBDOP<3:0>	Output	4	Port B parity data output bus/Data parity output bus addressed by RDADDR. When RAM_MODE="SDP", DOPBDOP is the logical DOP<7:4>.
ECCPARITY<7 :0>	Output	8	8-bit data generated by the ECC encoder used by the ECC decoder for memory error detection and correction. Not used if RAM_MODE="TDP".
ENARDEN	Input	1	Port A RAM enable/Read enable.
ENBWREN	Input	1	Port B RAM enable/Write enable.
INJECTDBITE RR	Input	1	Inject a double bit error if ECC feature is used.
INJECTSBITE RR	Input	1	Inject a single bit error if ECC feature is used.
RDADDRECC<8 :0>	Output	9	ECC read address. Not used when RAM_MODE="TDP".
REGCEAREGCE	Input	1	Port A output register clock enable input/Output register clock enable input (valid only when DO_REG=1).
REGCEB	Input	1	Port B output register clock enable (valid only when DO_REG=1 and RAM_MODE="TDP").
RSTRAMARSTR AM	Input	1	Synchronous data latch set/reset to value indicated by SRVAL_A. RSTRAMARSTRAM sets/resets the BRAM data output latch when DO_REG=0 or 1. If DO_REG=1 there is a cycle of latency between the internal data latch node that is reset by RSTRAMARSTRAM and the DO output of the BRAM. This signal resets port A RAM output when RAM_MODE="TDP" and the entire RAM output when RAM_MODE="SDP".
RSTRAMB	Input	1	Synchronous data latch set/reset to value indicated by SRVAL_B. RSTRAMB sets/resets the BRAM data output latch when DO_REG=0 or 1. If DO_REG=1 there is a cycle of latency between the internal data latch node that is reset by RSTRAMB and the DO output of the BRAM. Not used when RAM_MODE="SDP".
RSTREGARSTR EG	Input	1	Synchronous output register set/reset to value indicated by SRVAL_A. RSTREGARSTREG sets/resets the output register when DO_REG=1. RSTREG_PRIORITY_A determines if this signal gets priority over REGCEAREGCE. This signal resets port A output when RAM_MODE="TDP" and the entire output port when RAM_MODE="SDP".
RSTREGB	Input	1	Synchronous output register set/reset to value indicated by SRVAL_B. RSTREGB sets/resets the output register when DO_REG=1. RSTREG_PRIORITY_B determines if this signal gets priority over REGCEB. Not used when RAM_MODE="SDP".

Port	Type	Width	Function
SBITERR	Output	1	Status output from ECC function to indicate a single bit error was detected. EN_ECC_READ needs to be TRUE in order to use this functionality. Not used when RAM_MODE="TDP".
WEA<3:0>	Input	4	Port A byte-wide write enable. Not used when RAM_MODE="SDP". See User Guide for WEA mapping for different port widths.
WEBWE<7:0>	Input	8	Port B byte-wide write enable/Write enable. See User Guide for WEBWE mapping for different port widths.

Design Entry Method

Instantiation	Yes
Inference	Recommended
CORE Generator™ and wizards	Yes
Macro support	Yes

Available Attributes

Attribute	Type	Allowed Values	Default	Description
RDADDR_COLLISION_HWCONFIG	STRING	"DELAYED_WRITE", "PERFORMANCE"	"DELAYED_WRITE"	When set to "PERFORMANCE" allows for higher clock performance (frequency) in READ_FIRST mode. If using the same clock on both ports of the RAM with "PERFORMANCE" mode, the address overlap collision rules apply where in "DELAYED_WRITE" mode, you can safely use the BRAM without incurring collisions.
SIM_COLLISION_CHECK	STRING	"ALL", "GENERATE_X_ONLY", "NONE", "WARNING_ONLY"	"ALL"	Allows modification of the simulation behavior so that if a memory collision occurs • "ALL" = warning produced and affected outputs/memory location go unknown (X) • "WARNING_ONLY" = warning produced and affected outputs/memory retain last value • "GENERATE_X_ONLY" = no warning however affected outputs/memory go unknown (X)

Attribute	Type	Allowed Values	Default	Description
				• "NONE" = no warning and affected outputs/memory retain last value **Note** Setting this to a value other than ALL can allow problems in the design go unnoticed during simulation. Care should be taken when changing the value of this attribute.
DOA_REG, DOB_REG	DECIMAL	0, 1	0	A value of 1 enables the output registers to the RAM enabling quicker clock-to-out from the RAM at the expense of an added clock cycle of read latency. A value of 0 allows a read in one clock cycle but will result in slower clock-to-out timing. Applies to port A/B in TDP mode and up to 36 lower bits (including parity bits) in "SDP" mode.
EN_ECC_READ	BOOLEAN	FALSE, TRUE	FALSE	Enable the ECC decoder circuitry.
EN_ECC_WRITE	BOOLEAN	FALSE, TRUE	FALSE	Enable the ECC encoder circuitry.
INIT_A, INIT_B	HEX	36 bit HEX	36'h000000000	Specifies the initial value on the port output after configuration. Applies to port A/B in TDP mode and up to 36 lower bits (including parity bits) in "SDP" mode.
INIT_00 to INIT_7F	HEX	Any 256-bit HEX value	All zeros	Allows specification of the initial contents of the 32KB data memory array.
INIT_FILE	STRING	File name	None	File name of file used to specify initial RAM contents.
INITP_00 to INITP_0F	HEX	Any 256-bit HEX value	All zeros	Allows specification of the initial contents of the 4KB parity data memory array.
RAM_EXTENSION_A, RAM_EXTENSION_B	STRING	"NONE", "LOWER", "UPPER"	"NONE"	Selects cascade mode. If not cascading two BlockRAMs to form a 64K x 1 RAM set to "NONE". If cascading RAMs, set to either "UPPER" or "LOWER" to indicate relative RAM location for proper configuration of the RAM. Not used if RAM_MODE="SDP".
RAM_MODE	STRING	"TDP", "SDP"	"TDP"	Selects simple dual port (SDP) or true dual port (TDP) mode.

Attribute	Type	Allowed Values	Default	Description
READ_WIDTH_A, READ_WIDTH_B, WRITE_WIDTH _A, WRITE_WIDTH _B	DECIMAL	0, 1, 2, 4, 9, 18, 36, 72	0	Specifies the desired data width for a read/write on port A/B, including parity bits. This value must be 0 if the port is not used. Otherwise, it should be set to the desired port width.
RSTREG _PRIORITY_A, RSTREG _PRIORITY_B	STRING	"RSTREG", "REGCE"	"RSTREG"	Selects register priority for "RSTREG" or "REGCE". Applies to port A/B in TDP mode and up to 18 lower bits (including parity bits) in SDP mode.
SIM_DEVICE	STRING	7SERIES	"7SERIES"	Must be set to "7SERIES" in order to exhibit proper simulation behavior under all conditions.
SRVAL_A, SRVAL_B	HEX	36 bit HEX	36'h000000000	Specifies the output value of the RAM upon assertion of the synchronous reset (RSTREG) signal.
WRITE_MODE_A, WRITE_MODE_B	STRING	"WRITE_FIRST", "NO_CHANGE", "READ_FIRST"	"WRITE_FIRST"	Specifies output behavior of the port being written to. • "WRITE_FIRST" = written value appears on output port of the RAM • "READ_FIRST" = previous RAM contents for that memory location appears on the output port • "NO_CHANGE" = previous value on the output port remains the same When RAM_MODE="SDP", WRITE_MODE can not be set to "NO_CHANGE". For simple dual port implementations, your should generally set WRITE_MODE to "READ_FIRST" if using the same clock on both ports and to set it to "WRITE_FIRST" if using different clocks. This generally yields an improved collision or address overlap behavior when using the BRAM in this configuration.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
```

```
use UNISIM.vcomponents.all;


-- RAMB36E1: 36K-bit Configurable Synchronous Block RAM
--           7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

RAMB36E1_inst : RAMB36E1
generic map (
   -- Address Collision Mode: "PERFORMANCE" or "DELAYED_WRITE"
   RDADDR_COLLISION_HWCONFIG => "DELAYED_WRITE",
   -- Collision check: Values ("ALL", "WARNING_ONLY", "GENERATE_X_ONLY" or "NONE")
   SIM_COLLISION_CHECK => "ALL",
   -- DOA_REG, DOB_REG: Optional output register (0 or 1)
   DOA_REG => 0,
   DOB_REG => 0,
   EN_ECC_READ => FALSE,                                                    -- Enable ECC decoder,
                                                                            -- FALSE, TRUE
   EN_ECC_WRITE => FALSE,                                                   -- Enable ECC encoder,
                                                                            -- FALSE, TRUE
   -- INITP_00 to INITP_0F: Initial contents of the parity memory array
   INITP_00 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_01 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_02 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_03 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_04 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_05 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_06 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_07 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_08 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_09 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_0A => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_0B => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_0C => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_0D => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_0E => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_0F => X"0000000000000000000000000000000000000000000000000000000000000000",
   -- INIT_00 to INIT_7F: Initial contents of the data memory array
   INIT_00 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_01 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_02 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_03 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_04 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_05 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_06 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_07 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_08 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_09 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_0A => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_0B => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_0C => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_0D => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_0E => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_0F => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_10 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_11 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_12 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_13 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_14 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_15 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_16 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_17 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_18 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_19 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_1A => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_1B => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_1C => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_1D => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_1E => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_1F => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_20 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_21 => X"0000000000000000000000000000000000000000000000000000000000000000",
```

```
INIT_22 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_23 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_24 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_25 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_26 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_27 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_28 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_29 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_2A => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_2B => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_2C => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_2D => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_2E => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_2F => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_30 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_31 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_32 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_33 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_34 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_35 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_36 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_37 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_38 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_39 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_3A => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_3B => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_3C => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_3D => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_3E => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_3F => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_40 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_41 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_42 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_43 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_44 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_45 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_46 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_47 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_48 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_49 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_4A => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_4B => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_4C => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_4D => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_4E => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_4F => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_50 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_51 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_52 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_53 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_54 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_55 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_56 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_57 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_58 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_59 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_5A => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_5B => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_5C => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_5D => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_5E => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_5F => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_60 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_61 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_62 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_63 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_64 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_65 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_66 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_67 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_68 => X"0000000000000000000000000000000000000000000000000000000000000000",
INIT_69 => X"0000000000000000000000000000000000000000000000000000000000000000",
```

```
      INIT_6A => X"0000000000000000000000000000000000000000000000000000000000000000",
      INIT_6B => X"0000000000000000000000000000000000000000000000000000000000000000",
      INIT_6C => X"0000000000000000000000000000000000000000000000000000000000000000",
      INIT_6D => X"0000000000000000000000000000000000000000000000000000000000000000",
      INIT_6E => X"0000000000000000000000000000000000000000000000000000000000000000",
      INIT_6F => X"0000000000000000000000000000000000000000000000000000000000000000",
      INIT_70 => X"0000000000000000000000000000000000000000000000000000000000000000",
      INIT_71 => X"0000000000000000000000000000000000000000000000000000000000000000",
      INIT_72 => X"0000000000000000000000000000000000000000000000000000000000000000",
      INIT_73 => X"0000000000000000000000000000000000000000000000000000000000000000",
      INIT_74 => X"0000000000000000000000000000000000000000000000000000000000000000",
      INIT_75 => X"0000000000000000000000000000000000000000000000000000000000000000",
      INIT_76 => X"0000000000000000000000000000000000000000000000000000000000000000",
      INIT_77 => X"0000000000000000000000000000000000000000000000000000000000000000",
      INIT_78 => X"0000000000000000000000000000000000000000000000000000000000000000",
      INIT_79 => X"0000000000000000000000000000000000000000000000000000000000000000",
      INIT_7A => X"0000000000000000000000000000000000000000000000000000000000000000",
      INIT_7B => X"0000000000000000000000000000000000000000000000000000000000000000",
      INIT_7C => X"0000000000000000000000000000000000000000000000000000000000000000",
      INIT_7D => X"0000000000000000000000000000000000000000000000000000000000000000",
      INIT_7E => X"0000000000000000000000000000000000000000000000000000000000000000",
      INIT_7F => X"0000000000000000000000000000000000000000000000000000000000000000",
      -- INIT_A, INIT_B: Initial values on output ports
      INIT_A => X"000000000",
      INIT_B => X"000000000",
      -- Initialization File: RAM initialization file
      INIT_FILE => "NONE",
      -- RAM Mode: "SDP" or "TDP"
      RAM_MODE => "TDP",
      -- RAM_EXTENSION_A, RAM_EXTENSION_B: Selects cascade mode ("UPPER", "LOWER", or "NONE")
      RAM_EXTENSION_A => "NONE",
      RAM_EXTENSION_B => "NONE",
      -- READ_WIDTH_A/B, WRITE_WIDTH_A/B: Read/write width per port
      READ_WIDTH_A => 0,                                                              -- 0-72
      READ_WIDTH_B => 0,                                                              -- 0-36
      WRITE_WIDTH_A => 0,                                                             -- 0-36
      WRITE_WIDTH_B => 0,                                                             -- 0-72
      -- RSTREG_PRIORITY_A, RSTREG_PRIORITY_B: Reset or enable priority ("RSTREG" or "REGCE")
      RSTREG_PRIORITY_A => "RSTREG",
      RSTREG_PRIORITY_B => "RSTREG",
      -- SRVAL_A, SRVAL_B: Set/reset value for output
      SRVAL_A => X"000000000",
      SRVAL_B => X"000000000",
      -- Simulation Device: Must be set to "7SERIES" for simulation behavior
      SIM_DEVICE => "7SERIES",
      -- WriteMode: Value on output upon a write ("WRITE_FIRST", "READ_FIRST", or "NO_CHANGE")
      WRITE_MODE_A => "WRITE_FIRST",
      WRITE_MODE_B => "WRITE_FIRST"
   )
   port map (
      -- Cascade Signals: 1-bit (each) output: BRAM cascade ports (to create 64kx1)
      CASCADEOUTA => CASCADEOUTA,     -- 1-bit output: A port cascade
      CASCADEOUTB => CASCADEOUTB,     -- 1-bit output: B port cascade
      -- ECC Signals: 1-bit (each) output: Error Correction Circuitry ports
      DBITERR => DBITERR,             -- 1-bit output: Double bit error status
      ECCPARITY => ECCPARITY,         -- 8-bit output: Generated error correction parity
      RDADDRECC => RDADDRECC,         -- 9-bit output: ECC read address
      SBITERR => SBITERR,             -- 1-bit output: Single bit error status
      -- Port A Data: 32-bit (each) output: Port A data
      DOADO => DOADO,                 -- 32-bit output: A port data/LSB data
      DOPADOP => DOPADOP,             -- 4-bit output: A port parity/LSB parity
      -- Port B Data: 32-bit (each) output: Port B data
      DOBDO => DOBDO,                 -- 32-bit output: B port data/MSB data
      DOPBDOP => DOPBDOP,             -- 4-bit output: B port parity/MSB parity
      -- Cascade Signals: 1-bit (each) input: BRAM cascade ports (to create 64kx1)
      CASCADEINA => CASCADEINA,       -- 1-bit input: A port cascade
      CASCADEINB => CASCADEINB,       -- 1-bit input: B port cascade
      -- ECC Signals: 1-bit (each) input: Error Correction Circuitry ports
      INJECTDBITERR => INJECTDBITERR, -- 1-bit input: Inject a double bit error
      INJECTSBITERR => INJECTSBITERR, -- 1-bit input: Inject a single bit error
      -- Port A Address/Control Signals: 16-bit (each) input: Port A address and control signals (read port
      -- when RAM_MODE="SDP")
```

```
   ADDRARDADDR => ADDRARDADDR,     -- 16-bit input: A port address/Read address
   CLKARDCLK => CLKARDCLK,         -- 1-bit input: A port clock/Read clock
   ENARDEN => ENARDEN,             -- 1-bit input: A port enable/Read enable
   REGCEAREGCE => REGCEAREGCE,     -- 1-bit input: A port register enable/Register enable
   RSTRAMARSTRAM => RSTRAMARSTRAM, -- 1-bit input: A port set/reset
   RSTREGARSTREG => RSTREGARSTREG, -- 1-bit input: A port register set/reset
   WEA => WEA,                     -- 4-bit input: A port write enable
   -- Port A Data: 32-bit (each) input: Port A data
   DIADI => DIADI,                 -- 32-bit input: A port data/LSB data
   DIPADIP => DIPADIP,             -- 4-bit input: A port parity/LSB parity
   -- Port B Address/Control Signals: 16-bit (each) input: Port B address and control signals (write port
   -- when RAM_MODE="SDP")
   ADDRBWRADDR => ADDRBWRADDR,     -- 16-bit input: B port address/Write address
   CLKBWRCLK => CLKBWRCLK,         -- 1-bit input: B port clock/Write clock
   ENBWREN => ENBWREN,             -- 1-bit input: B port enable/Write enable
   REGCEB => REGCEB,               -- 1-bit input: B port register enable
   RSTRAMB => RSTRAMB,             -- 1-bit input: B port set/reset
   RSTREGB => RSTREGB,             -- 1-bit input: B port register set/reset
   WEBWE => WEBWE,                 -- 8-bit input: B port write enable/Write enable
   -- Port B Data: 32-bit (each) input: Port B data
   DIBDI => DIBDI,                 -- 32-bit input: B port data/MSB data
   DIPBDIP => DIPBDIP              -- 4-bit input: B port parity/MSB parity
);

-- End of RAMB36E1_inst instantiation
```

Verilog Instantiation Template

```
// RAMB36E1: 36K-bit Configurable Synchronous Block RAM
//           7 Series
// Xilinx HDL Libraries Guide, version 2012.2

RAMB36E1 #(
   // Address Collision Mode: "PERFORMANCE" or "DELAYED_WRITE"
   .RDADDR_COLLISION_HWCONFIG("DELAYED_WRITE"),
   // Collision check: Values ("ALL", "WARNING_ONLY", "GENERATE_X_ONLY" or "NONE")
   .SIM_COLLISION_CHECK("ALL"),
   // DOA_REG, DOB_REG: Optional output register (0 or 1)
   .DOA_REG(0),
   .DOB_REG(0),
   .EN_ECC_READ("FALSE"),                                                          // Enable ECC decoder,
                                                                                   // FALSE, TRUE
   .EN_ECC_WRITE("FALSE"),                                                         // Enable ECC encoder,
                                                                                   // FALSE, TRUE
   // INITP_00 to INITP_0F: Initial contents of the parity memory array
   .INITP_00(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_01(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_02(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_03(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_04(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_05(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_06(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_07(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_08(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_09(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_0A(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_0B(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_0C(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_0D(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_0E(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_0F(256'h0000000000000000000000000000000000000000000000000000000000000000),
   // INIT_00 to INIT_7F: Initial contents of the data memory array
   .INIT_00(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_01(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_02(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_03(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_04(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_05(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_06(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_07(256'h0000000000000000000000000000000000000000000000000000000000000000),
```

```
.INIT_08(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_09(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_0A(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_0B(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_0C(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_0D(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_0E(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_0F(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_10(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_11(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_12(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_13(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_14(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_15(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_16(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_17(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_18(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_19(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_1A(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_1B(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_1C(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_1D(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_1E(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_1F(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_20(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_21(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_22(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_23(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_24(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_25(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_26(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_27(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_28(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_29(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_2A(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_2B(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_2C(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_2D(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_2E(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_2F(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_30(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_31(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_32(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_33(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_34(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_35(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_36(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_37(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_38(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_39(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_3A(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_3B(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_3C(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_3D(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_3E(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_3F(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_40(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_41(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_42(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_43(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_44(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_45(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_46(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_47(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_48(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_49(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_4A(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_4B(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_4C(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_4D(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_4E(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_4F(256'h0000000000000000000000000000000000000000000000000000000000000000),
```

```
.INIT_50(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_51(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_52(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_53(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_54(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_55(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_56(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_57(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_58(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_59(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_5A(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_5B(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_5C(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_5D(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_5E(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_5F(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_60(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_61(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_62(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_63(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_64(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_65(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_66(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_67(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_68(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_69(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_6A(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_6B(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_6C(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_6D(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_6E(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_6F(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_70(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_71(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_72(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_73(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_74(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_75(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_76(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_77(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_78(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_79(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_7A(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_7B(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_7C(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_7D(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_7E(256'h0000000000000000000000000000000000000000000000000000000000000000),
.INIT_7F(256'h0000000000000000000000000000000000000000000000000000000000000000),
// INIT_A, INIT_B: Initial values on output ports
.INIT_A(36'h000000000),
.INIT_B(36'h000000000),
// Initialization File: RAM initialization file
.INIT_FILE("NONE"),
// RAM Mode: "SDP" or "TDP"
.RAM_MODE("TDP"),
// RAM_EXTENSION_A, RAM_EXTENSION_B: Selects cascade mode ("UPPER", "LOWER", or "NONE")
.RAM_EXTENSION_A("NONE"),
.RAM_EXTENSION_B("NONE"),
// READ_WIDTH_A/B, WRITE_WIDTH_A/B: Read/write width per port
.READ_WIDTH_A(0),                                                                  // 0-72
.READ_WIDTH_B(0),                                                                  // 0-36
.WRITE_WIDTH_A(0),                                                                 // 0-36
.WRITE_WIDTH_B(0),                                                                 // 0-72
// RSTREG_PRIORITY_A, RSTREG_PRIORITY_B: Reset or enable priority ("RSTREG" or "REGCE")
.RSTREG_PRIORITY_A("RSTREG"),
.RSTREG_PRIORITY_B("RSTREG"),
// SRVAL_A, SRVAL_B: Set/reset value for output
.SRVAL_A(36'h000000000),
.SRVAL_B(36'h000000000),
// Simulation Device: Must be set to "7SERIES" for simulation behavior
.SIM_DEVICE("7SERIES"),
// WriteMode: Value on output upon a write ("WRITE_FIRST", "READ_FIRST", or "NO_CHANGE")
```

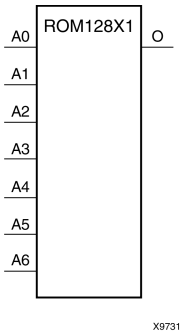
```
   .WRITE_MODE_A("WRITE_FIRST"),
   .WRITE_MODE_B("WRITE_FIRST")
)
RAMB36E1_inst (
   // Cascade Signals: 1-bit (each) output: BRAM cascade ports (to create 64kx1)
   .CASCADEOUTA(CASCADEOUTA),     // 1-bit output: A port cascade
   .CASCADEOUTB(CASCADEOUTB),     // 1-bit output: B port cascade
   // ECC Signals: 1-bit (each) output: Error Correction Circuitry ports
   .DBITERR(DBITERR),             // 1-bit output: Double bit error status
   .ECCPARITY(ECCPARITY),         // 8-bit output: Generated error correction parity
   .RDADDRECC(RDADDRECC),         // 9-bit output: ECC read address
   .SBITERR(SBITERR),             // 1-bit output: Single bit error status
   // Port A Data: 32-bit (each) output: Port A data
   .DOADO(DOADO),                 // 32-bit output: A port data/LSB data
   .DOPADOP(DOPADOP),             // 4-bit output: A port parity/LSB parity
   // Port B Data: 32-bit (each) output: Port B data
   .DOBDO(DOBDO),                 // 32-bit output: B port data/MSB data
   .DOPBDOP(DOPBDOP),             // 4-bit output: B port parity/MSB parity
   // Cascade Signals: 1-bit (each) input: BRAM cascade ports (to create 64kx1)
   .CASCADEINA(CASCADEINA),       // 1-bit input: A port cascade
   .CASCADEINB(CASCADEINB),       // 1-bit input: B port cascade
   // ECC Signals: 1-bit (each) input: Error Correction Circuitry ports
   .INJECTDBITERR(INJECTDBITERR), // 1-bit input: Inject a double bit error
   .INJECTSBITERR(INJECTSBITERR), // 1-bit input: Inject a single bit error
   // Port A Address/Control Signals: 16-bit (each) input: Port A address and control signals (read port
   // when RAM_MODE="SDP")
   .ADDRARDADDR(ADDRARDADDR),     // 16-bit input: A port address/Read address
   .CLKARDCLK(CLKARDCLK),         // 1-bit input: A port clock/Read clock
   .ENARDEN(ENARDEN),             // 1-bit input: A port enable/Read enable
   .REGCEAREGCE(REGCEAREGCE),     // 1-bit input: A port register enable/Register enable
   .RSTRAMARSTRAM(RSTRAMARSTRAM), // 1-bit input: A port set/reset
   .RSTREGARSTREG(RSTREGARSTREG), // 1-bit input: A port register set/reset
   .WEA(WEA),                     // 4-bit input: A port write enable
   // Port A Data: 32-bit (each) input: Port A data
   .DIADI(DIADI),                 // 32-bit input: A port data/LSB data
   .DIPADIP(DIPADIP),             // 4-bit input: A port parity/LSB parity
   // Port B Address/Control Signals: 16-bit (each) input: Port B address and control signals (write port
   // when RAM_MODE="SDP")
   .ADDRBWRADDR(ADDRBWRADDR),     // 16-bit input: B port address/Write address
   .CLKBWRCLK(CLKBWRCLK),         // 1-bit input: B port clock/Write clock
   .ENBWREN(ENBWREN),             // 1-bit input: B port enable/Write enable
   .REGCEB(REGCEB),               // 1-bit input: B port register enable
   .RSTRAMB(RSTRAMB),             // 1-bit input: B port set/reset
   .RSTREGB(RSTREGB),             // 1-bit input: B port register set/reset
   .WEBWE(WEBWE),                 // 8-bit input: B port write enable/Write enable
   // Port B Data: 32-bit (each) input: Port B data
   .DIBDI(DIBDI),                 // 32-bit input: B port data/MSB data
   .DIPBDIP(DIPBDIP)              // 4-bit input: B port parity/MSB parity
);

// End of RAMB36E1_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

ROM128X1

Primitive: 128-Deep by 1-Wide ROM



Introduction

This design element is a 128-word by 1-bit read-only memory. The data output (O) reflects the word selected by the 7-bit address (A6:A0). The ROM is initialized to a known value during configuration with the INIT=value parameter. The value consists of 32 hexadecimal digits that are written into the ROM from the most-significant digit A=FH to the least-significant digit A=0H. An error occurs if the INIT=value is not specified.

Logic Table

Input				Output
I0	**I1**	**I2**	**I3**	**O**
0	0	0	0	INIT(0)
0	0	0	1	INIT(1)
0	0	1	0	INIT(2)
0	0	1	1	INIT(3)
0	1	0	0	INIT(4)
0	1	0	1	INIT(5)
0	1	1	0	INIT(6)
0	1	1	1	INIT(7)
1	0	0	0	INIT(8)
1	0	0	1	INIT(9)
1	0	1	0	INIT(10)
1	0	1	1	INIT(11)
1	1	0	0	INIT(12)
1	1	0	1	INIT(13)
1	1	1	0	INIT(14)
1	1	1	1	INIT(15)

Design Entry Method

Instantiation	Yes
Inference	Recommended
CORE Generator™ and wizards	No
Macro support	No

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 128-Bit Value	All zeros	Specifies the contents of the ROM.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- ROM128X1: 128 x 1 Asynchronous Distributed (LUT) ROM
--           7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

ROM128X1_inst : ROM128X1
generic map (
   INIT => X"00000000000000000000000000000000")
port map (
   O => O,   -- ROM output
   A0 => A0, -- ROM address[0]
   A1 => A1, -- ROM address[1]
   A2 => A2, -- ROM address[2]
   A3 => A3, -- ROM address[3]
   A4 => A4, -- ROM address[4]
   A5 => A5, -- ROM address[5]
   A6 => A6  -- ROM address[6]
);

-- End of ROM128X1_inst instantiation
```

Verilog Instantiation Template

```
// ROM128X1: 128 x 1 Asynchronous Distributed (LUT) ROM (Mapped to two SliceM LUT6s)
//           7 Series
// Xilinx HDL Libraries Guide, version 2012.2

ROM128X1 #(
   .INIT(128'h00000000000000000000000000000000) // Contents of ROM
) ROM128X1_inst (
   .O(O),   // ROM output
   .A0(A0), // ROM address[0]
   .A1(A1), // ROM address[1]
   .A2(A2), // ROM address[2]
   .A3(A3), // ROM address[3]
   .A4(A4), // ROM address[4]
   .A5(A5), // ROM address[5]
   .A6(A6)  // ROM address[6]
);
```

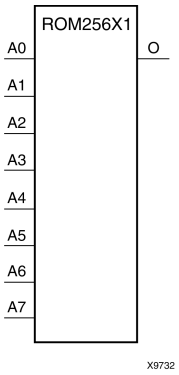
```
// End of ROM128X1_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

ROM256X1

Primitive: 256-Deep by 1-Wide ROM



Introduction

This design element is a 256-word by 1-bit read-only memory. The data output (O) reflects the word selected by the 8-bit address (A7:A0). The ROM is initialized to a known value during configuration with the INIT=value parameter. The value consists of 64 hexadecimal digits that are written into the ROM from the most-significant digit A=FH to the least-significant digit A=0H.

An error occurs if the INIT=value is not specified.

Logic Table

Input				Output
I0	**I1**	**I2**	**I3**	**O**
0	0	0	0	INIT(0)
0	0	0	1	INIT(1)
0	0	1	0	INIT(2)
0	0	1	1	INIT(3)
0	1	0	0	INIT(4)
0	1	0	1	INIT(5)
0	1	1	0	INIT(6)
0	1	1	1	INIT(7)
1	0	0	0	INIT(8)
1	0	0	1	INIT(9)
1	0	1	0	INIT(10)
1	0	1	1	INIT(11)
1	1	0	0	INIT(12)
1	1	0	1	INIT(13)

Input				Output
I0	I1	I2	I3	O
1	1	1	0	INIT(14)
1	1	1	1	INIT(15)

Design Entry Method

Instantiation	Yes
Inference	Recommended
CORE Generator™ and wizards	No
Macro support	No

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 256-Bit Value	All zeros	Specifies the contents of the ROM.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- ROM256X1: 256 x 1 Asynchronous Distributed (LUT) ROM
--           7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

ROM256X1_inst : ROM256X1
generic map (
   INIT => X"0000000000000000000000000000000000000000000000000000000000000000")
port map (
   O => O,    -- ROM output
   A0 => A0, -- ROM address[0]
   A1 => A1, -- ROM address[1]
   A2 => A2, -- ROM address[2]
   A3 => A3, -- ROM address[3]
   A4 => A4, -- ROM address[4]
   A5 => A5, -- ROM address[5]
   A6 => A6,  -- ROM address[6]
   A7 => A7  -- ROM address[7]
);

-- End of ROM256X1_inst instantiation
```

Verilog Instantiation Template

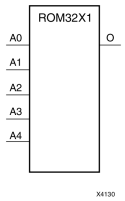
```
// ROM256X1: 256 x 1 Asynchronous Distributed (LUT) ROM (Mapped to forur SliceM LUT6s)
//           7 Series
// Xilinx HDL Libraries Guide, version 2012.2

ROM256X1 #(
   .INIT(256'h0000000000000000000000000000000000000000000000000000000000000000) // Contents of ROM
) ROM256X1_inst (
   .O(O),   // ROM output
   .A0(A0), // ROM address[0]
   .A1(A1), // ROM address[1]
   .A2(A2), // ROM address[2]
   .A3(A3), // ROM address[3]
   .A4(A4), // ROM address[4]
   .A5(A5), // ROM address[5]
   .A6(A6), // ROM address[6]
   .A7(A7)  // ROM address[7]
);

// End of ROM256X1_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

ROM32X1

Primitive: 32-Deep by 1-Wide ROM



Introduction

This design element is a 32-word by 1-bit read-only memory. The data output (O) reflects the word selected by the 5-bit address (A4:A0). The ROM is initialized to a known value during configuration with the INIT=value parameter. The value consists of eight hexadecimal digits that are written into the ROM from the most-significant digit A=1FH to the least-significant digit A=00H.

For example, the INIT=10A78F39 parameter produces the data stream: 0001 0000 1010 0111 1000 1111 0011 1001. An error occurs if the INIT=value is not specified.

Logic Table

Input				Output
I0	**I1**	**I2**	**I3**	**O**
0	0	0	0	INIT(0)
0	0	0	1	INIT(1)
0	0	1	0	INIT(2)
0	0	1	1	INIT(3)
0	1	0	0	INIT(4)
0	1	0	1	INIT(5)
0	1	1	0	INIT(6)
0	1	1	1	INIT(7)
1	0	0	0	INIT(8)
1	0	0	1	INIT(9)
1	0	1	0	INIT(10)
1	0	1	1	INIT(11)
1	1	0	0	INIT(12)
1	1	0	1	INIT(13)
1	1	1	0	INIT(14)
1	1	1	1	INIT(15)

Design Entry Method

Instantiation	Yes
Inference	Recommended
CORE Generator™ and wizards	No
Macro support	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 32-Bit Value	All zeros	Specifies the contents of the ROM.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- ROM32X1: 32 x 1 Asynchronous Distributed (LUT) ROM
--          7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

ROM32X1_inst : ROM32X1
generic map (
   INIT => X"00000000")
port map (
   O => O,    -- ROM output
   A0 => A0, -- ROM address[0]
   A1 => A1, -- ROM address[1]
   A2 => A2, -- ROM address[2]
   A3 => A3, -- ROM address[3]
   A4 => A4  -- ROM address[4]
);
-- End of ROM32X1_inst instantiation
```

Verilog Instantiation Template

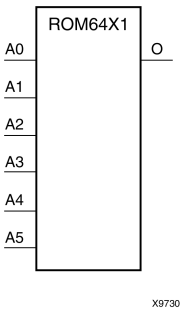
```
// ROM32X1: 32 x 1 Asynchronous Distributed (LUT) ROM (Mapped to a SliceM LUT6)
//          7 Series
// Xilinx HDL Libraries Guide, version 2012.2

ROM32X1 #(
   .INIT(32'h00000000) // Contents of ROM
) ROM32X1_inst (
   .O(O),    // ROM output
   .A0(A0), // ROM address[0]
   .A1(A1), // ROM address[1]
   .A2(A2), // ROM address[2]
   .A3(A3), // ROM address[3]
   .A4(A4)  // ROM address[4]
);

// End of ROM32X1_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

ROM64X1

Primitive: 64-Deep by 1-Wide ROM



Introduction

This design element is a 64-word by 1-bit read-only memory. The data output (O) reflects the word selected by the 6-bit address (A5:A0). The ROM is initialized to a known value during configuration with the INIT=value parameter. The value consists of 16 hexadecimal digits that are written into the ROM from the most-significant digit A=FH to the least-significant digit A=0H. An error occurs if the INIT=value is not specified.

Logic Table

Input				Output
I0	**I1**	**I2**	**I3**	**O**
0	0	0	0	INIT(0)
0	0	0	1	INIT(1)
0	0	1	0	INIT(2)
0	0	1	1	INIT(3)
0	1	0	0	INIT(4)
0	1	0	1	INIT(5)
0	1	1	0	INIT(6)
0	1	1	1	INIT(7)
1	0	0	0	INIT(8)
1	0	0	1	INIT(9)
1	0	1	0	INIT(10)
1	0	1	1	INIT(11)
1	1	0	0	INIT(12)
1	1	0	1	INIT(13)
1	1	1	0	INIT(14)
1	1	1	1	INIT(15)

Design Entry Method

Instantiation	Yes
Inference	Recommended
CORE Generator™ and wizards	No
Macro support	No

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 64-Bit Value	All zeros	Specifies the contents of the ROM.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- ROM64X1: 64 x 1 Asynchronous Distributed (LUT) ROM
--          7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

ROM64X1_inst : ROM64X1
generic map (
   INIT => X"0000000000000000")
port map (
   O => O,   -- ROM output
   A0 => A0, -- ROM address[0]
   A1 => A1, -- ROM address[1]
   A2 => A2, -- ROM address[2]
   A3 => A3, -- ROM address[3]
   A4 => A4, -- ROM address[4]
   A5 => A5  -- ROM address[5]
);

-- End of ROM64X1_inst instantiation
```

Verilog Instantiation Template

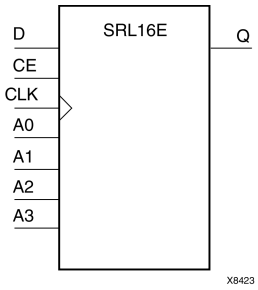
```
// ROM64X1: 64 x 1 Asynchronous Distributed (LUT) ROM (Mapped to a SliceM LUT6)
//          7 Series
// Xilinx HDL Libraries Guide, version 2012.2

ROM64X1 #(
   .INIT(64'h0000000000000000) // Contents of ROM
) ROM64X1_inst (
   .O(O),   // ROM output
   .A0(A0), // ROM address[0]
   .A1(A1), // ROM address[1]
   .A2(A2), // ROM address[2]
   .A3(A3), // ROM address[3]
   .A4(A4), // ROM address[4]
   .A5(A5)  // ROM address[5]
);

// End of ROM64X1_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

SRL16E

Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Clock Enable



Introduction

This design element is a shift register look-up table (LUT). The inputs A3, A2, A1, and A0 select the output length of the shift register.

The shift register can be of a fixed, static length or it can be dynamically adjusted.

- **To create a fixed-length shift register:** Drive the A3 through A0 inputs with static values. The length of the shift register can vary from 1 bit to 16 bits, as determined by the following formula: Length = (8 x A3) +(4 x A2) + (2 x A1) + A0 +1 If A3, A2, A1, and A0 are all zeros (0000), the shift register is one bit long. If they are all ones (1111), it is 16 bits long.
- **To change the length of the shift register dynamically:** Change the values driving the A3 through A0 inputs. For example, if A2, A1, and A0 are all ones (111) and A3 toggles between a one (1) and a zero (0), the length of the shift register changes from 16 bits to 8 bits. Internally, the length of the shift register is always 16 bits and the input lines A3 through A0 select which of the 16 bits reach the output.

The shift register LUT contents are initialized by assigning a four-digit hexadecimal number to an INIT attribute. The first, or the left-most, hexadecimal digit is the most significant bit. If an INIT value is not specified, it defaults to a value of four zeros (0000) so that the shift register LUT is cleared during configuration.

When CE is High, the data (D) is loaded into the first bit of the shift register during the Low-to-High clock (CLK) transition. During subsequent Low-to-High clock transitions, when CE is High, data shifts to the next highest bit position as new data is loaded. The data appears on the Q output when the shift register length determined by the address inputs is reached. When CE is Low, the register ignores clock transitions.

Logic Table

Inputs				Output
Am	**CE**	**CLK**	**D**	**Q**
Am	0	X	X	Q(Am)
Am	1	↑	D	Q(Am - 1)
m= 0, 1, 2, 3				

Port Descriptions

Port	Direction	Width	Function
Q	Output	1	Shift register data output
D	Input	1	Shift register data input
CLK	Input	1	Clock
CE	Input	1	Active high clock enable
A0	Input	1	Select[0] input
A1	Input	1	Select[1] input
A2	Input	1	Select[2] input
A3	Input	1	Select[3] input

Design Entry Method

Instantiation	Yes
Inference	Recommended
CORE Generator™ and wizards	No
Macro support	No

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexa-decimal	Any 16-Bit Value	All zeros	Sets the initial value of content and output of shift register after configuration.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- SRL16E: 16-bit shift register LUT with clock enable operating on posedge of clock (Mapped to SliceM LUT6)
--         7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

SRL16E_inst : SRL16E
generic map (
   INIT => X"0000")
port map (
   Q => Q,       -- SRL data output
   A0 => A0,     -- Select[0] input
   A1 => A1,     -- Select[1] input
   A2 => A2,     -- Select[2] input
   A3 => A3,     -- Select[3] input
   CE => CE,     -- Clock enable input
   CLK => CLK,   -- Clock input
   D => D        -- SRL data input
);
```

```
-- End of SRL16E_inst instantiation
```

Verilog Instantiation Template

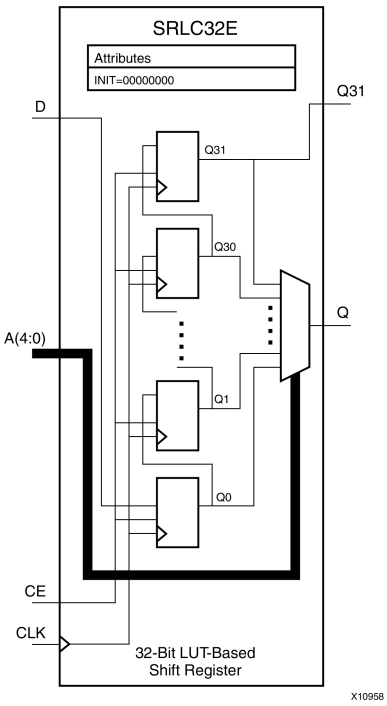
```
// SRL16E: 16-bit shift register LUT with clock enable operating on posedge of clock (Mapped to a SliceM LUT6
//         7 Series
// Xilinx HDL Libraries Guide, version 2012.2

SRL16E #(
   .INIT(16'h0000) // Initial Value of Shift Register
) SRL16E_inst (
   .Q(Q),       // SRL data output
   .A0(A0),     // Select[0] input
   .A1(A1),     // Select[1] input
   .A2(A2),     // Select[2] input
   .A3(A3),     // Select[3] input
   .CE(CE),     // Clock enable input
   .CLK(CLK),   // Clock input
   .D(D)        // SRL data input
);

// End of SRL16E_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

SRLC32E

Primitive: 32 Clock Cycle, Variable Length Shift Register Look-Up Table (LUT) with Clock Enable



Introduction

This design element is a variable length, 1 to 32 clock cycle shift register implemented within a single look-up table (LUT). The shift register can be of a fixed length, static length, or it can be dynamically adjusted by changing the address lines to the component. This element also features an active-high clock enable and a cascading feature in which multiple SRLC32Es can be cascaded in order to create greater shift lengths.

Port Descriptions

Port	Direction	Width	Function
Q	Output	1	Shift register data output
Q31	Output	1	Shift register cascaded output (connect to the D input of a subsequent SRLC32E)
D	Input	1	Shift register data input
CLK	Input	1	Clock
CE	Input	1	Active high clock enable
A	Input	5	Dynamic depth selection of the SRL A=00000 ==> 1-bit shift length A=11111 ==> 32-bit shift length

Design Entry Method

Instantiation	Yes
Inference	Recommended
CORE Generator™ and wizards	No
Macro support	No

If instantiated, the following connections should be made to this component:

- Connect the CLK input to the desired clock source, the D input to the data source to be shifted/stored and the Q output to either an FDCE or an FDRE input or other appropriate data destination.
- The CE clock enable pin can be connected to a clock enable signal in the design or else tied to a logic one if not used.
- The 5-bit A bus can either be tied to a static value between 0 and 31 to signify a fixed 1 to 32 bit static shift length, or else it can be tied to the appropriate logic to enable a varying shift depth anywhere between 1 and 32 bits.
- If you want to create a longer shift length than 32, connect the Q31 output pin to the D input pin of a subsequent SRLC32E to cascade and create larger shift registers.
- It is not valid to connect the Q31 output to anything other than another SRLC32E.
- The selectable Q output is still available in the cascaded mode, if needed.
- An optional INIT attribute consisting of a 32-bit Hexadecimal value can be specified to indicate the initial shift pattern of the shift register.
- (INIT[0] will be the first value shifted out.)

Available Attributes

Attribute	Type	Allowed Values	Default	Description
INIT	Hexa-decimal	Any 32-Bit Value	All zeros	Specifies the initial shift pattern of the SRLC32E.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- SRLC32E: 32-bit variable length shift register LUT
--          with clock enable (Mapped to a SliceM LUT6)
--          7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

SRLC32E_inst : SRLC32E
generic map (
   INIT => X"00000000")
port map (
   Q => Q,         -- SRL data output
   Q31 => Q31,     -- SRL cascade output pin
   A => A,         -- 5-bit shift depth select input
   CE => CE,       -- Clock enable input
   CLK => CLK,     -- Clock input
```

```
   D => D         -- SRL data input
);

-- End of SRLC32E_inst instantiation
```

Verilog Instantiation Template

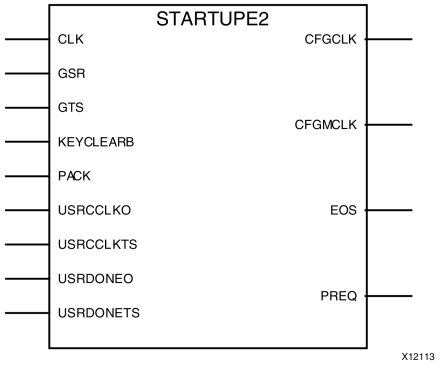
```
// SRLC32E: 32-bit variable length cascadable shift register LUT  (Mapped to a SliceM LUT6)
//          with clock enable
//          7 Series
// Xilinx HDL Libraries Guide, version 2012.2

SRLC32E #(
   .INIT(32'h00000000) // Initial Value of Shift Register
) SRLC32E_inst (
   .Q(Q),     // SRL data output
   .Q31(Q31), // SRL cascade output pin
   .A(A),     // 5-bit shift depth select input
   .CE(CE),   // Clock enable input
   .CLK(CLK), // Clock input
   .D(D)      // SRL data input
);

// End of SRLC32E_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

STARTUPE2

Primitive: STARTUP Block



Introduction

This design element is used to interface device pins and logic to the global asynchronous set/reset (GSR) signal, the global 3-state (GTS) dedicated routing or the internal configuration signals or a few of the dedicated configuration pins.

Port Descriptions

Port	Type	Width	Function
CFGCLK	Output	1	Configuration main clock output
CFGMCLK	Output	1	Configuration internal oscillator clock output
CLK	Input	1	User start-up clock input
EOS	Output	1	Active high output signal indicating the End Of Startup.
GSR	Input	1	Global Set/Reset input (GSR cannot be used for the port name)
GTS	Input	1	Global 3-state input (GTS cannot be used for the port name)
KEYCLEARB	Input	1	Clear AES Decrypter Key input from Battery-Backed RAM (BBRAM)
PACK	Input	1	PROGRAM acknowledge input
PREQ	Output	1	PROGRAM request to fabric output
USRCCLKO	Input	1	User CCLK input
USRCCLKTS	Input	1	User CCLK 3-state enable input
USRDONEO	Input	1	User DONE pin output control
USRDONETS	Input	1	User DONE 3-state enable output

Design Entry Method

Instantiation	Recommended
Inference	No
CORE Generator™ and wizards	No
Macro support	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
PROG_USR	STRING	"FALSE", "TRUE"	"FALSE"	Activate program event security feature. Requires encrypted bitstreams.
SIM_CCLK _FREQ	FLOAT(nS)	0.0 to 10.0	0.0	Set the Configuration Clock Frequency(ns) for simulation.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- STARTUPE2: STARTUP Block
--            7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

STARTUPE2_inst : STARTUPE2
generic map (
   PROG_USR => "FALSE",  -- Activate program event security feature. Requires encrypted bitstreams.
   SIM_CCLK_FREQ => 0.0  -- Set the Configuration Clock Frequency(ns) for simulation.
)
port map (
   CFGCLK => CFGCLK,       -- 1-bit output: Configuration main clock output
   CFGMCLK => CFGMCLK,     -- 1-bit output: Configuration internal oscillator clock output
   EOS => EOS,             -- 1-bit output: Active high output signal indicating the End Of Startup.
   PREQ => PREQ,           -- 1-bit output: PROGRAM request to fabric output
   CLK => CLK,             -- 1-bit input: User start-up clock input
   GSR => GSR,             -- 1-bit input: Global Set/Reset input (GSR cannot be used for the port name)
   GTS => GTS,             -- 1-bit input: Global 3-state input (GTS cannot be used for the port name)
   KEYCLEARB => KEYCLEARB, -- 1-bit input: Clear AES Decrypter Key input from Battery-Backed RAM (BBRAM)
   PACK => PACK,           -- 1-bit input: PROGRAM acknowledge input
   USRCCLKO => USRCCLKO,   -- 1-bit input: User CCLK input
   USRCCLKTS => USRCCLKTS, -- 1-bit input: User CCLK 3-state enable input
   USRDONEO => USRDONEO,   -- 1-bit input: User DONE pin output control
   USRDONETS => USRDONETS  -- 1-bit input: User DONE 3-state enable output
);

-- End of STARTUPE2_inst instantiation
```

Verilog Instantiation Template

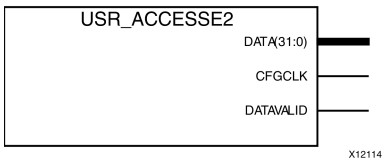
```
// STARTUPE2: STARTUP Block
//            7 Series
// Xilinx HDL Libraries Guide, version 2012.2

STARTUPE2 #(
   .PROG_USR("FALSE"),  // Activate program event security feature. Requires encrypted bitstreams.
   .SIM_CCLK_FREQ(0.0)  // Set the Configuration Clock Frequency(ns) for simulation.
)
STARTUPE2_inst (
   .CFGCLK(CFGCLK),       // 1-bit output: Configuration main clock output
   .CFGMCLK(CFGMCLK),     // 1-bit output: Configuration internal oscillator clock output
   .EOS(EOS),             // 1-bit output: Active high output signal indicating the End Of Startup.
   .PREQ(PREQ),           // 1-bit output: PROGRAM request to fabric output
   .CLK(CLK),             // 1-bit input: User start-up clock input
   .GSR(GSR),             // 1-bit input: Global Set/Reset input (GSR cannot be used for the port name)
   .GTS(GTS),             // 1-bit input: Global 3-state input (GTS cannot be used for the port name)
   .KEYCLEARB(KEYCLEARB), // 1-bit input: Clear AES Decrypter Key input from Battery-Backed RAM (BBRAM)
   .PACK(PACK),           // 1-bit input: PROGRAM acknowledge input
   .USRCCLKO(USRCCLKO),   // 1-bit input: User CCLK input
   .USRCCLKTS(USRCCLKTS), // 1-bit input: User CCLK 3-state enable input
   .USRDONEO(USRDONEO),   // 1-bit input: User DONE pin output control
   .USRDONETS(USRDONETS)  // 1-bit input: User DONE 3-state enable output
);

// End of STARTUPE2_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

USR_ACCESSE2

Primitive: Configuration Data Access



Introduction

This design element enables you to access a 32-bit register within the configuration logic. This enables fabric to access data that can be set from the bitstream.

Port Descriptions

Port	Type	Width	Function
CFGCLK	Output	1	Configuration Clock output
DATA<31:0>	Output	32	Configuration Data output
DATAVALID	Output	1	Active high data valid output

Design Entry Method

Instantiation	Recommended
Inference	No
CORE Generator™ and wizards	No
Macro support	No

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- USR_ACCESSE2: Configuration Data Access
--               7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

USR_ACCESSE2_inst : USR_ACCESSE2
port map (
   CFGCLK => CFGCLK,       -- 1-bit output: Configuration Clock output
   DATA => DATA,           -- 32-bit output: Configuration Data output
   DATAVALID => DATAVALID  -- 1-bit output: Active high data valid output
);

-- End of USR_ACCESSE2_inst instantiation
```

Verilog Instantiation Template

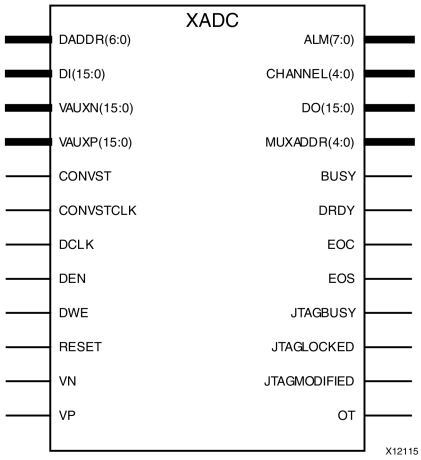
```
// USR_ACCESSE2: Configuration Data Access
//               7 Series
// Xilinx HDL Libraries Guide, version 2012.2

USR_ACCESSE2 USR_ACCESSE2_inst (
   .CFGCLK(CFGCLK),       // 1-bit output: Configuration Clock output
   .DATA(DATA),           // 32-bit output: Configuration Data output
   .DATAVALID(DATAVALID)  // 1-bit output: Active high data valid output
);

// End of USR_ACCESSE2_inst instantiation
```

For More Information

- See the *7 series FPGA SelectIO Resources User Guide (UG471)*.
- See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

XADC

Primitive: Dual 12-Bit 1MSPS Analog-to-Digital Converter



Introduction

The XADC includes a dual 12-bit, 1 Mega sample per second (MSPS) ADC and on-chip sensors. These ADCs are fully tested and specified (see the respective 7 series FPGAs data sheet). The ADCs provide a general-purpose, high-precision analog interface for a range of applications. The dual ADCs support a range of operating modes, for example, externally triggered and simultaneous sampling on both ADCs and various analog input signal types, for example, unipolar and differential. The ADCs can access up to 17 external analog input channels.
The XADC also includes a number of on-chip sensors that support measurement of the on-chip power supply voltages and die temperature. The ADC conversion data is stored in dedicated registers called status registers. These registers are accessible via the FPGA interconnect using a 16-bit synchronous read and write port called the Dynamic Reconfiguration Port (DRP). ADC conversion data is also accessible via the JTAG TAP. In the latter case, users are not required to instantiate the XADC because it is a dedicated interface that uses the existing FPGA JTAG infrastructure. AIf the XADC is not instantiated in a design, the device operates in a predefined mode (called default mode) that monitors on-chip temperature and supply voltages.
XADC operation is user defined by writing to the control registers using either the DRP or JTAG interface. It is also possible to initialize these register contents when the XADC is instantiated in a design using the block attributes.

Port Descriptions

Port	Type	Width	Function
ALM<7:0>	Output	8	Output alarm for temperature, Vccint, Vccaux and Vccbram. • ALM[0] - XADC temperature sensor alarm output. • ALM[1] - XADC Vccint sensor alarm output. • ALM[2] - XADC Vccaux sensor alarm output. • ALM[3] - XADC Vccbram sensor alarm output. • ALM[6:4] - Not defined.

Port	Type	Width	Function
BUSY	Output	1	ADC busy signal. This signal transitions High during an ADC conversion. This signal also transitions High for an extended period during an ADC or sensor calibration.
CHANNEL<4:0>	Output	5	Channel selection outputs. The ADC input MUX channel selection for the current ADC conversion is placed on these outputs at the end of an ADC conversion.
CONVST	Input	1	Convert start input. This input controls the sampling instant on the ADC(s) input and is only used in event mode timing. This input comes from the general-purpose interconnect in the FPGA logic.
CONVSTCLK	Input	1	Convert start clock input. This input is connected to a clock net. Like CONVST, this input controls the sampling instant on the ADC(s) inputs and is only used in event mode timing. This input comes from the local clock distribution network in the FPGA logic. Thus, for the best control over the sampling instant (delay and jitter), a global clock input can be used as the CONVST source.
DADDR<6:0>	Input	7	Address bus for the dynamic reconfiguration port.
DCLK	Input	1	Clock input for the dynamic reconfiguration port.
DEN	Input	1	Enable signal for the dynamic reconfiguration port.
DI<15:0>	Input	16	Input data bus for the dynamic reconfiguration port.
DO<15:0>	Output	16	Output data bus for dynamic reconfiguration port.
DRDY	Output	1	Data ready signal for the dynamic reconfiguration port.
DWE	Input	1	Write enable for the dynamic reconfiguration port.
EOC	Output	1	End of Conversion signal. This signal transitions to an active High at the end of an ADC conversion when the measurement is written to the status registers.
EOS	Output	1	End of Sequence. This signal transitions to active High when the measurement data from the last channel in an automatic channel sequence is written to the status registers.
JTAGBUSY	Output	1	Used to indicate that a JTAG DRP transaction is in progress.
JTAGLOCKED	Output	1	Indicates that a DRP port lock request has been made by the JTAG interface. This signal is also used to indicate that the DRP is ready for access (when Low).
JTAGMODIFIED	Output	1	Used to indicate that a JTAG Write to the DRP has occurred.
MUXADDR<4:0>	Output	5	These outputs are used in external multiplexer mode. They indicate the address of the next channel in a sequence to be converted. They provide the channel address for an external multiplexer.
OT	Output	1	Over-Temperature alarm
RESET	Input	1	Reset signal for the XADC control logic.
VAUXN<15:0>	Input	16	N-side auxiliary analog input
VAUXP<15:0>	Input	16	P-side auxiliary analog input
VN	Input	1	N-side analog input
VP	Input	1	P-side analog input

Design Entry Method

Instantiation	Yes
Inference	No
CORE Generator™ and wizards	Recommended
Macro support	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
INIT_4A	HEX	16'h0000 to 16'hffff	16'h0000	Sequence register 2
INIT_4B	HEX	16'h0000 to 16'hffff	16'h0000	Sequence register 3
INIT_4C	HEX	16'h0000 to 16'hffff	16'h0000	Sequence register 4
INIT_4D	HEX	16'h0000 to 16'hffff	16'h0000	Sequence register 5
INIT_4E	HEX	16'h0000 to 16'hffff	16'h0000	Sequence register 6
INIT_4F	HEX	16'h0000 to 16'hffff	16'h0000	Sequence register 7
INIT_5C	HEX	16'h0000 to 16'hffff	16'h0000	Vbram lower alarm threshold
INIT_40	HEX	16'h0000 to 16'hffff	16'h0000	Configuration register 0
INIT_41	HEX	16'h0000 to 16'hffff	16'h0000	Configuration register 1
INIT_42	HEX	16'h0000 to 16'hffff	16'h0800	Configuration register 2
INIT_43	HEX	16'h0000 to 16'hffff	16'h0000	Test register 0
INIT_44	HEX	16'h0000 to 16'hffff	16'h0000	Test register 1
INIT_45	HEX	16'h0000 to 16'hffff	16'h0000	Test register 2
INIT_46	HEX	16'h0000 to 16'hffff	16'h0000	Test register 3
INIT_47	HEX	16'h0000 to 16'hffff	16'h0000	Test register 4
INIT_48	HEX	16'h0000 to 16'hffff	16'h0000	Sequence register 0
INIT_49	HEX	16'h0000 to 16'hffff	16'h0000	Sequence register 1
INIT_50	HEX	16'h0000 to 16'hffff	16'h0000	Alarm limit register 0
INIT_51	HEX	16'h0000 to 16'hffff	16'h0000	Alarm limit register 1
INIT_52	HEX	16'h0000 to 16'hffff	16'h0000	Alarm limit register 2
INIT_53	HEX	16'h0000 to 16'hffff	16'h0000	Alarm limit register 3
INIT_54	HEX	16'h0000 to 16'hffff	16'h0000	Alarm limit register 4
INIT_55	HEX	16'h0000 to 16'hffff	16'h0000	Alarm limit register 5
INIT_56	HEX	16'h0000 to 16'hffff	16'h0000	Alarm limit register 6
INIT_57	HEX	16'h0000 to 16'hffff	16'h0000	Alarm limit register 7
INIT_58	HEX	16'h0000 to 16'hffff	16'h0000	Vbram upper alarm threshold

Attribute	Type	Allowed Values	Default	Description
INIT_59, INIT_5A, INIT_5B, INIT_5D, INIT_5E, INIT_5F	HEX	16'h0000 to 16'hffff	16'h0000	Reserved for future use
SIM_DEVICE	STRING	"7SERIES", "ZYNQ"	"7SERIES"	Selects target device to allow for proper simulation.
SIM_MONITOR_FILE	STRING	File name	None	Specify the file name (and directory if different from simulation directory) of file containing analog voltage and temperature data for XADC simulation behavior.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- XADC: Dual 12-Bit 1MSPS Analog-to-Digital Converter
--       7 Series
-- Xilinx HDL Libraries Guide, version 2012.2

XADC_inst : XADC
generic map (
   -- INIT_40 - INIT_42: XADC configuration registers
   INIT_40 => X"0000",
   INIT_41 => X"0000",
   INIT_42 => X"0800",
   -- INIT_48 - INIT_4F: Sequence Registers
   INIT_48 => X"0000",
   INIT_49 => X"0000",
   INIT_4A => X"0000",
   INIT_4B => X"0000",
   INIT_4C => X"0000",
   INIT_4D => X"0000",
   INIT_4F => X"0000",
   INIT_4E => X"0000",               -- Sequence register 6
   -- INIT_50 - INIT_58, INIT5C: Alarm Limit Registers
   INIT_50 => X"0000",
   INIT_51 => X"0000",
   INIT_52 => X"0000",
   INIT_53 => X"0000",
   INIT_54 => X"0000",
   INIT_55 => X"0000",
   INIT_56 => X"0000",
   INIT_57 => X"0000",
   INIT_58 => X"0000",
   INIT_5C => X"0000",
   -- Simulation attributes: Set for proper simulation behavior
   SIM_DEVICE => "7SERIES",          -- Select target device (values)
   SIM_MONITOR_FILE => "design.txt"  -- Analog simulation data file name
)
port map (
   -- ALARMS: 8-bit (each) output: ALM, OT
   ALM => ALM,                   -- 8-bit output: Output alarm for temp, Vccint, Vccaux and Vccbram
   OT => OT,                     -- 1-bit output: Over-Temperature alarm
   -- Dynamic Reconfiguration Port (DRP): 16-bit (each) output: Dynamic Reconfiguration Ports
   DO => DO,                     -- 16-bit output: DRP output data bus
   DRDY => DRDY,                 -- 1-bit output: DRP data ready
   -- STATUS: 1-bit (each) output: XADC status ports
```

```
   BUSY => BUSY,                 -- 1-bit output: ADC busy output
   CHANNEL => CHANNEL,           -- 5-bit output: Channel selection outputs
   EOC => EOC,                   -- 1-bit output: End of Conversion
   EOS => EOS,                   -- 1-bit output: End of Sequence
   JTAGBUSY => JTAGBUSY,         -- 1-bit output: JTAG DRP transaction in progress output
   JTAGLOCKED => JTAGLOCKED,     -- 1-bit output: JTAG requested DRP port lock
   JTAGMODIFIED => JTAGMODIFIED, -- 1-bit output: JTAG Write to the DRP has occurred
   MUXADDR => MUXADDR,           -- 5-bit output: External MUX channel decode
   -- Auxiliary Analog-Input Pairs: 16-bit (each) input: VAUXP[15:0], VAUXN[15:0]
   VAUXN => VAUXN,               -- 16-bit input: N-side auxiliary analog input
   VAUXP => VAUXP,               -- 16-bit input: P-side auxiliary analog input
   -- CONTROL and CLOCK: 1-bit (each) input: Reset, conversion start and clock inputs
   CONVST => CONVST,             -- 1-bit input: Convert start input
   CONVSTCLK => CONVSTCLK,       -- 1-bit input: Convert start input
   RESET => RESET,               -- 1-bit input: Active-high reset
   -- Dedicated Analog Input Pair: 1-bit (each) input: VP/VN
   VN => VN,                     -- 1-bit input: N-side analog input
   VP => VP,                     -- 1-bit input: P-side analog input
   -- Dynamic Reconfiguration Port (DRP): 7-bit (each) input: Dynamic Reconfiguration Ports
   DADDR => DADDR,               -- 7-bit input: DRP address bus
   DCLK => DCLK,                 -- 1-bit input: DRP clock
   DEN => DEN,                   -- 1-bit input: DRP enable signal
   DI => DI,                     -- 16-bit input: DRP input data bus
   DWE => DWE                    -- 1-bit input: DRP write enable
);

-- End of XADC_inst instantiation
```

Verilog Instantiation Template

```
// XADC: Dual 12-Bit 1MSPS Analog-to-Digital Converter
//       7 Series
// Xilinx HDL Libraries Guide, version 2012.2

XADC #(
   // INIT_40 - INIT_42: XADC configuration registers
   .INIT_40(16'h0000),
   .INIT_41(16'h0000),
   .INIT_42(16'h0800),
   // INIT_48 - INIT_4F: Sequence Registers
   .INIT_48(16'h0000),
   .INIT_49(16'h0000),
   .INIT_4A(16'h0000),
   .INIT_4B(16'h0000),
   .INIT_4C(16'h0000),
   .INIT_4D(16'h0000),
   .INIT_4F(16'h0000),
   .INIT_4E(16'h0000),              // Sequence register 6
   // INIT_50 - INIT_58, INIT5C: Alarm Limit Registers
   .INIT_50(16'h0000),
   .INIT_51(16'h0000),
   .INIT_52(16'h0000),
   .INIT_53(16'h0000),
   .INIT_54(16'h0000),
   .INIT_55(16'h0000),
   .INIT_56(16'h0000),
   .INIT_57(16'h0000),
   .INIT_58(16'h0000),
   .INIT_5C(16'h0000),
   // Simulation attributes: Set for proper simulation behavior
   .SIM_DEVICE("7SERIES"),          // Select target device (values)
   .SIM_MONITOR_FILE("design.txt")  // Analog simulation data file name
)
XADC_inst (
   // ALARMS: 8-bit (each) output: ALM, OT
   .ALM(ALM),                   // 8-bit output: Output alarm for temp, Vccint, Vccaux and Vccbram
   .OT(OT),                     // 1-bit output: Over-Temperature alarm
   // Dynamic Reconfiguration Port (DRP): 16-bit (each) output: Dynamic Reconfiguration Ports
   .DO(DO),                     // 16-bit output: DRP output data bus
   .DRDY(DRDY),                 // 1-bit output: DRP data ready
```

```
   // STATUS: 1-bit (each) output: XADC status ports
   .BUSY(BUSY),                 // 1-bit output: ADC busy output
   .CHANNEL(CHANNEL),           // 5-bit output: Channel selection outputs
   .EOC(EOC),                   // 1-bit output: End of Conversion
   .EOS(EOS),                   // 1-bit output: End of Sequence
   .JTAGBUSY(JTAGBUSY),         // 1-bit output: JTAG DRP transaction in progress output
   .JTAGLOCKED(JTAGLOCKED),     // 1-bit output: JTAG requested DRP port lock
   .JTAGMODIFIED(JTAGMODIFIED), // 1-bit output: JTAG Write to the DRP has occurred
   .MUXADDR(MUXADDR),           // 5-bit output: External MUX channel decode
   // Auxiliary Analog-Input Pairs: 16-bit (each) input: VAUXP[15:0], VAUXN[15:0]
   .VAUXN(VAUXN),               // 16-bit input: N-side auxiliary analog input
   .VAUXP(VAUXP),               // 16-bit input: P-side auxiliary analog input
   // CONTROL and CLOCK: 1-bit (each) input: Reset, conversion start and clock inputs
   .CONVST(CONVST),             // 1-bit input: Convert start input
   .CONVSTCLK(CONVSTCLK),       // 1-bit input: Convert start input
   .RESET(RESET),               // 1-bit input: Active-high reset
   // Dedicated Analog Input Pair: 1-bit (each) input: VP/VN
   .VN(VN),                     // 1-bit input: N-side analog input
   .VP(VP),                     // 1-bit input: P-side analog input
   // Dynamic Reconfiguration Port (DRP): 7-bit (each) input: Dynamic Reconfiguration Ports
   .DADDR(DADDR),               // 7-bit input: DRP address bus
   .DCLK(DCLK),                 // 1-bit input: DRP clock
   .DEN(DEN),                   // 1-bit input: DRP enable signal
   .DI(DI),                     // 16-bit input: DRP input data bus
   .DWE(DWE)                    // 1-bit input: DRP write enable
);

// End of XADC_inst instantiation
```

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.