Zynq-7000 All Programmable SoC Packaging and Pinout

Product Specification

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
06/14/2017	1.7	Added the XC7Z007S, XC7Z012S, and XC7Z014S devices where applicable. In Chapter 5: Updated the packages and Peak Package Reflow Body Temperature. Other updates to the Support for Thermal Models, Applied Pressure from Heat Sink to the Package via Thermal Interface Materials, and Conformal Coating sections. In Chapter 6: Updated Figure 6-1 to add the bar code marking and the Pb-free character. Added the Pb-free Character description as outlined in XCN16022: *Cross-ship of Lead-free Bump and Substrates in Lead-free (FFG/FBG/SBG) Packages* [Ref 14]. Revised the Bar Code section of Table 6-1 to include changes outlined in XCN16014: *Top Marking change for 7 Series, UltraScale, and UltraScale+ Products*. Updated the Legal Disclaimers on page 121.
03/01/2016	1.6	Updated to add RF1156 packages and RoHS compliant options (FFV packages) where applicable. In Table 1-5, updated the PS_POR_B and SRCC descriptions. Added the XC7Z035 in the FF/FFG/FFV900 package to Table 1-6. Updated many of the drawings in Chapter 4. Replaced the FF/FFG/FFV1156 package mechanical drawing in Figure 4-14. Completely revised Chapter 5, Thermal Specifications with industry standard guidelines for all sections. Updated the Thermal Interface Material section previously in Appendix B, and added the Applied Pressure from Heat Sink to the Package via Thermal Interface Materials. In Appendix B: Moved the *Reasons for* Thermal Interface Material section to Chapter 5. Removed the *Package Loading Specifications* section.
11/17/2014	1.5	Added the XC7Z035 device throughout the specification. Added a discussion on ULA materials on page 6. Added *Note* on page 27. Updated Figure 5-4: *Thermal Management Options for Flip-Chip BGA Packages*. In Table 5-2 and Figure 5-7, revised the peak temperature (body) values and the ramp-up rate and ramp-down rate to 2°C/s. Updated the Peak Package Reflow Body Temperature values in Table 5-3 and added Note 1. Updated Soldering Guidelines section. Added Post Reflow/Cleaning/Washing and Conformal Coating sections. Updated References.

Date	Version	Revision
06/11/2014	1.4	Added the RF900 package for the XQ7Z045 to Table 1-1, Table 1-3, Table 1-4, Table 2-1, Table 3-1, Figure 3-45, Figure 3-46, Figure 3-47, Figure 3-48, Figure 4-17, and Table 5-1. Updated the XC7Z015 bank numbering (Figure 1-2). Added XA7Z030 to Table 1-3, Table 1-4, Table 2-1, Table 3-1, Figure 1-4, Figure 3-25, Figure 3-26, Figure 3-27, Figure 3-28, Figure 4-6, Figure 4-7, and Table 5-1. Updated the PUDC_B and PS_MIO_VREF descriptions in Table 1-5. Added the GTP/GTX XY coordinates to Figure 1-2, Figure 1-4, Figure 1-5, and Figure 1-6. In Chapter 3, updated the memory groupings legend's DCI pin descriptions. Added the Heat Sink Removal Procedure and Package Pressure Handling Capacity sections. For clarity, updated Figure 5-7 and Table 5-3 with specific device information. Added Chapter 7, Packing and Shipping.
11/12/2013	1.3	Added the CLG485, SBG485, and FFG1156 packages. Added the XC7Z015 and XC7Z100 devices. Added the XA Zynq-7000 AP SoC devices (XA7Z010 and XA7Z020). Added the Zynq-7000Q AP SoC devices (XQ7Z020, XQ7Z030, and XQ7Z045) and the RF484 and RF676 packages. Updated the *Notice of Disclaimer*. Clarified the maximum and available PS I/O pins as 128 in Table 1-1 and Table 1-4. In Table 1-5, updated the PUDC_B description. Added Note 1 and updated the data in Table 5-1. Updated the Pb-Free Reflow Soldering in Chapter 5 discussion. Updated the MSL for flip-chip packages in Table 5-3. Removed the engineering sample notation from the top mark drawings in Figure 6-1. Updated Appendix A, Recommended PCB Design Rules.
02/14/2013	1.2	Updated VCCPLL in Table 1-5 and added Note 2. Updated Figure 3-8 and Figure 3-16. Revised Figure 4-1, increased the A and A2 maximum dimensions. Updated Figure 4-11. Added Figure 4-6, Figure 4-7. Figure 4-9, and Figure 4-12. In Table 5-1, updated thermal resistance data for the XC7Z010 and XC7Z020 devices. Updated Appendix B, Heat Sink Guidelines for Lidless Flip-Chip Packages.
09/24/2012	1.1	Added the CLG225 throughout document. Clarified RSVDVCC[3:1] and PS_MIO_VREF in Table 1-5, page 11. Added Note 9 to the DXN_0 description. Chapter 3: Updated the legends for the pinout diagrams. Chapter 4: Added mechanical drawings.
05/08/2012	1.0	Initial Xilinx release.

Table of Contents

Package Overview

Summary

This chapter covers the following topics:

- Introduction
- Device/Package Combinations and Maximum I/Os
- Pin Definitions
- Pin Compatibility Between Packages
- Die Level Bank Numbering Overview

Introduction

This section describes the pinouts for the Zynq®-7000 All Programmable (AP) SoC available in 0.8 mm pitch wire bond and various 0.8 mm and 1.0 mm pitch flip-chip and fine-pitch BGA packages.

Package inductance is minimized as a result of optimal placement and even distribution as well as an optimal number of Power and GND pins.

The FFG, FBG, SBG, and RFG flip-chip packages are RoHS 6 of 6 compliant, with exemption 15 where there is lead in the C4 bumps that are used to complete a viable electrical connection between the semiconductor die and the package substrate. The FFG, FBG, and SBG devices marked with the Pb-free Character are RoHS 6 of 6 compliant (without the use of exemption 15).

The FFV, FBV, SBV flip-chip packages are RoHS 6 of 6 compliant (without the use of exemption 15). The CLG non-flip chip packages are RoHS 6 of 6 compliant. Select packages include a Pb-only option.

All of the Zynq-7000 AP SoC devices supported in a particular package are pinout compatible.

The Zynq-7000 AP SoC contains a large number of fixed and flexible I/O. Zynq-7000 AP SoC has a constant 128 pins dedicated to memory interfaces (DDR I/O), multiplexed peripherals (MIO), and control. Programmable logic provides additional pins for SelectIO™ resources (SIO) and multi-gigabit serial transceivers (GTP or GTX) that scale by device as well as fixed pins for configuration and analog-to-digital conversion (XADC). SIO can be used to extend the MIO to further leverage the fixed peripherals of the processing system (PS).

Each device is split into I/O banks to allow for flexibility in the choice of I/O standards (see the *7 Series FPGAs SelectIO Resources User Guide* (UG471) [Ref 8]. The PS I/Os are described in the *Zynq-7000 All Programmable SoC Technical Reference Manual* (UG585) [Ref 1]. Table 1-5 provides definitions for all pin types.

Zynq-7000 AP SoCs flip-chip assembly materials are manufactured using ultra-low alpha (ULA) materials defined as <0.002 cph/cm^2 or materials that emit less than 0.002 alpha-particles per square centimeter per hour.

Device/Package Combinations and Maximum I/Os

Table 1-1 shows the maximum number of user I/Os possible in the Zynq-7000 AP SoC BGA packages.

Table 1-1: **Zynq-7000 AP SoC Package Specifications**

Packages[1]	Description	Package Specifications				
		Package Type	Pitch (mm)	Size (mm)	Maximum SelectIO Resources[2]	Maximum PS I/Os
CL/CLG225	Wire-bond	BGA	0.8	13 x 13	54	86
CL/CLG400		BGA	0.8	17 x 17	125	128
CL/CLG484		BGA	0.8	19 x 19	200	128
CL/CLG485		BGA	0.8	19 x 19	150	128
SBG/SBV485	Flip-chip lidless	BGA	0.8	19 x 19	150	128
FB/FBG/FBV484		BGA	1.0	23 x 23	163	128
FB/FBG/FBV676		BGA	1.0	27 x 27	250	128
FF/FFG/FFV676	Flip-chip	BGA	1.0	27 x 27	250	128
FF/FFG/FFV900		BGA	1.0	31 x 31	362	128
FF/FFG/FFV1156		BGA	1.0	35 x 35	400	128
RB484	Ruggedized Flip-Chip Lidless	BGA	1.0	23 x 23	163	128
RF/RFG676	Ruggedized Flip-chip	BGA	1.0	27 x 27	250	128
RF900		BGA	1.0	31 x 31	362	128
RF1156		BGA	1.0	35 x 35	400	128

Notes:

1. Leaded package options (CLxxx/FFxxx/FBxxx) are available. RoHS compliant options (FFG/FFV, FBG/FBV, SBG/SBV, CLG, and RFG) are described in the Introduction, page 6.
2. The maximum I/O numbers do not include pins in the configuration Bank 0 (Table 1-2) or the GT serial transceivers.

Table 1-2 lists the 17 dedicated pins.

Table 1-2: **Zynq-7000 AP SoC Pins in the Dedicated Configuration Bank (Bank0)**

DXP_0	VCCBATT_0	INIT_B_0	TDO_0	TDI_0	GNDADC_0
DXN_0	DONE_0	VN_0	TCK_0	VREFN_0	VCCADC_0
PROGRAM_B_0		VP_0	TMS_0	VREFP_0	CFGBVS_0

Serial Transceiver Channels by Device/Package

Table 1-3 lists the quantity of GTX serial transceiver channels for most of the Zynq-7000 AP SoC devices. In all devices, a serial transceiver channel is one set of MGTRXP, MGTRXN, MGTTXP, and MGTTXN pins. The XC7Z012S and XC7Z015, in the CLG485 package, have four GTP serial transceiver channels.

Table 1-3: **Serial Transceiver Channels by Device/Package**

Device	GTX (or GTP) Channels by Package					
	CL/CLG225 CL/CLG400 CL/CLG484	CL/CLG485	FB/FBG/FBV484 SBG/SBV485 RB484	FB/FBG/FBV676 FF/FFG/FFV676 RF/RFG676	FF/FFG/FFV900 RF900	FF/FFG/FFV1156 RF1156
XC7Z007S	–	–	–	–	–	–
XC7Z010 XA7Z010	–	–	–	–	–	–
XC7Z012S	–	4 (GTP)	–	–	–	–
XC7Z015	–	4 (GTP)	–	–	–	–
XC7Z014S	–	–	–	–	–	–
XC7Z020 XA7Z020	–	–	–	–	–	–
XC7Z030	–	–	4	4	–	–
XA7Z030	–	–	4	–	–	–
XC7Z035	–	–	–	8	16	–
XC7Z045	–	–	–	8	16	–
XC7Z100	–	–	–	–	16	16
XQ7Z020	–	–	–	–	–	–
XQ7Z030	–	–	4	4	–	–
XQ7Z045	–	–	–	8	16	–
XQ7Z100	–	–	–	–	16	16

Table 1-4 shows the number of available SelectIO resources (SIO), the number of differential SIO pairs, and the number of available PS I/Os for each Zynq-7000 AP SoC device/package combination. When applicable, it also lists the number of SIOs in the 3.3V-capable high-range (HR) banks and the number of 1.8V-capable high-performance (HP) banks.

IMPORTANT: *Because of package inductance, each device/package supports a limited number of simultaneous switching outputs. Limitations for specific applications can be determined using the Vivado Design Suite report_ssn tool. See the Simultaneous Switching Outputs section of the 7 Series FPGAs SelectIO Resources User Guide (UG471) [Ref 8] for more information.*

Table 1-4: **Available SIO and PS I/O Pins by Device/Package Combination**

Device	I/O Pins	CL225 CLG225			CL400 CLG400			CL484 CLG484 CLG485			FB484 FBG484 FBV484 RB484			SBG485 SBV485			FB676 FBG676 FBV676 FF676 FFG676 FFV676 RF676 RFG676			FF900 FFG900 FFV900 RF900			FF1156 FFG1156 FFV1156 RF1156		
		SIO		PS I/O	SIO		PS I/O	SIO		PS I/O	SIO		PS I/O	SIO		PS I/O	SIO		PS I/O	SIO		PS I/O	SIO		PS I/O
		HR	HP		HR	HP		HR	HP		HR	HP		HR	HP		HR	HP		HR	HP		HR	HP	
XC7Z007S	User I/O	54	0	86	100	0	128	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	Differential	27	0	–	48	0	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
XC7Z010 XA7Z010	User I/O	54	0	86	100	0	128	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	Differential	27	0	–	48	0	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
XC7Z012S	User I/O	–	–	–	–	–	–	150	0	128	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	Differential	–	–	–	–	–	–	72	0	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
XC7Z015	User I/O	–	–	–	–	–	–	150	0	128	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	Differential	–	–	–	–	–	–	72	0	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
XC7Z014S	User I/O	–	–	–	125	0	128	200	0	128	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	Differential	–	–	–	60	0	–	96	0	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
XC7Z020 XA7Z020	User I/O	–	–	–	125	0	128	200	0	128	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	Differential	–	–	–	60	0	–	96	0	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
XC7Z030	User I/O	–	–	–	–	–	–	–	–	–	100	63	128	50	100	128	100	150	128	–	–	–	–	–	–
	Differential	–	–	–	–	–	–	–	–	–	48	29	–	24	48	–	48	72	–	–	–	–	–	–	–
XA7Z030	User I/O	–	–	–	–	–	–	–	–	–	100	63	128	–	–	–	–	–	–	–	–	–	–	–	–
	Differential	–	–	–	–	–	–	–	–	–	48	29	–	–	–	–	–	–	–	–	–	–	–	–	–
XC7Z035	User I/O	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	100	150	128	212	150	128	–	–	–
	Differential	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	48	72	–	102	72	–	–	–	–
XC7Z045	User I/O	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	100	150	128	212	150	128	–	–	–
	Differential	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	48	72	–	102	72	–	–	–	–
XC7Z100	User I/O	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	212	150	128	250	150	128
	Differential	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	102	72	–	120	72	–
XQ7Z020	User I/O	–	–	–	125	0	128	200	0	128	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	Differential	–	–	–	60	0	–	96	0	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
XQ7Z030	User I/O	–	–	–	–	–	–	–	–	–	100	63	128	–	–	–	100	150	128	–	–	–	–	–	–
	Differential	–	–	–	–	–	–	–	–	–	48	29	–	–	–	–	48	72	–	–	–	–	–	–	–
XQ7Z045	User I/O	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	100	150	128	212	150	128	–	–	–
	Differential	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	48	72	–	102	72	–	–	–	–
XQ7Z100	User I/O	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	212	150	128	250	150	128
	Differential	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	102	72	–	120	72	–

Pin Definitions

Table 1-5 lists the pin definitions used in Zynq-7000 AP SoC packages.

Note: There are dedicated general purpose user I/O pins listed separately in Table 1-5. There are also multi-function pins where the pin names start with either IO_LXXY_ZZZ_# or IO_XX_ZZZ_#, where ZZZ represents one or more functions in addition to being general purpose user I/O. If not used for their special function, these pins can be user I/O.

Table 1-5: **Zynq-7000 AP SoC Pin Definitions**

Pin Name	Type	Direction	Description
User I/O Pins			
IO_LXXY_# IO_XX_#	Dedicated	Input/ Output	Most user I/O pins are capable of differential signaling and can be implemented as pairs. The top and bottom I/O pins are always single ended. Each user I/O is labeled IO_LXXY_#, where: • IO indicates a user I/O pin. • L indicates a differential pair, with XX a unique pair in the bank and Y = [P|N] for the positive/negative sides of the differential pair. • # indicates a bank number.
Configuration Pins			
For more information about these pins, see the *Configuration Pin Definitions* table in the *7 Series FPGAs Configuration User Guide* (UG470) [Ref 10]. See also the *Boot and Configuration* chapter in the *Zynq-7000 All Programmable SoC Technical Reference Manual* (UG585)[Ref 1].			
DONE_0	Dedicated(1)	Bidirectional	Active High, DONE indicates successful completion of configuration.
INIT_B_0	Dedicated(1)	Bidirectional (open-drain)	Active Low, indicates initialization of configuration memory.
PROGRAM_B_0	Dedicated(1)	Input	Active Low, asynchronous reset to configuration logic.
TCK_0	Dedicated(1)	Input	JTAG clock.
TDI_0	Dedicated(1)	Input	JTAG data input.
TDO_0	Dedicated(1)	Output	JTAG data output.
TMS_0	Dedicated(1)	Input	JTAG mode select.
CFGBVS_0	Dedicated(1)	Input	This pin selects the preconfiguration I/O standard type for the dedicated configuration bank 0. If the V_{CCO} for bank 0 is 2.5V or 3.3V, then this pin must be connected to V_{CCO_0}. If the V_{CCO} for bank 0 is less than or equal to 1.8V, then this pin should be connected to GND. ***Note:*** To avoid device damage, this pin must be connected correctly. See the *Configuration Bank Voltage Select* section in the *7 Series FPGAs Configuration User Guide* (UG470) [Ref 10] for more information.

Table 1-5: **Zynq-7000 AP SoC Pin Definitions *(Cont'd)***

Pin Name	Type	Direction	Description
PUDC_B	Multi-function	Input	Pull-Up During Configuration (bar) Active-Low PUDC_B input enables internal pull-up resistors on the SelectIO pins after power-up and during configuration. ◦ When PUDC_B is Low, internal pull-up resistors are enabled on each SelectIO pin. ◦ When PUDC_B is High, internal pull-up resistors are disabled on each SelectIO pin. PUDC_B must be tied either directly (or through a 1KΩ or less resistor) to VCCO_34 or GND. **CAUTION!** *Do not allow this pin to float before and during configuration.*
Power/Ground Pins			
GND	Dedicated	N/A	Ground, tied common.
VCCPINT	Dedicated	N/A	1.0V logic supply for PS. Independent from PL V_{CCINT} supply.
VCCPAUX	Dedicated	N/A	1.8V auxiliary power supply for PS. Independent from PL V_{CCAUX} supply.
VCCO_MIO0	Dedicated	N/A	1.8V–3.3V PS I/O supply for MIO bank 500.
VCCO_MIO1	Dedicated	N/A	1.8V–3.3V PS I/O supply for MIO bank 501.
VCCO_DDR	Dedicated	N/A	1.2V–1.8V DDR I/O supply.
VCCPLL(2)	Dedicated	N/A	1.8V PLL supply for PS. A 0.47 µF to 4.7 µF 0402 capacitor must be placed near the V_{CCPLL} BGA via. In addition, when powered by V_{CCPAUX}, the V_{CCPLL} must be filtered through a 120Ω at 100 MHz (size 0603) ferrite bead and a 10 µF (size 0603) decoupling capacitor to minimize PLL jitter.
VCCAUX	Dedicated	N/A	1.8V power-supply pins for auxiliary circuits.
VCCAUX_IO_G#(3)	Dedicated	N/A	1.8V/2.0V power-supply pins for auxiliary I/O circuits.
VCCINT	Dedicated	N/A	1.0V power-supply pins for the internal core logic.
VCCO_#(4)	Dedicated	N/A	Power-supply pins for the output drivers (per bank).
VCCBRAM	Dedicated	N/A	1.0V power-supply pins for the PL block RAM.
VCCBATT_0	Dedicated	N/A	Decryptor key memory backup supply; this pin should be tied to the appropriate V_{CC} or GND when not used.(5)
VREF	Multi-function	N/A	These are input threshold voltage pins. They become user I/Os when an external threshold voltage is not needed (per bank).
RSVDVCC[3:1]	Dedicated	N/A	Reserved pins—must be tied to V_{CCO_0}.
RSVDGND	Dedicated	N/A	Reserved pins—must be tied to GND.

Table 1-5: **Zynq-7000 AP SoC Pin Definitions *(Cont'd)***

Pin Name	Type	Direction	Description
PS MIO Pins			
PS_POR_B	Dedicated	Input	Power on reset. The PS_POR_B must be asserted to GND during the power-on sequence until V_{CCPINT}, V_{CCPAUX}, and V_{CCO_MIO0} have reached the minimum operating levels and the PS_CLK reference is within specification. When deasserted, the PS begins the boot process. Before V_{CCPINT} reaches 0.80V, at least one of these four conditions is required during the power-off stage: ◦ The PS_POR_B input is asserted to GND. ◦ The reference clock to the PS_CLK input is disabled. ◦ V_{CCPAUX} is lower than 0.70V. ◦ V_{CCO_MIO0} is lower than 0.90V. To ensure PS eFUSE integrity, the applicable condition must be held until V_{CCPINT} reaches 0.40V. See the *Zynq-7000 All Programmable SoC (Z-7010, Z-7015, and Z-7020) Data Sheet: DC and AC Switching Characteristics* (DS187) [Ref 4] and *Zynq-7000 All Programmable SoC (Z-7030, Z-7035, Z-7045, and Z-7100) Data Sheet: DC and AC Switching Characteristics* (DS191) [Ref 5] for more information on the power-on sequence.
PS_CLK	Dedicated	Input	System reference clock. PS_CLK must be between 30 MHz and 60 MHz.
PS_SRST_B	Dedicated	Input	System reset. For use with debuggers. When 0, forces the PS to enter the system reset sequence.
PS_MIO_VREF	Dedicated	Voltage Reference	The PS_MIO_VREF provides a reference voltage for the RGMII input receivers. If an RGMII interface is not being used, the PS_MIO_VREF pin can be left to float. If an RGMII interface is being used, tie this pin to a voltage equal to ½ V_{CCO_MIO1}. Example: When using a HSTL18 RGMII interface the V_{CCO_MIO1} is set to 1.8V. The PS_MIO_VREF must be set to 0.9V. A resistor divider can be used to generate the PS_MIO_VREF. See the *Zynq-7000 All Programmable SoC PCB Design Guide* (UG933) [Ref 2] for decoupling recommendations.
PS_MIO[53:0]	Multi-function	Input/Output	Multiuse I/O. Multiuse I/O can be configured to support multiple I/O interfaces. These interfaces include SPI and Quad-SPI flash, NAND, USB, Ethernet, SDIO, UART, SPI, and GPIO interfaces.

Table 1-5: **Zynq-7000 AP SoC Pin Definitions *(Cont'd)***

Pin Name	Type	Direction	Description
PS DDR Pins			
PS_DDR_CKP	Dedicated	Output	DDR differential clock positive.
PS_DDR_CKN	Dedicated	Output	DDR differential clock negative.
PS_DDR_CKE	Dedicated	Output	DDR clock enable.
PS_DDR_CS_B	Dedicated	Output	DDR chip select.
PS_DDR_RAS_B	Dedicated	Output	DDR RAS control signal.
PS_DDR_CAS_B	Dedicated	Output	DDR CAS control signal.
PS_DDR_WE_B	Dedicated	Output	DDR write enable signal.
PS_DDR_BA[2:0]	Dedicated	Output	DDR bank address.
PS_DDR_A[14:0]	Dedicated	Output	DDR row and column address.
PS_DDR_ODT	Dedicated	Output	DDR termination control.
PS_DDR_DRST_B	Dedicated	Output	DDR reset signal for DDR3 devices.
PS_DDR_DQ[31:0]	Dedicated	Input/Output	DDR data.
PS_DDR_DM[3:0]	Dedicated	Output	DDR data mask.
PS_DDR_DQS_P[3:0]	Dedicated	Input/Output	DDR differential data strobe positive.
PS_DDR_DQS_N[3:0]	Dedicated	Input/Output	DDR differential data strobe negative.
PS_DDR_VRP	Dedicated	Output	DDR DCI voltage reference positive. Used to calibrate DDR I/O drive strength. Connect to a resistor to GND. The value of the resistor should be twice the DDR termination and trace impedance.
PS_DDR_VRN	Dedicated	Output	DDR DCI voltage reference negative. Used to calibrate DDR I/O drive strength. Connect to a resistor to V_{CCO_DDR}. The value of the resistor should be twice the DDR termination and trace impedance.
PS_DDR_VREF[1:0]	Dedicated	Voltage Reference	Voltage reference for the DDR interface.
Analog to Digital Converter (XADC) Pins			
For more information, see the *XADC Package Pins* table in the *7 Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide* (UG480) [Ref 9].			
VCCADC_0(6)	Dedicated	N/A	XADC analog positive supply voltage.
GNDADC_0(6)	Dedicated	N/A	XADC analog ground reference.
VP_0(6)	Dedicated	Input	XADC dedicated differential analog input (positive side).
VN_0(6)	Dedicated	Input	XADC dedicated differential analog input (negative side).
VREFP_0(6)	Dedicated	N/A	1.25V reference input.
VREFN_ 0(6)	Dedicated	N/A	1.25V reference GND reference.
AD0P through AD15P AD0N through AD15N	Multi-function	Input	XADC (analog-to-digital converter) differential auxiliary analog inputs 0–15.

Table 1-5: **Zynq-7000 AP SoC Pin Definitions *(Cont'd)***

Pin Name	Type	Direction	Description
Multi-gigabit Serial Transceiver Pins (GTXE2 and GTPE2)			
For more information on the GTXE2 pins see the *Pin Description and Design Guidelines* section in the *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476) [Ref 11]. The GTPE2 pins are described in the *Pin Description and Design Guidelines* section of the *7 Series FPGAs GTP Transceivers User Guide* (UG482) [Ref 12].			
MGTXRXP[0:3] or MGTPRXP[0:3]	Dedicated	Input	Positive differential receive port.
MGTXRXN[0:3] or MGTPRXN[0:3]	Dedicated	Input	Negative differential receive port.
MGTXTXP[0:3] or MGTPTXP[0:3]	Dedicated	Output	Positive differential transmit port.
MGTXTXN[0:3] or MGTPTXN[0:3]	Dedicated	Output	Negative differential transmit port.
MGTAVCC_G#(7)	Dedicated	Input	1.0V analog power-supply pin for the receiver and transmitter internal circuits.
MGTAVTT_G#(7)	Dedicated	Input	1.2V analog power-supply pin for the transmit driver.
MGTVCCAUX_G#(7)	Dedicated	Input	1.8V auxiliary analog Quad PLL (QPLL) voltage supply for the GTXE2 transceivers only.
MGTREFCLK0/1P	Dedicated	Input	Positive differential reference clock for the transceivers.
MGTREFCLK0/1N	Dedicated	Input	Negative differential reference clock for the transceivers.
MGTAVTTRCAL	Dedicated	N/A	GTXE2 precision reference resistor pin for internal calibration termination. Not used for the XC7Z007S, XC7Z010, XC7Z012S, XC7Z014S, XC7Z015, or XC7Z020 devices.
MGTRREF	Dedicated	Input	Precision reference resistor pin for internal calibration termination.
Other Pins			
MRCC	Multi-function	Input	These are the clock capable I/Os driving BUFRs, BUFIOs, BUFGs, and MMCMs/PLLs. In addition, these pins can drive the BUFMR for multi-region BUFIO and BUFR support. These pins become regular user I/Os when not needed as a clock. When connecting a single-ended clock to the differential CC pair of pins, it must be connected to the positive (P) side of the pair. The MRCC (multi-region) pins, when used as single-region resource, can drive four BUFIOs and four BUFRs in a single bank.
SRCC	Multi-function	Input	These are the clock capable I/Os driving BUFRs, BUFIOs, BUFGs, and MMCMs/PLLs. These pins become regular user I/Os when not needed for clocks. When connecting a single-ended clock to the differential CC pair of pins, it must be connected to the positive (P) side of the pair. The SRCC (single-region) pins can drive four BUFIOs and four BUFRs in a single bank.

Table 1-5: **Zynq-7000 AP SoC Pin Definitions *(Cont'd)***

Pin Name	Type	Direction	Description
VRN[8]	Multi-function	N/A	This pin is for the DCI voltage reference resistor of N transistor (per bank, to be pulled High with reference resistor).
VRP[8]	Multi-function	N/A	This pin is for the DCI voltage reference resistor of P transistor (per bank, to be pulled Low with reference resistor).
DXP_0, DXN_0[9]	Dedicated	Input	Temperature-sensing diode pins (Anode: DXP; Cathode: DXN). The thermal diode is accessed by using the DXP and DXN pins in bank 0. When not used, tie to GND. To use the thermal diode an appropriate external thermal monitoring IC must be added. The recommended temperature monitoring solution for Zynq-7000 AP SoC devices uses the temperature sensor in the XADC block.
T0, T1, T2, or T3	Multi-function	Input	This pin belongs to the memory byte group 0-3.
T0_DQS, T1_DQS, T2_DQS, or T3_DQS	Multi-function	Input/Output	The DDR DQS strobe pin that belongs to the memory byte group T0–T3.

Notes:

1. All dedicated pins (JTAG and configuration) are powered by V_{CCO_0}.
2. See the V_{CCPLL}*—PS PLL Supply* section in the *Processing System Power and Signaling* chapter in the *Zynq-7000 All Programmable SoC PCB Design Guide* (UG933) [Ref 2].
3. For devices that do not include $V_{CCAUX\_IO\_G\#}$ pins, auxiliary I/O circuits are powered by V_{CCAUX} pins.
4. V_{CCO} pins in unbonded banks must be connected to the V_{CCO} for that bank for package migration. Do NOT connect unbonded V_{CCO} pins to different supplies. Without a package migration requirement, V_{CCO} pins in unbonded banks can be tied to a common supply (V_{CCO} or ground).
5. Refer to the data sheet for V_{CCBATT_0} specifications.
6. See the *7 Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide* (UG480) [Ref 9] for the default connections required to support on-chip monitoring.
7. In packages with only one MGT power group, the MGTAVCC_G#, MGTAVTT_G#, and MGTVCCAUX_G# pins are labeled without the _G#. These pins also appear without a number in the power and GND placement diagrams in Chapter 3, Device Diagrams.
8. The DCI guidelines in the Zynq-7000 AP SoC devices are different from previous Virtex device DCI guidelines. See the DCI sections in the *7 Series FPGAs SelectIO Resources User Guide* (UG471) [Ref 8] for more information on the VRN/VRP pins.
9. The DXN_0 pin is not accessible in the XC7Z007S/XC7Z010/XA7Z010 devices in the CL225/CLG225 package. For designs connecting the thermal diode in this package to a thermal monitoring IC, use GNDADC_0 in place of DXN_0.

Pin Compatibility Between Packages

Zynq-7000 AP SoC devices are pin compatible only with other Zynq-7000 AP SoC devices in the same package. In addition, FB/FBG/FBV and FF/FFG/FFV packages of the same pin-count designator are pin compatible. Table 1-6 shows the pin compatible devices available for each Zynq-7000 AP SoC device package. Pins that are available in one device but are not available in another device with a compatible package include the other device's name in the *No Connect* column of the package file. These pins are labeled as *No Connects* in the other device's package file.

Some FB/FBG/FBV packages include V_{CCAUX_IO} pins, but they are not utilized by the I/O. These pins are placeholders to ensure pin compatibility with FF/FFG/FFV packages. In the FF/FFG/FFV packages, if the high-performance option is chosen for the HP I/O, the V_{CCAUX_IO} pins must be connected to a power supply separate from V_{CCAUX}. Therefore, if there are plans to migrate to FF/FFG/FFV packages, V_{CCAUX_IO} must be connected to the appropriate voltage regulator.

Table 1-6: **Pin Compatibility**

Package	Pin Compatible Devices			
CL225/CLG225	7Z007S	7Z010		
CL400/CLG400	7Z007S	7Z010	7Z014S	7Z020
CL484/CLG484	7Z014S	7Z020		
SB/SBG/SBV485 or CL/CLG485	7Z012S	7Z015	7Z030	
FB/FBG/FBV484 or RB484	7Z030			
FB/FBG/FBV676 or FF/FFG/FFV676 or RF/RFG676	7Z030		7Z035	7Z045
FF/FFG/FFV900 or RF900	7Z035		7Z045	7Z100
FF/FFG/FFV1156 or RF1156	7Z100			

Notes:

1. Pin compatible packages as well as the FB/FBG/FBV and FF/FFG/FFV packages have substantially different decoupling capacitor recommendations. Refer to the *Zynq-7000 All Programmable SoC PCB Design Guide* (UG933) [Ref 2].

Die Level Bank Numbering Overview

Banking and Clocking Summary

- The center clocking backbone contains all vertical clock tracks and clock buffer connectivity.
- The CMT backbone contains all vertical CMT connectivity and is located in the CMT column.
- Not all banks are bonded out in every part/package combination.
- GTP/GTX columns summary:
  - One bank = One GTP/GTX Quad = Four transceivers = Four GTPE2 or GTXE2 primitives.
  - Not all GTP/GTX Quads are bonded out in every package.
- I/O banks summary:
  - Each bank has four pairs of clock capable (CC) inputs for four differential or four single-ended clock inputs.
    - Can connect to the CMT in the same region and the region above and below (with restrictions).
    - Two MRCC pairs can connect to the BUFRs and BUFIOs in the same region/banks and the regions/banks above and below.
    - Two SRCC pairs can only connect to the BUFRs and BUFIOs in the same region/bank.
    - MRCC and SRCC inputs can connect to the CMT and BUFGs to provide global clocking.
  - Each user I/O bank has 50 single-ended I/Os or 24 differential pairs (48 differential I/Os). The top and bottom I/O pin are always single ended. All 50 pads of a bank are not always bonded out to pins.
- Bank locations of dedicated and dual-purpose pins:
  - In Zynq-7000 AP SoC devices, banks 500 and 501 contain the PS MIO pins and bank 502 contains the PS DDR pins. Bank 35 contains the XADC auxiliary inputs.
  - All dedicated configuration I/Os (bank 0) are 3.3V capable
- The physical XY locations for each IDELAYCTRL start at X0Y0 in the bottom left-most bank. The locations then increment by one starting with the lowest bank number in each column in the vertical Y direction and by one for each column in the horizontal X direction. IDELAYCTRLs are located in each of the HROWs.

Figure 1-1 through Figure 1-6 visually describe a die view of the PL bank numbering.

XC7Z007S, XC7Z010, and XA7Z010 Banks

Figure 1-1 shows the I/O banks for the XC7Z007S, XC7Z010, and XA7Z010. These devices do not include transceiver banks.

CL225/CLG225 Packages

- All HR I/O banks 34 and 35 are partially bonded out on this package.
- PS banks 500, 501, and 502 are partially bonded out on this package.

CL400/CLG400 Packages

- All HR I/O banks are fully bonded out.
- All PS banks are fully bonded out.

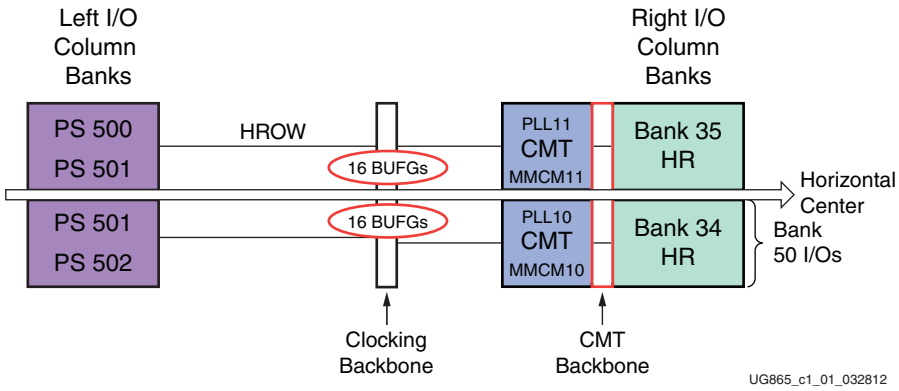


Figure 1-1: **XC7Z007S, XC7Z010, and XA7Z010 Banks**

XC7Z012S and XC7Z015 Banks

Figure 1-2 shows the I/O banks for the XC7Z012S and XC7Z015.

CL485/CLG485 Packages

- HR I/O banks 13, 34, and 35 are fully bonded out.
- All GTP Quads are fully bonded out.
- All PS banks are fully bonded out.

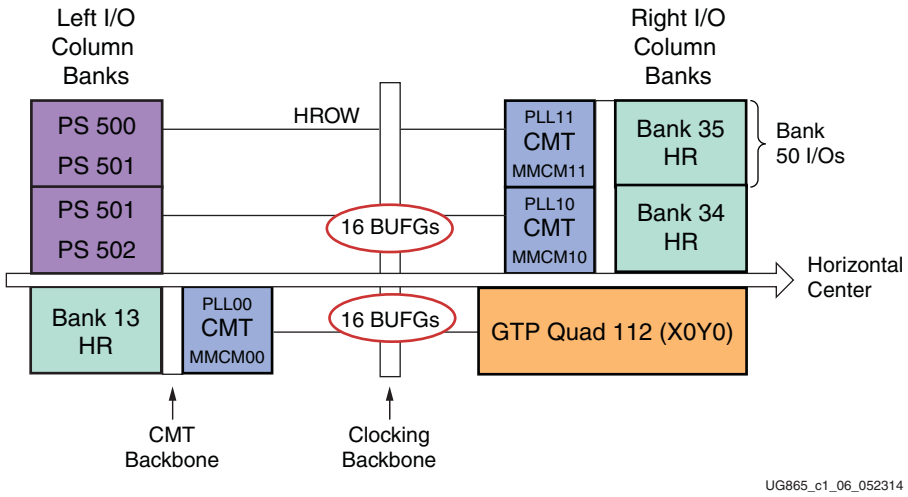


Figure 1-2: **XC7Z012S and XC7Z015 Banks**

XC7Z014S, XC7Z020, XA7Z020, and XQ7Z020 Banks

Figure 1-3 shows the I/O banks for the XC7Z014S, XC7Z020, XA7Z020, and XQ7Z020. These devices do not include transceiver banks.

CL400/CLG400 Packages

- HR I/O bank 33 is not bonded out in this package.
- HR I/O bank 13 is partially bonded out in this package.
- All PS banks are fully bonded out.

CL484/CLG484 Packages

- All HR I/O banks are fully bonded out.
- All PS banks are fully bonded out.

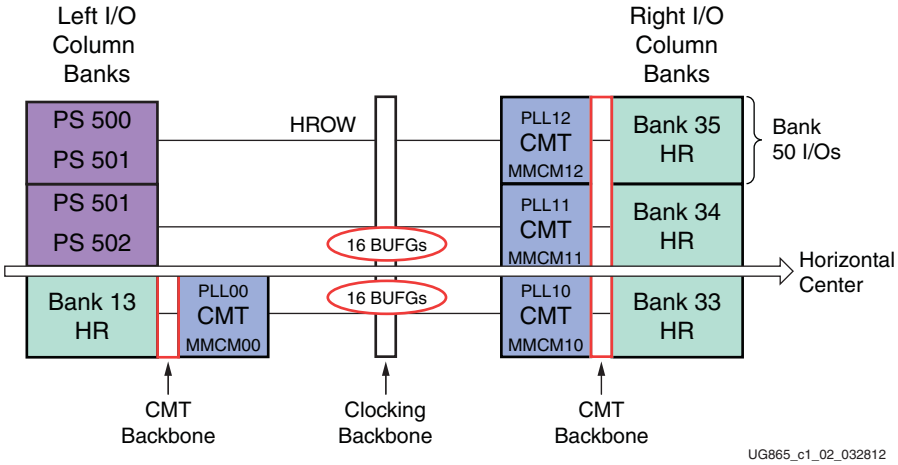


Figure 1-3: **XC7Z014S, XC7Z020, XA7Z020, and XQ7Z020 Banks**

XC7Z030, XA7Z030, and XQ7Z030 Banks

Figure 1-4 shows the I/O banks for the XC7Z030, XA7Z030, and XQ7Z030. In all packages listed:

- All GTX Quads are fully bonded out.
- All PS banks are fully bonded out.

FB484/FBG484/FBV484 and RB484 Packages

- All HR I/O banks are fully bonded out.
- HP I/O bank 33 is not bonded out in this package.
- HP I/O bank 35 is partially bonded out in this package.

SBG485/SBV485 Packages

- HR I/O bank 13 is fully bonded out.
- HP I/O banks 34 and 35 are fully bonded out.
- HR I/O bank 12 is not bonded out in this package.
- HP I/O bank 33 is not bonded out in this package.

FB676/FBG676/FBV676, FF676/FFG676/FFV676, and RF676 Packages

- All HR I/O banks are fully bonded out.
- All HP I/O banks are fully bonded out.

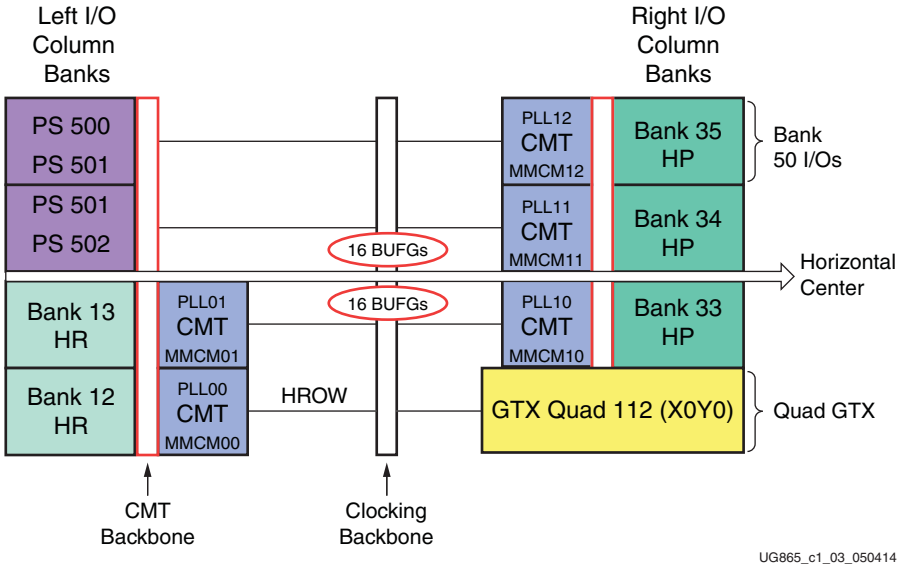


Figure 1-4: **XC7Z030, XA7Z030, and XQ7Z030 Banks**

XC7Z035, XC7Z045, and XQ7Z045 Banks

Figure 1-5 shows the I/O banks for the XC7Z035, XC7Z045, and XQ7Z045.

FB676/FBG676/FBV676, FF676/FFG676/FFV676, and RF676/RFG676 Packages

- HR I/O banks 9, 10, and 11 are not bonded out in this package.
- All HP I/O banks are fully bonded out.
- GTX Quads 109 and 110 are not bonded out in this package.
- All PS banks are fully bonded out.

FF900/FFG900/FFV900 and RF900 Packages

- HR I/O bank 9 is partially bonded out in this package.
- All HP I/O banks are fully bonded out.
- All GTX Quads are fully bonded out.
- All PS banks are fully bonded out.

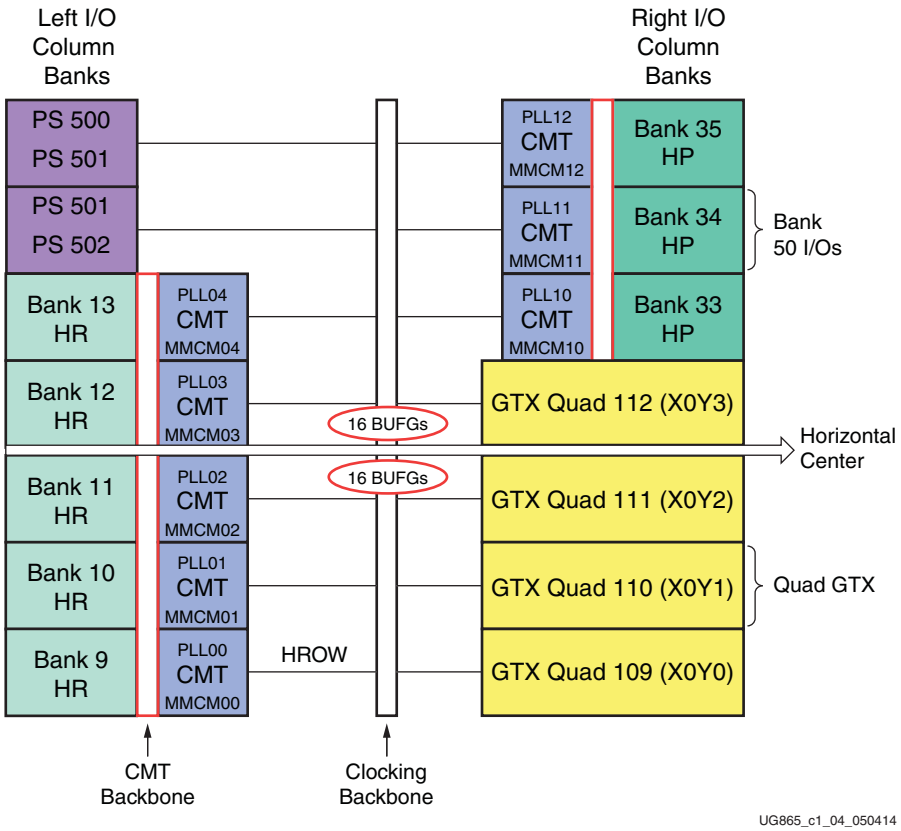


Figure 1-5: **XC7Z035, XC7Z045, and XQ7Z045 Banks**

XC7Z100 or XQ7Z100 Banks

Figure 1-6 shows the I/O banks for the XC7Z100 or XQ7Z100.

FF900/FFG900/FFV900 or RF900 Packages

- HR I/O bank 9 is partially bonded out in this package.
- All HP I/O banks are fully bonded out.
- All GTX Quads are fully bonded out.
- All PS banks are fully bonded out.

FF1156/FFG1156/FFV1156 or RF1156 Packages

- All HR I/O banks are fully bonded out.
- All HP I/O banks are fully bonded out.
- All GTX Quads are fully bonded out.
- All PS banks are fully bonded out.

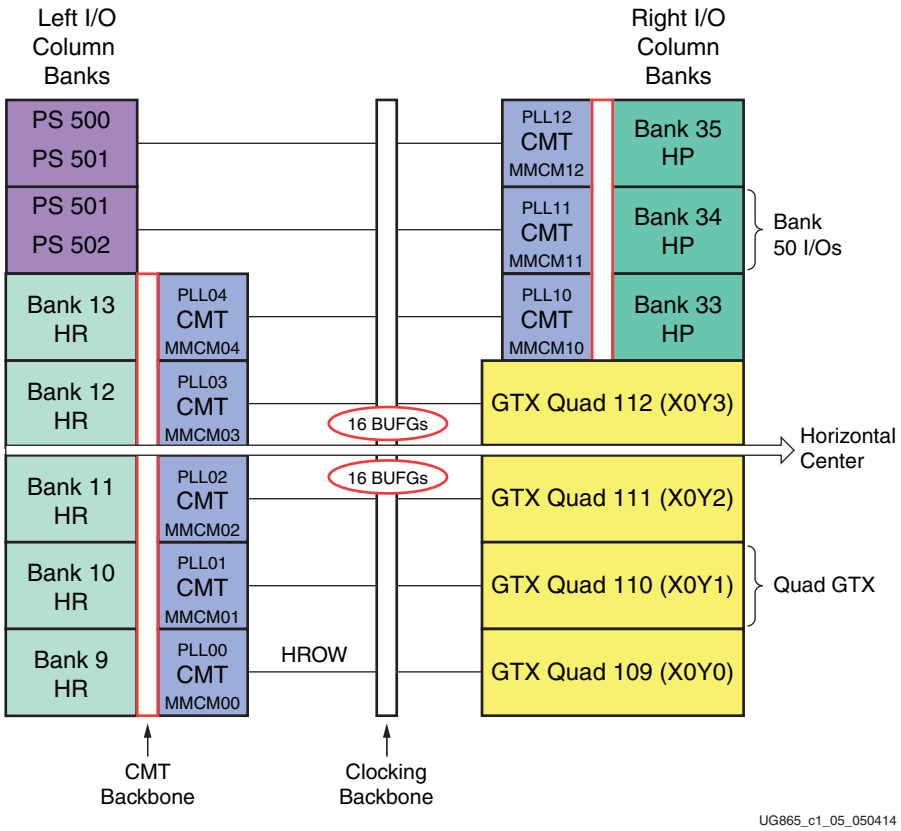


Figure 1-6: **XC7Z100 or XQ7Z100 Banks**

Zynq-7000 AP SoC Package Files

About ASCII Package Files

The ASCII files for each package include a comma-separated-values (CSV) version and a text version optimized for a browser or text editor. Each of the files consists of the following:

- Device/Package name (Device—Package), date and time of creation
- Eight columns containing data for each pin:
  - Pin—Pin location on the package.
  - Pin Name—The name of the assigned pin.
  - Memory Byte Group—Memory byte group between 0 and 3. For more information on the memory byte group, see the *7 Series FPGAs Memory Interface Solutions User Guide* (UG586) [Ref 7].
  - Bank—Bank number.
  - V_{CCAUX} Group—Number corresponding to the V_{CCAUX_IO} power supply for the given pin. V_{CCAUX} is shown for packages with only one V_{CCAUX} group.
  - Super Logic Region—Number corresponding to the super logic region (SLR) in the devices implemented with stacked silicon interconnect (SSI) technology.
  - I/O Type—CONFIG, HR, HP, MIO, DDR, or GTP/GTX depending on the I/O type. For more information on the I/O type, see the *7 Series FPGAs SelectIO Resources User Guide* (UG471) [Ref 8].
  - No-Connect—This list of devices is used for migration between devices that have the same package size and are not connected at that specific pin.
- Total number of pins in the package.

ASCII Pinout Files

This chapter includes the pinout information for the Zynq-7000 AP SoC by device.

The files listed in Table 2-1 are linked and consolidated here:

www.xilinx.com/support/package-pinout-files/zynq7000-pkgs.html

Table 2-1: **Zynq-7000 AP SoC Package/Device Pinout Files**

Device	CL225 CLG225	CL400 CLG400	CL484 CLG484	CLG485	SBG485 SBV485	FB484 FBG484 FBV484 RB484	FB676 FBG676 FBV676	FF676 FFG676 FFV676 RF676 RFG676	FF900 FFG900 FFV900 RF900	FF1156 FFG1156 FFV1156 RF1156
XC7Z007S	CLG225	CLG400								
XC7Z010 XA7Z010	CLG225	CLG400								
XC7Z012S				CLG485						
XC7Z015				CLG485						
XC7Z014S		CLG400	CLG484							
XC7Z020 XA7Z020		CLG400	CLG484							
XC7Z030					SBG485	FBG484	FBG676	FFG676		
XA7Z030						FBG484				
XC7Z035							FBG676	FFG676	FFG900	
XC7Z045							FBG676	FFG676	FFG900	
XC7Z100									FFG900	FFG1156
XQ7Z020		CL400	CL484							
XQ7Z030						RB484		RF676		
XQ7Z045								RF676	RF900	
XQ7Z100									RF900	RF1156

Download all available Zynq-7000 AP SoC ASCII package files (TXT and CSV file formats) from this link:

www.xilinx.com/support/packagefiles/z7packages/z7all.zip

Device Diagrams

Summary

This chapter provides pinout, high-performance and high-range I/O bank, memory groupings, and power and ground placement diagrams for each Zynq-7000 AP SoC package/device combination.

The figures provide a top-view perspective.

The symbols for the multi-function I/O pins are represented by only one of the available pin functions; with precedence (by functionality) in this order:

- PUDC_B
- AD0P/AD0N–AD15P/AD15N
- VRN, VRP, or VREF
- DQS, MRCC, or SRCC

For example, a pin description such as IO_L8P_SRCC_35 is represented with a SRCC symbol, a pin description such as IO_L19N_T3_AD0P_VREF_35 is represented with a AD0P/AD0N-AD15P/AD15N symbol, and a pin description such as IO_L21N_T3_DQS_PUDC_B_34 is represented with a PUDC_B symbol.

Note: For brevity, prefix for Xilinx commercial (XC) devices are used when the defense-grade (XQ) or the automotive (XA) could also be available. See the Zynq-7000 Product Table for ordering options.

Zynq-7000 AP SoC Device Diagrams

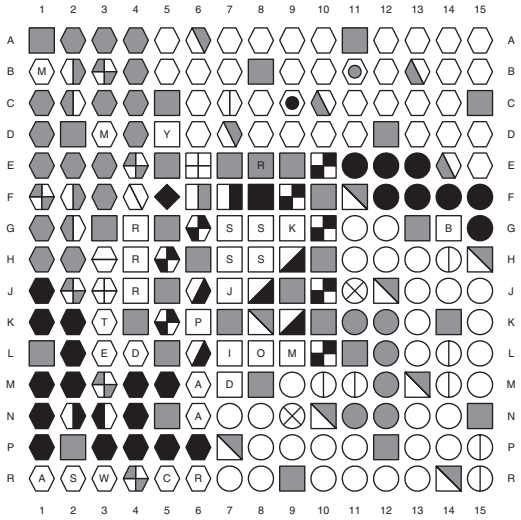
The device diagrams are linked from Table 3-1.

Note: Figures for some Zynq-7000 AP SoC devices are in development.

Table 3-1: **Zynq-7000 AP SoC Device Diagrams Cross-Reference**

Device	CL225 CLG225	CL400 CLG400	CL484 CLG484	CLG485	SBG485 SBV485	FB484 FBG484 FBV484 RB484	FB676 FBG676 FBV676	FF676 FFG676 FFV676 RF676	FF900 FFG900 FFV900 RF900	FF1156 FFG1156 FFV1156 RF1156
XC7Z007S	page 29	page 32								
XC7Z010 XA7Z010	page 29	page 32								
XC7Z012S				page 34						
XC7Z015				page 34						
XC7Z014S		page 37	page 40							
XC7Z020 XA7Z020		page 37	page 40							
XC7Z030 XA7Z030					page 43	page 46	page 49	page 52		
XC7Z035							page 55	page 58	page 62	
XC7Z045							page 55	page 58	page 62	
XC7Z100									page 66	page 70
XQ7Z020		page 37	page 40							
XQ7Z030						page 46		page 52		
XQ7Z045								page 58	page 62	
XQ7Z100									page 66	page 70

CL225/CLG225 Packages—XC7Z007S, XC7Z010, and XA7Z010



User I/O Pins	Dedicated Pins	Other Pins	PS MIO Pins	PS DDR Pins
IO_LXXY_# IO_XX_#	CFGBVS_0 DONE_0 DXP_0 DXN_0 GNDADC_0 INIT_B_0 PROGRAM_B_0 TCK_0 TDI_0 TDO_0 TMS_0 VCCADC_0 VCCBATT_0 VP_0 VN_0 VREFP_0 VREFN_0	GND VCCAUX_IO_G# VCCAUX VCCINT VCCO_# VCCBRAM VCCPINT VCCPAUX VCCO_MIO0 VCCO_MIO1 VCCO_DDR VCCPLL RSVDVCC[3:1] RSVDGND NC	PS_POR_B PS_CLK PS_SRST_B PS_MIO_VREF PS_MIO	PS_DDR_CKP PS_DDR_CKN PS_DDR_CKE PS_DDR_CS_B PS_DDR_RAS_B PS_DDR_CAS_B PS_DDR_WE_B PS_DDR_BA PS_DDR_A PS_DDR_ODT PS_DDR_DRST_B PS_DDR_DQ PS_DDR_DM PS_DDR_DQS_P PS_DDR_DQS_N PS_DDR_VRP PS_DDR_VRN PS_DDR_VREF
Multi–Function Pins				
PUDC_B AD0P/AD0N–AD15P/AD15N VRN VRP VREF DQS MRCC SRCC				

ug865_c3_05_091712

Figure 3-1: **CL225/CLG225 Packages—XC7Z007S, XC7Z010, and XA7Z010 Pinout Diagram**

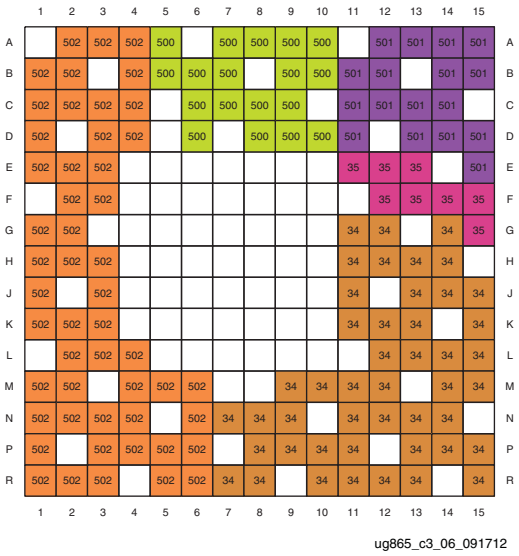


Figure 3-2: **CL225/CLG225 Packages—XC7Z007S, XC7Z010, and XA7Z010 I/O Banks**

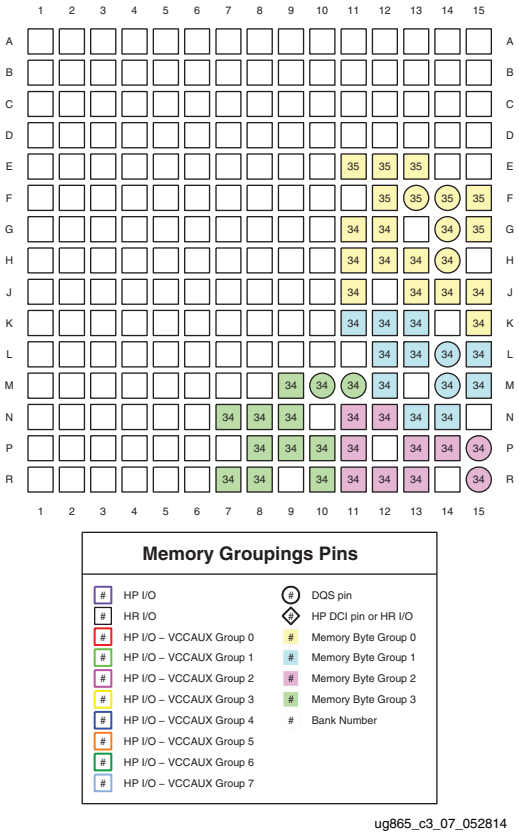


Figure 3-3: **CL225/CLG225 Packages—XC7Z007S, XC7Z010, and XA7Z010 Memory Groupings**

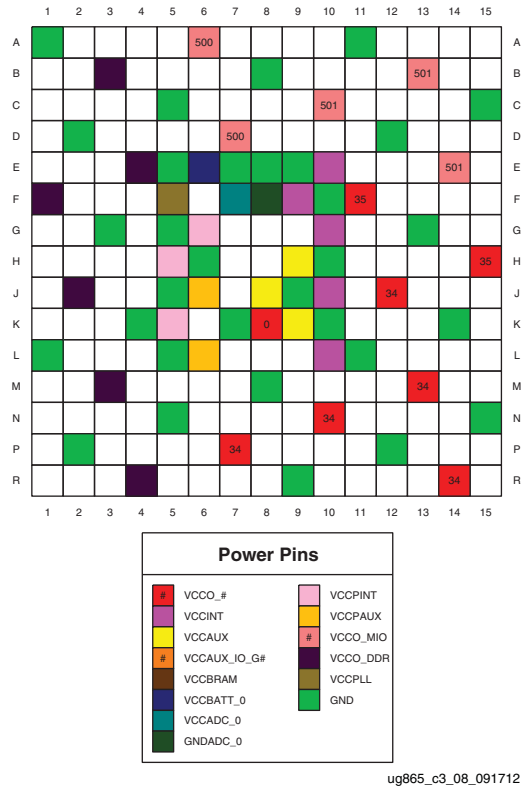


Figure 3-4: **CL225/CLG225 Packages—XC7Z007S, XC7Z010, and XA7Z010 Power and GND Placement**

CL400/CLG400 Packages—XC7Z007S, XC7Z010, and XA7Z010

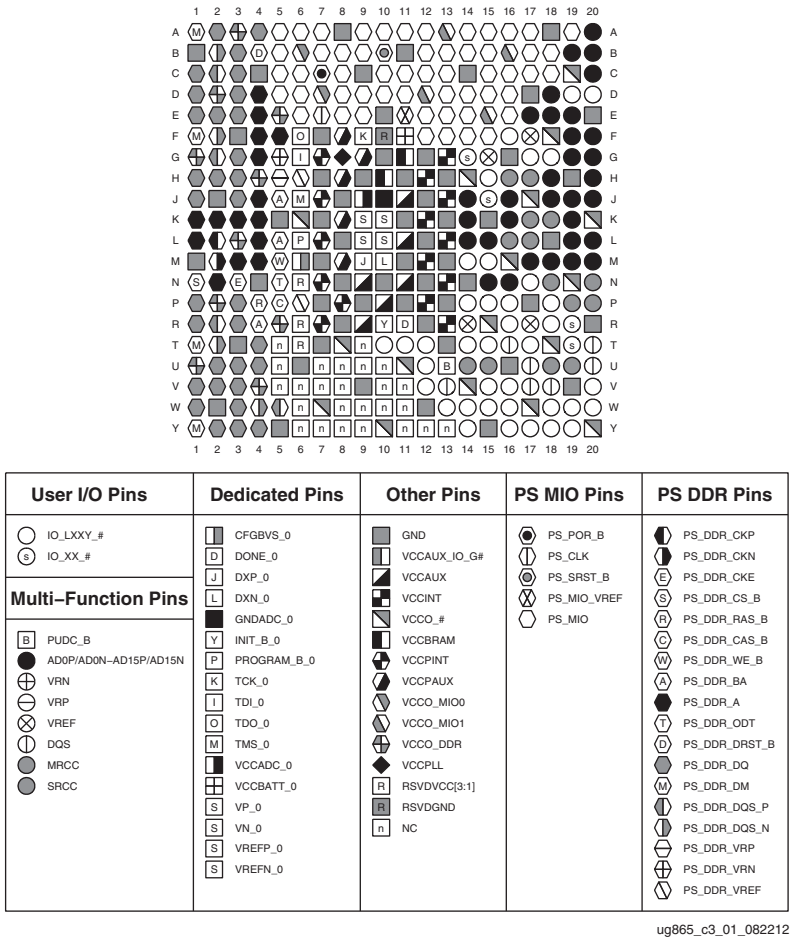


Figure 3-5: **CL400/CLG400 Packages—XC7Z007S, XC7Z010, and XA7Z010 Pinout Diagram**

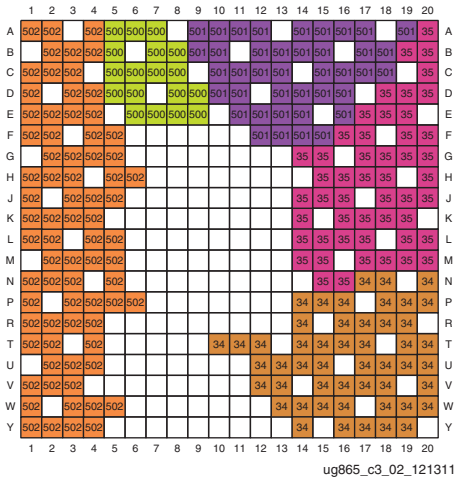


Figure 3-6: **CL400/CLG400 Packages—XC7Z007S, XC7Z010, and XA7Z010 I/O Banks**

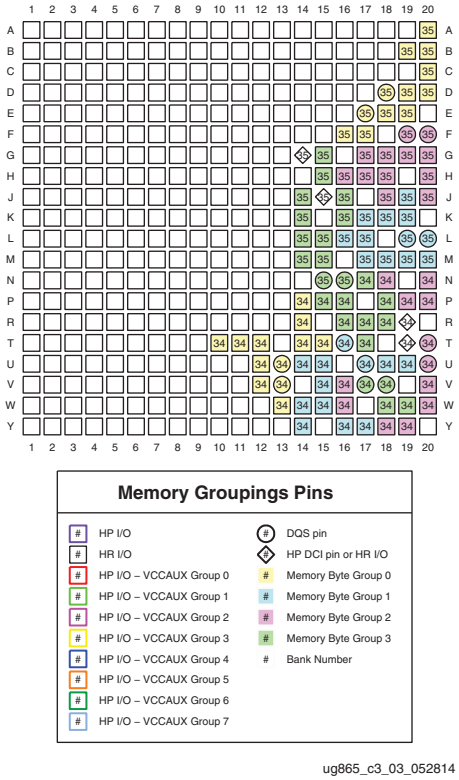


Figure 3-7: **CL400/CLG400 Packages—XC7Z007S, XC7Z010, and XA7Z010 Memory Groupings**

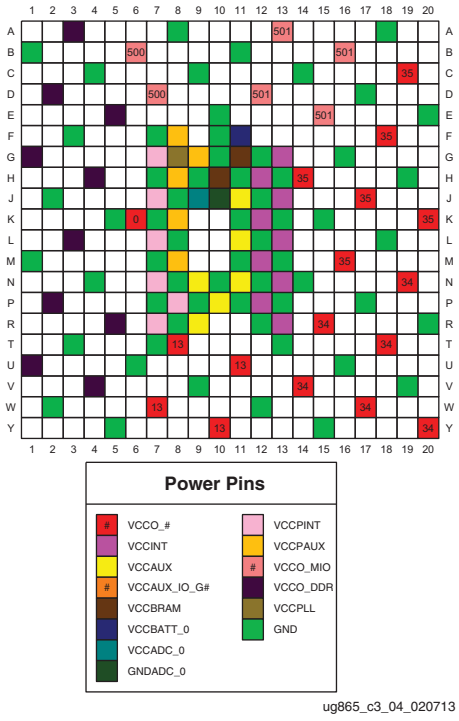


Figure 3-8: **CL400/CLG400 Packages—XC7Z007S, XC7Z010, and XA7Z010 Power and GND Placement**

CL485/CLG485 Packages—XC7Z012S and XC7Z015

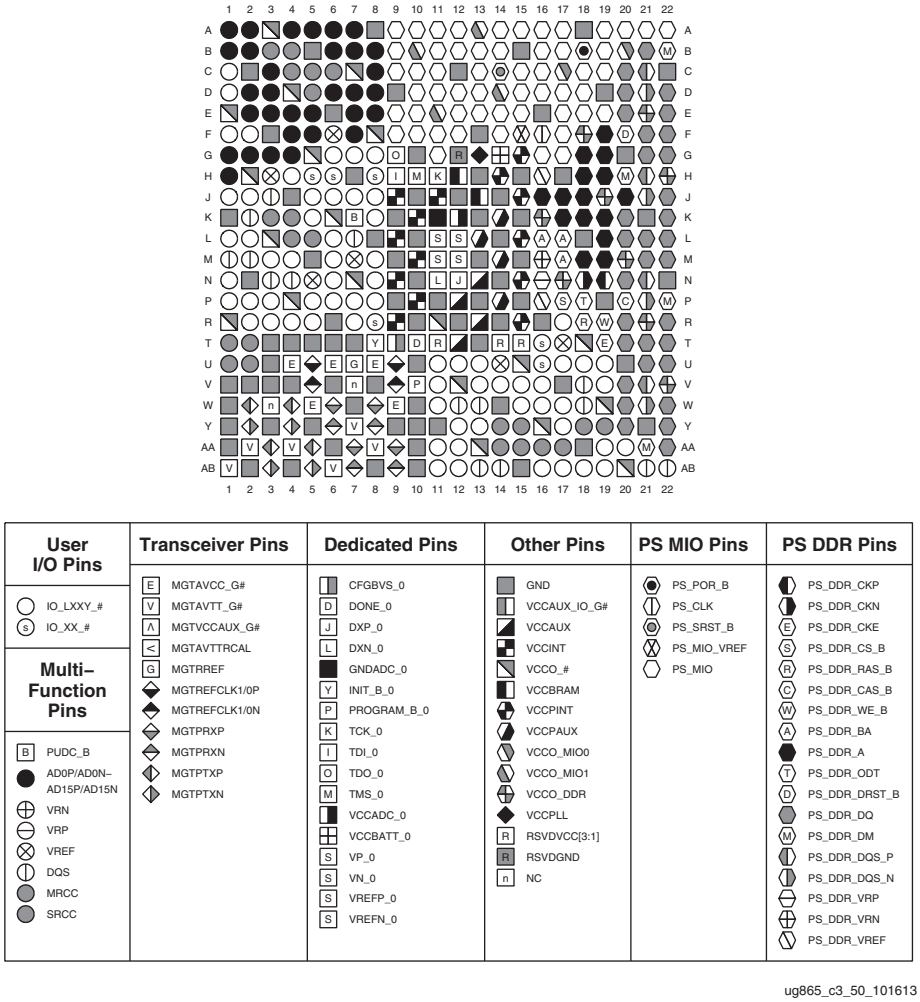


Figure 3-9: **CL485/CLG485 Packages—XC7Z012S and XC7Z015 Pinout Diagram**

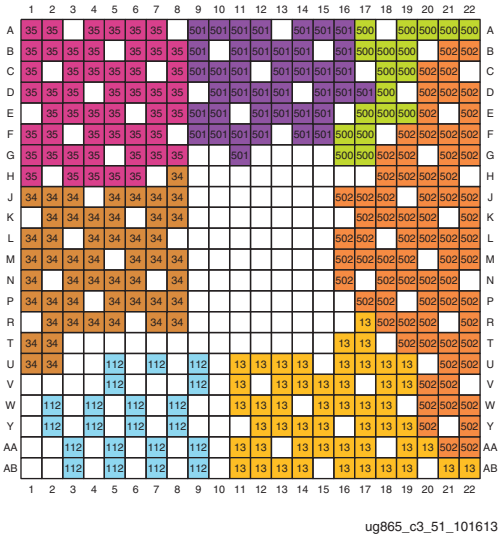


Figure 3-10: **CL485/CLG485 Packages—XC7Z012S and XC7Z015 I/O Banks**

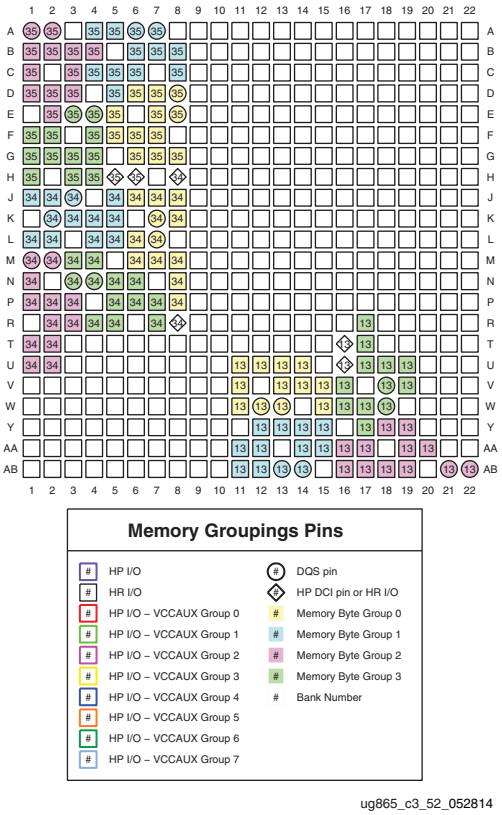


Figure 3-11: **CL485/CLG485 Packages—XC7Z012S and XC7Z015 Memory Groupings**

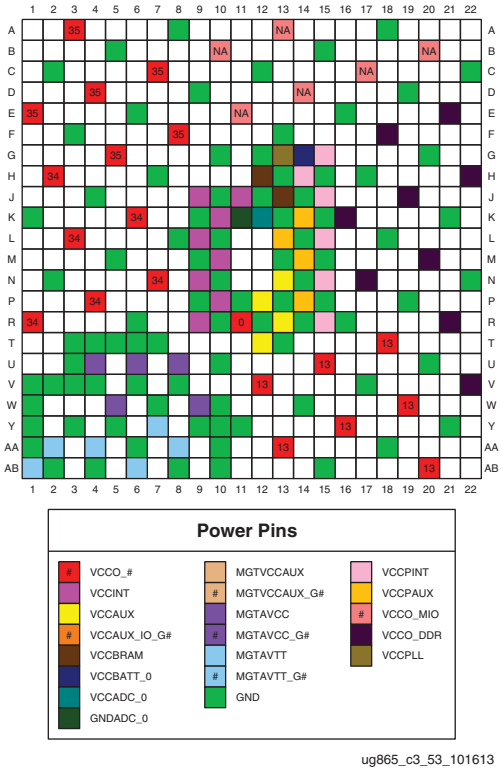


Figure 3-12: **CL485/CLG485 Packages—XC7Z012S and XC7Z015 Power and GND Placement**

CL400/CLG400 Packages—XC7Z014S, XC7Z020, XA7Z020, and XQ7Z020

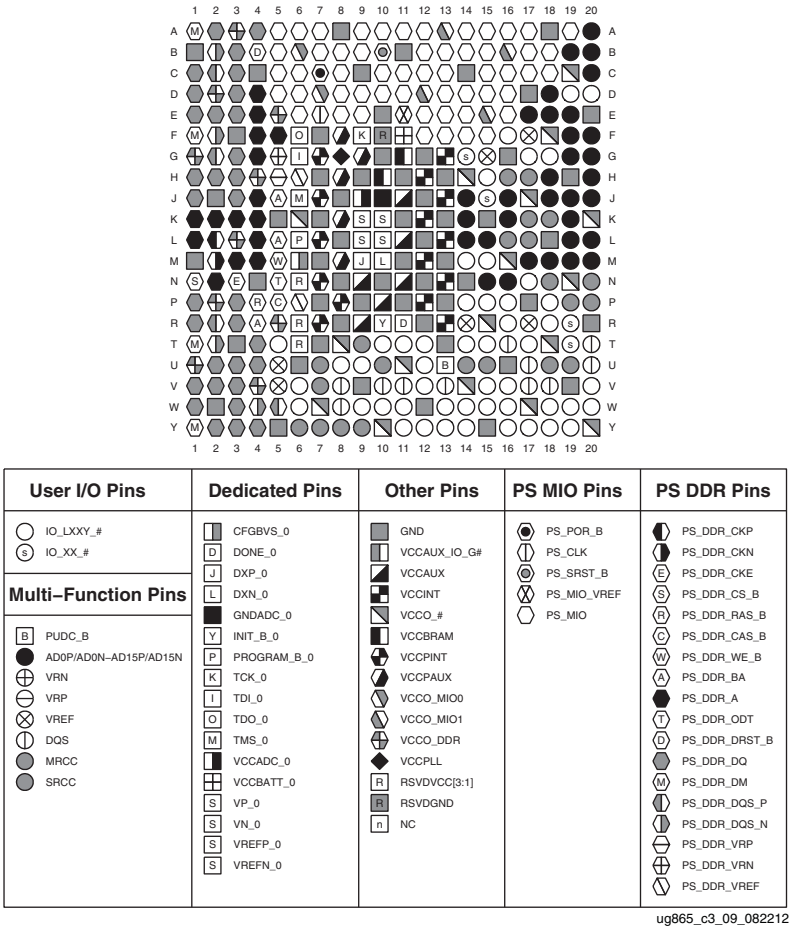


Figure 3-13: **CL400/CLG400 Packages—XC7Z014S, XC7Z020, XA7Z020, and XQ7Z020 Pinout Diagram**

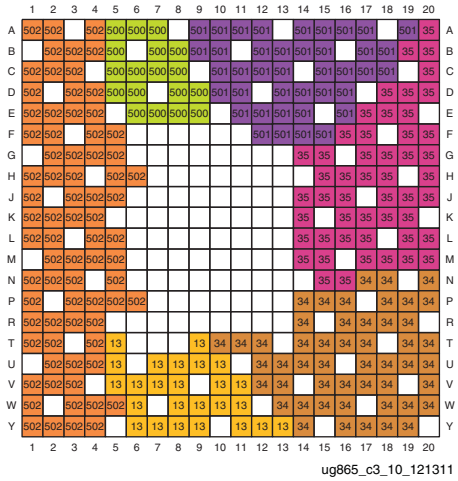


Figure 3-14: **CL400/CLG400 Packages—XC7Z014S, XC7Z020, XA7Z020, and XQ7Z020 I/O Banks**

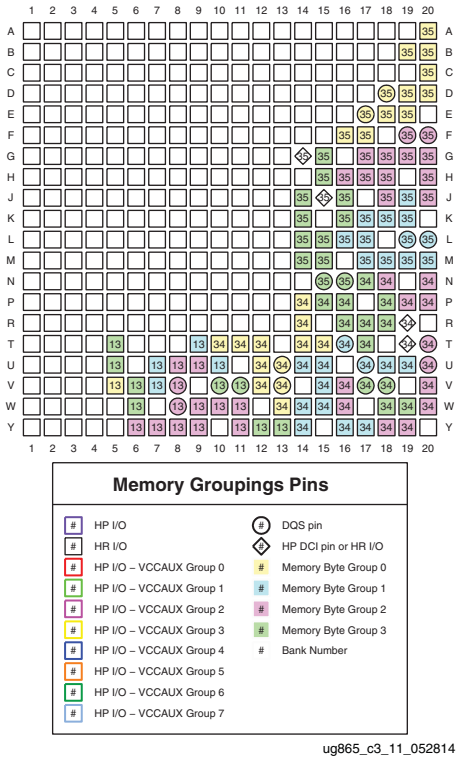


Figure 3-15: **CL400/CLG400 Packages—XC7Z014S, XC7Z020, XA7Z020, and XQ7Z020 Memory Groupings**

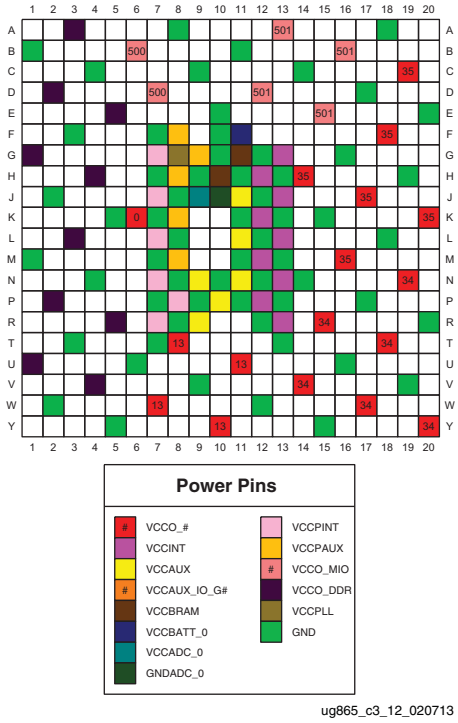


Figure 3-16: **CL400/CLG400 Packages—XC7Z014S, XC7Z020, XA7Z020, and XQ7Z020 Power and GND Placement**

CL484/CLG484 Packages—XC7Z014S, XC7Z020, XA7Z020, and XQ7Z020

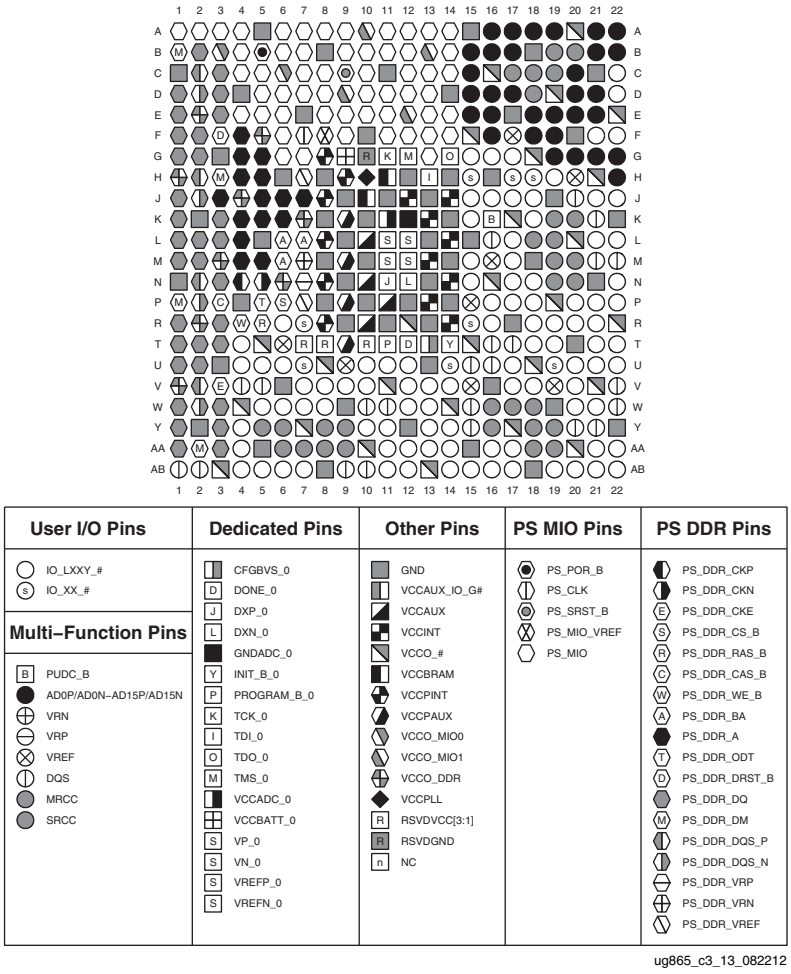


Figure 3-17: **CL484/CLG484 Packages—XC7Z014S, XC7Z020, XA7Z020, and XQ7Z020 Pinout Diagram**

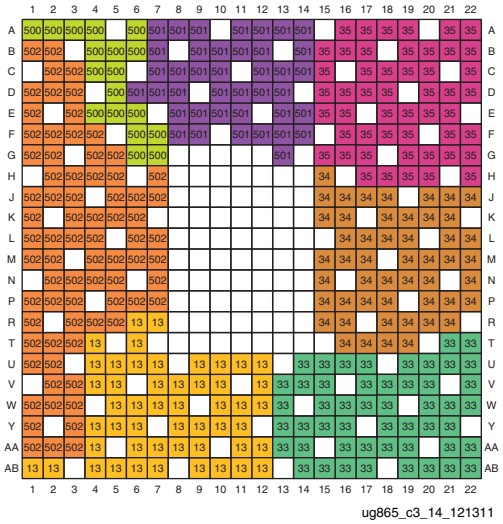


Figure 3-18: **CL484/CLG484 Packages—XC7Z014S, XC7Z020, XA7Z020, and XQ7Z020 I/O Banks**

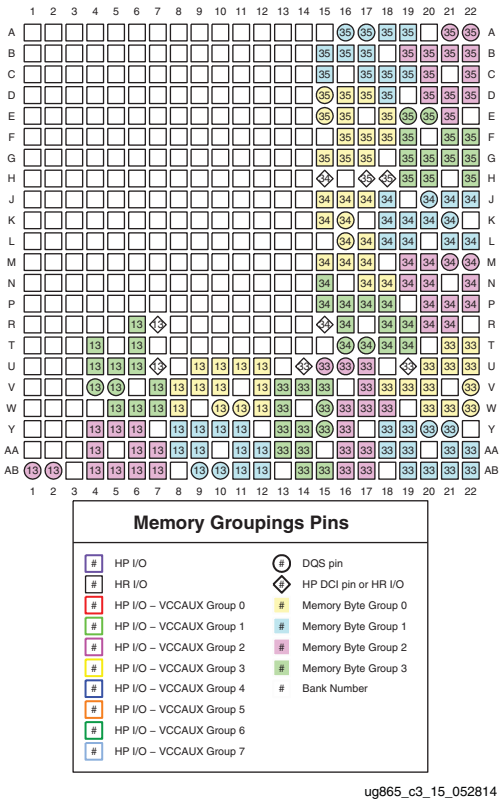


Figure 3-19: **CL484/CLG484 Packages—XC7Z014S, XC7Z020, XA7Z020, and XQ7Z020 Memory Groupings**

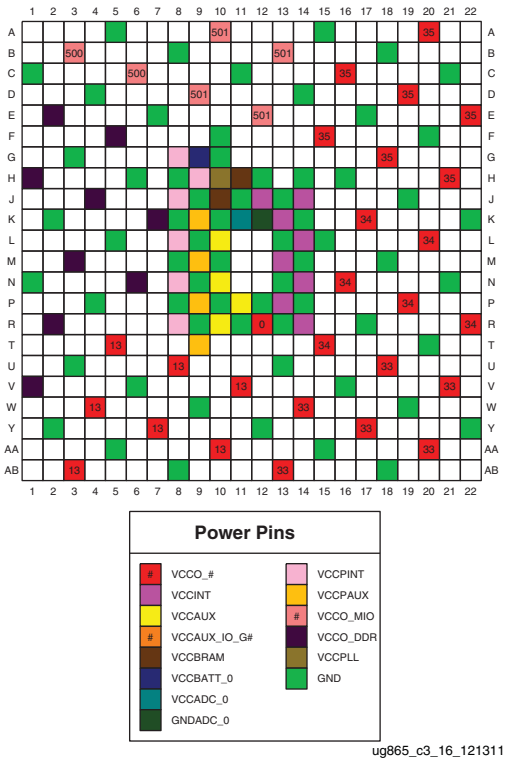


Figure 3-20: **CL484/CLG484 Packages—XC7Z014S, XC7Z020, XA7Z020, and XQ7Z020 Power and GND Placement**

SBG485/SBV485 Packages—XC7Z030

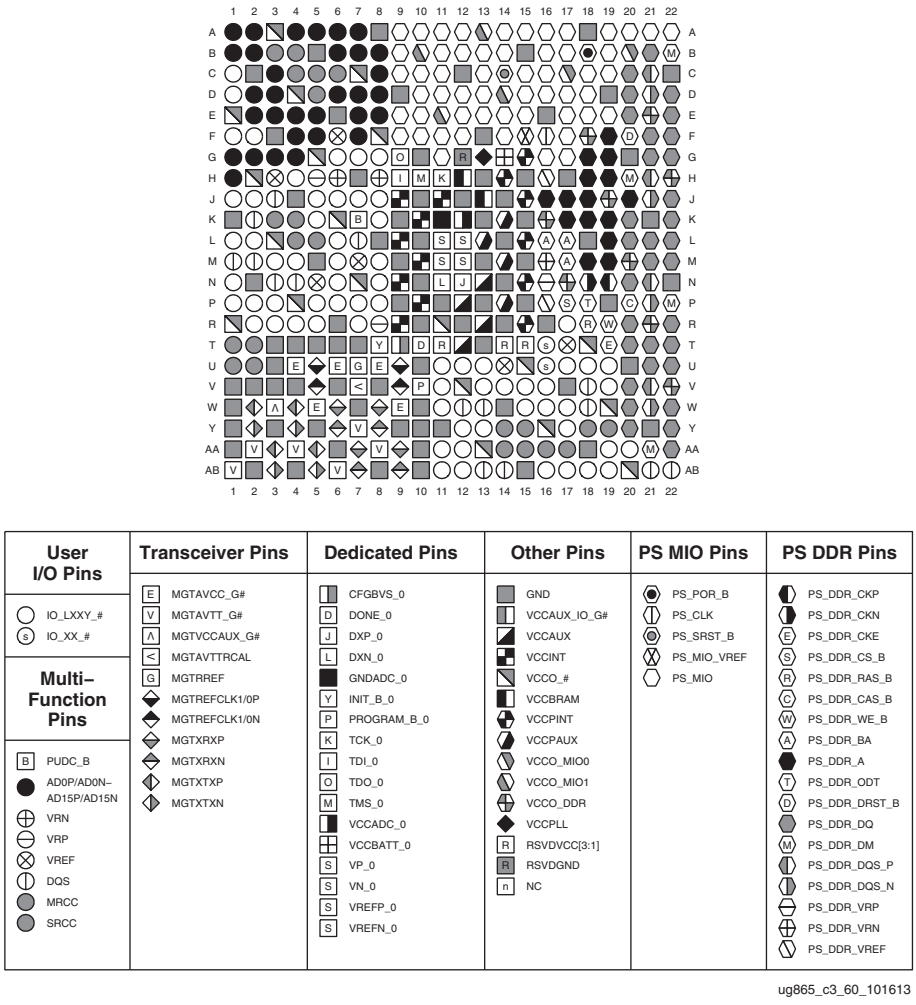


Figure 3-21: **SBG485/SBV485 Packages—XC7Z030 Pinout Diagram**

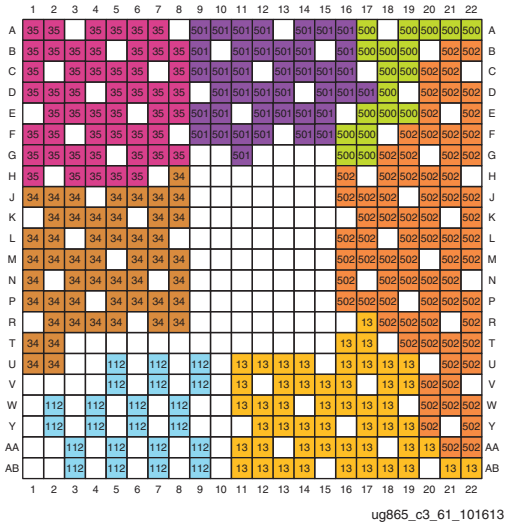


Figure 3-22: **SBG485/SBV485 Packages—XC7Z030 I/O Banks**

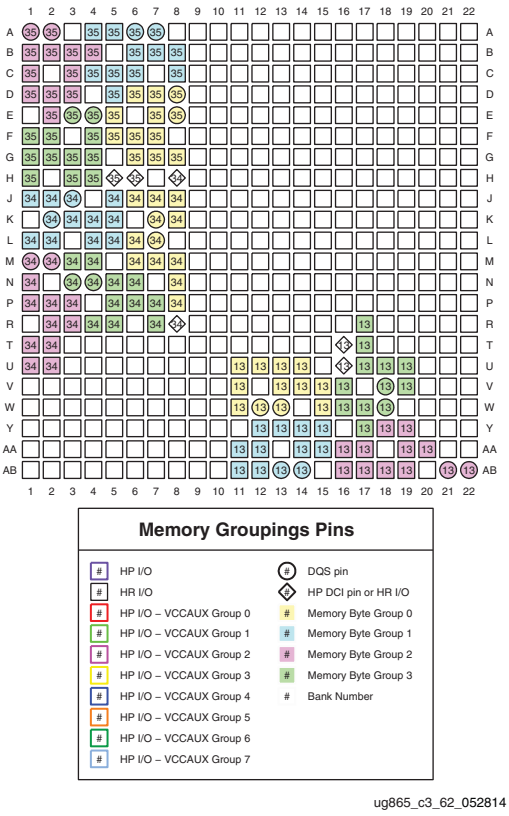


Figure 3-23: **SBG485/SBV485 Packages—XC7Z030 Memory Groupings**

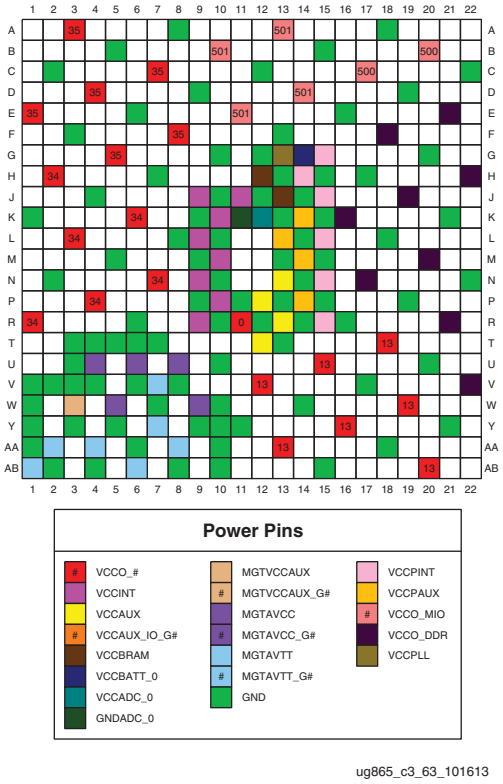


Figure 3-24: **SBG485/SBV485 Packages—XC7Z030 Power and GND Placement**

FB484/FBG484/FBV484/RB484 Packages—XC7Z030, XA7Z030, and XQ7Z030

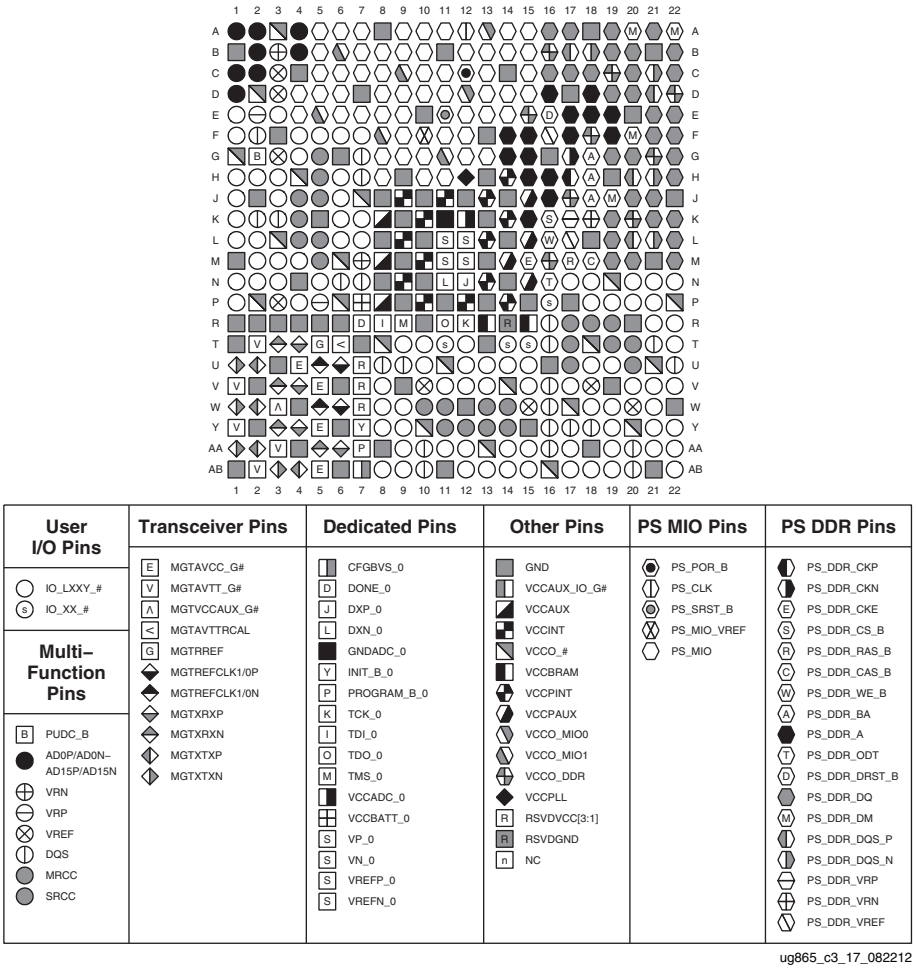


Figure 3-25: **FB484/FBG484/FBV484/RB484 Packages—XC7Z030, XA7Z030, and XQ7Z030 Pinout Diagram**

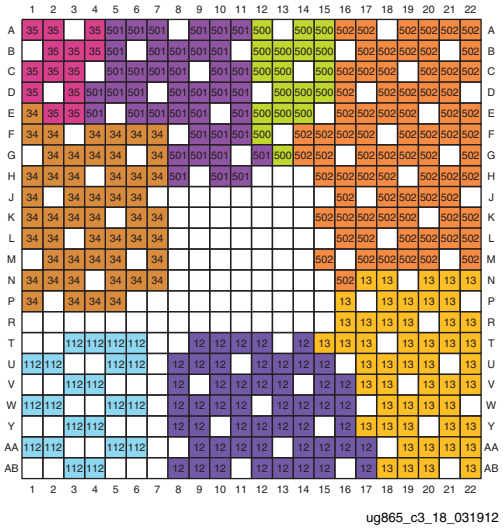


Figure 3-26: **FB484/FBG484/FBV484/RB484 Packages—XC7Z030, XA7Z030, and XQ7Z030 I/O Banks**

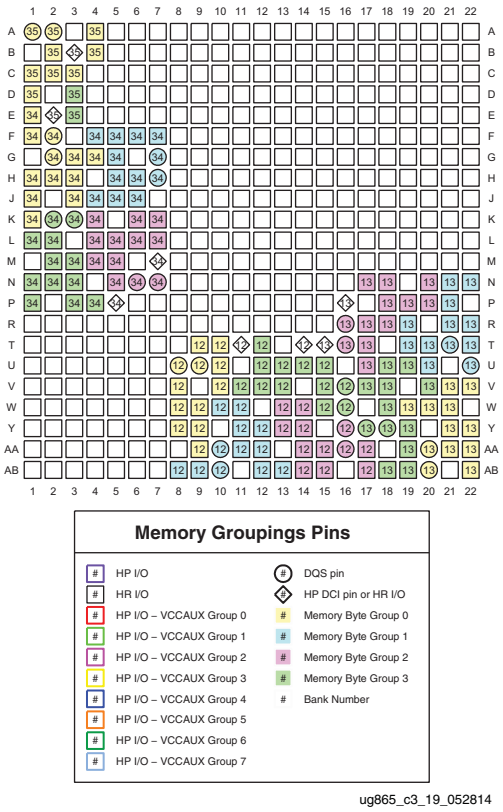


Figure 3-27: **FB484/FBG484/FBV484/RB484 Packages—XC7Z030, XA7Z030, and XQ7Z030 Memory Groupings**

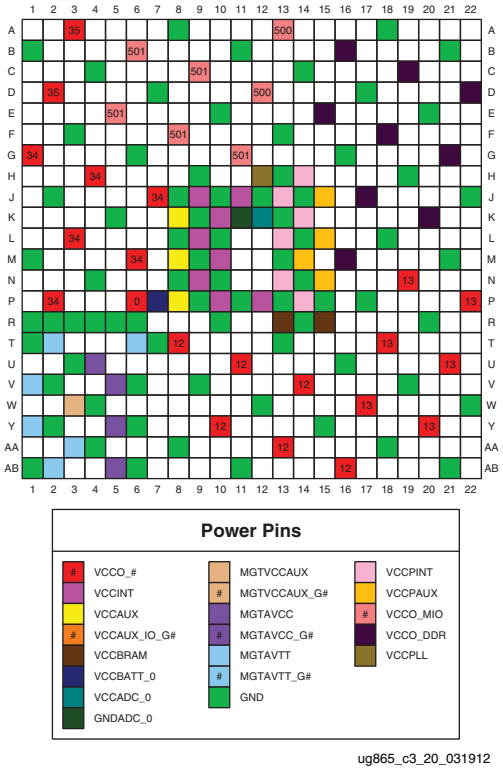


Figure 3-28: **FB484/FBG484/FBV484/RB484 Packages—XC7Z030, XA7Z030, and XQ7Z030 Power and GND Placement**

FB676/FBG676/FBV676 Packages—XC7Z030

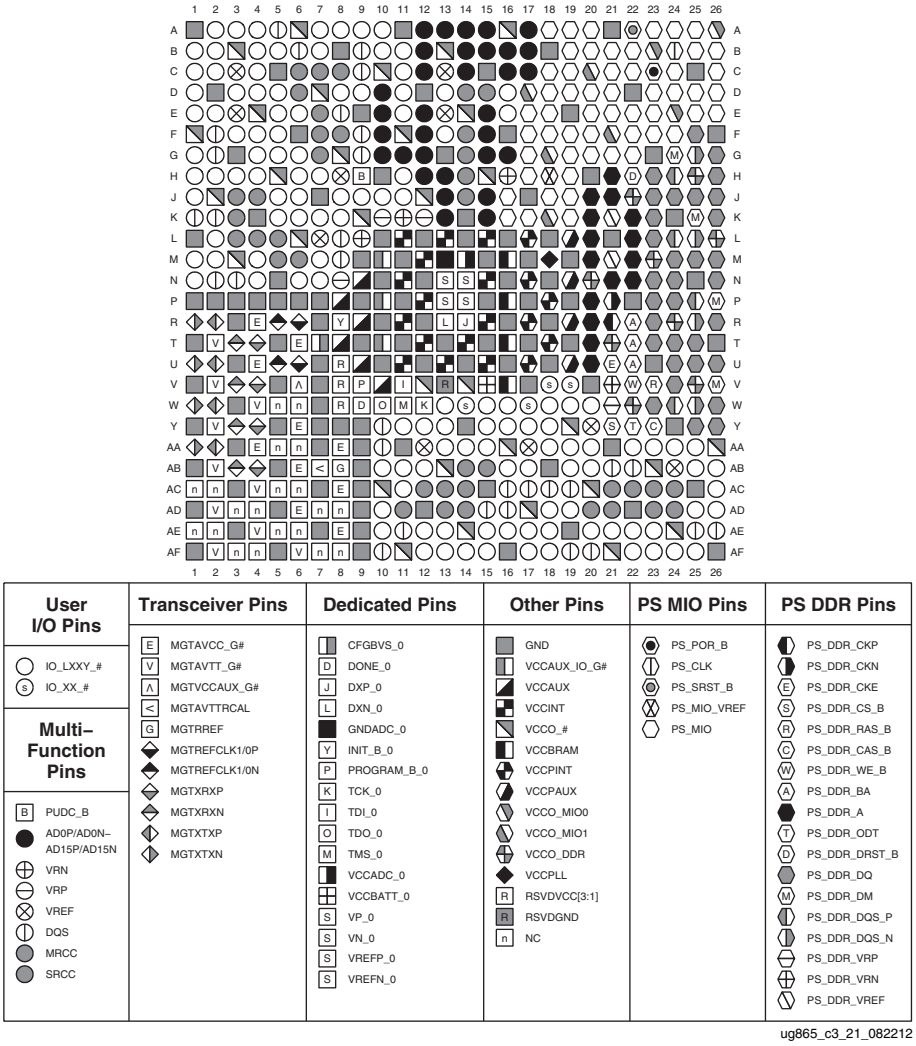


Figure 3-29: **FB676/FBG676/FBV676 Packages—XC7Z030 Pinout Diagram**

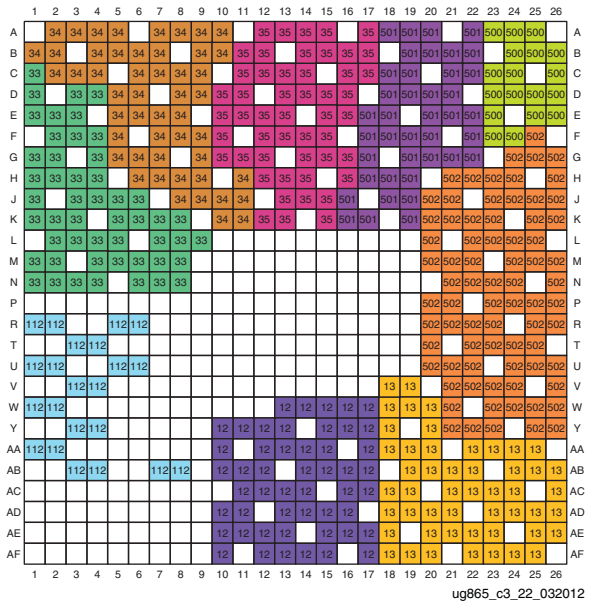


Figure 3-30: **FB676/FBG676/FBV676 Packages—XC7Z030 I/O Banks**

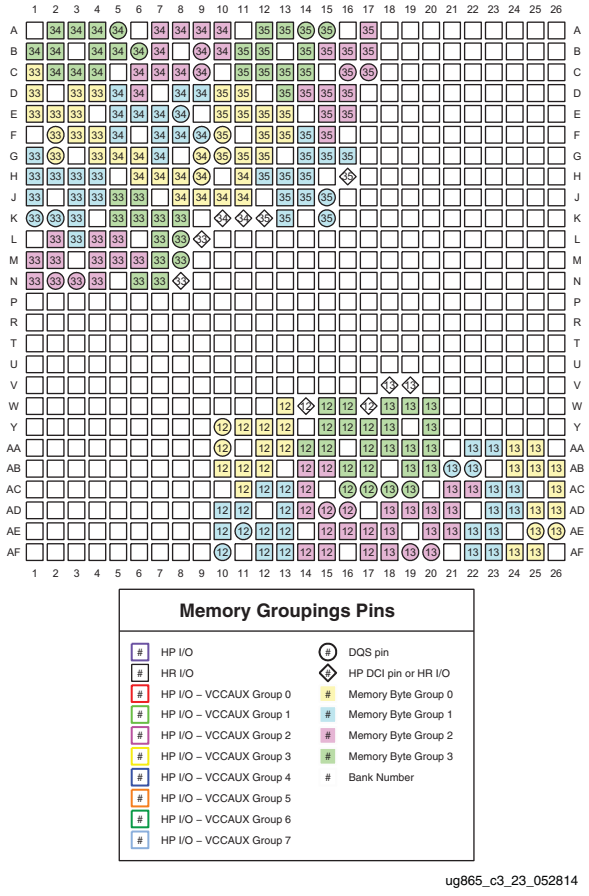


Figure 3-31: **FB676/FBG676/FBV676 Packages—XC7Z030 Memory Groupings**

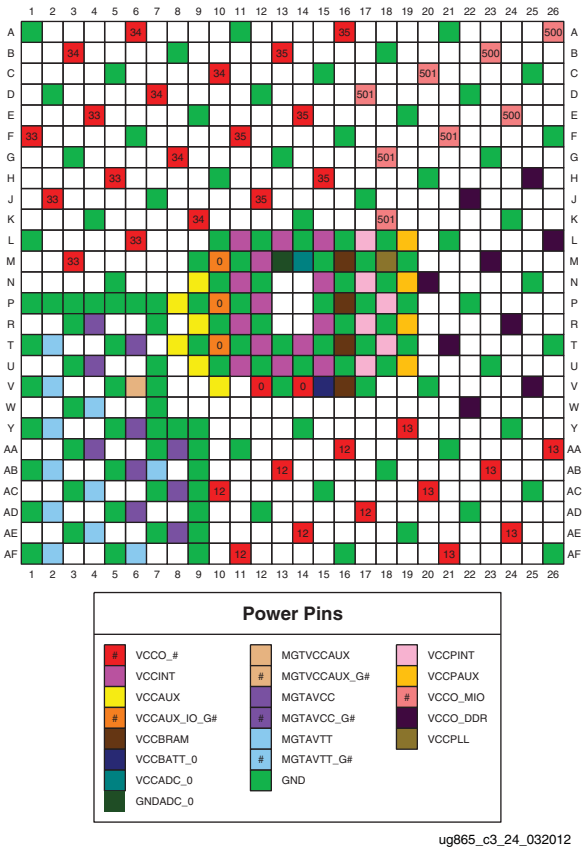


Figure 3-32: **FB676/FBG676/FBV676 Packages—XC7Z030 Power and GND Placement**

FF676/FFG676/FFV676/RF676 Packages—XC7Z030 and XQ7Z030

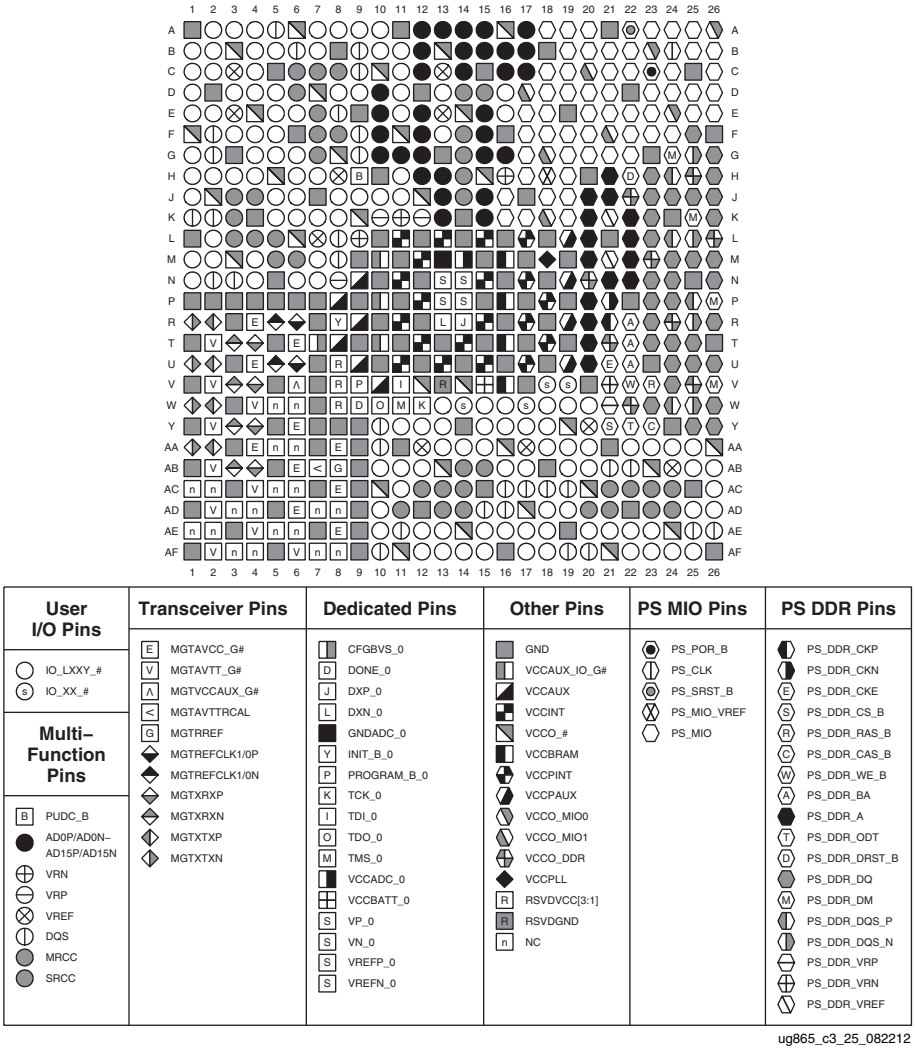


Figure 3-33: **FF676/FFG676/FFV676/RF676 Packages—XC7Z030 and XQ7Z030 Pinout Diagram**

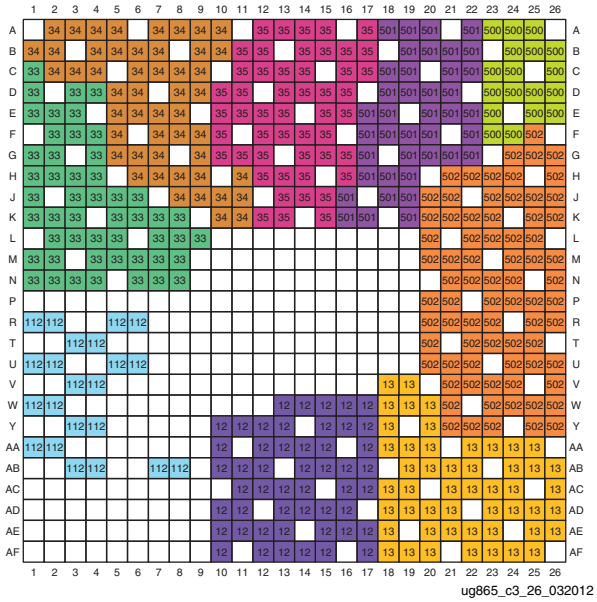


Figure 3-34: **FF676/FFG676/FFV676/RF676 Packages—XC7Z030 and XQ7Z030 I/O Banks**

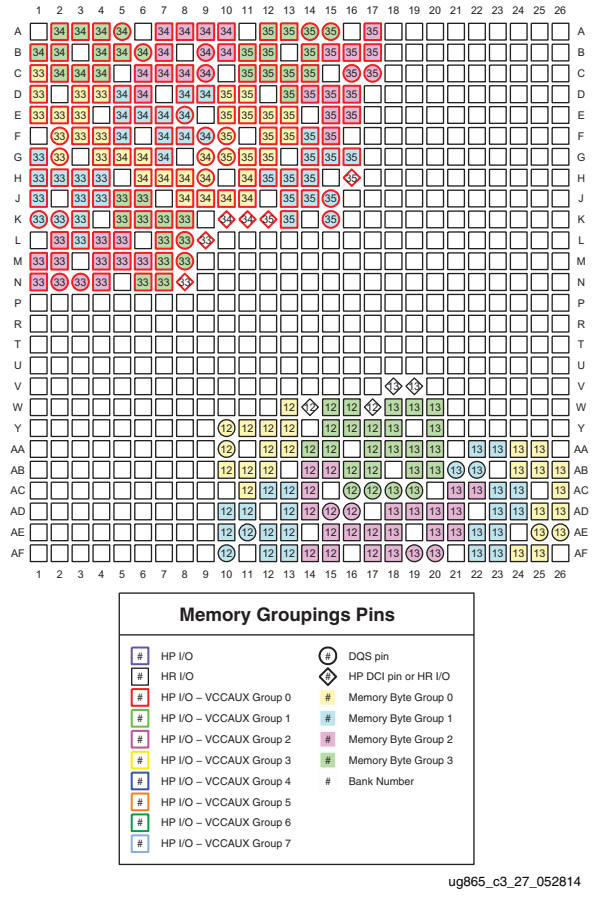


Figure 3-35: **FF676/FFG676/FFV676/RF676 Packages—XC7Z030 and XQ7Z030 Memory Groupings**

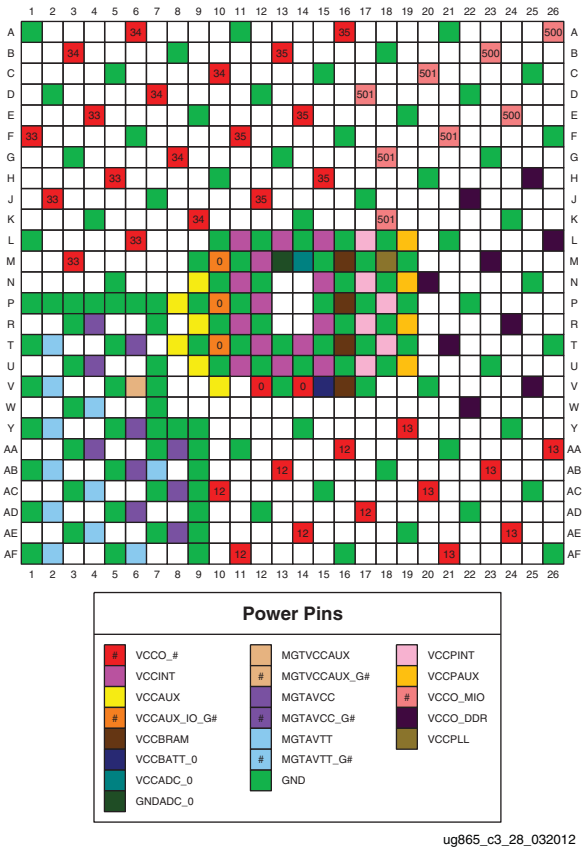


Figure 3-36: **FF676/FFG676/FFV676/RF676 Packages—XC7Z030 and XQ7Z030 Power and GND Placement**

FB676/FBG676/FBV676 Packages—XC7Z035 and XC7Z045

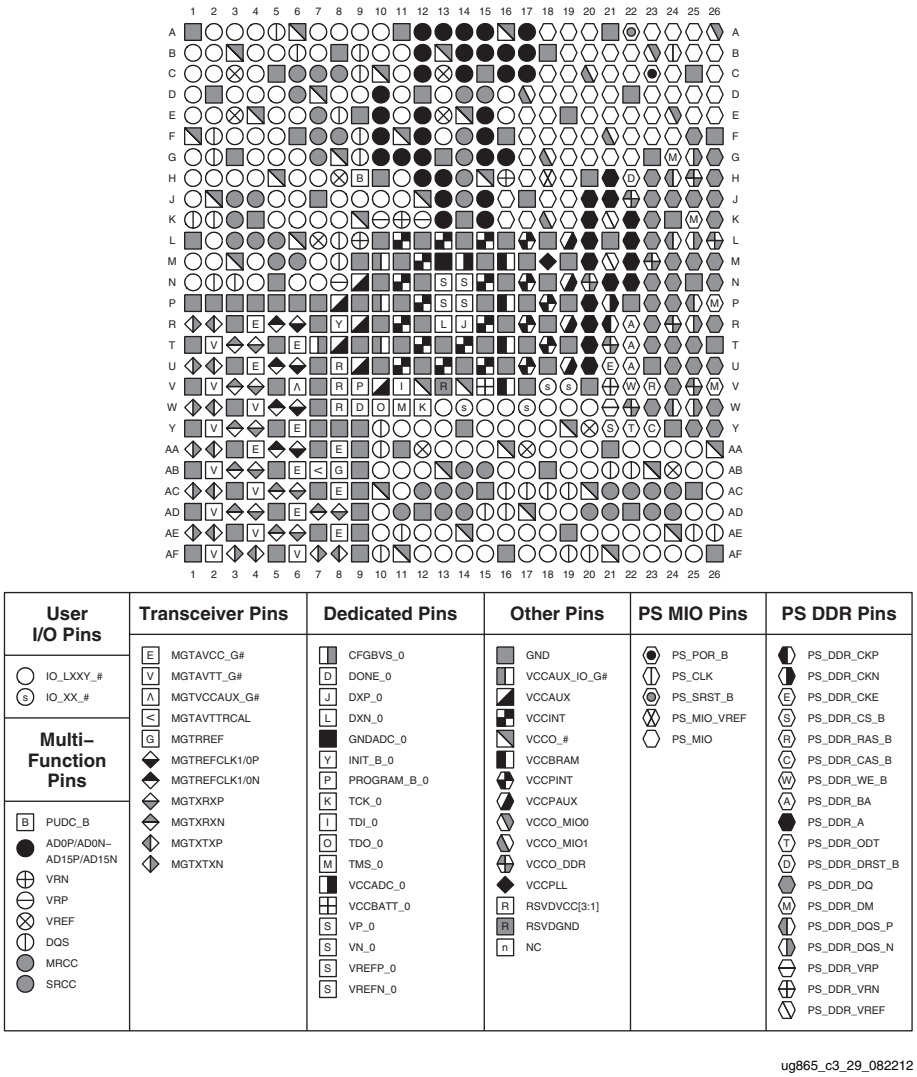


Figure 3-37: **FB676/FBG676/FBV676 Packages—XC7Z035 and XC7Z045 Pinout Diagram**

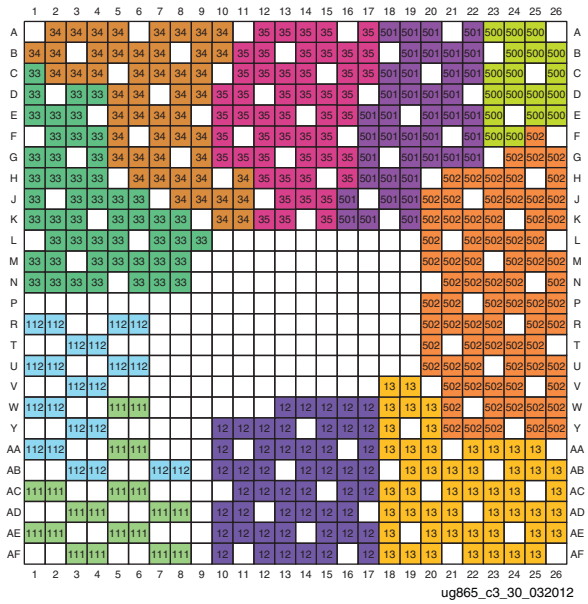


Figure 3-38: **FB676/FBG676/FBV676 Packages—XC7Z035 and XC7Z045 I/O Banks**

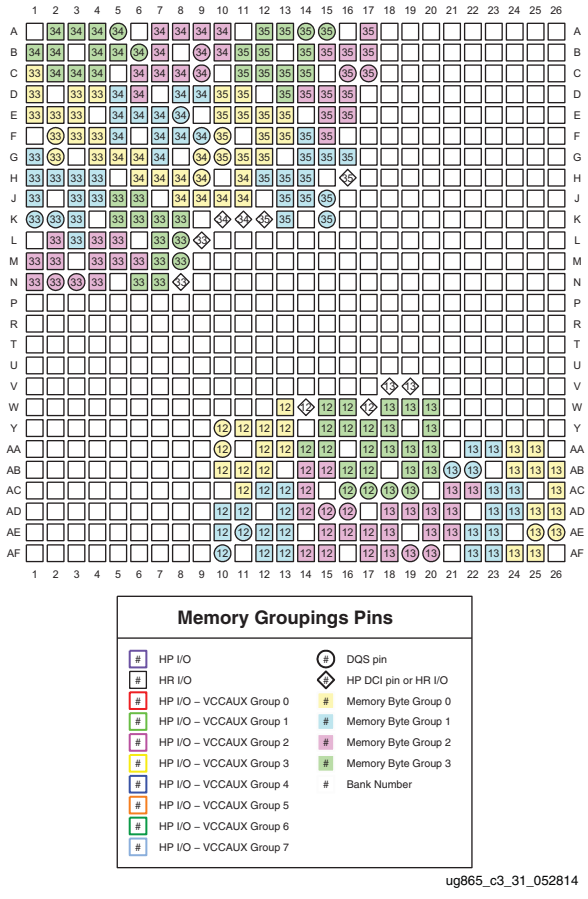


Figure 3-39: **FB676/FBG676/FBV676 Packages—XC7Z035 and XC7Z045 Memory Groupings**

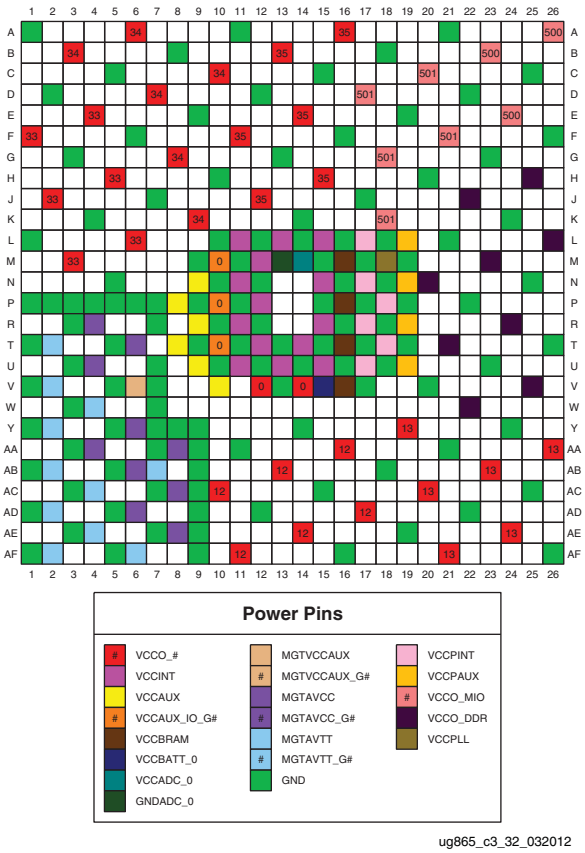


Figure 3-40: **FB676/FBG676/FBV676 Packages—XC7Z035 and XC7Z045 Power and GND Placement**

FF676/FFG676/FFV676/RF676/RFG676 Packages—XC7Z035, XC7Z045, and XQ7Z045

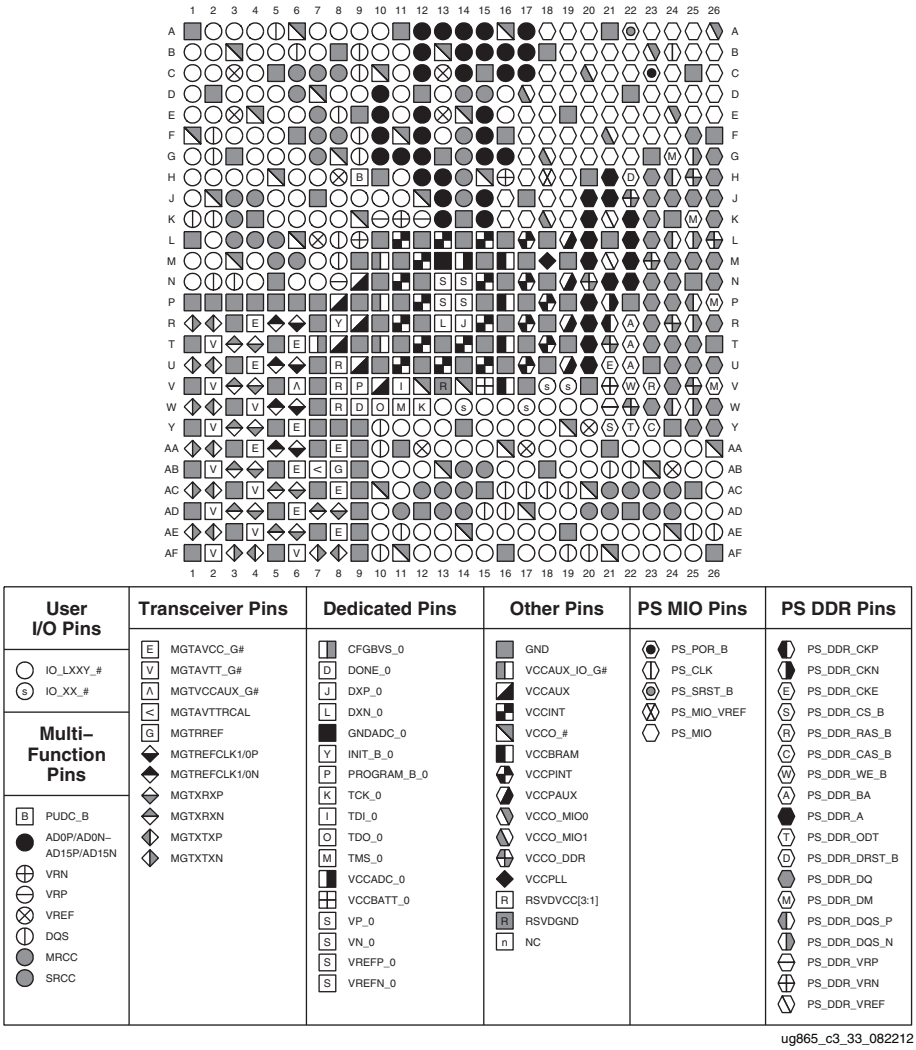


Figure 3-41: **FF676/FFG676/FFV676/RF676/RFG676 Packages—XC7Z035, XC7Z045, and XQ7Z045 Pinout Diagram**

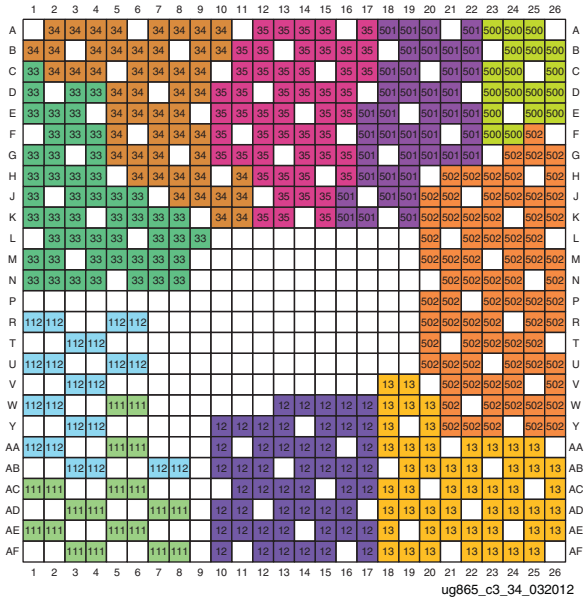


Figure 3-42: **FF676/FFG676/FFV676/RF676/RFG676 Packages—XC7Z035, XC7Z045, and XQ7Z045 I/O Banks**

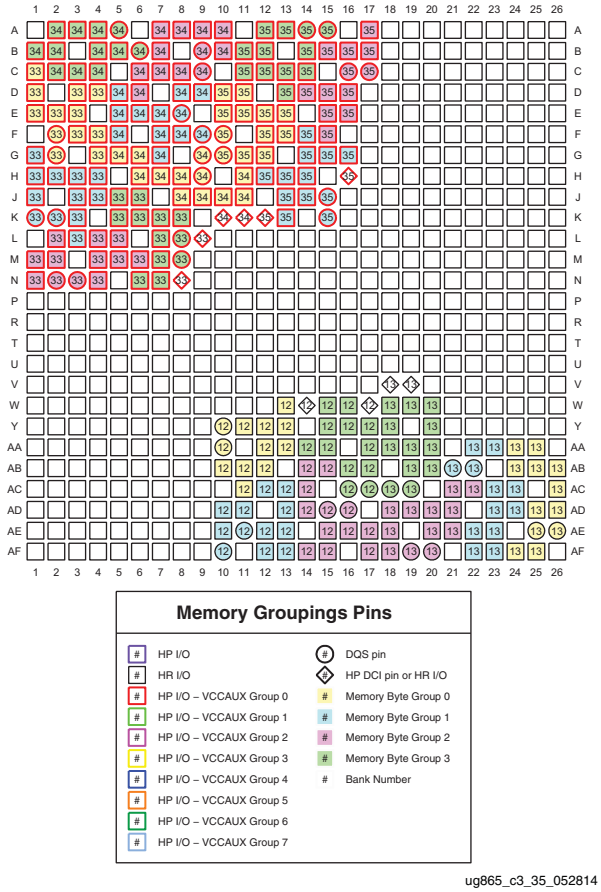


Figure 3-43: **FF676/FFG676/FFV676/RF676/RFG676 Packages—XC7Z035, XC7Z045, and XQ7Z045 Memory Groupings**

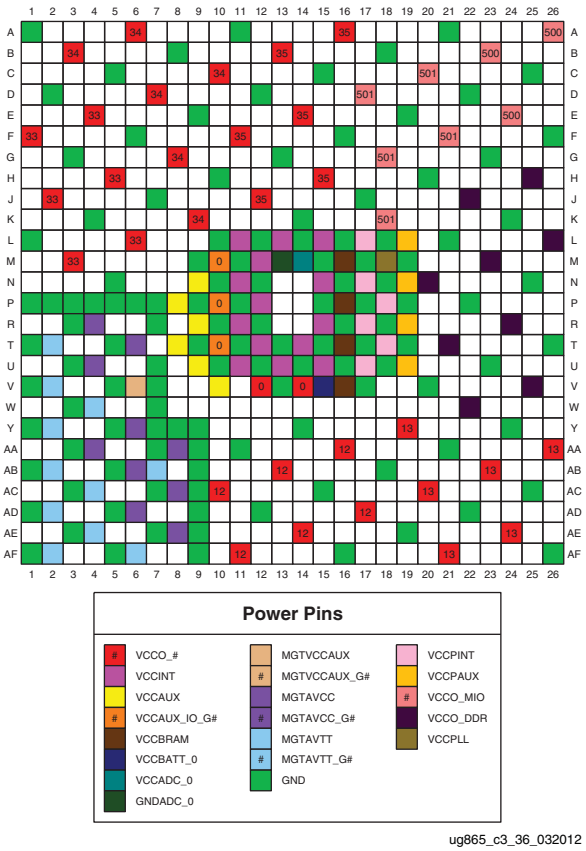


Figure 3-44: **FF676/FFG676/FFV676/RF676/RFG676 Packages—XC7Z035, XC7Z045, and XQ7Z045 Power and GND Placement**

FF900/FFG900/FFV900/RF900 Packages—XC7Z035, XC7Z045, and XQ7Z045

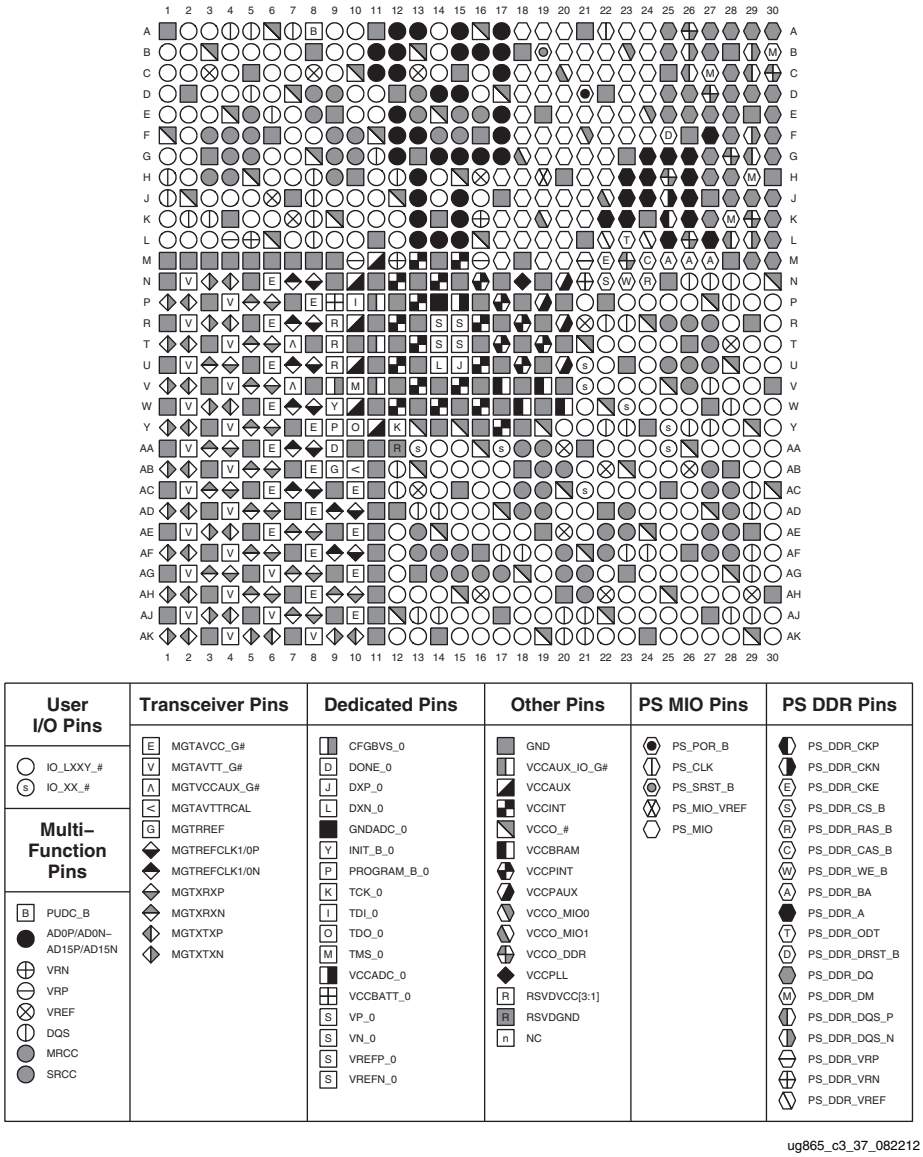


Figure 3-45: **FF900/FFG900/FFV900/RF900 Packages—XC7Z035, XC7Z045, and XQ7Z045 Pinout Diagram**

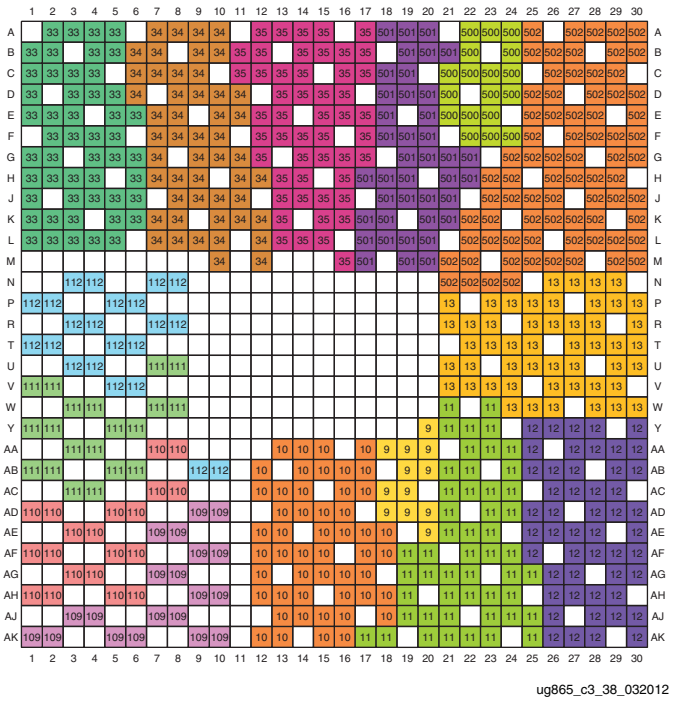


Figure 3-46: **FF900/FFG900/FFV900/RF900 Packages—XC7Z035, XC7Z045, and XQ7Z045 I/O Banks**

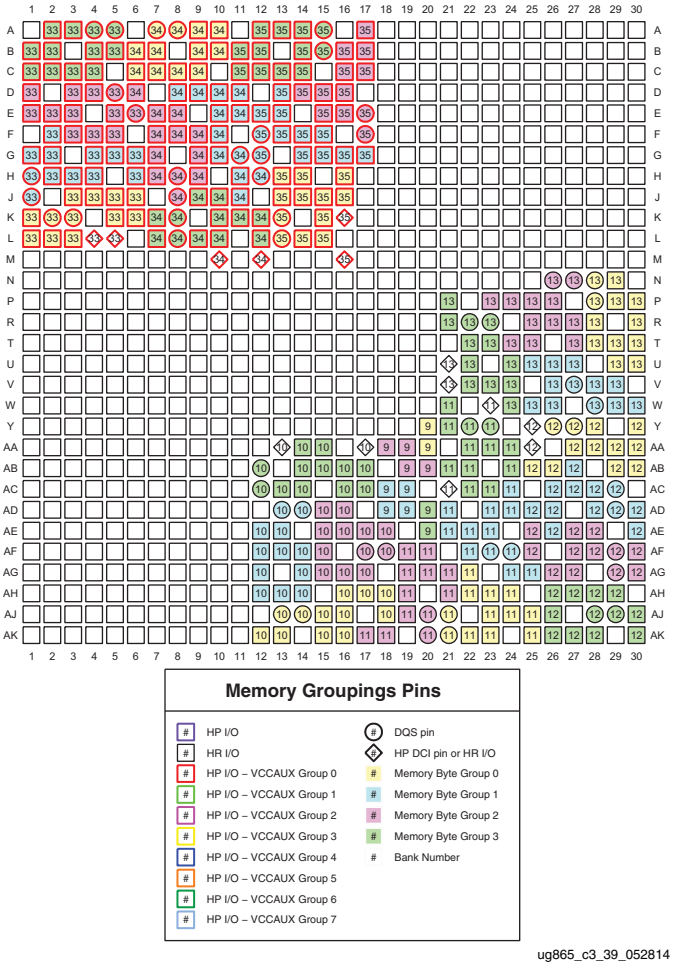


Figure 3-47: **FF900/FFG900/FFV900/RF900 Packages—XC7Z035, XC7Z045, and XQ7Z045 Memory Groupings**

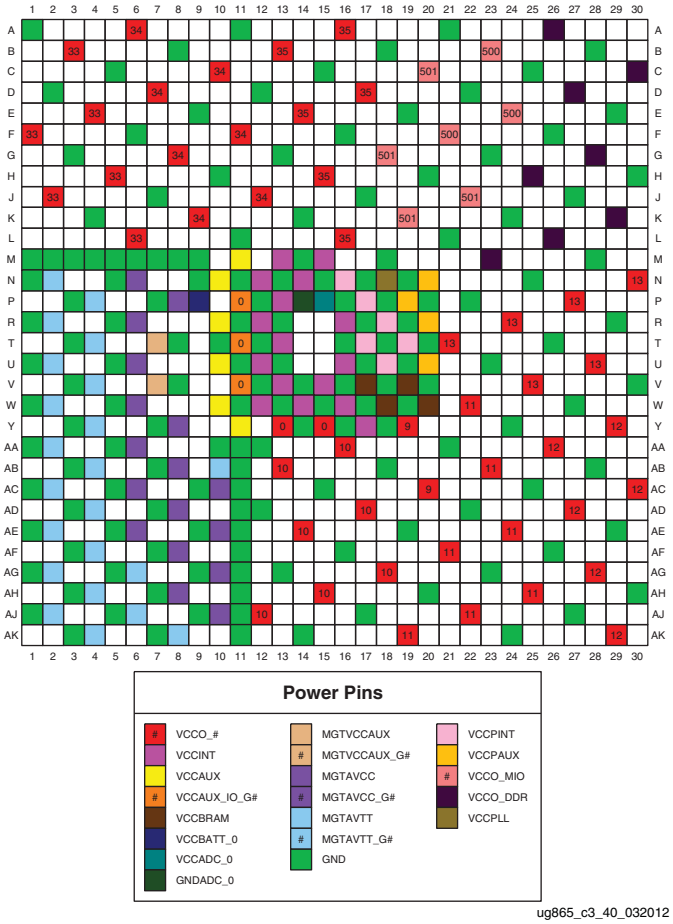


Figure 3-48: **FF900/FFG900/FFV900/RF900 Packages—XC7Z035, XC7Z045, and XQ7Z045 Power and GND Placement**

FF900/FFG900/FFV900/RF900 Packages—XC7Z100 and XQ7Z100

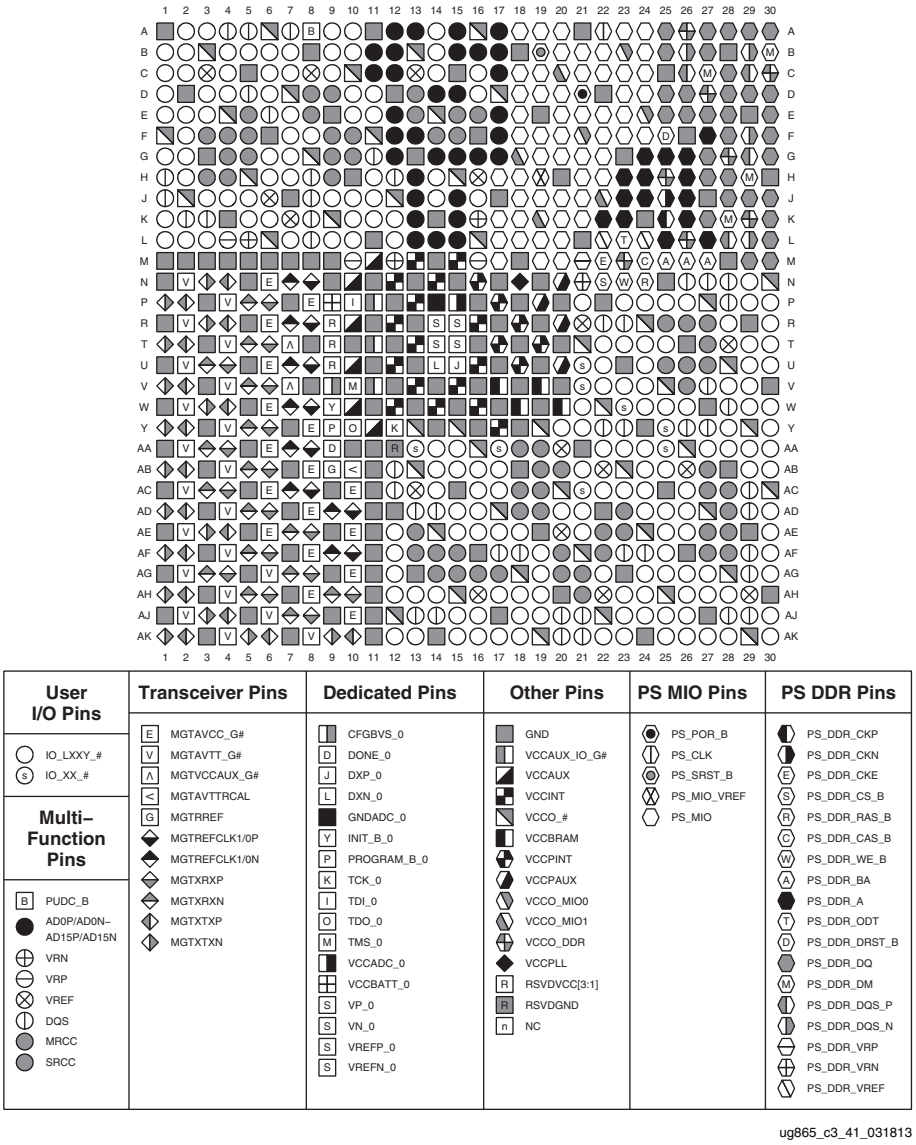


Figure 3-49: **FF900/FFG900/FFV900/RF900 Packages—XC7Z100 and XQ7Z100 Pinout Diagram**

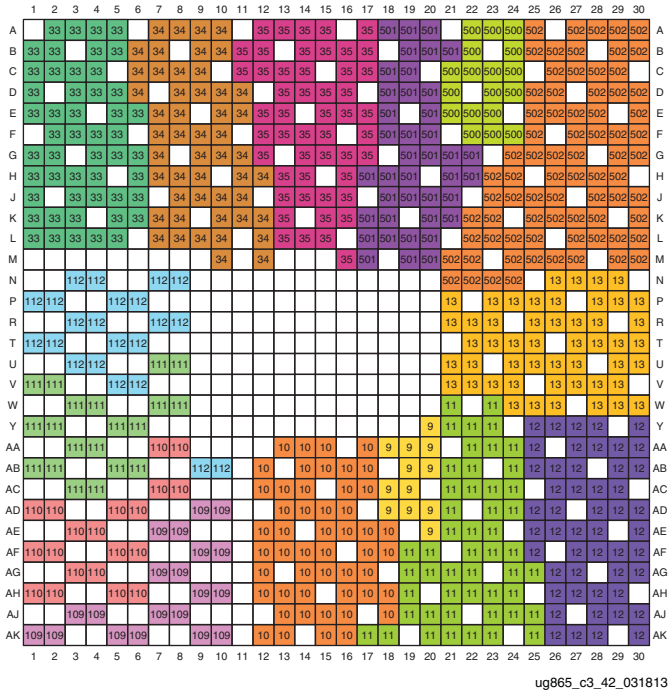


Figure 3-50: **FF900/FFG900/FFV900/RF900 Packages—XC7Z100 and XQ7Z100 I/O Banks**

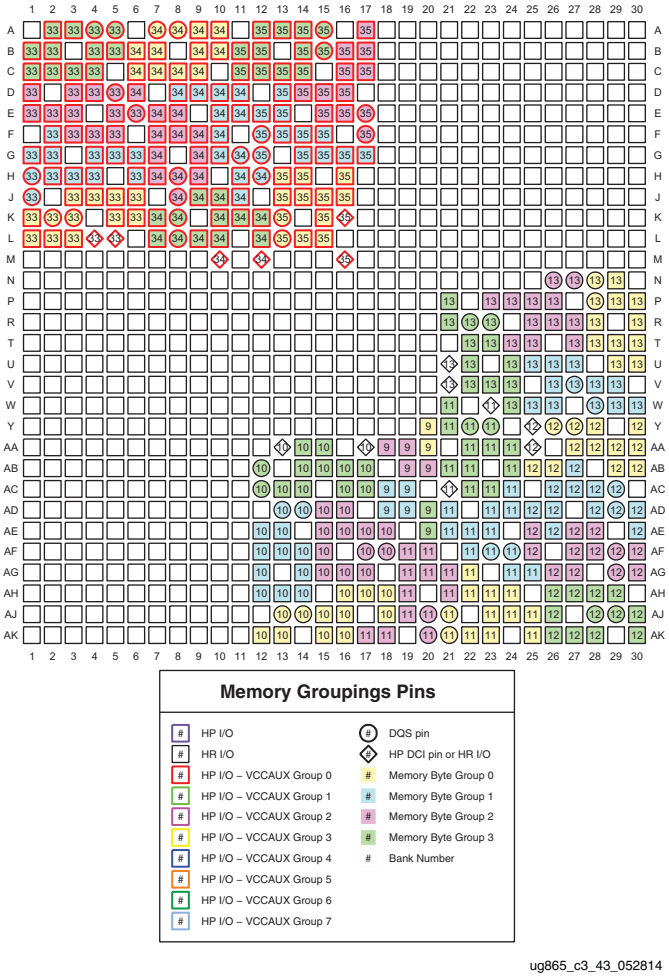


Figure 3-51: **FF900/FFG900/FFV900/RF900 Packages—XC7Z100 and XQ7Z100 Memory Groupings**

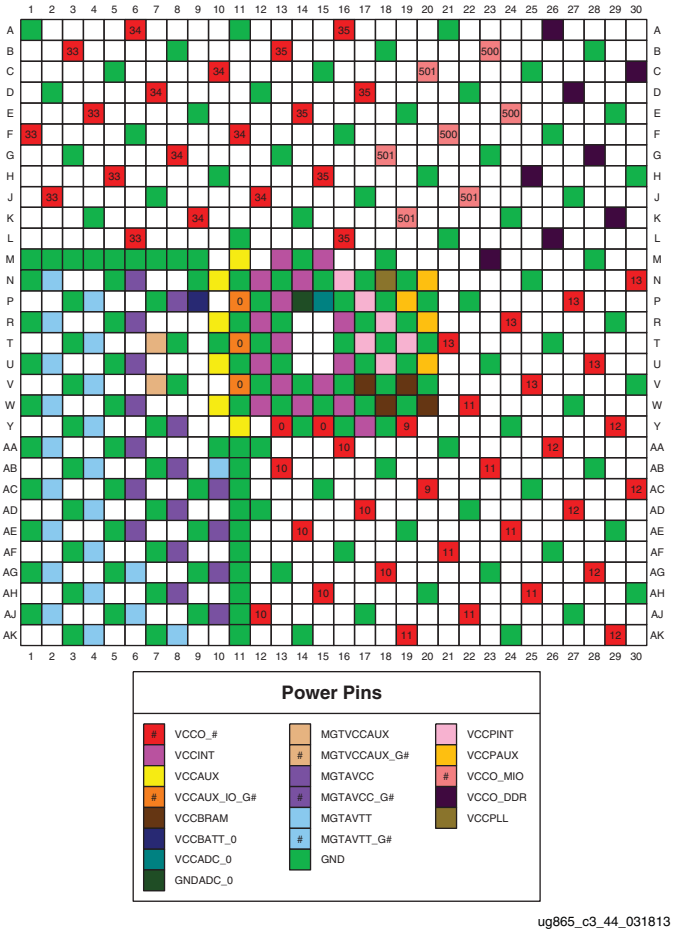
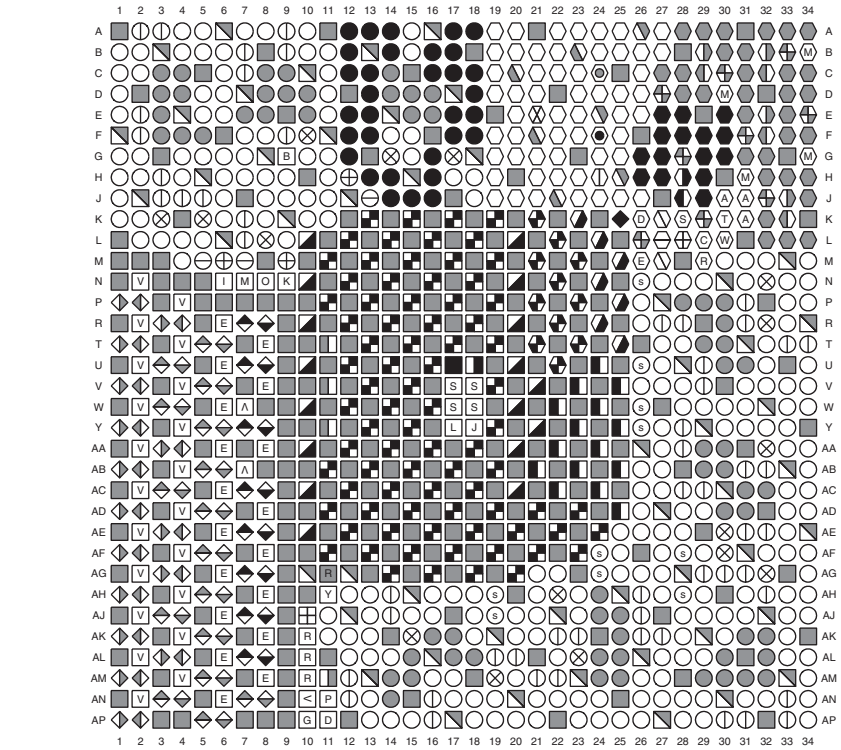


Figure 3-52: **FF900/FFG900/FFV900/RF900 Packages—XC7Z100 and XQ7Z100 Power and GND Placement**

FF1156/FFG1156/FFV1156/RF1156 Packages—XC7Z100 and XQ7Z100



User I/O Pins	Transceiver Pins	Dedicated Pins	Other Pins	PS MIO Pins	PS DDR Pins
IO_LXXY_# IO_XX_#	MGTAVCC_G# MGTAVTT_G# MGTVCCAUX_G# MGTAVTTRCAL MGTRREF MGTREFCLK1/0P MGTREFCLK1/0N MGTXRXP MGTXRXN MGTXTXP MGTXTXN	CFGBVS_0 DONE_0 DXP_0 DXN_0 GNDADC_0 INIT_B_0 PROGRAM_B_0 TCK_0 TDI_0 TDO_0 TMS_0 VCCADC_0 VCCBATT_0 VP_0 VN_0 VREFP_0 VREFN_0	GND VCCAUX_IO_G# VCCAUX VCCINT VCCO_# VCCBRAM VCCPINT VCCPAUX VCCO_MIO0 VCCO_MIO1 VCCO_DDR VCCPLL RSVDVCC[3:1] RSVDGND NC	PS_POR_B PS_CLK PS_SRST_B PS_MIO_VREF PS_MIO	PS_DDR_CKP PS_DDR_CKN PS_DDR_CKE PS_DDR_CS_B PS_DDR_RAS_B PS_DDR_CAS_B PS_DDR_WE_B PS_DDR_BA PS_DDR_A PS_DDR_ODT PS_DDR_DRST_B PS_DDR_DQ PS_DDR_DM PS_DDR_DQS_P PS_DDR_DQS_N PS_DDR_VRP PS_DDR_VRN PS_DDR_VREF
Multi–Function Pins					
PUDC_B AD0P/AD0N–AD15P/AD15N VRN VRP VREF DQS MRCC SRCC					

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Figure 3-53: **FF1156/FFG1156/FFV1156/RF1156 Packages—XC7Z100 and XQ7Z100 Pinout Diagram**

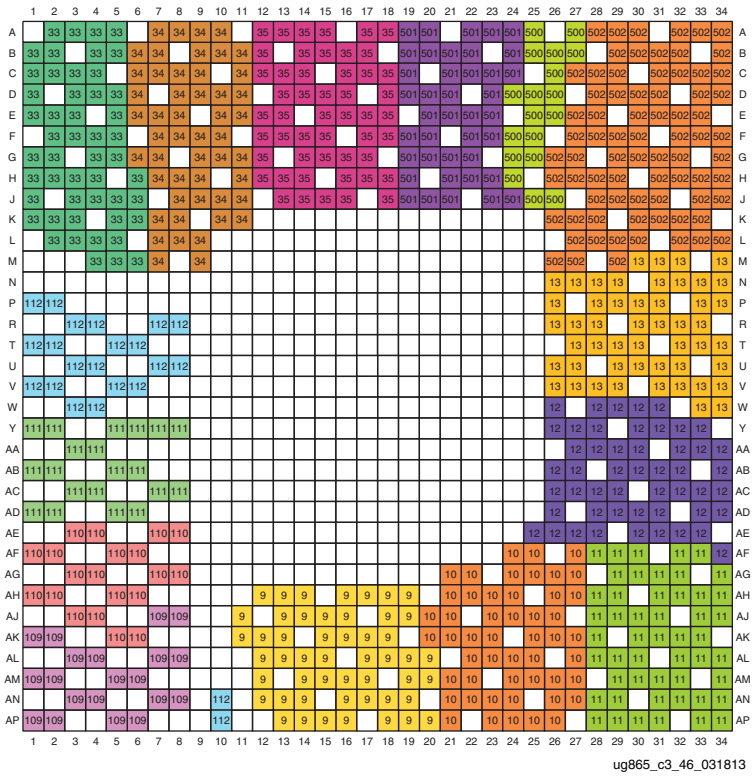


Figure 3-54: **FF1156/FFG1156/FFV1156/RF1156 Packages—XC7Z100 and XQ7Z100 I/O Banks**

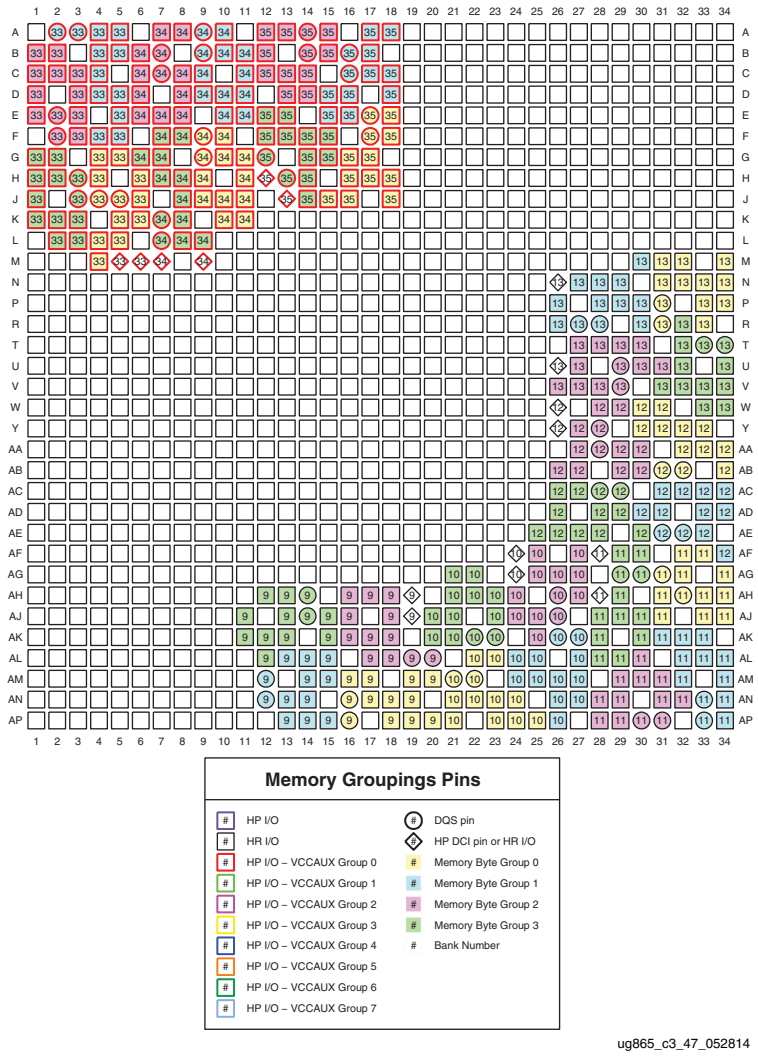


Figure 3-55: **FF1156/FFG1156/FFV1156/RF1156 Packages—XC7Z100 and XQ7Z100 Memory Groupings**

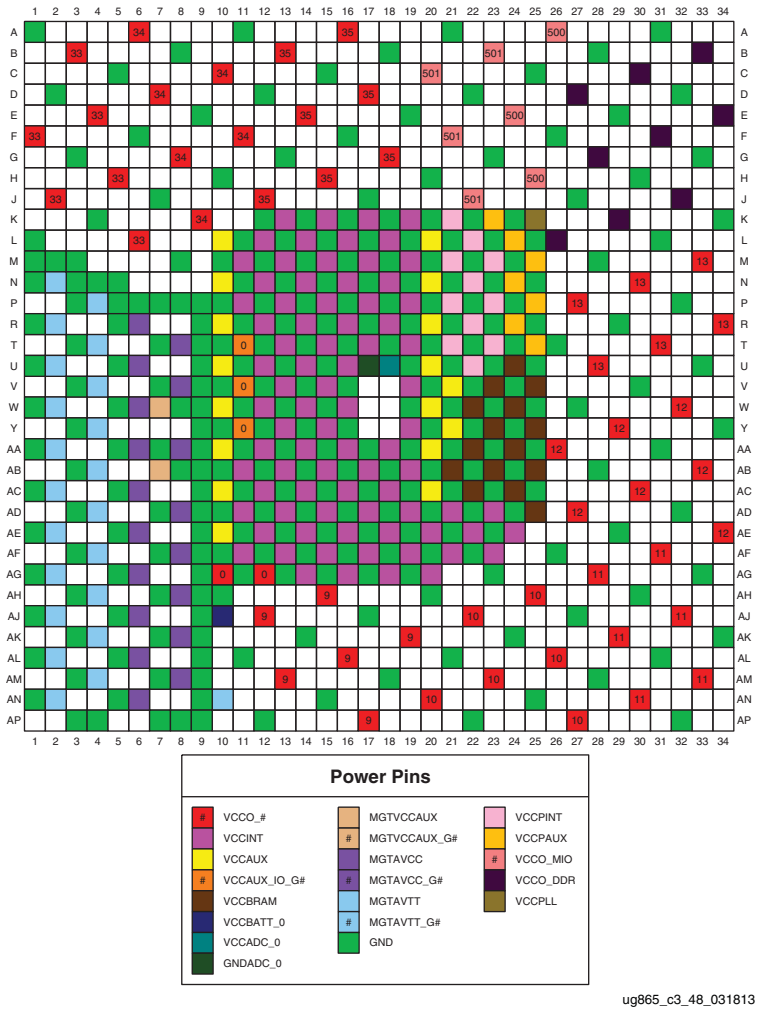


Figure 3-56: **FF1156/FFG1156/FFV1156/RF1156 Packages—XC7Z100 and XQ7Z100 Power and GND Placement**

Mechanical Drawings

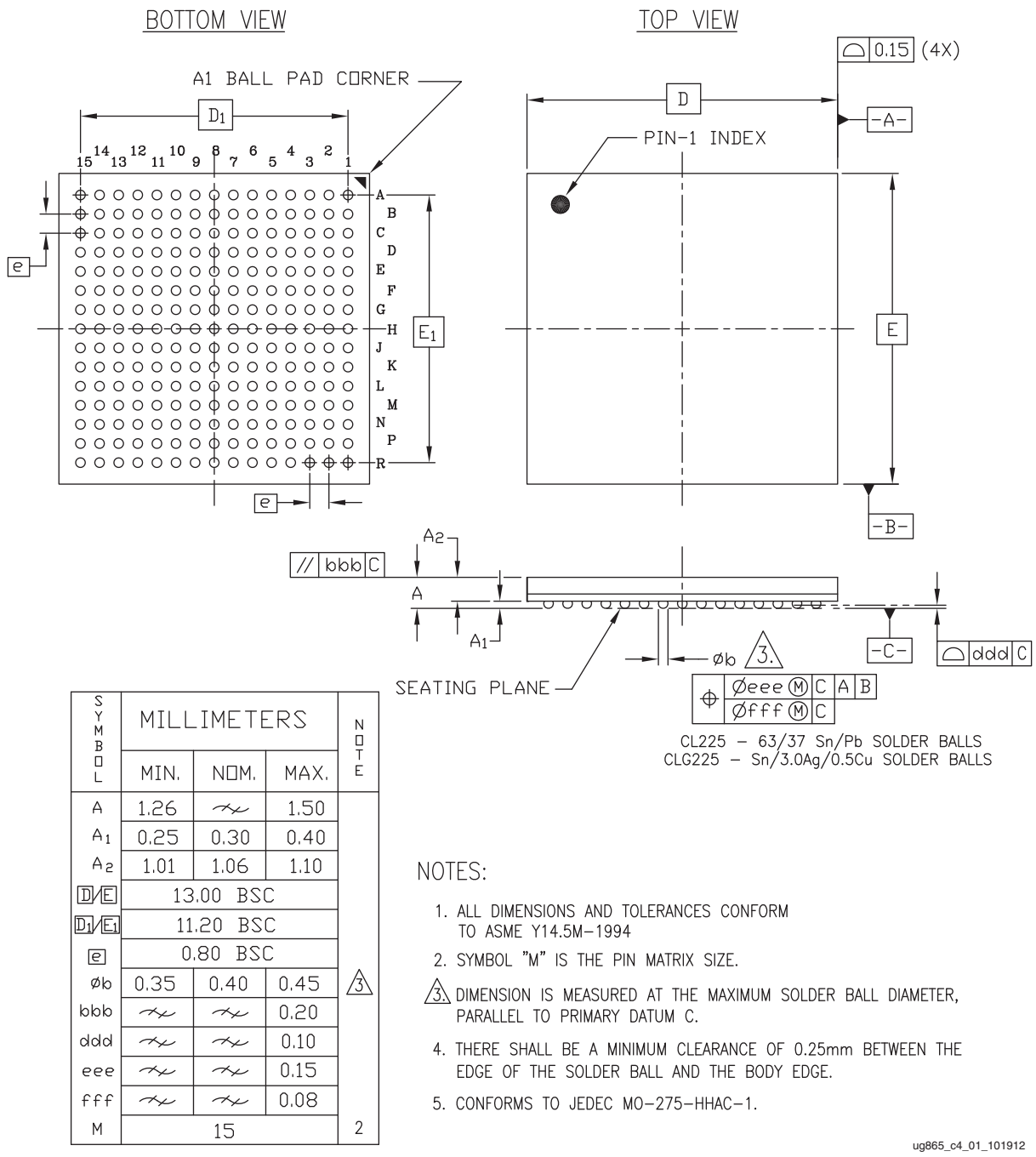
Summary

This chapter provides mechanical drawings (package specifications) of the following Zynq-7000 AP SoC packages:

- RF676 (XQ7Z030 and XQ7Z045) and RFG676 (XQ7Z045) Ruggedized Flip-Chip BGA (1.0 mm Pitch), page 91
- RF900 (XQ7Z045 and XQ7Z100) Ruggedized Flip-Chip BGA (1.0 mm Pitch), page 92
- RF1156 (XQ7Z100) Ruggedized Flip-Chip BGA (1.0 mm Pitch), page 93

Material Declaration Data Sheets (MDDS) are available for each package on the Xilinx website.

CLG225 Wire-Bond Chip-Scale BGA (XC7Z007S, XC7Z010, and XA7Z010) (0.8 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	1.26		1.50	
A_1	0.25	0.30	0.40	
A_2	1.01	1.06	1.10	
D/E	13.00 BSC			
D_1/E_1	11.20 BSC			
e	0.80 BSC			
øb	0.35	0.40	0.45	3
bbb			0.20	
ddd			0.10	
eee			0.15	
fff			0.08	
M	15			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.
5. CONFORMS TO JEDEC MO–275–HHAC–1.

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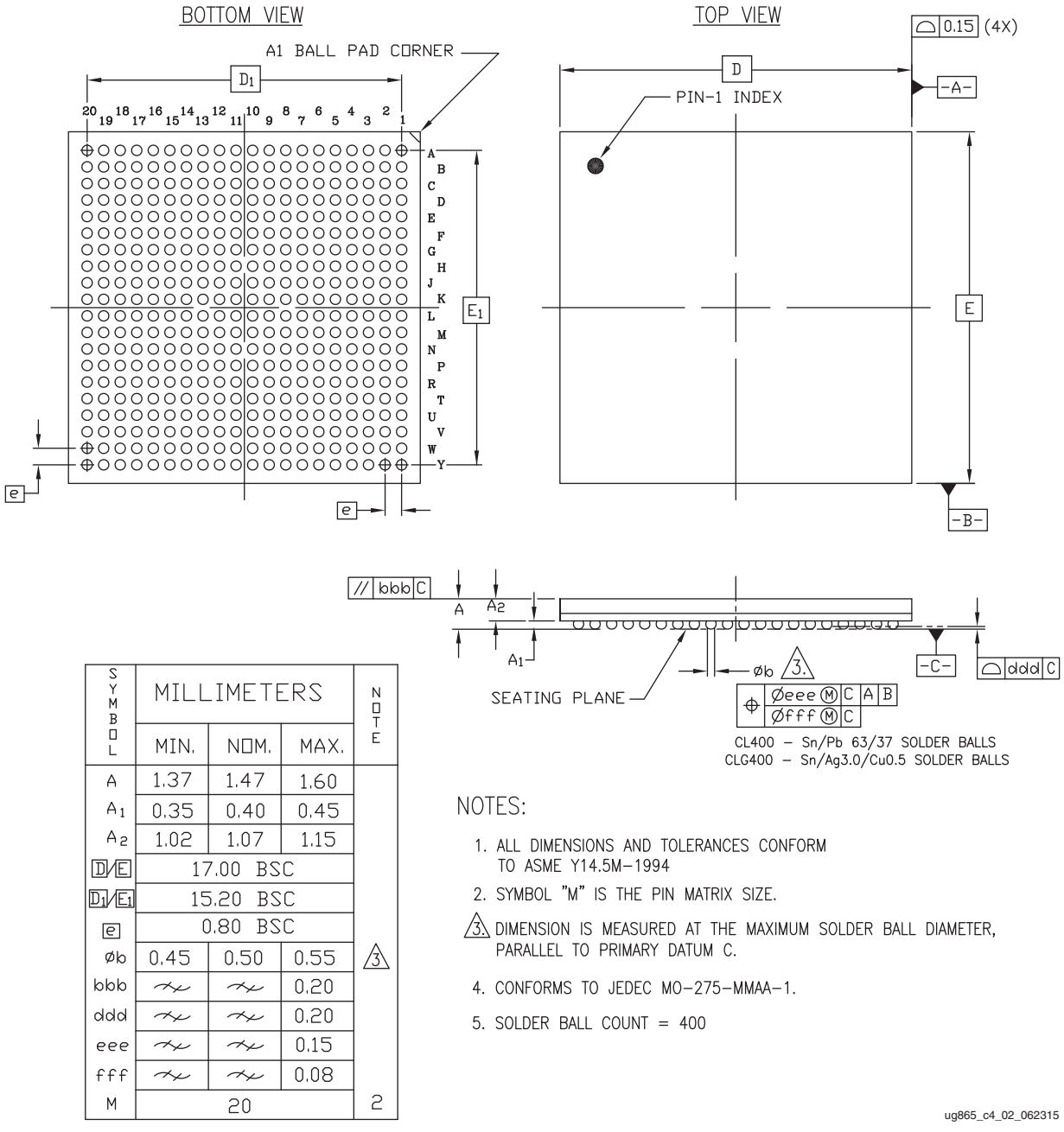
Figure 4-1: **CLG225 Wire-Bond Chip-Scale BGA Package Specifications for XC7Z007S, XC7Z010, and XA7Z010**

CLG400 (XC7Z007S, XC7Z010, XA7Z010, XC7Z014S, XC7Z020, and XA7Z020) and CL400 (XQ7Z020) Wire-Bond Chip-Scale BGA (0.8 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	1.37	1.47	1.60	
A_1	0.35	0.40	0.45	
A_2	1.02	1.07	1.15	
D/E	17.00 BSC			
D_1/E_1	15.20 BSC			
e	0.80 BSC			
øb	0.45	0.50	0.55	3
bbb	—	—	0.20	
ddd	—	—	0.20	
eee	—	—	0.15	
fff	—	—	0.08	
M	20			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. CONFORMS TO JEDEC MO–275–MMAA–1.
5. SOLDER BALL COUNT = 400

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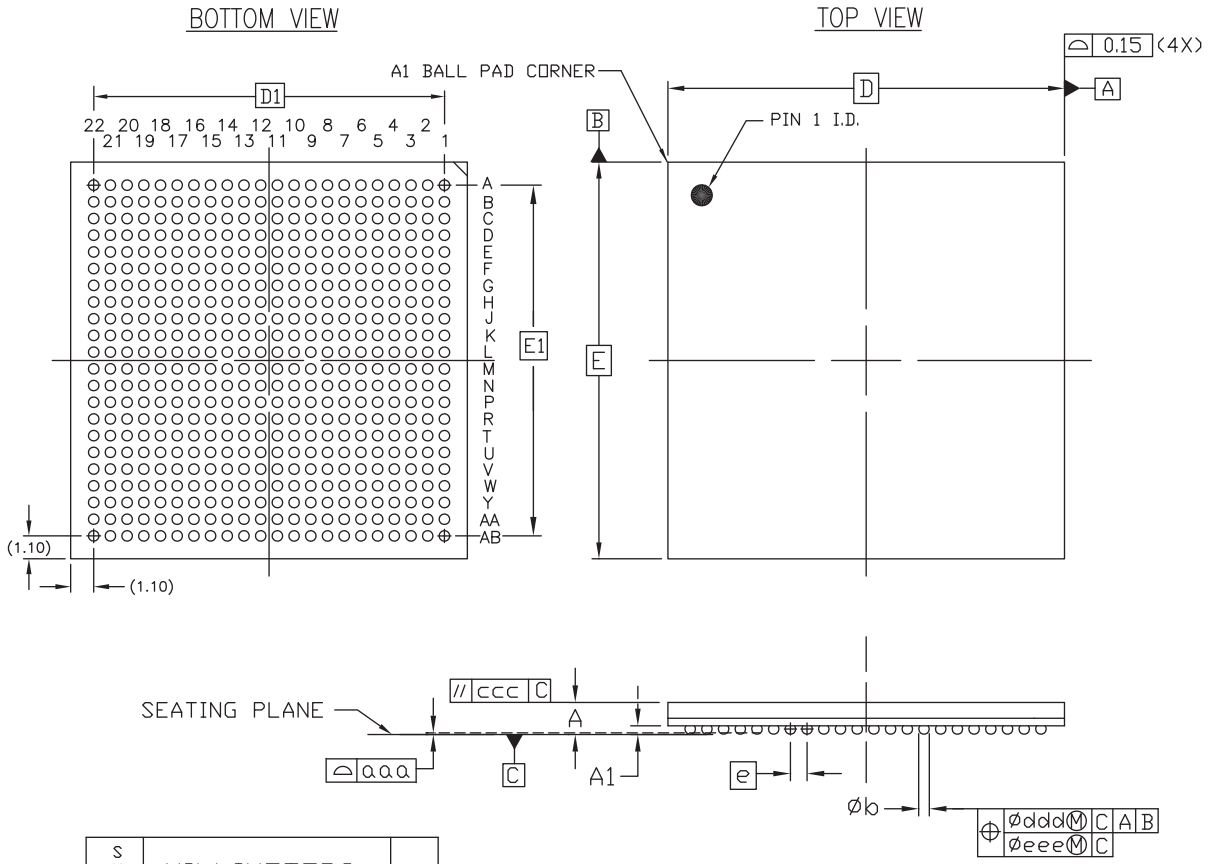
Figure 4-2: **CLG400 (XC7Z007S, XC7Z010, XA7Z010, XC7Z014S, XC7Z020, and XA7Z020) and CL400 (XQ7Z020) Wire-Bond Chip-Scale BGA Package Specifications**

CLG484 (XC7Z014S, XC7Z020, XA7Z020), CL484 (XQ7Z020) and CLG485 (XC7Z012S and XC7Z015) Wire-Bond Chip-Scale BGA (0.8 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	1.37	1.47	1.60	
A_1	0.35	0.40	0.45	
D/E	19.00 BSC			
D_1/E_1	16.80 BSC			
e	0.80 BSC			
øb	0.40	0.50	0.55	
aaa	~	~	0.20	
ccc	~	~	0.20	
ddd	~	~	0.15	
eee	~	~	0.08	
M	22			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MO–275–PPAA–2
4. SOLDER BALL COUNT = 484

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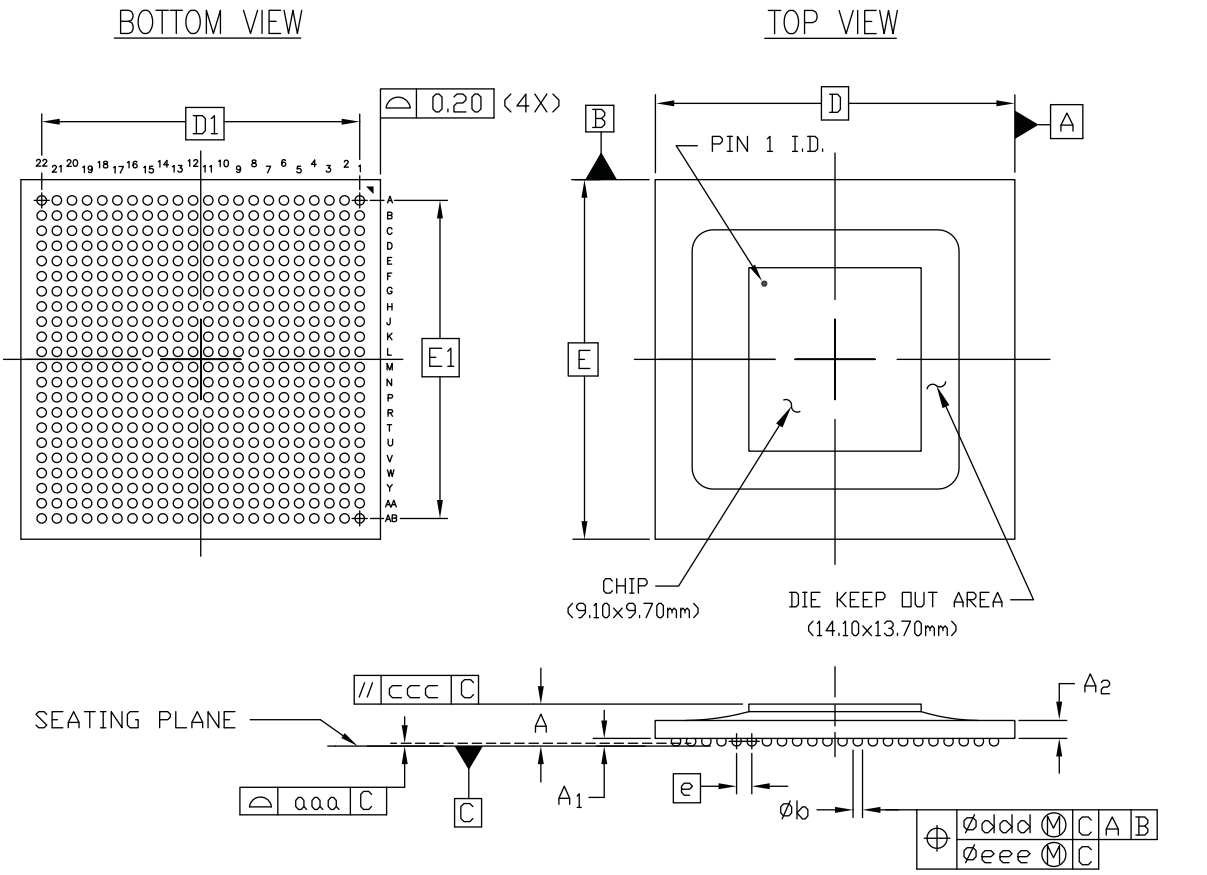
Figure 4-3: **CLG484 (XC7Z014S, XC7Z020, and XA7Z020), CL484 (XQ7Z020), and CLG485 (XC7Z012S and XC7Z015) Wire-Bond Chip-Scale BGA Package Specifications**

SBG485/SBV485 (XC7Z030) Flip-Chip Lidless BGA (0.8 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.04	2.24	2.44	
A_1	0.36	0.40	0.44	
A_2	0.88	0.98	1.08	
D/E	19.00 BASIC			
D_1/E_1	16.80 REF			
e	0.80 BASIC			
øb	0.45	0.50	0.55	
aaa	~	~	0.20	
ccc	~	~	0.20	
ddd	~	~	0.15	
eee	~	~	0.08	
M	22			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MO-275-PPA2 EXCEPT DIM "A"
4. SEE NEXT PAGE FOR CHIP CAPACITOR LOCATION

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Figure 4-4: **SBG485/SBV485 Flip-Chip Lidless BGA Package Specifications for XC7Z030**

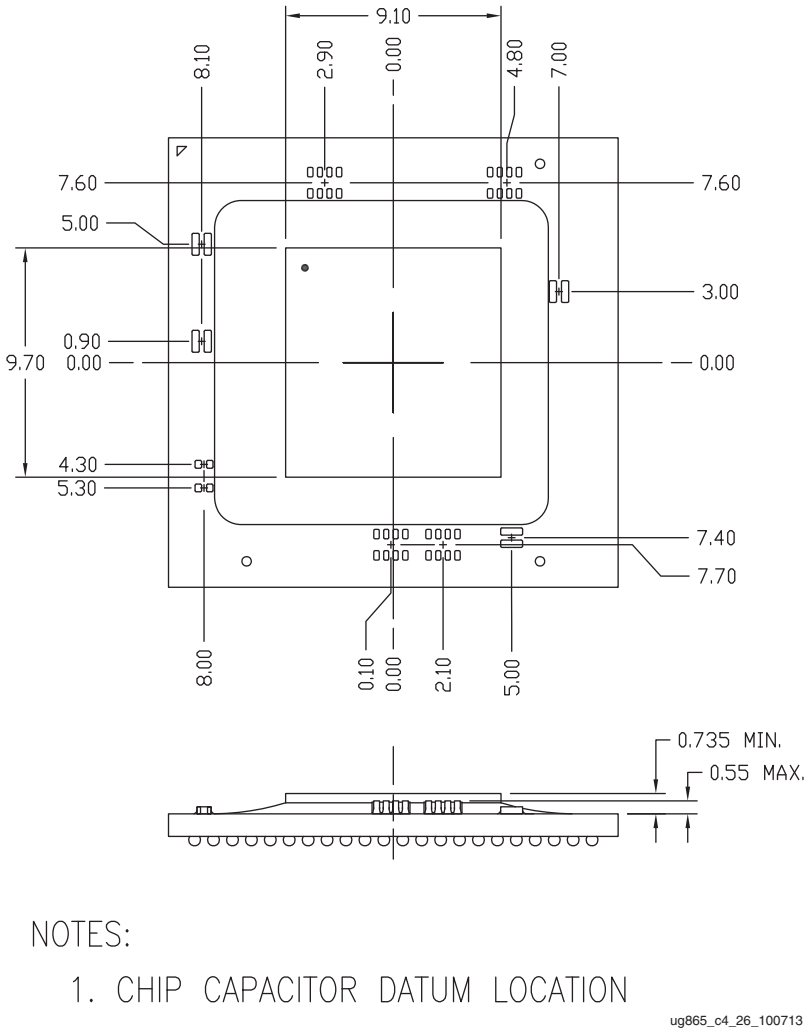
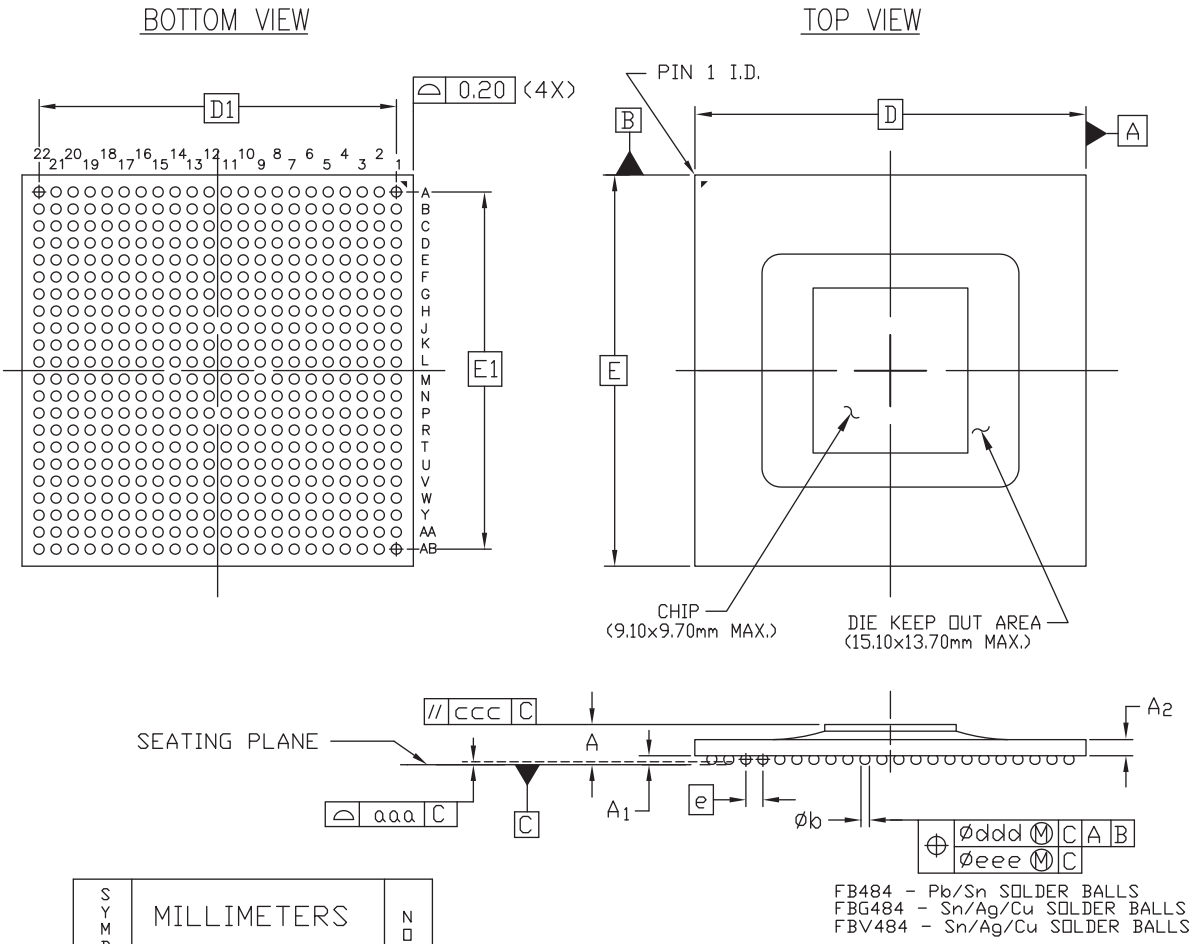


Figure 4-5: **XC7Z030 SBG485/SBV485 Die Dimensions with Capacitor Locations**

FBG484/FBV484 (XC7Z030, XA7Z030, and XQ7Z030) Flip-Chip Lidless BGA (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.14	2.34	2.54	
A_1	0.40	0.50	0.60	
A_2	0.83	0.98	1.13	
D/E	23.00 BASIC			
D_1/E_1	21.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa	~	~	0.20	
ccc	~	~	0.25	
ddd	~	~	0.25	
eee	~	~	0.10	
M	26			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MS–034
4. SEE FOLLOWING PAGE FOR CHIP CAPACITOR LOCATION

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Figure 4-6: **FBG484/FBV484 (XC7Z030, XA7Z030, and XQ7Z030) Flip-Chip Lidless BGA Package Specifications**

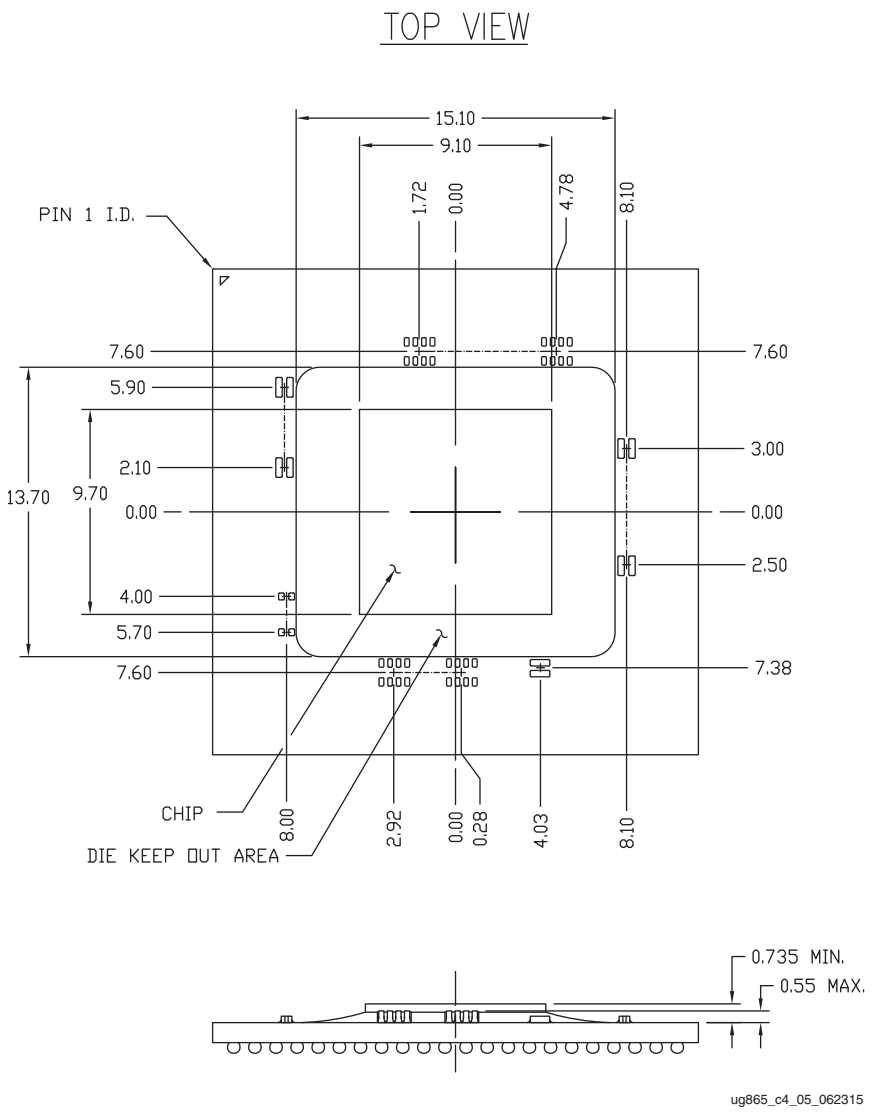
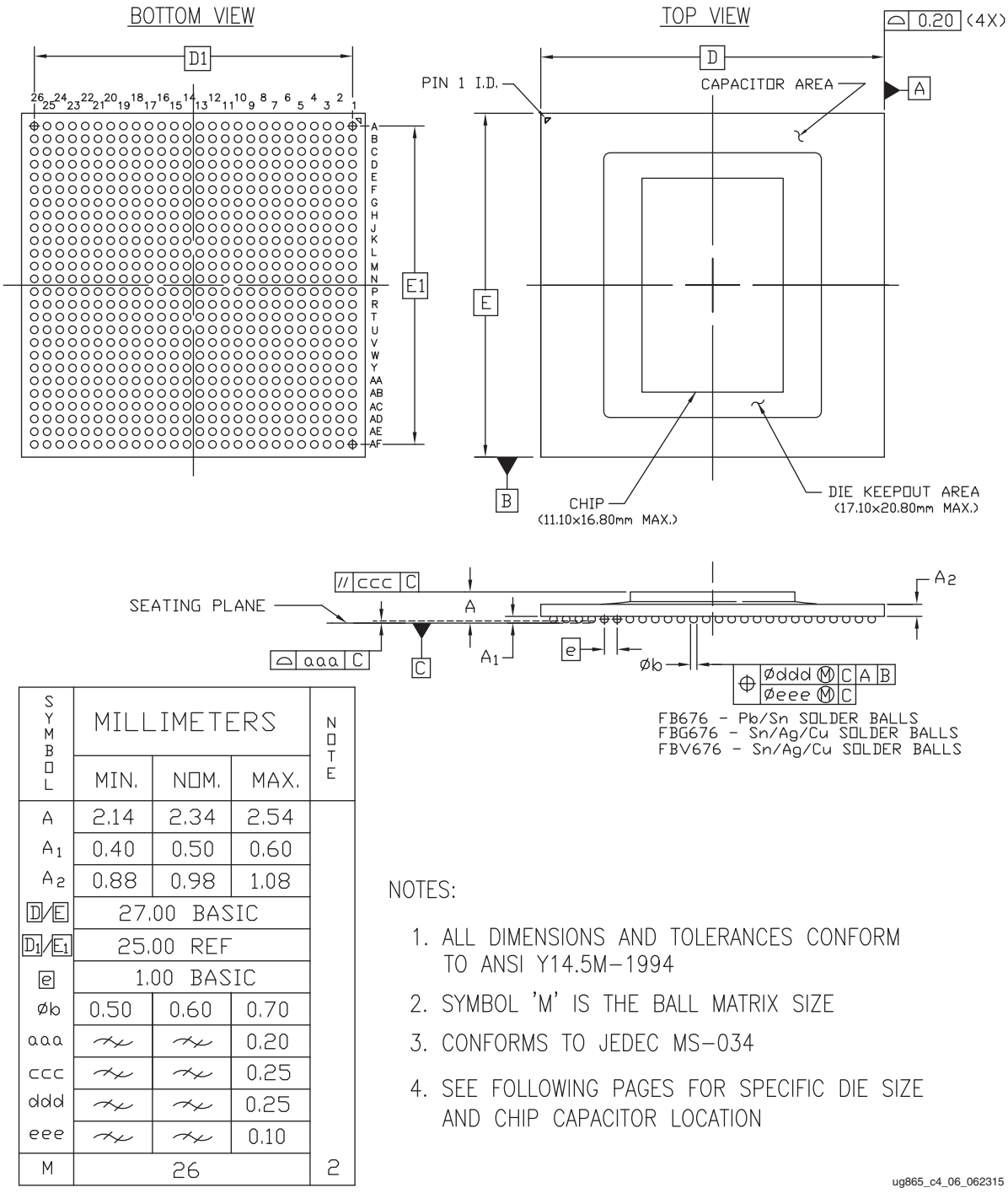


Figure 4-7: **XC7Z030 and XA7Z030 FBG484/FBV484 Die Dimensions with Capacitor Locations**

FBG676/FBV676 (XC7Z030, XC7Z035, and XC7Z045) Flip-Chip Lidless BGA (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.14	2.34	2.54	
A_1	0.40	0.50	0.60	
A_2	0.88	0.98	1.08	
D/E	27.00 BASIC			
D_1/E_1	25.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa	~	~	0.20	
ccc	~	~	0.25	
ddd	~	~	0.25	
eee	~	~	0.10	
M	26			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MS–034
4. SEE FOLLOWING PAGES FOR SPECIFIC DIE SIZE AND CHIP CAPACITOR LOCATION

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Figure 4-8: **FBG676/FBV676 (XC7Z030, XC7Z035, and XC7Z045) Flip-Chip Lidless BGA Package Specifications**

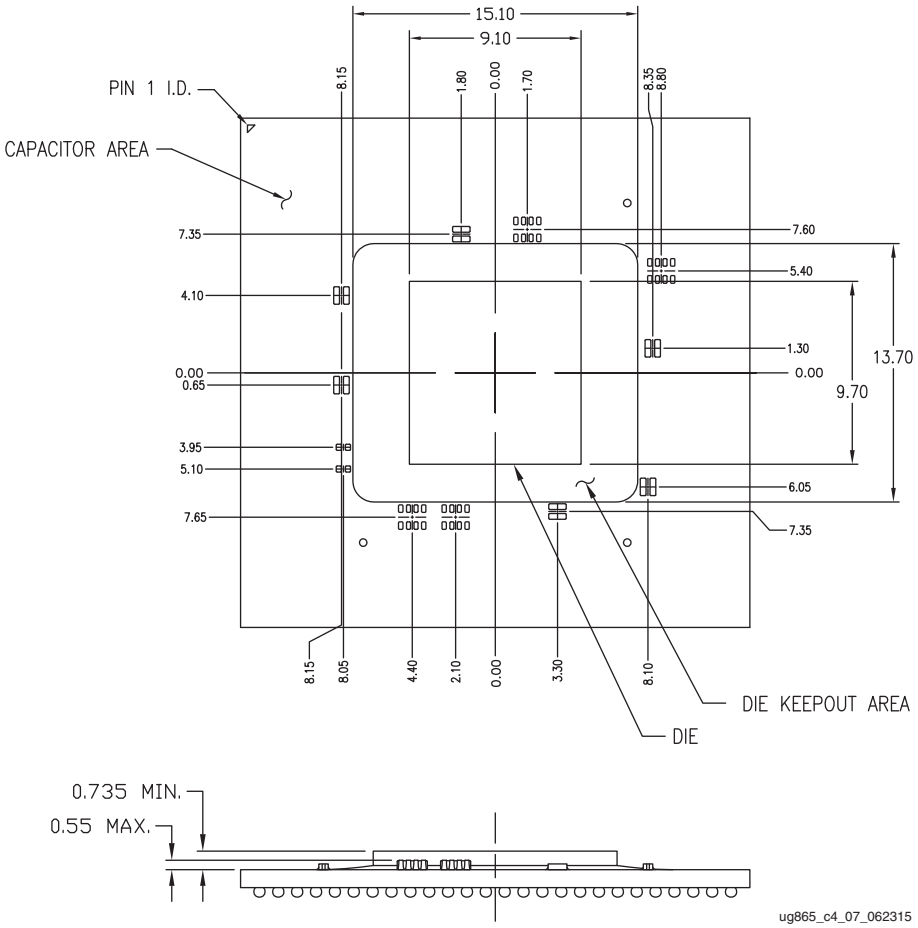


Figure 4-9: **XC7Z030 FBG676/FBV676 Die Dimensions with Capacitor Locations**

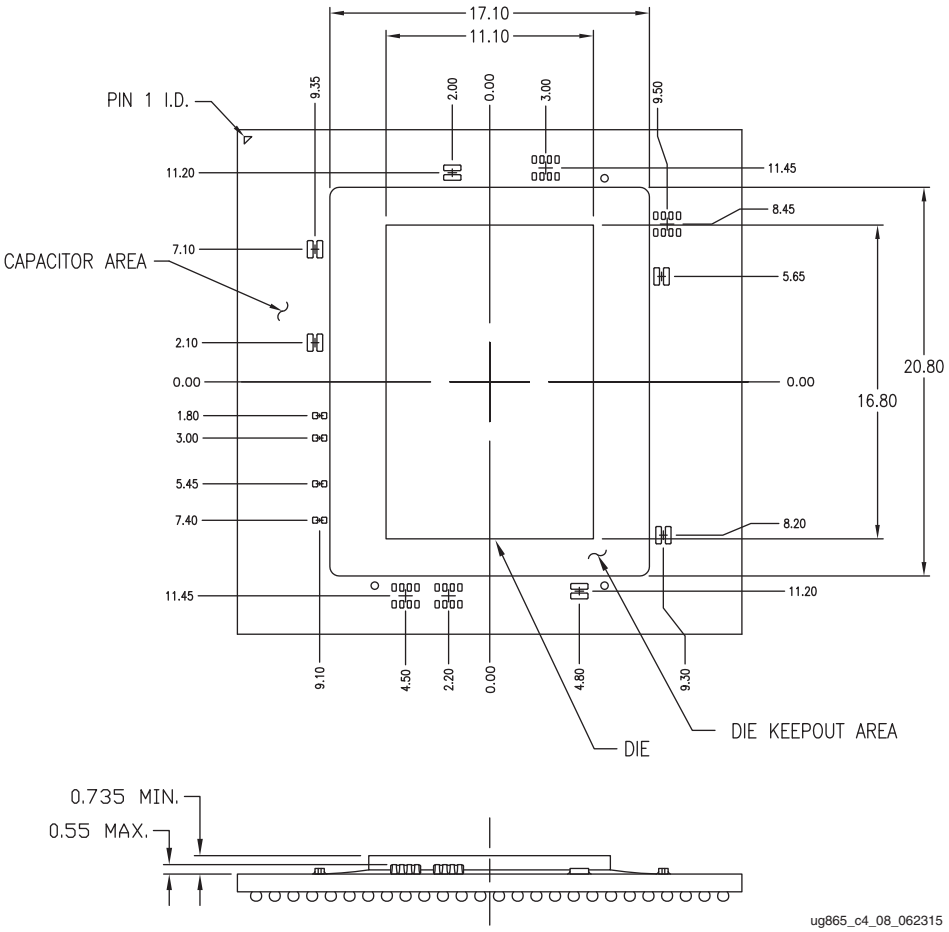
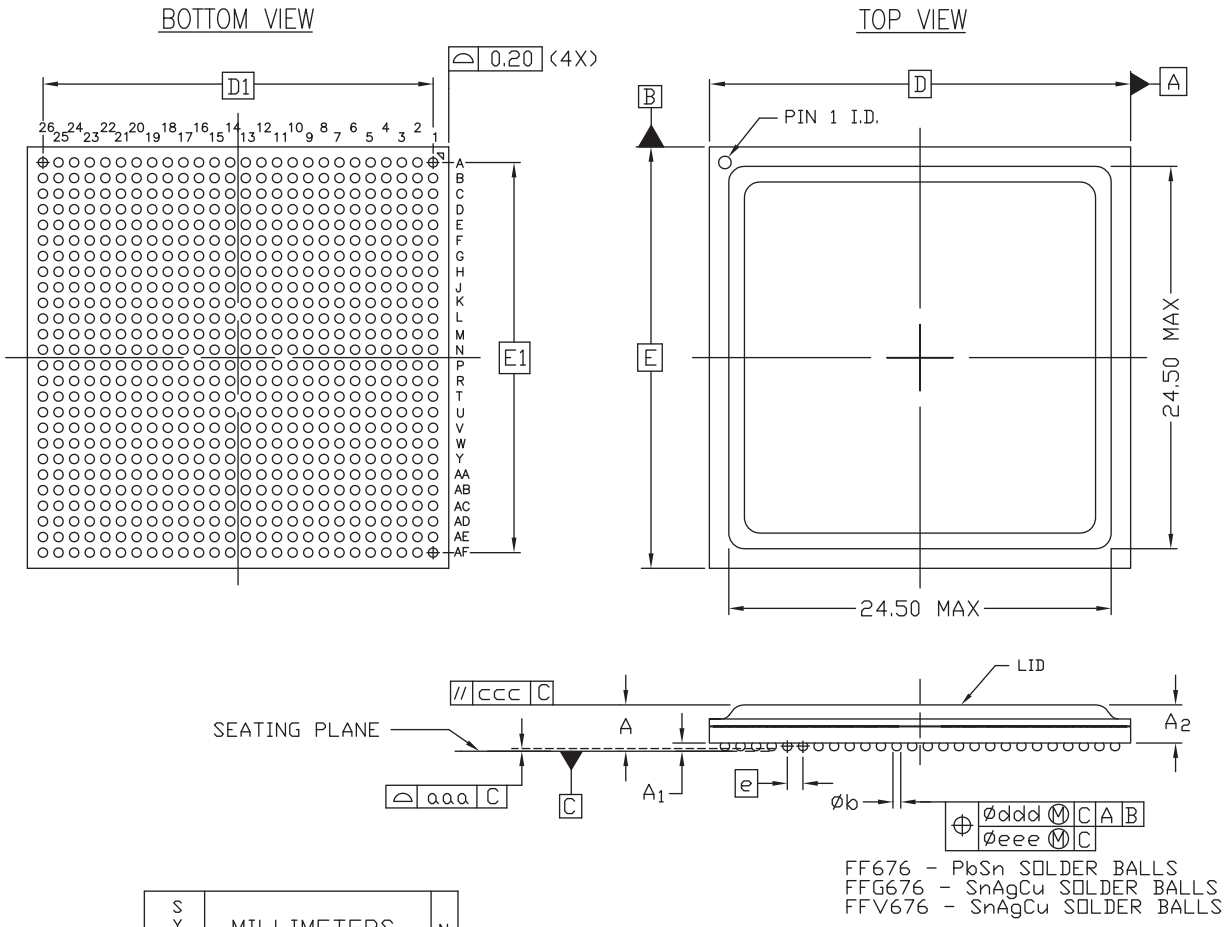


Figure 4-10: **XC7Z035 and XC7Z045 FBG676/FBV676 Die Dimensions with Capacitor Locations**

FFG676/FFV676 (XC7Z030) Flip-Chip BGA (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.64		3.24	
A_1	0.40	0.50	0.60	
A_2	2.24		2.64	
D/E	27.00 BASIC			
D_1/E_1	25.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa			0.20	
ccc			0.25	
ddd			0.25	
eee			0.10	
M	26			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAL–1

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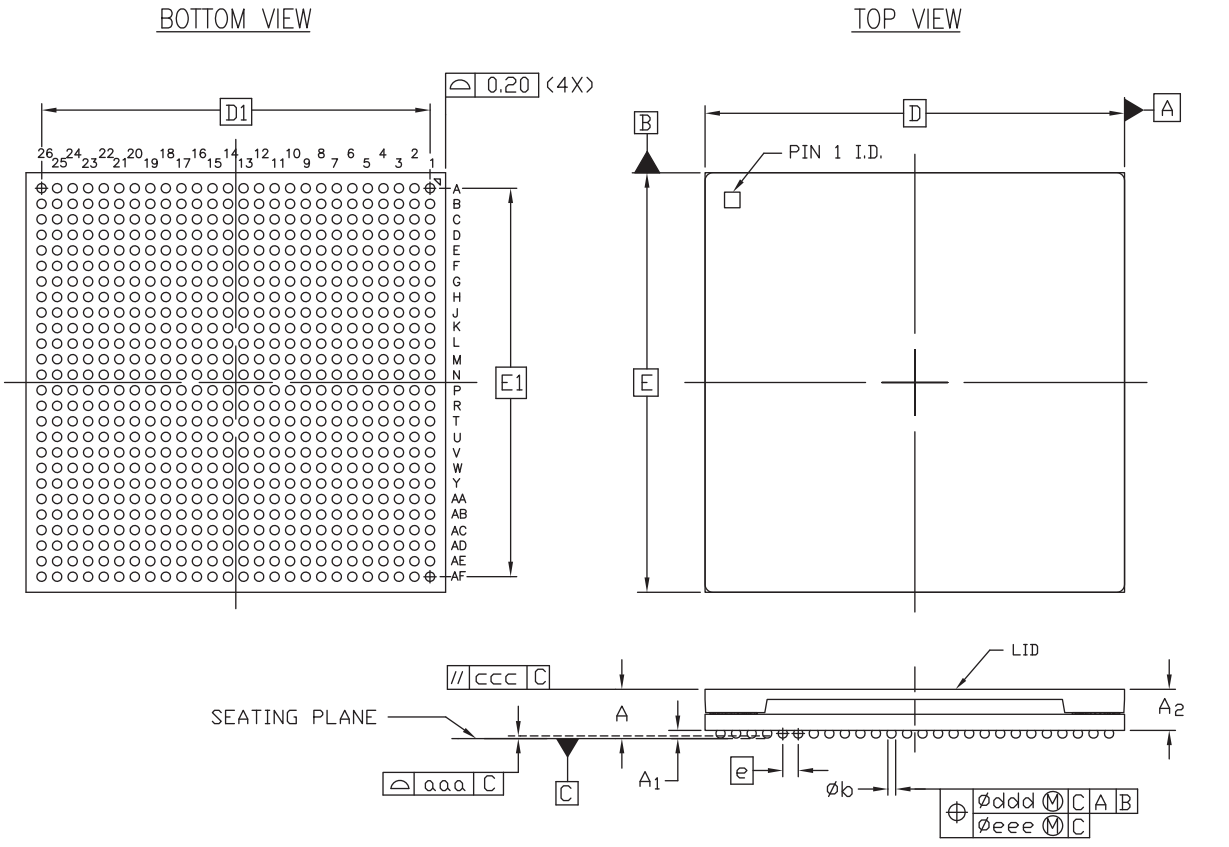
Figure 4-11: **FFG676/FFV676 (XC7Z030) Flip-Chip BGA Package Specifications**

FFG676/FFV676 Flip-Chip BGA (XC7Z035 and XC7Z045)(1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.97	3.17	3.37	
A_1	0.40	0.50	0.60	
A_2	2.57	~	2.77	
D/E	27.00 BASIC			
D_1/E_1	25.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa	~	~	0.20	
ccc	~	~	0.25	
ddd	~	~	0.25	
eee	~	~	0.10	
M	26			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAL–1

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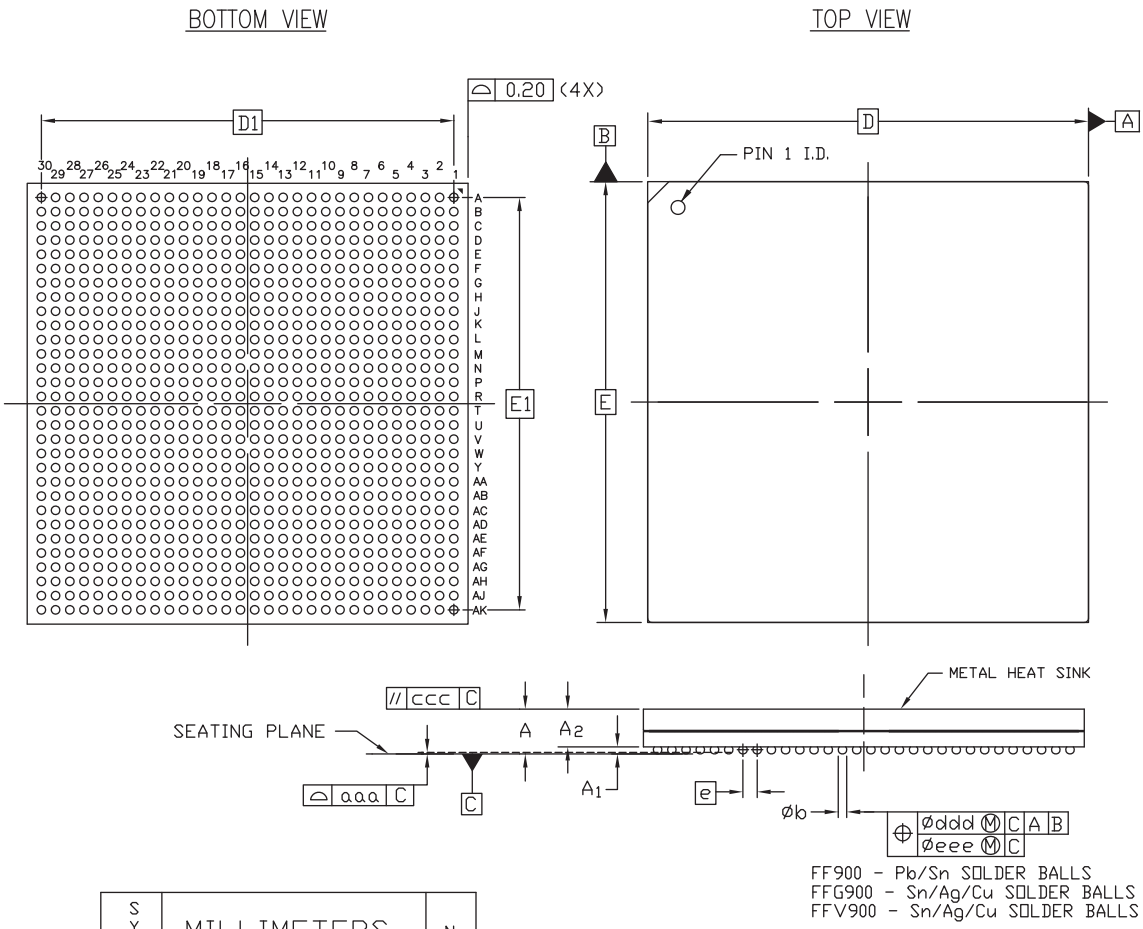
Figure 4-12: **FFG676/FFV676 (XC7Z035 and XC7Z045) Flip-Chip BGA Package Specifications**

FFG900/FFV900 (XC7Z035, XC7Z045, and XC7Z100) Flip-Chip BGA (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.95	3.15	3.35	
A_1	0.40	0.50	0.60	
A_2	2.55	~~	2.75	
D/E	31.00 BASIC			
D_1/E_1	29.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	4
aaa	~~	~~	0.20	
ccc	~~	~~	0.35	
ddd	~~	~~	0.30	
eee	~~	~~	0.10	
M	30			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MS–034–AAN–1
4. ACTUAL SOLDER BALL COUNT = 900

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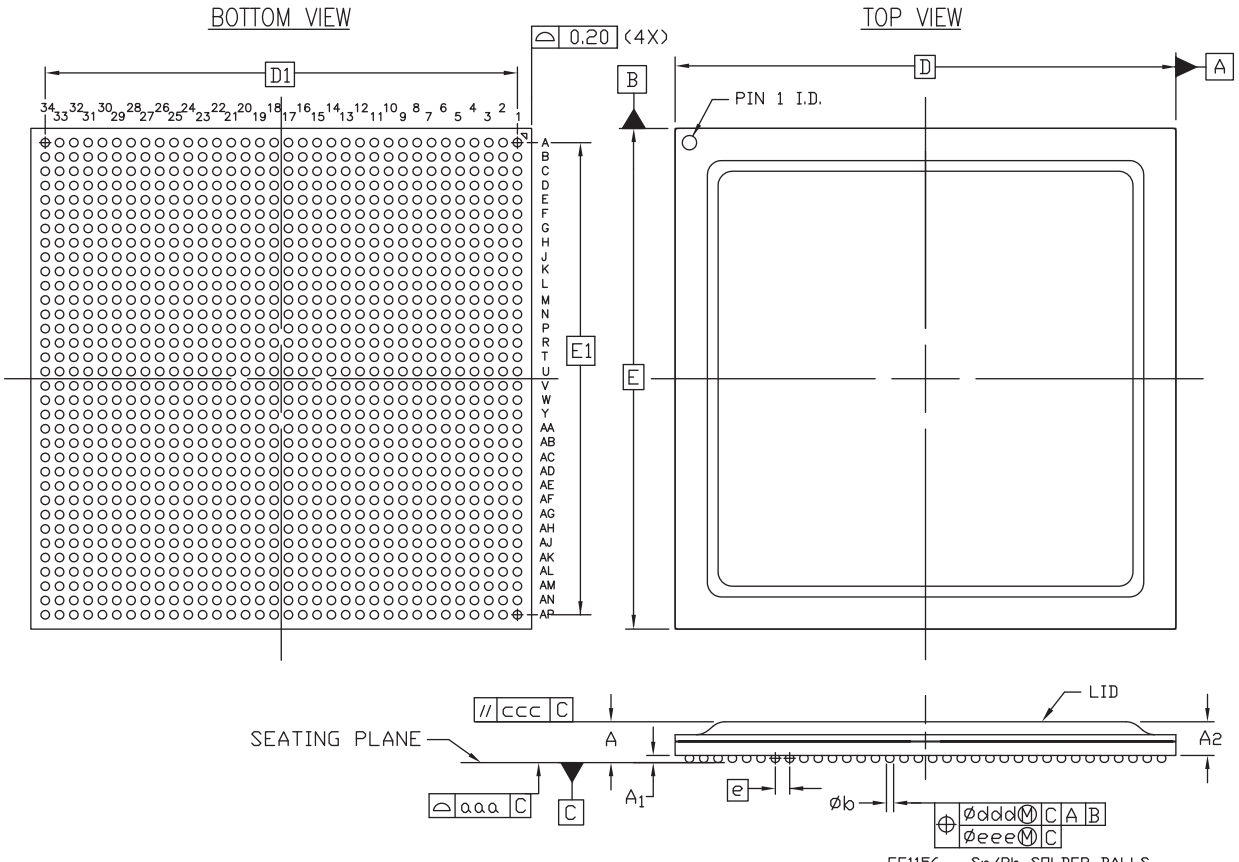
Figure 4-13: **FFG900/FFV900 (XC7Z035, XC7Z045, and XC7Z100) Flip-Chip BGA Package Specifications**

FFG1156/FFV1156 (XC7Z100) Flip-Chip BGA (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.70	2.90	3.10	
A_1	0.40	0.50	0.60	
A_2	2.30	2.40	2.50	
D/E	35.00 BASIC			
D_1/E_1	33.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	4
aaa			0.20	
ccc			0.35	
ddd			0.30	
eee			0.10	
M	34			2

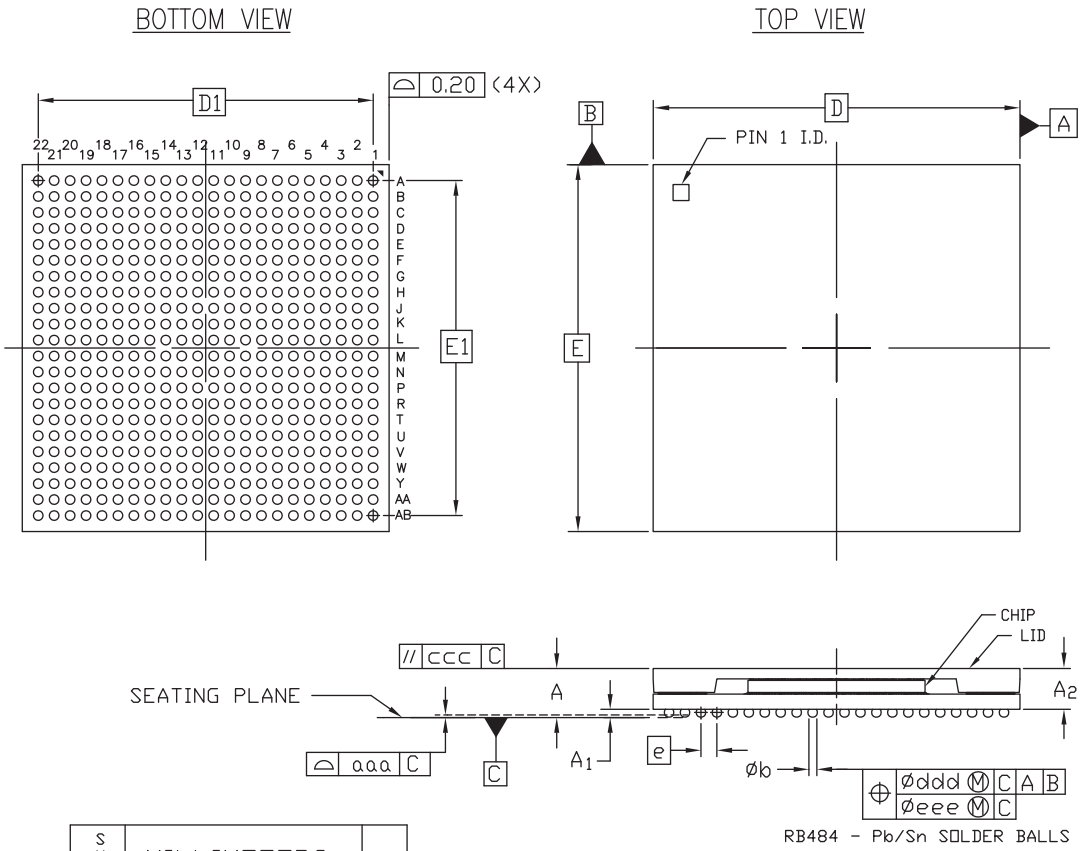
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MS–034–AAR–1
4. ACTUAL SOLDER BALL COUNT = 1156

ug865_c4_12_0062315

Figure 4-14: **FFG1156/FFV1156 Flip-Chip BGA Package Specifications for XC7Z100**

RB484 Ruggedized Flip-Chip BGA (XQ7Z030) (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.75	3.05	3.35	
A_1	0.40	0.50	0.60	
A_2	2.35	2.55	2.75	
D/E	23.00 BASIC			
D_1/E_1	21.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa			0.20	
ccc			0.25	
ddd			0.25	
eee			0.10	
M	26			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MS–034

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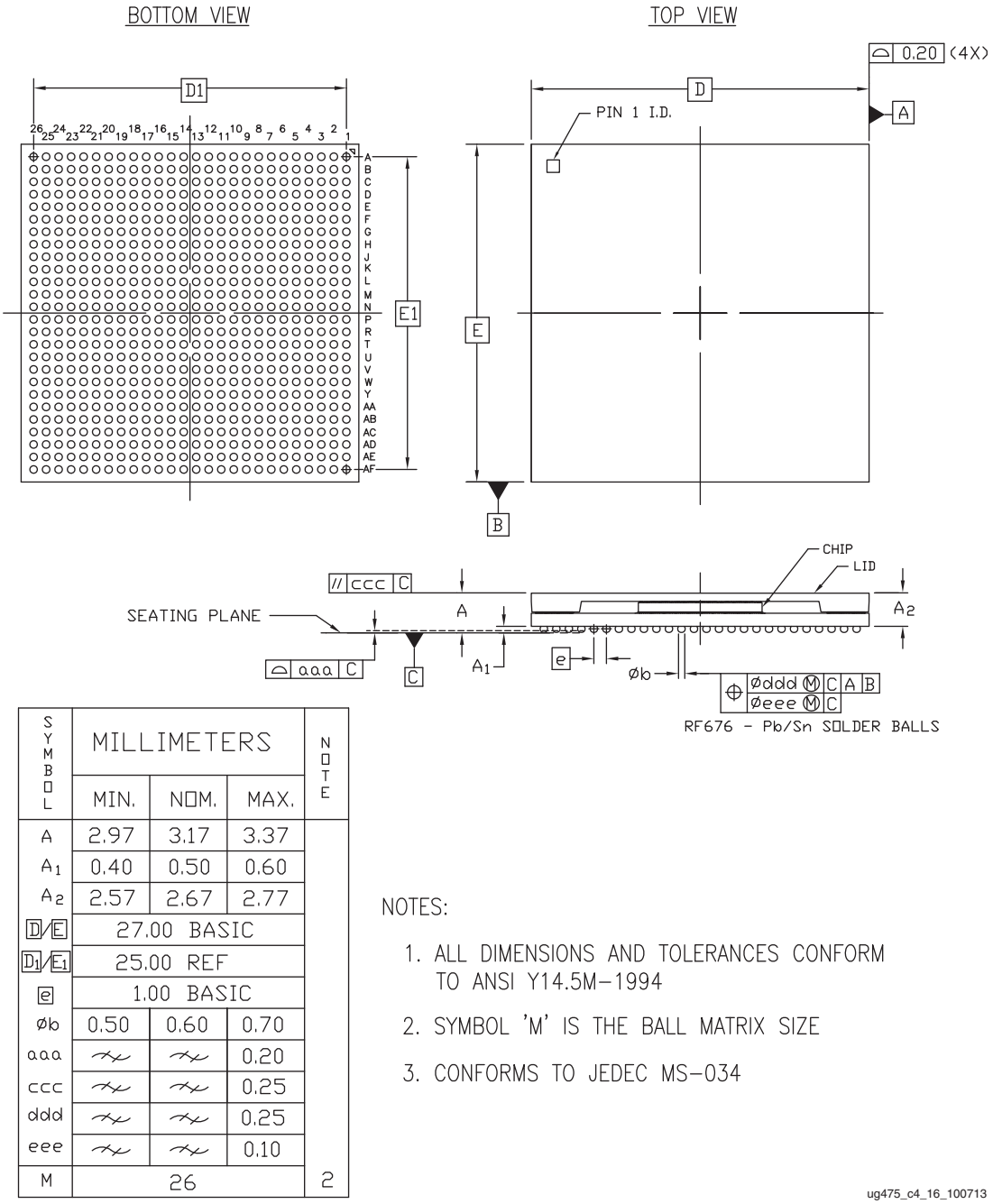
Figure 4-15: **RB484 Ruggedized Flip-Chip BGA Package Specifications for XQ7Z030**

RF676 (XQ7Z030 and XQ7Z045) and RFG676 (XQ7Z045) Ruggedized Flip-Chip BGA (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.97	3.17	3.37	
A_1	0.40	0.50	0.60	
A_2	2.57	2.67	2.77	
D/E	27.00 BASIC			
D_1/E_1	25.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa			0.20	
ccc			0.25	
ddd			0.25	
eee			0.10	
M	26			2

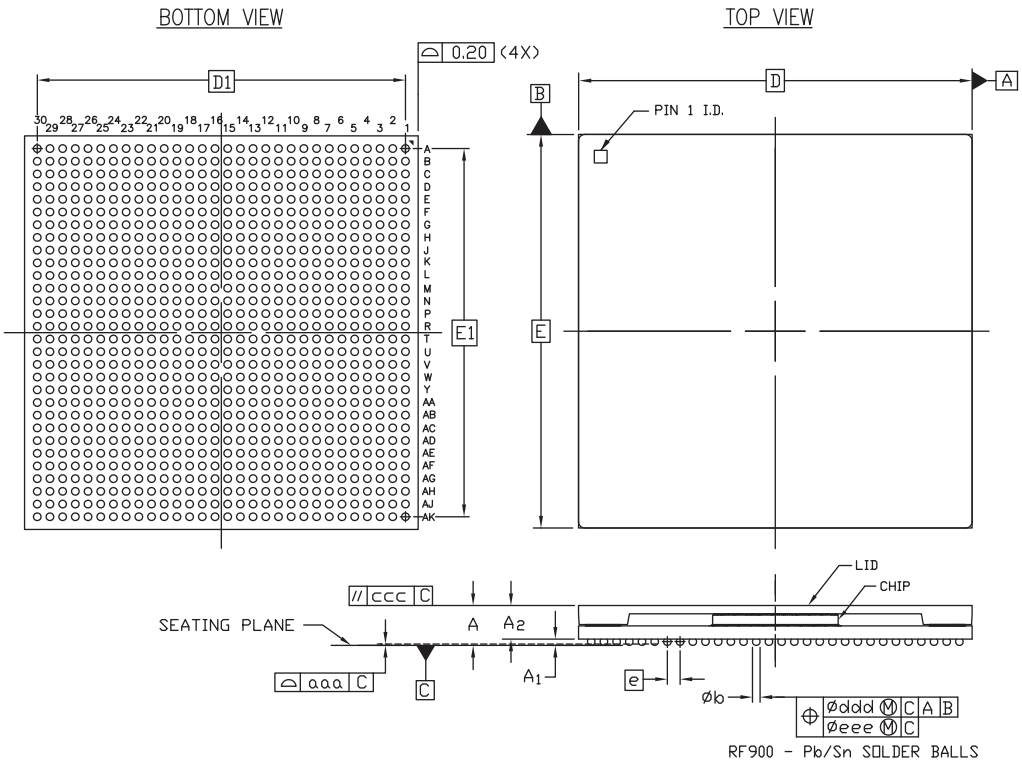
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MS–034

ug475_c4_16_100713

Figure 4-16: **RF676/RFG676 Ruggedized Flip-Chip BGA Package Specifications for XQ7Z030 and XQ7Z045**

RF900 (XQ7Z045 and XQ7Z100) Ruggedized Flip-Chip BGA (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.84	3.14	3.44	
A_1	0.40	0.50	0.60	
A_2	2.44	2.64	2.84	
D/E	31.00 BASIC			
D_1/E_1	29.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa			0.20	
ccc			0.35	
ddd			0.30	
eee			0.10	
M	30			2

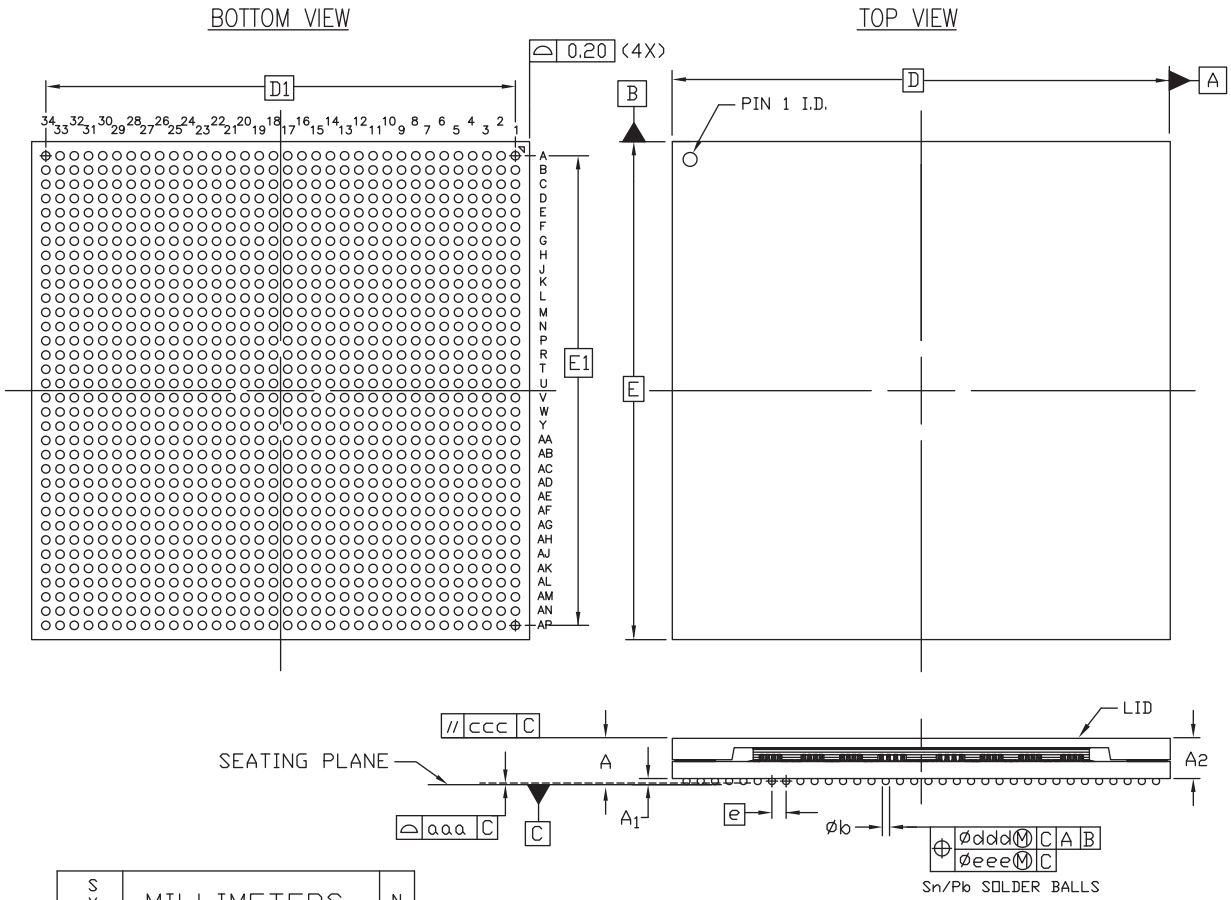
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MS–034–AAN–1

ug865_c4_27_050714

Figure 4-17: **RF900 Ruggedized Flip-Chip BGA Package Specifications for the XQ7Z045 and XQ7Z100**

RF1156 (XQ7Z100) Ruggedized Flip-Chip BGA (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	3.03	3.28	3.53	
A_1	0.40	0.50	0.60	
A_2	2.63	2.78	2.93	
D/E	35.00 BASIC			
D_1/E_1	33.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	4
aaa			0.20	
ccc			0.35	
ddd			0.30	
eee			0.10	
M	34			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAR–1
4. ACTUAL SOLDER BALL COUNT = 1156

ug865_c4_18_071014

Figure 4-18: **RF1156 Ruggedized Flip-Chip BGA Package Specifications for the XQ7Z100**

Thermal Specifications

Summary

This chapter provides thermal data associated with Zynq-7000 AP SoC packages. The following topics are discussed:

- Introduction
- Thermal Resistance Data
- Support for Thermal Models
- Thermal Management Strategy
- Thermal Interface Material
- Heat Sink Removal Procedure
- Soldering Guidelines
- References

Introduction

Zynq-7000 AP SoC devices are offered in thermally efficient wire-bond and flip-chip BGA packages. These 0.8 mm pitch and 1.0 mm pitch packages range in pin-count from the smaller 13 x 13 mm CLG225 to the 35 x 35 mm FFG1156. The suite of packages is used to address the various power requirements of the Zynq-7000 AP SoC devices. All Zynq-7000 AP SoC devices are implemented in the 28 nm process technology.

Unlike features in an ASIC or ASSP, the combination of device features used in a user application are not known to the component supplier. Therefore, it remains a challenge for Xilinx to predict the power requirements of a given device when it leaves the factory. Accurate estimates are obtained when the board design takes shape. For this purpose, Xilinx offers and supports a suite of integrated device power analysis tools to help users quickly and accurately estimate their design power requirements. Zynq-7000 AP SoC devices are supported similarly to previous Xilinx products. The uncertainty of design power requirements makes it difficult to apply canned thermal solutions to fit all users. Therefore,

Xilinx devices do not come with preset thermal solutions. Your design's operating conditions dictate the appropriate solution.

Thermal Resistance Data

Table 5-1 shows the thermal resistance data for Zynq-7000 AP SoC devices (grouped in the packages offered). The data includes junction-to-ambient in still air, junction-to-case, and junction-to-board data based on standard JEDEC four-layer measurements.

IMPORTANT: *The data in Table 5-1 is for device/package comparison purposes only. Attempts to recreate this data are only valid using the transient 2-phase measurement techniques outlined in JESD51-14.*

TIP: *The thermal data query for all available devices by package is available on the Xilinx website:* www.xilinx.com/cgi-bin/thermal/thermal.pl.

Table 5-1: **Thermal Resistance Data—Zynq-7000 AP SoC Devices**

Package	Package Body Size	Devices	θ_{JB} (°C/W)	θ_{JC} (°C/W)	θ_{JA} (°C/W)	$\theta_{JA\text{-}Effective}$ (°C/W)(1)		
						@250 LFM	@500 LFM	@750 LFM
CLG225	13 x 13	XC7Z007S	11.6	4.95	25.4	20.3	18.6	17.6
		XC7Z010	11.6	4.95	25.4	20.3	18.6	17.6
		XA7Z010	11.6	4.95	25.4	20.3	18.6	17.6
CLG400	17 x 17	XC7Z007S	9.3	4.52	20.9	16.4	15.1	14.4
		XC7Z010	9.3	4.52	20.9	16.4	15.1	14.4
		XA7Z010	9.3	4.52	20.9	16.4	15.1	14.4
		XC7Z014S	7.4	3.44	19.0	14.6	13.4	12.7
		XC7Z020	7.4	3.44	19.0	14.6	13.4	12.7
		XA7Z020	7.4	3.44	19.0	14.6	13.4	12.7
CLG484	19 x 19	XC7Z014S	7.4	3.35	18.2	13.9	12.6	12.0
		XC7Z020	7.4	3.35	18.2	13.9	12.6	12.0
		XA7Z020	7.4	3.35	18.2	13.9	12.6	12.0
CLG485	19 x 19	XC7Z012S	7.7	3.45	18.5	13.4	12.2	11.6
		XC7Z015	7.7	3.45	18.5	13.4	12.2	11.6
SBG485 SBV485	19 x 19	XC7Z030	5.8	0.10	16.2	11.9	10.7	10.1
FBG484 FBV484	23 x 23	XC7Z030	5.7	0.10	15.2	11.1	10.0	9.5
		XA7Z030	5.7	0.10	15.2	11.1	10.0	9.5

Table 5-1: **Thermal Resistance Data—Zynq-7000 AP SoC Devices *(Cont'd)***

Package	Package Body Size	Devices	θ_{JB} (°C/W)	θ_{JC} (°C/W)	θ_{JA} (°C/W)	$\theta_{JA\text{-}Effective}$ (°C/W)(1)		
						@250 LFM	@500 LFM	@750 LFM
FBG676 FBV676	27 x 27	XC7Z030	5.6	0.10	14.5	10.5	9.5	9.0
		XC7Z035	4.0	0.06	12.6	8.7	7.8	7.3
		XC7Z045	4.0	0.06	12.6	8.7	7.8	7.3
FFG676 FFV676	27 x 27	XC7Z030	3.6	0.46	11.5	7.7	6.8	6.3
		XC7Z035	3.4	0.23	11.0	7.2	6.2	5.6
		XC7Z045	3.4	0.23	11.0	7.2	6.2	5.6
FFG900 FFV900	31 x 31	XC7Z035	2.7	0.23	9.6	6.5	5.6	5.1
		XC7Z045	2.7	0.23	9.6	6.5	5.6	5.1
		XC7Z100	2.6	0.18	9.5	6.2	5.2	4.6
FFG1156 FFV1156	35 x 35	XC7Z100	2.4	0.18	9.0	5.9	4.9	4.4
CL400	17 x 17	XQ7Z020	7.4	3.44	19.0	14.6	13.4	12.7
CL484	19 x 19	XQ7Z020	7.4	3.35	18.2	13.9	12.6	12.0
RB484	23 x 23	XQ7Z030	4.4	0.37	12.8	8.6	7.5	6.8
RF676	27 x 27	XQ7Z030	4.2	0.48	12.0	7.9	6.8	6.2
RFG676		XQ7Z045	3.4	0.23	11.0	7.2	6.2	5.6
RF900	31 x 31	XQ7Z045	3.2	0.23	10.0	6.4	5.4	4.9
		XQ7Z100	3.0	0.18	9.8	6.5	5.5	4.9
RF1156	35 x 35	XQ7Z100	2.8	0.18	8.9	5.6	4.7	4.3

Notes:

1. All $\theta_{JA\text{-}Effective}$ values assume no heat sink and include thermal dissipation through a standard JEDEC four-layer board. The Xilinx power estimation tools (Vivado® Power Analysis, and Xilinx Power Estimator), which require detailed board dimensions and layer counts, are useful for deriving more precise $\theta_{JA\text{-}Effective}$ values.

Support for Thermal Models

Table 5-1 provides the traditional thermal resistance data for Zynq-7000 AP SoC devices. These resistances are measured using a prescribed JEDEC standard that might not necessarily reflect the user's actual board conditions and environment. The quoted θ_{JA} and θ_{JC} numbers are environmentally dependent, and JEDEC has traditionally recommended that these be used with that awareness. For more accurate junction temperature predictions, a system-level thermal simulation might be required.

Though Xilinx continues to support this figure of merit data, for Zynq-7000 AP SoC devices, boundary conditions independent thermal resistor network (Delphi) models are offered. These compact models seek to capture the thermal behavior of the packages more

accurately at predetermined critical points (junction, case, top, leads, and so on) with the reduced set of nodes as illustrated in Figure 5-1.

Unlike a full 3D model, these are computationally efficient and work well in an integrated system simulation environment. Delphi models are available for download on the Xilinx website (under the Device Model tab).

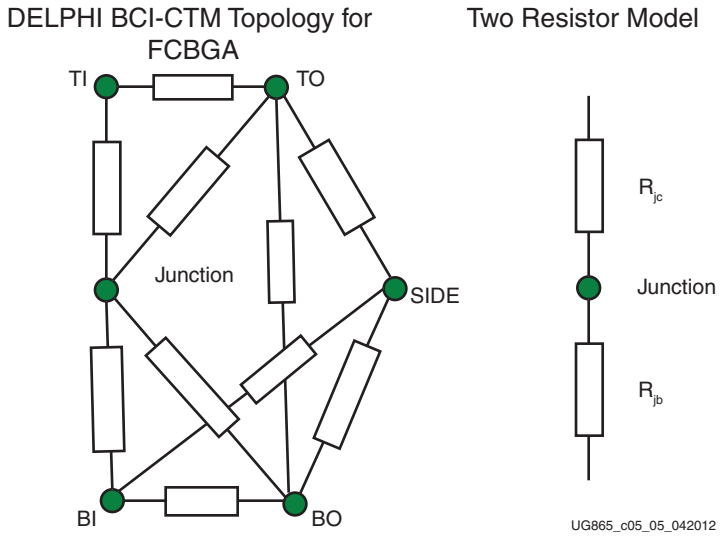


Figure 5-1: **Thermal Model Topologies**

RECOMMENDED: *Xilinx recommends use of the Delphi thermal model during thermal modeling of a package. The Delphi thermal model includes consideration of the thermal interface material parameters and the manufacture variation on the thermal solution. Examples of manufacture variations include the tolerance in airflow from a fan, the tolerance on performance of the heat pipe and vapor chamber, and the manufacture variation of the attachment of fins to the heat-sink base and the flatness of the surface.*

Thermal Management Strategy

As described in this section, Xilinx relies on a multi-pronged approach to consuming less power and dissipating heat for systems using Zynq-7000 AP SoC devices.

Cavity-Up Plastic BGA Packages

BGA is a plastic package technology that utilizes area array solder balls at the bottom of the package to make electrical contact with the circuit board in the users system. The area array format of solder balls reduces package size considerably when compared to leaded products. It also results in improved electrical performance as well as having higher manufacturing yields. The substrate is made of a multi-layer BT (bismaleimide triazene)

epoxy-based material. Power and ground pins are grouped together and signal pins are assigned to the perimeter for ease of routing on the board. The package is offered in a die-up format and contains a wire-bond device covered with a mold compound. As shown in the cross section of Figure 5-2, the BGA package contains a wire- bond die on a single-core printed circuit board with an overmold.

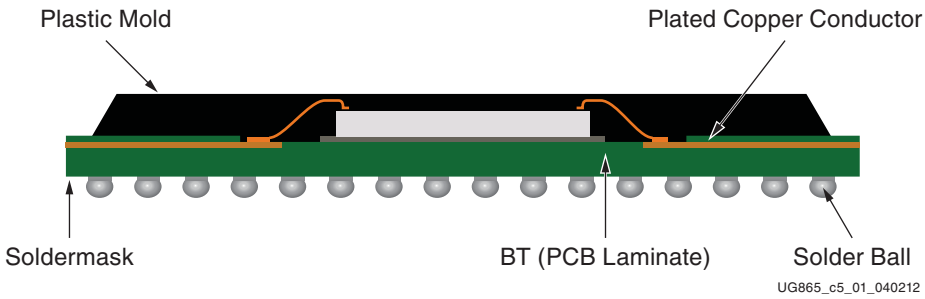


Figure 5-2: **Cavity-Up Ball Grid Array Package**

The key features/advantages of cavity-up BGA packages are:

- Low profile and small footprint
- Enhanced thermal performance
- Excellent board-level reliability

Wire-Bond Packages

Wire-bond packages meet the demands required by miniaturization while offering improved performance. Applications for wire-bond packages are targeted to portable and consumer products where board space is of utmost importance, miniaturization is a key requirement, and power consumption/dissipation must be low. By employing Zynq-7000 AP SoC wire-bond packages, system designers can dramatically reduce board area requirements. Xilinx wire-bond packages are rigid BT-based substrates (see Figure 5-3).

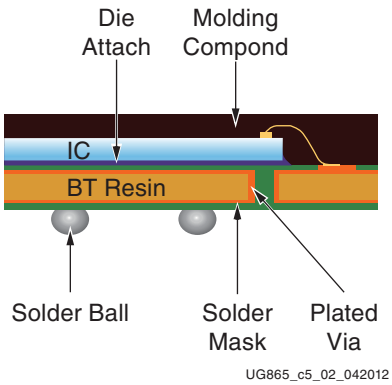


Figure 5-3: **Rigid BT-Based Substrate Wire-Bond Packages**

The key features/advantages of wire-bond packages are:

- An extremely small form factor which significantly reduces board area requirements for portable and wireless designs and PC add-in card applications.
- Lower inductance and lower capacitance
- The absence of thin, fragile leads found on other small package types
- A very thin, light-weight package

Flip-Chip Packages

For larger Zynq-7000 AP SoC devices, Xilinx offers the flip-chip BGA packages, which present a low thermal path. These packages incorporate a heat spreader with additional thermal interface material (TIM), as shown in Figure 5-4.

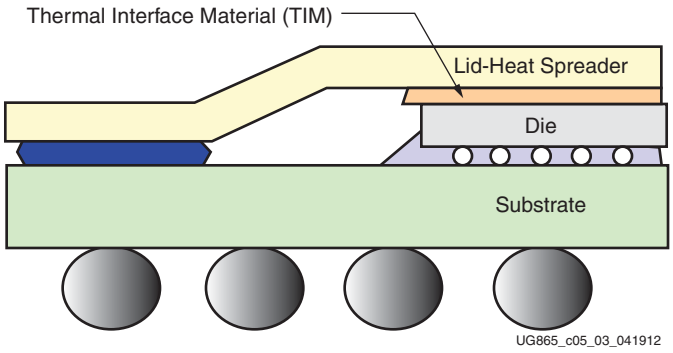


Figure 5-4: **Heat Spreader with Thermal Interface Material**

Materials with better thermal conductivity and consistent process applications deliver low thermal resistance to the heat spreader. A parallel effort to ensure optimized package electrical return paths produces the added benefit of enhanced power and ground plane arrangement in the packages. A boost in copper density on the planes improves the overall thermal conductivity through the laminate. In addition, the extra dense and distributed via fields in the package increase the vertical thermal conductivity.

System Level Heat Sink Solutions

To complete a comprehensive thermal management strategy, an overall thermal budget that includes custom or OEM heat sink solutions depends on the physical and mechanical constraints of the system. A heat-sink solution, managed by the system-level designer, should be tailored to the design and specific system constraints. This includes understanding the inherent device capabilities for delivering heat to the surface.

Thermal Interface Material

When installing heat sinks for Zynq-7000 AP SoCs, a suitable thermal interface material (TIM) must be used. This thermal material significantly aids the transfer of heat from the component to the heat sink.

For lidless flip-chip BGAs, the surface of the silicon contacts the heat sink. For lidded flip-chip BGAs, the lid contacts the heat sink. The surface size of the lidless flip-chip BGA and lidded flip-chip BGAs are different. Xilinx recommends a different type of thermal material for long-term use with each type of flip-chip BGAs package.

Thermal interface material is needed because even the largest heat sink and fan cannot effectively cool an Zynq-7000 AP SoC unless there is good physical contact between the base of the heat sink and the top of the Zynq-7000 AP SoC. The surfaces of both the heat sink and the Zynq-7000 AP SoC silicon are not absolutely smooth. This surface roughness is observed when examined at a microscopic level. Because surface roughness reduces the effective contact area, attaching a heat sink without a thermal interface material is not sufficient due to inadequate surface contact.

A thermal interface material such as phase-change material, thermal grease, or thermal pads fills these gaps and allows effective transference of heat between the Zynq-7000 AP SoC die and the heat sink.

The selection of the thermal interface (TIM) between the package and the thermal management solution is critical to ensure the lowest thermal contact resistance. Therefore, the following parameters must be considered.

1. The flatness of the lid and the flatness of the contact surface of the thermal solution.
2. The applied pressure of the thermal solution on the package, which must be within the allowable maximum pressure that can be applied on the package.
3. The total thermal contact of the thermal interface material. This value is determined based on the parameters in step 1 and step 2, which are published in the data sheet of the thermal interface supplier.

Types of TIM

There are many type of TIM available for sale. The most commonly used thermal interface materials are listed.

- Thermal grease
- Thermal pads
- Phase change material
- Thermal paste

- Thermal adhesives
- Thermal tape

Guidelines for Thermal Interface Materials

Five factors affect the choice, use, and performance of the interface material used between the processor and the heat sink:

- Thermal Conductivity of the Material
- Electrical Conductivity of the Material
- Spreading Characteristics of the Material
- Long-Term Stability and Reliability of the Material
- Ease of Application
- Applied Pressure from Heat Sink to the Package via Thermal Interface Materials

Thermal Conductivity of the Material

Thermal conductivity is the quantified ability of any material to transfer heat. The thermal conductivity of the interface material has a significant impact on its thermal performance. The higher the thermal conductivity, the more efficient the material is at transferring heat. Materials that have a lower thermal conductivity are less efficient at transferring heat, causing a higher temperature differential to exist across the interface. To overcome this less efficient heat transfer, a better cooling solution (typically, a more costly solution) must be used to achieve the desired heat dissipation.

Electrical Conductivity of the Material

Some metal-based TIM compounds are electrically conductive. Ceramic-based compounds are typically not electrically conductive. Manufacturers produce metal-based compounds with low-electrical conductivity, but some of these materials are not completely electrically inert. Metal-based thermal compounds are not hazardous to the Zynq-7000 AP SoC die itself, but other elements on the Zynq-7000 AP SoC or motherboard can be at risk if they become contaminated by the compound. For this reason, Xilinx does not recommend the use of electrically conductive thermal interface material.

Spreading Characteristics of the Material

The spreading characteristics of the thermal interface material determines its ability, under the pressure of the mounted heat sink, to spread and fill in or eliminate the air gaps between the Zynq-7000 AP SoC and the heat sink. Because air is a very poor thermal conductor, the more completely the interface material fills the gaps, the greater the heat transference.

Long-Term Stability and Reliability of the Material

The long-term stability and reliability of the thermal interface material is described as the ability to provide a sufficient thermal conductance even after an extended time or extensive. Low-quality compounds can harden or leak out over time (the pump-out effect), leading to overheating or premature failure of the Zynq-7000 AP SoC. High-quality compounds provide a stable and reliable thermal interface material throughout the lifetime of the device. Thermal greases with higher viscosities are typically more resistant to pump out effects on lidless devices.

Ease of Application

A spreadable thermal grease requires the surface mount supplier to carefully use the appropriate amount of material. Too much or too little material can cause problems. The thermal pad is a fixed size and is therefore easier to apply in a consistent manner.

Applied Pressure from Heat Sink to the Package via Thermal Interface Materials

RECOMMENDED: *Xilinx recommends that the applied pressure on the package be in the range of 20 to 40 PSI for optimum performance of the thermal interface material (TIM) between the package and the heat sink. Thermocouples should not be present between the package and the heat sink, as their presence will degrade the thermal contact and result in incorrect thermal measurements. The best practice is to select the appropriate pressure (in the 20 to 40 PSI range) for the optimum thermal contact performance between the package and the thermal system solution, and the mechanical integrity of the package (with the thermal solution to pass all mechanical stress and vibration qualification tests).*

RECOMMENDED: *Xilinx recommends using dynamic mounting around the four corners of the device package. On the PCB, use a bracket clip as part of the heat sink attachment to provide mechanical package support. See Figure 5-5.*

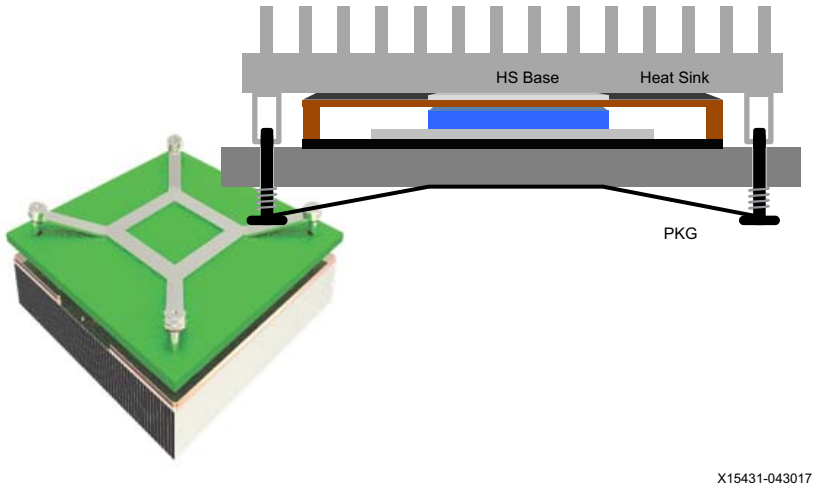


Figure 5-5: **Dynamic Mounting and Bracket Clips on Heat Sink Attachment**

Heat Sink Removal Procedure

The heat spreader on the package provides mechanical protection for the die and serves as the primary heat dissipation path. It is attached with an epoxy adhesive to provide the necessary adhesion strength to hold the package together. For an application in which an external heat sink subjects the lid adhesion joint to continuous tension or shear, extra support might be required.

In addition, if the removal of an attached external heat sink subjects the joint to tension, torque, or shear, care should be exercised to ensure that the lid itself does not come off. In such cases, it has been found useful to use a small metal blade or metal wire to break the lid to heat sink joint from the corners and carefully pry the heat sink off. The initial cut should reach far in enough so that the blade has leverage to exert upward pressure against the heat sink. Contact the heat sink and heat sink adhesive manufacturer for more specific recommendations on heat sink removal.

Soldering Guidelines

To implement and control the production of surface-mount assemblies, the dynamics of the Pb-free solder reflow process and how each element of the process is related to the end result must be thoroughly understood.

RECOMMENDED: *Xilinx recommends that customers qualify their custom PCB assembly processes using package samples.*

The primary phases of the reflow process are:

- Melting the particles in the solder paste
- Wetting the surfaces to be joined
- Solidifying the solder into a strong metallurgical bond

The peak reflow temperature of a plastic surface-mount component (PSMC) body should not be more than 250°C maximum (260°C for dry rework only) for Pb-free packages (220°C for eutectic packages) and is size dependent. For multiple BGAs in a single board and because of surrounding component differences, Xilinx recommends checking all BGA sites for varying temperatures.

The infrared reflow (IR) process is strongly dependent on equipment and loading. Components might overheat due to lack of thermal constraints. Unbalanced loading can lead to significant temperature variation on the board. These guidelines are intended to assist users in avoiding damage to the components; the actual profile should be determined by those using these guidelines. For complete information on package moisture / reflow classification and package reflow conditions, refer to the Joint IPC/JEDEC Standard J-STD-020C.

Sn/Pb Reflow Soldering

Figure 5-6 shows typical conditions for solder reflow processing of Sn/Pb soldering using IR/convection. Both IR and convection furnaces are used for BGA assembly. The moisture sensitivity of PSMCs must be verified prior to surface-mount flow.

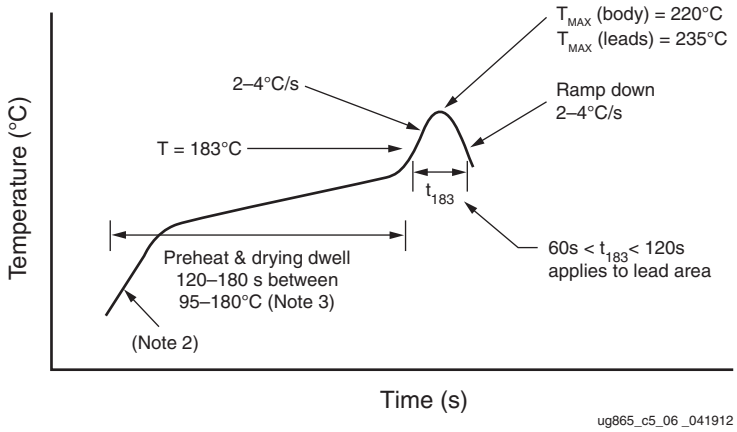


Figure 5-6: **Typical Conditions for IR Reflow Soldering of Sn/Pb Solder**

Notes for Figure 5-6:

1. Maximum temperature range = 220°C (body). Minimum temperature range before 205°C (leads/balls).
2. Preheat drying transition rate 2–4°C/s

3. Preheat dwell 95–180°C for 120–180 seconds
4. IR reflow must be performed on dry packages

Pb-Free Reflow Soldering

Xilinx uses SnAgCu solder balls for BGA packages. In addition, suitable material are qualified for the higher reflow temperatures (250°C maximum, 260°C for dry rework only) required by Pb-free soldering processes.

Xilinx does not recommend soldering SnAgCu BGA packages with SnPb solder paste using a Sn/Pb soldering process. Traditional Sn/Pb soldering processes have a peak reflow temperature of 220°C. At this temperature range, the SnAgCu BGA solder balls do not properly melt and wet to the soldering surfaces. As a result, reliability and assembly yields can be compromised.

The optimal profile must take into account the solder paste/flux used, the size of the board, the density of the components on the board, and the mix between large components and smaller, lighter components. Profiles should be established for all new board designs using thermocouples at multiple locations on the component. In addition, if there is a mixture of devices on the board, then the profile should be checked at various locations on the board. Ensure that the minimum reflow temperature is reached to reflow the larger components and at the same time, the temperature does not exceed the threshold temperature that might damage the smaller, heat sensitive components.

Table 5-2 and Figure 5-7 provide guidelines for profiling Pb-free solder reflow.

In general, a gradual, linear ramp into a spike has been shown by various sources to be the optimal reflow profile for Pb-free solders (Figure 5-7). SAC305 alloy reaches full liquidus temperature at 235°C. When profiling, identify the possible locations of the coldest solder joints and ensure that those solder joints reach a minimum peak temperature of 235°C for at least 10 seconds. It might not be necessary to ramp to peak temperatures of 260°C and above. Reflowing at high peak temperatures of 260°C and above can damage the heat sensitive components and cause the board to warp. Users should reference the latest IPC/JEDEC J-STD-020 standard for the allowable peak temperature on the component body. The allowable peak temperature on the component body is dependent on the size of the component. Refer to Table 5-2 for peak package reflow body temperature information. In any case, use a reflow profile with the lowest peak temperature possible.

Table 5-2: **Pb-Free Reflow Soldering Guidelines**

Profile Feature	Convection, IR/Convection
Ramp-up rate	2°C/s maximum
Preheat Temperature 150°–200°C	60–120 seconds
Temperature maintained above 217°C	60–150 seconds (60–90 seconds typical)
Time within 5°C of actual peak temperature	30 seconds maximum

Table 5-2: **Pb-Free Reflow Soldering Guidelines *(Cont'd)***

Profile Feature	Convection, IR/Convection
Peak Temperature (lead/ball)	235°C minimum, 245°C typical (depends on solder paste, board size, component mixture)
Peak Temperature (body)	245°C–250°C, package body size dependent (reference Table 5-3)
Ramp-down Rate	2°C/s maximum
Time 25°C to Peak Temperature	3.5 minutes minimum, 5.0 minutes typical, 8 minutes maximum

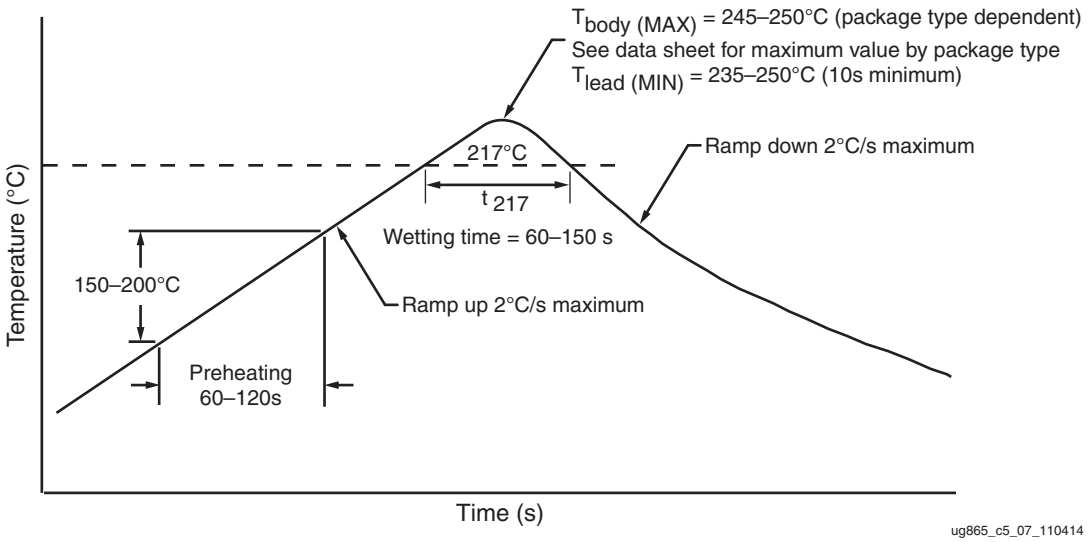


Figure 5-7: **Typical Conditions for Pb-Free Reflow Soldering**

Table 5-3: **Peak Package Reflow Body Temperature for Xilinx Pb-Free Packages (Based on J-STD-020 Standard)[(1)]**

Package		Peak Package Reflow Body Temperature	JEDEC Moisture Sensitivity Level (MSL)
BGA			
Flip-Chip	FBG484/FBV484, FBG676/FBV676, FFG676/FFV676, SBG485/SBV485	250°C	4
	FFG900/FFV900, FFG1156/FFV1156	245°C	
	RB484, RF676/RFG676, RF900, RF1156	225°C	
Wire-Bond	CLG225, CLG400, CLG484	260°C	3

Notes:

1. See the specific Zynq-7000 AP SoC data sheet [Ref 4][Ref 5].

For sophisticated boards with a substantial mix of large and small components, it is critical to minimize the DT across the board (<10°C) to minimize board warpage and thus, attain higher assembly yields. Minimizing the DT is accomplished by using a slower rate in the warm-up and preheating stages. Xilinx recommends a heating rate of less than 1°C/s during the preheating and soaking stages, in combination with a heating rate of not more than 2°C/s throughout the rest of the profile.

It is also important to minimize the temperature gradient on the component, between top surface and bottom side, especially during the cooling down phase. The key is to optimize cooling while maintaining a minimal temperature differential between the top surface of the package and the solder joint area. The temperature differential between the top surface of the component and the solder balls should be maintained at less than 7°C during the critical region of the cooling phase of the reflow process. This critical region is in the part of the cooling phase where the balls are not completely solidified to the board yet, usually between the 200°C–217°C range. To efficiently cool the parts, divide the cooling section into multiple zones, with each zone operating at different temperatures.

Post Reflow/Cleaning/Washing

Many PCB assembly subcontractors use a no-clean process in which no post-assembly washing is required. Although a no-clean process is recommended, if cleaning is required, Xilinx recommends a water-soluble paste and a washer using a deionized-water. Baking after the water wash is recommended to prevent fluid accumulation.

Cleaning solutions or solvents are not recommended because some solutions contain chemicals that can compromise the lid adhesive, thermal compound, or components inside the package.

Conformal Coating

Xilinx has no information about the reliability of flip-chip BGA packages on a board after exposure to conformal coating. Any process using conformal coating should be qualified for the specific use case to cover the materials and process steps.

RECOMMENDED: *When a conformal coating is required, Parylene-based material should be used to avoid potential risk of weakening the lid adhesive used in Xilinx packages.*

References

The following websites contain additional information on heat management and contact information.

- Aavid: www.aavidthermalloy.com
- Wakefield: www.wakefield-vette.com
- Advanced Thermal Solutions: www.qats.com
- CTS: www.ctscorp.com
- Radian Thermal Products: www.radianheatsinks.com
- Thermo Cool: www.thermocoolcorp.com

Refer to the following websites for interface material sources:

- Henkel: www.henkel.com
- Bergquist Company: www.bergquistcompany.com
- AOS Thermal Compound: www.aosco.com
- Chometrics: www.chomerics.com
- Kester: www.kester.com

Refer to the following websites for CFD tools Xilinx supports with thermal models.

- Mentor: Flotherm www.mentor.com/products/mechanical/flomerics
- ANSYS Icepak: www.ansys.com

Package Marking

Marking

All Zynq-7000 AP SoC devices have package top-markings similar to the examples shown in Figure 6-1 and explained in Table 6-1.

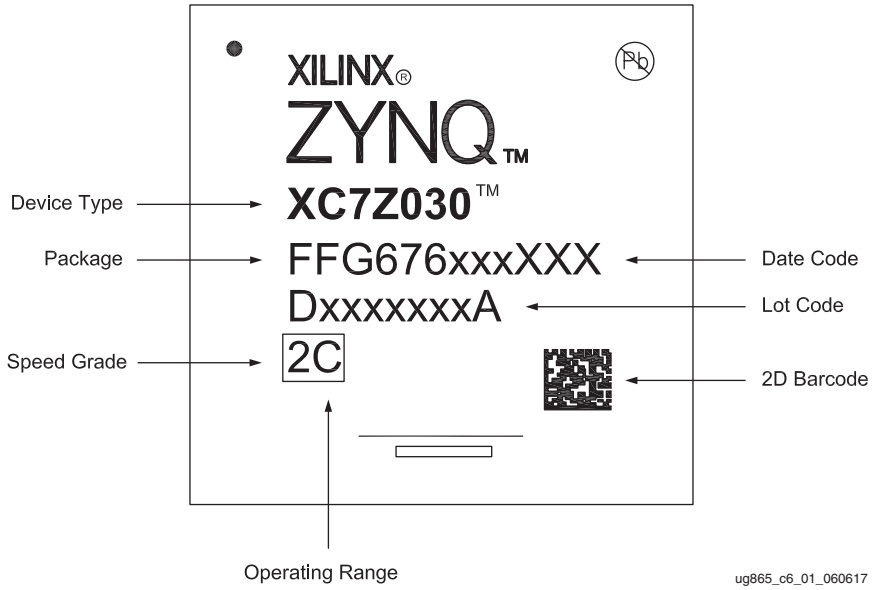


Figure 6-1: **Zynq-7000 AP SoC Device Package Marking**

Table 6-1: **Xilinx Device Marking Definition—Example**

Item	Definition
Xilinx Logo	Xilinx logo, Xilinx name with trademark, and trademark-registered status.
Pb-free Character	For FFG, FBG, or SBG packages, a Pb-free character is marked in the upper right corner of the device to denote that the device is manufactured using a lead-free material set as described in *Cross-ship of Lead-free Bump and Substrates in Lead-free (FFG/FBG/SBG) Packages* (XCN16022) [Ref 14].
Family Brand Logo	Device family name with trademark and trademark-registered status. This line is optional and could appear blank.
1st Line	Device type.

Table 6-1: **Xilinx Device Marking Definition—Example *(Cont'd)***

Item	Definition	
2nd Line	Package code, circuit design revision, the location code for the wafer fab, the geometry code, and date code. A G (or V) in the third letter of a package code indicates a Pb-free RoHS compliant package. For more details on Xilinx Pb-Free and RoHS Compliant Products, see: www.xilinx.com/pbfree.	
3rd Line	Ten alphanumeric characters for Assembly, Lot, and Step information. The last digit is usually an A or an M if a stepping version does not exist.	
4th Line	When marked, this line describes the device speed grade and temperature range. For more information on the ordering codes, see the *Zynq-7000 All Programmable SoC Overview* (DS190) [Ref 13]. Other variations for the 4th line:	
	2C xxxx	The xxxx indicates the SCD for the device. An SCD is a special ordering code that is not always marked in the device top mark.
	2C ES	The ES indicates an Engineering Sample.
	This line is not marked on some devices. Refer to the bar code for device speed grade and temperature range information.	
Bar Code	A device-specific bar code is marked on each device. Refer to the *FAQ: Top Marking Change for 7 Series, UltraScale, and UltraScale+ Products* (XTP424) [Ref 15].	

Packing and Shipping

Introduction

The Zynq-7000 AP SoCs are packed in trays. Trays are used to pack most Xilinx surface-mount devices since they provide excellent protection from mechanical damage. In addition, they are manufactured using anti-static material to provide limited protection against ESD damage and can withstand a bake temperature of 125°C. The maximum operating temperature is 140°C. Table 7-1 lists the maximum number of devices per tray and in one internal box.

Table 7-1: **Standard Device Counts per Tray and Box**

Package	Maximum Number of Devices Per Tray	Maximum Number of Devices In One Internal Box
CLG225	160	800
CLG400	90	450
CLG484	84	420
CLG485	84	420
SBG485 (SBV485)	84	420
FBG484 (FBV484)	60	300
FBG676 (FBV676)	40	200
FFG676 (FFV676)	40	200
FFG900 (FFV900)	27	135
FFG1156 (FFV1156)	24	120
RB484	60	300
RF676 (RFG676)	40	200
RF900	27	135
RF1156	24	120

Recommended PCB Design Rules

BGA Packages

Xilinx provides the diameter of a land pad on the package side. This information is required prior to the start of the board layout so the board pads can be designed to match the component-side land geometry. The typical values of these land pads are described in Figure A-1 and summarized in Table A-1 for both 0.8 mm and 1.0 mm pitch packages. For Xilinx BGA packages, non-solder mask defined (NSMD) pads on the board are suggested to allow a clearance between the land metal (diameter L) and the solder mask opening (diameter M) as shown in Figure A-1. An example of an NSMD PCB pad solder joint is shown in Figure A-2. It is recommended to have the board land pad diameter with a 1:1 ratio to the package solder mask defined (SMD) pad for improved board level reliability. The space between the NSMD pad and the solder mask as well as the actual signal trace widths depend on the capability of the PCB vendor. The cost of the PCB is higher when the line width and spaces are smaller

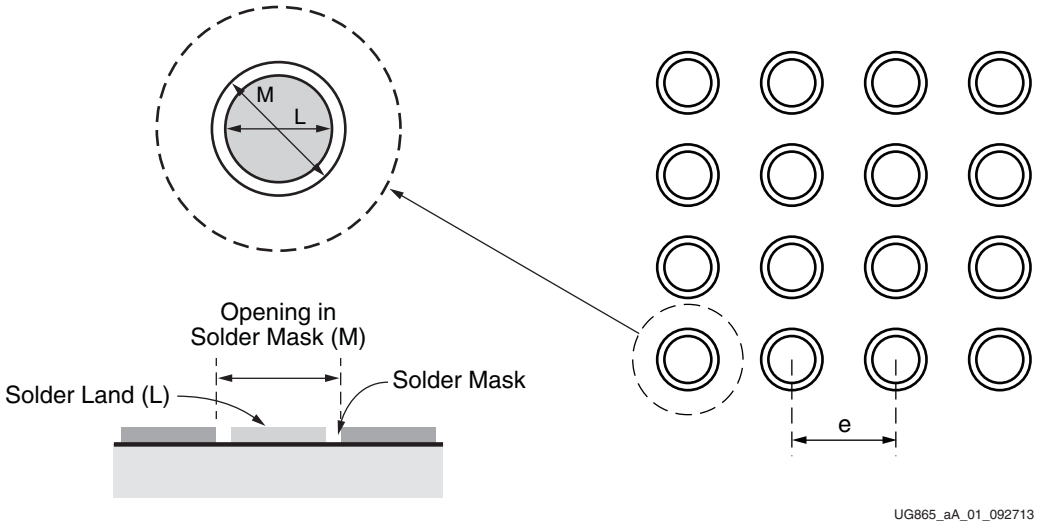


Figure A-1: **Suggested Board Layout of Soldered Pads for BGA Packages**

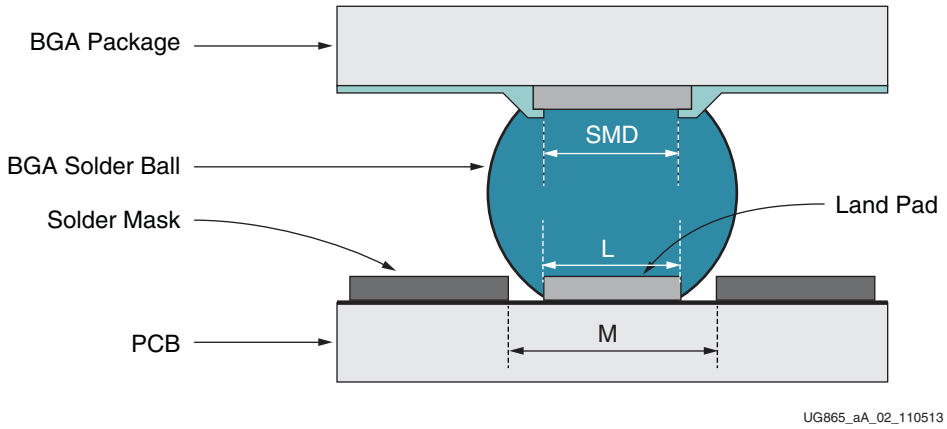


Figure A-2: **Example of an NSMD PCB Pad Solder Joint**

Table A-1: **BGA Package Design Rules**

Packages	**0.8 mm Pitch**	**1.0 mm Pitch**
	SB/SBG/SBV, CL/CLG	**FF/FFG/FFV, FB/FBG/FBV, RF/RFG**
Design Rule	**Dimensions in mm (mils)**	
Package land pad opening (SMD)	0.40 mm (15.7 mils)	0.53 mm (20.9 mils)
Maximum PCB solder land (L) diameter	0.40 mm (15.7 mils)	0.53 mm (20.9 mils)
Opening in PCB solder mask (M) diameter	0.50 mm (19.7 mils)	0.63 mm (24.8 mils)
Solder ball land pitch (e)	0.80 mm (31.5 mils)	1.00 mm (39.4 mils)

Notes:

1. Controlling dimension in mm.

Heat Sink Guidelines for Lidless Flip-Chip Packages

Heat Sink Attachments for Lidless Flip-chip BGA (FB/FBG/FBV)

Heat sinks can be attached to the package in multiple ways. For heat to dissipate effectively, the advantages and disadvantages of each heat sink attachment method must be considered. Factors influencing the selection of the heat sink attachment method include the package type, contact area of the heat source, and the heat sink type.

Silicon and Decoupling Capacitors Height Consideration

When designing heat sink attachments for lidless flip-chip BGA packages, the height of the die above the substrate and also the height of decoupling capacitors must be considered (Figure B-1). This is to prevent electrical shorting between the heat sink (metal) and the decoupling capacitors.

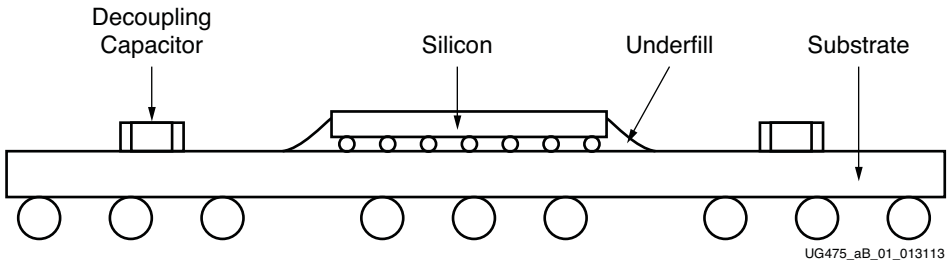


Figure B-1: **Cross Section of Lidless Flip-chip BGA**

Types of Heat Sink Attachments

There are six main methods for heat sink attachment. Table B-1 lists their advantages and disadvantages.

- Thermal tape
- Thermally conductive adhesive or glue
- Wire form Z-clips
- Plastic clip-ons
- Threaded stand-offs (PEMs) and compression springs
- Push-pins and compression springs

Table B-1: **Heat Sink Attachment Methods**

Attachment Method	Advantages	Disadvantages
Thermal tape	• Generally easy to attach and is inexpensive. • Lowest cost approach for aluminum heat sink attachment. • No additional space required on the PCB.	• The surfaces of the heat sink and the chip must be very clean to allow the tape to bond correctly. • Because of the small contact area, the tape might not provide sufficient bond strength. • Tape is a moderate to low thermal conductor that could affect the thermal performance.
Thermally conductive adhesive or glue	• Outstanding mechanical adhesion. • Fairly inexpensive, costs a little more than tape. • No additional space required on the PCB.	• Adhesive application process is challenging and it is difficult to control the amount of adhesive to use. • Difficult to rework. • Because of the small contact area, the adhesive might not provide sufficient bond strength.
Wire form Z-clips	• It provides a strong and secure mechanical attachment. In environments that require shock and vibration testing, this type of strong mechanical attachment is necessary. • Easy to apply and remove. Does not cause the semiconductors to be destroyed (epoxy and occasionally tape can destroy the device). • It applies a preload onto the thermal interface material (TIM). Pre-loads actually improve thermal performance.	• Requires additional space on the PCB for anchor locations.

Table B-1: **Heat Sink Attachment Methods *(Cont'd)***

Attachment Method	Advantages	Disadvantages
Plastic clip-ons	• Suitable for designs where space on the PCB is limited. • Easy to rework by allowing heat sinks to be easily removed and reapplied without damaging the PCB board. • Can provide a strong enough mechanical attachment to pass shock and vibration test.	• Needs a keep out area around the silicon devices to use the clip. • Caution is required when installing or removing clip-ons because localized stress can damage the solder balls or chip substrate.
Threaded stand-offs (PEMs) and compression springs	• Provides stable attachments to heat source and transfers load to the PCB, backing plate, or chassis. • Suitable for high mass heat sinks. • Allows for tight control over mounting force and load placed on chip and solder balls.	• Holes are required in the PCB taking valuable space that can be used for trace lines. • Tends to be expensive, especially since holes need to be drilled or predrilled onto the PCB board to use stand-offs.
Push-pins and compression springs	• Provides a stable attachment to a heat source and transfers load to the PCB. • Allows for tight control over mounting force and load placed on chip and solder balls.	• Requires additional space on the PCB for push-pin locations.

Heat Sink Attachment

Component Pick-up Tool Consideration

For pick-and-place machines to place lidless flip-chip BGAs onto PCBs, Xilinx recommends using soft tips or suction cups for the nozzles. This prevents chipping, scratching, or even cracking of the bare die (Figure B-2).

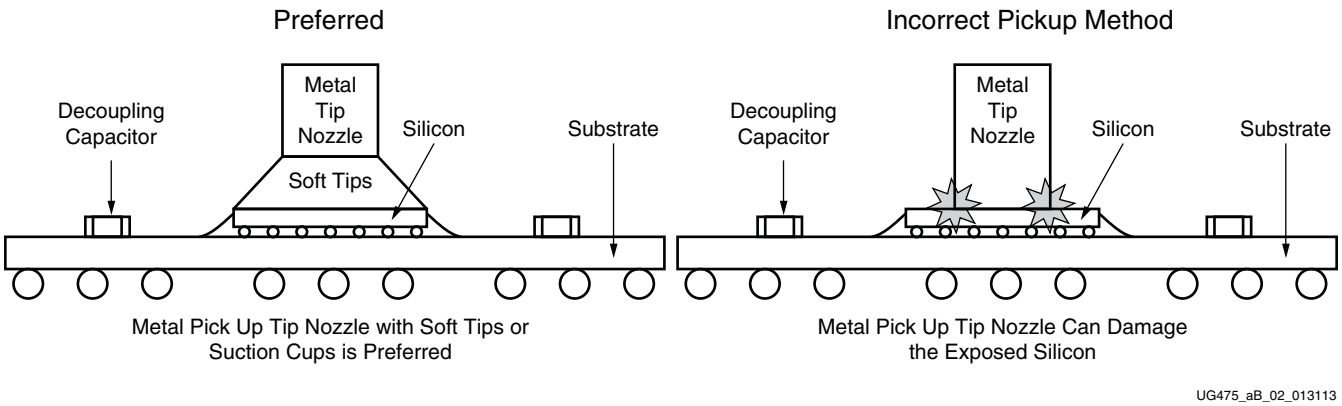


Figure B-2: **Recommended Method For Using Pick-up Tools**

Heat Sink Attachment Process Considerations

After the component is placed onto the PCBs, when attaching a heat sink to the lidless package, the factors in Table B-2 must be carefully considered (see Figure B-3).

Table B-2: **Heat Sink Attachment Considerations**

Consideration(s)	Effect(s)	Recommendation(s)
In heat sink attach process, what factors can cause damage to the expose die and passive capacitors?	• Uneven heat sink placement • Uneven TIM thickness • Uneven force applied when placing heat sink placement	• Even heat sink placement • Even TIM thickness • Even force applied when placing heat sink placement
Does the heat sink tilt or tip the post attachment?	Uneven heat sink placement will damage the silicon and can cause field failures.	• Careful handling not to contact the heat sink with the post attachment. • Use a fixture to hold the heat sink in place with post attachment until it is glued to the silicon.

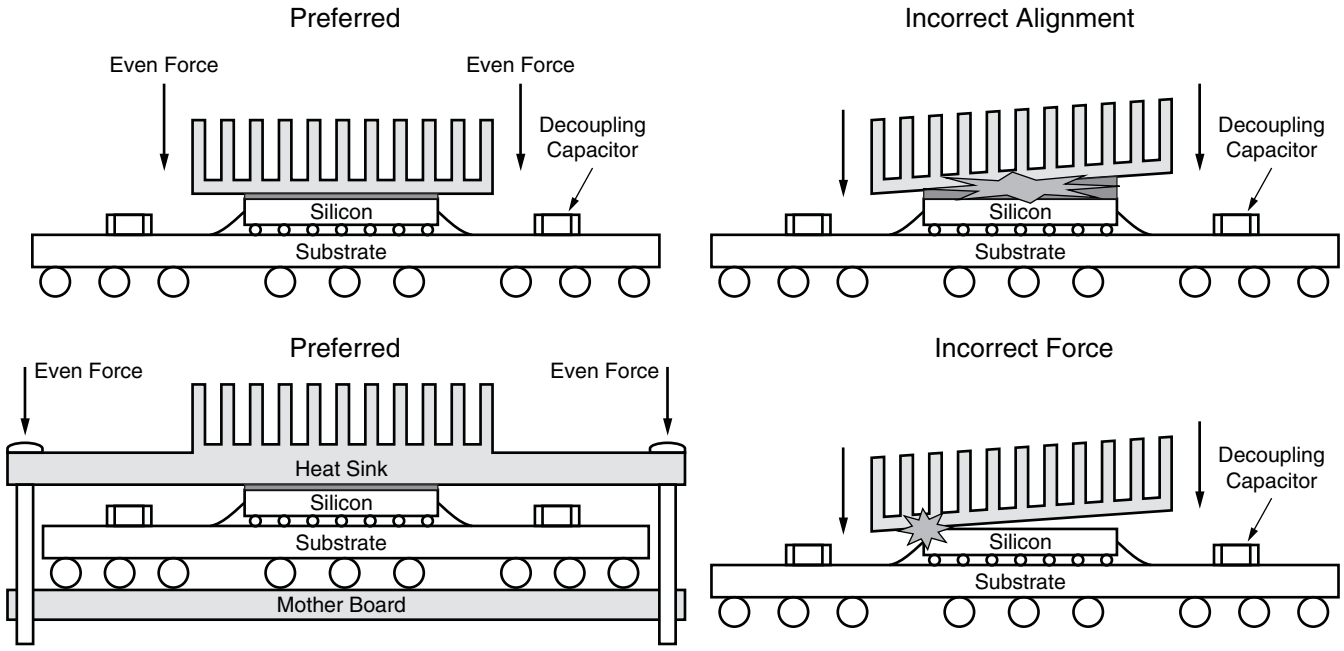


Figure B-3: **Recommended Application of Heat Sink**

Standard Heat Sink Attach Process with Thermal Conductive Adhesive

Prior to attaching the heat sink, the package needs be surface mounted on the motherboard.

1. Place the motherboard into a jig or a fixture to hold the motherboard steady to prevent any movement during the heat sink attachment process.
2. Thermoset material (electrically non-conductive) is applied over the backside surface of silicon in a pattern using automated dispensing equipment. Automated dispensers are often used to provide a stable process speed at a relatively low cost. The optimum dispensing pattern needs to be determined by the SMT supplier.

   Note: Minimal volume coverage of the backside of the silicon can result in non-optimum heat transfer.
3. The heat sink is placed on the backside of the silicon with a pick and place machine. A uniform pressure is applied over the heat sink to the backside of the silicon. As the heat sink is placed, the adhesive spreads to cover the backside silicon. A force transducer is normally used to measure and limit the placement force.
4. The epoxy is cured with heat at a defined time.

   Note: The epoxy curing temperature and time is based on manufacturer's specifications.

Standard Heat Sink Attach Process with Thermal Adhesive Tape

Prior to attaching the heat sink, the package needs be surface mounted on the motherboard.

1. Place the motherboard into a jig or a fixture to hold the motherboard steady to prevent any movement during the heat sink attachment process.
2. Thermal adhesive tape cut to the size of the heat sink is applied on the underside of the heat sink at a modest angle with the use of a squeegee rubber roller. Apply pressure to help reduce the possibility of air entrapment under the tape during application.
3. The heat sink is placed on the backside of the silicon with a pick and place machine. A uniform pressure is applied over the heat sink to the backside of the silicon. As the heat sink is placed, the thermal adhesive tape is glued to the backside of the silicon. A force transducer is normally used to measure and limit the placement force.
4. A uniform and constant pressure is applied uniformly over the heat sink and held for a defined time.

   Note: The thermal adhesive tape hold time is based on manufacturer's specifications.

Push-Pin and Shoulder Screw Heat Sink Attachment Process with Phase Change Material (PCM) Application

Prior to attaching the heat sink, the package needs be surface mounted on the motherboard.

1. Place the motherboard into a jig or a fixture to hold the motherboard steady to prevent any movement during the heat sink attachment process.

   Note: The jig or fixture needs to account for the push pin depth of the heat sink.

2. PCM tape, cut to the size of the heat sink, os applied on the underside of the heat sink at a modest angle with the use of a squeegee rubber roller. Apply pressure to help reduce the possibility of air entrapment under the tape during application.

3. Using the push-pin tool, heat sinks are applied over the packages ensuring a pin locking action with the PCB holes. The compression load from springs applies the appropriate mounting pressure required for proper thermal interface material performance.

   Note: Heat sinks must not tilt during installation. This process cannot be automated due to the mechanical locking action which requires manual handling. The PCB drill hole tolerances need to be close enough to eliminate any issues concerning the heat sink attachment.

Additional Resources

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

For a glossary of technical terms used in Xilinx documentation, see the Xilinx Glossary.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

References

These documents provide supplemental material useful with this guide:

1. UG585, *Zynq-7000 All Programmable SoC Technical Reference Manual*
2. UG933, *Zynq-7000 All Programmable SoC PCB Design Guide*
3. UG821, *Zynq-7000 All Programmable SoC Software Developer's Guide*
4. DS187, *Zynq-7000 All Programmable SoC (Z-7010, Z-7015, and Z-7020) Data Sheet: DC and AC Switching Characteristics*
5. DS191, *Zynq-7000 All Programmable SoC (Z-7030, Z-7035, Z-7045, and Z-7100) Data Sheet: DC and AC Switching Characteristics*
6. Zynq-7000 AP SoC package/device/pinout files are available at:

   www.xilinx.com/support/package-pinout-files/zynq7000-pkgs.html

7. UG586, *7 Series FPGAs Memory Interface Solutions User Guide*

8. UG471, *7 Series FPGAs SelectIO Resources User Guide*
9. UG480, *7 Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide*
10. UG470, *7 Series FPGAs Configuration User Guide*
11. UG476, *7 Series FPGAs GTX/GTH Transceivers User Guide*
12. UG482, *7 Series FPGAs GTP Transceivers User Guide*
13. DS190, *Zynq-7000 All Programmable SoC Overview*
14. XCN16022, *Cross-ship of Lead-free Bump and Substrates in Lead-free (FFG/FBG/SBG) Packages*
15. XTP424, *FAQ: Top Marking Change for 7 Series, UltraScale, and UltraScale+ Products*

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